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### *Solid-State Qubits: 3D Integration and Packaging*

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# 3D integration and packaging for solid-state qubits

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## I. QUANTUM PROCESSING WITH SOLID-STATE QUBITS

Quantum processing has the potential to transform the computing landscape by enabling efficient solutions to problems that are intractable on classical processors. The field was sparked by a suggestion by Richard Feynman in 1981 that a controllable quantum system can be used to simulate other quantum systems, such as materials and chemistry. In the 1990's, interest in quantum computing grew rapidly with the introduction of the first quantum “killer app”—the potential of a large-scale quantum processor to break certain types of public encryption schemes [1]. Recently, there has been growing consensus that myriad other fields besides data security could be impacted by the development of a quantum processor, including machine learning [2], many optimization problems [3], and Feynman's original idea of simulation of materials properties [4].

The fundamental logic element of a quantum computer is a quantum bit—termed “qubit.” Unlike a classical bit, which can take on one of two possible values, “0” or “1”, a quantum bit can be represented as a point on a sphere (the Bloch sphere), where the poles correspond to the classical 0 and 1 states, and all other points on the sphere represent coherent superpositions, or combinations, of these states. Single-qubit operations correspond to rotations on the Bloch sphere, and two-qubit operations can result in entanglement between different qubits. Quantum algorithms exploit quantum parallelism and quantum interference to efficiently solve certain problems that are classically intractable.

A qubit can be made from any two-level system, provided certain criteria are met. In 1996, David DiVincenzo published a paper listing the minimum requirements a candidate technology must have for building a quantum computer [5]. These have come to be known as the “DiVincenzo criteria.” They include scalability in the number of qubits, the ability to perform operations and measurements on qubits, and the requirement that the decoherence time, a measure of the lifetime of the quantum information, be much longer than the time to perform operations. The latter two requirements can be in conflict; ensuring that the lifetime of quantum information in the system is long requires *isolating* the qubit from its environment, while the need to operate on qubits requires some degree of coupling to the outside world.

There are several modalities currently being explored for quantum computing, including photonic, atomic, and solid-state systems. This article focuses on solid-state qubits, such as

those formed by an electron spin [6] or a superconducting circuit [7], which have transition frequencies in the GHz range. Because their frequencies are in this range, they are compatible with commercial-off-the-shelf (COTS) RF and microwave components. Solid-state qubits have the further advantage that they leverage decades of investment in fabrication by the semiconductor industry, which also provides a path towards fulfilling the scalability requirement.

Although convenient from the point of view of using COTS equipment, operation in the few-GHz range introduces the need for cooling the devices to avoid the qubit being inadvertently excited from “0” to “1” due to thermal effects. The equivalent temperature corresponding to 5 GHz is approximately  $T = \frac{hf}{k_B} = 250 \text{ mK}$ , where  $h$  is Planck’s constant and  $k_B$  is Boltzmann’s constant. It is necessary to be well below this temperature to avoid thermal excitation, typically  $\sim 10 \text{ mK}$ . This is well within the capabilities of dilution refrigerators, which operate by evaporative cooling of a mixture of two isotopes of helium. Thirty years ago, dilution refrigerators were highly specialized products, and operating them required cryogenic training and consumable liquid cryogens for the first stages of cooling. Today, commercial systems generally use pulse-tube coolers that run off wall-plug power. Automated gas handling systems have further transformed dilution refrigerators from specialized equipment to nearly push-button systems. However, understanding the limitations of operating in a cryogenic environment is still important. For example, dilution refrigerators are limited in the cooling power they can provide, and every cable that enters the fridge introduces a passive heat load, simply by being connected to room temperature. If resistive current-carrying wires are used, this can further introduce power that must be dissipated. Additionally, the differential thermal contraction of different materials must be considered when designing low-temperature apparatus, and samples must be properly heat sunk so that they can thermalize with the low-temperature stage of the refrigerator.

Packaging of solid-state qubits in a cryogenic environment introduces challenges due to the sensitivity of the qubits to the electromagnetic environment. For example, it has long been known that at low temperatures, disordered solids have defects that can be modeled as a collection of a large number of two-level systems (TLS) [8, 9]. Electrically-active TLS, such as those found in dielectric materials or at surfaces, can interact with a qubit’s electric field and provide a decay channel for the quantum information [10]. Therefore, it is important to make sure that the fraction of the qubit’s electric field that interacts with TLS is small.

Similarly, the fraction of the electric field that interacts with normal metal must be small to avoid resistive losses. Magnetic impurities can also impact qubit performance by introducing magnetic field noise, or “flux noise,” that can cause decoherence in superconducting qubits. Spurious modes in the packaging, or even on or within the qubit chips themselves, can impact qubit performance by providing a way for quantum information to leave the system in an uncontrolled manner. Worse, coupling to spurious modes can increase microwave crosstalk between qubits and introduce correlated errors, which are particularly hard to correct using quantum error correction schemes. Microwave crosstalk can also result in the control signal for one qubit shifting the energy levels of another qubit through the Stark shift, another source of decoherence.

Developing a packaging scheme that meets all of the requirements for operation of solid-state qubits in a cryogenic environment can be a formidable challenge. In this article, we discuss work being done in our group as well as in the broader community, focusing on the role of 3D integration and packaging in quantum processing with solid-state qubits. In sections II and III, we discuss the role of 3D integration in building arrays of qubits and controlling their microwave environment. While this discussion focuses on applications to superconducting qubits, we note here that the work is more generally relevant to any solid-state qubit operating at cryogenic temperatures since it is often desirable to use superconducting circuits for readout and control of any qubit in a dilution refrigerator. Sections IV and V focus on the challenges of routing signals from the chip to the output of a dilution refrigerator, and section VI discusses challenges and ideas for future systems with larger numbers of qubits.

## II. THE TYRANNY OF INTERCONNECTS

One of the advantages of solid state qubits is that they are amenable to fabrication on silicon wafers with industry-standard processes and tools. While this greatly simplifies fabrication, laterally addressing large numbers of qubits from the edge of a chip quickly becomes infeasible due to interconnect crowding. Just as the semiconductor and imaging industries moved to 3D integration to reduce latency, dissipate power more efficiently, and allow for heterogeneous integration, the solid-state qubit field is also looking to 3D integration to address arrays of coherent qubits, which are needed for some quantum error correction schemes

[11]. Solving the interconnect problem to address a 2D array requires “breaking the plane” to route wires past each other so they can access the interior qubits. This can be accomplished using either multi-layer fabrication processes or plane-breaking packaging schemes. In this section, we will discuss the former; the latter is covered in section IV.

One multi-layer fabrication method for routing traces past each other is the use of superconducting air bridges, using resist or dielectric material as scaffolding that is removed to leave a free-standing bridge [13]. These air bridges can also be used to tie sections of the ground plane together, improving microwave hygiene and reducing the probability of exciting spurious modes. Figure 1 shows images of air bridges fabricated at Lincoln Laboratory to connect ground planes and to route wires past each other. [12].

Another option that enables wires to cross is the use of flip chip integration to bond the qubit chip to another chip. We have used this method to demonstrate off-chip readout and control of a superconducting flux qubit, as shown in Figure 2. The left side of the figure shows the layout of a test chip with six superconducting qubits. Each of the qubits has a bias line that applies magnetic flux to the qubit loop, changing its energy, and each has a far-detuned quarter wave transmission line resonator that experiences a shift in resonance based on the qubit state and is used to read out the qubit state. The six readout resonators, which each have a slightly different resonance frequency, are coupled to a single transmission line to enable multiplexed readout. The right side of the figure shows the flip chip version of the same circuit, where the qubits and the control/readout circuitry are split into two different

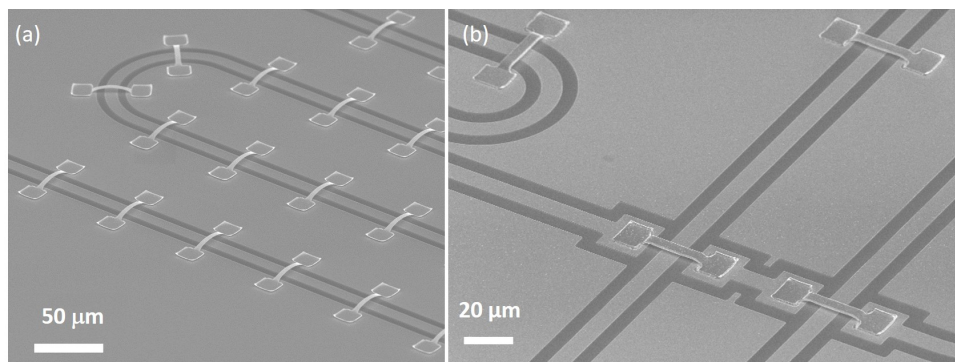


FIG. 1. Images of air bridges fabricated at MIT Lincoln Laboratory. In (a), the air bridges are used to connect the ground planes on two sides of a coplanar waveguide transmission line resonator, and in (b) the air bridges are used to route coplanar waveguide lines past each other [12].

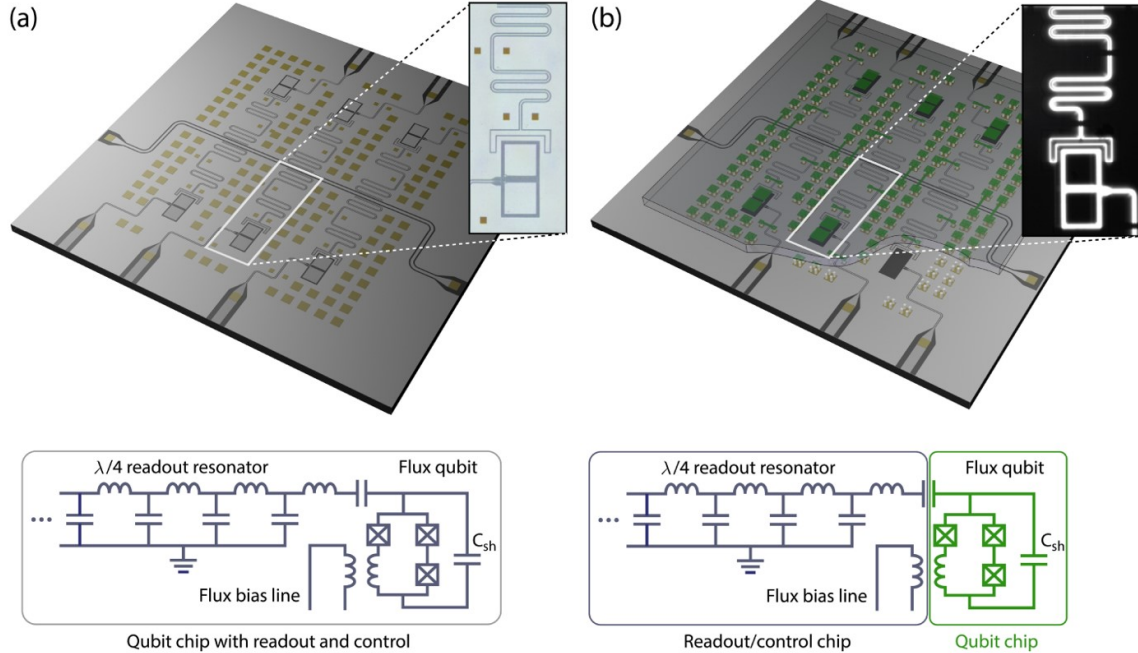


FIG. 2. Comparison of single-chip and flip-chip versions of a superconducting flux qubit. a) Single chip with 6 flux qubits, where each qubit is controlled and read out with on-chip elements. b) 3D integrated qubits, where a chip with six qubits is flipped onto and bonded to another chip with control and readout elements. Qubits on both chips had similar performance. Reprinted from [14].

chips. The qubits are on the top chip, which is attached to the bottom control/readout chip using thermocompression bonding of indium bumps. The bottom chip contains the bias lines, which couple inductively across the few- $\mu\text{m}$  gap between the chips, and readout resonators, which couple capacitively across the gap. An underbump metallization layer of Ti/Pt/Au provides a low-resistance galvanic path between the chips, which is used to connect the ground plane of the chips. We found that the single-chip qubits had nearly identical lifetimes compared to the flip-chip version, indicating that flip chip processing and bump bonding did not have a significant impact on qubit lifetimes of  $\approx 20 \mu\text{s}$  [14]. Other groups are pursuing flip chip integration, with recent demonstrations of a fully superconducting path between two bump-bonded chips [15, 16].

Although both flip chip integration and superconducting air bridges can be used to access the interior qubits of a 2D array, efficient wire routing requires more layers of metal. The typical method for doing this is to use a multi-layer process, where deposited dielectrics isolate wiring layers. Superconducting multilayer processing has been developed for classical digi-

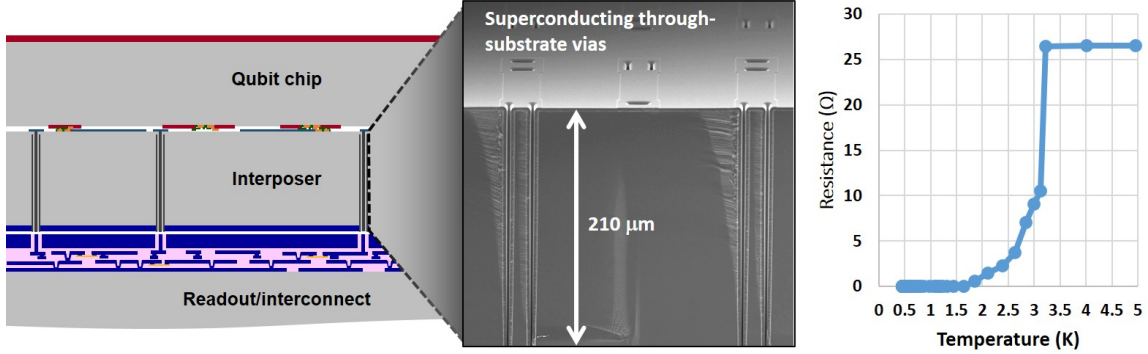


FIG. 3. Envisioned three-tier stack for control and readout of a 3D integrated quantum processor. The three chips are bonded together using indium bump bonds, and superconducting through-substrate vias provide connectivity between the qubit chip on the top and the readout/interconnect chip on the bottom. The inset shows a cross section of a chip with superconducting through-substrate vias. The graph on the right displays a measurement of via resistance as it is cooled through the superconducting transition temperature.

tal superconducting logic at commercial and government foundries [17, 18]. Unfortunately, the lossy dielectric materials generally associated with these processes are not compatible with low-loss superconducting circuits. As a result, simply constructing superconducting microwave circuits on top of a multilayer chip, or bump bonding a qubit chip to a multilayer chip in close proximity, can reduce the lifetime of a solid-state qubit. One approach to solve this problem is to develop multilayer superconducting wiring without lossy materials [19]. Another approach, which we are pursuing, is to separate the lossy multilayer chip from the qubit chip through the use of an interposer chip with superconducting through-substrate vias (TSVs), as shown in Figure 3 [14]. Several groups are developing superconducting TSVs for vertical signal delivery and for reducing spurious chip modes [20, 21].

Our approach to TSV fabrication focuses on the development of compact, high-aspect-ratio TSVs to enable high-density vertical wiring. We first use reactive ion etching to etch  $200\ \mu\text{m}$ -deep blind vias in a  $725\ \mu\text{m}$  thick,  $200\ \text{mm}$  diameter silicon wafer. After the vias have been etched, we deposit superconducting TiN on the wafer and line the TSVs using chemical vapor deposition. The planar metal is patterned and the wafer is then flipped and temporarily bonded to a carrier wafer. The TSVs are revealed by using chemical mechanical planarization to thin the wafer to  $200\ \mu\text{m}$ . Superconducting metal is deposited and patterned



on the revealed side of the TSV wafer, and the wafer is diced and the chips are debonded from the carrier. The resulting chip has superconducting metal on both sides, with connections between the top and bottom plane provided by compact ( $10\ \mu\text{m} \times 25\ \mu\text{m}$ ) superconducting TSVs. Figure 3 shows a scanning electron micrograph of a cross-sectioned TSV chip, showing the superconductor-lined TSVs and patterned metal on one side of the chip.

We have characterized the superconducting TSVs at DC and microwave frequencies. At DC frequencies, we perform 4-wire resistance measurements on test structures comprising many TSV links in series, connected to each other through alternating strips of metal on the top and bottom of the chip. These measurements indicate excellent yield; chains with as many as 3,200 TSV links in series have displayed a superconducting critical temperature of 2.5-3 Kelvin [22].

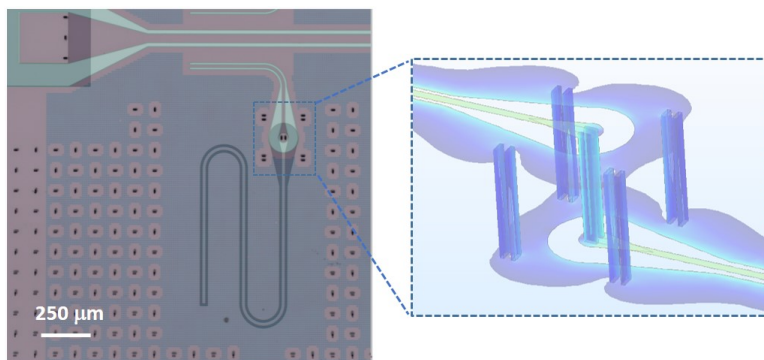


FIG. 4. Example of a shielded microwave TSV transition designed to minimize reflections. The main figure shows the top and bottom of a TSV chip overlaid, with the bottom image mirrored for ease of viewing. The structure shown is a quarter-wave coplanar waveguide transmission line resonator that is split between the top and bottom of the chip, with a microwave TSV transition connecting them. A pair of TSVs connect the center traces on either side of the chip, and four pairs of TSVs connect the ground planes. The inset shows the results of a simulation of the current flow in the transition.

At microwave frequencies, a single TSV connection in the signal line of a planar waveguide structure would introduce a significant impedance mismatch between high-frequency lines on either side of the chip, resulting in signal reflection and distortion. Therefore, it is essential to design a TSV transition that minimizes such mismatch and properly routes the return currents for microwave lines. The inset of Figure 4 shows one of the structures we have

designed to connect co-planar waveguide (cpw) transmission lines on two sides of a chip. A pair of TSVs provides a connection for the center trace of the cpw, and four pairs of TSVs connect the ground plane on either side of the chip. The cpw shape near the TSV transition is tailored to minimize reflections of microwave signals, and the simulated reflection at the transition is less than -30 dB.

In order to characterize the losses associated with the TSV transition, we incorporated the structure shown in the inset to Figure 4 into superconducting transmission line resonators. As shown in Figure 4, each resonator comprises two sections of transmission lines, one on the top of the chip and one on the bottom, with a TSV transition providing a connection between the two sections. Measuring the quality factor of the resonator can indicate if the TSV transition is introducing loss at microwave frequencies. In most microfabricated superconducting resonators, the quality factor at low power is limited by the presence of two-level systems at interfaces that interact with the electric field and constitute a loss mechanism [23]. The effect of these two-level systems is dependent on temperature and power, so it is essential to measure the quality factor at low temperatures and at a sufficiently low power that the mean photon number in the resonator is approximately unity, to reproduce the environment seen by the qubits. If we are interested in characterizing the loss associated with a particular component integrated into a resonator, such as a microwave TSV transition, shifting the location of the component relative to the voltage and current nodes of the resonator can provide useful insight; if the primary loss mechanism is resistive, it will have the biggest effect at the current anti-node, and if it is related to two-level systems, the effect will be largest at the voltage anti-node where the electric field is high. We have measured quality factors of more than 20 resonators of the type shown in Fig 4, with locations of the transition ranging from the position shown in the figure (near the current anti-node) to the voltage anti-node. In all cases, the quality factor ranged from 100,000 to 300,000, consistent with the intrinsic quality factors of planar transmission line resonators on each surface [24]. These results indicate that the TSVs do not introduce significant ohmic or TLS loss at microwave frequencies.

### III. USING 3D INTEGRATION TO TAILOR THE MICROWAVE ENVIRONMENT

In addition to solving the interconnect problem, 3D integration can also be used to tightly control the microwave environment surrounding the qubit to an unprecedented degree. The microwave environment surrounding the qubits and control/readout lines can influence the performance of a quantum processor because any mode that couples to the qubit can reduce the qubit lifetime and/or result in microwave crosstalk. Of course, some interaction with the outside world is needed in order to control and read out the qubits, and quantum circuit designers must carefully balance the need for control of the quantum system with the potential for adding loss channels.

Spurious modes that can impact performance include cavity resonances, quasi-lumped-element modes involving the inductance and capacitance between the chip and package grounds, and modes corresponding to undesired excitations of superconducting planar elements. Box modes can be excited in any cavity with metallized walls, at a frequency that depends on the shape and size of the cavity. In general, for packaged single-chip superconducting circuits on silicon chips, two of the dimensions are much larger than the third, so the lowest-frequency mode that is excited is the transverse magnetic TM<sub>110</sub> mode. If the dielectric in the cavity is air, a cavity with the largest dimensions 10 mm x 10 mm will have a resonant frequency of 22 GHz, while for a 10x10 mm silicon chip with  $\epsilon_r \approx 11.5$ , the lowest box mode frequency is 6 GHz. Within the qubit package, care must be taken to avoid large cavities that can host box modes, or the qubit must be shielded from them. Box modes in the chip can be mitigated by including an air-gap under the chip to increase the frequencies of the modes, but as chips get larger, eventually another approach must be used, such as the use of vias to decouple the frequency dependence of the chip box modes from the size of the chip [20].

The finite-impedance connections between the chip ground plane and the package ground are another source of spurious modes. Researchers have shown that the inductance of the ground plane wire bonds, when combined with the capacitance between the chip ground plane and the package ground plane, can result in resonances near qubit frequencies and significantly increase microwave crosstalk [25]. One method for reducing the impact of these modes is to reduce the capacitance between the chip ground plane and the package ground,

which can push the resonances higher than the frequency range of interest. This can be accomplished by selectively removing metal directly below the qubit chip [25], or by using TSVs to directly short out the capacitance. Similarly, flip chip bump bonds can be used instead of wire bonds to significantly reduce the inductance of the connection between the chip and package ground planes.

Finally, spurious modes can result from the excitation of alternate waveguide modes in the superconducting metal than the ones intended. For example, slotline modes can be excited on a coplanar waveguide if there is not a good connection between the groundplane on both sides of the signal trace, or if there are discontinuities in the ground plane. The probability of exciting these modes can be greatly reduced by forming a well-connected ground plane, which can be accomplished using superconducting bump bonds in a flip chip configuration [15], or by using superconducting air bridges [19].

In many cases, finite-element electromagnetic simulation software can be used to identify, determine the impact of, and mitigate the presence of spurious modes. For superconducting circuits, a technique called black-box quantization [27, 28] provides a useful framework for determining how spurious modes and coupling can impact qubit performance. Classical simulation software is first used to find the admittance that the qubit sees at microwave

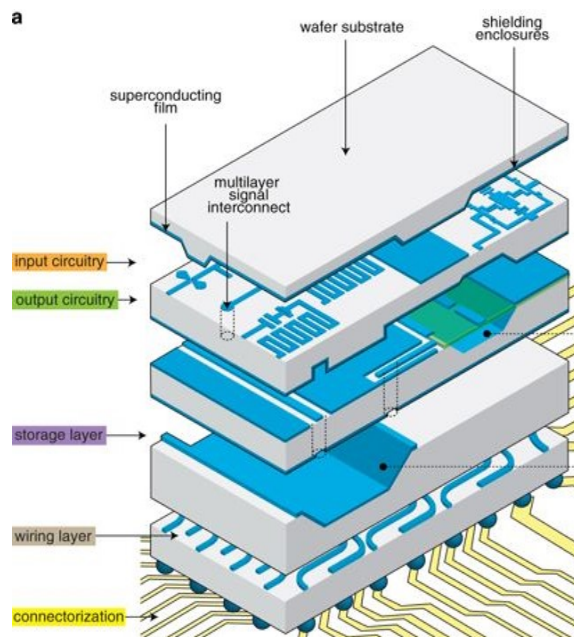


FIG. 5. Concept for a multilayer microwave circuit, reprinted from [26]. Wafers are micromachined and bonded together with superconducting materials to form shielding enclosures and circuitry.

frequencies. Foster's method or Brune synthesis [28] is then used to provide an equivalent lumped-element circuit that reproduces the results of the simulation, and those lumped elements can then be incorporated into the circuit model to determine the effect on the qubit.

Exciting recent work has focused on the use of 3D integration to build enclosures around qubits and components to shield them from unintended coupling to other components or modes. For example, researchers have created a micromachined superconducting “cap” that is bump bonded to a superconducting qubit chip to isolate the qubit from other elements in the circuit. The cap has a layer of sputtered aluminum lined with a continuous layer of thin molybdenum to prevent native oxidation of the aluminum, and indium bumps provide a connection between elements on the two chips [16]. In other work, researchers are looking at micromachined superconducting cavities not only for shielding, but also to store and manipulate quantum information. Figure 5 shows a concept for a multilayer microwave integrated quantum circuit (MMIQC) [26], which includes vertical interconnects, shielding enclosures, and high-Q storage cavities. Some elements of this concept, such as coupling superconducting qubits to high-Q micromachined cavities, have been demonstrated [29].

#### IV. GETTING SIGNALS OFF THE CHIP

Whether a single chip or a 3D-integrated chip is used, there must be a reliable interface between the silicon and a path that eventually leads out of the fridge to room temperature. This connection can be made either directly to the qubit chip or through a printed circuit board (PCB) or other interposer that can be interfaced with microwave connectors. The standard method is to wire bond between the edges of a silicon chip and a PCB. In some cases, the PCB may house components that are needed for qubit operation. For example, Figure 6 shows a schematic of a cryogenic package developed for solid-state qubits. The authors' modular platform, which includes 74 DC connections and 36 RF and microwave connections, comprises two PCBs: a simpler one that is wire-bonded directly to the qubit chip, and a more complex board that includes components such as bias tees and filters. With this system, the cost and complexity are mainly in the larger board, so a qubit chip can be permanently bonded to the smaller board [30].

Flip chip bump bonds can also be used to connect solid state qubits to a microwave

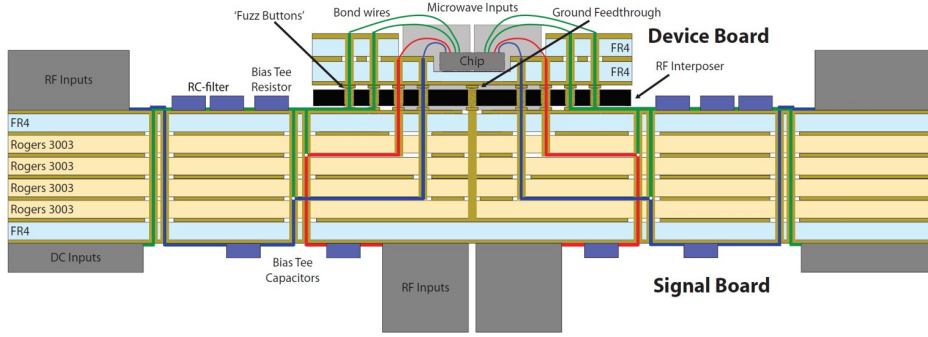


FIG. 6. Interconnect platform developed for controlling and reading out solid-state qubits. The qubit chip is bonded to a small device board, which is then connected to a more complex, reusable board through contact pins. Reprinted from [30]

interposer [31]. For example, we are investigating using indium or solder bumps to form the connection between the three-tier stack discussed in Section II and a PCB, as shown in Figure 7. As discussed in Section III, the use of bumps rather than wire bonds is expected to provide better impedance matching and reduce crosstalk. An important consideration is the coefficient of thermal expansion for the silicon chip and the microwave interposer, which should be adequately matched to ensure mechanical robustness with thermal cycling.

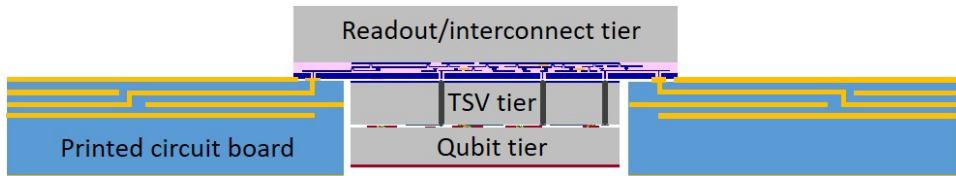


FIG. 7. Schematic of the three-tier stack shown in Figure 3 attached via flip chip to a microwave interposer. The readout and interconnect chip is larger than the other chips, allowing a peripheral connection to the microwave interposer. Depending on the density of wires, one or more rows of bumps can make a connection to buried striplines in the PCB.

Some researchers have noted that interfacing with a PCB or connectors offers another opportunity for “breaking the plane” to allow access to interior qubits in a 2D array. For example, the authors of Ref [32] use pogo pins to make contact between a PCB and an array of seven qubits on a silicon chip with an interior qubit that cannot be addressed laterally, and the authors of Ref [33, 34] use a novel double-sided coaxial line approach to capacitively

couple to qubits for control and read out. Researchers have also flipped a silicon chip with 13 qubits directly on top of a PCB, making contact by pushing the silicon chip against vias in the PCB signal lines [35]. Finally, a concept called the “quantum socket” uses custom spring-loaded micro-wires to make contact between pads on the silicon chip and standard microwave connectors [36].

These novel approaches greatly simplify testing and prototyping by shifting the wiring complexity to the PCB, where well-established techniques exist to route transmission lines within multiple layers. However, there are some drawbacks to approaches that require directly contacting to a qubit chip. First, though photolithographic techniques used on silicon chips generally can define very small features  $\approx 0.1 - 1 \mu m$ , printed circuit boards and pins have much larger features, typically  $> 100 \mu m$ . This larger feature size and the desire to avoid complicated alignment procedures pushes the required contact pad size on the qubit chip to a few hundred  $\mu m$ . Contact pads of this size limit the density of active components, and can lead to excess crosstalk. Furthermore, pins and PCBs generally contain dielectric layers that could lead to reductions in qubit coherence time, so care must be taken to spatially isolate the qubits from these materials. Finally, contact resistance is generally higher for contacts based on pressure rather than wire bonds or bump bonds. This is particularly a problem in schemes that involve directly contacting the qubit chip, since any resistive heating will be generated directly on the qubit chip.

Resistive heating within the interposer can also be an issue when the number of lines in a package becomes high enough. The use of superconducting materials on microwave interposers is of interest both to reduce heating and to improve signal quality. Research has shown that the use of superconducting materials can vastly reduce transients observed when applying fast control pulses to qubits [37].

## V. GETTING OUT OF THE FRIDGE

Now that we have discussed strategies for routing signals on and off of the qubit chip, we also need to consider how to get signals into and out of the dilution fridge. Fridge wiring is typically divided into two categories— RF and DC. The RF wiring is typically used to control and read out the qubits, while DC wiring can be used for qubit control and for powering active components inside the fridge, such as amplifiers and switches. Due to the

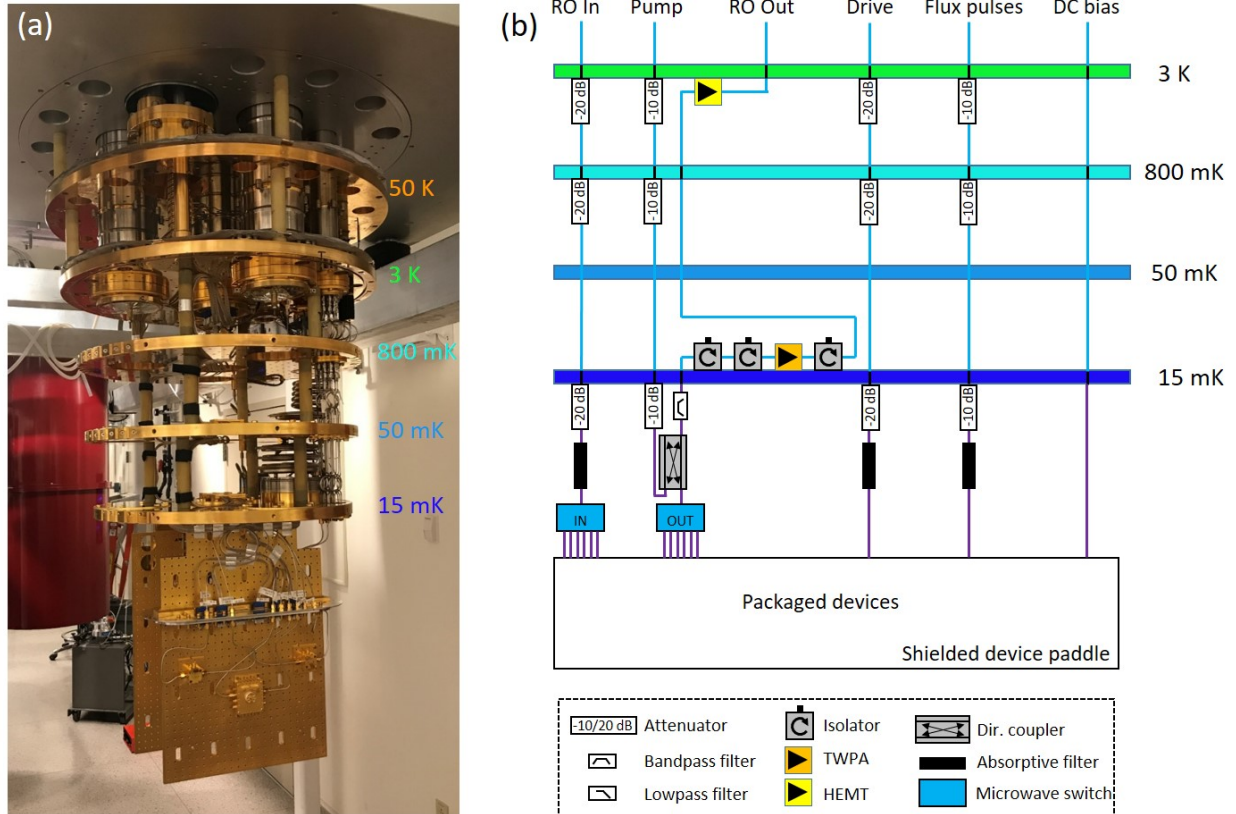


FIG. 8. Dilution fridge wiring for superconducting qubit experiments. (a) Photograph of a dilution refrigerator. Each circular plate is operated at a progressively lower temperature. (b) Example schematic of the internal fridge wiring for typical superconducting qubit experiments. Microwave cables are used for qubit readout, amplifier pump tones, qubit drive tones, and magnetic flux pulses.

cryogenic environment and the high sensitivity of the qubits to noise, several mechanical and electrical considerations must be taken into account when wiring a dilution fridge for qubit experiments.

As shown in Figure 8, the inside of a dilution fridge is composed of stages that are operated at progressively lower temperatures. In order for each stage to remain cold, it needs to be thermally isolated from the warmer stages above. The fridge wiring acts as a heat link between stages, creating a passive heat load that scales with the number of connections. Therefore, when scaling up to larger numbers of connections, careful attention must be paid to thermal engineering, as described in Ref [38]. For example, typically materials with low thermal conductivity are used, such as stainless steel and superconducting metals. It is also



important to minimize the active heat load from resistive losses in the DC lines by reducing contact resistances and using superconducting wires whenever possible.

While these mechanical wiring considerations affect the fridge temperature, electrical considerations can have a more direct impact on qubit performance. Because solid-state qubits are highly sensitive to noise, careful steps must be taken to protect the qubits from room temperature thermal noise and any added noise from the control electronics. This is achieved, in part, by applying low-pass filters to the DC lines and progressively attenuating the RF lines at several different temperature stages. In addition, IR absorbing shields and filters are often used at the coldest temperature stage to protect the qubits from radiation coming from the warmer stages [39, 40].

Finally, there are additional considerations that come into play when designing the microwave readout chain. Solid-state qubits are often read out through capacitively coupled microwave resonators. The resonators are designed to efficiently measure the qubit state when probed at very low powers, on the order of -110 dBm or lower. To achieve high fidelity readout, these small signals must then be amplified with as little added noise as possible. Most state-of-the-art readout chains use nearly-quantum-limited amplifiers, such as the traveling-wave parametric amplifier (TWPA) [41] at the lowest temperature stage and high-electron-mobility transistor (HEMT) amplifiers at the 3 Kelvin stage.

Looking forward, considerable engineering efforts are needed to scale up existing infrastructure to accommodate larger solid-state qubit processors. Existing approaches to fridge wiring will be difficult to extend beyond the scale of hundreds of qubits due to thermal and space constraints. Several alternative approaches are currently under consideration, including commercial multi-coax assemblies and superconducting flex-print [42, 43] and rigid-flex wiring [44]. There are also efforts underway to develop on-chip microwave isolators to replace existing bulky components made with magnetic materials [45, 46].

## VI. LOOKING TO THE FUTURE

As the number of qubits in a system gets larger, the brute force approach of generating control signals at room temperature and sending one or more lines into the cryostat for each qubit will no longer be feasible. It has been estimated [47] that this will occur at approximately 1,000 physical qubits. Several options exist for generating control signals at

cryogenic temperatures, including cryogenic CMOS and superconducting digital electronics such as single-flux-quantum-based (SFQ) circuits. Researchers have demonstrated the use of cryogenic CMOS [48] and SFQ [49, 50] circuits for readout and control of superconducting qubits. Figure 9 shows a circuit schematic from Ref [50] for an SFQ driver used for coherent single-qubit control. Single-qubit gate fidelities as high as 95% were observed, with the primary limitation being from non-equilibrium quasiparticles generated in the SFQ driver. The authors suggest several options for mitigating this, including the use of flip-chip bonding to separate the SFQ chip from the qubit chip. It is estimated that addressing the quasiparticle poisoning problem can increase the gate fidelity past the fault-tolerant threshold [51, 52].

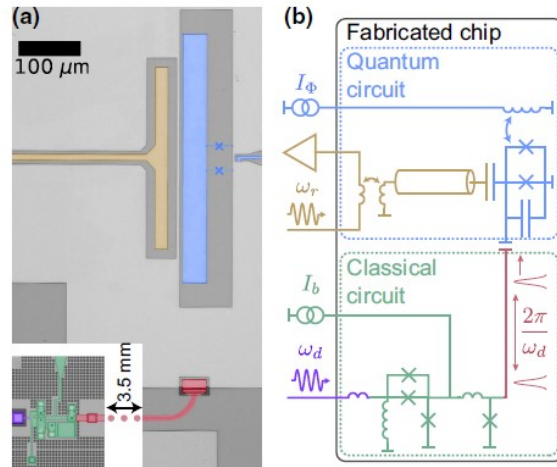


FIG. 9. Single flux quantum (SFQ) circuit coupled to qubit, reprinted from [50]. The SFQ driver circuit delivers a train of pulses at a subharmonic of the qubit frequency to perform single-qubit control.

A complementary approach to generating signals at cryogenic temperatures is to convert to the optical domain and utilize the large bandwidth available on optical fiber. The process of converting between the microwave and optical domain can be performed classically, for example by mixing two optical signals on a photo-detector, or in a way that preserves the quantum information in a single photon. If the quantum information is preserved, a bi-directional microwave to optical interface would also enable an optical link to connect nodes of a quantum computer in a distributed quantum computing environment, and it could form an integral part of a quantum network [53]. Coherent microwave to optical conversion has been demonstrated using Rydberg atoms [54] with 0.3% efficiency, and with 9% in a system

using a mechanical resonator to mediate the microwave to optical interaction [55]. In both cases, there are clear paths to increase the efficiency, though there are still many integration challenges to overcome with this approach.

The nascent field of quantum engineering is steadily advancing towards commercial viability. While there are still numerous and significant technical hurdles to overcome before a fault-tolerant quantum computer can be built, we are currently at the stage where an interdisciplinary approach is needed. In particular, microwave engineering and packaging are central to the ability to develop more complex systems, and the field will benefit from more collaborations between scientist and engineers in this area.

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