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CMOS-Compatible Protonic Programmable Resistor Based on Phosphosilicate Glass Electrolyte for Analog Deep Learning

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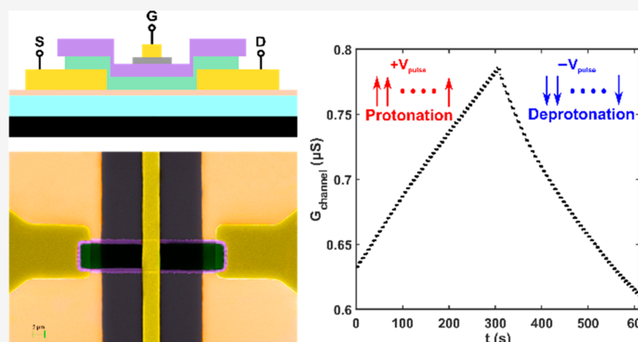
ABSTRACT: Ion intercalation based programmable resistors have emerged as a potential next-generation technology for analog deep-learning applications. Proton, being the smallest ion, is a very promising candidate to enable devices with high modulation speed, low energy consumption, and enhanced endurance. In this work, we report on the first back-end CMOS-compatible nonvolatile protonic programmable resistor enabled by the integration of phosphosilicate glass (PSG) as the proton solid electrolyte layer. PSG is an outstanding solid electrolyte material that displays both excellent protonic conduction and electronic insulation characteristics. Moreover, it is a well-known material within conventional Si fabrication, which enables precise deposition control and scalability. Our scaled all-solid-state three-terminal devices show desirable modulation characteristics in terms of symmetry, retention, endurance, and energy efficiency. Protonic programmable resistors based on phosphosilicate glass, therefore, represent promising candidates to realize nanoscale analog crossbar processors for monolithic CMOS integration.



KEYWORDS: *analog computing, doped silicon dioxide films, proton intercalation, programmable resistors*

1. INTRODUCTION

The success of deep learning in classifying and clustering representations of data at multiple levels of abstraction has fundamentally changed how information is processed.[1] However, conventional digital architectures face increasing difficulties in supporting the heavy computational workloads required to train state of the art deep neural networks (DNNs).[2] The pressing need for faster and more energy-efficient deep-learning processors has therefore led to an intensive investigation of in-memory computation schemes using analog crossbar arrays.[3,4]

The basic building block of analog crossbar arrays is the crosspoint element, which can be described as a programmable, nonvolatile resistor.[5] For a DNN to be trained successfully (i.e., without degradation of classification performance) with such architectures, the resistive devices need to have many nonvolatile conductance states that can be modulated reversibly, symmetrically, and reproducibly.[3,6] A plethora of device technologies has been proposed for analog deep learning applications such as phase-change memories,[7] filamentary[8] and bulk-switching[9] resistive memories, ferroelectric tunnel junctions,[10] spintronics,[11] and superconducting nanowires.[12] Despite significant advances in the aforementioned fields, no device technology has been identified so far that meets all of the requirements.[3]

Recently, a novel device family relying on electrochemically controlled ion intercalation in transition-metal oxide channels (also referred to as electrochemical random access memory, ECRAM) has shown promising characteristics.[13−19] Due to their similarities to solid-state batteries, the most mature versions of these devices rely on shuffling Li^+ ions across a Li^+-conducting electron-insulating electrolyte, metered by electron flow in the outer metallic circuit.[13−15] Approaches based on alkali-metal ions (Li^+, Na^+, K^+, Ca^{2+}) suffer from CMOS incompatibility, due to contamination concerns of the fabrication tools. Proton (H^+) intercalation devices are thus considered to have the edge in realizing scalable programmable resistors that are back-end-of-line (BEOL) integrable.[17−19] Moreover, the smallest ionic radius of protons (Shannon−Prewitt effective ionic radius of −0.18 Å if 2-fold coordinated and −0.38 Å if one-fold coordinated) promises high modulation speed, low energy consumption, and enhanced endurance. Indeed, in our recent work,[18] we demonstrated promising device characteristics using a PdH_x solid hydrogen

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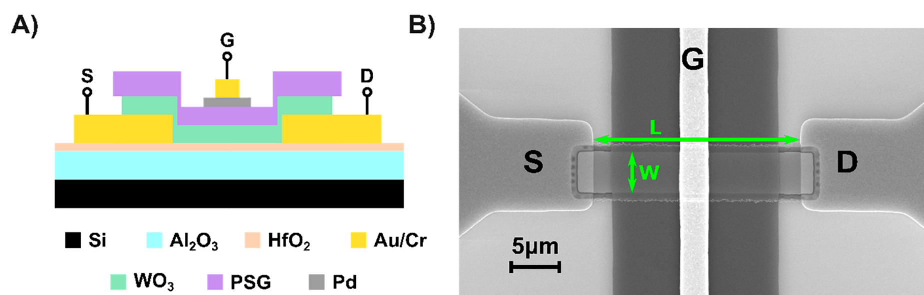

Figure 1. (A) Schematic of the protonic programmable resistor studied in this work. (B) Top-view scanning electron microscope image of a finished device showing the source (S), drain (D), and gate (G) of a device with a nominal channel width (W) of 5 μm and a length (L) of 25 μm.

reservoir, polymeric Nafion electrolyte, and WO_3 channel material for proton intercalation.

However, the main bottleneck with developing protonic programmable resistors has been the absence of a CMOS-compatible all-solid-state electrolyte that conducts protons but blocks electrons. All designs so far have relied on approaches that either cannot be integrated and scaled down, such as using organic materials,[17] using chemically and thermally sensitive polymers (e.g. Nafion),[18] or suffer from energy inefficiency such as high electric-field-induced water hydrolysis.[19] Furthermore, some protonic electrolytes rely on water absorption for proton conduction, requiring repeated rehydration of the material during operation.[20]

In this work, we demonstrate a CMOS-compatible protonic programmable resistor based on a nanoporous phosphosilicate glass (PSG) solid electrolyte. PSG is an excellent choice for this application due to its (1) good electronic insulation, (2) high room-temperature proton conductivity, (3) conduction mechanism based on P doping (instead of structural water), and (4) ready availability in conventional Si processing. The selection of this material has allowed us to use standard CMOS-fabrication techniques and consequently scale down the device footprint. Our devices show desirable modulation characteristics in terms of symmetry, retention, endurance, and energy efficiency. This new device technology appears promising in the quest to satisfy the stringent performance requirements for analog crosspoint elements. Furthermore, PSG enables exploration of alternative channel and hydrogen reservoir layers, while using a fully CMOS compatible and scalable fabrication platform.

2. DEVICE OPERATION

The protonic programmable resistor demonstrated in this work is a three-terminal device that employs a WO_3 channel, a PSG electrolyte layer, and a Pd gate reservoir (Figure 1A). We adopt a transistor-like notation to refer to the three terminals of this device. The terms "source" and "drain" are used to refer to the two ends of the WO_3 channel, while the term "gate" is used to refer to the PdH_x proton reservoir.

The basic operation principle of the device relies on modulating the channel conductance via the electrochemically controlled intercalation of protons into WO_3, as explained in our recent work.[18] Initially, protons are stored in the gate reservoir as PdH_x, which is achieved by the hydrogen uptake of Pd in a forming gas ambient (3% H_2 in N_2).[21] With the application of a voltage pulse, a controlled number of protons are moved from the gate to the channel through the solid electrolyte, while electrons concurrently move through the external circuit in the same direction. This process can be reversed by the application of a voltage pulse of inverse polarity, forcing protons out of the channel back into the gate reservoir. Protons are n-type dopants in WO_3,[22] and as they move in and out, the conductivity of the channel is modulated up and down. Furthermore, in the absence of a programming pulse (i.e., floating gate), proton motion toward either the gate or the channel is precluded, as the electrolyte prevents the electron flow required to satisfy charge neutrality in the channel and reservoir layers. This last feature establishes nonvolatility with the channel conductance remaining constant at its last programmed level.

Among several oxides whose electronic conductivity can be tuned via cation intercalation (WO_3,[18] V_2O_5,[23] MoO_3,[24] Nb_2O_5[25]), we chose to use amorphous tungsten oxide (a-WO_3) as the channel material. This selection was motivated by the well-established conductivity modulation[13,16,18] and electrochromism[19] dynamics with cation intercalation. a-WO_3 is a CMOS-compatible semiconductor with a band gap of 2.8–3.2 eV whose conductivity can be precisely modulated by protonation, taking place concurrently with charge-balancing electron filling of the W 5d orbital dominated conduction band in the dilute regime. The structure of a-WO_3 at room temperature is assumed to be similar to that of its crystalline counterpart (monoclinic based on corner-sharing WO_6 octahedra), but with disordered bond lengths and angles. The most common defect present in the WO_3 lattice structure is an oxygen vacancy, which bonds to a W^{6+} ion, reduces the oxidation state of the neighboring W^{5+} ion, and increases the conductivity, in a way analogous to the way the electron does with proton intercalation (see Figure S1). The extent of conductivity modulation in a-WO_3 by proton intercalation, therefore, depends on its initial defect concentration that determines its initial conductivity.[26]

In the search for an inorganic CMOS-compatible electrolyte layer, we focused on silicate glasses (SiO_2), which are widely used in Si technology as electron insulators.[27] Deposition conditions of silicate glasses can be engineered to yield a nanoporous structure with defect −OH terminated Si groups (silanol), providing a surface-site path for ion transport along the pores.[28] The acidic nature of silanol acts as a proton donor, which then migrates by hopping between hydroxyl groups and structural water.[29,30] Doping silicate glasses with phosphorus sterically hinders the glass network to increase nonbridging oxygen bonds,[31] replaces Si−O−Si bonds with −Si−OH and −Si−O−P−OH groups, and increases both the pore volume and surface area.[32] The P−OH groups not only have higher acidity in comparison to silanol but are also amphoteric, meaning that they can act as both proton donors and acceptors.[33] These are all key properties that provide

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phosphosilicate glass (PSG, P-SiO_2) high proton conductivity at room temperature (2.54×10^{-4} S cm^{-1}), which stands among the highest values in comparison with several perovskite, fluorite, and simple oxide proton-conducting materials,[34] while retaining their electron-insulating properties.[35] Furthermore, even though the proton conductivity of PSG can be further increased to 10^{-1} S cm^{-1} by an additional hydrothermal treatment[36] and chemisorption of water in the pore structure,[37] such modifications also result in an increased electronic conductivity of the material, which is undesirable for our design that requires nonvolatile throttling of hydrogen in WO_3.

3. METHODS

The protonic programmable resistors were fabricated on a Si substrate covered with 10/90 nm HfO_2/Al_2O_3 deposited by atomic layer deposition (ALD) for electrical and protonic insulation. Channel contacts (15/5 nm Au/Cr) were first patterned using a direct-write photolithography and liftoff process. A 10 nm WO_3 channel and 10 nm PSG electrolyte layers were blanket-deposited using ALD and plasma-enhanced chemical vapor deposition (PECVD) processes, respectively. The deposition conditions for PSG (T = 100 °C, 60 W plasma power, and gas flow ratio of 12 sccm SiH_4/12 sccm PH_3 diluted at 2% in H_2) were found to be optimal to maximize proton conductivity, as reported in ref 35. The PSG/WO_3 stack was subsequently patterned with a self-aligned reactive ion etching (RIE) process, followed by TMAH-based wet etching of WO_3 to create a PSG overhang that prevents shorting of the channel with the gate at the edges of the device. Different channel dimensions (i.e., width and length) were patterned in the range between 2 and 100 μm. Finally, the 5 nm Pd reservoir and 150/10 nm Au/Cr gate interconnect and pads were electron beam evaporated and patterned through separate liftoff processes. A cross-sectional view of a finished device is shown in Figure 1A. Full details of the fabrication process can be found in Figure S2 in the Supporting Information. Figure 1B shows the top-view scanning electron microscope image of a fabricated structure. Given the standard Si-fabrication compatibility of this process flow, it can easily be adapted to yield nanoscale devices by replacing the photolithography steps with their electron-beam lithography versions.

An atomic force microscopy (AFM) image of a PSG film deposited under the optimum conditions on a Si substrate is shown in Figure 2A. A nanogranular structure (so-called nanoglass) with a mean glassy grain diameter of ∼80 nm and an RMS roughness of ∼1 nm is observed. This image also evidences the presence of nanopores with a high surface to volume ratio, an essential requirement for efficient proton transport in this material.

The stoichiometric ratio of each element in the optimized PSG film (PSG 12:12) was found to be 0.55% P, 45.65% Si, and 53.8% O using X-ray photoelectron spectroscopy (XPS). The spectra of undoped (SiO_2), optimized (PSG 12:12), and more highly doped (PSG 12:24) films, deposited with 12:0, 12:12 and 12:24 SiH_4:PH_3 flux, respectively, were acquired (Figure 2B). While the intensity of the P 2p peak, located at a binding energy of ∼134 eV (inset), increases with PH_3 flux, that of the Si 2p peak decreases. The estimated P concentration of the PSG 12:12 film is 0.55%, a value similar to those reported for PSG films with optimized proton conductivity (2.5×10^{-4} S cm^{-1}).[35]

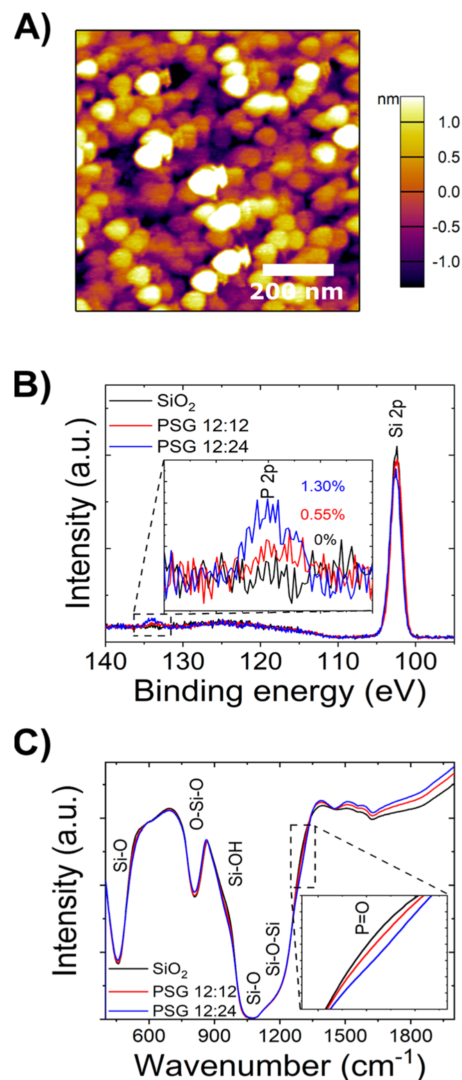

Figure 2. (A) Atomic force microscopy image of the PSG 12:12 thin film surface deposited on a Si surface. (B) X-ray photoelectron spectra of the P 2p and Si 2p peaks and (C) Fourier transform infrared spectra of the SiO_2, PSG 12:12, and PSG 12:24 thin films. The inset in (B) shows enlarged spectra in the P 2p energy range, while the inset in (C) shows enlarged spectra in the P=O absorption region.

The presence of P in the films was also confirmed by Fourier transform infrared spectroscopy (FTIR). As shown in Figure 2C, the increase in PH_3 flux results in the appearance of P=O and Si−OH absorption bands around 1300 cm^{-1} (inset) and 1130 cm^{-1}, respectively, as well as a decrease in the intensity of the Si−O and Si−O−Si bands. All of these features are indicative of the successful incorporation of P atoms in the glass structure.

4. RESULTS

Electrical characterization of the devices was conducted at room temperature in an enclosed probe station (NEXTRON MPS-PT) filled with forming gas (3% H_2 in N_2, see the Supporting Information for further details). The basic modulation properties of the devices were first measured to assess their conductance modulation depth, symmetry, retention, and endurance (Figure 3) in a pulsing mode. Figure 3A shows the increase in conductance upon the application of 100 positive voltage pulses (increment, red, V_G = 3 V, 1 s) and

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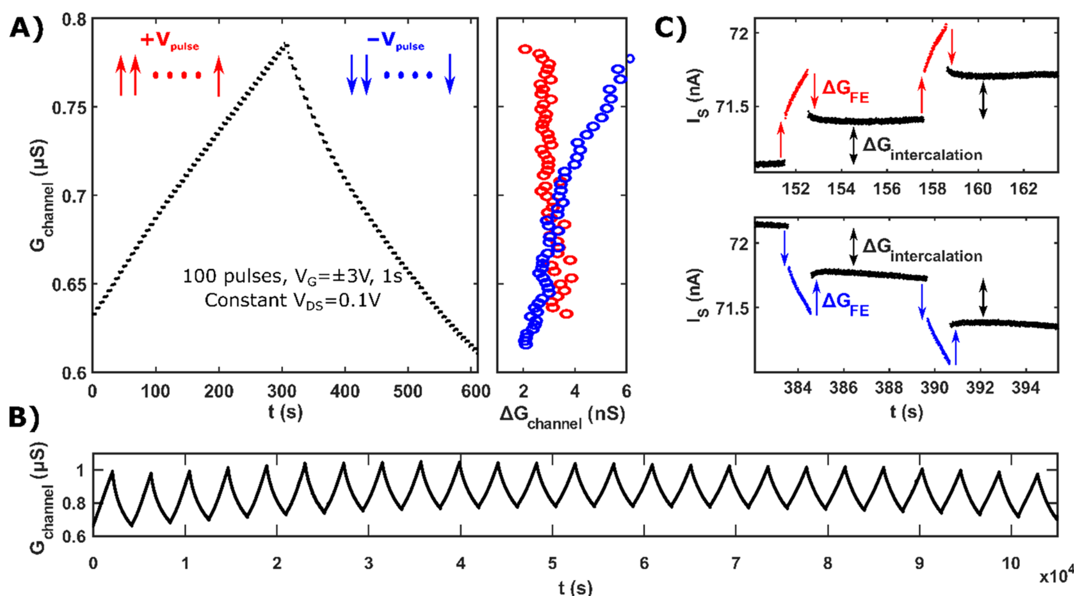

Figure 3. (A) (left) Modulation characteristics of a protonic programmable resistor (5 μm width, 50 μm length) determined by applying 50 voltage pulses of ±3 V and 1 s width in either direction. Each state is monitored for 2 s by measuring the channel current while V_{DS} = 0.1 V is applied. (right) Conductance change ($\Delta G_{channel}$) plotted at different conductance levels ($G_{channel}$). Incremental changes are shown with red markers, while decremental changes are shown with blue markers. (B) Endurance characterization throughout the application of 50000 voltage pulses (25 × [1000 ↑ 1000 ↓]) of ±3 V and 0.1 s width over the course of ~30 h. (C) Detailed picture of (A) where the channel current, I_S, is constantly recorded in the presence (colored dots) and absence (dark dots) of gate pulses.

decrease upon that of 100 negative pulses (decrement, blue, V_G = 3 V, 1 s). V_{DS} was constantly maintained at 0.1 V throughout the update sequence.

Figure 3A demonstrates very clean device conductance modulation characteristics with high symmetry and non-volatility of the programmed conductance, due to the electron-blocking properties of the PSG thin-film electrolyte (see Figure S3). A well-defined symmetry point (i.e., a conductance level at which the incremental change is equal to the decremental change in conductance) is also evidenced, as well as excellent cycling endurance characteristics, with very little variation in conductance values even after the application of 50000 pulses over the course of ~30 h (Figure 3B). Furthermore, we did not observe any noticeable open-circuit voltage development across the gate stack, allowing the operation under constant voltage pulses.

It should be noted that the base (i.e., unprotonated) conductance of the channel material is significantly higher than that of stoichiometric WO_3, therefore limiting the conductance modulation depth and the speed of the channel upon proton intercalation.[18,26] Such behavior is expected on consideration of the oxygen-deficient nature of the ALD-deposited WO_3. Indeed, an XPS analysis (Figure S6) clearly evidences a large degree of initial tungsten reduction (W^{5+}:W^{6+} ratio) and in-gap states present in the film. To mitigate this issue, the deposition method of WO_3 can be modified to target the optimal stoichiometry or alternative channel materials (e.g., V_2O_5, MoO_3, Nb_2O_5) can be used as a replacement.

A careful analysis of the modulation dynamics (Figure 3C) unravels interesting device physics, comprised of both volatile and nonvolatile changes in conductance, as programming pulses are applied. Under constant V_{DS} = 0.1 V, the source current, I_S, immediately steps up/down when a gate pulse (±3 V) is applied and then smoothly increases/decreases for the remainder of the pulse duration (colored dots). Once the pulse disappears (i.e., floating gate), another sudden drop/rise in I_S is observed. In the absence of a gate pulse, I_S remains approximately constant, at a level different from that before the application of the pulse, indicating nonvolatile programming of the channel conductance (dark dots). These sudden changes in I_S do not reflect an increase in gate current, I_G (<pA), but are due to a field-effect enhancement of the channel conductance (ΔG_{FE}). This behavior can be explained by a field-effect increase in the electron concentration and a resulting increase in conductance of the n-type WO_3 channel by the electrostatic field of protons driven within the electrolyte close to the WO_3 interface.[38,39] Unlike the nonvolatile, electrochemical intercalation induced conductance modulation ($\Delta G_{intercalation}$), this additional channel current only flows during the application of a gate voltage pulse and therefore it is volatile.

The initial channel conductance and average modulation magnitude of protonic crosspoint elements for 20 devices with varying dimensions were also examined. Figure 4A shows that both parameters scale linearly with the channel width/length (W/L) ratio, as expected. This well-behaved scaling demonstrates both a promising yield and uniformity for these PSG-based devices.

Using different channel dimensions, we have also estimated the energy efficiency and its scaling for protonic programmable resistors presented in this work. As the figure of merit, we chose the ratio of energy consumption required to change the channel conductance by a small amount ($E/\Delta G_{channel}$). This choice also enables us to compare the same value with those reported for O^{2-} ion intercalation devices in ref 16. Figure 4B reveals that, at the same device area of 200 μm^2, our devices consume 0.45 mJ/S, which is 1000× more energy efficient with respect to its heavier-ion alternative. Considering that this metric scales with L^2 (not area), we estimate the pulse energy required for a single state increment of a 100 × 100 nm^2

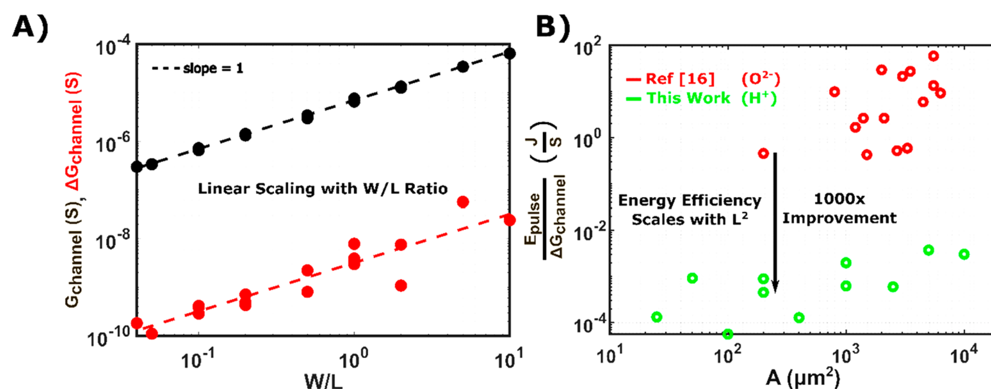

Figure 4. (A) Scaling of conductance and average conductance modulation magnitude for different channel geometries (W/L). (B) Comparison of device energy efficiency with respect to other CMOS-compatible oxygen ion intercalation devices reported in ref 16.

protonic device would be ~1 fJ, assuming a conductance range of 1−10 MΩ modulated with 1 nS incremental changes (i.e., 900 states). We expect this number to further improve upon the implementation of a stoichiometric WO_3 channel, since the oxygen-deficient nature of the current material limits its overall modulation amplitude ($\Delta G_{channel}$), as explained earlier.

5. CONCLUSION

In this work, we demonstrated a back-end CMOS-compatible protonic programmable resistor that can serve as a crosspoint element in analog crossbar processors. Conductance modulation, device scalability, and process control are ensured by the use of a thin nanoporous PSG layer, a common and CMOS-compatible material, as the proton electrolyte layer. Our devices, which also include a WO_3 channel and a PdH_x reservoir, display low energy consumption along with symmetric and nonvolatile conductance modulation for an extended number of voltage pulses. Downscaling of the device dimensions, using electron-beam lithography or other techniques, as well as the possibility of BEOL integration to CMOS chips, can be also envisioned for our technology. Ultimately, PSG can serve as a platform to explore alternative channel and hydrogen reservoir layers in protonic programmable resistors, which present desirable characteristics to realize next-generation analog accelerators for deep-learning applications.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.1c01614.

Details of fabrication, characterization methods, additional results, and discussions (PDF)

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Notes

The authors declare no competing financial interest.

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