FUNDAMENTAL STUDY OF DC TO DC CONVERSION SYSTEMS

by

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SUBMITTED IN PARTIAL FULFILLMENT OF THE
REQUIREMENTS FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
January 22, 1969

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Department of Electrical Engineering, January 22, 1969

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ABSTRACT

What is the fundamental process common to every dc to dc conversion system? How is the operation of the system limited by the characteristics of the elements composing it? In seeking answers to these questions, the thesis establishes a well-defined framework for discussing the problem. Basic results are stated in purely mathematical form, but the main application here is to electrical networks.

Graph theory is used to find bounds on dc power, ac power, and average voltages and currents within a dc to dc conversion network. The main graph theorems are derived from a theorem by Berge and Ghouila-Houri which does not seem to have received much use previously in electrical network theory.

Optimization techniques, including Pontryagin's principle, are used to relate the dc power, ac power, and average voltage and current of an element to the element's characteristics.

Also included is a theorem bounding the dc gain of a positive operator feedback system with one time-varying unit. This result is applied to electrical networks to show that every dc to dc conversion network must include at least two resistors which are time-varying and/or nonlinear.

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ACKNOWLEDGMENT

The author's appreciation and respect for mathematical preciseness and rigour has increased greatly through the encouragement and example of Professor Roger Brockett. His guidance often brought valuable insight to fundamental concepts and approaches. The advice and suggestions of Professor James Roberge and Professor Amar Bose, who served as Readers, were also highly valued.

During discussions, many useful comments and criticisms were received from Ronald Skoog, Professor Paul Penfield, and Professor Jan Willems. Their contributions are greatly appreciated.

Clara Conover has done an excellent job of typing the thesis, correcting errors, and putting the manuscript in a clear, consistent form.

Part of the research was done while the author held a National Science Foundation fellowship. The research was also supported in part by NASA under Grant No. NGR-22-009(124) with the M.I.T. Electronic Systems Laboratory and by the U. S. Army Research Office -- Durham.

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I. INTRODUCTION

1.1 Objectives: The purpose of the thesis is to meet to some degree the following main objectives:

1. To establish a framework for the discussion and investigation of the dc to dc conversion problem. It is hoped that the definitions and approaches given here will serve as a clear and rigorous foundation for this and future study of the problem. An attempt has been made to avoid leaving concepts undefined, making assumptions without justification, and using "folk lore".

2. To expose the basic concept behind the dc to dc conversion process--the features common to every dc to dc conversion system. As will be shown, every dc to dc conversion network must include at least two resistors* which are time-varying and/or nonlinear. The conversion process can be viewed in terms of their operation.

3. To indicate the different types of dc to dc conversion systems. Another feature common to all dc to dc conversion networks is that they include at least one reactance. The different types of networks can then be classified according to the types of reactances present.

4. To establish a relationship between the port parameters of a dc to dc conversion system and the parameters of the elements composing it. Most of the thesis is devoted to this objective, and the results throw some light on the other objectives. The two classes of parameters to be related might be called the converter and element specifications or the

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* Resistors are defined as the broadest sense of passive resistors (see Definition 2.2).

external and internal parameters. Below is a list of the parameters to be considered in this thesis.

External	Internal
1. Voltage (or current) step-up.	1. Number of switches.
2. Output voltage (or current).	2. Number of capacitors.
3. Output power.	3. Number of inductors.
4. Efficiency.	4. Presence of mutual coupling.
	5. Power storage capability of reactances.
	6. Voltage and current capability of elements.
	7. Lossiness of elements.
	8. Frequency limitations of switches.

Other external parameters which are usually of importance are output ripple, regulation, stability, and nonelectrical considerations such as size, weight, and cost. The thesis will not be directly concerned with these parameters.

1.2 Scope: The term "systems" in the thesis title suggests considerations broader than just electrical networks. While application to electrical networks is the underlying motivation and primary focus of the thesis, an attempt has been made to keep the development general. All basic results are stated in purely mathematical terms so that they may be applied to any system which meets the conditions set forth.

As will be seen in the mathematical development, a dc to dc conversion system in the broadest sense is a system which can be reduced to a linear graph representation. One set of variables must be a flow (satisfy Kirchoff's current law), and a second set must be a tension

(satisfy Kirchoff's voltage law). There must be only one (source-like) edge of the graph for which the average of the product of its flow variable and tension variable is negative, and one of the two variables must be constant. There must be another edge for which the average of one of the variables is greater than the like (flow or tension) variable of the "source-like" edge. Any of the basic results of the thesis can be immediately applied to a system which meets these conditions.*

In the broadest sense power conditioning may be defined as the process of receiving power with a given voltage or current waveform and delivering (almost all) that power with a different waveform. Then dc to dc conversion is a form of power conditioning since the average voltage or current level is changed.

Another type of power conditioning is frequency conversion; power is received "at a given frequency" (see Definition 2.10) and delivered at another. Examples of systems satisfying this description are modulation mixers, parametric amplifiers, dc to ac inverters, and ac to dc rectifiers. It will be shown in the thesis that a necessary part of dc to dc conversion is dc to ac and ac to dc power conversion within the network. Therefore this thesis also deals with frequency conversion where one of the frequencies is zero (dc).

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* An example of a nonelectrical system which meets the above conditions could be a system of one-way toll roads. The tolls can be adjusted to always satisfy Kirchoff's voltage law, and the flow of cars per minute satisfies Kirchoff's current law. Let one road have a fixed negative toll, and let this be the only road on which the net transfer of money at the end of some period is from the tollgate keeper to the drivers. If the number of cars passing over this road in the period is less than the number of cars passing over another road in the period, then the system is a dc to dc conversion system. If Theorem 4.3 is applied to this system, one result is that there are at least two roads for which the toll is not constant.

Several of the basic results of the thesis follow from Theorems 4.2 and 4.3, which might be called "positive decomposition theorems for positive flows and positive tensions." They appear to be due to Berge and Ghouila-Houri (3); the author has been unable to find them presented elsewhere in the literature.

Theorem 4.4, Corollary 4.4.1, and Theorem 4.5 make use of these theorems. Theorem 4.4 implies what may be a new necessary condition on resistive n-ports (see Theorem 4.6). In Appendix A Theorem 4.4 is generalized to fields in three-space. Corollary 4.4.1 implies that a set of resistors cannot produce a voltage or current greater than the sum of the voltages or currents of the sources to which it is connected (see Appendix B). This is believed to be the first that a topological proof of this intuitive fact has been given.

Theorems 5.1 and 5.2 imply that every dc to dc conversion network must include at least two resistors that are time-varying and/or nonlinear. Appendix C proves this result from a different approach, giving a basic result for a feedback system with positive operators.

1.3 Need for Research: There has been a lack of basic research in the study of dc to dc conversion systems. Most works on the subject have dealt with specific network designs or narrowly restricted classes. To the author's knowledge, the only works dealing with dc to dc conversion in a broad, fundamental way have a master's thesis by the author (16) and a paper by Moore and Wilson (8). The work by Moore and Wilson, described in Chapter III, served as the starting point for several results in this thesis.

The objectives given in the first section indicate the gaps in knowledge which the thesis seeks to fill. The assumption is, of course, that the answers to such fundamental questions will aid in the design of dc to dc conversion networks. The method of design has generally been intuitive or "cut-and-try" as a result of not knowing basic relationships between element parameters and converter parameters.

A sample design problem will illustrate some of the difficulties encountered in trying to select a configuration and component values without the knowledge of basic relations. Suppose that an engineer is given the following specifications for a dc to dc converter:

voltage in: 10 volts dc

voltage out: 40 volts dc

current out: 2 amps dc

efficiency: $\geq 85\%$

output ripple: $\leq 5\%$

size, weight, and cost restrictions

The engineer decides to try the design using no inductors since capacitors seem easier to work with than coils. An all-capacitor converter which he has seen frequently is the "ladder step-up configuration" shown in Fig. 1.1.

The configuration does not seem to require too many capacitors and switches, so the engineer decides to use this network.

He knows that it is good to use as large a capacitor as possible, so he chooses 10,000 μf, the largest permitted by the size and weight restrictions. These also have a fairly small "equivalent series resistance" of 0.06 ohms, which should be good for efficiency.

For a low output ripple, the switching frequency should be high. The 0.6 ms time constant of the capacitors restricts the frequency of operation to 400 Hz.

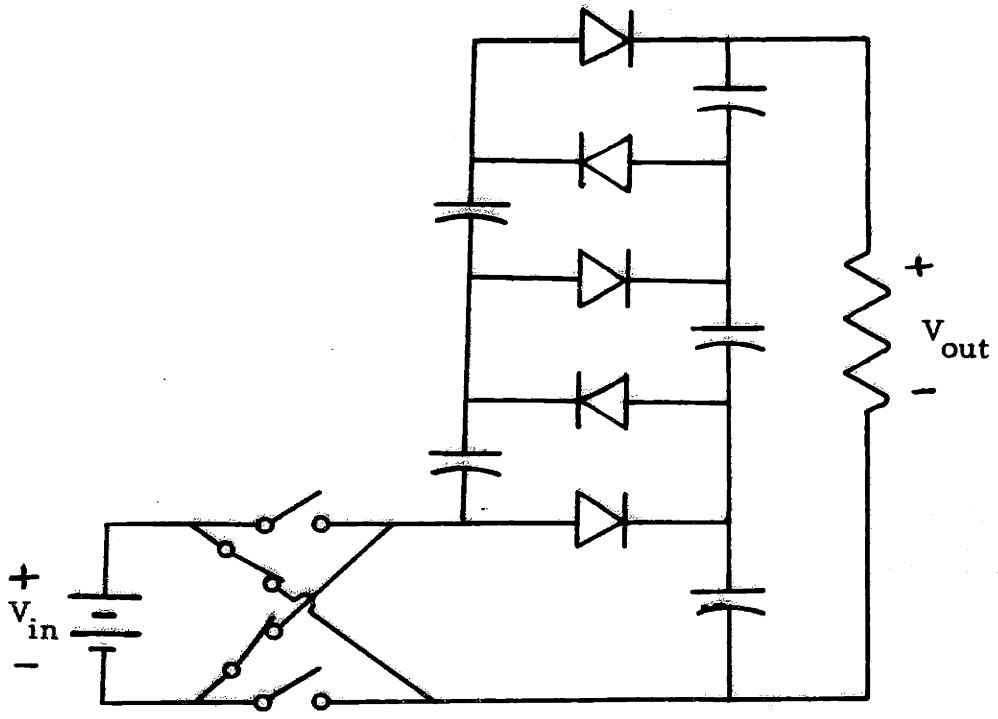


Fig. 1.1 "Ladder Step-up" dc to dc Conversion Network

The engineer then measures or calculates the losses in the network: 4 watts in the switches, 5 watts in the diodes, and 13 watts in the equivalent series resistance of the capacitors. These losses reduce the output voltage to 40 from the ideal 50, as required, but the efficiency is only 78%! Besides that the output ripple is 10%.

Were the specifications given the engineer unrealistic, considering available components? Is there another "all-capacitor" configuration which will use less capacitors and do the job better? Was it wrong to try to do without inductors in this case?

It is hoped that the results of this thesis will answer questions of this nature.

1.4 Outline of Approach: After establishing some terminology and concepts in Chapter II, we will derive some basic theorems in graph theory in Chapter IV. Chapters V and VI apply these results to dc to dc conversion networks to obtain some bounds on power, voltage, and current associated with the elements in terms of the external network parameters. In Chapter VII the power, voltage, and current associated with an element are related to the element's characteristics. Thus a relationship is finally established between the external and the internal parameters of the network (see Objective 4).

II. DEFINING THE PROBLEM CONTEXT

There are many types of dc to dc conversion systems which are in use and many more which exist in theory. The treatment in this thesis is not so general as to include all these systems, but is restricted to purely electrical systems. This excludes systems which include rotating machines, intermediate stages of radiant or thermal energy, etc. The following definitions give a further and more precise description of the context of the investigation.

Definition 2.1: When the voltage across an element (or a port) and the current through an element (or a port) are referred to, the usual convention of the current entering the positive terminal of the voltage is assumed.

Definition 2.2: A resistor is an element which constrains the voltage v across it and the current i through it according to a relation

$$f(v, i, t) = 0$$

for which any v and i which satisfy the constraint for some time t also satisfy

$$vi \geq 0$$

Note that this definition classifies diodes, transistors, switches, and most passive devices without energy storage as resistors.

The element defined here is usually called a "passive resistor". However, there will never be need to refer to resistors that are not passive.

The resistor is called time-invariant if the constraint function f is not dependent on time.

The resistor is called linear if the constraint can also be written

$$v = r(t)\, i$$

A resistor that is either not time-invariant or not linear will be called time-varying/nonlinear.

A resistor is called quasi-active if the constraint is $f(v,i,t) = 0$, and there exist v_1, i_1, t_1, v_2, i_2, and t_2 such that

$$f(v_1, i_1, t_1) = 0$$

$$f(v_2, i_2, t_2) = 0$$

$$v_2 > v_1$$

$$i_2 < i_1$$

Moore and Wilson (8) call a resistor so defined an "active resistor", but this is usually used to indicate a resistor that is not passive.

Definition 2.3: If the voltage v across an element and the current i through an element are constrained according to the relation

$$v = V \qquad \text{(a constant)},$$

the element is called a dc voltage source.

If the constraint can be written

$$i = I \qquad \text{(a constant)},$$

the element is called a dc current source.

Definition 2.4: An inductor is an element which constrains the voltage v across it and the current i through it according to the following relations:

$$v = d\lambda/dt$$

$$i = f(\lambda)$$

where $f(\lambda)$ is a monotonic increasing function of λ such that $f(0) = 0$, and $\lambda < \infty$ for $f(\lambda) < \infty$. If f is also linear, then the inductor is called a linear inductor.

Consider two n-vectors $\underline{v}$ and $\underline{i}$ where the entries of $\underline{v}$ and $\underline{i}$ indicate the voltage across and current through each of n elements. The elements are called inductors with mutual coupling if the constraint on the voltages and currents is given by

$$\underline{v} = d\underline{\lambda}/dt$$

$$\underline{i} = \underline{f}(\underline{\lambda})$$

where $\underline{\lambda}$ is an n-vector, and where the Jacobian matrix $(\partial \underline{f})/(\partial \underline{\lambda})$ of $\underline{f}$ is symmetric and positive definite for all $\underline{\lambda}$, and where the Euclidean norm $\|\underline{\lambda}\|$ of $\underline{\lambda}$ is finite for $\|\underline{f}(\underline{\lambda})\|$ finite. (This treatment follows Stern (11), p. 24.)

Note that in the case when $\underline{f}(\underline{\lambda})$ is a diagonal matrix, the elements become inductors without mutual coupling.

Definition 2.5: A capacitor is an element which constrains the voltage v across it and the current i through it according to the relations

$$i = dq/dt$$

$$v = f(q)$$

where f is a monotonic increasing function such that $f(0) = 0$, and $q < \infty$ for $f(q) < \infty$. If f is also linear, then the capacitor is called a linear capacitor.

The class of reactances consists of inductors and capacitors.

Definition 2.6: The average $\bar{x}$ of a function of time x is defined by

$$\bar{x} = \lim_{T \to \infty} \frac{1}{T} \int_0^T x \, dt$$

provided the limit exists. An over-bar is always used to indicate the average operation.

When x is periodic, this definition coincides with the usual concept of average over one period.

Definition 2.7: Consider a two-port with one of the ports designated the "input" and the other port the "output". The dc voltage (current) gain of the two-port is the magnitude of the average of the output voltage (current) divided by the magnitude of the average of the input voltage (current). If G_v represents the dc voltage gain, and v_1 and v_0 the input and output voltage, then

$$G_v = |\bar{v}_0| / |\bar{v}_1|$$

Definition 2.8: Consider a two-port network of resistors, inductors (including mutual coupling), and capacitors, with a dc voltage or current source at the input and a finite, linear, time-invariant resistor (called the load) at the output. If there exists an initial condition of the network such that the two-port has a dc voltage gain or dc current gain greater than unity, then the two-port network together with the dc source and the load is called a dc to dc conversion network. This is basically the same as the definition suggested by Moore and Wilson (8), p. 621.

Notice that a network with a dc voltage source at the input and a dc voltage gain always less than unity is considered a dc to dc conversion network if the dc current gain can be greater than unity.

A dc to dc conversion network, together with one of its solutions starting from an initial condition that gives a dc gain greater than unity, is called an operating dc to dc conversion network. We will then be able to speak of various voltages and currents in an operating network.

Definition 2.9: The power $p(t)$ absorbed at time t by an element with voltage $v(t)$ across it and current $i(t)$ through it is given by the product

$$p(t) = v(t)\ i(t)$$

If the power $p(t)$ is known for all $t > 0$, the average power $\overline{P}$ absorbed (or dissipated) by the element is given by the average of p:

$$\overline{P} = \overline{p} = \overline{vi}$$

Definition 2.10: Suppose that the voltage $v(t)$ across an element and the current $i(t)$ through the element are known for all $t > 0$. The dc power P_{dc} absorbed by the element is the product of the averages of v and i:

$$P_{dc} = \overline{v}\ \overline{i}$$

When P_{dc} is negative, it is sometimes convenient to refer to $-P_{dc}$ as the dc power delivered.

The ac power P_{ac} absorbed by the element is defined as the average power less the dc power:

$$P_{ac} = \overline{P} - P_{dc} = \overline{vi} - \overline{v}\ \overline{i}$$

The ac power delivered is the negative of P_{ac}.

NOTE: In the case when v and i are composed of a countable number of sinusoids

$$v(t) = V_0 + \mathrm{Re} \sum_{i=1}^{\infty} V_i\ e^{j\omega_i t}$$

$$i(t) = I_0 + \mathrm{Re} \sum_{i=1}^{\infty} I_i e^{j\omega_i t}$$

the average power is

$$P = V_0 I_0 + \frac{1}{2} \mathrm{Re} \sum_{i=1}^{\infty} V_i I_i^*$$

Then the definition of dc power above coincides with the definition of dc power P_0 as

$$P_0 = V_0 I_0 = \overline{v}\ \overline{i}$$

(see Penfield (9), p. 2). We also have in this case that the ac power is the sum of the powers at the frequencies other than zero, where the power P_i at the frequency ω_i is

$$P_i = \frac{1}{2} \mathrm{Re}\ V_i I_i^*$$

Some of the definitions that have been made may seem unnecessarily restrictive or too general. The following remarks will explain the motivation behind some of these definitions.

Remark 2.1: Although most dc to dc converters that are designed are periodic, the operation of averaging was defined in such a way that it did not require a period function. Thus the development in the thesis does not need to bother with specifying a period, although it applies, as a special case, to periodic systems. Also, we will gain some generality with hardly any increase in the complexity of the development.

Remark 2.2: Definition 2.8 has indicated that we will not be considering networks that include ideal transformers. The reason is that the ideal transformer is not a good model of the physical device at zero frequency (dc); and we will be very concerned with the dc characteristics of devices. In fact, if ideal transformers were allowed, the problem

of dc to dc conversion would become trivial in theory. Notice that we have allowed inductors with mutual coupling, which adequately model physical transformers, even down to zero frequency.

Remark 2.3: The definition of a dc to dc conversion network allows for only linear, time-invariant loads. This insures that the load remains distinct from those nonlinear and time-varying resistors within the network which perform the dc to dc conversion. It is true that many practical converters must deliver power to time-varying loads, and there are many problems involving transients and stability with such loads. However, the thesis will not deal with these problems. Also, specifying a linear, time-invariant load will often permit results to be expressed in a simple, meaningful way.

Remark 2.4: The definition of a dc to dc conversion network did not require that the voltage (or current) delivered to the load be constant. This coincides with reality and with most theory, where a small amount of "ripple" is always present at the output. While a good converter has only a small amount of ripple, it would be arbitrary to specify a percentage of ripple below which a network can be called a dc to dc conversion network. Therefore we require only that there be an increase in the level of the average voltage or average current.

Of the average power delivered to the load, only the dc power P_0 is of interest here:

$$P_0 = \bar{v}_0 \, \bar{i}_0$$

where v_0 and i_0 are the voltage across and current through the load. We will not be concerned with how much ac power is delivered to the load. In practice, the ac power can be spearated arbitrarily well from

the dc power, so that as little ac power as desired reaches the load. This is done by inserting the filter of Fig. 2.1 before the load.

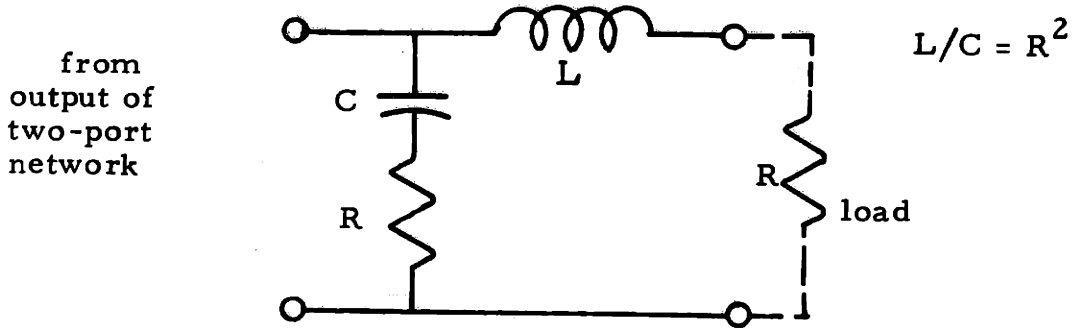


Fig. 2.1 Output Filter

The ripple at the load (and thus the ac power reaching the load) can be made arbitrarily small by increasing L and C. Notice that the output of the two-port network still sees a pure resistance, as required by Definition 2.8.

The following facts point out some basic properties of the elements that have been defined. They are not difficult to prove and, in the case of Property 2.1, can be readily seen from the definitions. In that case no proof is given. Despite their simplicity, however, the properties are fundamental to the development and will be referred to in proving theorems.

Property 2.1: A quasi-active resistor is nonlinear and/or time-varying.

A linear resistor is quasi-active if and only if it is time-varying.

A time-invariant resistor is quasi-active if and only if it is nonlinear and a portion of its v-i characteristic has a negative incremental resistance.

Property 2.2: The average voltage across an inductor is zero if the current remains finite. This implies that the dc power absorbed by the inductor is zero.

The average power absorbed by an inductor is zero if the current remains finite. Together with the first statement, this implies that the ac power absorbed by the inductor is zero.

Proof: The definition of an inductor gives us the following relation between the voltage across and the current through the inductor:

$$v = d\lambda/dt$$

$$i = f(\lambda)$$

Now, $$\overline{v} = \lim_{T\to\infty} \int_0^T v\, dt = \lim_{T\to\infty} \int_{\lambda(0)}^{\lambda(T)} d\lambda$$

$$= \lim_{T\to\infty} \frac{1}{T} [\lambda(T) - \lambda(0)]$$

But since i remains finite, $\lambda(t)$ is finite for all $t \geq 0$. Therefore

$$\overline{v} = 0$$

which proves the first statement.

Now the average power absorbed is

$$\overline{iv} = \lim_{T\to\infty} \frac{1}{T} \int_0^T f(\lambda)(d\lambda/dt)dt$$

Since $f(\lambda)$ is a monotonic increasing function of λ, this can be written

$$\overline{iv} = \lim_{T\to\infty} \frac{1}{T} \int_{\lambda(0)}^{\lambda(T)} f(\lambda)d\lambda$$

But $i = f(\lambda)$ remains finite; say $|f(\lambda)| \leq M$ for λ between $\lambda(0)$ and $\lambda(T)$, which are also finite. Then

$$|\overline{iv}| \leq \lim_{T\to\infty} \frac{1}{T} M |\lambda(T) - \lambda(0)| = 0$$

Therefore $$\overline{iv} = 0$$

Property 2.3: Consider a set of inductors with mutual coupling. If the current in each inductor remains finite, the average voltage across each must be zero. This implies that the dc power absorbed by each inductor is zero.

The sum, over the set, of the average power absorbed by each inductor is zero if the currents remain finite. Together with the first statement this implies that the total, over the set, of the ac power absorbed by the inductors is zero.

Proof: The definition of inductors with mutual coupling relates the vectors representing the voltages and currents by

$$\underline{v} = d\underline{\lambda}/dt$$

$$\underline{i} = \underline{f}(\underline{\lambda})$$

The proof that $\overline{\underline{v}} = \underline{0}$ proceeds in the same way as the proof for a single inductor.

The total average power absorbed (sum over the set of inductors) is given by

$$\overline{\underline{i}'\underline{v}} = \lim_{T\to\infty} \frac{1}{T} \int_0^T \underline{f}'(\underline{\lambda})(d\underline{\lambda}/dt)dt$$

Since $(\partial \underline{f})/(\partial \underline{\lambda})$ is a symmetric, positive-definite matrix for all $\underline{\lambda}$, we may write

$$\overline{\underline{i}'\underline{v}} = \lim_{T\to\infty} \frac{1}{T} \int_{\underline{\lambda}(0)}^{\underline{\lambda}(T)} \underline{f}'(\underline{\lambda})\, d\underline{\lambda}$$

where the integral is the same for any path between $\underline{\lambda}(0)$ and $\underline{\lambda}(T)$ in $\underline{\lambda}$-space (see Apostol (1), p. 296). But the current in each inductor remaining finite says $\|\underline{f}(\underline{\lambda})\|$ is finite; say $\|\underline{f}(\underline{\lambda})\| \leq M$ on the straight line between $\underline{\lambda}'(0)$ and $\underline{\lambda}(T)$, which also have finite norms. Then

$$\left|\overline{\underline{i}'\underline{v}}\right| \leq \lim_{T\to\infty} \frac{1}{T} nM \|\lambda(T) - \lambda(0)\| = 0$$

Therefore $$\overline{\underline{i}'\underline{v}} = 0$$

Property 2.4: The average current through a capacitor is zero if the voltage remains finite. This implies that the dc power absorbed by the capacitor is zero.

The average power absorbed by a capacitor is zero if the voltage remains finite. Together with the first statement this implies that the ac power absorbed by the capacitor is zero.

The proof is the dual of the proof of Property 2.2.

Property 2.5: The ac power absorbed by a dc voltage source or dc current source is zero.

Proof: The ac power absorbed by an element is defined as $\overline{vi} - \overline{v}\,\overline{i}$. Now, for a dc voltage source $v = \overline{v}$, and for a dc current source $i = \overline{i}$. In either case $\overline{vi} = \overline{v}\,\overline{i}$, and zero ac power is absorbed.

III. PREVIOUS RESEARCH ON THE PROBLEM

As mentioned in Chapter I, the only previous general work on dc to dc conversion networks was done by Moore and Wilson (8). This chapter will summarize their contributions.

The objectives of the paper by Moore and Wilson are to establish some definitions as guidelines in discussing the dc to dc conversion problem, to state some "basic conditions" for dc to dc conversion, and to stimulate further basic research in the area of power conditioning.

A somewhat broader context is allowed by Moore and Wilson by allowing a "network" to include nonelectrical energy storage, mechanical power transfer, and time-varying reactances which are conservative. (Compare Definitions 2.2, 2.4, 2.5 and 2.8.) Other than this, their definition of a "dc to dc conversion network" is basically the same as that used in this thesis. (See Definitions 2.3, 2.7, and 2.8.) The "active resistor" defined by Moore and Wilson is the same as the quasi-active resistor of Definition 2.2.

Four basic conditions which all dc to dc conversion networks must satisfy are stated in the paper. These are given below, making use of some definitions in Chapter II. Statements 1) and 2) are proved by Duffin (4) and Leine (7), respectively. Statements 3) and 4) are proved later in this thesis (see Theorem 5.3 and Corollary 5.4.1).

1) A network cannot convert to ac power any portion of the power it receives from a dc source unless the dc source is in a loop which contains a quasi-active resistor and no capacitors. ("Loop" is used as defined by Seshu and Reed (11), p. 15.)

2) The ac power $-P_{ac}$ which is delivered by a quasi-active resistor with the constitutive relation $f(v,i,t) = 0$ is bounded by

$$-P_{ac} \geq \max_{\substack{(v_1,i_1)\in S \\ (v_2,i_2)\in S}} [(v_2-v_1)(i_1-i_2)]$$

where S is the set of all pairs (v,i) which satisfy $f(v,i,t) = 0$ for some t.

3) A dc to dc conversion network must, within the network, convert at least a portion of the dc power it receives to ac power.

4) Let G be the dc voltage gain or dc current gain, which ever is greater than unity. Let P_0 be the dc power delivered to the load. Then the total ac power delivered by some set S of elements in the dc to dc conversion network is bounded by

$$\sum_{k\in S} P_{ac}^k \geq \frac{G-1}{G} P_0$$

IV. GRAPH THEORY

This chapter will establish some theorems about directed graphs, flows, and tensions. In Chapters V and VI these will be applied to the dc to dc conversion problem. Most of the theorems presented here are not new results but are included to lay the groundwork for Theorems 4.4 and 4.5.

Definition 4.1: We will use the following common terms as defined by Seshu and Read (11): vertex, edge, graph, loop, cut-set, connected, and nonseparable.

The remaining definitions are patterned after Berge and Ghouila-Houri (3). When their term is different, it follows in parentheses the term used here.

Definition 4.2: A directed graph (graph) is a graph for which an orientation has been assigned to each edge in the graph by ordering the pair of endpoints of each edge.

Definition 4.3: An oriented cut-set (elementary coboundary) is a cut-set to which an orientation has been assigned by ordering the pair of maximal connected subgraphs into which the cut-set divides the graph.

Let the edges of a directed graph be ordered. Then an oriented cut-set in the graph is identified with an ordered set $\{q_k\}$ where

$$q_k = \begin{cases} 0 & \text{if the } k^{th} \text{ edge is not in the cut-set.} \\ +1 & \text{if the } k^{th} \text{ edge is in the cut-set and has its orientation corresponding to the orientation of the cut-set.} \\ -1 & \text{if the } k^{th} \text{ edge is in the cut-set and has its orientation opposite to the orientation of the cut-set.} \end{cases}$$

An aligned cut-set (cocircuit) is an oriented cut-set for which the orientation of the edges in the cut-set correspond with the orientation of the cut-set. Then if $\{q_k\}$ is an aligned cut-set, each q_k is 0 or 1.

Definition 4.4: An oriented loop (elementary cycle) is a loop to which an orientation has been assigned by ordering the vertices in the loop such that successive vertices are the endpoints of an edge in the loop.

Let the edges of a directed graph be ordered. Then an oriented loop in the graph is identified with an ordered set $\{b_k\}$ where

$$b_k = \begin{cases} 0 & \text{if the } k^{th} \text{ edge is not in the loop.} \\ +1 & \text{if the } k^{th} \text{ edge is in the loop and has its orientation corresponding to the orientation of the loop.} \\ -1 & \text{if the } k^{th} \text{ edge is in the loop and has its orientation opposite to the orientation of the loop.} \end{cases}$$

An aligned loop (circuit) is an oriented loop for which the orientation of the edges in the loop correspond with the orientation of the loop. If $\{b_k\}$ is an aligned loop, then each b_k is either 0 or 1.

Definition 4.5: Let the n edges of a directed graph be ordered. A flow, relative to the graph, is an ordered set $\{\phi_k\}$ of real numbers, with each member of $\{\phi_k\}$ corresponding to an edge of the graph, which satisfies

$$\sum_{k=1}^{n} q_k \phi_k = 0$$

for every oriented cut-set $\{q_k\}$ in the graph.

It can be shown that it is sufficient if the condition is satisfied for every cut-set consisting of edges incident at a node.

A positive flow is a flow $\{\phi_k\}$ for which each member ϕ_k satisfies $\phi_k \geq 0$.

Notice that a linear combination of flows is a flow. If a flow is a function of time, then a linear function or a linear functional of the flow is a flow. That is, if $\{\phi_k(t)\}$ is a flow for all t, then $\{d\phi_k/dt\}$ and $\{\int_a^b f(t)\phi_k(t)dt\}$ are flows.

In electrical engineering the condition on a flow is called Kirchoff's current law because the currents in a network are observed to satisfy the condition.

Definition 4.6: Let the n edges of a directed graph be ordered. A tension, relative to the graph, is an ordered set $\{\theta_k\}$ of real numbers, with each member corresponding to an edge of the graph, which satisfies

$$\sum_{k=1}^{n} b_k \theta_k = 0$$

for every oriented loop $\{b_k\}$ in the graph.

A positive tension is a tension $\{\theta_k\}$ whose members satisfy $\theta_k \geq 0$.

As for a flow, a linear combination of tensions is a tension. If $\{\theta_k(t)\}$ is a tension for all t, then $\{d\theta_k/dt\}$ and $\{\int_a^b f(t)\theta_k(t)dt\}$ are tensions.

The condition on a tension is often called Kirchoff's voltage law because voltages in a network are observed to satisfy the condition.

Definition 4.7: Given a condition, result, or proof, the dual condition, result, or proof is obtained by interchanging the terms "loop" and "cut-set", and "flow" and "tension".

Theorem 4.1 (Berge and Ghouila-Houri (3), p. 147): Consider the space R^n of ordered sets of n real numbers. Given a directed graph, $\{\phi_k\}$ is a flow if and only if

$$\sum_{k=1}^{n} \theta_k \phi_k = 0$$

for every tension $\{\theta_k\}$ in R^n. Given a directed graph, $\{\theta_k\}$ is a tension if and only if

$$\sum_{k=1}^{n} \theta_k \phi_k = 0$$

for every flow $\{\phi_k\}$ in R^n.

This may be stated: the space of flows and the space of tensions are orthogonal, and they span the space R^n.

This important theorem is known in electrical engineering as Tellegen's theorem after the author who first indicated its wide application to network theory (14). For a comprehensive discussion of the history and application of Tellegen's theorem, see Penfield et al. (10).

Theorem 4.2 (Berge and Ghouila-Houri (3), p. 143): Given a directed graph with n edges, the set $\{\phi_k\}$ is a positive flow if and only if

$$\phi_k = \sum_{\ell=1}^{m} b_{k\ell} \mu_\ell \quad ; \quad k=1,2,\ldots,n$$

where the set $\{b_{k\ell}\}$ over the index k is the ℓ^{th} aligned loop of a set of m aligned loops, and the $\mu_\ell \geq 0$. As noted in Definition 4.4, each $b_{k\ell}$ is either 0 or 1.

Since $\mu_\ell \{b_{k\ell}\}$ is a positive flow for each ℓ, this theorem amounts to expressing a positive flow as a sum of "positive loop flows". (See Appendix A for a descriptive discussion.)

Theorem 4.3 (Berge and Ghouila-Houri (3), p. 146): Given a directed graph with n edges, the set $\{\theta_k\}$ is a positive tension if and only if

$$\theta_k = \sum_{\ell=1}^{m} q_{k\ell}\omega_\ell \quad ; \quad k=1,2,\ldots,n$$

where the set $\{q_{k\ell}\}$ over the index k is the ℓ^{th} aligned cut-set of a set of m aligned cut-sets, and the ω_ℓ corresponding to each cut-set satisfies $\omega_\ell \geq 0$. As noted in Definition 4.3, each $q_{k\ell}$ is either 0 or 1.

Since $\omega_\ell\{q_{k\ell}\}$ is a positive tension for each ℓ, the theorem says that a positive tension can be expressed as the sum of "positive cut-set tensions". (See Appendix A for a descriptive discussion.)

Theorem 4.4: Consider a flow $\{\phi_k\}$ and a tension $\{\theta_k\}$ relative to a directed graph G. Let the set S of edges of the graph be divided into four sets S_1, S_2, S_3, and S_4 so that

$$\theta_k\phi_k \geq 0 \quad ; \quad k\epsilon S_4$$

Then,

(a) $$\sum_{k\epsilon S_1} |\theta_k| \sum_{j\epsilon S_2} |\phi_j| - \sum_{k\epsilon S_2} \theta_k\phi_k + \sum_{k\epsilon S_3} |\theta_k\phi_k| \geq 0$$

(b) $$\sum_{k\epsilon S_1} |\phi_k| \sum_{j\epsilon S_2} |\theta_j| - \sum_{k\epsilon S_2} \theta_k\phi_k + \sum_{k\epsilon S_3} |\theta_k\phi_k| \geq 0$$

Proof: Reorient the edges of G to form a new directed graph G' as follows: reverse the orientation of the k^{th} edge if and only if $k\epsilon S^-$, where

$$S^- = \{k\epsilon S : \phi_k < 0\}$$

Form a new set $\{\theta'_k\}$ by

$$\theta'_k = \begin{cases} -\theta_k & ; \quad k \in S^- \\ +\theta_k & ; \quad \text{otherwise} \end{cases}$$

Form a new set $\{\phi'_k\}$ by

$$\phi'_k = |\phi_k| \tag{4.1}$$

It should be clear from the construction that $\{\theta'_k\}$ is a tension relative to G', $\{\phi'_k\}$ is a positive flow relative to G', and

$$\theta'_k \phi'_k = \theta_k \phi_k \quad ; \quad k \in S \tag{4.2}$$

$$|\theta'_k| = |\theta_k| \quad ; \quad k \in S \tag{4.3}$$

$$\theta'_k \geq 0 \quad ; \quad k \in S_4 \tag{4.4}$$

Now, from Theorem 4.2 we can find a set L of aligned loops $\{b_{k\ell}\}$; $\ell \in L$, with

$$b_{k\ell} = 0, 1 \qquad \text{for all} \qquad k \in S, \ \ell \in L$$

and a set $\{\mu_\ell\}$ with each member corresponding to a loop in L, and with

$$\mu_\ell \geq 0 \quad ; \quad \ell \in L$$

such that

$$\phi'_k = \sum_{\ell \in L} b_{k\ell} \mu_\ell \quad ; \quad k \in S$$

Define a new set $\{\psi'_k\}$ by

$$\psi'_k = \sum_{\ell \in L_2} b_{k\ell} \mu_\ell \quad ; \quad k \in S$$

where $L_2 = \{\ell \in L : b_{k\ell} = 1 , \ k \in S_2\}$

Then by Theorem 4.2, $\{\psi'_k\}$ is a positive flow relative to G'. Other properties of $\{\psi'_k\}$ are:

$$\psi'_k \leq \phi'_k \quad ; \quad k\epsilon S \tag{4.5}$$

$$\psi'_k = \phi'_k \quad ; \quad k\epsilon S_2 \tag{4.6}$$

Then

$$\sum_{k\epsilon S_2} \phi'_k = \sum_{k\epsilon S_2} \psi'_k = \sum_{k\epsilon S_2} \sum_{\ell\epsilon L_2} b_{k\ell}\mu_\ell = \sum_{\ell\epsilon L_2} \mu_\ell \sum_{k\epsilon S_2} b_{k\ell}$$

But for each $\ell\epsilon L_2$, $b_{k\ell} = 1$ for some $k\epsilon S_2$. Therefore

$$\sum_{k\epsilon S_2} b_{k\ell} \geq 1 \quad ; \quad \ell\epsilon L_2$$

and

$$\sum_{k\epsilon S_2} \phi'_k \geq \sum_{\ell\epsilon L_2} \mu_\ell \ .$$

But

$$\psi'_k = \sum_{\ell\epsilon L_2} b_{k\ell}\mu_\ell \leq \sum_{\ell\epsilon L_2} \mu_\ell \quad ; \quad k\epsilon S$$

Therefore

$$\psi'_k \leq \sum_{j\epsilon S_2} \phi'_j \quad ; \quad k\epsilon S \tag{4.7}$$

Now, since $\{\theta'_k\}$ is a tension and $\{\psi'_k\}$ is a (positive) flow, Theorem 4.1 can be applied to give

$$\sum_{k\epsilon S} \theta'_k \psi'_k = 0$$

or

$$\sum_{k\epsilon S_1} \theta'_k\psi'_k + \sum_{k\epsilon S_2} \theta'_k\psi'_k + \sum_{k\epsilon S_3} \theta'_k\psi'_k + \sum_{k\epsilon S_4} \theta'_k\psi'_k = 0$$

Observing that

$$|\theta'_k| \geq \theta'_k \quad ; \quad k\epsilon S$$
$$\theta'_k \geq 0 \quad ; \quad k\epsilon S_4 \qquad (4.4)$$
$$\psi'_k \geq 0 \quad ; \quad k\epsilon S$$

we obtain

$$-\sum_{k\epsilon S_1} |\theta'_k|\,\psi'_k + \sum_{k\epsilon S_2} \theta'_k \psi'_k - \sum_{k\epsilon S_3} |\theta'_k|\,\psi'_k \leq 0$$

The properties of ψ'_k given in Eqs. (4.5), (4.6), and (4.7) then give us

$$-\sum_{k\epsilon S_1} |\theta'_k| \sum_{j\epsilon S_2} \phi'_j + \sum_{k\epsilon S_2} \theta'_k \phi'_k - \sum_{k\epsilon S_3} |\theta'_k|\,\phi'_k \leq 0$$

The parameters relative to the graph G' are related to the parameters relative to G by Eqs. (4.1), (4.2), and (4.3). Using these relations, we obtain

$$-\sum_{k\epsilon S_1} |\theta_k| \sum_{j\epsilon S_2} |\phi_j| + \sum_{k\epsilon S_2} \theta_k \phi_k - \sum_{k\epsilon S_3} |\theta_k|\,|\phi_k| \leq 0$$

which gives result (a) of the theorem.

Result (b) of the theorem is the dual of result (a), and its proof is the dual of the above. Theorem 4.3 is used in place of Theorem 4.2 in the proof.

Appendix A gives a theorem involving fields in three-dimensional space. It is analogous to Theorem 4.4 and gives some insight.

Corollary 4.4.1: Consider a flow $\{\phi_k\}$ and a tension $\{\theta_k\}$ relative to a directed graph. Let the edges of the graph be divided into

two sets $\tilde{S}_1$ and $\tilde{S}_2$ so that

$$\theta_k \phi_k < 0 \quad ; \quad k \epsilon \tilde{S}_1$$

$$\theta_k \phi_k \geq 0 \quad ; \quad k \epsilon \tilde{S}_2$$

Then

(a) $$|\theta_k| \leq \sum_{j \epsilon \tilde{S}_1} |\theta_j| \quad ; \quad k \epsilon \tilde{S}_2$$

(b) $$|\phi_k| \leq \sum_{j \epsilon \tilde{S}_1} |\phi_j| \quad ; \quad k \epsilon \tilde{S}_2$$

Proof: Consider result (a) of Theorem 4.4. Let a particular edge k_o of $\tilde{S}_2$ correspond to S_2, and let the rest of $\tilde{S}_2$ correspond to S_4. Let $\tilde{S}_1$ correspond to S_1. Nothing corresponds to S_3, so that S_3 is empty. Then Theorem 4.4 gives

$$\sum_{j \epsilon \tilde{S}_1} |\theta_j| \, |\phi_{k_o}| - \theta_{k_o} \phi_{k_o} \geq 0$$

Since $\theta_{k_o} \phi_{k_o} \geq 0$, we may write

$$\sum_{j \epsilon \tilde{S}_1} |\theta_j| \, |\phi_{k_o}| - |\theta_{k_o}| \, |\phi_{k_o}| \geq 0$$

Therefore $$|\theta_{k_o}| \leq \sum_{j \epsilon \tilde{S}_1} |\theta_j|$$

But k_o was any edge of $\tilde{S}_2$, so that

$$|\theta_k| \leq \sum_{j \epsilon \tilde{S}_1} |\theta_j| \quad ; \quad k \epsilon \tilde{S}_2$$

which is result (a) of the corollary.

Result (b) of the corollary proceeds in a similar manner from result (b) of Theorem 4.4.

The results of Corollary 4.4.1 are well known in electrical engineering as the fact that a resistive network cannot give voltage gain or current gain. Talbot (13) proved the result for one source (one edge in S_1.) The result of Corollary 4.4.1, applied to a linear resistive network, is usually proved by applying superposition to Talbot's result.

To the author's knowledge, this is the first time that the results of Corollary 4.4.1 have been proved where more than one source is considered and nonlinear resistors are allowed by topological considerations only.

A direct proof of Corollary 4.4.1 (from Kirchoff's voltage and current laws) is given in Appendix B.

Theorem 4.5: Consider a flow $\{\phi_k\}$ and a tension $\{\theta_k\}$ relative to a directed graph G. Let the set S of edges of the graph be divided into four sets S_1, S_2, S_3, and S_4 so that

$$\theta_k \phi_k \geq 0 \quad ; \quad k \epsilon S_3$$

$$\theta_k \phi_k \geq 0 \quad ; \quad k \epsilon S_4$$

If (i) $$|\theta_k| > \sum_{j \epsilon S_1} |\theta_j| \quad ; \quad k \epsilon S_3$$

then (a) $$|\phi_k| \leq \sum_{j \epsilon S_2} |\phi_j| \quad ; \quad k \epsilon S_3$$

If (ii) $$|\phi_k| > \sum_{j \epsilon S_1} |\phi_j| \quad ; \quad k \epsilon S_3$$

(but (i) does not necessarily hold), then

$$\text{(b)} \qquad |\theta_k| \leq \sum_{j \in S_2} |\theta_j| \quad ; \quad k \in S_3$$

Proof: As in the proof of Theorem 4.4, reorient the edges of G to form a new directed graph G' as follows: reverse the orientation of the k^{th} edge if and only if $k \in S^-$, where

$$S^- = \{k \in S : \phi_k < 0\}$$

Form a new set $\{\theta'_k\}$ by

$$\theta'_k = \begin{cases} -\theta_k & ; \quad k \in S^- \\ +\theta_k & ; \quad \text{otherwise} \end{cases}$$

Form a new set $\{\phi'_k\}$ by

$$\phi'_k = |\phi_k| \quad ; \quad k \in S \tag{4.8}$$

It should be clear from the construction that $\{\theta'_k\}$ is a tension relative to G', $\{\phi'_k\}$ is a positive flow relative to G', and

$$|\theta'_k| = |\theta_k| \quad ; \quad k \in S \tag{4.9}$$

$$\theta'_k = |\theta_k| \quad ; \quad k \in S_3 \tag{4.10}$$

$$\theta'_k \geq 0 \quad ; \quad k \in S_4 \tag{4.11}$$

From Theorem 4.2 we can find a set L of aligned loops $\{b_{k\ell}\}$; $\ell \in L$, with

$$b_{k\ell} = 0, 1 \qquad \text{for all } k \in S, \ \ell \in L$$

and a set $\{\mu_\ell\}$ with each member corresponding to a loop in L, and with

$$\mu_\ell \geq 0 \quad ; \quad \ell \in L$$

such that

$$\phi'_k = \sum_{\ell \epsilon L} b_{k\ell} \mu_\ell \quad ; \quad k \epsilon S$$

Since $\{b_{k\ell}\}$ is a loop, $\ell \epsilon L$; and $\{\theta'_k\}$ is a tension, we have by Definition 4.6

$$\sum_{k \epsilon S} b_{k\ell} \theta'_k = 0 \quad ; \quad \ell \epsilon L_3$$

where $L_3 = \{\ell \epsilon L : b_{k\ell} = 1, \quad k \epsilon S_3\}$

or $$\sum_{k \epsilon S_1} b_{k\ell} \theta'_k + \sum_{k \epsilon S_2} b_{k\ell} \theta'_k + \sum_{k \epsilon S_3} b_{k\ell} \theta'_k + \sum_{k \epsilon S_4} b_{k\ell} \theta'_k = 0 \; ; \; \ell \epsilon L_3$$

But $$|\theta'_k| \geq \theta'_k \quad ; \quad k \epsilon S$$

and $$\theta'_k \geq 0 \quad ; \quad k \epsilon S_4 \qquad (4.11)$$

Then

$$-\sum_{k \epsilon S_1} |\theta'_k| + \sum_{k \epsilon S_2} b_{k\ell} \theta'_k + \sum_{k \epsilon S_3} b_{k\ell} \theta'_k \leq 0 \quad ; \quad \ell \epsilon L_3 \qquad (4.12)$$

Assume that condition (i) of the theorem holds. Then substituting according to Eq. (4.9) and Eq. (4.10), the condition gives

$$\theta'_k > \sum_{j \epsilon S_1} |\theta'_j| \quad ; \quad k \epsilon S_3$$

Since

$$b_{k\ell} = 1 \qquad \text{for some } k \epsilon S_3, \text{ for all } \ell \epsilon L_3$$

we may write

$$\sum_{k \epsilon S_3} b_{k\ell} \, \theta'_k > \sum_{j \epsilon S_1} |\theta'_j| \quad ; \quad k \epsilon L_3$$

Together with Ineq. (4.12) this requires

$$\sum_{k\epsilon S_2} b_{k\ell}\,\theta_k < 0 \quad ; \quad \ell\epsilon L_3$$

which implies

$$b_{k\ell} = 1 \qquad \text{for some } k\epsilon S_2, \quad \text{for all } \ell\epsilon L_3 \tag{4.13}$$

Now,

$$\sum_{j\epsilon S_2} \phi'_j = \sum_{j\epsilon S_2} \sum_{\ell\epsilon L} b_{j\ell}\mu_\ell$$

$$\geq \sum_{j\epsilon S_2} \sum_{\ell\epsilon L_3} b_{j\ell}\mu_\ell = \sum_{\ell\epsilon L_3} \mu_\ell \sum_{j\epsilon S_2} b_{j\ell}$$

Then, with Eq. (4.13), we have

$$\sum_{j\epsilon S_2} \phi'_j \geq \sum_{\ell\epsilon L_3} \mu_\ell$$

We also have

$$\phi'_k = \sum_{\ell\epsilon L} b_{k\ell}\mu_\ell = \sum_{\ell\epsilon L_3} b_{k\ell}\mu_\ell \leq \sum_{\ell\epsilon L_3} \mu_\ell \quad ; \quad k\epsilon S_3$$

Therefore $$\phi'_k \leq \sum_{j\epsilon S_2} \phi'_j \quad ; \quad k\epsilon S_3$$

The parameters in graph G' are then related back to the parameters in G by Eq. (4.8) to give

$$|\phi_k| \leq \sum_{j\epsilon S_2} |\phi_j| \quad ; \quad k\epsilon S_3$$

which proves result (a) of the theorem, given condition (i).

Condition (ii) and result (b) are duals of condition (i) and result (a). The proof that result (b) follows from condition (ii) is the dual of the above proof.

Theorem 4.4 has a very direct result when applied to resistive n-ports. The following theorem will not be used later in the thesis, but its results may be of interest in characterizing the properties of resistive n-ports.

Theorem 4.6: Consider a resistive n-port (which includes no transformers) whose set S of ports, at a given time, has voltages and currents $\{v_k\}$ and $\{i_k\}$, $k \epsilon S$. Let the ports be divided into three sets: $\tilde{S}_1$, $\tilde{S}_2$, and $\tilde{S}_3$. Then

$$\sum_{k \epsilon \tilde{S}_1} |v_k| \sum_{j \epsilon \tilde{S}_2} |i_j| + \sum_{k \epsilon \tilde{S}_2} v_k i_k + \sum_{k \epsilon \tilde{S}_3} |v_k i_k| \geq 0$$

and

$$\sum_{k \epsilon \tilde{S}_1} |i_k| \sum_{j \epsilon \tilde{S}_2} |v_j| + \sum_{k \epsilon \tilde{S}_2} v_k i_k + \sum_{k \epsilon \tilde{S}_3} |v_k i_k| \geq 0$$

Proof: Let an element be connected across each of the ports. Then the voltages and currents of the elements can be taken as $\{v_k\}$ and $\{-i_k\}$. (Note that the reference convention necessitates changing the sign of either voltage or current.) Considering Theorem 4.4, let the set S_ℓ be the set of elements across the ports in the set $\tilde{S}_\ell$, and let S_4 be the (linear, time-invariant) resistors in the n-port. Let the resistors and added elements generate the graph G. Then the currents through the resistors and elements are a flow relative to G, and the voltages across the resistors and elements are a tension relative to G. Application of Theorem 4.4 gives the results immediately.

Consider the case when a resistive n-port can be characterized by an impedance or admittance matrix. If ideal transformers are allowed, then any positive-semidefinite matrix can be realized. If ideal transformers are not allowed in the resistive n-port, then positive-semidefiniteness of the matrix is necessary but not sufficient for realizability. Another necessary condition is that the n-port not be capable of voltage gain or current gain (satisfies Corollary 4.4.1). A stronger necessary condition is that the matrix be paramount (see Weinberge (15)).

A resistive n-port must also satisfy Theorem 4.6. It is not known whether this theorem is implied by paramoncy, or whether it is a new condition on a resistive n-port.

The following example illustrates an application of Theorem 4.1, Corollary 4.4.1, and Theorem 4.5.

Example 4.1: A number of dc voltage sources with given current capabilities are available as follows:

Source 1: 1 volt at 15 amps (maximum)
Source 2: 2 volts at 8 amps (maximum)
Source 3: 2 volts at 4 amps (maximum)
Source 4: 3 volts at 2 amps (maximum)
Source 5: 4 volts at 1 amp (maximum)

It is desired to connect the sources through resistors (and wires) to a load such that the voltage across the load is seven volts. Find a bound on the current which can be delivered to the load.

We will try several approaches and compare the results. Let v_k and i_k represent the voltage and current of source k, and let v_o and i_o represent the voltage and current of the load. Let R be the set

of connecting resistors. Now since the voltages and currents of all the elements in the network form a tension and a flow, Theorems 4.1, 4.4, and 4.5 can be applied.

Considering Corollary 4.4.1, let the sources constitute S_1, and the load together with R constitute S_2. Since the load is a member of S_2, result (b) of Corollary 4.4.1 gives

$$|i_o| \leq \sum_{k=1}^{5} |i_k| \leq \boxed{30 \text{ amps}}$$

Considering Theorem 4.1 we have

$$\sum_{k=1}^{5} v_k i_k + v_o i_o + \sum_{k \epsilon R} v_k i_k = 0$$

But $$v_o i_o \geq 0$$

$$v_k i_k \geq 0 \quad ; \quad k \epsilon R$$

Therefore $$|v_o i_o| \leq -\sum_{k=1}^{5} v_k i_k \leq \sum_{k=1}^{5} |v_k i_k|$$

and $$|i_o| \leq \frac{1}{|v_o|} \sum_{k=1}^{5} |v_k i_k| \leq 49/7 = \boxed{7 \text{ amps}}$$

Considering Theorem 4.5, let $S_1 = \{1,2,3\}$, $S_2 = \{4,5\}$, S_3 = load, $S_4 = R$. Then condition (i) is satisfied:

$$|v_o| = 7 > \sum_{k \epsilon S_1} |v_k| = 5$$

Result (a) of Theorem 4.5 then gives

$$|i_o| \leq \sum_{k \epsilon S_2} |i_k| \leq \boxed{3 \text{ amps}}$$

How good the bound obtained by this last method is depends, of course, on how the sources are assigned to S_1 and S_2. An algorithm can probably be developed to find the lowest bound without trying all combinations.

A simple construction procedure shows that Theorem 4.4, properly applied, gives the lowest obtainable bound for this type of problem if

$$|i_k| \geq \sum_{j \epsilon S_2} |i_j| \quad ; \quad k \epsilon S_1$$

V. RESISTORS IN DC TO DC CONVERSION NETWORKS

As applied to networks, the flow and tension in the preceding chapter are the currents and voltages of the network and linear functions and functionals of them. The theorems of Chapter 4 require only that the network in which the currents are observed and the network in which the voltages are observed generate the same directed graph (see Definition 5.4 below). No other relation is necessary. The many applications of Theorem 4.1 (Tellegen's theorem) arise from making use of this fact. (See Penfield et al. (10).)

We will not take advantage of this flexibility of the theorems here; currents and voltages will be observed in the same network and under the same excitation. Rather we will use another kind of flexibility which Theorem 4.4 and Theorem 4.5 possess. Different applications of these theorems can be generated by dividing up the network elements into the four sets in different ways.

In this thesis we will be primarily concerned with the averages of the network parameters. Since the averaging operation (Definition 2.6) is a linear functional, the average of the currents in a network is also a flow, and the average of the voltages is also a tension. Then the operation of averaging may be performed either before or after one of the theorems in Chapter IV is invoked.

If the currents and voltages are averaged before using one of the theorems of Chapter IV, the effect is to ignore the role played by the reactances. This is because the average voltage across an inductor is zero (Properties 2.2 and 2.3), and the average current through a capacitor is zero (Property 2.4).

The following definitions will help in the study of the role of resistors in a dc to dc conversion network.

Definition 5.1: The dc-active set in an operating dc to dc conversion network is the set of elements which each absorb negative dc power (deliver positive dc power). The ac-active set in an operating dc to dc converter is the set of elements which each absorb negative ac power (deliver positive ac-power). Definition 2.10 defines dc power and ac power.

Definition 5.2: Given a network of resistors, inductors, capacitors, and dc sources, the corresponding dc network is formed as follows: Remove all capacitors from the network. Combine all nodes connected by inductors, and remove the inductors.

Definition 5.3: The primary set of a dc to dc conversion network is the set of elements in the maximal nonseparable portion of the corresponding dc network which includes the dc source. The secondary set is the set of elements in the maximal nonseparable portion of the corresponding dc network which includes the load.

The term "primary" follows Duffin's use of it (4). However, we use the term "secondary" in an entirely different way from Duffin.

Definition 5.4: The directed graph generated by a network is obtained in the obvious way: vertices correspond to nodes, edges to elements, and orientations to references. In fact, if the identity of the elements is ignored, a network is a graph. Therefore we will sometimes apply graphical terms to a network.

Definition 5.5: Given a condition, result, or proof, the dual condition, result, or proof is obtained by interchanging the terms "loop" and "cut-set", "flow" and "tension", "voltage" and "current", "inductor" and "capacitor", and "flux-linkage" and "charge".

The following properties should be clear from the definitions. No proofs are given.

Property 5.1: A linear, time-invariant resistor cannot absorb negative dc power or negative ac power.

This fact follows easily from the constraint imposed by the resistor: $v=Ri$.

Property 5.2: Any resistors in the dc-active set of an operating dc to dc converter must be time-varying/nonlinear.

This is merely a restatement of part of Property 5.1 in a specialized context.

Property 5.3: Any resistors in the ac-active set of an operating dc to dc converter must be time-varying/nonlinear.

Any resistors in the ac-active set of an operating dc to dc converter must be quasi-active (see Definition 2.2).

The first statement follows from Property 5.1. The second statement is stricter than the first, and is proved by Leine (7).

Property 5.4: The dc-active set and the ac-active set in an operating dc to dc conversion network are disjoint.

This is a result of the passivity of the resistors, inductors, and capacitors, and the fact that dc sources absorb zero ac power.

Property 5.5: Consider a network with currents $\{i_k\}$ and voltages $\{v_k\}$. Let G be the graph generated by the network, and let $\{\bar{i}_k\}$ and $\{\bar{v}_k\}$ be the averages of $\{i_k\}$ and $\{v_k\}$. Then $\{i_k\}$ and $\{\bar{i}_k\}$ are flows relative to G, and $\{v_k\}$ and $\{\bar{v}_k\}$ are tensions relative to G.

Property 5.6: Consider an operating dc to dc conversion network with currents $\{i_k\}$ and voltages $\{v_k\}$. Let $\bar{G}$ be the graph generated

by the corresponding dc network. Let the sets $\{\bar{i}_k\}$ and $\{\bar{v}_k\}$ be the averages of the i_k and v_k corresponding to elements in the corresponding dc network. Then $\{\bar{i}_k\}$ is a flow relative to $\bar{G}$, and $\{\bar{v}_k\}$ is a tension relative to $\bar{G}$.

Property 5.7: Consider an operating dc to dc conversion network with currents $\{i_k\}$ and voltages $\{v_k\}$. Let $\bar{G}$ be the graph generated by the primary set in the corresponding dc network. Let the sets $\{\bar{i}_k'\}$ and $\{\bar{v}_k'\}$ be the averages of the i_k and v_k corresponding to elements in the primary set. Then $\{\bar{i}_k'\}$ is a flow relative to $\bar{G}'$, and $\{\bar{v}_k'\}$ is a tension relative to $\bar{G}'$.

Property 5.8: Consider an operating dc to dc conversion network with currents $\{i_k\}$ and voltages $\{v_k\}$. Let $\bar{G}''$ be the graph generated by the secondary set in the corresponding dc network. Let the sets $\{\bar{i}_k''\}$ and $\{\bar{v}_k''\}$ be the averages of the i_k and v_k corresponding to elements in the secondary set. Then $\{\bar{i}_k''\}$ is a flow relative to $\bar{G}''$, and $\{\bar{v}_k''\}$ is a tension relative to $\bar{G}''$.

Theorem 5.1: There is at least one resistor which is in both the dc-active set and the secondary set of an operating dc to dc conversion network.

Proof. Case 1: The network achieves dc voltage gain greater than unity.

Let the sets $\{\bar{i}_k''\}$ and $\{\bar{v}_k''\}$ be the averages of the currents and voltages corresponding to elements in the secondary set. Then Property 5.8 says that we may apply Corollary 4.4.1 to $\{\bar{i}_k''\}$, $\{\bar{v}_k''\}$, and the graph $\bar{G}''$ generated by the secondary set. Assume that no elements of the dc-active set, other than possibly the dc source, are in the secondary set. If the dc source is in the secondary set, then according

to Corollary 4.4.1 the set S_1 consists of the dc source, and S_2 consists of the other elements in the secondary set (resistors, including the load). Let the average of the voltage across the dc source be $\bar{v}_1''$. Then result (a) of Corollary 4.4.1 gives

$$|\bar{v}_k''| \leq |\bar{v}_1''| \quad ; \qquad k \epsilon S_2 \tag{5.1}$$

But by Definition 5.3, the load is a member of S_2, and thus the average $\bar{v}_0$ of the load voltage is a member of $\{\bar{v}_k''\}$. The network has voltage gain greater than unity, so that

$$|\bar{v}_0''| > |\bar{v}_1''|$$

which contradicts Ineq. (5.1). Therefore an element in the dc-active set other than the dc source must be in the secondary set. This element must be a resistor since the secondary set includes no capacitors or inductors.

Case 2: The network achieves dc current gain greater than unity. The proof in this case is the dual of the proof in Case 1. Result (b) of Corollary 4.4.1 is used in place of result (a).

Corollary 5.1.1: The secondary set of a dc to dc conversion network includes at least one time-varying/nonlinear resistor.

This follows from Property 5.2.

Lemma 5.2.1. (Penfield et al. (10)): Let P_{dc}^k, P_{ac}^k, and $\bar{P}^k$ be the dc power, ac power, and average power absorbed by the k^{th} element. Let S be the set of elements in the network. Then

$$\sum_{k \epsilon S} P_{dc}^k = \sum_{k \epsilon S} P_{ac}^k = \sum_{k \epsilon S} \bar{P}^k = 0$$

Proof: Property 5.5 together with Theorem 4.1 imply

$$\sum_{k\epsilon S} v_k i_k = 0 \qquad (5.2)$$

and $$\sum_{k\epsilon S} \bar{v}_k \bar{i}_k = \sum_{k\epsilon S} P_{dc}^k = 0$$

The average of Eq. (5.2) is

$$\sum_{k\epsilon S} \overline{v_k i_k} = \sum_{k\epsilon S} \bar{P}^k = 0$$

Now the ac power absorbed by element k is

$$P_{ac}^k = \bar{P}^k - P_{dc}^k \quad ; \quad k\epsilon S$$

Therefore $$\sum_{k\epsilon S} P_{ac}^k = \sum_{k\epsilon S} \bar{P}^k - \sum_{k\epsilon S} P_{dc}^k = 0$$

which completes the results of the lemma.

Theorem 5.2. (after Duffin (4)): There is at least one resistor which is in both the ac-active set and the primary set of an operating dc to dc conversion network.

Proof: Let P_{dc}^k, P_{ac}^k, and $\bar{P}^k$ be the dc power, ac power, and average power absorbed by the k^{th} element. Let S be the set of elements in the network, and let S' be the primary set.

Property 5.6 and Theorem 4.1 imply

$$\sum_{k\epsilon S'} P_{dc}^k = 0$$

we also have from Lemma 5.2.1

$$\sum_{k\epsilon S} \bar{P}^k = 0$$

or $$\sum_{k\epsilon S'} \bar{P}^k + \sum_{k\epsilon(S-S')} \bar{P}^k = 0$$

Therefore $$\sum_{k\epsilon S'} \bar{P}^k - \sum_{k\epsilon S'} P_{dc}^k + \sum_{k\epsilon(S-S')} \bar{P}^k = 0$$

or $$\sum_{k\epsilon S'} P_{ac}^k + \sum_{k\epsilon(S-S')} \bar{P}^k = 0 \qquad (5.3)$$

Case 1: The load is in $(S-S')$. Now by Definition 5.3 the dc source is in S'; then $\bar{P}^k \geq 0$, $k\epsilon(S-S')$. But Definition 2.8 requires the load to be finite, so that the average power absorbed by the load is non-zero. Therefore

$$\sum_{k\epsilon(S-S')} \bar{P}^k > 0$$

and Eq. (5.3) therefore implies

$$\sum_{k\epsilon S'} P_{ac}^k < 0$$

Since the dc source absorbs no ac power, and S' includes no inductors or capacitors, there must be a resistor k' in S', for which $P_{ac}^{k'} < 0$; that is, k' is in the ac-active set.

Case 2: The load is in S'. Then by Definition 5.3 S' is also the secondary set. Theorem 5.1 implies then that there is at least one resistor k'' in S' for which $P_{dc}^{k''} < 0$. But $P_{ac}^{k''} = \bar{P}^{k''} - P_{dc}^{k''}$, so that for this resistor $P_{ac}^{k''} > 0$.

Assume that no member of the ac-active set is in S'. Then $P_{ac}^k \geq 0$; $k\epsilon S'$. But $k''\epsilon S'$, and $P_{ac}^{k''} > 0$. Therefore

$$\sum_{k\epsilon S'} P_{ac}^k > 0 \qquad (5.4)$$

Also, since the dc source is in S', $\bar{P}^k \geq 0$; $k\epsilon(S-S')$, and

$$\sum_{k\epsilon(S-S')} \bar{P}^k \geq 0 \tag{5.5}$$

But Ineq. (5.4) together with Ineq. (5.5) contradict Eq. (5.3). Then there must be at least one member k' of the ac-active set in S'. Since the dc source absorbs no ac power, and S' includes no inductors or capacitors, that member must be a resistor.

Corollary 5.2.1: The primary set of a dc to dc conversion network includes at least one time-varying/nonlinear resistor which is quasi-active.

This follows from Property 5.3.

Theorem 5.3: Consider an operating dc to dc conversion network. Let R_{dc} be the set of resistors in the dc-active set, and R_{ac} be the set of resistors in the ac-active set. If P_{dc}^k and P_{ac}^k are the dc power and the ac power absorbed by the k^{th} element, then

$$\sum_{k\epsilon R_{ac}} P_{dc}^k \geq -\sum_{k\epsilon R_{ac}} P_{ac}^k \geq \sum_{k\epsilon R_{dc}} P_{ac}^k \geq -\sum_{k\epsilon R_{dc}} P_{dc}^k > 0$$

Proof: Let the sets of resistors, inductors, and capacitors in the network be R, L, and C. Let the ac power absorbed by the dc source be P_{ac}^1. According to Lemma 5.2.1, the total of the ac power absorbed by all elements in a network is zero:

$$P_{ac}^1 + \sum_{k\epsilon L} P_{ac}^k + \sum_{k\epsilon C} P_{ac}^k + \sum_{k\epsilon R} P_{ac}^k = 0 \tag{5.6}$$

But we have from Properties 2.2, 2.3, 2.4, and 2.5,

$$\sum P_{ac}^k = 0 \quad ; \quad k\epsilon L$$

$$P_{ac}^k = 0 \quad ; \quad k\epsilon C$$

$$P_{ac}^1 = 0$$

Then Eq. (5.6) becomes

$$\sum_{k\epsilon R} P_{ac}^{k} = 0$$

Let the set of resistors in neither R_{dc} nor R_{ac} be designated R^{*}. Then, observing Property 5.4, we may write

$$\sum_{k\epsilon R_{dc}} P_{ac}^{k} + \sum_{k\epsilon R_{ac}} P_{ac}^{k} + \sum_{k\epsilon R^{*}} P_{ac}^{k} = 0$$

But by definition, $P_{ac}^{k} \geq 0$; $k\epsilon R^{*}$. Therefore

$$-\sum_{k\epsilon R_{ac}} P_{ac}^{k} \geq \sum_{k\epsilon R_{dc}} P_{ac}^{k} \tag{5.7}$$

Now $$P_{ac}^{k} = \overline{P}^{k} - P_{dc}^{k} \quad ; \quad k\epsilon R \tag{5.8}$$

where $\overline{P}^{k}$ is the average power absorbed, which is non-negative for a resistor. Applying this to $k\epsilon R_{dc}$

$$\sum_{k\epsilon R_{dc}} P_{ac}^{k} \geq -\sum_{k\epsilon R_{dc}} P_{dc}^{k} \tag{5.9}$$

Eq. (5.8), applied to $k\epsilon R_{ac}$, gives

$$\sum_{k\epsilon R_{ac}} P_{dc}^{k} \geq -\sum_{k\epsilon R_{ac}} P_{ac}^{k} \tag{5.10}$$

Theorem 5.1 implies

$$\sum_{k\epsilon R_{dc}} P_{dc}^{k} > 0 \tag{5.11}$$

Inequalities (5.7), (5.9), (5.10), and (5.11) together constitute the result of the theorem.

Theorem 5.4: The total dc power delivered by the set R_{dc} of resistors in the dc-active set of an operating dc to dc conversion network is bounded in terms of the dc voltage gain G and the dc power P_0 delivered to the load by

$$-\sum_{k\epsilon R_{dc}} P_{dc}^{k} \geq \frac{G-1}{G} P_0$$

The result also holds for G the dc current gain.

Proof: Property 5.6 says that we may apply Theorem 4.4 to the set of average currents $\{\bar{i}_k\}$ and the set of average voltages $\{\bar{v}_k\}$ corresponding to elements in the corresponding dc network and to the graph which it generates. Considering result (a) of Theorem 4.4, let S_1 be the dc source with voltage v_1. Let S_2 be the load with voltage v_0 and current i_0. Let S_3 be the set R_{dc} of resistors in the dc-active set. Let S_4 be the remaining resistors in the corresponding dc network. Then result (a) of Theorem 4.4 is

$$|\bar{v}_1|\,|\bar{i}_0| - \bar{v}_0\,\bar{i}_0 + \sum_{k\epsilon R_{dc}} |\bar{v}_k\,\bar{i}_k| \geq 0$$

Now the load is a linear, time-invariant resistor, so $\bar{v}_0\,\bar{i}_0 \geq 0$. Also $\bar{v}_k\,\bar{i}_k < 0$; $k\epsilon R_{dc}$. Then

$$|\bar{v}_1|\,|\bar{i}_0| - |\bar{v}_0|\,|\bar{i}_0| - \sum_{k\epsilon R_{dc}} \bar{v}_k\bar{i}_k \geq 0$$

or

$$-\sum_{k\epsilon R_{dc}} \bar{v}_k\,\bar{i}_k \geq \frac{|\bar{v}_0| - |\bar{v}_1|}{|\bar{v}_0|}\,|\bar{v}_0|\,|\bar{i}_0|$$

But

$$P_{dc}^{k} \equiv \bar{v}_k \bar{i}_k$$

$$P_0 \equiv \bar{v}_0 \bar{i}_0 = |\bar{v}_0| |\bar{i}_0|$$

$$G \equiv |\bar{v}_0| / |\bar{v}_1|$$

The result follows.

The proof for G the dc current gain proceeds similarly, using result (b) of Theorem 4.4 instead of result (a).

Corollary 5.4.1: A bound on the total ac power delivered by the set R_{ac} of resistors in the ac-active set of an operating dc to dc conversion network is given by

$$-\sum_{k \epsilon R_{ac}} P_{ac}^{k} \geq \frac{G-1}{G} P_0$$

where G is either the dc voltage gain or the dc current gain, and P_0 is the dc power delivered to the load.

This follows from Theorem 5.3 and Theorem 5.4.

The corollary proves statement 4 made by Moore and Wilson (8).

Corollary 5.4.2: A bound on the total dc power absorbed by the set R_{ac} of resistors in the ac-active set of an operating dc to dc conversion network is given by

$$\sum_{k \epsilon R_{ac}} P_{dc}^{k} \geq \frac{G-1}{G} P_0$$

where G is either the dc voltage gain or the dc current gain, and P_0 is the dc power delivered to the load.

This also follows from Theorem 5.3 and Theorem 5.4.

If we make a constraint on the topology of the dc to dc conversion network, we can obtain a somewhat better bound than that given by Theorem 5.4. The next theorem investigates this.

Theorem 5.5: Let R_{dc} and R_{ac} be the sets of resistors in the dc-active set and ac-active set of an operating dc to dc conversion network. Let P_{dc}^k and P_{ac}^k be the dc power and ac power absorbed by the k^{th} element. If the primary set of the network is not also the secondary set, then

$$\sum_{k\epsilon R_{ac}} P_{dc}^k \geq -\sum_{k\epsilon R_{ac}} P_{ac}^k \geq -\sum_{k\epsilon R_{dc}} P_{dc}^k \geq P_0$$

where P_0 is the dc power delivered to the load.

Proof: According to Property 5.8, we may apply Theorem 5.1 to the set of average currents $\{\bar{i}_k\}$ and the set of average voltages $\{\bar{v}_k\}$ of the elements in the secondary set and to the graph generated by the secondary set in the corresponding dc network. Let S'' be the secondary set. Then Theorem 4.1 gives

$$\sum_{k\epsilon S''} \bar{v}_k \bar{i}_k = \sum_{k\epsilon S''} P_{dc}^k = 0$$

Since the primary set is different from the secondary set, the dc source is not in S''. Also, S'' includes no reactances. Let R^* be the set of resistors (other than the load) which are not in R_{dc}. Then

$$\sum_{k\epsilon R_{dc}} P_{dc}^k + \sum_{k\epsilon R^*} P_{dc}^k + P_0 = 0$$

But by definition $P_{dc}^k \geq 0$; $k\epsilon R^*$. Therefore

$$-\sum_{k\epsilon R_{dc}} P_{dc}^k \geq P_0$$

Together with Theorem 5.3, this gives the result of the theorem.

Theorem 5.6: Let R_{ac} be the set of resistors in the ac-active set of an operating dc to dc conversion network. Then we have the following bounds on the average currents $\bar{i}_k$ and the average voltages $\bar{v}_k$ of the resistors R_{ac}:

(a) $$\sum_{k\epsilon R_{ac}} |\bar{i}_k| \geq (G_v - 1)\ |\bar{i}_0|$$

where G_v is the dc voltage gain, and i_0 is the load voltage.

(b) $$\sum_{k\epsilon R_{ac}} |\bar{v}_k| \geq (G_i - 1)\ |\bar{v}_0|$$

where G_i is the dc current gain, and v_0 is the load voltage.

Proof: Property 5.6 says that we may apply Theorem 4.4 to the set of average currents $\{\bar{i}_k\}$ and the set of average voltages $\{\bar{v}_k\}$ corresponding to elements in the corresponding dc network and to the graph which it generates. Considering result (a) of Theorem 4.4, let S_1 be the dc source with voltage v_1. Let S_2 be the set R_{ac} of resistors in the ac-active set, together with the load with voltage v_0 and current i_0. Let S_3 be the set R_{dc} of resistors in the dc-active set. Let S_4 be the remaining resistors in the corresponding dc network. Then result (a) of Theorem 4.4 is

$$|\bar{v}_1| \sum_{k\epsilon R_{ac}} |\bar{i}_k| + |\bar{v}_1|\,|\bar{i}_0| - \sum_{k\epsilon R_{ac}} \bar{v}_k\bar{i}_k - \bar{v}_0\bar{i}_0 + \sum_{k\epsilon R_{dc}} |\bar{v}_k\bar{i}_k| \geq 0$$

Now $v_0 i_0 \geq 0$; and $\bar{v}_k\bar{i}_k < 0$, $k\epsilon R_{dc}$. Then

$$|\bar{v}_1| \sum_{k\epsilon R_{ac}} |\bar{i}_k| + |\bar{v}_1|\,|\bar{i}_0| - \sum_{k\epsilon R_{ac}} \bar{v}_k\bar{i}_k - |\bar{v}_0|\,|\bar{i}_0| - \sum_{k\epsilon R_{dc}} \bar{v}_k\bar{i}_k \geq 0$$

By Theorem 5.3

$$\sum_{k\epsilon R_{ac}} \bar{v}_k \bar{i}_k \geq - \sum_{k\epsilon R_{dc}} \bar{v}_k \bar{i}_k$$

Therefore $$|\bar{v}_1| \sum_{k\epsilon R_{ac}} |\bar{i}_k| + |\bar{v}_1| |\bar{i}_0| - |\bar{v}_0| |i_0| \geq 0$$

or $$\sum_{k\epsilon R_{ac}} |\bar{i}_k| \geq (|\bar{v}_0|/|\bar{v}_1| - |) |\bar{i}_0| = (G_v - 1) |\bar{i}_0|$$

which is result (a) of the theorem.

Result (b) follows in a similar manner, using result (b) of Theorem 4.4 instead of result (a).

Theorem 5.7: Let R_{dc} be the set of resistors in the dc-active set of an operating dc to dc conversion network. Then the average voltages $\bar{v}_k$ and the average currents $\bar{i}_k$ of the resistors in R_{dc} are bounded as follows:

(a) $$\sum_{k\epsilon R_{dc}} |\bar{v}_k| \geq \frac{G_v - 1}{G_v} |\bar{v}_0|$$

where G_v is the dc voltage gain, and v_0 is the load voltage.

(b) $$\sum_{k\epsilon R_{dc}} |\bar{i}_k| \geq \frac{G_i - 1}{G_i} |\bar{i}_0|$$

where G_i is the dc current gain, and i_0 is the load current.

Proof: Property 5.6 says that we may apply Corollary 4.4.1 to the set of average currents $\{\bar{i}_k\}$ and the set of average voltages $\{\bar{v}_k\}$ corresponding to elements in the corresponding dc network and to the graph $\bar{G}$ which it generates. Considering result (a) of Corollary 4.4.1, the

set S_1 is the set R_{dc} of resistors in the dc-active set together with the dc source with voltage v_1. The set S_2 consists of the remaining resistors in the corresponding dc network, including the load with voltage v_0. Then result (a) of Corollary 4.4.1 gives

$$|\bar{v}_0| \leq \sum_{k \epsilon R_{dc}} |\bar{v}_k| + |\bar{v}_1|$$

or $$\sum_{k \epsilon R_{dc}} |\bar{v}_k| \geq \frac{|\bar{v}_0|/|\bar{v}_1| - 1}{|\bar{v}_0|/|\bar{v}_1|} |\bar{v}_0| = \frac{G_v - 1}{G_v} |\bar{v}_0|$$

which is result (a) of the theorem.

Result (b) follows in a similar manner, using result (b) of Corollary 4.4.1 instead of result (a).

Theorem 5.7 does not give a meaningful bound on the $\bar{v}_k$ in R_{dc} when $G_v < 1$ or on the $\bar{i}_k$ in R_{dc} when $G_i < 1$. The bounds given by the following theorem are meaningful in these cases, although they are not so strong as the bounds in Theorem 5.7 in other cases.

Theorem 5.8: Let R_{dc} be the set of resistors in the dc-active set of an operating dc to dc conversion network. If the dc voltagegain is greater than unity; that is, for v_1 the dc source voltage and v_0 the load voltage,

(i) $$|\bar{v}_i| < |\bar{v}_0|$$

then (a) $$\sum_{k \epsilon R_{dc}} |\bar{i}_k| \geq |\bar{i}_0|$$

where i_0 is the load current.

If the dc current gain is greater than unity; that is, for i_1 the dc source current,

(ii) $$|\bar{i}_1| < |\bar{i}_0|$$

then (b) $$\sum_{k \epsilon R_{dc}} |\bar{v}_k| \geq |\bar{v}_0|$$

Proof: Property 5.6 says that we may apply Theorem 4.5 to the set of average currents $\{\bar{i}_k\}$ and the set of average voltages $\{\bar{v}_k\}$ corresponding to elements in the corresponding dc network and to the graph which it generates.

Considering result (a) of Theorem 4.5, let the set S_1 be the dc source. Let S_2 be the set R_{dc} of resistor in the dc-active set. Let S_3 be the load. Let S_4 be the remaining resistors in the corresponding dc network. Then condition (i) of Theorem 4.5 is satisfied, and result (a) of Theorem 4.5 is

$$\sum_{k \epsilon R_{dc}} |\bar{i}_k| \geq |\bar{i}_0|$$

which is also result (a) of this theorem.

Result (b) follows in a similar manner from condition (ii), using result (b) of Theorem 4.5 in place of result (a).

It is a well-known fact that a passive network cannot achieve both voltage gain and current gain greater than unity. Conservation of power is cited as the proof. For completeness we will prove this fact for dc voltage gain and dc current gain as we have defined them.

Theorem 5.9: Let the dc voltage gain and dc current gain of an operating dc to dc conversion network be G_v and G_i. Then

$$G_v G_i \leq 1$$

Proof: Lemma 5.2.1 states that the total average power absorbed by the set S of all the elements in a network is zero:

$$\sum_{k\epsilon S} \bar{P}^k = 0$$

Since the $\bar{P}^k = 0$ for the reactances, and $\bar{P}^k \geq 0$ for the resistances, we then have

$$\bar{P}^1 + \bar{P}^0 \leq 0$$

where $\bar{P}^1$ and $\bar{P}^0$ are the average power dissipated by the dc source and the load, respectively. Now Property 2.5 implies

$$\bar{P}^1 \equiv P^1_{dc} + P^1_{ac} = P^1_{dc} = \bar{v}_1 \bar{i}_1$$

Also, since the load is a linear, time-invariant resistor, Property 5.1 implies

$$\bar{P}^0 \equiv P^0_{dc} + P^0_{ac} \geq P^0_{dc} = \bar{v}_0 \bar{i}_0$$

Therefore

$$\bar{v}_1 \bar{i}_1 + \bar{v}_0 \bar{i}_0 \leq 0$$

$$|\bar{v}_0|\,|\bar{i}_0| \leq |\bar{v}_1|\,|\bar{i}_1|$$

$$\frac{|\bar{v}_0|}{|\bar{v}_1|}\,\frac{|\bar{i}_0|}{|\bar{i}_1|} \leq 1$$

$$G_v G_i \leq 1 \qquad \text{Q.E.D.}$$

A consequence of Theorem 5.9 is that G_v and G_i cannot both be greater than unity.

Remark 5.1: Theorems 5.1, 5.2, and 5.3 imply that every dc to dc conversion network has at least two time-varying/nonlinear resistors. The purpose of one of these, the resistor in the ac-active set, can be viewed as converting dc power to ac power. The resistor in the dc-active

set converts the ac power back to dc power. This dc power, and possibly dc power directly from the dc source, are delivered to the load. Figure 5.1 illustrates this process.

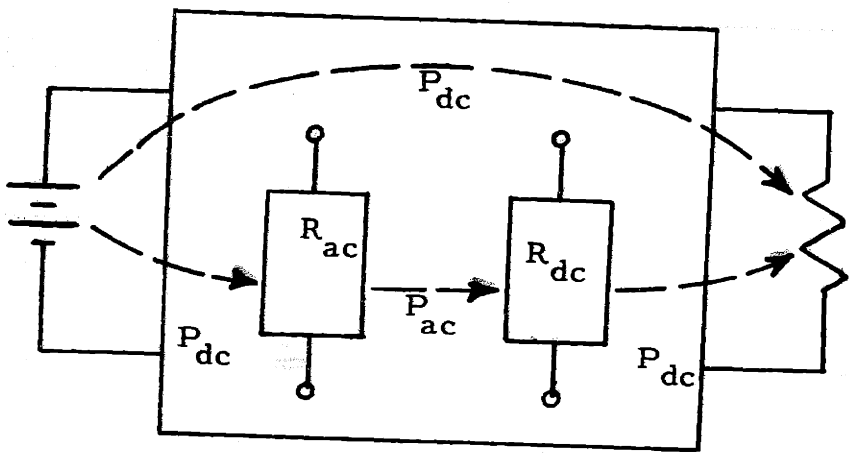


Figure 5.1 Power Transfer in a dc to dc Conversion Network

Remark 5.2: Notice that the requirement that a resistor absorb negative dc power is equivalent to saying that the average current and average voltage have opposite sign. This implies that a locus of current versus voltage must lie in both the first and third quadrants. The device usually used to realize the necessary resistor(s) in the dc-active set is a diode. The v-i characteristic of a typical diode is shown in Fig. 5.2.

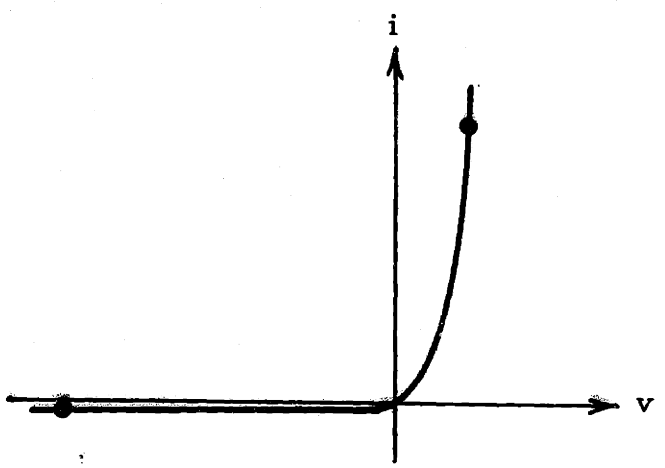
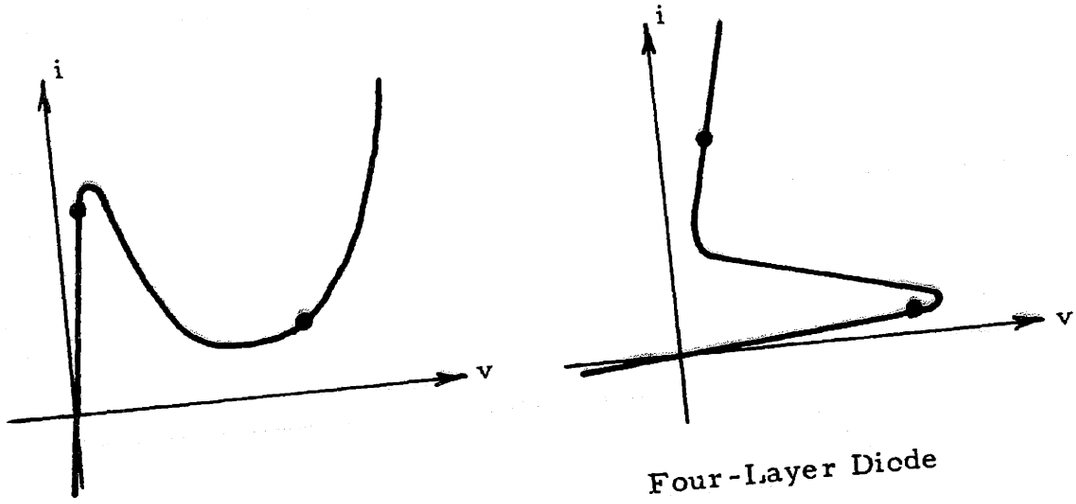


Figure 5.2 v-i Characteristic of a Diode

The diode is said to switch if its operating point changes quadrants. If the "open" voltage and "closed" current are not too small, the diode will absorb negative dc power.

The resistor in the ac-active set has no requirement that it operate in both the first and third quadrants. However, it is quasi-active, and as Property 2.1 points out: if the resistor is time-invariant, its v-i characteristic must have a portion with negative incremental resistance. Therefore a simple diode cannot be used to realize the necessary resistor(s) in the ac-active set. Examples of time-invariant devices which have satisfactory v-i characteristics are tunnel diodes and four-layer diodes. The v-i characteristics of these two devices are shown in Fig. 5.3



Tunnel Diode

Four-Layer Diode

Figure 5.3 v-i Characteristics of Devices which May Be in the ac-Active Set

It is easy to show that any time-varying resistor may be made to absorb negative ac power. Two time-varying devices commonly used to realize the resistor(s) in the ac-active set are relays and transistors. Figure 5.4 shows the v-i characteristics of these devices for two different times.

Typical operating points are indicated on the characteristics.

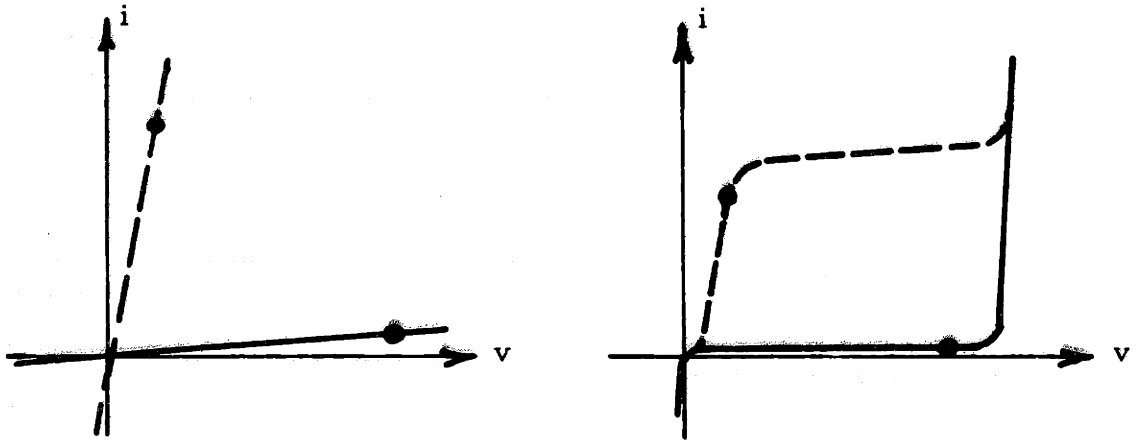


Figure 5.4 v-i Characteristics of Two Time-Varying Devices

Remark 5.3: Referring to Fig. 5.1, if the "lower path" of power transfer is eliminated, the network cannot act as a dc to dc converter. One would then expect that if the power through this path is restricted, then the dc gain or some other parameter of the converter would be restricted. Theorem 5.4 gives the relationship. It indicates that less dc power delivered by resistors in the dc-active set (or less ac power delivered by resistors in the ac-active set) implies less dc gain or less dc power delivered to the load.

The condition of Theorem 5.5 is equivalent to eliminating the "upper path" of power transfer in Fig. 5.1. The result of Theorem 5.5 then gives the lower bound on the power transferred by "lower path".

The next chapter will show how the maximum dc power or ac power that a resistor can deliver is dependent on its characteristics. We will also see how the average power dissipated by a resistor is related to the dc power or ac power that it delivers.

Remark 5.4: Theorems 5.6, 5.7, and 5.8 give bounds on the average current and average voltage of the resistors in the dc-active and ac-active sets. Note that a restriction on the average current in terms of the average voltage (and vice-versa) may always be obtained through the restriction on the dc power given by Theorems 5.4 and 5.5.

The utility of these bounds is obvious since the average current of a device is often limited. In the next chapter, the average voltage and current will be related to peak voltage and current.

Example 5.1: We will consider a specific dc to dc conversion network to illustrate the results of the theorems in this chapter. Figure 5.5 shows a simple inductor fly-back dc to dc converter with dc voltage gain greater than unity.

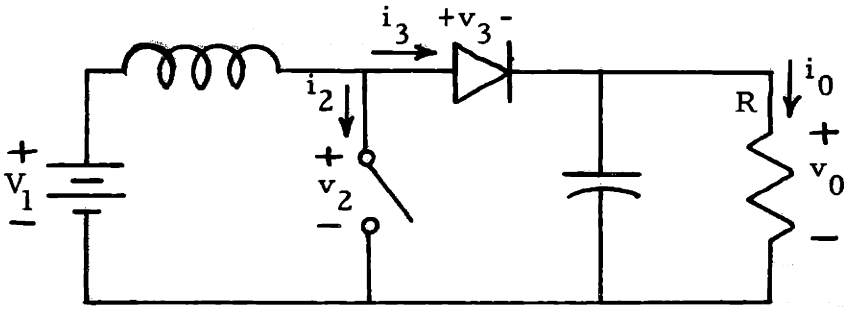


Figure 5.5 Simple dc to dc Conversion Network

The dc voltage gain depends on the duty cycle of the switch. Assume that the inductor and capacitor are large enough that their current and voltage, respectively, are nearly constant in steady-state. Then the dc voltage gain is given by $G = (1-d)^{-1}$ where d is the duty cycle of the switch.

Consider the case for $V_1 = 1$, $d = 2/3$, and $R = 1$. Then

$$G = 3$$

$$v_0 = 3 \;,\; i_0 = 3 \;,\; P_0 = 9$$

$$\bar{v}_2 = 1 \;,\; \bar{i}_2 = 6 \;,\; P^2_{dc} = 6$$

$$\bar{v}_3 = -2 \;,\; \bar{i}_3 = 3 \;,\; P^3_{dc} = -6$$

Now the dc-active set consists of the dc voltage source and the diode, and the ac-active set consists of the switch. Then we may check that the above figures satisfy the theorems of this chapter:

Theorem 5.3: $P^2_{dc} \geq - P^2_{ac} \geq P^3_{ac} \geq - P^3_{dc} > 0$

$$6 \geq 6 \geq 6 \geq 6 \geq 0$$

Theorem 5.4: $-P^3_{dc} \geq \frac{G-1}{G} P_0$

$$6 \geq \frac{3-1}{3} 9$$

Theorem 5.6: $|\bar{i}_2| \geq (G-1)\,|\bar{i}_0|$

$$6 \geq (3-1)\,3$$

Theorem 5.7: $|\bar{v}_3| \geq \frac{G-1}{G}\,|\bar{v}_0|$

$$2 \geq \frac{3-1}{3}\,3$$

Theorem 5.8: $|\bar{i}_3| \geq |\bar{i}_0|$

$$3 \geq 3$$

Remark 5.5: Example 5.1 shows that Theorems 5.4, 5.6, 5.7, and 5.8 give a greatest lower bound (not for a specific network, but in general).

Remark 5.6: The purpose of the theorems is obviously not to obtain bounds on the parameters in a specific network since the actual values may easily be found directly from the network. Rather the theorems give a priori bounds for all dc to dc conversion networks. They tell

"the best that can be done", and the parameters of a specific network can be checked against these results to see if it is possible to better the parameters.

Example 5.2: To illustrate when Theorem 5.5 is applicable, we give an example of a dc to dc conversion network for which the primary set is not also the secondary set.

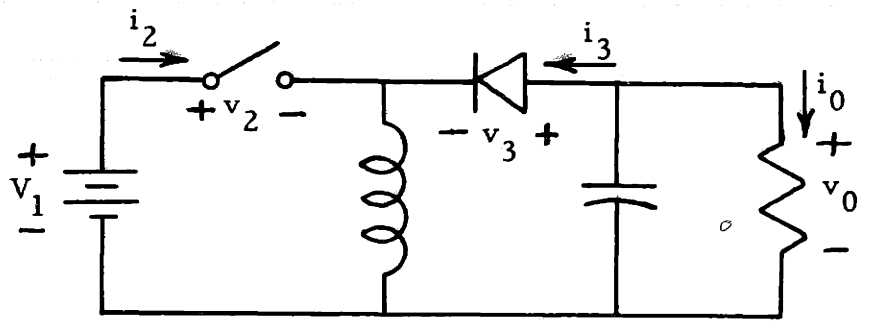


Figure 5.6 Dc to dc Conversion Network with Disjoint Primary and Secondary Sets

Consider the network of Fig. 5.6. Identifying the nodes to which the inductor is connected causes the network to become separable at that node. Then the primary set consists of the dc voltage source and the switch, and the secondary set consists of the load and the diode.

Assume that the inductor and capacitor are large enough that their current and voltage are nearly constant in steady-state. Then the dc voltage gain is given by $G_v = d/(1-d)$, where d is the duty cycle of the switch. For $d = 3/4$, $V_1 = 1$, and $R = 1$, we have

$$v_0 = -3 \quad , \quad i_0 = -3 \quad , \quad P_0 = 9$$

$$\bar{v}_2 = 1 \quad , \quad \bar{i}_2 = 9 \quad , \quad P_{dc}^2 = 9$$

$$\bar{v}_3 = -3 \quad , \quad \bar{i}_3 = 3 \quad , \quad P_{dc}^3 = -9$$

so that $$P_{dc}^{2} \geq -P_{dc}^{3} \geq P_{0}$$

as required by Theorem 5.5.

Remark 5.7: Example 5.2 shows that Theorem 5.5 gives a greatest lower bound (not for a specific network, but in general).

As mentioned after Definition 2.8, a network with a dc voltage source at the input and which has a dc voltage gain less than unity is still considered a dc to dc conversion network if the dc current gain is greater than unity. Such a "voltage step-down" network is illustrated in the next example.

Example 5.3: Consider the dc to dc conversion network in Fig. 5.7,

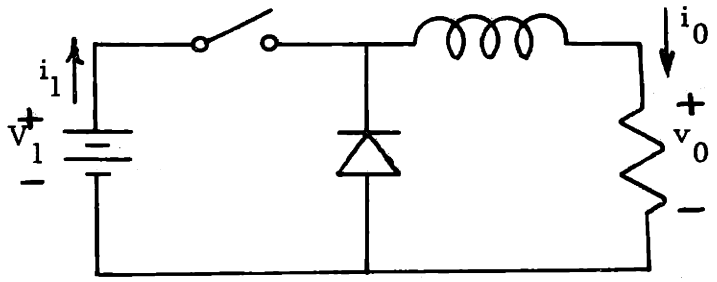


Figure 5.7 Voltage Step-Down dc to dc Conversion Network

An analysis similar to that of Fig. 5.5 in Example 5.1 shows that

$$G_v = d \leq 1$$
$$G_i = d^{-1} \geq 1$$

where d is the duty cycle of the switch.

It is easy to show that this network also satisfies Theorems 5.3, 5.4, 5.6, 5.7, and 5.8, as it must since it meets the conditions of a dc to dc conversion network.

VI. REACTANCES IN DC TO DC CONVERSION NETWORKS

In this chapter we will study dc to dc conversion networks by first applying a theorem from Chapter IV and then performing the averaging operation. The purpose is to observe some average parameters associated with the reactances. Now, the average power absorbed by a reactance, the average voltage across an inductor, and the average current through a capacitor are all zero. However, we will select time-dependent sets (in the theorems) so that the parameters of interest do not vanish.

Lemma 6.1.1: Given v_1, v_0, and i_0 which satisfy

$$v_1 = \bar{v}_1 \quad \text{(constant)}$$

$$v_0 = R i_0 \quad ; \quad R \text{ constant}$$

$$|\bar{v}_0| \geq |\bar{v}_1|$$

then $$\overline{v_0 i_0} - \overline{|v_1||i_0|} \geq (|\bar{v}_0| - |\bar{v}_1|)\,\overline{|i_0|}$$

The dual lemma also holds.

Proof:

$$\overline{v_0 i_0} = R\,\overline{i_0 i_0} \geq R\,\overline{|i_0|}\;\overline{|i_0|}$$

$$\geq R\,|\bar{i}_0|\;\overline{|i_0|} = |\bar{v}_0|\;\overline{|i_0|}$$

Also, since $v_1 = \bar{v}_1$,

$$\overline{|v_1|\,|i_0|} = |\bar{v}_1|\;\overline{|i_0|}$$

Then $$\overline{v_0 i_0} - \overline{|v_1|\,|i_0|} \geq (|\bar{v}_0| - |\bar{v}_1|)\,\overline{|i_0|}$$

But $$|\bar{v}_0| \geq |\bar{v}_1|$$

Therefore $$\overline{v_0 i_0} - \overline{|v_1|\,|i_0|} \geq (|\bar{v}_0| - |\bar{v}_1|)\,|\bar{i}_0|$$

Lemma 6.1.2: Let X be a set of reactances, and let

$$X^-(t) = \{k \epsilon X : v_k(t)\, i_k(t) < 0\}$$

Then

$$\overline{\sum_{k \epsilon X^-(t)} v_k i_k} = -\frac{1}{2} \sum_{k \epsilon X} \overline{|v_k i_k|}$$

Proof:

$$\overline{\sum_{k \epsilon X^-(t)} v_k i_k} \triangleq \lim_{T \to \infty} \frac{1}{T} \int_0^T \sum_{k \epsilon X^-(t)} v_k i_k \, dt$$

Let

$$Q_k^+(T) = \{t : v_k(t) i_k(t) \geq 0 \ , \ 0 \leq t \leq T\}$$

$$Q_k^-(T) = \{t : v_k(t) i_k(t) < 0 \ , \ 0 \leq t \leq T\}$$

Then we may write equivalently,

$$\overline{\sum_{k \epsilon X^-(t)} v_k i_k} = \sum_{k \epsilon X} \lim_{T \to \infty} \frac{1}{T} \int_{Q_k^-(T)} v_k i_k \, dt \qquad (6.1)$$

Now, the average power absorbed by a reactance is zero; viz.,

$$\overline{v_k i_k} \triangleq \lim_{T \to \infty} \frac{1}{T} \int_0^T i_e v_e \, dt$$

(continued on next page)

$$= \lim_{T\to\infty} \frac{1}{T} \left[\int_{Q_k^+(T)} v_k i_k dt + \int_{Q_k^-(T)} v_k i_k \, dt \right]$$

$$= 0 \quad ; \quad k\epsilon X$$

Therefore

$$\lim_{T\to\infty} \frac{1}{T} \int_{Q_k^+(T)} v_k i_k \, dt = - \lim_{T\to\infty} \frac{1}{T} \int_{Q_k^-(T)} v_k i_k \, dt \quad ; \quad k\epsilon X$$

Then

$$\overline{|v_k i_k|} \triangleq \lim_{T\to\infty} \frac{1}{T} \int_0^T |v_k i_k| \, dt$$

$$= \lim_{T\to\infty} \frac{1}{T} \left[\int_{Q_k^+(T)} v_k i_k \, dt - \int_{Q_k^-(T)} v_k i_k \, dt \right]$$

$$= -2 \lim_{T\to\infty} \frac{1}{T} \int_{Q_k^-(T)} v_k i_k \, dt \quad ; \quad k\epsilon X$$

Together with Eq. (6.1), this gives the result of the lemma.

Theorem 6.1: Consider a dc to dc conversion network which has a dc voltage source at the input. Let X be the set of reactances, P_0 be the dc power delivered to the load, and G_v be the dc voltage gain. If $G_v > 1$, then

$$\frac{1}{2} \sum_{k\epsilon X} \overline{|v_k i_k|} \geq \frac{G_v - 1}{G_v} P_0$$

The dual theorem also holds.

Proof: By Property 5.5 we may apply Thecrem 4.4 to the currents $\{i_k\}$ and voltages $\{v_k\}$ of the elements in the network and to the graph G which it generates. Considering result (a) of Theorem 4.4, let S_1 be the dc voltage source with voltage v_1. Let S_2 be the load with voltage v_0 and current i_0. Let S_3 be the set $X^-(t)$ of reactances for which $v_k(t)i_k(t) < 0$; $k\epsilon X$. Let S_4 be the resistors, together with the reactances for which $v_k(t)i_k(t) \geq 0$; $k\epsilon X$. Then result (a) of Theorem 4.4 gives

$$|v_1||i_0| - v_0 i_0 + \sum_{k\epsilon X^-(t)} |v_k i_k| \geq 0$$

But by definition

$$|v_k i_k| = -v_k i_k \quad ; \quad k\epsilon X^-(t)$$

Therefore we can write

$$|v_1||i_0| - v_0 i_0 - \sum_{k\epsilon X^-(t)} v_k i_k \geq 0$$

Taking the average of both sides,

$$\overline{|v_1|\,|i_0|} - \overline{v_0 i_0} - \overline{\sum_{k\epsilon X^-(t)} v_k i_k} \geq 0$$

Then Lemma 6.1.1 and Lemma 6.1.2 give

$$\frac{1}{2}\sum_{k\epsilon X} \overline{|v_k i_k|} \geq (|\bar{v}_0| - |\bar{v}_1|)\,|\bar{i}_0|$$

$$= \frac{|\bar{v}_0|/|\bar{v}_1| - 1}{|\bar{v}_0|/|\bar{v}_1|}\; |\bar{v}_0|\,|\bar{i}_0|$$

$$= \frac{G_v - 1}{G_v}\; P_0$$

The proof of the dual theorem is the dual of the above proof.

Lemma 6.2.1: Consider a capacitor as characterized in Definition 2.5; that is, the constitutive relations are

$$v = f(q)$$

$$i = dq/dt$$

where $df(q)/dq \geq 0 \quad ; \quad f(0) = 0$

Let $Q^+(T) = \{t : v(t)i(t) \geq 0 \ , \ 0 \leq t \leq T\}$

$Q^-(T) = \{t : v(t)i(t) < 0 \ , \ 0 \leq t \leq T\}$

If the voltage v remains finite, then

$$\lim_{T\to\infty} \frac{1}{T} \int_{Q^-(T)} |i|\,dt = \lim_{T\to\infty} \frac{1}{T} \int_{Q^+(T)} |i|\,dt = \frac{1}{2}\overline{|i|}$$

Proof:

$$\frac{dq}{dt} = i$$

$$\frac{d(q^2)}{dt} = 2q\frac{dq}{dt} = 2qi$$

Then if the zero-crossings of $q(t)$ are countable,

$$\operatorname{sgn}\frac{d|q|}{dt} \equiv \operatorname{sgn}\frac{d(q^2)}{dt} = \operatorname{sgn}(qi)$$

except on a set of measure zero. But the conditions on $f(q)$ imply that

$$\operatorname{sgn}(q) = \operatorname{sgn}(v)$$

Then $$\operatorname{sgn}\frac{d|q|}{dt} = \operatorname{sgn}(vi)$$

Now, $$\left|\frac{d|q|}{dt}\right| \equiv \left|\frac{dq}{dt}\right|$$

Therefore $$\frac{d|q|}{dt} \equiv \left[\operatorname{sgn}\frac{d|q|}{dt}\right]\left|\frac{dq}{dt}\right| = \left[\operatorname{sgn}(vi)\right]|i|$$

Noting the definition for $Q^+(T)$ and $Q^-(T)$, we may write

$$|q(T)| \equiv \int_0^T \frac{d|q|}{dt}\, dt + |q(0)|$$

$$= \int_{Q^+(T)} |i|\, dt - \int_{Q^-(T)} |i|\, dt + |q(0)| \qquad (6.2)$$

Definition 2.5 also requires that v finite implies q finite. Then

$$\lim_{T\to\infty} \frac{1}{T} |q(T)| = \lim_{T\to\infty} \frac{1}{T} |q(0)| = 0$$

Applying these facts to Eq. (6.2), we obtain

$$\lim_{T\to\infty} \frac{1}{T} \int_{Q^+(T)} |i|\, dt = \lim_{T\to\infty} \frac{1}{T} \int_{Q^-(T)} |i|\, dt$$

which is the first result of the lemma. Now,

$$\overline{|i|} \triangleq \lim_{T\to\infty} \frac{1}{T} \int_0^T |i|\, dt$$

$$= \lim_{T\to\infty} \frac{1}{T} \int_{Q^+(T)} |i|\, dt + \lim_{T\to\infty} \frac{1}{T} \int_{Q^-(T)} |i|\, dt$$

$$= 2 \lim_{T\to\infty} \frac{1}{T} \int_{Q^+(T)} |i|\, dt$$

which gives the second result of the lemma.

Theorem 6.2: Consider a dc to dc conversion network which has a dc voltage source at the input. Let C be the set of capacitors, L be the set of inductors, G_v be the dc voltage gain, and i_0 be the load current. If $G_v > 1$, then

$$\frac{1}{2} \sum_{k\in C} \overline{|i_k|} + \sum_{k\in L} \overline{|i_k|} \geq (G_v - 1)\, \overline{|i_0|}$$

The dual theorem also holds.

Proof: By Property 5.5 we can apply Theorem 4.4 to the currents $\{i_k\}$ and voltages $\{v_k\}$ of the elements in the network and to the directed graph which it generates. Considering result (a') of Theorem 4.5, let S_1 be the dc voltage source with voltage v_1. Let S_2 be the set $X^+(t)$ of reactances for which $v_k(t)i_k(t) \geq 0$, together with the load with voltage v_0 and current i_0. Let S_3 be the set $X^-(t)$ of reactances for which $v_k(t)i_k(t) < 0$. Let S_4 be the set of resistors in the network. Then result (a) of Theorem 4.4 gives

$$|v_1|\,|i_0| + |v_1| \sum_{k\in X^+(t)} |i_k| - v_0 i_0 - \sum_{k\in X^+(t)} v_k i_k + \sum_{k\in X^-(t)} |v_k i_k| \geq 0 \tag{6.3}$$

By definition

$$|v_k i_k| = -v_k i_k \quad ; \quad k\in X^-(t)$$

and the union of $X^+(t)$ and $X^-(t)$ is the set X of all reactances. Then we may combine the last two terms of Ineq. (6.3) and write

$$|v_1|\,|i_0| + |v_1| \sum_{k\in X^+(t)} |i_k| - v_0 i_0 - \sum_{k\in X} v_k i_k \geq 0$$

Taking the average of both sides,

$$\overline{|v_1|\,|i_0|} - \overline{v_0 i_0} + \overline{|v_1| \sum_{k\in X^+(t)} |i_k|} + \sum_{k\in X} \overline{v_k i_k} \geq 0 \tag{6.4}$$

Now, Lemma 6.1.1 has

$$\overline{v_0 i_0} - \overline{|v_1|\,|i_0|} \geq (|\overline{v}_0| - |\overline{v}_1|)\,|\overline{i}_0|$$

Since v_1 is constant,

$$\overline{|v_1| \sum_{k\in X^+(t)} |i_k|} = |\overline{v}_1| \overline{\sum_{k\in X^+(t)} |i_k|}$$

In accord with Properties 2.2, 2.3, and 2.4,

$$\sum_{k\epsilon X} \overline{v_k i_k} = 0$$

Using these three facts in Ineq. (6.4), we obtain

$$|\overline{v}_1| \overline{\sum_{k\epsilon X^+(t)} |i_k|} \geq (|\overline{v}_0| - |\overline{v}_1|) |\overline{i}_0|$$

$$\overline{\sum_{k\epsilon X^+(t)} |i_k|} \geq \left[\frac{|\overline{v}_0|}{|\overline{v}_1|} - 1\right] |\overline{i}_0| = (G_v - 1) |\overline{i}_0|$$

Let $C^+(t)$ be the set of capacitors for which $v_k(t)i_k(t) \geq 0$, and let $L^+(t)$ be the set of inductors for which $v_k(t)i_k(t) \geq 0$. Then we have

$$\overline{\sum_{k\epsilon C^+(t)} |i_k|} + \overline{\sum_{k\epsilon L^+(t)} |i_k|} \geq (G_v - 1) |\overline{i}_0| \tag{6.5}$$

Now, $$\overline{\sum_{k\epsilon C^+(t)} |i_k|} \triangleq \lim_{T\to\infty} \frac{1}{T} \int_0^T \sum_{k\epsilon C^+(t)} |i_k| \, dt$$

Let $Q_k^+(T) = \{t : v_k(t)i_k(t) \geq 0, \quad 0 \leq t \leq T\}$

Then $$\overline{\sum_{k\epsilon C^+(t)} |i_k|} = \sum_{k\epsilon C} \lim_{T\to\infty} \frac{1}{T} \int_{Q_k^+(T)} |i_k| \, dt$$

Lemma 6.2.1 then gives

$$\overline{\sum_{k\epsilon C^+(t)} |i_k|} = \frac{1}{2} \sum_{k\epsilon C} \overline{|i_k|} \tag{6.6}$$

Now, since $L^+(t)$ is a subset of L,

$$\overline{\sum_{k\epsilon L^+(t)} |i_k|} \leq \overline{\sum_{k\epsilon L} |i_k|} = \sum_{k\epsilon L} \overline{|i_k|} \tag{6.7}$$

Inequality (6.5), Eq. (6.6), and Ineq. (6.7) yield the result of the theorem.

The proof of the dual theorem is the dual of the above proof, using result (b) of Theorem 4.4 in place of result (a), and using the Lemma 6.3.1 (stated next) in place of Lemma 6.2.1.

Lemma 6.3.1: Consider an inductor as characterized in Definition 2.3; that is, the constitutive relations are

$$i = f(\lambda)$$

$$v = d\lambda/dt$$

where $df(\lambda)/d\lambda \geq 0$; $f(0) = 0$

Let $Q^+(T) = \{t : v(t)i(t) \geq 0 \ , \ 0 \leq t \leq T\}$

$Q^-(T) = \{t : v(t)i(t) < 0 \ , \ 0 \leq t \leq T\}$

If the current remains finite, then

$$\lim_{T\to\infty} \frac{1}{T} \int_{Q^-(T)} |v|dt = \lim_{T\to\infty} \frac{1}{T} \int_{Q^+(T)} |v|dt = \frac{1}{2} \overline{|v|}$$

Proof: The proof is the dual of that for Lemma 6.2.1.

Theorem 6.3: Consider a dc to dc conversion network which has a dc voltage source at the input. Let C be the set of capacitors, L be the set of inductors, G_v be the dc voltage gain, and v_0 be the load voltage. Then

$$\sum_{k\in C} \overline{|v_k|} + \frac{1}{2} \sum_{k\in L} \overline{|v_k|} \geq \frac{G_v - 1}{G_v} |\overline{v}_0|$$

The dual theorem also holds.

Proof: By Property 5.5 we can apply Corollary 4.4.1 to the currents $\{i_k\}$ and the voltages $\{v_k\}$ of the elements in the network and to the directed graph which it generates. Considering result (a) of Corollary 4.4.1, S_1 is the source with voltage v_1 together with the set $X^-(t)$ of

reactances for which $v(t)i(t) < 0$. And S_2 consists of the load with voltage v_o together with the set of resistors and the set $X^+(t)$ of reactances for which $v(t)i(t) \geq 0$. Since the load is a member of S_2, result (a) of Corollary 4.4.1 gives

$$|v_1| + \sum_{k\epsilon X^+(t)} |v_k| \geq |v_0|$$

or

$$\sum_{k\epsilon X^+(t)} |v_k| \geq |v_0| - |v_1|$$

Taking the average of both sides,

$$\overline{\sum_{k\epsilon X^+(t)} |v_k|} \geq \overline{|v_0|} - \overline{|v_1|} = \overline{|v_0|} - |\bar{v}_1|$$

$$\geq |\bar{v}_0| - |\bar{v}_1| = \frac{|\bar{v}_0|/|\bar{v}_1| - 1}{|\bar{v}_0|/|\bar{v}_1|} |\bar{v}_0| = \frac{G_v - 1}{G_v} |\bar{v}_0|$$

Let $C^+(t)$ be the set of capacitors for which $v_k(t)i_k(t) \geq 0$, and let $L^+(t)$ be the set of inductors for which $v_k(t)i_k(t) \geq 0$. Then we have

$$\overline{\sum_{k\epsilon C^+(t)} |v_k|} + \overline{\sum_{k\epsilon L^+(t)} |v_k|} \geq \frac{G_v - 1}{G_v} |\bar{v}_0| \qquad (6.8)$$

Now,

$$\overline{\sum_{k\epsilon L^+(t)} |v_k|} \triangleq \lim_{T\to\infty} \frac{1}{T} \int_0^T \sum_{k\epsilon L^+(t)} |v_k| \, dt$$

Let

$$Q_k^+(T) = \{t : v_k(t)i_k(t) \geq 0, \quad 0 \leq t \leq T\}$$

Then

$$\overline{\sum_{k\epsilon L^+(t)} |v_k|} = \sum_{k\epsilon L} \lim_{T\to\infty} \frac{1}{T} \int_{Q_k^+(T)} |v_k| \, dt$$

Lemma 6.3.1 then gives

$$\overline{\sum_{k\epsilon L^+(t)} |v_k|} = \frac{1}{2} \sum_{k\epsilon L} \overline{|v_k|} \tag{6.9}$$

Now, since $C^+(t)$ is a subset of C,

$$\overline{\sum_{k\epsilon C^+(t)} |v_k|} \leq \overline{\sum_{k\epsilon C} |v_k|} = \sum_{k\epsilon C} \overline{|v_k|} \tag{6.10}$$

Inequality (6.8), E . (6.9), and Ineq. (6.10) yield the result of the theorem.

The proof of the dual theorem is the dual of the above proof, using result (b) of Corollary 4.4.1 in place of result (a), and using Lemma 6.2.1 in place of Lemma 6.3.1.

Remark 6.1: Consider a dc to dc conversion network whose operation is periodic with period T, and whose inductors have no mutual coupling. Let X be the set of reactances, and let $\hat{W}_k$ be the maximum energy stored by the k^{th} reactance. If the power $v_k i_k$ absorbed by each reactance changes sign not more than 2s times during each period, then

$$\frac{1}{2} \frac{1}{T} \overline{|v_k i_k|} \leq s\hat{W}_k \quad ; \quad k\epsilon X$$

Then the bound given by Theorem 6.1 gives

$$\sum_{k\epsilon X} \hat{W}_k \geq \frac{1}{sT} \frac{G-1}{G} P_0$$

where G is the dc voltage or current gain and P_0 is the dc power delivered to the load.

Since $\hat{W}_k$ is related to the size of the reactance, and T is limited by the switching speed of devices in the network, the above inequality has meaningful design implications.

Remark 6.2: Consider a dc to dc conversion network whose operation is periodic with period T, and whose inductors have no mutual coupling. Let C be the set of capacitors, and $\hat{q}_k$ be the maximum charge in the k^{th} capacitor. Let L be the set of inductors, and $\hat{\lambda}_k$ be the maximum flux-linkage in the k^{th} inductor. If the power $v_k i_k$ absorbed by each reactance changes sign not more than 2s times during each period, then

$$\frac{1}{2}\,\frac{1}{T}\,\overline{|i_k|} \leq s\,\hat{q}_k \quad ; \quad k\epsilon C$$

$$\frac{1}{2}\,\frac{1}{T}\,\overline{|v_k|} \leq s\,\hat{\lambda}_k \quad ; \quad k\epsilon L$$

Now, the size of a reactance is related to the maximum charge or flux-linkage it must store. Then the above facts together with Theorems 6.2 and 6.3 relate the size and number of reactances in a dc to dc conversion network to the period of operation, the dc gain, and the load voltage or current.

Remark 6.3: Theorem 6.2 and Theorem 6.3, which give bounds on the average magnitude of the currents and voltages of the reactances, also imply bounds on the peak currents and voltages of the reactances.

In the next chapter we will relate the dissipation due to losses in the reactances to the current in the reactances. Theorems 6.2 and 6.3 will then be used to extend the relation to the external parameters of the network.

Remark 6.4: Theorem 6.1 implies that if a network has no reactances, then the dc gain must be unity or less. That is, every dc to dc conversion network must include at least one reactance.

Then the types of dc to dc conversion networks might be classed according to the types of reactance they include: capacitors, inductance,

mutual coupling, or any combination of these. The most important of the combinations is the inductor-capacitor network. In the other two combinations the roles of the different reactance types seem to be independent.

The "all capacitor" and "all inductor" (without mutual coupling) networks show a dependence of dc gain on the number of reactances; this is discussed in Chapter VIII. Another characteristic seems to be that there is no efficient way to change the dc gain. This is a disadvantage of these types of circuits when a fair amount of regulation is required.

A network using only the mutual coupling (transformer) property of inductors has a similar problem with regulation. The dc gain can be varied without sacrificing efficiency only by changing the "turns ratio" of the mutual coupling. But this results in quantized regulation.

The following examples will concentrate on the role of the reactances in several dc to dc conversion networks. We will compare their voltage, current, and power with the bounds given by the theorems of this chapter.

Example 6.1: Figure 6.1 show a dc to dc conversion network without inductors.

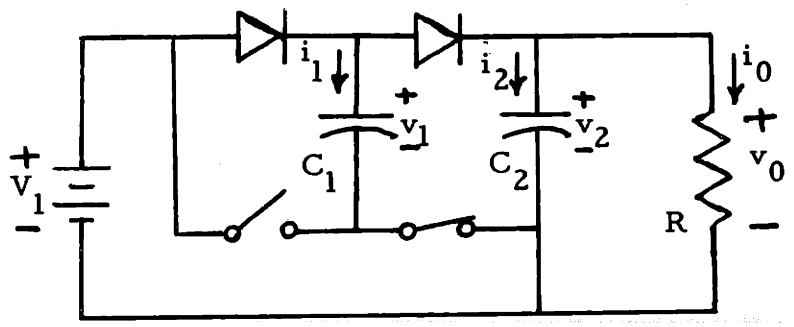


Figure 6.1 Dc to Dc Conversion Network Without Inductors

The switches operate periodically, remaining in the position shown for a time T_1 and in the opposite position for a time T_2. For low output ripple, $RC_2 \gg T_1$. If $T_1 \ll T_2$ and $C_1 \gg C_2$, then $\overline{|i_2|}$ is very small, say ϵ, compared to the load current. The dc voltage gain is $G_v = 2$.

For $V_1=1$ and $R=1$ we have the following parameters:

$$|\bar{v}_0| = 2 \quad ; \quad |\bar{i}_0| = 2 \quad ; \quad P_0 = 4$$

$$\overline{|v_1|} = 1 \quad ; \quad \overline{|i_1|} = 4 \quad ; \quad \overline{|v_1 i_1|} = 4$$

$$\overline{|v_2|} = 2 \quad ; \quad \overline{|i_2|} = \epsilon \quad ; \quad \overline{|v_2 i_2|} = 2\epsilon$$

We compare these figures with the results of the theorems of this chapter:

Theorem 6.1:

$$\frac{1}{2} \sum_{k \epsilon X} \overline{|v_k i_k|} \geq \frac{G_v - 1}{G_v} P_0$$

$$2 + \epsilon \geq 2$$

Theorem 6.2:

$$\frac{1}{2} \sum_{k \epsilon C} \overline{|i_k|} \geq (G_v - 1) |\bar{i}_0|$$

$$2 + \frac{1}{2}\epsilon \geq 2$$

Theorem 6.3:

$$\sum_{k \epsilon C} \overline{|v_k|} \geq \frac{G_v - 1}{G_v} |\bar{v}_0|$$

$$3 \geq 1$$

Example 6.2: Figure 6.2 shows a dc to dc conversion network which has no capacitors. The switches are closed alternately for equal lengths of time. Let the period of the network be T. For low output ripple, $L/R \gg T$. The dc voltage gain is $G_v = 2$.

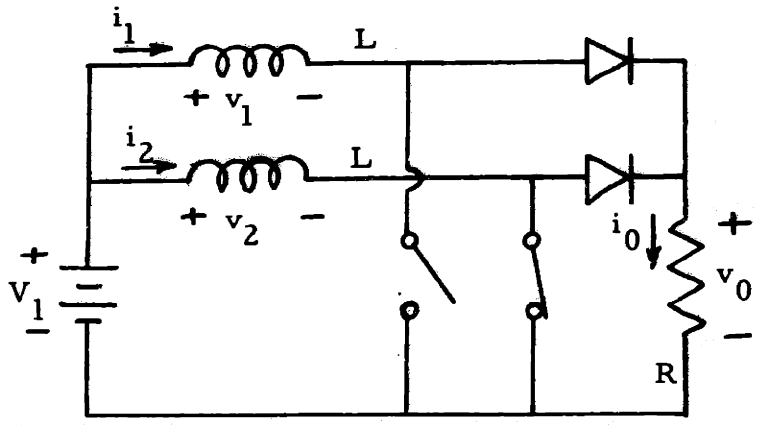


Figure 6.2 Dc to Dc Conversion Network Without Capacitors

For $V_1=1$ and $R=1$, we have the following parameters:

$$|\overline{v_0}| = 2 \quad ; \quad \overline{|i_0|} = 2 \quad ; \quad P_0 = 4$$

$$\overline{|v_1|} = 1 \quad ; \quad \overline{|i_1|} = 2 \quad ; \quad \overline{|v_1 i_1|} = 2$$

$$\overline{|v_2|} = 1 \quad ; \quad \overline{|i_2|} = 2 \quad ; \quad \overline{|v_2 i_2|} = 2$$

Comparing these figures with the theorems of this chapter, we find:

Theorem 6.1:

$$\frac{1}{2}\sum_{k\epsilon X} \overline{|v_k i_k|} \geq \frac{G_v-1}{G_v} P_0$$

$$2 \geq 2$$

Theorem 6.2:

$$\sum_{k\epsilon L} |i_k| \geq (G_v-1)\ \overline{|i_0|}$$

$$4 \geq 2$$

Theorem 6.3:

$$\frac{1}{2}\sum_{k\epsilon L} |v_k| \geq \frac{G_v-1}{G_v}\ |\overline{v_0}|$$

$$1 \geq 1$$

Example 6.3: Figure 6.3 shows a dc to dc conversion network using inductors with mutual coupling.

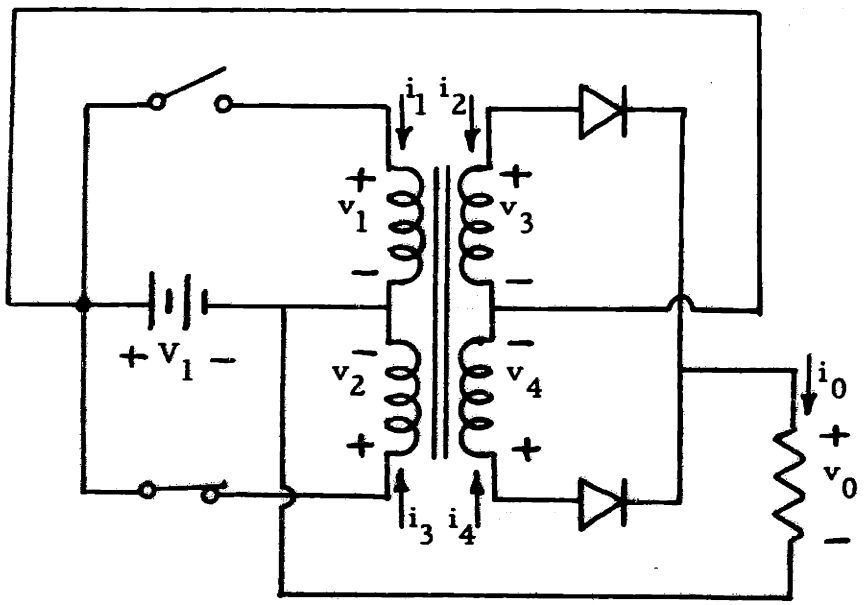


Figure 6.3 Dc to Dc Conversion Network
Using Inductors with Mutual Coupling

The coupling coefficient is unity, and the inductors are large enough to keep the magnetization current reasonable. The switches are closed alternately for equal lengths of time. For a "turns ratio" of n, the dc voltage gain is $G_v = n+1$.

For $V_1=1$, $R=1$, and $n=1$, we have the following parameters:

$$G_v = 2$$

$$|\overline{v_0}| = 2 \quad ; \quad |\overline{i_0}| = 2 \quad ; \quad P_0 = 4$$

$$\overline{|v_k|} = 1 \quad ; \quad \overline{|i_k|} = 1 \quad ; \quad \overline{|v_k i_k|} = 1 \quad ; \quad k=1,2,3,4$$

Compare these figures with the results of the theorems of this chapter.

Theorem 6.1:

$$\frac{1}{2} \sum_{k \in X} \overline{|v_k i_k|} \geq \frac{G_v - 1}{G_v} P_0$$

$$2 \geq 2$$

Theorem 6.2:

$$\sum_{k\epsilon L} \overline{|i_k|} \geq (G_v - 1)\ |\overline{i_0}|$$

$$4 \geq 2$$

Theorem 6.3:

$$\frac{1}{2} \sum_{k\epsilon L} \overline{|v_k|} \geq \frac{G_v - 1}{G_v}\ |\overline{v}_0|$$

$$2 \geq 1$$

Example 6.4: Figure 6.4 shows a dc to dc conversion network using both inductive and capacitive energy storage.

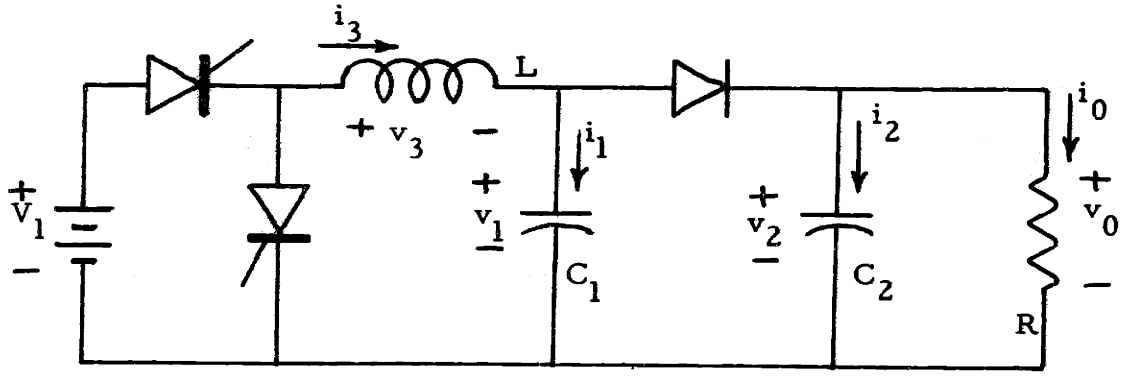


Figure 6.4 Dc to Dc Conversion Network Using Both Inductive and Capacitive Energy Storage

The two SCR's are pulsed alternately and so that both are not on at the same time. Let the period of the network operation be T. For low output ripple, $RC_2 >> T$. For $R >> \sqrt{L/C_1}$, the dc voltage gain is given closely by

$$G_v = \frac{2RC_1}{T} \leq \frac{R}{\pi}\sqrt{\frac{C_1}{L}}$$

For G_v near its maximum for given element values, the voltages across L and C_1 are nearly sinusoidal, and the analysis is easier.

The network parameters are then given by

$$\overline{|v_1|} = \overline{|v_3|} = \frac{2}{\pi}|\overline{v}_0| \; ; \quad \overline{|v_2|} = |\overline{v}_0|$$

$$\overline{|i_1|} = \overline{|i_3|} = 2G_v\overline{|i_0|} \; ; \quad \overline{|i_2|} = 2\overline{|i_0|}$$

$$\overline{|v_1 i_1|} = \overline{|v_3 i_3|} = \frac{1}{2}G_v P_0 \; ; \quad \overline{|v_2 i_2|} = 2P_0$$

For $V_1=1$, $R=10$, $G_v=10$, we have

$$|\overline{v}_0| = 10 \; ; \quad \overline{|i_0|} = 1 \; ; \quad P_0 = 10$$

$$\overline{|v_1|} = 6.3 \; ; \quad \overline{|i_1|} = 20 \; ; \quad \overline{|v_1 i_1|} = 50$$

$$\overline{|v_2|} = 10 \; ; \quad \overline{|i_2|} = 2 \; ; \quad \overline{|v_2 i_2|} = 20$$

$$\overline{|v_3|} = 6.3 \; ; \quad \overline{|i_3|} = 20 \; ; \quad \overline{|v_3 i_3|} = 50$$

We compare these figures with the results of the theorems of this chapter:

Theorem 6.1:

$$\frac{1}{2}\sum_{k\epsilon X}\overline{|v_k i_k|} \geq \frac{G_v-1}{G_v}P_0$$

$$60 \geq 9$$

Theorem 6.2:

$$\frac{1}{2}\sum_{k\epsilon C}\overline{|i_k|} + \sum_{k\epsilon L}\overline{|i_k|} \geq (G_v-1)\,\overline{|i_0|}$$

$$31 \geq 9$$

Theorem 6.3:

$$\sum_{k\epsilon C}\overline{|v_k|} + \frac{1}{2}\sum_{k\epsilon L}\overline{|v_k|} \geq \frac{G_v-1}{G_v}|\overline{v}_0|$$

$$19.5 \geq 9$$

Remark 6.5: Example 6.1 and Example 6.2 show that Theorems 6.1, 6.2, and 6.3 give a greatest lower bound (not for a specific network, but in general).

VII. ELEMENT CHARACTERISTICS AND LIMITATIONS

In this chapter we will consider some models for devices which might be used to realize the elements in a dc to dc conversion network. These models will be used to find a relationship between the element characteristics and limitations and the electrical variables associated with the element: average voltage and current, dc power and ac power, and average power. The relationships will be found in terms of bounds by fixing certain parameters and optimizing others.

Theorem 7.1: If the periodic functions $v(t)$ and $i(t)$ with period T satisfy

(i) $\quad v(t)i(t) \geq 0 \quad ; \quad 0 \leq t \leq T$

(ii) $\quad \bar{v}\,\bar{i} < 0$

where $\bar{v}$ and $\bar{i}$ are the averages of $v(t)$ and $i(t)$, then

$$\hat{v}\,\hat{i} \geq \hat{v}\,|\bar{i}| + \hat{i}\,|\bar{v}|$$

where

$$\hat{v} = \max_{0 \leq t \leq T} |v(t)|$$

$$\hat{i} = \max_{0 \leq t \leq T} |i(t)|$$

Proof: We will put the problem in a form such that it can be treated by Pontryagin's principle for finding an optimum control (see Athans and Falb (2)).

Consider the controls $v(t)$ and $i(t)$ with the restriction that their values be in the set Ω for $0 \leq t \leq T$, where Ω is the region

$$\Omega \left\{ \begin{array}{l} vi \geq 0 \\ |v| < V \\ |i| < I \end{array} \right.$$

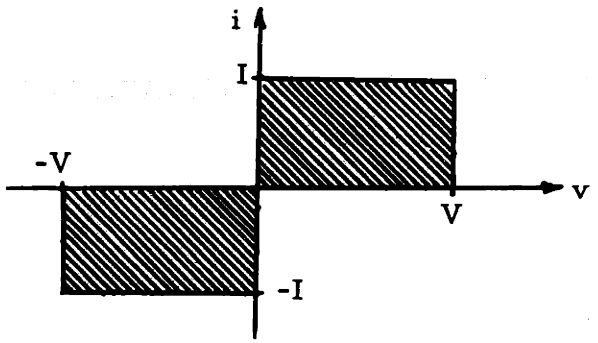


Figure 7.1 Region of Allowable Controls

Case 1: $\bar{i} > 0$. Then $\bar{v} < 0$ in order that $\bar{v}\,\bar{i} < 0$.

Let $\bar{i}$ be fixed and find the minimum $\bar{v}$ which can be obtained for the given restriction on the controls. Then let

$$\dot{x} = i \quad , \qquad x(0) = 0$$

Requiring that

$$x(T) = T\,\bar{i}$$

insures that the average of i :

$$\frac{1}{T}\int_0^T i\,dt$$

attains the desired value.

The average value of v:

$$\bar{v} = \frac{1}{T}\int_0^T v\,dt$$

which must be negative, is to be minimized.

Following the procedure of Pontryagin's principle, we form the Hamiltonian

$$H = L + \langle \underline{p}\,,\, \underline{f} \rangle$$

where L is the integrand of the parameter to be minimized, $\underline{p}$ is a "costate", and $\underline{f}$ is the right hand side of the (vector) state equation. Then

$$H = v + p\,i$$

and the costate equation is

$$\dot{p} = -\partial H/\partial x = 0$$

or

$$p = \text{const}$$

The theory states that the controls v and i satisfying Ω, attaining $\bar{i}$, and minimizing $\bar{v}$ must also minimize H at all times.

Now, if $p \geq 0$, H is minimized by setting $v(t) = -V$, which implies that $i(t) \leq 0$; $0 \leq t \leq T$, which makes it impossible to attain a positive $\bar{i}$, Therefore $p < 0$.

Figure 7.2 shows loci of constant values of H for $p = -V/I$.

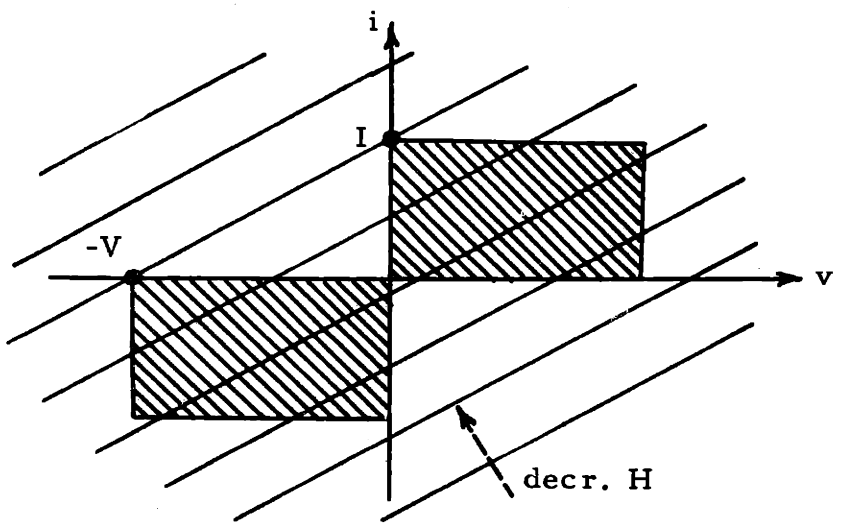


Figure 7.2 Loci of Constant Values of The Hamiltonian for $p = -V/I$

The value of H decreases as the operating point moves toward the upper left. For $p = -V/I$ the locus of $H = -V$ passes through both the points $(-V, 0)$ and $(0, I)$. Then H is minimized for either $(v, i) = (-V, 0)$ or $(v, i) = (0, I)$.

If p is greater or less than $-V/I$, then the slope of the loci of constant H changes so that H is minimized for $(v, i) = (-V, 0)$ or $(v, i) = (0, I)$, respectively. In the first case $\bar{v} = 0$, and in the second $\bar{i} = 0$. In either case $\bar{v}\,\bar{i} = 0$, which does not satisfy the conditions of the theorem.

Then we must have $p = -V/I$, as in Figure 7.2. The desired value of $\bar{i}$ is attained by having $(v, i) = (0, I)$ for part of the interval $[0, T]$, and then $(v, i) = (-V, 0)$ for the remainder of $[0, T]$. If d is the fraction of $[0, T]$ for which $(v, i) = (0, I)$, then

$$d = \bar{i}/I$$

The minimum average value of $\bar{v}$ is then obtained and is given by

$$\bar{v}_{min} = -(1-d)V = -\frac{I-\bar{i}}{I}\,V$$

Since $\bar{v}_{min}$ is a monotonic decreasing function of V, the equation states conversely that V is the minimum bound on $|v|$ for which $\bar{v} = \bar{v}_{min}$ can be attained. If $v(t)$ is other than the optimum, then the maximum v of $|v(t)|$ over $[0, T]$ must exceed V. Therefore we may write

$$\bar{v} \geq -\frac{I-\bar{i}}{I}\,\hat{v}$$

Now, $\bar{v}_{min}$ is also a monotonic decreasing function of I for $I > \bar{i}$, the region for which a solution exists. Then by a similar argument,

$$\bar{v} \geq -\frac{\hat{i}-\bar{i}}{\hat{i}}\,\hat{v}$$

$$\hat{v}\,\hat{i} \geq \hat{v}\,\bar{i} - \bar{v}\,\hat{i}$$

But $\overline{i} > 0$

$\overline{v} < 0$

Then $\hat{v}\,\hat{i} \geq \hat{v}\,|\overline{i}| + \hat{i}\,|\overline{v}|$

which proves the theorem for the case $\overline{i} > 0$, $\overline{v} < 0$.

Case 2: $\overline{v} > 0$, $\overline{i} < 0$. The proof of the theorem for this case is the dual of the proof for Case 1.

Corollary 7.1.1: Consider a periodic operating dc to dc conversion network with load voltage v_0 and load current i_0, with dc voltage gain G_v, and for which there is only one resistor in the dc-active set. Let the voltage and current of this resistor be v and i.

(i) If there is a constraint $|v| \leq V$,

(a) Then the maximum $\hat{i}$ of $|i|$ over a period is bounded by

$$\hat{i} \geq \frac{V\,|i_0|}{V - \beta\,|\overline{v}_0|}$$

where $$\beta = \frac{G_v - 1}{G_v}$$

(ii) If there is a constraint $|i| \leq I$

(b) Then the maximum $\hat{v}$ of $|v|$ over a period is bounded by

$$\hat{v} \geq \frac{I\beta\,|v_0|}{I - |\overline{i}_0|}$$

The dual theorem also holds.

Proof: The result of Theorem 7.1 may be written

$$\hat{i} \geq \frac{\hat{v}\,|\overline{i}|}{\hat{v} - |\overline{v}|}$$

Assume that condition (i) of the Corollary holds. Then

$$\hat{v} = \max |v| \leq V$$

Also, from Theorem 5.7 we have

$$|\bar{v}| \geq \frac{G_v - 1}{G_v} |\bar{v}_0| = \beta |\bar{v}_0|$$

and from Theorem 5.8 we have

$$|\bar{i}| \geq |\bar{i}_0|$$

Then

$$\hat{i} \geq \frac{V |\bar{i}_0|}{V - \beta |\bar{v}_0|}$$

which is result (a) of the Corollary.

Result (b) follows from condition (ii) in a similar manner, solving the result of Theorem 7.1 for $\hat{v}$ rather than $\hat{i}$.

The proof of the dual theorem (involving the dc current gain) is the dual of the above proof.

In the examples of this chapter the units of voltage and current are volts and amperes, unless otherwise specified.

Example 7.1: The specifications of a dc to dc conversion network are

$$G_v = 10$$
$$\bar{v}_0 = 100$$
$$\bar{i}_0 = 1$$

Is it possible to construct the network using only one diode, for which the maximum peak voltage is 200, and not have the diode current exceed 1.5? (There are to be no other resistors in the dc-active set.)

Applying result (a) of Corollary 6.1.1 we have

$$\hat{i} \geq \frac{V |\bar{i}_0|}{V - \beta |\bar{v}_0|}$$

where $$\beta = \frac{G_v - 1}{G_v} = \frac{9}{10}$$

Then $$\hat{i} \geq \frac{200}{200 - 90} \cong 1.8$$

so the diode current must, in fact, exceed 1.5.

Several theorems of Chapter V deal with the dc power and ac power which must be delivered by certain resistors in a dc to dc conversion network. If these resistors are not lossless, one would expect the average power dissipated to be an increasing function of the dc power or ac power delivered. The next several results deal with this question.

Theorem 7.2: If the periodic functions $v(t)$ and $i(t)$ with period T satisfy

(i) $0 \leq R_1 \leq v(t)/i(t) \leq R_2 \quad ; \quad 0 \leq t \leq T$

(ii) $\overline{v\,i} < 0$

then (a) $$\overline{v\,i} \geq \frac{4\sqrt{R_1/R_2}}{(1-\sqrt{R_1/R_2})^2}\,(-\overline{v}\,\overline{i})$$

If condition (i) holds and

(iii) $\overline{v}\,\overline{i} > \overline{v\,i}$

then (b)

$$\overline{v\,i} \geq \frac{4\sqrt{R_1/R_2}}{(1+\sqrt{R_1/R_2})^2}\,(\overline{v}\,\overline{i})$$

Proof: This theorem will also be proved by using Pontryagin's principle. Let

$$r(t) = v(t)/i(t)$$

Then $$\overline{v}\,\overline{i} = \frac{1}{T^2}\int_0^T i\,dt \int_0^T ir\,dt$$

and $$\overline{v\,i} = \frac{1}{T}\int_0^T i^2 r\, dt$$

We state the problem as an optimum control problem: Given the controls i(t) and r(t) which satisfy

$$R_1 \le r(t) \le R_2 \quad ; \quad 0 \le t \le T$$

and the state equations

$$\dot{x}_1 = i \quad ; \quad x_1(0) = 0$$

$$\dot{x}_2 = ir \quad ; \quad x_2(0) = 0$$

we desire to find the controls which attain a given $\bar{v}\,\bar{i} < 0$:

$$x_1(T)\, x_2(T) = T^2 \bar{v}\, \bar{i}$$

and for which $\overline{v\,i}$ is minimized.

Forming the Hamiltonian,

$$H = L + \langle \underline{p}, \underline{f} \rangle$$
$$= i^2 r + p_1 i + p_2 ir$$

where p_1 and p_2 are the costate variables that satisfy

$$\dot{p}_1 = -\partial H/\partial x_1 = 0$$

$$\dot{p}_2 = -\partial H/\partial x_2 = 0$$

and $$\frac{p_1(T)}{p_2(T)} = \frac{x_2(T)}{x_1(T)}$$

Therefore

$$p_1 = \text{const}$$

$$p_2 = \text{const}$$

$$\frac{p_1}{p_2} = \frac{x_2(T)}{x_1(T)} = \frac{T^2 \bar{v}\,\bar{i}}{x_1^2(T)} \triangleq b$$

For each value of r, the value of i must be such that H is minimized. Now H is minimized for

$$\frac{\partial H}{\partial i} = 2ir + p_1 + p_2 r = 0$$

$$i = -\frac{p_1 + p_2 r}{2r} = -\frac{p_2(b+r)}{2r}$$

Substituting this value of i into H, we obtain a Hamiltonian H(r) which is dependent only on r:

$$H(r) = -\frac{(b+r)^2 p_2^2}{4r}$$

This function is plotted for $b = -\sqrt{R_1 R_2}$ and for $b = \sqrt{R_1 R_2}$ in Fig. 7.3

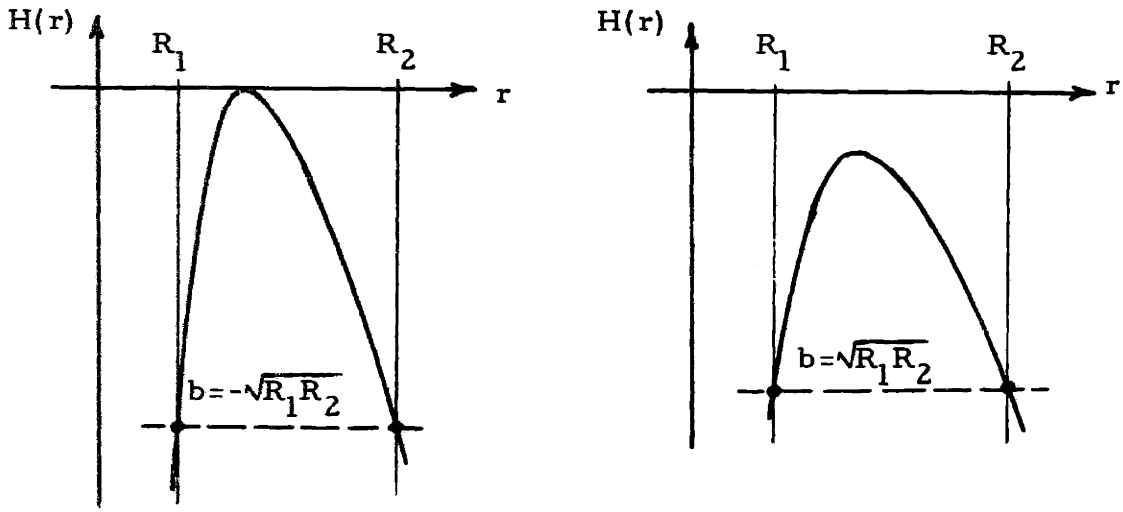


Figure 7.3 Hamiltonian vs. Control r

If $|b| < \sqrt{R_1 R_2}$, the curves shift to the left, and the minimum of H(r) in the interval $[R_1, R_2]$ occurs for $r=R_2$. If $|b| > \sqrt{R_1 R_2}$, the curves shift to the right, and the minimum of H(r) in $[R_1, R_2]$ occurs for $r=R_1$. In either case the control r is constant, and condition (ii) or (iii) of the theorem cannot be satisfied. Therefore $|b| = \sqrt{R_1 R_2}$, and H(r) is minimized for either $r=R_1$ or $r=R_2$, as in Fig. 7.3.

We can now solve for our "target set" $x_1(T)$ and $x_2(T)$:

$$x_1(T) = T\sqrt{\frac{\bar{v}\,\bar{i}}{b}}$$

$$x_2(T) = bx_1(T) = T\sqrt{b\bar{v}\,\bar{i}}$$

(We must take $b = -\sqrt{R_1R_2}$ for $\bar{v}\,\bar{i} < 0$, and $b = \sqrt{R_1R_2}$ for $\bar{v}\,\bar{i} > 0$.) In order to reach this target set, we must have $r=R_1$ for half the time during $[0, T]$, and $r=R_2$ for the other half of the time. We must also have $i=I_1$ when $r=R_1$ and $i=I_2$ when $r=R_2$, where

$$I_1 = \frac{\pm 2\,|\bar{v}\,\bar{i}|}{(R_1R_2)^{1/4}(1-\sqrt{R_1/R_2})}$$

$$I_2 = \pm I_1\sqrt{R_1/R_2} \quad ; \quad \bar{v}\,\bar{i} \gtrless 0$$

For these controls we obtain the minimum average power:

$$\overline{v\,i}_{min} = \frac{4\sqrt{R_1/R_2}}{(1-\sqrt{R_1/R_2})^2}(-\bar{v}\,\bar{i}) \quad ; \quad \bar{v}\,\bar{i} < 0$$

$$\overline{v\,i}_{min} = \frac{4\sqrt{R_1/R_2}}{(1+\sqrt{R_1/R_2})^2}(-\bar{v}\,\bar{i}) \quad ; \quad \bar{v}\,\bar{i} > \overline{v\,i}$$

The equations yield the results of the theorem.

Corollary 7.2.1: If the periodic functions v(t) and i(t) with period T satisfy

(i) $0 \le R_1 \le v(t)/i(t) \le R_2 \quad ; \quad 0 \le t \le T$

(ii) $\overline{v\,i} - \bar{v}\,\bar{i} < 0$

then $$\overline{v\,i} \ge \frac{4\sqrt{R_1/R_2}}{(1-\sqrt{R_1/R_2})^2}(\bar{v}\,\bar{i} - \overline{v\,i})$$

Proof: The conditions of the corollary satisfy conditions (i) and (iii) of Theorem 7.2. Then result (b) of the theorem gives

$$\bar{v}\,\bar{i} \le \frac{(1+\sqrt{R_1/R_2})^2}{4\sqrt{R_1/R_2}}\,\overline{(v\,i)}$$

Therefore $$\bar{v}\,\bar{i} - \overline{v\,i} \le \frac{(1-\sqrt{R_1R_2})^2}{4\sqrt{R_1/R_2}}\,\overline{(v\,i)}$$

which gives the result of the corollary.

The following theorem is an interesting implication of Theorem 7.2. It will not be used later in the thesis, however.

Theorem 7.3: Consider a one-port network of n linear, time-varying resistors $r_k(t)$ which satisfy

$$0 \le R_k' \le r_k(t) \le R_k'' \quad ; \quad k = 1,2,\ldots,n$$

Then the resistance $r_0(t)$ seen at the port must satisfy

$$R_0' \le r_0(t) \le R_0''$$

$$R_0'/R_0'' \ge \min_k [R_k'/R_k'']$$

Proof: Suppose that there is a current source $i_0(t)$ connected to the port. Let the voltage across the current source be $v_0(t)$. Let the average power and dc power absorbed by the k^{th} element be $\bar{P}^k$ and P_{dc}^k. Then Lemma 5.2.1 gives us for the source

$$P_{dc}^0 = \sum_{k=1}^{n} (-P_{dc}^k)$$

and

$$-\bar{P}^0 = \sum_{k=1}^{n} \bar{P}^k \qquad (7.1)$$

Now Theorem 7.2 gives

$$(-P_{dc}^{k}) \leq a_k \bar{P}^k \quad ; \quad k=1,2,\ldots,n$$

where $$a_k = \frac{(1-\sqrt{R_k'/R_k''})}{4\sqrt{R_k'/R_k''}} \quad ; \quad k=0,1,2,\ldots,n$$

Therefore $$P_{dc}^{0} \leq \sum_{k=1}^{n} a_k \bar{P}^k \tag{7.2}$$

Now suppose that the $r_k(t)$ are varied periodically so that $r_0(t) = R_0'$ for a given length of time and $r_0(t)=R_0''$ for an equal length of time. Then $r_0(t)$ satisfies the optimum control for Theorem 7.2. Let $i_0(t)$ be chosen so that it satisfies the optimum control of Theorem 7.2. Then the equality of result (a) of Theorem 7.2 holds, giving the following value of P_{dc}^{0}:

$$P_{dc}^{0*} = \frac{(1-\sqrt{R_0'/R_0''})}{4\sqrt{R_0'/R_0''}} (-\bar{P}^{0*}) = a_0(-\bar{P}^{0*})$$

and using Eq. (7.1),

$$P_{dc}^{0*} = \sum_{k=1}^{n} a_0 \bar{P}^{k*} \tag{7.3}$$

We will prove the theorem by contradiction. Assume R_0'/R_0'' $< \min_k [R_k'/R_k'']$. Since a_k is a monotonic decreasing function of (R_k'/R_k''), we then have

$$a_0 > a_k \quad ; \quad k=1,2,\ldots,n \tag{7.4}$$

Since $\bar{P}^k \geq 0$; $k=1,2,\ldots,n$, Eq. (7.3) and Ineq. (7.4) give

$$P_{dc}^{0*} > \sum_{k=1}^{n} a_k \bar{P}^{k*}$$

But this contradicts Ineq. (7.2). Therefore we must have

$$R_0'/R_0'' \geq \min_k [R_k'/R_k''] \qquad \text{Q.E.D.}$$

This theorem is also a result of a more general theorem by Kawakami (5). It follows from the fact that (R_k'/R_k'') is a monotonic decreasing function of the "figure of merit" given by Kawakami. The proof above has been included as an interesting application of the concept of dc power.

Example 7.2: The specifications for a dc to dc conversion network are

$$G_v = 10$$

$$P_0 = 100$$

It is desired to construct the network using one transistor and one diode, both of which can be modeled by linear, time-varying resistors which satisfy $0.1 \leq r(t) \leq 100$ K. What is the best efficiency which the network can possibly have?

Let $-P_{ac}^1$ be the ac power delivered by the transistor, and let $-P_{dc}^2$ be the dc power delivered by the diode. Theorem 5.4 and Corollary 5.4.1 give us

$$-P_{dc}^2 \geq \frac{G_v - 1}{G_v} P_0 = 80$$

$$-P_{ac}^1 \geq \frac{G_v - 1}{G_v} P_0 = 80$$

Let $\bar{P}^1$ and $\bar{P}^2$ be the average power dissipated by the transistor and the diode. Theorem 7.2 and Corollary 7.2.1 give us

$$\bar{P}^2 \geq \frac{4\sqrt{R_1/R_2}}{(1-\sqrt{R_1/R_2})^2} \quad (-P_{dc}^2)$$

$$\bar{P}^1 \geq \frac{4\sqrt{R_1/R_2}}{(1-\sqrt{R_1/R_2})^2} \quad (-P_{ac}')$$

where $R_1 = 0.1$ and $R_2 = 100K$. Then

$$\bar{P}^2 \geq 0.32$$

$$\bar{P}^1 \geq 0.32$$

Define the network efficiency as

$$\eta = \frac{P_0}{P_0+\bar{P}^1+\bar{P}^2} \leq 99.2\%$$

The proof of Theorem 6.2 gives us the optimum voltage and current in the devices (to approach the 99.2% efficiency): The peak voltage in both transistor and diode is 180 and the peak current in both transistor and diode is 1.8.

The above analysis did not account for switching losses and other losses. Also the model for the transistor and diode was not very good; the "off" state is not modeled well by a 100K resistor, and the breakdown voltages were not accounted for. The following propositions consider better models.

Proposition 7.1: Consider a device which has the time-varying characteristic shown in Fig. 7.4. The characteristic of the device alternates between the dashed and solid curves. The slope of the dashed curve is $1/R$.

If the maximum average power which the device may dissipate is P, and if $V^2/R \geq 300\ P$ then the bound on the ac power $-P_{ac}$ which the

device delivers is given to within 10% by

$$-P_{ac} \leq \frac{2}{9} V\sqrt{3P/R} - P$$

The equality holds when the operating point is at (V, 0) for two-thirds of the time and at (RI, I) for one-third of the time, where

$$I = \sqrt{3P/R}$$

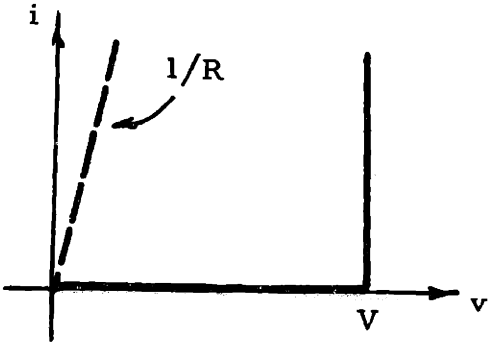


Figure 7.4 Time-Varying v-i Characteristic

Notice that the bound on $(-P_{ac}/P)$ is a monotonic decreasing function of P. This indicates that if a given total amount of ac power is to be delivered, the "efficiency" is always increased by using more of the devices, each device delivering less ac power and dissipating less average power. The ac power delivered per watt dissipated increases without bound as the number of devices increases.

Outline of Proof: It is assumed that the optimum operation is for the operating point to remain at (V, 0) for a fraction (1-d) of the time and at (RI, I) for a fraction d of the time, for some d and I.

Then d is chosen as $d = P/(RI^2)$ so that $P=dRI^2 = \overline{v\,i}$.

To simplify the solution, the approximation is made that $V \geq 10RI$. (This will be true if $V^2/R \geq 300P$.) Then the average voltage $\bar{v}$ is about (1-d)V, and the average current $\bar{i}$ is dI. Maximizing

$-P_{ac} = \overline{v}\,\overline{i} - P \tilde{=} d(i-d)\,VI - P$ over I (and corresponding d) gives the result of the proposition.

Example 7.3: The characteristic of a transistor is approximated by Fig. 7.4, where $V = 100$ and $R = 1/8$. The value of R takes into account dissipation due to the base drive. The maximum power dissipation of the transistor is 10. If the "switching losses" are known to be 5, then the "conductance loss" is limited to $P = 5$. What is the maximum ac power which the transistor can deliver?

From Proposition 7.1 we have

$$(-P_{ac})_{max} = \frac{2}{9} V \sqrt{3P/R} - P$$

$$= 235$$

To realize this, the peak current must be

$$I = \sqrt{3P/R} = 11$$

Proposition 7.2: Consider a device which has the characteristic shown in Fig. 7.5

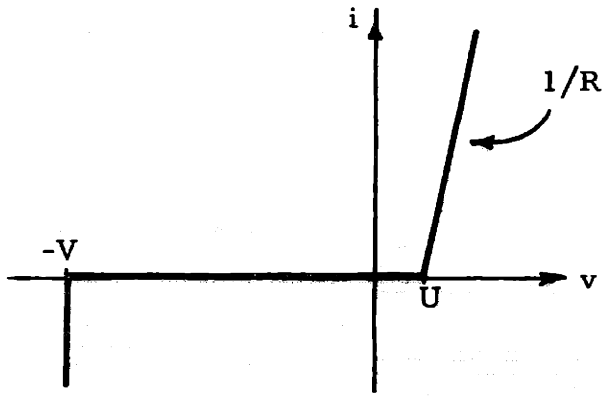


Figure 7.5 v-i Characteristic

The finite slope of the graph is $1/R$.

If the maximum average power which the device may dissipate is P, and if

$$V \geq 40\,U$$

and

$$\frac{1}{4} \leq \frac{U^2}{PR} \leq 15$$

then the bound on the dc power $-P_{dc}$ which the device delivers is given to within 20% by

$$-P_{dc} \leq \frac{V}{U} \frac{(\sqrt{aP}+1)P}{(2\sqrt{aP}+1)^2}$$

where

$$a = \frac{R}{2U^2}$$

The equality holds when the operating point is at $(-V, 0)$ for $(1-d)$ of the time and at $(U + RI, I)$ for d of the time, where

$$I = \sqrt{2P/R}$$

and

$$d = \frac{P}{2P + UI}$$

Notice that the bound on $(-P_{dc}/P)$ is a monotonic decreasing function of P. This indicates that if a given total amount of dc power is to be delivered, the "efficiency" is always increased by using more devices. The dc power delivered per watt dissipated cannot exceed V/U, however.

Outline of Proof: It is assumed that the optimum operation is for the operating point to remain at $(-V, 0)$ for a fraction $(1-d)$ of the time and at $(U + RI, I)$ for a fraction d of the time, for some d and I.

Then d is chosen as $d = P/(UI + RI^2)$ so that $P = d(UI + RI^2) = \overline{vi}$.

To simplify the solution, the approximation is made that $V \geq 10(U+RI)$. (This will be true if the conditions of the theorem are satisfied.) Then the average voltage $\bar{v}$ is about $-(1-d)V$, and the average current $\bar{i}$ is

dI. Maximizing $-P_{dc} = \bar{v}\,\bar{i} \cong d(1-d)VI$ over I (and corresponding d) gives a polynomial to solve for the optimum I.

If $1/4 \leq U^2/PR \leq 15$, this polynomial is approximated by a quadratic, giving a simple expression for the optimum I. The result of the theorem is given by the $-P_{dc}$ for this (approximation of) the optimum I.

Example 7.4: The characteristic of a diode is approximated by Fig. 7.5, where $V = 200$, $U = 0.7$, and $R = 0.04$. The maximum power dissipation is $P = 2$.

It is desired to use several of these diodes in the construction of a dc to dc converter with the following specifications:

$$G_v = 5$$

$$P_0 = 500$$

What is the smallest number of diodes that can be used. What is the least dissipation for this number?

By Proposition 7.2 the dc power $-P_{dc}^k$ delivered by each diode is bounded by

$$-P_{dc}^k \leq \frac{V}{U} \frac{(\sqrt{aP} + 1)P}{(2\sqrt{aP} + 1)^2} \tag{7.5}$$

where $$a = \frac{R}{2U^2} = 0.04$$

Then $$-P_{dc}^k \leq 300 \tag{7.6}$$

The peak current to realize $-P_{dc}^k = 300$ is

$$I = \sqrt{2P/R} = 10$$

and the duty cycle is

$$d = P/(2P + UI) = 2/11$$

Now, Theorem 5.4 gives the bound on the total dc power delivered:

$$\sum_{k=1}^{n} (-P_{dc}^{k}) \geq \frac{G_v - 1}{G_v} P_0 = 400$$

Considering Ineq. (7.6), we must have

$$\boxed{n \geq 2}$$

If $n=2$, then the $(-P_{dc}^{k})$ for each diode must be 200. Inequality (7.5) is difficult to solve in terms of P, but a graphical solution gives for

$$-P_{dc}^{k} = 200,$$

$$\overline{P}^{k} = P \geq 1.2 .$$

Then for $n=2$ the total dissipation in the diodes is

$$\sum_{k=1}^{2} \overline{P}^{k} \geq \boxed{2.4} \text{ watts}$$

In the limit as $n \to \infty$, the $\overline{P}^{k} \to 0$ and $-P_{dc}^{k} \to 0$, and the bound on $\overline{P}^{k}$ approaches

$$\overline{P}^{k} = P \geq \frac{U}{V} (-P_{dc}^{k})$$

Then for $n \to \infty$ the total dissipation in the diodes is

$$\sum_{k=1}^{\infty} \overline{P}^{k} \geq \frac{U}{V} \sum_{k=1}^{\infty} (-P_{dc}^{k})$$

$$\geq \frac{U}{V} \frac{G_v - 1}{G_v} P_0 = \boxed{1.4} \text{ watts}$$

This example has ignored bounds on the average voltage and average current given by Theorems 5.7 and 5.8, which must also be satisfied. For instance, for $-P_{dc}^{k} = 200$, in order to realize $\overline{P}^{k} = P = 1.2$ the average

current in the diode must be $\bar{i} = dI = 1.19$. Then if $n=2$, and the output current is $\bar{i}_0=3$, Theorem 5.8 says $\bar{P}^k=1.2$ cannot be realized.

Theorem 7.4 (Leine (7)): If $f(v,i,t) = 0$, then

$$-(\overline{v\,i} - \bar{v}\,\bar{i}) \leq \max_{\substack{(v_1,i_1)\in S \\ (v_2,i_2)\in S}} \left[\frac{1}{4}(v_2-v_1)(i_1-i_2)\right]$$

where S is the set of pairs (v,i) which satisfy $f(v,i,t) = 0$ for some t.

The equality holds for the operating point at (v_1,i_1) half the time and at (v_2,i_2) half the time.

This is a restatement of condition 2) given in Chapter III. It is included here for completeness. The paper by Leine (7) gives an algorithm for finding the bound for a given nonlinear characteristic.

Example 7.5: It is desired to construct a low-power dc to dc converter using a tunnel diode. The specifications of the converter are

$$G_v = 2$$
$$v_0 = 300 \text{ mv}$$
$$i_0 = 0.5 \text{ ma}$$

The v-i characteristic of the tunnel diode to be used is shown in Fig. 7.6.

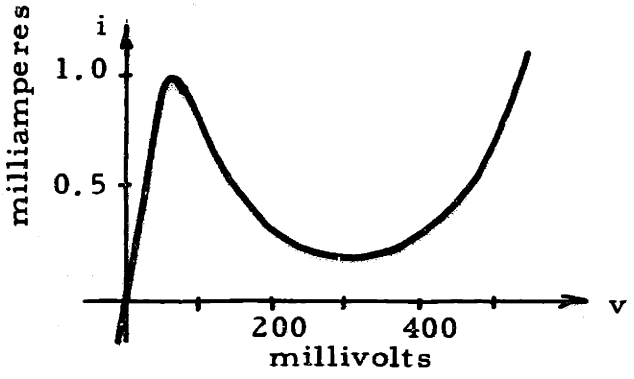


Figure 7.6 v-i Characteristic of Tunnel Diode

First we shall apply some theorems of Chapter V to see if operating points on the characteristic can be found to satisfy the theorems.

Theorem 5.6 requires that

$$|\bar{i}| \geq (G_v - 1)\,|\bar{i}_0| \;=\; 0.5 \text{ ma}$$

This can be satisfied if the operating point (v, i) is at (50 mv, 1.0 ma) half the time. Now, Corollary 5.4.2 requires

$$|\bar{v}\ \bar{i}| \geq \frac{G_v - 1}{G_v}\,|\bar{v}_0\ \bar{i}_0| \;=\; 75\ \mu\text{w}$$

For $|\bar{i}| = 0.5$ ma,

$|\bar{v}| \geq 150$ mv.

This can be satisfied if the operating point is at (300 mv, 0.2 ma) for half the time. So it appears that the tunnel diode might be suitable for this application.

Let us now check with Corollary 5.4.1. This requires that

$$-P_{ac} \geq \frac{G_v - 1}{G_v}\,|\bar{v}_0\ \bar{i}_0| \;=\; 75\ \mu\text{w}$$

Now, Theorem 7.3 states that

$$-P_{ac} \leq \max_{\substack{(v_1, i_1)\in S \\ (v_2, i_2)\in S}} \left[\frac{1}{4}(v_2 - v_1)(i_1 - i_2)\right]$$

A little trial-and-error finds the values $(v_1, i_1)=(50, 1.0)$ and $(v_2, i_2)=(400, 0.3)$. then

$$-P_{ac} \leq 62.5\ \mu\text{w}$$

and the tunnel diode, by itself, is not compatible with the specifications for the converter.

We turn our attention now to the reactances in a dc to dc conversion network. Unlike resistors, the average power dissipated by a reactance is not related only to the power it handles (the rate at which it stores and unstores energy). This will be illustrated in the following remark.

Remark 7.1: Consider a dc to dc conversion network which includes n reactances, has a dc voltage source at the input, has a dc voltage gain G_v, and delivers a dc power P_0 to the load. Then Theorem 6.1 gives

$$\frac{1}{2} \sum_{k \epsilon X} |\overline{v_k i_k}| \geq \frac{G_v - 1}{G_v} P_0$$

where X is the set of reactances. We also have

$$\overline{|v_k i_k|} \leq \hat{v}_k \, \overline{|i_k|} \quad ; \quad k \epsilon X$$

where $$\hat{v}_k = \max_t |v_k(t)| \quad ; \quad k \epsilon X$$

Suppose that $$\hat{v}_k \leq V \quad ; \quad k \epsilon X$$

Then $$\sum_{k \epsilon X} |i_k| \geq \frac{2}{V} \frac{G_v - 1}{G_v} P_0$$

Suppose that each reactance has an equivalent series resistance of R. Let the average power dissipated in the k^{th} reactance due to R be $\overline{P}^k$. Then

$$\overline{P}^k = R \overline{i_k^2} \geq R(\overline{|i_k|})^2 \quad ; \quad k \epsilon X$$

$$\sum_{k \epsilon X} \overline{P}^k \geq R \sum_{k \epsilon X} (\overline{|i_k|})^2 \geq \frac{R}{n} \left[\sum_{k \epsilon X} |i| \right]^2$$

$$\geq \frac{4R}{nV^2} \left[\frac{G_v - 1}{G_v} P_0 \right]^2 .$$

Evidentally the dissipation decreases for greater V; that is, the network can be more efficient if the reactances are operated at a higher voltage. However, for a given G_v, v_0, and i_0, the dissipation cannot be made arbitrarily small by operation the reactances at an arbitrarily high voltage.

It appears, then, that Theorem 6.2 and Theorem 6.3 are better suited for obtaining a bound on the power dissipated in the reactances.

Theorem 7.5: Consider a dc to dc conversion network which includes n reactances, has a dc voltage source at the input, has a dc voltage gain G_v, and has a load current i_0. If each reactance has an equivalent series resistance of R, then the total average power dissipated in the reactances is bounded by

(a) $$\sum_{k\epsilon X} \bar{P}^k \geq \frac{R}{n} (G_v-1)^2 |\bar{i}_0|^2$$

If the network includes no inductors, then

(b) $$\sum_{k\epsilon C} \bar{P}^k \geq \frac{4R}{n} (G_v-1)^2 |\bar{i}_0|^2$$

Proof: If $\bar{P}^k$ is the average power dissipated in the k^{th} reactance, then

$$\sum_{k\epsilon X} \bar{P}^k = \sum_{k\epsilon X} R\,\bar{i_k^2} \geq R \sum_{k\epsilon X} \overline{|i_k|}^2 \geq \frac{R}{n}\left[\sum_{k\epsilon X} \overline{|i_k|}\right]^2$$

But Theorem 6.2 implies

$$\sum_{k\epsilon X} \overline{|i_k|} \geq (G_v-1)\,|\bar{i}_0|$$

which yields result (a).

If the network includes no inductors, Theorem 6.2 implies

$$\sum_{k\epsilon C} \overline{|i_k|} \geq 2(G_v - 1)\,|\overline{i}_0|$$

which yields result (b).

Theorem 7.6: Consider a dc to dc conversion network which includes n reactances, has a dc current source at the input, has a dc current gain G_i, and has a load current i_0. If each reactance has an equivalent series resistance of R, then the total average power dissipated in the reactances is bounded by

(a) $$\sum_{k\epsilon X} \overline{P}^k \geq \frac{R}{n}\left[\frac{G_i - 1}{G_i}\right]^2 |\overline{i}_0|^2$$

If the network includes no inductors, then

(b) $$\sum_{k\epsilon C} \overline{P}^k \geq \frac{4R}{n}\left[\frac{G_i - 1}{G_i}\right]^2 |\overline{i}_0|^2$$

Proof: If $\overline{P}^k$ is the average power dissipated in the k^{th} reactance, then

$$\sum_{k\epsilon X} \overline{P}^k = \sum_{k\epsilon X} R\,\overline{i_k^2} \geq R \sum_{k\epsilon X} (\overline{|i_k|})^2 \geq \frac{R}{n}\left[\sum_{k\epsilon X} \overline{|i_k|}\right]^2$$

But the dual of Theorem 6.3 implies

$$\sum_{k\epsilon X} \overline{|i_k|} \geq \frac{G_i - 1}{G_i}\,|\overline{i}_0|$$

which yields result (a).

If the network includes no inductors, then the dual of Theorem 6.3 implies

$$\sum_{k\epsilon C} \overline{|i_k|} \geq 2\,\frac{G_i - 1}{G_i}\,|\overline{i}_0|$$

which yields result (b).

Example 7.6: It is desired to construct a dc to dc converter which includes no inductors, has a dc voltage source at the input, and has the following specifications:

$$G_v = 4$$

$$\bar{i}_0 = 2$$

If the four capacitors used in the construction each have an equivalent series resistance

$$R = 0.06$$

find a bound on the power dissipated in the capacitors.

Result (b) of Theorem 6.4 gives

$$\sum_{k \in C} \bar{P}^k \geq \frac{4R}{n} (G_v - 1)^2 |\bar{i}_0|^2 \cong 2.2$$

Compare this with the dissipated power of 13 in Example 1.1. There has been no statement that Theorem 7.4 or Theorem 7.5 gives a greatest lower bound, but networks can be constructed which come close to realizing the lower bound. When operated at the proper frequency, a network of the type in Example 5.1 comes close to doing this, for example.

VIII. NETWORKS WITH ONE TYPE OF REACTANCE

Dc to dc conversion networks which include only one type of reactance—inductors or capacitors—possess several distinctive properties. Some of these were discussed in Remark 6.4. This chapter will initiate an investigation of a conjecture (not yet proved) that the dc gain is limited by the number of reactances. This seems to be the case, more specifically, for the dc voltage gain when a dc voltage source is at the input, and for the dc current gain when a dc current source is at the input.

Consider a set of n capacitors with value C_k, where $C_1 << C_2 << \ldots << C_n$. Let these capacitors (initially discharged) be connected in various consecutive configurations with a dc voltage source (battery) of value 1. Suppose that the maximum voltage that can be generated in this manner is V_n.

Now consider a set of $(n+1)$ capacitors with $C_1 << C_2 << \ldots << C_{n+1}$ and a battery of voltage 1. By repeatedly operating with the first n capacitors as above, capacitor $(n+1)$ can be charged (almost) to a value of V_n. Let the voltage on capacitor k be v_k. We have $v_{n+1}=V_n$. Now put capacitor $(n+1)$ in series with the battery, and charge capacitor n. Since $C_n << C_{n+1}$, the v_{n+1} remains nearly V_n, and v_n becomes nearly (V_n+1). If capacitor n, capacitor $(n+1)$, and the battery are now put in series we have generated a voltage twice (V_n+1). The voltage can be doubled in this manner by charging successively each of the smaller capacitors. The final voltage will then be $2^n(V_n+1)$.

There is no proof that this is the highest voltage which can be attained by $(n+1)$ capacitors related as described or for $(n+1)$ capacitors

in general. However, if it is the highest voltage, it would imply that the maximum dc voltage gain $G_{max}(n+1)$ which a dc to dc conversion network with a voltage source at the input can achieve with $(n+1)$ capacitors and no inductors is given by

$$G_{max}(n+1) = 2^n[G_{max}(n) + 1] \qquad (8.1)$$

where $G_{max}(0) = 1$

There is some indication that a dc to dc conversion network using no capacitors or mutual coupling will also display the restriction given by Eq. (8.1). It is true at least for the case $n=1$, as is proved by the following theorems.

Theorem 8.1: Consider a dc to dc conversion network which consists of linear (time-varying) resistors, one linear capacitor, and a dc voltage source. If G_v is the dc voltage gain, then

$$G_v \leq 2$$

Proof: Let the network seen from the terminals of the capacitor be replaced by the Thevenin equivalent, as shown in Fig. 8.1

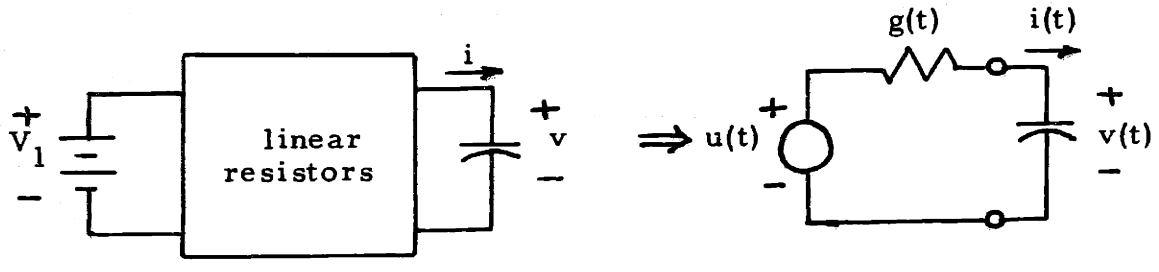


Figure 8.1 Thevenin Equivalent

The "driving point conductance" $g(t)$ is always positive, and the "open circuit voltage" $u(t)$ is bounded by

$$|u(t)| \leq |V_1| \quad ; \quad t \geq 0$$

as may be shown from Corollary 4.4.1. The first step is to show that $\overline{|v|} \leq V_1$.

For simplicity let the system be scaled so the value of the capacitor is unity. Then the constitutive relation is

$$\frac{dv}{dt} = i$$

We have from the Thevenin equivalent

$$i = g(u-v)$$

Then

$$\frac{dv}{dt} = g(u-v)$$

$$v(t) = b(t,0)v(0) + \int_0^t b(t,\tau)g(\tau)u(\tau)\,d\tau$$

where

$$b(t,\tau) \triangleq e^{-\int_\tau^t g(\sigma)\,d\sigma}$$

Then

$$|v(t)| \leq b(t,0)|v(0)| + |V_1| \int_0^t g(\tau)b(t,\tau)\,d\tau$$

$$= b(t,0)|v(0)| + |V_1|[1 - b(t,\tau)]$$

But

$$0 \leq b(t,\tau) \leq 1 \quad ; \quad \tau < t$$

Therefore

$$|v(t)| \leq b(t,0)|v(0)| + |V_1|$$

$$\overline{|v(t)|} \triangleq \lim_{T\to\infty} \frac{1}{T}\int_0^T |v(t)|\, dt$$

$$\leq \lim_{T\to\infty} \frac{1}{T}\int_0^T [\, b(t,0)\, |v(0)| + |V_1|\,]\, dt$$

Now, for t greater than some finite t_1, we must have

$$\int_0^t g(\sigma)\, d\sigma \geq a\, t \quad ; \quad a > 0$$

Otherwise $\overline{g} = 0$, and we cannot satisfy Theorem 6.2, which requires

$$\overline{|i|} \geq 2\,(G_v - 1)\,|\overline{i}_0| > 0$$

Then for $t > t_1$

$$b(t,0) \leq e^{-a\,t}$$

and $$\overline{|v(t)|} \leq \lim_{T\to\infty} \frac{1}{T}\int_0^T [\, e^{-a\,t}|v(0)| + |V_1|\,]\, dt$$

$$= |V_1|$$

With this estimate on $\overline{|v(t)|}$ we can get a bound on the output voltage v_0 in terms of $|V_1|$. A simple application of Corollary 4.4.1 gives

$$|v_0(t)| \leq |V_1| + |v(t)|$$

$$|\overline{v}_0| \leq \overline{|v_0|} \leq |V_1| + \overline{|v|} \leq 2|V_1|$$

Now $$G_v \triangleq |\overline{v}_0|/|V_1| \leq 2$$ Q.E.D.

It should be clear that the theorem holds when the capacitor and resistors are nonlinear. The development to show $\overline{|v(t)|} \leq |V_1|$ is more difficult then.

Theorem 8.2: Consider a dc to dc conversion network which consists of resistors, one inductor, and a dc voltage source. If G_v is the dc voltage gain, then

$$G_v \leq 2$$

Proof: Let the voltage of the dc voltage source be V_1, and let the inductor voltage and current be v and i. Define the sets of time

$$Q^+(T) = \{t : v(t)i(t) \geq 0 \ , \ 0 \leq t \leq T\}$$

$$Q^-(T) = \{t : v(t)i(t) < 0 \ , \ 0 \leq t \leq T\}$$

Let v_0 be the load voltage. A simple application of Corollary 4.4.1 shows

$$|v_0(t)| \leq |V_1| \quad ; \quad t \epsilon Q^+(T) \tag{8.2}$$

$$|v_0(t)| \leq |V_1| + |v(t)| \quad ; \quad t \epsilon Q^-(T) \tag{8.3}$$

A similar application of Corollary 4.4.1 shows

$$|v(t)| \leq |V_1| \quad ; \quad t \epsilon Q^+(T) \tag{8.4}$$

Now, $$\overline{|v_0|} \triangleq \lim_{T \to \infty} \frac{1}{T} \int_0^T |v_0| dt$$

$$= \lim_{T \to \infty} \frac{1}{T} \int_{Q^+(T)} |v_0| dt + \lim_{T \to \infty} \frac{1}{T} \int_{Q^-(T)} |v_0| \, dt$$

Inequalities (8.2) and (8.3) then give

$$\overline{|v_0|} \leq |V_1| + \lim_{T \to \infty} \frac{1}{T} \int_{Q^-(T)} |v| \, dt \tag{8.5}$$

But Lemma 6.3.1 states

$$\lim_{T\to\infty} \frac{1}{T} \int_{Q^-(T)} |v|dt = \lim_{T\to\infty} \int_{Q^+(T)} |v|dt$$

Then Ineq. (8.4) gives

$$\lim_{T\to\infty} \frac{1}{T} \int_{Q^-(T)} |v|dt \leq |V_1|$$

and so with Ineq. (8.5) we have

$$\overline{|v_0|} \leq 2\,|V_1|$$

But

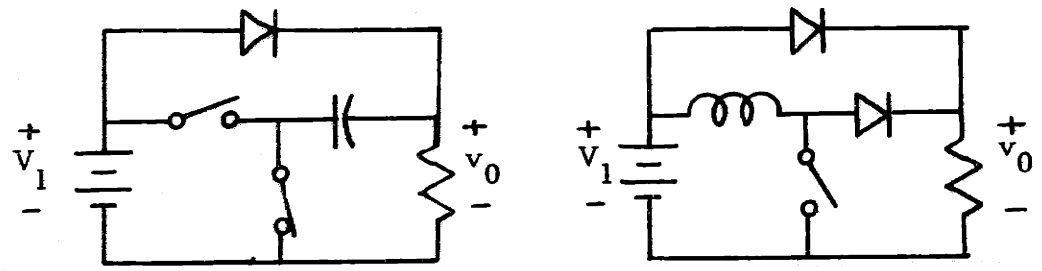
$$|\bar{v}_0| \leq \overline{|v_0|} \leq 2\,|V_1|$$

and

$$G_v \triangleq |\bar{v}_0|/|V_1| \leq 2$$

which is the desired result.

Example 8.1: Figure 8.2 shows two dc to dc conversion networks, which meet the requirements of Theorems 8.1 and 8.2, respectively.



(a) (b)

Figure 8.2 Dc to dc Conversion Networks Using Only One Reactance

Consider the network using the capacitor. With the switches in the position shown, the capacitor is charged instantaneously, in theory. The position of the switches then reverses and applies a voltage of $2V_1$ across

the load. As the period of operation approaches zero, and the ratio of charge to discharge time approaches zero, the dc voltage gain approaches two.

Consider the network using the inductor. As the duty cycle of the switch approaches unity, the current in the inductor becomes arbitrarily large, and the average voltage across the load approaches $2V_1$.

Remark 8.1: The peak deviation of the load voltage from the average load voltage cannot be made arbitrarily small in a dc to dc conversion network described in Theorem 8.1 or Theorem 8.2 (unless the dc voltage gain approaches unity). This is because the reactance must receive power from the source at some time. During this time the load voltage cannot exceed the source voltage, as can be shown from Corollary 4.4.1.

In the case of the network with one capacitor, the ac power delivered to the load can still be made arbitrarily small. This is done by letting the charging time of the capacitor approach zero.

Remark 8.2: Theorem 8.2 does not hold when (all other conditions remaining the same) the dc current gain is considered instead of the dc voltage gain. The network in Fig. 5.7 is a counter-example, showing that the dc current gain is not bounded, although there is one inductor and no capacitors.

IX. SUMMARY

Brief statements of the major results of the thesis are assembled here for convenience. The summary is designed to be understandable by itself, given the definitions in the thesis. However, a complete listing of the conditions is not always given in order to keep the presentation simple.

The symbols used below have the following meanings:

$\{\phi_k\}$, $\{\theta_k\}$: flow, tension. (Def. 4.5, Def. 4.6)

v_0, i_0 : load voltage, load current.

G_v, G_i : dc voltage gain, dc current gain. (Def. 2.7)

$\bar{P}^k$, P^k_{dc}, P^k_{ac} : average, dc, and ac power absorbed by the k^{th} element. (Def. 2.9, Def. 2.10)

P_0 : dc power delivered to the load.

R_{dc}, R_{ac} : set of resistors in the dc-active set, in the ac-active set. (Def. 5.1)

S', S'' : primary set, secondary set. (Def. 5.3)

C, L, X : set of capacitors, inductors, reactances in the network.

Theorems in Chapters V, VI, VII, and VIII apply to a dc to dc conversion network, which is defined as follows: A two-port network together with a dc source at the input and a linear, time-invariant resistor (load) at the output; the two-port network includes only passive resistors (may be nonlinear and/or time-varying) and time-invariant inductors and capacitors (may be nonlinear, and inductors may have mutual coupling); either the dc voltage gain or the dc current gain of the network is greater than unity.

Many of the theorems in the thesis have two parts which are duals. In these cases only one part will be stated.

Thm. 4.1 (p. 24) : $\sum_{k=1}^{n} \theta_k \phi_k = 0$ (Result not new.)

Thm. 4.4 (p. 25) : If $\theta_k \phi_k \geq 0 \quad ; \quad k \epsilon S_4$

then $\sum_{j \epsilon S_1} |\theta_j| \sum_{k \epsilon S_2} |\phi_k| - \sum_{k \epsilon S_2} \theta_k \phi_k + \sum_{k \epsilon S_3} |\theta_k \phi_k| \geq 0$

Cor. 4.4.1 (p. 28) : If $\theta_k \phi_k < 0 \quad ; \quad k \epsilon S_1$

$\theta_k \phi_k \geq 0 \quad ; \quad k \epsilon S_2$

then $|\theta_k| \leq \sum_{j \epsilon S_1} |\theta_j| \quad ; \quad k \epsilon S_2$

Thm. 4.5 (p. 30) : If $\theta_k \phi_k \geq 0 \quad ; \quad k \epsilon S_3, S_4$

$|\theta_k| > \sum_{j \epsilon S_1} |\theta_j| \quad ; \quad k \epsilon S_3$

then $|\phi_k| \leq \sum_{j \epsilon S_2} |\phi_k| \quad ; \quad k \epsilon S_3$

Thm. 5.1 (p. 41) : $S'' \cap R_{dc} \neq \emptyset$

Thm. 5.2 (p. 43) : $S' \cap R_{ac} \neq \emptyset$

Thm. 5.3 (p. 45) : $\sum_{k \epsilon R_{ac}} P_{dc}^k \geq - \sum_{k \epsilon R_{ac}} P_{ac}^k \geq \sum_{k \epsilon R_{dc}} P_{ac}^k \geq - \sum_{k \epsilon R_{dc}} P_{dc}^k > 0$

Thm. 5.4 (p. 47) : $- \sum_{k \epsilon R_{dc}} P_{dc}^k > \frac{G_v - 1}{G_v} P_0$

Thm. 5.5 (p. 49) : If $S' \neq S''$

then $$-\sum_{k\epsilon R_{dc}} P_{dc}^{k} \geq P_0$$

Thm. 5.6 (p. 50) : $$\sum_{k\epsilon R_{ac}} |\bar{i}_k| \geq (G_v - 1)\,|\bar{i}_0|$$

Thm. 5.7 (p. 51) : $$\sum_{k\epsilon R_{dc}} |\bar{v}_k| \geq \frac{G_v - 1}{G_v}\,|\bar{v}_0|$$

Thm. 5.8 (p. 52) : If $G_v > 1$

then $$\sum_{k\epsilon R_{dc}} |\bar{i}_k| \geq |\bar{i}_0|$$

Thm. 6.1 (p. 64) : If source is dc voltage source,

then $$\frac{1}{2}\sum_{k\epsilon X} \overline{|v_k i_k|} \geq \frac{G_v - 1}{G_v}\,P_0$$

Thm. 6.2 (p. 67) : If source is dc voltage source,

then $$\frac{1}{2}\sum_{k\epsilon C} \overline{|i_k|} + \sum_{k\epsilon L} \overline{|i_k|} \geq (G_v - 1)\,|\bar{i}_0|$$

Thm. 6.3 (p. 70) : If source is dc voltage source,

then $$\sum_{k\epsilon C} \overline{|v_k|} + \frac{1}{2}\sum_{k\epsilon L} \overline{|v_k|} \geq \frac{G_v - 1}{G_v}\,|\bar{v}_0|$$

Thm. 7.1 (p. 81) : If $v\,i \geq 0$ and $\bar{v}\,\bar{i} < 0$

then $$\hat{v}\,\hat{i} \geq \hat{v}\,|\bar{i}| + \hat{i}\,|\bar{v}|$$

where $\hat{v}$ and $\hat{i}$ are the maxima of v and i.

Cor. 7.1.1 (p. 85) : There is only one resistor in R_{dc}. The maxima of its voltage v and current i are $\hat{v}$ and $\hat{i}$.

If $|v(t)| \leq V$ for all t,

then $\hat{i} \geq \dfrac{V|\bar{i}_0|}{V-\beta|\bar{v}_0|}$

If $|i(t)| \leq I$ for all t,

then $\hat{v} \geq \dfrac{I\beta|\bar{v}_0|}{I-|\bar{i}_0|}$

where $\beta = \dfrac{G_v - 1}{G_v}$

Thm. 7.2 (p. 87) : If $0 < R_1 \leq v/i \leq R_2$

and $\bar{v}\,\bar{i} < 0$

then $\overline{vi} \geq \dfrac{4\sqrt{R_1/R_2}}{(1-\sqrt{R_1/R_2})^2}\,(-\bar{v}\,\bar{i})$

Cor. 7.2.1 (p. 90) : If $0 < R_1 \leq v/i \leq R_2$

and $\overline{vi} - \bar{v}\,\bar{i} < 0$

then $\overline{vi} \geq \dfrac{4\sqrt{R_1/R_2}}{(1-\sqrt{R_1/R_2})^2}\,(\bar{v}\,\bar{i} - \overline{vi})$

Thm. 7.4 (p. 100) : If $f(v,i,t) = 0$

then $-(\overline{vi} - \bar{v}\,\bar{i}) \leq \max_{\substack{(v_1,i_1)\in S \\ (v_2,i_2)\in S}} \left[\frac{1}{4}(v_2-v_1)(i_1-i_2)\right]$

where S is set of (v,i) satisfying $f(v,i,t) = 0$

(Result not new.)

Thm. 7.5 (p. 103) : Source is dc voltage source; network includes no inductors; all n capacitors have ESR of value R.

then $$\sum_{k\epsilon C} \bar{P}^k \geq \frac{4R}{n} (G_v - 1)^2 |\bar{i}_0|^2$$

Thm. 7.6 (p. 104) : Source is dc current source; network includes no inductors; all n capacitors have ESR of value R.

then $$\sum_{k\epsilon C} \bar{P}^k \geq \frac{4R}{n} \left[\frac{G_i - 1}{G_i}\right]^2 |\bar{i}_0|^2$$

Thm. 8.1 (p. 107) : Network consists of dc voltage source, one linear capacitor, and linear resistors. Then $G_v \leq 2$.

Thm. 8.2 (p. 110) : Network consists of dc voltage source, one inductor, and resistors. Then $G_v \leq 2$.

APPENDIX A

DISCUSSION OF THEOREMS 4.2 AND 4.3 AND AN EXTENSION OF THEOREM 4.4 TO FIELDS IN THREE-SPACE

Theorems 4.2 and 4.3, due to Berge and Ghouila-Houri (3), may be stated as follows: In a linear graph a positive flow (or tension) may be expressed as the sum of positive loop flows (or cutset tensions). The method of proof is to find an aligned loop (or cutset) in the graph and subtract a multiple of it, leaving all flow (or tension) members non-negative. This process is repeated until all members are zero.

That one may always find an aligned cutset in a graph with a positive tension is shown by construction in the proof of Theorem B.1. However, that one may always find an aligned loop in a graph with a positive flow is not so obvious. Some insight is gained by looking at the decomposition on a microscopic level (e.g., as the flow of electrons) or, equivalently, by considering the case of continuous flow densities and potential differences in three-space.

Consider a (compressible) fluid in motion in a box. If the rate and direction of flow is constant at every point, then it should be clear that a particle of the fluid at a certain time and position returns to that position at a later time without crossing the path of another particle. That is, lines of flow can be established. If the vector field J represents the rate of mass flow as a function of position in space, then we have

$$\nabla \cdot J \equiv \frac{\partial J_x}{\partial x} + \frac{\partial J_y}{\partial y} + \frac{\partial J_z}{\partial z} = 0$$

at every point in space. By Gauss' Law, this is equivalent to the fact that the net flow through a closed surface is zero for a stationary flow. (see Kaplan (6), p. 270).

Consider a number of surfaces in the space for which the direction of flow over each surface is uniform. Select a reference such that the net flow through each surface is positive. By a simple construction it is possible to find a set of "bundles" of flow lines such that the flow through each surface can be expressed as the sum of the flows in certain of these bundles.

That such a construction is possible is analogous to Theorem 4.2.

Consider a potential function ϕ in a box whose walls are at a constant potential. The potential may be electric potential, pressure, temperature, distance from a point within the box, etc. We may define a vector field by the gradient of the potential:

$$E = \nabla\phi = E_x i + E_y j + E_z k$$

where $E_x = \frac{\partial\phi}{\partial x}$; $E_y = \frac{\partial\phi}{\partial y}$; $E_z = \frac{\partial\phi}{\partial z}$

Then
$$\nabla \times E = \left[\frac{\partial E_z}{\partial y} - \frac{\partial E_y}{\partial z}\right] i + \left[\frac{\partial E_x}{\partial z} - \frac{\partial E_z}{\partial x}\right] j + \left[\frac{\partial E_y}{\partial x} - \frac{\partial E_x}{\partial y}\right] k = 0$$

everywhere in the space. Also, $\nabla \times E = 0$ only if $E = \nabla\phi$ for some ϕ, (see Kaplan (6) , p. 280). By Stokes' theorem, $\nabla \times E = 0$ is equivalent to the fact that the sum of potential rises around a closed path is zero, (see Kaplan (6) , p. 276).

Consider a number of pairs of points in the space and the potential rise from the lower to higher potential in each pair. By a simple construction it is possible to find a set of positive potential rises such the potential rise for each pair of points is the sum of certain potential rises in the set. Such a construction would be: pass a surface of constant potential through each point considered, and take the potential differences between successive surfaces as the desired set of potential rises.

That such a construction is possible is analogous to Theorem 4.3.

A physical electrical network consists of electron flows and electric fields in the wires and elements of the network. When the elements are "lumped" (not distributed), the network can be modeled well by a linear graph. In this case there are analogous theorems between the flows and tensions in the graph and the fields in three space. The graph theorems are usually simpler to state, but they cannot be applied to networks with distributed elements.

We will now state a theorem for fields in three-space which is analogous to Theorem 4.4. In the proof of the theorem the variables are assumed to be sufficiently smooth that the mathematical operations will hold.

In the following, line, surface, and volume integrals are indicated by $\int B \cdot d\ell$, $\int B \cdot da$, and $\int B dv$, respectively. A reference is associated with $d\ell$ and da, and $B \cdot d\ell$ and $B \cdot da$ are scalar products.

Lemma A.1.1: If Z is a space with two fields $\mathbf{J}$ and $\mathbf{E}$ defined in Z such that

$$\nabla \cdot J = 0$$

$$E = \nabla \phi$$

where ϕ is some scalar function over Z, then

$$\int_Z E \cdot J \, dv = \int_{\partial Z} \phi J \cdot da$$

Throughout this lemma and the following theorem ∂Z indicates the boundary of Z.

Proof: Gauss's theorem states that for any field F in Z,

$$\int_Z \nabla \cdot F \, dv = \int_{\partial Z} F \cdot da$$

where the orientation of da is directed into Z. Let $F = \phi J$. Then

$$\int_Z \nabla \cdot (\phi J)\, dv = \int_{\partial Z} \phi\, J \cdot da$$

But

$$\nabla \cdot (\phi J) = \nabla\phi \cdot J + \phi\, \nabla \cdot J$$

$$= \nabla\phi \cdot J = E \cdot J$$

and the result follows.

Theorem A.1: Consider a closed, bounded, three-dimensional space S with two fields J and E with bounded magnitude which satisfy

$$\nabla \cdot J = 0$$

$$\nabla \times E = 0$$

$$\int_{A_s} J \cdot da = 0$$

$$\int_{C_s} E \cdot d\ell = 0$$

where A_s is any portion of the boundary of S, and C_s is a curve between two points on the boundary of S.

Let S be divided into disjoint subspaces S_1, S_2, S_3, and S_4, whose union is S. The only requirement in this division is that $E \cdot J \leq 0$ everywhere in S_4. Then

a. $$\sum_{i=1}^{n} \left[\max_{C_i \subset S_1^i} \int_{C_i} E \cdot d\ell \right] \frac{1}{2} \int_{\partial S_2} |J \cdot da| + \int_{S_1} E \cdot J\, dv + \int_{S_3} |E \cdot J|\, dv \geq 0$$

and b. $$\sum_{i=1}^{n} \left[\max_{C_i \subset S_1^i} \int_{C_i} E \cdot d\ell \right] \frac{1}{2} \int_{\partial S_2} |J \cdot da| + \int_{S_2} E \cdot J\, dv + \int_{S_3} |E \cdot J|\, dv \geq 0$$

where S_1^i is closed and connected, $i=1,2,\ldots,n$, and

$$\bigcup_{i=1}^{n} S_1^i = S_1$$

Proof: Let a scalar potential function be defined over S as follows: assign a reference potential of zero to a point p_0 on ∂S, and let the potential $\phi(p)$ at a point p be given by

$$\phi(p) = \int_{p_0}^{p} \mathbf{E} \cdot d\boldsymbol{\ell}$$

The function ϕ is well defined since the integral is independent of path, and $\phi(p_0) = 0$ for all $p_0 \epsilon \partial S$. Then

$$\mathbf{E} = \nabla\phi$$

An equipotential surface is one on which ϕ is constant. Equivalently, $\int \mathbf{E} \cdot d\boldsymbol{\ell} = 0$ between any two points on the surface.

Now the space S_1 is composed of the S_1^i spaces:

$$S_1 = \bigcup_{i=1}^{n} S_1^i$$

Let V_i be the space of minimum volume which includes S_1^i and whose boundary consists of equipotential surfaces. Let X_i be defined as follows:

$$X_1 = V_1$$

$$X_i = V_i - X_{i-1} \quad ; \quad i=2,3,\ldots n$$

so that the X_i are disjoint, and the boundary of each X_i consists of equi-potential surfaces. Also

$$\bigcup_{i=1}^{n} X_i = \bigcup_{i=1}^{n} V_i$$

Since by construction $V_i \supset S_1^i$, we have

$$\bigcup_{i=1}^{n} X_i = \bigcup_{i=1}^{n} V_i \supset \bigcup_{i=1}^{n} S_1^i = S_1$$

Let the equi-potential surfaces which form the boundary of X_i be $A_{i1}, A_{i2}, \ldots A_{im_i}$ with the corresponding potentials $\phi_{i1}, \phi i_2, \ldots \phi_{im_i}$. From the lemma we have

$$\int_{X_i} E \cdot J = \sum_{j=1}^{m_i} \phi_{ij} \int_{A_{ij}} J \cdot da$$

Let B_{ij} be the space enclosed by the equipotential surface A_{ij} (A_{ij} is assured of completely enclosing a space in S since ∂S is an equi-potential surface.) Then by Gauss's theorem,

$$\int_{X_i} E \cdot J \, dv = \sum_{j=1}^{m} \phi_i \int_{B_{ij}} \nabla \cdot J \, dv = 0 \qquad (A.1)$$

Now,

$$S = \bigcup_{j=1}^{4} S_j$$

$$X_i = X_i \cap S = \bigcup_{j=1}^{4} (X_i \cap S_j)$$

Then Eq. (A.1) becomes

$$\sum_{j=1}^{4} \int_{X_i \cap S_j} E \cdot J \, dv = 0 \qquad (A.2)$$

Because S_4 was chosen so that $E \cdot J \leq 0$ everywhere in S_4,

$$\int_{X_i \cap S_4} E \cdot J \, dv \leq 0$$

Then Eq. (A.2) gives

$$\int_{X_i \cap S_1} E \cdot J \, dv + \int_{X_i \cap S_2} E \cdot J \, dv + \int_{X_i \cap S_3} E \cdot J \, dv \geq 0 \qquad (A.3)$$

We will now get an estimate on the middle term. The notation $\hat{Z} = Z - \partial S_2$ will be used below so that all unions become disjoint. Consider the boundary of $X_i \cap S_2$.

$$\partial(X_i \cap S_2) \equiv (X_i \cap \partial S_2) \cup (S_2 \cap \partial X_i)$$

$$= (X_i \cap \partial S_2) \cup (S_2 \cap \partial \hat{X}_i) \qquad [\text{disjoint}]$$

where $$\partial \hat{X}_i = \bigcup_{j=1}^{m} \hat{A}_j$$

Then applying the lemma to the middle term of Eq. (A.3),

$$\int_{X_i \cap S_2} E \cdot J \, dv = \int_{X_i \cap \partial S_2} \phi J \cdot da + \sum_{j=1}^{m} \phi_i \int_{S_2 \cap \hat{A}_j} J \cdot da \qquad (A.4)$$

Let $X_i^c = S - X_i$. Consider the boundary of $X_i^c \cap S_2$.

$$\partial(X_i^c \cap S_2) = (X_i^c \cap \partial S_2) \cup (S_2 \cap \partial \hat{X}_i^c)$$

where $$\partial \hat{X}_i^c = \left(\bigcup_{j=1}^{m} \hat{A}_j\right) \cup \partial \hat{S}$$

Noting that $S_2 \cap \partial \hat{S} = \phi$, apply Gauss's theorem to $X_i^c \cap S_2$:

$$-\sum_{j=1}^{m} \int_{S_2 \cap \hat{A}_j} J \cdot da + \int_{X_i^c \cap \partial S_2} J \cdot da = \int_{\partial(X_i^c \cap S_2)} J \cdot da$$

$$= \int_{X_i^c \cap S_2} \nabla \cdot J \, dv = 0$$

The first term on the left, if it is to be consistent with the same expression in Eq. (A.4), must have the minus sign. This is because the orientation of da, as used in Eq. (A.4), is directed out of $X_i^c \cap S_2$. Therefore

$$\sum_{j=1}^{m} \int_{S_2 \cap \hat{A}_j} J \cdot da = \int_{X_i^c \cap \partial S_2} J \cdot da$$

Then Eq. (A.4) yields

$$\int_{X_i \cap S_2} E \cdot J \, dv \leq \int_{X_i \cap \partial S_2} \phi J \cdot da + \left| \max_{i \leq u \leq m} \phi_j \right| \int_{X_i^c \cap \partial S_2} J \cdot da$$

Let Z^+ be the region of Z over which $J \cdot da > 0$, and let Z^- be the region over which $J \cdot da \leq 0$. Then

$$\int_{X_i \cap S_2} E \cdot J \, dv \leq \left[\max_{(X_i \cap \partial S_2)^+} \phi \right] \int_{(X_i \cap \partial S_2)^+} |J \cdot da| + \left[\max_{1 \leq j \leq m} \phi_j \right] \int_{(X_i^c \cap \partial S_2)^+} |J \cdot da|$$

$$- \left[\min_{(X_i \cap \partial S_2)^-} \phi \right] \int_{(X_i \cap \partial S_2)^-} |J \cdot da| - \left[\min_{1 \leq j \leq m} \phi_j \right] \int_{(X_i^c \cap \partial S_2)^-} |J \cdot da|$$

where $\bar{Z}$ is the closure of Z.

Now,

$$\max_{1 \leq j \leq m} \phi_j = \max_{\partial X_i} \phi \leq \max_{\bar{X}_i} \phi$$

$$\min_{1 \leq j \leq m} \phi_j = \max_{\partial X_i} \phi \geq \min_{\bar{X}_i} \phi$$

$$\max_{(X_i \quad \partial S_2)^+} \phi \leq \max_{\bar{X}_i} \phi$$

and

$$\min_{(X_i \quad \partial S_2)^-} \phi \geq \min_{\bar{X}_i} \phi \, .$$

We also have

$$(X_i^c \cap \partial S_2)^+ \cup (X_i^c \cap \partial S_2)^+ = (S \cap \partial S_2)^+ = \partial S_2^+$$

$$(X_i \cap \partial S_2)^- \cup (X_i^c \cap \partial S_2)^- = (S \cap \partial S_2)^- = \partial S_2^-$$

Therefore,

$$\int_{X_i \cap S_2} \mathbf{E} \cdot \mathbf{J} dv \leq \left[\max_{\bar{X}_i} \phi\right] \int_{\partial S_2^+} |\mathbf{J} \cdot d\mathbf{a}| - \left[\min_{\bar{X}_i} \phi\right] \int_{\partial S_2^-} |\mathbf{J} \cdot d\mathbf{a}|$$

But $$\int_{\partial S_2^+} |\mathbf{J} \cdot d\mathbf{a}| - \int_{\partial S_2^-} |\mathbf{J} \cdot d\mathbf{a}| = \int_{\partial S_2} \mathbf{J} \cdot d\mathbf{a} = \int_{S_2} \nabla \cdot \mathbf{J} \, dv = 0$$

and $$\int_{\partial S_2^+} |\mathbf{J} \cdot d\mathbf{a}| + \int_{\partial S_2^-} |\mathbf{J} \cdot d\mathbf{a}| = \int_{\partial S_2} |\mathbf{J} \cdot d\mathbf{a}|$$

so that $$\int_{\partial S_2^+} |\mathbf{J} \cdot d\mathbf{a}| = \int_{\partial S_2^-} |\mathbf{J} \cdot d\mathbf{a}| = \frac{1}{2} \int_{\partial S_2} |\mathbf{J} \cdot d\mathbf{a}|$$

and $$\int_{X_i \cap S_2} \mathbf{E} \cdot \mathbf{J} \, dv \leq \left[\max_{\bar{X}_i} \phi - \min_{\bar{X}_i} \phi\right] \frac{1}{2} \int_{\partial S_2} |\mathbf{J} \cdot d\mathbf{a}| \qquad \text{(A.5)}$$

We will now get an estimate on the "potential difference" factor in Eq. (A.5). From the way X_i was constructed, it is clear that

$$X_i \subset V_i$$

where V_i was defined as the space of minimum volume which includes S_1^i and whose boundary consists of equipotential surfaces. Therefore

$$\max_{\bar{X}_i} \phi - \min_{\bar{X}_i} \phi \leq \max_{V_i} \phi - \min_{V_i} \phi \qquad (A.6)$$

The claim is that

$$\max_{V_i} \phi \leq \max_{\partial S_1^i} \phi$$

and

$$\min_{V_i} \phi \geq \min_{\partial S_1^i} \phi$$

which will be proved by contradiction. Let

$$\max_{\partial S_1^i} \phi = \phi_m$$

Suppose that there is a point p in V_i for which $\phi(p) > \phi_m$. Because E is bounded, ϕ is continuous. Therefore there are distinct points q and r close to p such that $\phi(q) > \phi_m$, $\phi(r) > \phi_m$, q lies on an equipotential surface A_q, and r lies on an equipotential surface A_r. Let the closed space whose boundary is $A_q \bigcup A_r$ be V_{qr}. Since equipotential surfaces do not cross, $V_{qr} \subsetneq V_i$. Now V_{qr} does not include S_1^i since V_i is the space of minimum volume which includes S_1^i and whose boundary is equipotential surfaces. Also, A_q and A_r do not intersect ∂S_1^i since $\phi(q) > \phi_m$ and $\phi(r) > \phi_m$. Then the connectedness of S_1^i implies that $V_{qr} \bigcap S_1^i = 0$. Therefore the space $V_i - V_{qr}$ includes S_1^i and has a boundary consisting of equipotentials, and the volume of $V_i - V_{qr}$ is less than the volume of V_i. But this contradicts the assumption on V_i. Therefore

$$\max_{V_i} \phi \leq \max_{\partial S_1^i} \phi$$

In a similar manner

$$\min_{V_i} \phi \geq \min_{\partial S_1^i} \phi$$

Then Ineq. (A.6) gives

$$\max_{\bar{X}_i} \phi - \min_{\bar{X}_i} \phi \leq \max_{\partial S_1^i} \phi - \min_{\partial S_1^i} \phi$$

$$= \max_{C_i \subset \partial S_1^i} \int_{C_i} \mathbf{E} \cdot d\boldsymbol{\ell}$$

With this, Ineq. (A.5) becomes

$$\int_{X_i \cap S_2} \mathbf{E} \cdot \mathbf{J} dv \leq \left[\max_{C_i \subset S_1^i} \int_{C_i} \mathbf{E} \cdot d\boldsymbol{\ell} \right] \frac{1}{2} \int_{\partial S_2} |\mathbf{J} \cdot d\mathbf{a}|$$

Finally, we can use this in Ineq. (A.3) to get

$$\int_{X_i \cap S_1} \mathbf{E} \cdot \mathbf{J} dv + \left[\max_{C_i \subset S_1^i} \int_{C_i} \mathbf{E} \cdot d\boldsymbol{\ell} \right] \frac{1}{2} \int_{\partial S_2} |\mathbf{J} \cdot d\mathbf{a}| + \int_{X_i \cap S_3} \mathbf{E} \cdot \mathbf{J} dv \geq 0$$

Noting that the X_i are disjoint, we sum the inequality over i.

$$\int_{X \cap S_1} \mathbf{E} \cdot \mathbf{J} dv + \sum_{i=1}^{n} \left[\max_{C_i \subset S_1^i} \int_{C_i} \mathbf{E} \cdot d\boldsymbol{\ell} \right] \frac{1}{2} \int_{\partial S_2} |\mathbf{J} \cdot d\mathbf{a}| + \int_{X \cap S_3} \mathbf{E} \cdot \mathbf{J}\, dv \geq 0 \qquad \text{(A.7)}$$

where $$X = \bigcup_{i=1}^{n} X_i$$

As pointed out when the X_i were constructed, $X \supset S_1$, so that

$$X \cap S_1 = S_1$$

Also $$\int_{X \cap S_3} \mathbf{E} \cdot \mathbf{J}\, dv \leq \int_{X \cap S_3} |\mathbf{E} \cdot \mathbf{J}|\, dv \leq \int_{S_3} |\mathbf{E} \cdot \mathbf{J}|\, dv$$

Together with Ineq. (A.7) this gives

$$\int_{S_1} E \cdot J \, dv + \sum_{i=1}^{n} \left[\max_{C_i \subset S_1^i} \int_{C_i} E \cdot d\ell \right] \frac{1}{2} \int_{\partial S_2} |J \cdot da| + \int_{S_3} |E \cdot J| dv \geq 0$$

which proves result (a).

Result (b) is proved in a similar way, constructing spaces V_i which include S_2 and whose boundaries are not crossed by lines of the field J. This is analogous to finding a decompositon for $\{\psi_k'\}$ in Theorem 4.4.

APPENDIX B

A DIRECT PROOF OF COROLLARY 4.4.1

It has long been recognized as an intuitively obvious fact that, given a network of resistors and sources, the voltage magnitude across any resistor is not greater than the sum of the voltage magnitudes across the sources, and the current magnitude through any resistor is not greater than the sum of the current magnitudes through the sources. For the case of one source and linear resistors, this is sometimes stated that the voltage and current transfer ratios of a resistive two-port are not greater than unity.

Talbot (13) and Schwartz (21) prove the "no voltage gain" result for one source and general (nonlinear, time-varying) resistors by showing that the nodes of maximum and minimum potential must be connected to a source. Talbot also proves the "no current gain" result for one source by a method that makes use of cutsets. (The basis of his proof is similar to the proof here of Theorem B.1.)

When the resistors are linear there are many other proofs of these results, and the case of many sources can be included by using superposition. The result may then be extended to nonlinear resistors by considering the operating point of the network of resistors at a given time. A network with the same operating point can be constructed by replacing the nonlinear resistors with linear resistors, and the result follows. (See Desoer and Kuh (18).)

Corollary 4.4.1 provides a purely graphical proof of the result--without reference to the element characteristics, except that $v\,i > 0$. It is an interesting application of Theorems 4.2 and 4.3 due to Berge and Ghouila-Houri (3).

We will now prove the result of Corollary 4.4.1 more directly and in the terms of electrical engineering.

Theorem B.1: Given a network of sources and (nonlinear, time-varying) positive resistors, the current magnitude through any resistor at a given time is not greater than the sum of the current magnitudes through the sources at that time.

Proof: Let the element references be chosen so that all voltages are positive. Theorem 4.3 then implies that every element is included in at least one aligned cutset. (This fact is actually the result of a theorem by Minty (20) which is used in the proof of Theorem 4.3.) A simple method of constructing such an aligned cutset is as follows. Consider any element, and select a potential e_0 which lies between the potentials of the nodes to which the element is connected. Divide the nodes in the network into two sets E_1 and E_2 so that a node is in E_1 if its potential is greater than e_0 and is in E_2 otherwise. Then the elements connected to nodes in both E_1 and E_2 constitute an aligned cutset (all the element references have the same orientation as the cutset).

Select any resistor with current i_0. Select (or construct as above) an aligned cutset which includes this resistor. Let S be the set of sources in this cut set and let R be the set of the other resistors in the cutset. Now, the sum of currents in a cutset is zero:

$$i_0 + \sum_{k \epsilon S} i_k + \sum_{k \epsilon R} i_k = 0$$

But since all voltages are positive, the currents in all resistors are positive, and (in the worst case) the currents in all sources are negative. Then we can write

$$|i_0| - \sum_{k \epsilon S} |i_k| + \sum_{k \epsilon R} |i_k| = 0$$

Therefore $$|i_0| \leq \sum_{k \epsilon S} |i_k|$$

But the term on the right is less than the sum over all sources, and i_0 was the current in any resistor. Then the current magnitude through any resistor is less than the sum of the current magnitudes through the sources.

Theorem B.2: Given a network of sources and (nonlinear, time-varying) positive resistors, the voltage magnitude across any resistor is not greater than the sum of the voltage magnitudes across the sources.

Proof: Let the element references be chosen so that all currents are positive. The proof of the theorem is then exactly the dual of Theorem B.1. The only difference is that it is not so easy to construct an aligned loop as it is an aligned cutset. This is because the construction of an aligned cutset made use of nodes, and the node has no dual in the general (nonplanar) case.

APPENDIX C

DC GAIN OF A POSITIVE OPERATOR FEEDBACK SYSTEM WITH ONE TIME-VARYING UNIT

The system to be studied by Theorem C.1 can be represented by the block diagram in Figure C.1.

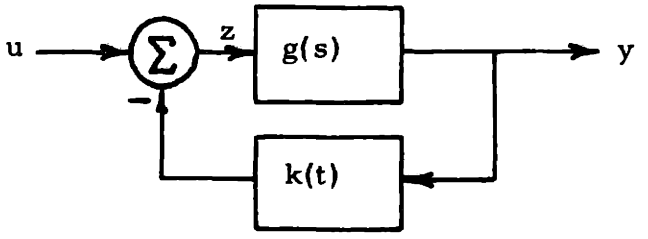


Figure C.1 Block Diagram of Feedback System Characterized by Eq. (C.2)

The operator in the forward path can be expressed as a convolution integral or by one of several differential equation forms. The time-varying gain in the reverse path is positive. We will find bounds on the average of the output when the input is constant.

Theorems C.2 and C.3 apply the result to electrical networks to show that a network of linear, time-invariant elements and only one time varying resistor cannot be a dc to dc conversion network. Now, Theorem 5.3 already implies this for the more general case allowing nonlinear reactances, and its proof is shorter. However, the main result here is Theorem C.1. Theorems C.2 and C 3 are included to show a particular application of Theorem C.1 to the dc to dc conversion problem.

Lemma C.1.1: Let $p(D)$ be an n^{th} order polynomial in D, where D is the operator d/dt. Let the average $\bar{x}$ of the function x be defined

by $$\overline{x} = \lim_{T\to\infty} \int_0^T \frac{1}{T} x(t)dt$$

If $x(t)$ is n times differentiable and its first $(n-1)$ derivatives are bounded for $t \geq 0$, then

$$\overline{p(D)x} = p(D)\overline{x} = p(0)\overline{x}$$

Proof: Let $p(D) = a_0 + a_1 D + \ldots + a_n D^n$. Now,

$$\overline{a_i D^i x} = \lim_{T\to\infty} \frac{1}{T} \int_0^T a_i D^i x(t)dt$$

$$= \lim_{T\to\infty} \frac{a_i}{T} [D^{i-1}x(T) - D^{i-1}x(0)] \quad ; \quad i=1,2,\ldots,n.$$

But $D^{i-1}x(t)$ is bounded for $t=0$ and $t=T$. Therefore

$$\overline{a_i D^i x} = 0 \quad ; \quad i = 1,2,\ldots,n$$

$$\overline{p(D)x} = \sum_{i=0}^{n} \overline{a_i D^i x} = \overline{a_0 x} = p(0)\overline{x}$$

Also $$D^i\overline{x} = 0 \quad ; \quad i = 1,2,\ldots,n$$

Therefore

$$p(D)\overline{x} = \sum_{i=0}^{n} a_i D^i\overline{x} = a_0\overline{x} = p(0)\overline{x}$$

which proves the lemma.

Lemma C.1.2: If $g(s) = q(s)/p(s)$ is a positive real function of s, where $p(s)$ is an n^{th} order polynomial in s, $q(s)$ is a polynomial of order less than n, and $p(s)$ and $q(s)$ have no common factors, then

$$\overline{[p(D)x(t)][q(D)x(t)]} \triangleq \lim_{T\to\infty} \frac{1}{T} \int_0^T [p(D)x(t)][q(D)x(t)]dt \geq 0$$

for all functions x which are n times differentiable and whose first (n-1) derivatives are bounded for $t \geq 0$.

Proof: We separate the integral of interest into two parts, one that is bounded and one that is positive, by adding and subtracting a term:

$$[p(D)x(t)][q(D)x(t)] = \lim_{T\to\infty} \frac{1}{T}\int_0^T \{[p(D)x(t)][q(D)x(t)] - [r(D)x(t)]^2\}dt + \lim_{T\to\infty} \frac{1}{T}\int_0^T [r(D)x(t)]^2 dt \qquad (C.1)$$

where $r(D) = [Ev\ p(D)q(-D)]^+$

Now, Brockett (17) has shown that the first integral in Eq. (C.1) is independent of path; that is, its value $F[\{x^{(i)}(0)\}, \{x^{(i)}(T)\}]$ depends only on the value of x(t) and its first (n-1) derivatives at t=0 and t=T. But the $x^{(i)}(t)$; i=0, 1, . . . , n-1 are bounded for $t \geq 0$. Then F is also bounded and

$$\lim_{T\to\infty} \frac{1}{T} F = 0$$

Therefore,

$$\overline{[p(D)x(t)][q(D)x(t)]} = \lim_{T\to\infty} \frac{1}{T}\int_0^T [r(D)x(t)]^2 dt \geq 0$$

which is the desired result.

When applied to electrical networks, this well-known result has the interpretation that a network of passive elements cannot deliver positive average power if the stored energy is bounded.

Theorem C.1: Consider the system equations

$$p(D)x(t) + k(t)q(D)x(t) = u \quad ; \quad t \geq 0$$

$$y(t) = q(D)x(t) \quad ; \quad t \geq 0$$

where $p(D)$ is an n^{th} order polynomial in D, $q(D)$ is a polynomial of order less than n, $p(D)$ and $q(D)$ have no common factors,

$$u = \text{constant} \geq 0$$

and $$k(t) \geq 0 \quad ; \quad t \geq 0$$

Let the average $\bar{x}$ of the function x be defined by

$$\bar{x} = \lim_{T \to \infty} \frac{1}{T} \int_0^T x(t)dt$$

where the limit exists. If $x(t)$ is n times differentiable and its first $(n-1)$ derivatives are bounded, and if $g(s) = q(s)/p(s)$ is a positive real function of s, then

$$\frac{g(0)u}{1 + \bar{k}g(0)} \leq \bar{y} \leq g(0)u$$

Proof: Let us define

$$z(t) = p(D)x(t) \quad ; \quad t \geq 0$$

Then the system equation is

$$z + ky = u \tag{C.2}$$

Therefore $$yz + yky = yu$$

$$\overline{yz} + \overline{yky} = \overline{yu} = \bar{y}u$$

But $$\overline{yz} = \bar{y}\bar{z} + \overline{(y-\bar{y})(z-\bar{z})}$$

Then $$\bar{y}\,\bar{z} + \overline{(y-\bar{y})(z-\bar{z})} + \overline{yky} = \bar{y}\,u$$

Now, by Lemma C.1.1,

$$\bar{y} \equiv \overline{q(D)x} = q(D)\bar{x}$$

$$\bar{z} \equiv \overline{p(D)x} = p(D)\bar{x}$$

so that $\overline{(y-\bar{y})(z-\bar{z})} = \overline{[q(D)(x-\bar{x})][p(D)(x-\bar{x})]}$

Then Lemma C.1.2 gives

$$\overline{(y-\bar{y})(z-\bar{z})} \geq 0$$

Therefore $$\bar{y}\,\bar{z} + \overline{yky} \leq \bar{y}\,u \qquad \text{(C.3)}$$

Also $$\overline{yky} \geq 0$$

Then $$\bar{y}\,\bar{z} \leq \bar{y}\,u \qquad \text{(C.4)}$$

We also have by Lemma C.1.1 and Lemma C.1.2

$$\bar{y}\,\bar{z} = q(D)\bar{x}\; p(D)\bar{x} = \overline{[q(D)\bar{x}][p(D)\bar{x}]} \geq 0$$

and as required in the conditions,

$$u \geq 0$$

Then Ineq. (C.4) gives

$$\bar{y} \geq 0$$

Dividing Ineq. (C.4) by $\bar{y}$,

$$\bar{z} \leq u$$

But by Lemma C.1.1,

$$\bar{y} \equiv \overline{q(D)x} = q(0)\bar{x}$$

$$\bar{z} \equiv \overline{p(D)x} = p(0)\bar{x} = \bar{y}/g(0)$$

Therefore $$\bar{y} \leq g(0)u$$

which is the upper bound of the theorem.

Now, $$\overline{yky} \equiv 2\bar{y}\overline{ky} - \bar{y}k\bar{y} + \overline{k(y-\bar{y})^2}$$

Substituting this into Ineq. (C.3),

$$\bar{y}\,\bar{z} + 2\overline{\bar{y}ky} - \bar{y}k\bar{y} + \overline{k(y-\bar{y})^2} \leq \bar{y}\,u$$

But $$\overline{k(y-\bar{y})^2} \geq 0$$

Therefore $$\bar{y}\,\bar{z} + 2\overline{\bar{y}ky} - \bar{y}k\bar{y} \leq \bar{y}\,u$$

Since $\bar{y} \geq 0$, dividing by $\bar{y}$ gives

$$\bar{z} + 2\overline{ky} - \bar{k}\,\bar{y} \leq u \qquad \text{(C.5)}$$

Now, taking the average of Eq. (C.2),

$$\bar{z} + \overline{ky} = u$$

$$2\bar{z} + 2\overline{ky} = 2u$$

Subtracting Ineq. (C.5) from this,

$$\bar{z} + \bar{k}\,\bar{y} \geq u$$

But $$\bar{z} = \bar{y}/g(0)$$

Therefore $$y \geq \frac{g(0)u}{1 + \bar{k}g(0)}$$

which is the lower bound of the theorem and completes the proof.

Example: Given the differential equation

$$\ddot{x} + f(t)\,\dot{x} + f(t)\,x = 1 \quad ; \quad f(t) = |\sin t| + 1$$

find bounds on $\bar{x}$.

The equation can be put in the form

$$\tilde{p}(D)x + f(t)\,\tilde{q}(D)x = 1$$

where $$\tilde{p}(D) = D^2$$

$$\tilde{q}(D) = D + 1$$

We have $$f(t) = |\sin t| + 1 \geq 0 \quad \text{for all } t.$$

But $$\tilde{g}(s) = \frac{\tilde{q}(s)}{\tilde{p}(s)} = \frac{s+1}{s^2}$$

is not a p.r. function because it has a pole of second order for $\mathrm{Re}[s] = 0$. Therefore Theorem C.1 is not applicable. However, the equation may also be put in the form

$$p(D)\, x + k(t)\, q(D)\, x = 1$$

where $$p(D) = D^2 + D + 1$$

$$q(D) = D + 1$$

$$k(t) = f(t) - 1 = |\sin t| \geq 0 \qquad \text{for all } t.$$

Now, $$g(s) = \frac{q(s)}{p(s)} = \frac{s+1}{s^2 + s + 1}$$

$$\mathrm{Re}[g(j\omega)] = \frac{1}{\omega^2 + (1-\omega^2)^2} > 0 \qquad \text{for all } \omega.$$

The poles of $g(s)$ occur for $\mathrm{Re}[s] \leq 0$. Also, $g(s)$ has no poles or zeros for $\mathrm{Re}[s] = 0$ of order greater than one. Therefore $g(s)$ is a p.r. function of s. (See Guillemin (19).) Then Theorem C.1 gives

$$\frac{g(0)}{1 + \bar{k} g(0)} \leq \bar{y} = q(0)\, \bar{x} \leq g(0)$$

$$\frac{1}{1 + 2/\pi} \leq \bar{x} \leq 1$$

Theorem C.2: If a system consisting of linear, time-invariant capacitors, inductors, and resistors is connected to a DC voltage source and to a time-varying, positive resistor, then the magnitude of the average voltage across any two nodes in the system is not greater than the magnitude of the DC voltage source. That is, for the network in Figure C.2, $\bar{v}_3 \leq V$.

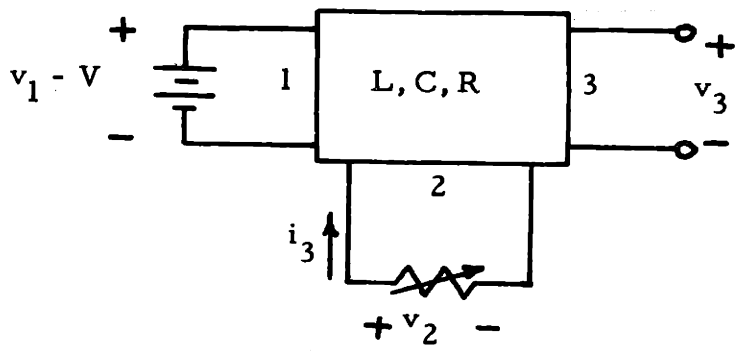


Figure C.2 Network With Ports of Interest Extracted to Show No Average Voltage Gain

Proof: Let the system be characterized by

$$\begin{bmatrix} \hat{v}_3 \\ \hat{v}_2 \end{bmatrix} = \begin{bmatrix} h_{11}(s) & h_{12}(s) \\ h_{21}(s) & h_{22}(s) \end{bmatrix} \begin{bmatrix} \hat{v}_1 \\ \hat{i}_2 \end{bmatrix}$$

$$i_2(t) = -k(t)\ v_2(t) \quad ; \quad k(t) \geq 0 \quad \text{for all } t.$$

where $\hat{\cdot}$ indicates the Laplace transform. Since $h_{22}(s)$ is the driving point impedance of port 2 with port 1 shorted and port 3 open,

$$\text{Re}\,[h_{22}(j\omega)] \geq 0 \qquad \text{for all } \omega$$

Since $h_{11}(s)$ is the voltage transfer function for port 2 open,

$$|h_{11}(0)| \leq 1$$

Since $[h_{11}(s) - h_{12}(s)h_{21}(s)h_{22}^{-1}(s)] \triangleq f(s)$ is the voltage transfer function for port 2 shorted,

$$|f(0)| \leq 1$$

Putting the system equations in block diagram form yields Figure C.3.

Since V is a constant, u is a constant. Specifically,

$$u = h_{21}(0)\, h_{22}^{-1}(0)\, V$$

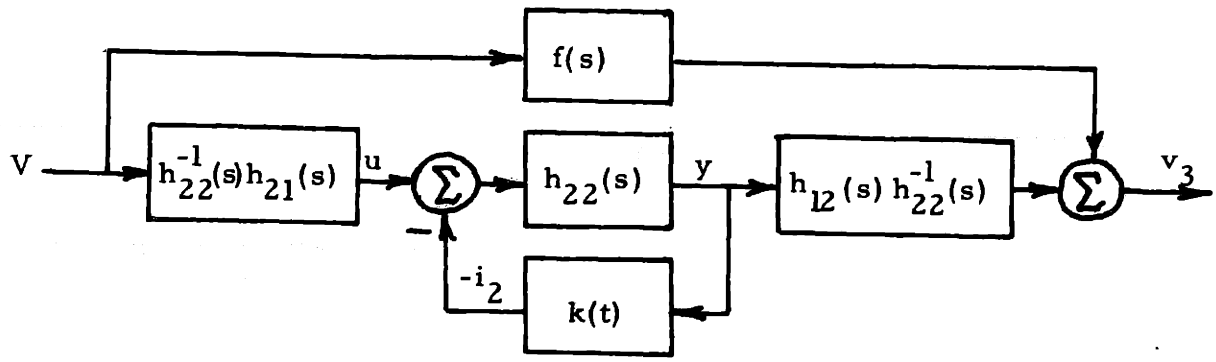


Figure C.3 Block Diagram of System Equations

Choose the labeling of voltage at port 2 such that $u \geq 0$. Then by Theorem C.1

$$0 \leq \bar{y} \leq h_{22}(0)\, u = h_{21}(0)\, V$$

Now,
$$\bar{v}_3 = h_{12}(0)\, h_{22}^{-1}(0)\, y + f(0)\, V$$

Since $\bar{v}_3$ is a linear function of $\bar{y}$, $|\bar{v}_3|$ will be a maximum when $\bar{y}$ is at one of its extreme values:

$$|\bar{v}_3| \leq \max \left[|\bar{v}_3|_{\bar{y}=0},\ |\bar{v}_3|_{\bar{y}=h_{21}(0)V} \right]$$

or
$$|\bar{v}_3| \leq \max \left[|f(0)|\,|V|,\ |h_{11}(0)|\,|V| \right]$$

But
$$|f(0)| \leq 1$$
$$|h_{11}(0)| \leq 1$$

therefore
$$|\bar{v}_3| \leq |V|$$

Theorem C.3: If a system consisting of linear, time-invariant capacitors, inductors, and resistors is connected to a time-varying, positive resistor and to a DC voltage source, then the magnitude of the

average current in any branch is less than the magnitude of the average current through the DC voltage source. That is, for the network of Figure C.4, $|\bar{i}_3| \leq |\bar{i}_1|$.

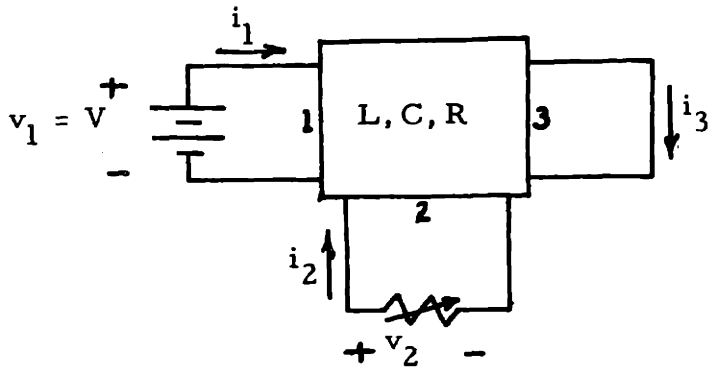


Figure C.4 Network With Ports of Interest Extracted to Show No Average Current Gain

Proof: Let the system be characterized by

$$\begin{bmatrix} \hat{i}_3 \\ \hat{v}_2 \\ \hat{i}_1 \end{bmatrix} = \begin{bmatrix} h_{11}(s) & h_{12}(s) \\ h_{21}(s) & h_{22}(s) \\ h_{31}(s) & h_{32}(s) \end{bmatrix} \begin{bmatrix} \hat{v}_1 \\ \hat{i}_2 \end{bmatrix}$$

$$i_2(t) = -k(t)\, v_2(t) \;; \quad k(t) \geq 0 \qquad \text{for all } t.$$

where $\hat{\cdot}$ is the Laplace transform. Since $h_{22}(s)$ is the driving point impedance at port 2 with port 1 shorted and port 3 shorted,

$$\mathrm{Re}[h_{22}(j\omega)] \geq 0 \qquad \text{for all } \omega.$$

Since $h_{31}(s)$ is the driving point admittance at port 1 with port 2 open and port 3 shorted,

$$h_{31}(0) > 0 \qquad (\text{assume } h_{31}(0) \neq 0).$$

Let $$f_3(s) \triangleq h_{31}(s) - h_{32}(s)\, h_{21}(s)\, h_{22}^{-1}(s)$$

Since $f_3(s)$ is the driving point admittance at port 1 with port 2 shorted and port 3 shorted,

$$f_3(0) > 0.$$

Since $h_{11}(s)/h_{31}(s)$ is the current transfer function for port 2 open

$$|h_{11}(0)/h_{31}(0)| \leq 1.$$

Let $$f_1(s) \triangleq h_{11}(s) - h_{12}(s)\, h_{21}(s)\, h_{22}^{-1}(s).$$

Since $f_1(s)/f_3(s)$ is the current transfer function for port 2 shorted,

$$|f_1(0)/f_3(0)| \leq 1.$$

Putting the system in block diagram form, we have Figure C.5

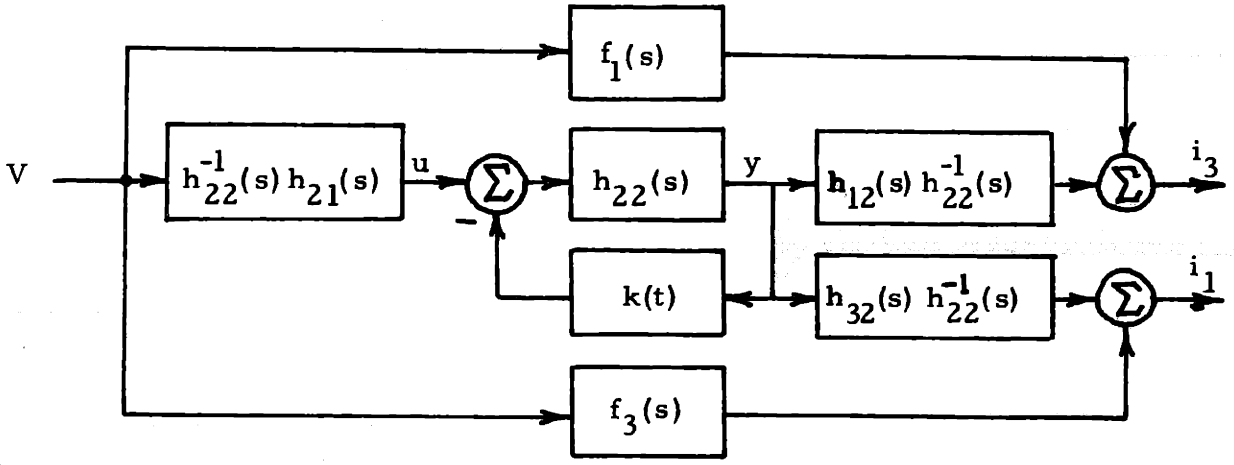


Figure C.5 Block Diagram of System Equations

Since V is a constant, u is a constant. Specifically,

$$u = h_{21}(0)\, h_{22}^{-1}(0)\, V$$

Choose the labeling of the voltage at port 2 such that $u \geq 0$. Then by Theorem C.1,

$$0 \leq \overline{y} \leq h_{22}(0)\, u = h_{21}(0)\, V$$

Now, $\bar{i}_3 = h_{12}(0)\, h_{22}^{-1}(0)\, \bar{y} + f_1(0)\, V$

$\bar{i}_1 = h_{32}(0)\, h_{22}^{-1}(0)\, \bar{y} + f_3(0)\, V$

therefore $\bar{i}_1 \big|_{\bar{y}=0} = f_3(0)\, V = |f_3(0)V|\ \text{sign}\ (V)$

$\bar{i}_1 \big|_{y=h_{21}(0)V} = h_{31}(0)\, V = |h_{31}(0)V|\ \text{sign}\ (V).$

Since $\bar{i}$ is a linear function of $\bar{y}$,

$$\text{sign}\ (\bar{i}_1) = \text{sign}\ (V) \quad ; \quad 0 \le \bar{y} \le h_{21}(0)\, V$$

Since $\bar{i}_3$ is also a linear function of $\bar{y}$, and $\bar{i}_1$ doesn't change sign as $\bar{y}$ varies over its range, the maximum of $|\bar{i}_3/\bar{i}_1|$ will be when $\bar{y}$ is at one of its extreme values:

$$|\bar{i}_3/\bar{i}_1| \le \max \left[|\bar{i}_3/\bar{i}_1|_{\bar{y}=0},\ |\bar{i}_3/\bar{i}_1|_{\bar{y}=h_{21}(0)V} \right]$$

or $$|\bar{i}_3/\bar{i}_1| \le \max \left[|f_1(0)/f_3(0)|,\ |h_{11}(0)/h_{31}(0)| \right]$$

But $$|f_1(0)/f_3(0)| \le 1 \quad ; \quad |h_{11}(0)/h_{31}(0)| \le 1$$

therefore $$|\bar{i}_3/\bar{i}_1| \le 1$$

which gives the result of the theorem.

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BIOGRAPHICAL NOTE

Dan Wolaver was born September 2, 1942 in Cleveland, Ohio, where he received his elementary and junior high school education. He attended high school in Maumee, Ohio.

In 1964 he graduated cum laude from Rensselaer Polytechnic Institute with a Bachelor of Electrical Engineering degree. While attending R.P.I., Mr. Wolaver participated in a cooperative program with General Electric Company.

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