CdTe photovoltaic cells performance under ambient lighting for internet of things applications

Ian Mathews[1,*], Sai Nithin Reddy Kantareddy[1], Zhe Liu[1], Amit Munshi[2], Kurt Barth[2], Walajabad Sampath[2], Tonio Buonassisi[1], Ian Marius Peters[1]

[1]Massachusetts Institute of Technology, Cambridge, MA 02139, USA
[2]Colorado State University, Fort Collins, CO, USA

Abstract

This paper investigates the suitability of CdTe photovoltaic cells to be used as power sources for wireless sensors located in buildings. Our cell structure is fabricated with a TCO front contact that provides for high photocurrents and low series resistance at low light intensities. We measure the photovoltaic response of this cell across five orders of magnitude of AM1.5G light intensity. Efficiencies of 10% and 17.1% are measured under ~1 W/m^2 AM1.5G and LED irradiance respectively. These measurements are some of the first for a CdTe cell under ambient lighting and the highest values measured to date. The measured results are fitted with two-diode simulation model to explore the role of cell parameters at these very low light intensities. We further discuss the potential of CdTe for internet of things devices in buildings given the many benefits of the technology such as the established manufacturing know-how, low-cost and long-term stability while we also evaluate issues around toxicity.

Introduction

The use of photovoltaic cells to power internet of things (IoT) devices in buildings has the potential to significantly reduce the maintenance issues associated with batteries and presents a significant market opportunity [1], [2]. A large number of photovoltaic technologies have been investigated for their effectiveness at converting ambient light from incandescent, compact fluorescent or LED bulbs into electrical energy including silicon, III-V, perovskite and organic PV devices [3]–[5]. Despite being the most successful thin-film photovoltaic technology in the solar power market, the use of CdTe to power IoT nodes has been little investigated. This is despite the many advantages of the technology for this application including its ~1.4 eV bandgap that is relatively well matched to typical indoor light spectra as compared to silicon [1], its proven stability as compared to perovskite and organic PV materials [6], its lower cost than III-V cells and its established manufacturing base. Furthermore, CdTe solar panels are known to perform better than their silicon counterparts under low level diffuse radiation [7].

Studies of CdTe PV cells under low light intensity have shown them to have a superior relative efficiency and voltage at low intensities than comparable c-Si and GaAs cells [8]. The CdTe/CdS solar cells show an STC efficiency of around 11% under 1000 W/m^2 AM1.5G and retain around 8 % efficiency at 1 W/m^2, while the open-circuit voltage remained as high as 600 mV under the low light conditions. More recently, a similar efficiency of 9% was measured for a CdTe cell under 8 W/m^2 AM1.5G with an open-circuit voltage of 600 mV – the fitted series resistance, R_s, for these cells was 150 ohm.cm^2 at the lowest light intensities. The only measurements of CdTe cell performance under typical indoor light sources in the literature is for a cell with an efficiency of 9.5% under STC, that increases to 10.9% under 9.1 W/m^2 compact fluorescent lighting - a smaller increase than might be expected for a cell under a better matched spectrum [9].

In this paper, we use measurements on an existing CdTe photovoltaic cell to discuss the physical changes and innovations needed to construct a good indoor CdTe device. We present a CdTe photovoltaic cell with a TCO front contact and measure its performance versus light intensity across five orders of magnitude AM1.5G and under low level LED irradiance. We discuss the implications of going to low light intensities; where the generated photocurrent reduces 3 orders of magnitude while

*correspondence: imathews@mit.edu

the photovoltage is, ideally, decreasing logarithmically. In a silicon cell at low light intensities, SRH recombination results in a stronger decrease in voltage, making them less suitable for indoor applications, but most thin-film cells, including ours, show close to the expected behavior. The fill factor behaviour depends on a range of contributors, resistances and ideality factors while series resistance is expected to go up, and does a little, but becomes less relevant because of the strongly reduced currents. Furthermore, we discuss how the cost and manufacturing scale of this technology offer significant benefits to its widespread use, while highlighting potential ROHS challenges in the use of cadmium in electronics devices.

Methods

The cells used in the study were deposited on NSG TEC 10 soda lime glass coated with fluorine-doped tin oxide (FTO) to function as a transparent conducting oxide (TCO). The FTO layer was deposited by the glass manufacturer. A 100 nm thick $Mg_xZn_{1-x}O$ (MZO) buffer layer was deposited using RF sputter deposition [10]. CdSeTe films were sublimated on TEC 10 glass substrate that was coated with MZO using an optimized deposition process followed by sublimation of the CdTe layer. Devices fabricated by a similar process was used to demonstrate over 19% device efficiency [11]. $CdSe_xTe_{1-x}$ (CdSeTe) and CdTe depositions were followed by $CdCl_2$ passivation, performed in-line without breaking vacuum. The substrate was heated to ~540°C before indexing the substrate into the deposition station for the sublimation of CdSeTe layer. The temperature of the substrate was measured in-situ using a pyrometer located outside the pre-heating station. The thin-films for this study were deposited using the advanced deposition system with 9 process stations at Colorado State University previously optimized for fabrication of CdTe based thin- film devices [12].

The CdSeTe composition used for this study had 40% CdSe in the source material and the as-deposited films had a band-gap of ~1.41 eV measured using optical transmission measurements and the Tauc plot method. The CdSeTe sublimation source was heated to 575°C while the substrate heater was maintained at 420°C and CdSeTe films of ~ 1.5–2.0 µm thickness were deposited. After deposition of CdSeTe, the substrate was moved to the CdTe sublimation vapor source and a film ~3.5 µm thick was deposited. The total thickness of CdSeTe and CdTe film stack was measured to be ~5 µm using a profilometer. The CdTe sublimation source temperature was maintained at 555°C and the substrate heater for this source was maintained at 500°C. One of the substrates was moved to the $CdCl_2$ vapor passivation treatment station in-situ without breaking vacuum after the CdTe film deposition. The $CdCl_2$ sublimation source was maintained at 450°C while the substrate heater for this source was heated to 425°C. The $CdCl_2$ passivation treatment was performed for 600 s. Such a $CdCl_2$ treatment causes grading of the absorber layer in addition to defect passivation that is understood to be critical for good device performance [13]. These temperatures were determined after several experimental iterations to optimize the $CdCl_2$ treatment such that at the end of the 600 s treatment there was a thin film of $CdCl_2$ deposited on the substrate. Following the

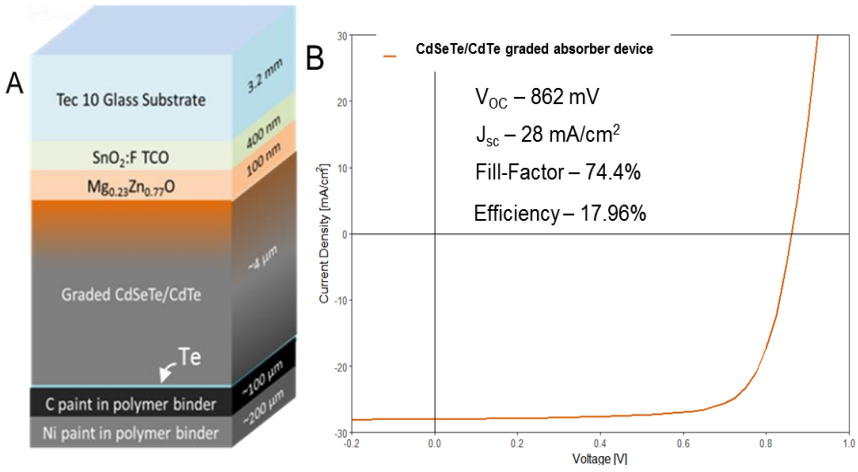

Figure 1: (a) Schematic of device structure (not to scale) under study and (b) Representative device performance immediately after cell fabrication.

*correspondence: imathews@mit.edu

$CdCl_2$ passivation treatment, the substrate was moved to a cooling station without any active heating and allowed to cool for 180 s. No annealing post $CdCl_2$ treatment was performed during this experiment. After this process step, the substrate was removed from the vacuum chamber and the residual $CdCl_2$ film was rinsed using de-ionized water.

Thereafter, the films were heated to ~140°C, and CuCl was deposited on the film surface for 110 s. This was followed by 220 s of annealing at 220°C, both in vacuum, to form a Cu doped back contact. A ~30-nm Te film was evaporated to improve the back-contact that has shown improvement in device performance in CdTe-only as well as CdSeTe/CdTe graded absorber devices [11], [14]. Carbon and nickel paint in a polymer binder were sprayed on these films to form the back electrode. After carbon and nickel back electrode films were masked and delineated to form 10 small scale devices with an area of ~ 0.65 cm^2. A schematic outline of the device structure used for this study is shown in Figure 1(a), while Figure 1(b) shows the current-voltage performance of a representative cell out of 25 cells measured immediately following cell fabrication.

The photovoltaic cells 1 sun characteristics were measured using a Solar Simulator that included an Oriel 3A Class AAA Solar Simulator and an AM1.5G optical filter designed to simulate the AM1.5G solar spectrum. Current–voltage sweeps were conducted using a Keithley 2400. A mono-Si reference cell, calibrated by National Renewable Energy Laboratory's Solar cell/Module Performance Group on March 6, 2018, was used when establishing 1 sun light intensity while a temperature control stage kept samples at 25 ^oC. The indoor photovoltaic performance measurement setup was housed in a dark box and used the same electronics as for 1 sun measurements, but the cell was illuminated using a dimmable Philips Hue E26 LED bulb. The intensity of this low-level illumination was controlled using the bulbs set points and was measured at the cell using a calibrated Si photodiode. The intensity of light on the solar cell was set for each measurement taken over a 0.2 – 3 W/m^2 range to mimic the expected illumination conditions in an office environment [6]. The EQE station included a Xenon lamp (with accompanying power supply), a monochromator and filter wheel assembly isolated light of a specific wavelength while optical mirrors guided the light onto the sample stage. The system measured the quantum efficiency by comparing the current from the device to a calibrated Si photodiode.

Results

The measured current-voltage curve for the CdTe PV cell used for low light measurements is presented in Figure 2(a) and shows the cell had an efficiency of 14.3% under 1 sun conditions with an open-circuit voltage of 840 mV, a short-circuit current density of 27.7 mA/cm^2 and a fill factor of 66% – the cell efficiency was lower than the best cell presented above owing to the low-light test set-up preventing probing of the best cells on the large glass substrate. Across five orders of magnitude decrease in AM 1.5G light intensity, as shown in Figure 1 (c), the V_{oc} of the measured cell decreases from 840 mV to 520 mV. The fill factor of the device increases with decreasing light intensity owing to the reduced impact of series resistance as the light generated current decreases. The efficiency of the device is presented in Figure 2 (b) and shows an initial increase to coincide with the increase in fill factor, but then a decrease as the reducing V_{oc} impacts efficiency. Overall the device performance under low-light AM1.5G compares well to other CdTe PV cells in the literature with an efficiency of 10% measured under 0.76 W/m^2 irradiance. Under the lowest light intensity, 0.14 W/m^2, the single cell maintains an open-circuit voltage of 495 mV and a maximum power point voltage (not shown) of 387 mV and an efficiency of 8.65%. The cell maintains significant power output and a stable operating voltage at very low light intensities suggesting the device would perform under very low-light indoor operating conditions.

*correspondence: imathews@mit.edu

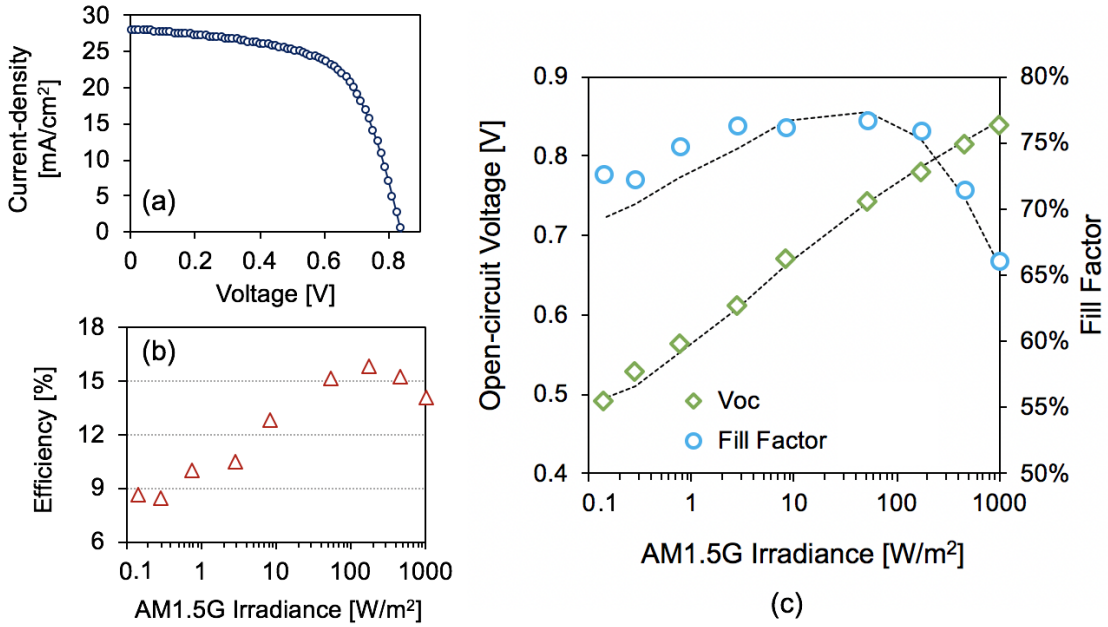

Figure 2: (a) Open-circuit voltage (green diamonds) and Fill Factor (blue circles) versus AM1.5G light intensity and corresponding fits to the data (dashed lines), (b) the measured external quantum efficiency of the cell, and (c) the measured photovoltaic conversion efficiency versus AM1.5G light intensity.

A fit of the electrical parameters of the cell to these measurements allows us to investigate the impact they have on the cell performance at different light intensities. We fit a two-diode model (Equation 1) to the data and begin by assuming the ideality, n_1 =1, and we set a limit to the maximum possible R_{sh} of $1x10^6$ ohm.cm^2.

$$J = J_L - J_{o1}\left\{exp\left[\frac{q(V+JR_S)}{n_1 kT}\right]-1\right\} - J_{o2}\left\{exp\left[\frac{q(V+JR_S)}{n_2 kT}\right]-1\right\} - \frac{V+JR_S}{R_{sh}} \qquad (1)$$

Our model results fit the plots of V_{oc} and *Fill Factor* closely, as shown in Figure 2 (c). The fitted electrical parameters are provided in Figure S1 of the Supplementary Information. We found that J_{o2} dominates at all light intensity in our devices with an ideality of n_2 ~2 up to 200 W/m^2 before increasing to ~4 at 1000 W/m^2, while the shunt resistance, R_{sh}, of the device decreases with light intensity – a high shunt resistance is vital to maintain high performance at low light intensity where shunt pathways can be the main loss in most cells under low-light conditions [16]. Our parameter fit shows how our CdTe cell is uniquely suited to low light IoT applications and explains why significant voltages are produced even at the lowest light intensities. The series resistance, R_s, also remains low across all light intensities, < 7 ohm.cm^2, indicating the quality of the TCO contact layer. In comparison to silicon cells, where the current path changes with light intensity and impacts R_s, in our cells, it remains relatively low as the only current path is through the TCO and there is no metal contact pattern.

Finally, to gauge how the cell will operate under indoor light conditions, we measure its efficiency under low-light LED irradiance in a 0.2 – 2.9 W/m^2 range – similar to 100 – 1000 lux levels in buildings. The results are plotted in Figure 3 (a). Again, the V_{oc} remains above 500 mV across all light intensities. The peak efficiency measured is 18.45% under 2.9 W/m^2 while an efficiency of 15.2% is measured under the lowest light intensity of 0.2 W/m^2. The cell efficiency remains above 17% down to a light intensity as low as 1 W/m^2 – these values are the highest measured for CdTe IPV cells under ambient lighting and compare favourably to other thin-film technologies such as GaAs where a maximum efficiency of ~20% has been measured using a flexible cell under 1.3 W/m^2 LED lighting [1]. This high

*correspondence: imathews@mit.edu

efficiency is partly attributable to the close match between the absorption and carrier collection of the 1.41 eV device as shown by the measured external quantum efficiency (EQE) of the device, presented in Figure 3 (b), to the measured incident spectrum from the LED lamp, also shown, and highlights the close match between the EQE of the device where it remains over 90% in a 400 - 830 nm range, with the peak of the spectrum between a 500 – 700 nm range.

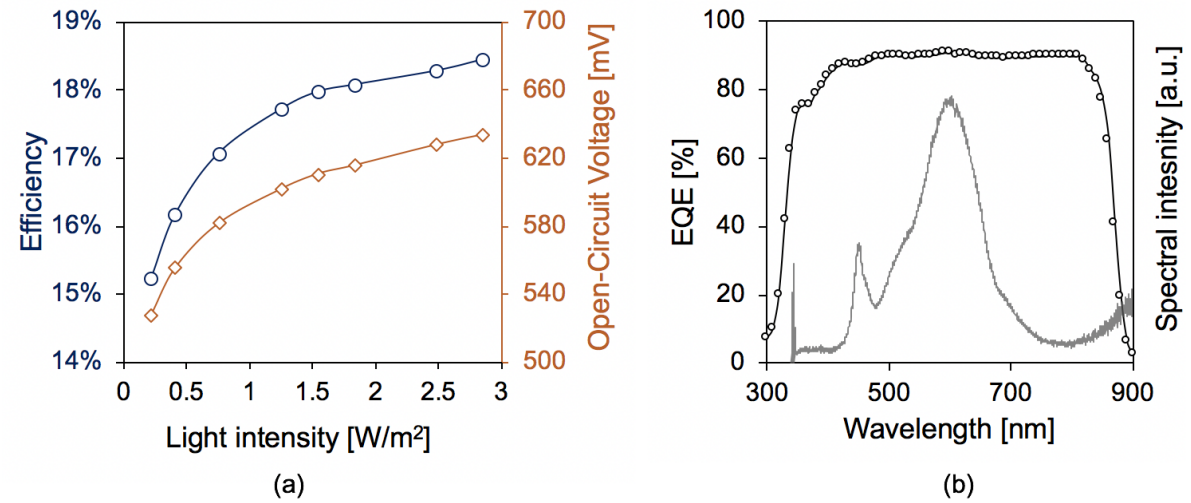

Figure 1: The CdTe PV cell efficiency and Open-Circuit Voltage under low intensity LED irradiance that is equivalent to ~200-2000 lux.

Discussion

Although still below the best indoor PV devices in terms of efficiency, CdTe has impressive performance at very low light levels. Combined with the know-how available around its manufacturing at scale, CdTe solar modules long-term stability and the low manufacturing cost compared to other PV technologies, CdTe is a strong contender for indoor PV applications.

Our modelling recently established the cost to manufacture single-junction CdTe solar modules at 42.44 US$/m^2 [17]. This represents the number for a large ~1 m^2 module produced in a factory with a maximum production capacity of 300 MW/year. Producing smaller IoT modules would lead to a loss in economies of scale both in terms of final product size, that will be on the cm^2-scale, and production capacity when only MWs are likely to be required each year. This number implies a minimum cost to produce a 10 cm^2 IoT module of ~4 US cents. We consider this value the minimum possible and a better understanding of the impact of economies of scale is required to determine the exact cost of the technology for IoT applications as we have seen undertaken for perovskites [18].

Nevertheless, CdTe is likely to be a low-cost option for IoT applications which combined with the high prices that can be obtained in this growing market [19], can justify the likely increase in production cost. Currently, CdTe companies ship GWs of solar modules each year and this market is likely to increase in the future as the solar power market grows. In the interest of diversification of revenue streams, the indoor IoT space is expected to grow to a US$1 Bn market by 2025 [1]. Although smaller than the solar power market, capturing a portion of it would add a significant revenue stream for established CdTe manufacturers. The high prices that can be obtained for products in this market could likely support manufacturing in higher cost regions such as the USA and EU and act as a testing ground for new technologies before production is scaled to enter the wider solar power market.

Owing to the use of Cd, any discussion on CdTe for indoor photovoltaics must include a section on the restriction of hazardous substances (ROHS) regulations. Currently, the most comprehensive regulations have been enacted in the EU where the ROHS directive 2011/65/EU came into full effect on the 22nd

*correspondence: imathews@mit.edu

July 2019 and applies to all electrical and electronic goods regardless of their type, design or purpose. The Directive bans anyone from placing on the EU market electrical and electronic equipment (EEE) in which any homogeneous material contains more than the tolerated maximum concentration values (MCVs) of six substances including Cadmium. In fact, the tolerated MCV for each restricted substance is 0.1%, or 1,000 parts per million (PPM), except for cadmium which has a stricter limit of 0.01% or 100 PPM. In this context a homogeneous material is one that has a uniform composition throughout, or any component of the finished product that cannot be removed or detached by any action such as unscrewing or cutting, i.e., the whole CdTe IPV panel can likely be treated as a homogenous material placing a limit on the thickness of the CdTe material that is a function of the thickness of the other materials in the PV stack. The glass substrate will make up the majority of a stack, and in our experiments has a thickness of 3.2 mm, placing a limit on the thickness of the CdTe film of ~640 nm (assuming the film is 50% Cd). While this is thinner than the current device design, photovoltaic films of this thickness are reasonable for indoor applications owing to the strong absorption of the shorter wavelengths in CdTe, and suggests a well-designed CdTe IPV device on glass should satisfy ROHS regulations. More generally, some types of EEE are exempt from restrictions on the use of hazardous substances including photovoltaic panels for public, commercial, industrial or residential use. In practice, under WEEE regulations [20], photovoltaic module manufacturers such as First Solar are responsible for the full life-cycle of their modules including the collection and recycling of panels. First Solar modules have been designed for recycling where 90% of the materials in each module is recoverable and they have built recycling facilities all over the world [21].

Conclusions

CdTe is the most successful thin-film photovoltaic technology on the solar power market today. Here, we investigated the suitability of a CdTe photovoltaic cells to be used as a power source for wireless sensors located in buildings to expand the range of applications for this technology. Our cell structure was fabricated with a TCO front contact that provided for high photocurrents and low series resistance at low light intensities – leading to significant power output and stable operating voltages at very low light intensities. Efficiencies of 10% and 17.1% were measured under 1 W/m^2 AM1.5G and LED irradiance respectively indicating CdTe devices are very suited to operation under low-light indoor conditions. While a greater understanding of the impact of economies of scale on the likely IoT module price is required, CdTe is a low-cost technology and it is likely that the higher prices obtainable in the IoT market will offset the extra cost in manufacturing small modules. While consideration is needed to ensure CdTe IPV modules will pass ROHS regulations in each geographic market, it is clear that this technology has significant potential to power the internet of things.

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*correspondence: imathews@mit.edu

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*correspondence: imathews@mit.edu