PARITY SIMULATION OF STATIC POWER CONVERSION SYSTEMS

by

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ABSTRACT

Static energy conversion systems are extremely difficult to analyze, design and control. When one requires a knowledge of issues such as transient behavior, fault effects, stability or design optimization, such systems must be investigated through the use of models. Conventional digital or analog approaches are severely limited in their usefulness when dealing with static energy conversion systems. A new modeling technique, Parity Simulation, is described which is both conceptually and philosophically distinct from presently employed digital and analog modeling techniques.

Parity Simulation provides a hybrid model in which the power circuit containing all the switching elements is modeled using synthetic element modules with each module simulating one element in the actual circuit. Consequently there is a high degree of correspondence between the topology of the model and the topology of the existing system. The existence of this topological isomorphism allows a true "bread board" approach to simulation.

A Parity Simulation model of a thyristor is developed and evaluated. The concept is explored in the application content and is shown to be both accurate and versatile. Results of a Current Commutated Chopper Simulation, and a Series Inverter Simulation are presented and compared with actual circuit behavior.

THESIS SUPERVISOR: John G. Kassakian

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GLOSSARY

NOTE: Unless otherwise mentioned, the subscripts listed below will identify the definitions of the symbols used in the text.

Subscripts

a	Actual circuit parameter
s	Simulated circuit parameter

Symbols

[A]	Digital attenuation facter
C_{tc}	Astable timing capacitor
F	Output of state inductor
f_c	Ringing frequency
f_u	Unity gain cross-over frequency
I_{FS}	Full scale output current of DAC-08
I_H	Holding current of the thyristor
I_{Ref}	Input reference current of the DAC-08
I_s	Diode saturation current
i_R	Reverse recovery current
K	Boltzmann's constant
K_f	Frequency scale factor
K_I	Current scale factor
K_v	Voltage scale factor
Q	Recovered charge
q	electronic charge
R_F	Feedback resistance

R_L	Load resistance
R_{tc}	Astable timing resistor
r_D	Dynamic resistance
T	Absolute temperature
t_{on}	Turn-on time of the thyristor
t_{rr}	Reverse recovery time
V_{AK}	Anode cathode voltage
V_T	Instantaneous on-state voltage
v_c	Capacitor voltage
Z_{in}	Input impedance

CHAPTER 1

INTRODUCTION

Early applications of silicon controlled rectifiers (SCR's) were restricted to devices which required low power and modest voltages because the rating of the SCR's was limited to a few hundred volts peak. Despite this limitation, SCR's found their way into lamp dimmers, phase control motor drives, and inverters for small power supplies. With the development of the chopper in the early sixties, SCR's of a higher rating were developed in order to accommodate the kVA ratings of equipment for specific functional areas of applications.

Technology must keep pace with the needs and demands of the changing sociopolitical structure. Often technology itself helps shape the reliability constraints placed upon it by society. Such is the case, for example, with the technological growth in the static power conversion area. The increasing problems resulting from the demand for greater reliability and from society's rising consciousness of the importance of product quality have stimulated engineers to turn to technology for a solution. A number of developments have been made technologically more attractive because of progress in SCR design and application within the past few years. Moreover, the increasing economic attractiveness of power thyristors is causing a further upsurge in the application of SCR's. Thyristor ratings of 4000 amperes for a single device and up to 200,000 amperes for multiple arrays are being proposed.

With the varied applications of these high current SCR's, the necessity for different evaluation methods arose. SCR power circuits rarely can be satisfactorily analyzed, except under the simplest

conditions; the analysis problem is particularly untractable when dynamic behavior is analyzed resulting from control system interactions or anomalous operating conditions. In such cases, one must resort to the use of models. These models can assume many forms, among which are the physical breadboard, the analog computer, the digital computer, and the hybrid computer, the latter being a composite of the previous two.

Analog and analog/digital computer simulation of static power conversion systems are powerful tools for the analysis and synthesis of electric power systems. The conventional analog computer, however, possesses several unfavorable characteristics: 1) the modeled physical system must be reduced to a mathematical system of state equations before being implemented on the computer; 2) patch-panel set-up is laborious and time-consuming; and 3) there is no correlation between the topology of the interconnected elements in the computer and the topology of the modeled system. This last characteristic is due to the fact that the conventional analog computer represents all state variables of the state equations as voltages whereas in the physical system the state variables are both voltages and currents.

This thesis presents a new approach to the modeling and simulation of static power conversion systems. This new approach designated "Parity Simulation", is specifically designed for switching circuits which employ dual-state elements such as diodes, transistors and thyristors for the processing of electrical power. There is a one-to-one correspondence between the physical elements of the system and the elements of the model. Whereas the conventional modeling approaches are rather inflexible with respect to changes in system topology and

limited in their interactive capabilities, Parity Simulation is designed to provide a high degree of investigative interaction and the ability to change element values or circuit topology with relative ease. The existence of such topological isomorphism allows a true "breadboard" approach to simulation. Design and construction of the element modules is discussed, demonstrating its practicality in three specific applications.

CHAPTER 2

SIMULATION APPROACHES

The decade of the sixties has truly been an explosive era for electrical engineering, particularly in the area of industrial electronics where the coming of the age of solid state devices has resulted in a virtual revolution in their application. The fast-growing success of the thyristor is paralled by the growth of its associated problems. It is simultaneously a rectifier, a high-speed static latching switch, and a high gain amplifier. Most of its characteristics are far superior to a transistor, since it has far greater power handling capabilities, both voltage and current, under both continuous and surge conditions. All the above assets of the SCR are still being improved upon, and the limitations and short-comings are becoming less significant as time passes. Newly introduced high voltage SCR's have raised the operating voltage barrier; high-speed SCR's allow operation at ultrasonic frequencies and under severe dynamic conditions. Most important, SCR's for every type of application.... industry, military, aerospace, or commercial are more economical than ever. This has contributed significantly to the increasing tempo of applications of this most influential member of the thyristor family.

Design considerations have certainly changed since the late sixties. Considerable attention is now paid to the changing SCR characteristics and limitations as they significantly affect equipment design. Voltage ratings provide a good example, for while dV/dt capabilities have risen by more than an order of magnitude in the past decade, dV/dt still remains an area of prime concern to the designer. First, because device voltage and current ratings have more than doubled; second, shorter turn-off time has resulted in higher operating frequencies with their corresponding increases in current

imposed dV/dt stresses ($L\frac{di}{dt}$ voltages). These higher voltage-rate stresses have kept up with, and in some applications have surpassed the gains made in device dV/dt capability, during the recent years. Other important aspects of these devices are 1) the static characteristics such as forward voltage drop, holding current, and 2) dynamic characteristics such as $\frac{di}{dt}$, turn-off time, etc. These characteristics, alone or together, strongly influence the thyristor's use in power conversion systems.

2.1 Evaluation Methods

The power circuits of static power conversion systems are deceivingly simple when compared with circuits comprising linear small signal processing systems such as communications equipment. The behavior of the latter, however, yields to a straightforward theoretical analysis, based on certain simplifying assumptions, the foundations of which are well established. This means that much of the required information can be obtained from the manufacturer's technical data sheets. Using this data in conjunction with standard theoretical principles and assumptions, the designer can fabricate a circuit which will almost certainly meet the required specifications.

Static power conversion systems, on the other hand, are not so easily designed. They are difficult to analyze, except under the simplest conditions. No set of hard and fast rules are applicable, and no dependence on assumptions of symmetry or balanced operation can be made. Worse, dynamic operation is almost impossible to analyze especially when closed-loop optimal control is involved. Nor is it any easier to analyze partial failure conditions in circuits where a device may have failed, either in the open or shorted mode. In such cases one resorts to the use of the basic "building block" of engineering - models.

2.2 Methodology of Simulation

Like other types of scientific analysis, electrical engineering is based on the formulation of models. To be useful, a model must, in general, simplify and abstract from the real situation. All these assumptions made by the model need not be exact replicas of reality. If it were exact, the model would be too complicated to use. The basic reason for using a model is that the real world is so complex that masses of details often obscure underlying patterns. However, a model may also be so over-simplfied that it is utterly useless. The trick is to construct a model so that irrelevant and unimportant considerations and variables are neglected, but the major factors - those that seriously affect the phenomena the model is designed to predict - are included. Models are of many forms, the principal ones being the physical breadboard, the digital computer, the analog computer, and the hybrid computer. These are briefly discussed in the following sections.

2.3 Breadboard Simulation

Of the four basic approaches to modeling cited, the breadboard is perhaps the most commonly employed. Often it consists of simply building the system, usually to scale, and experimenting until the desirable operation is obtained. Because of the rather unforgiving nature of power electronic systems, breadboarding is the least flexible of all existing simulation approaches, and provides the least insight into the margins for reliable operation and operational behavior under unusual system conditions. The advantage of the breadboard approach is that it requires no special facilities except patience and a good supply of devices.

2.4 Digital Computer Simulations

In principle, the digital computer is the ideal vehicle for model studies. Indeed, digital simulations of complex "quasi-linear" systems have been highly successful in predicting the response of circuit behavior to perturbations in element values caused, for instance, by radiation.[1] As a practical matter, however, the digital computer has been inflexible and expensive when applied to systems employing numerous switching elements, each of which cause a change in system topology. Its principal advantage is its availability.

2.4.1 Attributes Associated with the Digital Computer

Advantages

1. Handling of dependent variables, and data within the computer in quantized or discretized forms.
2. Accuracy relatively independent of the quality of system components and determined primarily by the number of bits contained in memory registers and by the specific numerical technique selected.
3. Facility for memorizing numerical and non-numerical data indefinitely.
4. Facility for floating point operation, thereby eliminating scale factor problems.
5. Facility to perform logical operations and decisions utilizing numerical and non-numerical data.
6. Ability to trade-off solution time and accuracy.

Disadvantages

1. Serial operation, involving time-sharing of all operational and memory units, only one or a limited number of operations being carried out at one time.

2. Solution times relatively long and determined by the complexity (number of arithmetic operations involved) of a problem. Disparate time-constants constitute a big problem too.
3. Ability to perform a limited number of arithmetic operations including particularly additions and multiplications; more complex operations such as integration and differentiation must be performed by approximate (numerical) techniques.
4. Programming techniques bear little if any relationship to the engineering problem under study, but facilitated by compilers and special interpretive routines.

2.4.2 Problem Solving Using a Digital Computer

Problems are usually solved on a digital computer by establishing a set of state equations of the form

$$[\dot{X}] = [A][X] + [B][U]$$

describing the response of each possible topological state of the circuit.[2,3,4,5] This set of equations is then integrated to obtain the desired response. The system state will change when a particular, predetermined condition of state variables exists. The program must check for these conditions at frequent intervals and respond by establishing the new set of state equations. If the number of possible states is small enough, the state equations may be obtained a priori, and entered as part of the network data. More complex systems are often treated by employing a nonlinear resistor as the switching element.[6] This approach has the advantage of providing a constant topology system, but runs the risk of introducing arbitrarily small time constants which can create havoc with numerical integration routines, if not treated properly,

a general problem of solving stiff systems numerically. A large inductance in series with the resistor in the off-state solves the stiffness problem, but prevents one from modeling reverse recovery current.

An alternate approach to integrating the state equations directly is to formulate the solution for each state in terms of the network A-matrix. Under appropriate assumptions particularly linearity, the response may be expressed rather simply in terms of the e^{At} matrix.[7] In this case, there may be an increase in computational efficiency over the straightforward integration of the state equations. However, the overhead associated with the desired topological and interactive flexibility is the same for both approaches.

2.5 Analog Computer Simulation

The analog computer has been successfully employed in the simulation of static conversion systems by a number of researchers.[8,9,10] The analog approach is similar to the digital approach in that both require the network to be formulated as a system of state equations. Digitally the equations are numerically integrated whereas the analog computer uses operational amplifiers to perform the integration.

2.5.1 Characteristics of Analog Computer Simulations

The following attributes are generally associated with the analog computer.

1) High speed or "real time" operation with computing speeds limited primarily by bandwidth characteristics of the computing elements and not by the complexity of the problem.
2) Dependent variables in the machine treated in continuous form.
3) Parallel operation with all computational elements operating simultaneously.

4) Great degree of control flexibility, and has provisions to permit the engineer to experiment by adjusting the coefficient settings on the computer, thereby gaining direct insight into system operation.

5) Ability to perform efficiently such operations as multiplication, addition, integration, and nonlinear function generations; on the other hand, very limited ability to make logical decisions or store numerical data.

6) The incorporation of switching devices is not a straightforward procedure. Generally this incorporation requires the artiface of a small inductance in series with the switching device to transform the branch current into a state variable. Even for systems of moderate complexity, the number of analog elements required in the simulation becomes quite large relative to the number generally available.

7) The interconnection of the analog computer, done manually via a patch board bears no correspondence to the original system topology. The impossibility of topological correspondence becomes apparent, when one realizes that in the simulation, state variables are all represented by node voltages whereas in the actual network, the state variables are a combination of node voltages and branch currents. The result is a model in which it is extremely difficult to incorporate topological changes, thus limiting its usefulness as a design tool.

8) Simulation of electrical systems on the analog computer involves setting up of the electrical circuit in consideration, obtaining the state equations and finally transforming them to another electrical circuit which is then patched on the board. This complex simulation procedure could be simplified if the state equation determination and transformation could be eliminated - a procedure which is not feasible at this time.

2.6 Hybrid Computing Techniques

Hybrid computing techniques inevitably represent an effort to combine in one computer system some of the characteristics normally associated with analog systems and some of the characteristics associated with the digital computer systems. In the actual sense of the term, a "hybrid computer system" involves the actual interconnecting of analog and digital portions within the system, such that both computers play an equally important role in the data handling process.

2.6.1 Motivation for Hybridization

Generally speaking, hybrid computer techniques are frequently employed to overcome certain shortcomings in present day analog or digital computers. As these limitations are reduced or eliminated, it is possible that some applications for hybrid computing systems will disappear. The following are, at present, the chief motivations for interconnecting digital and analog computers:

1) To combine the speed of an analog computer with the accuracy of a digital computer.
2) To permit the use of system hardware in a digital simulation.
3) To increase the flexibility of an analog simulation by using digital memory and control.
4) To increase the speed of the digital computation by using analog subroutines.

2.6.2 Spectrum of Hybrid Computer Applications

By far the most widespread application for hybrid computer systems has been in the simulation of distributed parameter systems. A mathematical model of a system to be designed is first formulated, and the equations

constituting this model are programmed on the analog computer. The objective is usually to facilitate the study of the effect of parameter modifications and the excitation-response relationship of the overall system. Some of the more important areas are sampled-data system simulations, random processes simulation, system optimization, trajectories of aerospace vehicles and process control systems. However, in all of the above modeling applications, the voltage representation of state variables is of no consequence since the physical system must be reduced to a mathematical representation before analog implementation anyway. When modeling an electrical system with an electrical analog, however, considerable facility is to be gained if there is a high degree of "equivalence" between the physical elements of the system and the elements of the model. In the case of the analog computer the interconnection of analog components done manually, via a patch board, bears no correspondence to the original electrical topology. The impossibility of topological correspondence becomes apparent when one realizes that in the simulation, state variables are all represented by node voltages, whereas in the actual network, the state variables are a combination of node voltages and branch currents. The result is a model in which it is extremely difficult to incorporate topological changes, thus limiting its usefulness as a design tool.

2.7 Parity Simulation

The power circuit of static power conversion systems generally consist of a relatively small number of discrete elements. This is then embedded in a control system incorporating both digital and analog components. If one addresses systems of this class, rather than the global problem of general circuit modeling, a very powerful model can be constructed. Parity Simulation does this by providing a hybrid model in which the power circuit,

containing all the switching elements, is modeled using synthetic element modules, and the control subsystem is simulated, for the most part, on a micro-processor based mini-computer. The mini-computer also provides simulation control, data processing and interactive graphics.

The power of the system results from the flexibility provided by the correspondence between the system and model topologies. This not only allows efficient "programming", but also permits topological changes to be incorporated in a straightforward manner. The element modules consist of electronic analogs whose terminal characteristics are described in terms of voltage and current. In this sense they differ from the conventional analog computer elements in which all circuit variables are represented by voltages. Currently there are modules to model inductors, capacitors, resistors, thyristors and diodes.

Figure 2.1 shows a block diagram of the Parity Simulation (11) system concept. The main parts of the system are the mini-computer and the element modules. Operator instruction is through a CRT display and key-board. Digital control of the element values allows the computer to calculate the scaled element values from specified scale factors as well as to change the element values for performance optimization. The circuit is wired by the computer using a switching matrix via instructions from the key-board. The circuit schematic can then be graphically displayed and interacted with in a manner analogous to that employed with a traditional breadboard: branch currents or node voltages can be observed, element values can be changed, and elements can be added or removed. Unlike the breadboard, however, fault conditions and failure modes can be investigated in a nondestructive fashion. There is also the possibility of including in the simulation digital models for components such as machines. These digital models are contained in the digital

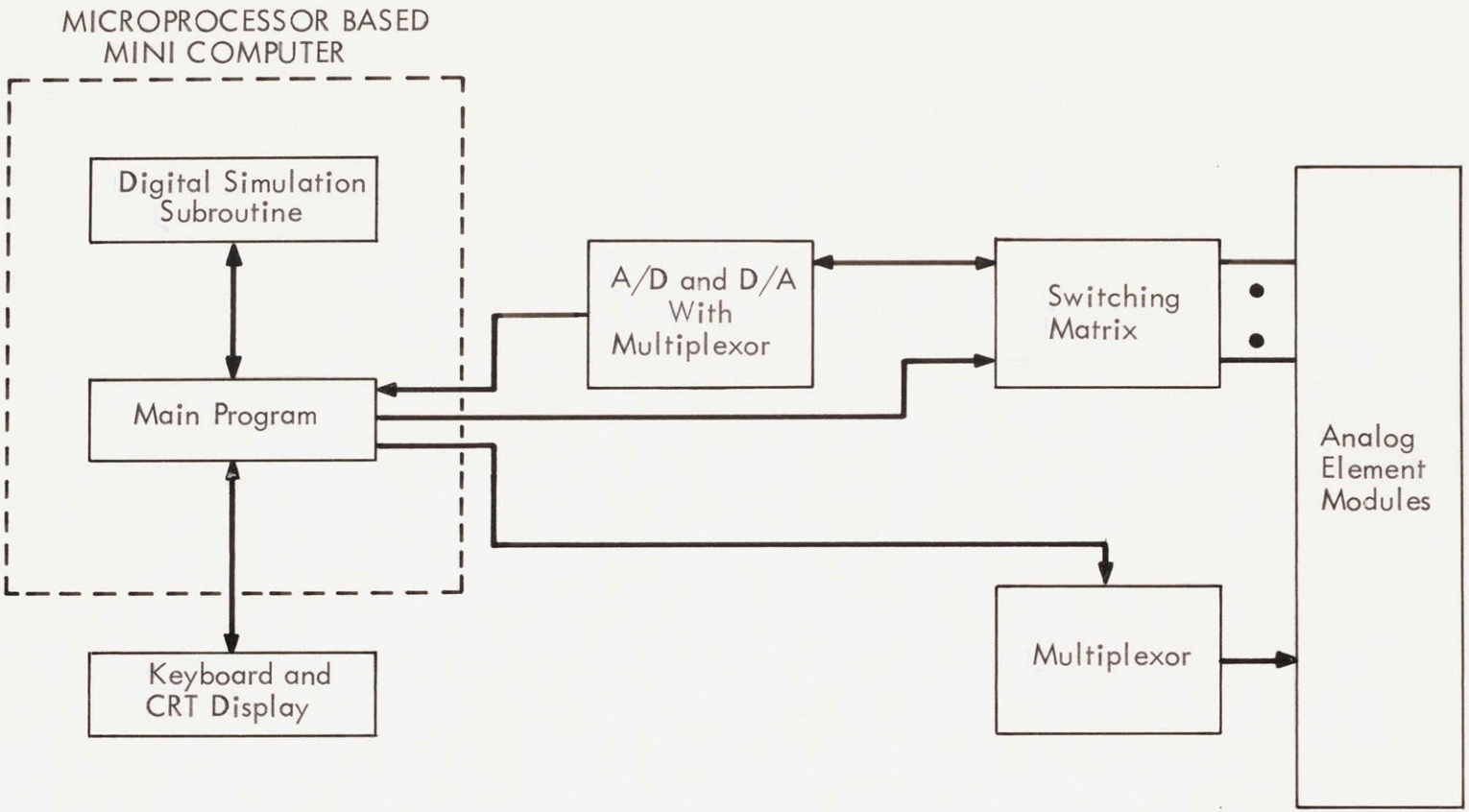


Fig. 2.1 Conceptual Block Diagram of the Parity Simulation System

simulation subroutines block of Fig. 2.1 Thus, the variety of components that may be included in a simulation is greatly increased.

The size of the system modeled on the Parity Simulator is virtually unlimited, the biggest problem being the automated interconnection matrix. Because of the topological parity, there is a 1:1 correspondence between the number of elements in the actual system, and the number of elements in the simulation. In the conventional analog computer, this ratio is generally considerably greater than 1, and the number of available components is limited by the size of the patchboard.

The real time digital computer interface makes possible the digital modeling of certain system elements, such as rotating machines. Since these elements can be described by a single set of state equations for the entire duration of the simulation, a digital implementation poses no obstacle. The particular computer used, of course, will determine what limitations must be imposed on such digital models. The digital/analog interaction in the Parity Simulator includes all capabilities of the conventional hybrid simulator with the important additional feature that elements can be added or removed during an automated system investigation. In the conventional hybrid, such topological changes must be anticipated and the patchboard wired accordingly. This capability makes the Parity Simulator, in concept a powerful vehicle for the development of "intelligent" computer aided design or parameter optimization algorithms.

2.7.1 Element Modules

The Parity Simulation technique is developed specifically for electrical energy conversion systems incorporating static and kinetic components. At present this simulation technique uses five types of synthetic element

modules - inductor, capacitor, resistor, thyristor and diode. Except for the thyristor these are two terminal modules through which a physical current may flow. The thyristor differs in that it is a three-terminal device. All elements with a value parameter incorporate multiplying DAC's (digital-to-analog converters) which allow the element values to be set digitally. Element values can be chosen over a range of eight decades. By incorporating decade switching with the multiplying DAC, an element value resolution of 1% is achieved. The digital control of element values allows great flexibility in introducing nonlinear elements such as saturating magnetic circuits. The synthetic element modules are discussed in detail in the succeeding sections.

2.7.2 Parity versus Analog Computer Simulation

The Parity Simulation technique has a high degree of correspondence between the topology of the model and the topology of the actual system. This allows the Parity Simulator to explicitly represent the system topology as against the analog computer which explicitly represents a set of state equations.

The analog computer's circuit representation on the patch panel bears no correspondence to the original system topology. State variables are all represented by node voltages, as against node voltages and branch currents in the actual network. Hence topological changes in the analog computer are extremely difficult to incorporate, limiting its usefulness as a design tool.

The modeling of switching elements on the analog computer generally requires the artiface of a small inductance in series with switching device to transform the branch current into a state variable. Even for systems of moderate complexity, the number of analog elements required in the simulation

becomes quite large relative to the number generally available. Certain assumptions can be made regarding the periodic nature of the response in order to minimize components, but such assumptions limit the model's usefulness, particularly with respect to unbalanced operation of polyphase systems.

On the other hand, in the Parity Simulation there is complete "parity" between the model and the actual system. All variables are topologically the same; voltages and currents in the actual circuit being represented by corresponding voltages and currents in the Parity Simulator. This not only allows greater flexibility in permitting topological changes, but allows parasitic effects, such as ringing due to snubber dynamics, to be easily incorporated. Models of rotating machines are as easily incorporated; modules for these machines can be designed to have all key parameters modeled in them so that "restricting assumptions" do not have to be made which would severely limit the model's usefulness. This is particularly true in the operation of large systems. There is no limit on the degree or order of nonlinearity, nor is there any restriction on the size of the modeled system. Modifications in the parameter values can be incorporated without any "plugboard repatching" as required in the analog/hybrid approach. Of course there is also completely interactive operation between the time dependent model parameters with real time data-processing and decision making. Automated design optimization can also be incorporated making the Parity Simulator a powerful tool for the design engineer.

2.7.3 Capabilities of the Parity Simulator

Due to the topological isomorphism in the Parity Simulator, numerous applications can be stated. Of course, this simulation technique is most outstanding in electrical systems with an electrical analog. The basic

objective in this system is to facilitate the study of the effect of parameter variations and topological modifications on the system. In this section, a brief description of some of the more important application areas is presented.

A) Variable Frequency Converters

The introduction of the silicon controlled rectifier has resulted in a new interest in static power frequency changers. These frequency changers can be subdivided into two classes, that is, frequency changers of the cycloconverter type or frequency changers of the DC link type. The accurate simulation of such a system would require the use of a Parity Simulator. This application is of considerable importance, because of the increasing utilization of frequency converters, both in air-borne and earth-bound transportation systems. Clearly, the various dynamic characteristics such as peak currents and voltages, load power factor and turn-off time presented all have an important effect on the overall system performance. Moreover, the effect of changes in component values, topology or control algorithms all play a major role - a role which the Parity Simulator can accurately model and correctly simulate.

B) HV DC Systems

Since the late sixties research and development of the high voltage thyristor has been actively promoted. Any HV DC system using thyristors contains several thousand individual electronic components. A detailed quantitative analysis would be extremely difficult to carry out. Parameter simulation techniques can be used to model the more important parameters of the system and thus to obtain necessary information regarding the system performance and reliability of operation.

C) Static Inverters

The greatest percentage of power utilized in all applications is in the form of alternating current. However, a great number of power sources are DC. The inverter is a convenient way to transform this power into the more usable AC form. An additional advantage is the ease with which the inverter transforms DC into AC with a wide variety of output frequencies for control purposes. The output waveforms vary widely with the application and the circuit that is used - usually being a square wave. Parity Simulation of inverters is immensely helpful in demonstrating the dependence of various parameters on the element values, with the operation even in the "partial failure mode". Harmonic analysis of the output waveform and design optimization are a few of the other control system applications which can be conveniently simulated on the Parity Simulator.

D) Simulation of Choppers

Choppers are used to obtain a variable DC voltage from a constant DC source. Frequency or pulse width modulation techniques can be used, the variable DC voltage being used to feed the armature of a DC machine, thus controlling its speed. The Parity Simulation technique is well suited to simulate the action of the chopper and even of the DC machine if necessary; going a step further, it could also simulate the entire control scheme. This makes it a very powerful tool in the hands of an experienced engineer who could simulate, and consequently optimize the entire system - the power circuitry as well as the control scheme.

E) Other Applications

Numerous other applications of the "Parity Approach" can be cited. Process control systems, DC/60 Hz conversion systems, uninterruptable power

supplies, lighting, welding, and induction heating. Furthermore, since the entire system can be very easily simulated, it seems likely that most problems involving high power devices will invariably be studied by means of the Parity Simulation techniques.

CHAPTER 3

INDUCTANCE SIMULATOR

The inductor is a two-terminal circuit element in which the terminal voltage is proportional to the time rate of change of current flowing through the elements.

3.1 Ideal Inductor

For the ideal inductor utilizing linear magnetic materials the terminal relations in terms of inductance L are

$$V_L = L\frac{di}{dt} \quad ; \quad i_L = \frac{1}{L}\int_0^t V_L\, dt + i_L(0) \qquad (3.1)$$

As with the ideal capacitor, the ideal inductor is lossless and has energy storage capability. This energy is stored in the magnetic field of the coil and is, later on, recovered when that field collapses.

As with other circuit elements, the ideal λ-ampere relationships of an inductor can only be approximated in practice. Circuit limitations in terms of frequency response, energy-loss mechanisms, and nonlinearities in the core, all combine to restrict the performance of an actual inductor to a very narrow spectrum as compared to physical capacitors and resistors. Moreover, due to the unusually large core dimensions encountered, the inductor is by far, the physically largest circuit element. For these reasons the designer tries to avoid the use of inductors in circuit applications.

3.2 Loss Mechanisms in Inductors

The performance of an actual inductor can never reach that of an ideal inductor. Nonlinear B-H characteristics, and energy losses both contribute to the actual inductor's departure from the ideal. Energy losses associated with the inductor fall into three categories:

a) Copper loss

b) Eddy current loss

c) Hysteresis loss

The first of these contributions is due to the I^2R heating which appears in the coil as a result of the circulating current. Second is the eddy-current losses. This is produced by currents in the magnetic material, and these currents are caused by electromotive forces set up by the varying fluxes. The third loss mechanism involves the behavior of the B-H curve, and is known as hysteresis loss. The hysteresis loss is a result of the energy required to reorient magnetic domains in the material. From the various loss mechanisms, the equivalent circuit of a lossy inductor can be determined.

3.3 Equivalent Circuit of a Lossy Inductor

An indepth circuit model which can represent the loss mechanisms in an actual inductor is shown in Fig. 3.1. This model is usually adequate for both air and iron-core inductors, except R_L, which represents the hysteresis loss, is removed for air-core types. The series resistance R_c represents the actual dc winding resistance, at low frequencies. This series resistance increases at higher frequencies because of skin and proximity effects. R_e represents the eddy

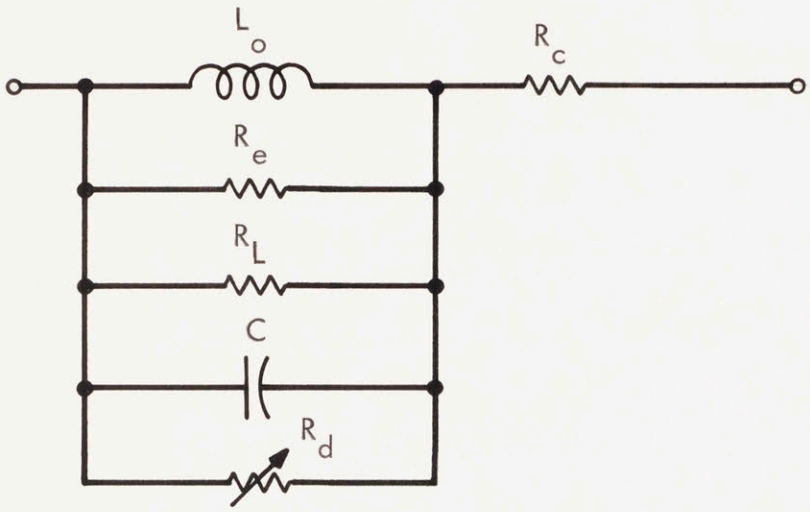


Fig. 3.1 Equivalent Circuit of a Lossy Inductor

current loss in the core and strongly depends on the resistivity and dimensions of the core laminations. All coils have distributed capacitance C, and the loss R_d in this distributed capacitance can be an important cause of reduction in the quality factor of coils at high frequencies.

3.4 Quality Factor of an Inductor

To obtain a measure of the relative figure of merit of inductors, a dimensionless quantity called the quality factor (Q) is often employed. The quality factor is given by

$$Q = \frac{2\omega \text{ (average stored energy in inductor)}}{\text{copper loss + core loss}} \qquad (3.2a)$$

If core loss is neglected,

$$Q = \frac{\omega L}{R_c} \qquad (3.2b)$$

where ω represents the angular frequency in radians and R_c, the copper loss in the windings. In a lossless inductor, $R_c = 0$ and hence $Q = \infty$ which represents the ideal case. The smaller the value of Q, the more lossy the inductor. In general, the quality factor Q is a function of frequency, flux density and the overall dimensions of core and coils.

3.5 Inductance Simulation

In Parity Simulation, the actual inductance is replaced by a two terminal device in which the terminal voltage is proportional to the time rate of change of the current flowing through the element. In

other words, this two terminal device behaves as an inductor and has a precisely controlled driving point impedance.

Scale factor requirements indicate that the simulated inductor can be up to six orders of magnitude greater than the actual inductance. This requirement can be clearly illustrated using the scaling example mentioned below.

The typical range of values for the voltages, currents and operating frequency in the actual circuit are:

$$V = 100 - 1000 \text{ volts}$$

$$I = 1 - 100 \text{ amps}$$

$$f = 60 - 10 \text{ kHz}$$

The scale factors for the simulation are

$$K_V = 10 - 100$$

$$K_I = 10^{+3} - 10^{+4}$$

$$K_f = 10 - 1000$$

where the subscripts V, I, and f denote voltage, current and frequency.

The simulated inductance L_s is given by

$$L_s = L_a\left(\frac{K_V}{K_I} K_f\right) \tag{3.3}$$

where L_a represents the inductance of the actual circuit. Calculations indicate the value of L_s to be $10^3 - 10^5$ times L_a. Obviously such large ranges are impractical except using op-amp based inductor simulations.

3.6 Simulation Schemes

Simulation of impedances, whether inductive or capacitive is invariably done using operational amplifiers. The versatility of op-amps allows the circuit designer many opportunities to create topologies which provide new and unique characteristics. These circuits use multiple feedback networks and can approximate transfer curves, perform mathematical operations and parameter enhancement. It is also possible to use these circuits to produce precisely controlled output or driving-point impedances, and hence to simulate an inductive reactance using capacitors as the reactive elements.

Two different schemes of simulating inductors using op-amps were considered. Both schemes provide simulated inductors that are relatively frequency independent and have moderately high Q-values.

3.7 Inductor Simulation by a Gyrator

It is possible to simulate the action of an inductor by a gyrator circuit which uses an active RC circuit to give the effects of coil action. The gyrator action is clearly shown in the circuit of Fig. 3.2, where two op-amps are used to provide a simulated inductor. The circuit relationships include

$$I_1 = \frac{V_i - V_a}{R_1} = -\frac{V_i}{R_1} \tag{3.4}$$

$$I_2 = \frac{V_i - V_b}{R_1} \tag{3.5}$$

$$V_b = -\frac{2\,V_i}{R_2\,Cs} \tag{3.6}$$

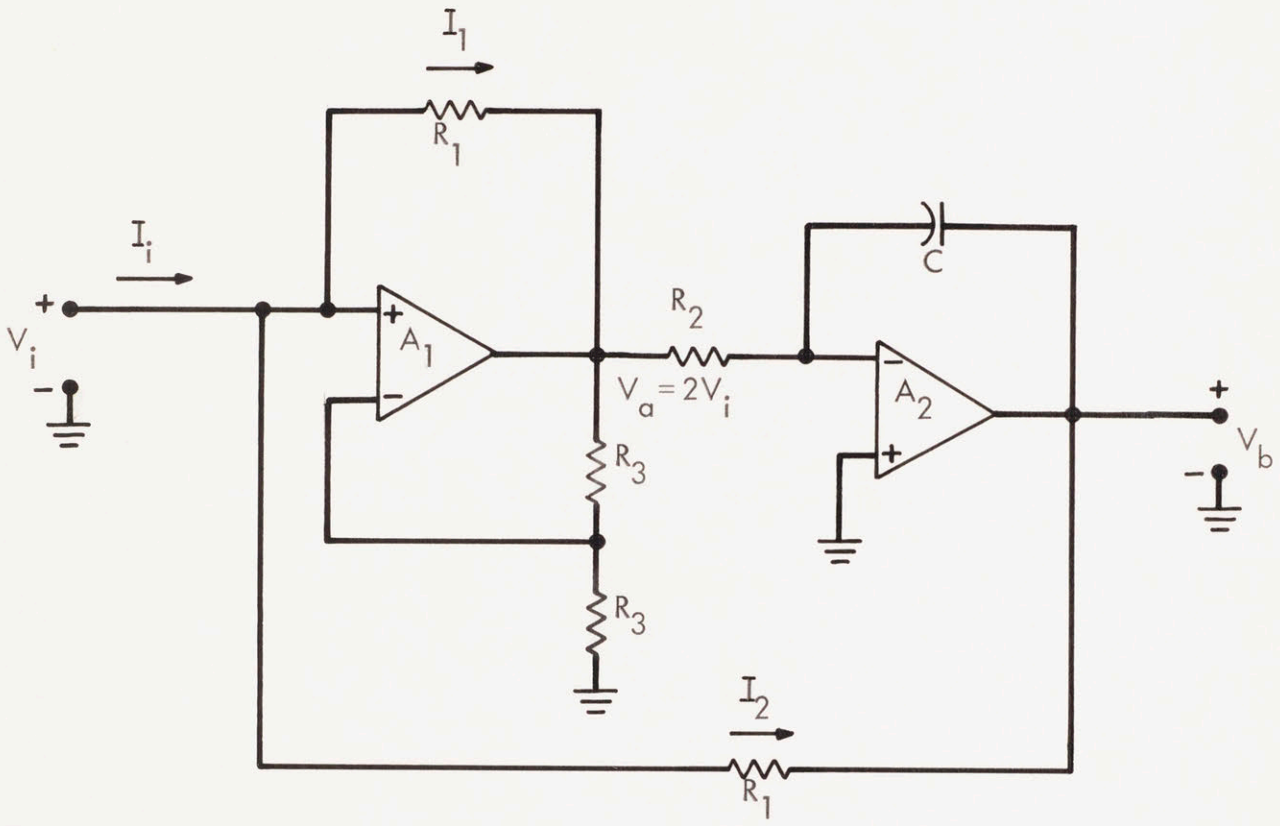


Fig. 3.2 Simulated Inductor using a Gyrator

$$I_i = I_1 + I_2 \tag{3.7}$$

Combining Eqs. (3.4) through (3.7), and solving for the transfer relationship $\frac{V_i}{I_i}$ shows that

$$\frac{V_i}{I_i} = \frac{1}{2}[R_1 R_2 Cs] \tag{3.8}$$

Hence this circuit can be used to synthesize elements that function as inductors using only capacitors, resistors and op-amps. However, the gyrator has one important drawback - the maximum voltage swing is limited to less than half the supply voltage. This is to prevent amplifier A_1 from going into saturation.

Hence another scheme is presented which simulates inductive reactance without the above-mentioned input voltage limitation.

3.8 Inductor Simulation Using a V-I-C

From Eq. (3.1), the inductor current is given by the integral of the voltage across the device. Hence an integrator in series with a voltage-to-current transformation circuit can be effectively used to simulate an inductor. The transformation is implemented using a voltage-to-current converter (V-I-C) and this converter together with an integrator forms the inductance simulator.

Figure (3.3a) illustrates the circuit diagram of the simulated inductor. Stage A_1 is an integrator which has a dc gain of R_I/R_o and a pole at $f_1 = \frac{1}{2}\pi R_I C_o$. Stages A_2 and A_3 are connected to form the voltage-to-current converter.

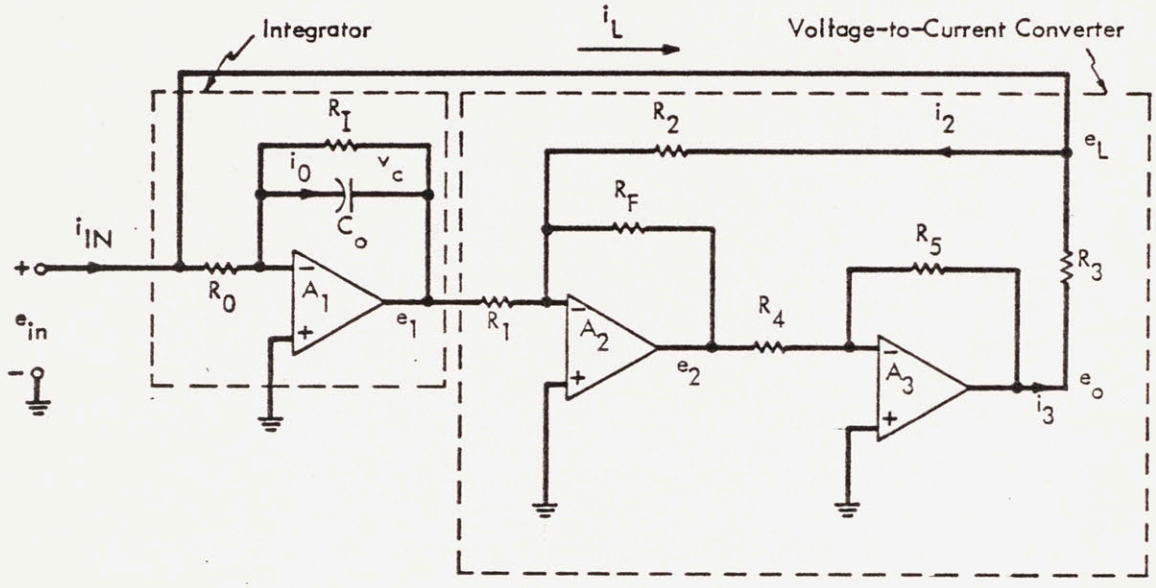


Fig. 3.3(a) Simulation of an Inductor Using a Voltage-to-Current Converter

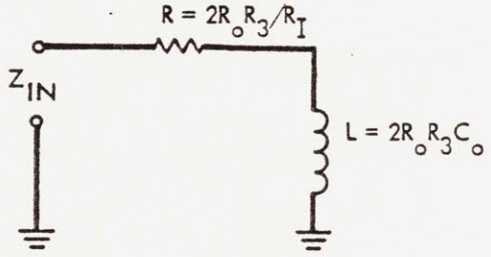


Fig. 3.3(b) Equivalent Circuit of the Simulated Inductor

3.8.1 Explanation of Operation

In order to illustrate the operation of the inductor circuit, it is necessary to find its closed loop transfer function. This may be obtained in the following manner:

3.8.1.1 Transfer Function of the Integrator

An ideal integrator produces an output voltage which is proportional to the integral of the input voltage. The integrator performs this mathematical operation on an instantaneous basis, producing an output proportional to the sum of the products of instantaneous voltages and vanishingly small increments of time. The integrator A_1 of Fig. 3.3a performs the integration function. Due to the presence of the feedback resistor, the transfer function of the integrator is given by:

$$\frac{e_1}{e_{1N}} = \frac{R_I/R_o}{1 + SR_I C_o} \qquad (3.9)$$

Equation (3.9) is the transfer function of the integrator. To transform e_1, the integrator output into current i_L, a voltage-to-current converter (V-I-C) is used.

3.8.1.2 Transfer Function of the V-I-C

Voltage-to-current converters are made with a simple application of Ohm's law; $I = \frac{V}{R}$. Hence a voltage amplifier and a sampling resistor are needed. The feedback voltage is generated across the sampling resistor R_s in Fig. 3.3a. From the transfer function expressions, i_L is given by

$$i_L = \frac{e_o/R_3}{(1 + Z_L\ (R_3 || R_2)^{-1})} \tag{3.10}$$

where Z_L is the source impedance. Hence e_o, the output of amplifier A_3 is given by

$$e_o = \frac{R_5}{R_4}\left[\frac{R_F}{R_1}\, e_1 + \frac{R_F}{R_2}\, i_L\, Z_L\right] \tag{3.11}$$

Since there is negligible current required at the inverting input of the amplifier, the output current i_L is

$$i_L = \frac{(R_5\ R_F)\ e_1/(R_4\ R_1)}{R_3 + Z_L\ (1 + R_3/R_2 - (R_5/R_4)(R_F/R_2))} \tag{3.12}$$

If resistors are selected so that

$$1 + \frac{R_3}{R_2} = \frac{R_5\ R_F}{R_4\ R_2}$$

then

$$i_L = \frac{e_1}{R_3} \cdot \frac{R_5\ R_F}{R_4\ R_1}$$

In particular, if

$$R_F = R_4 = R_5 = R_1/2$$

then

$$i_L = \frac{e_1}{2\ R_3} \tag{3.13}$$

and

$$R_2 = R_F - R_3 \tag{3.14}$$

3.8.1.3 Transfer Function of the Integrator/VIC Network

Equations (3.9) and (3.13) show the transfer functions of the integrator and the V-I-C. Combining these two equations gives

$$i_L = \frac{R_I\, e_{in}}{2\, R_o\, R_3\, (1 + s\, R_I\, C_o)} \tag{3.15}$$

This current must equal the input current i_{IN} since R_o is very large.

$$\therefore Z_{IN} = \frac{e_{in}}{i_{IN}} = \frac{2\, R_o\, R_3\, (1 + s\, R_I\, C_o)}{R_I} \tag{3.16}$$

which is the transfer function of the integrator/VIC network.

The input impedance is equivalent to a series RL circuit with a resistor of value

$$R = \frac{2\, R_o\, R_3}{R_I} \tag{3.17}$$

and an inductance of value

$$L = 2\, R_o\, R_3\, C_o \tag{3.18}$$

as shown in Fig. 3.3b.

Equation (3.17) shows the minimum value of the series resistor R. Precision ±1% tolerance resistors were used for the VIC to fulfill the conditions outlined in Section 3.8.1.2. With the selected values of $R_3 = 100\Omega$ and $R_I = 10M$, $R = 2\Omega$.

3.9 Digitally Programmable Inductor

Equation (3.18) indicates that the inductor L is a direct function of R_o, R_3 and C_o. Hence to control the value of L requires varying either R_o, R_3 or C_o or any of their combinations. In the simulated inductor circuit two network elements C_o and R_o are going to be changed. C_o is changed in decades, by switching in "decade increment capacitors" using computer controlled reed relays. Digital control of R_o is achieved by using a pair of multiplying DAC's (Digital-to-Analog Converters) as a "programmable attenuator".

Figure 3.4 illustrates the functional block diagram of the digitally programmable inductor model. The current buffer is to prevent loading between the input signal and the DAC's. The DAC's, which are programmed by the computer produce an output current which is transformed to a voltage by the differential I-V converter. The integrator and the V-I-C are identical to Fig. 3.3a. The current booster is for the sole purpose of increasing the operating current range of the module.

To appreciate the operation of this model, each of the fundamental decision blocks will be separately analyzed, with special emphasis on the digital/analog section.

3.9.1 Input Buffer

To prevent undesired interactions or "loading" effects between the input signal and the DAC, (Digital-to-Analog Converter) op-amp A_1 in Fig. 3.7 is used as a voltage follower. The advantage of this follower is that it provides impedance buffering - high input impedance and low output impedance. Using the internally compensated type 3140

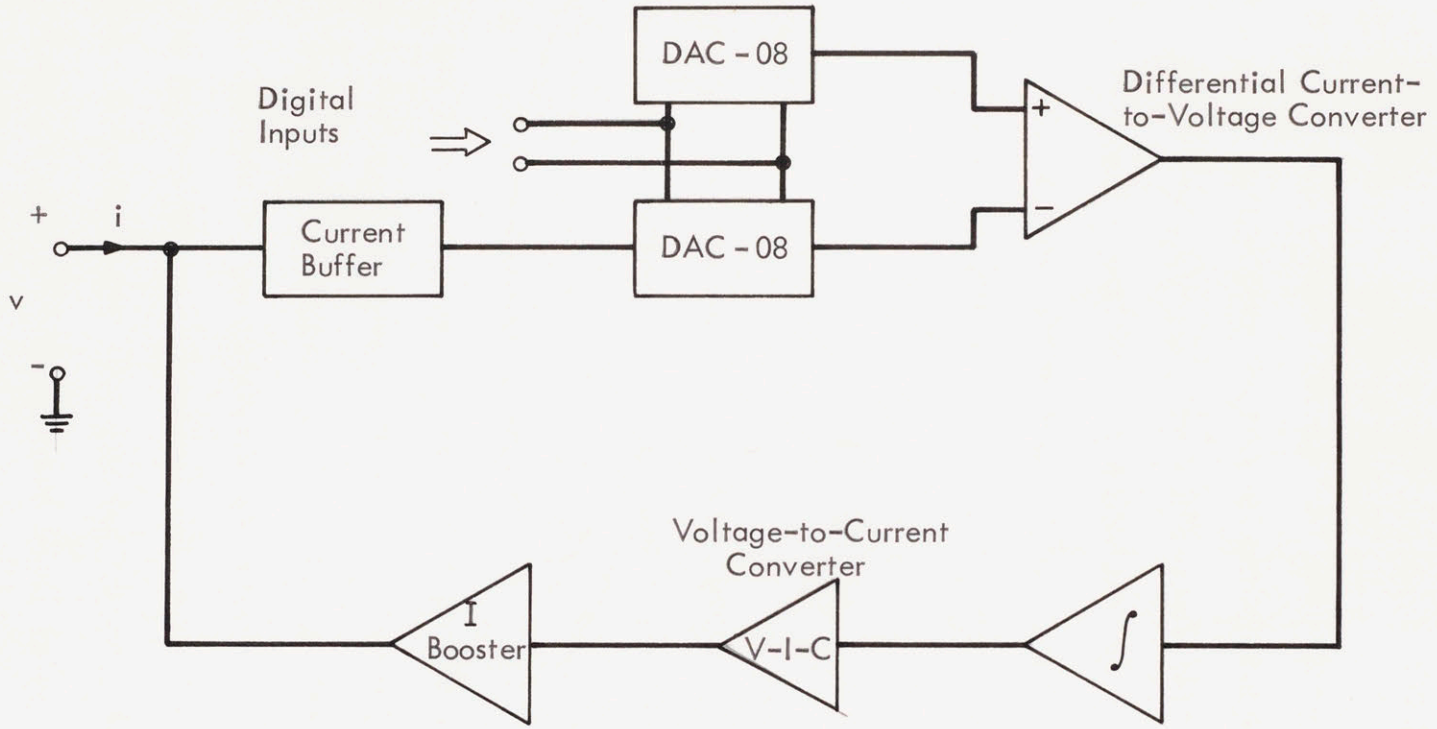


Fig. 3.4 Functional Block Diagram of the Inductor Module

op-amp, this very simple circuit serves quite effectively as an input buffer stage, providing high impedance isolation for the DAC's.

3.9.2 Digital-to-Analog Converters

To interface between the digital mini-computer and the analog inductor module, multiplying digital-to-analog converters (M-DAC's) are used. The DAC-08 is a multiplying 8 bit monolithic DAC which functions as a gain programmable amplifier and produces an output current which is a product of the input reference current I_{REF} and a digital number. The full scale output current I_{FS} is given by

$$I_{FS} = \frac{255}{256} I_{REF} \tag{3.19}$$

As seen in Fig. 3.5, the DAC-08 primarily consists of 8 fast switching current sources, a diffused R-2R resistor ladder network, a bias circuit and a reference amplifier. The diffused resistor ladder gives excellent temperature tracking and the monolithic fabrication results in excellent linearity and fast output settling. The reference amplifier provides a "turn-around" circuit or current mirror for feeding the resistor ladder network. Compensation capacitors C_1 and C_2 are for maintaining the proper phase margin in the reference amplifier.

The DAC-08 design incorporates a unique logic circuit which enables direct interface with CMOS DTL and TTL circuits. To accommodate bipolar inputs, a pair of DAC-08's are used, as shown in Fig. 3.6. Input voltage compliance is $\pm$ 10 volts, using load resistors $R_a = R_b$ of 1.5 kΩ, and $R_{IN} = 7.5$ kΩ. The output voltage e_2 is a weighted

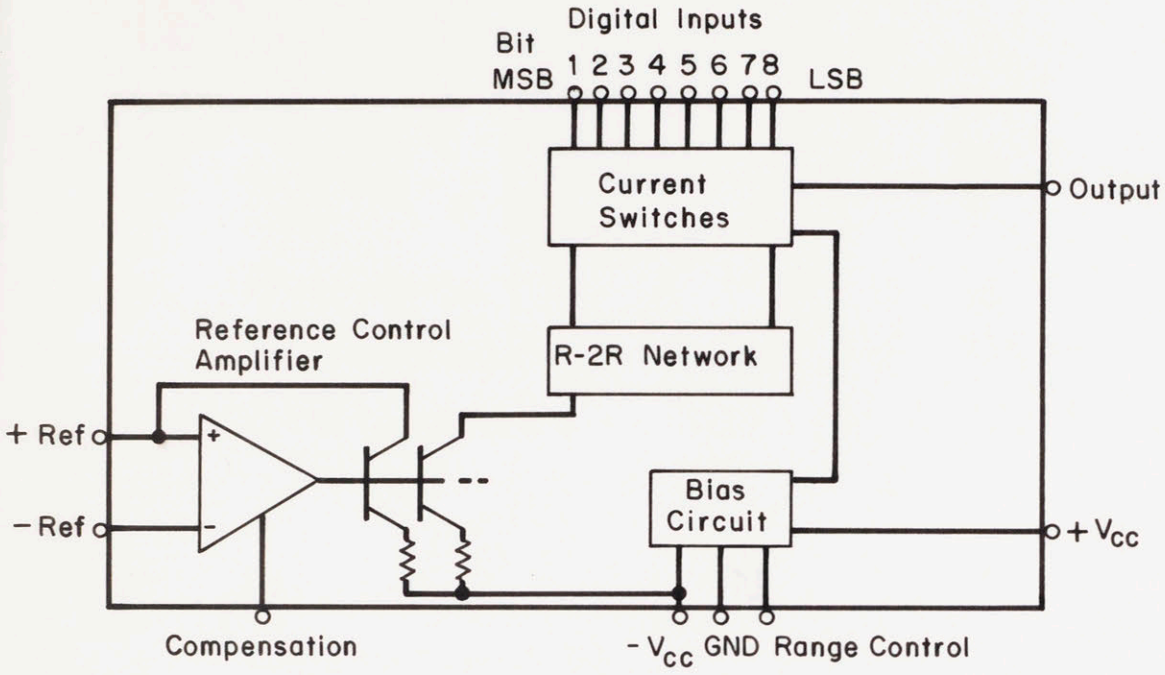


Fig. 3.5 Block Diagram of the 8-Bit Multiplying DAC

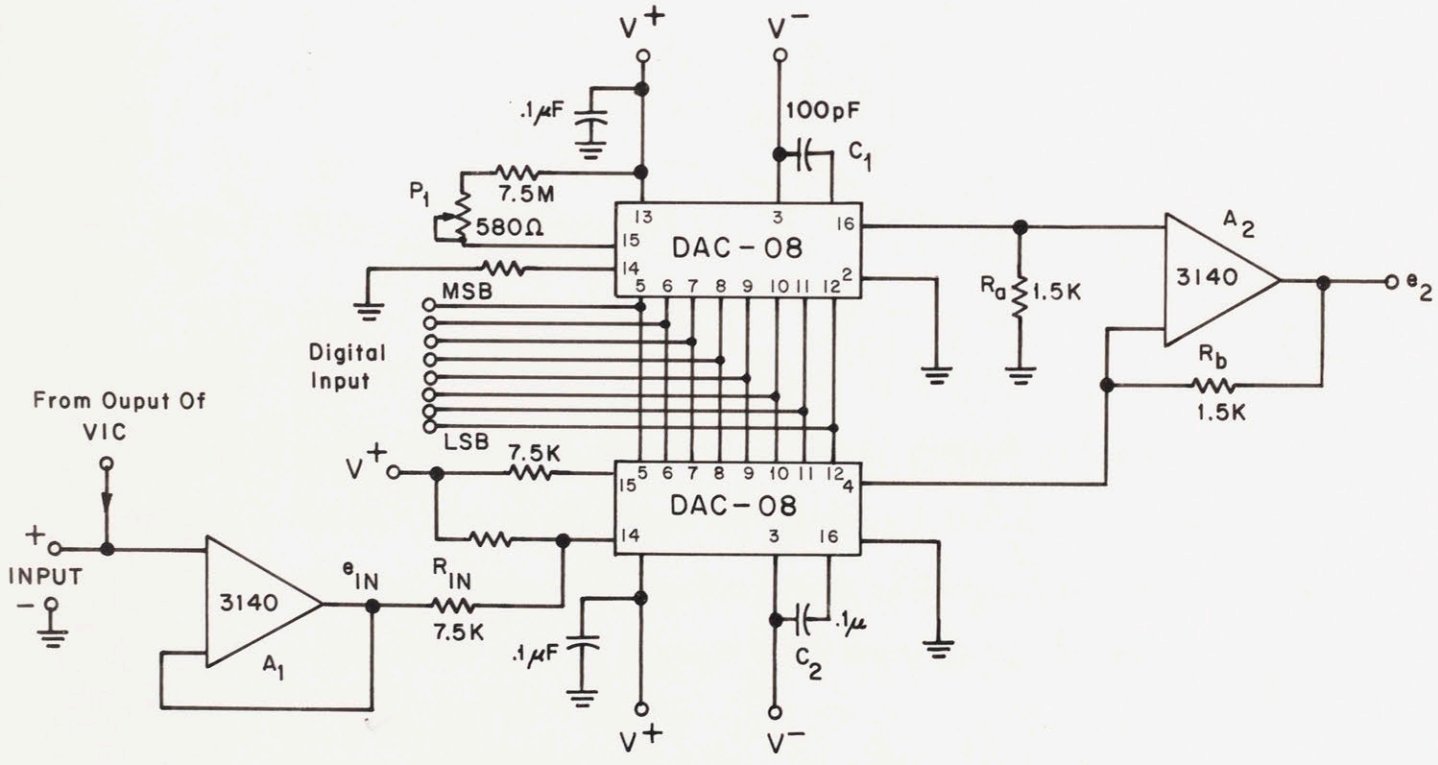


Fig. 3.6 Digital Attenuator

binary function of the input e_{in} and is given by

$$e_2 = e_{in} \frac{R_b}{R_{IN}} \left[\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256} \right] \tag{3.20}$$

where A_1 is the MSB

A_2 is the second MSB

A_3 is the third MSB

.
.
.
.

A_7 is the seventh MSB

A_8 is the LSB

If all bits (A_1 - A_8) are "high",

$$e_2 = \frac{1}{5} e_{in} \left[\frac{255}{256} \right] \tag{3.21}$$

If bits A_1 through A_7 are low, and bit A_8 "high"

$$e_2 = \frac{1}{5} e_{in} \left[\frac{1}{256} \right] \tag{3.22}$$

Combining Eqs. (3.21) and (3.22) shows that the circuit behaves as a digital attenuator with a gain that varies from 0.199 down to 0.001.

The digital attenuation factor [A] is often used to represent the digitally weighted BCD code A_1 through A_8. Hence [A] is given by

$$[A] = \left[\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256} \right] \tag{3.23}$$

Hence Eq. (3.20) can be simplified to

$$e_2 = \frac{1}{5} e_{in} [A] \tag{3.24}$$

which is the transfer function of the multiplying DAC's.

3.9.3 Analog Integrator

The analog integrator uses an op-amp (A_3) in the inverting configuration as shown in Fig. 3.7. Assuming ideal operation, the transfer function is given by

$$e_3 = - \frac{1}{R_o' C_o} \int e_2 \, dt \tag{3.25}$$

Potentiometer P_2 is used to zero the offset of the integrator, which also nulls the offset of the inductor module.

3.9.4 Voltage-to-Current Converter

The V-I-C of Fig. 3.7 uses two op-amps and a current buffer to drive a current into a grounded load. Precision high stability resistors are used for accurate voltage-to-current conversion. The V-I-C offset is eliminated by potentiometer P_3 and stability adjustment is obtained by adjustment of potentiometer P_4. The transfer function is given by

$$i_L = \frac{e_3}{2 R_3} \tag{3.26}$$

Combining Eqs. (3.24), (3.25) and (3.26) gives

$$L = \frac{10 R_o' R_3 C_o}{[A]} \tag{3.27}$$

R_o' and R_3 are selected to be 100 K and 100 Ω respectively. Substitution of these values of R_o and R_I in Eq. (3.35) results in

$$L = \frac{100\ C_o}{[A]} \tag{3.28}$$

Figure 3.7 illustrates the completed inductor model and Fig. 3.10 shows the model inductor on a printed circuit board. Prudent selection of values for C_o and [A] in Eq. (3.28) shows that the module can simulate any value of inductance lying between 0.1 and 25,600 H.

3.10 Frequency Limitations

Due to the finite open-loop gain of the op-amps, the inductor module has an upper cut-off frequency limit f_{max}, above which the input impedance no longer looks inductive. This upper frequency limit is where the closed loop gain of the integrator becomes equal to the open loop-gain of A_1. This frequency is

$$f_{max} = f_u \frac{R_o}{R_I} \tag{3.29}$$

where f_u is the unity-gain crossover frequency of A_1, which for the 3140 is 4.5 MHz. Substitution of the values of f_u, R_o and R_I in Eq. (3.29) gives the maximum frequency of operation to be 4.5 kHz. Because the multiplying DAC's have a large signal bandwidth of 2 kHz, they place a limitation on the maximum frequency of operation. However, it was decided to establish an upper frequency limit of 1 kHz for the simulator, so the inductor's bandwidth of 2 kHz was considered adequate for the purpose.

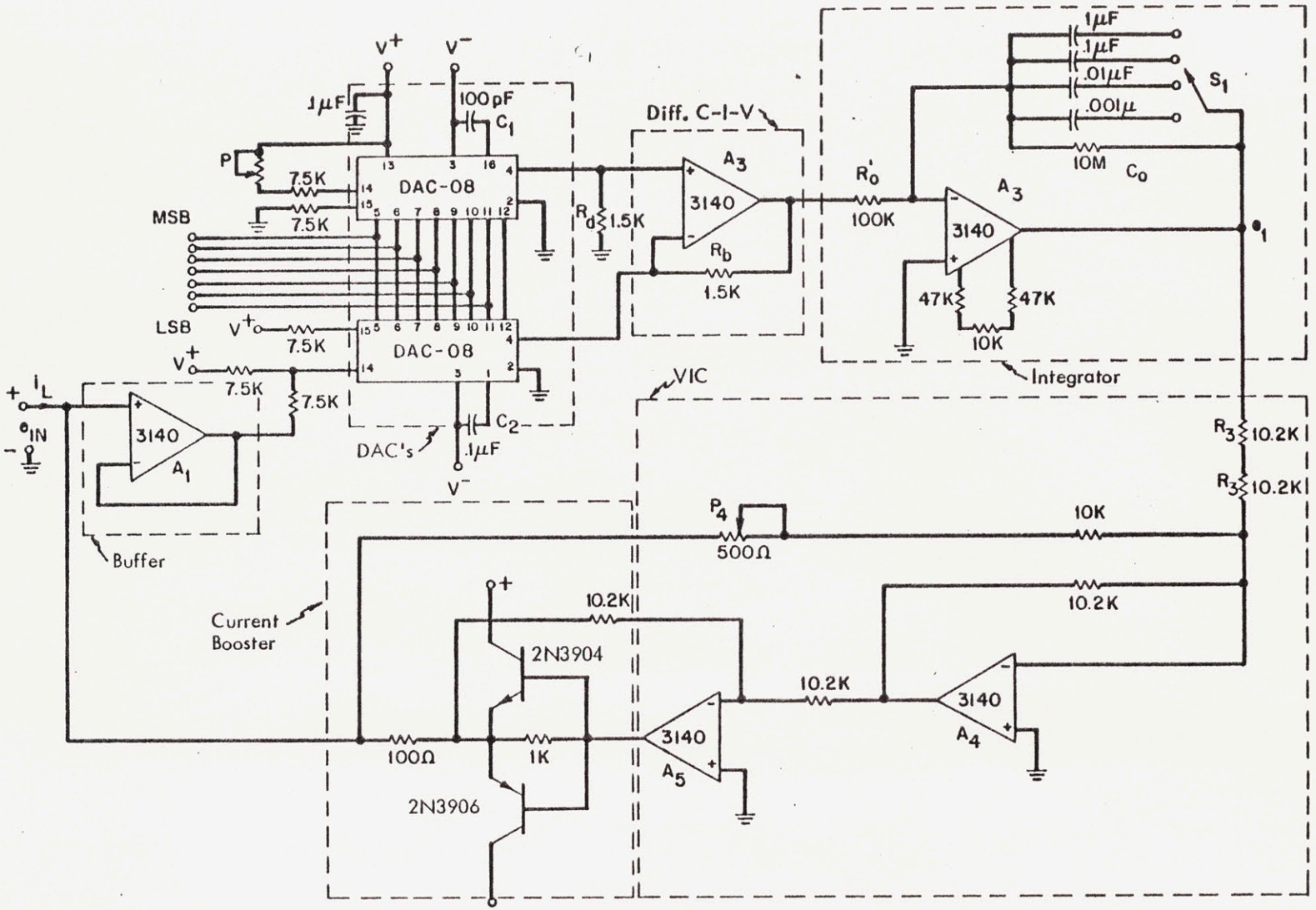


Fig. 3.7 Digitally Programmable Inductor

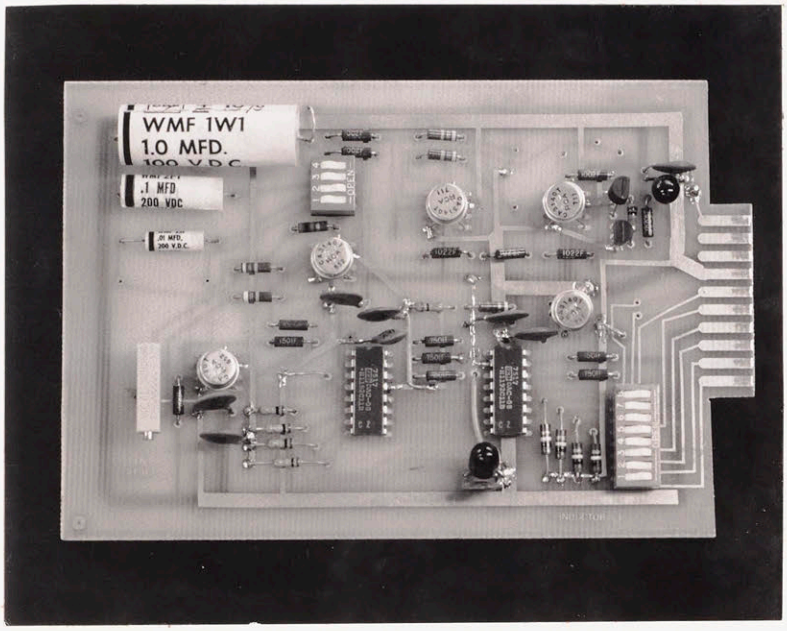


Fig. 3.8 Simulated Inductor on a PC Board

3.11 Electrical Characteristics of the Simulated Inductor

These specifications apply for $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified.

Table 3.1

Parameter	Symbol	Numerical Value
Inductance	L	$L = \frac{100\ C_o}{[A]}$ H
Maximum resolution		$\frac{1}{256}$ of maximum inductance for a particular C_o
Range of inductance values which can be simulated with .001 μ ≤ C_o ≤ 1 μF	L_{max} (C_o = 1 μF)	25,600 H
	L_{min} (C_o = .001 μF)	0.1 H
Quality factor for 10 Henry inductor at 10 Hz	Q	63
Terminal voltage range	V_{oc}	± 10 V
Terminal current range	I_L	± 120 mA
Maximum operating frequency	f_u	1 kHz

3.12 Experimental Results

With the described inductor model, the significant electrical parameters were accurately determined and recorded. Among the measured quantities are:

1. Step response of a simulated L-R circuit
2. Variation of impedance with frequency

These quantities were measured for various inductor values and various operating frequencies.

3.12.1 Step Response of a Simulated RL Circuit

Linear networks containing a single energy storage element (either an inductor or a capacitor) along with a combination of sources and dissipators (resistors) are called single time-constant networks, since the natural response always has an $e^{-t/\tau}$ behavior.

Figure 3.9a shows a general L-R circuit in series with a step source V_S. Applying continuity conditions, the current and voltage parameters can be expressed as

$$i_L = I_{-1}(t) \frac{V_S}{R} (1 - e^{-t/\tau}) \tag{3.30}$$

and

$$v_L = U_{-1}(t) V_S e^{-t/\tau} \tag{3.31}$$

Figure 3.9b and 3.9c show the time-dependance of i_L and v_L for the simulated inductor.

Figure 3.9d illustrates the current in the L/R network for two different time constants. From the figure, i_{L_1} is found to be

$$i_{L_1} = .0032 (1 - e^{-t/\tau_1})$$

where $\tau_1 = .001$

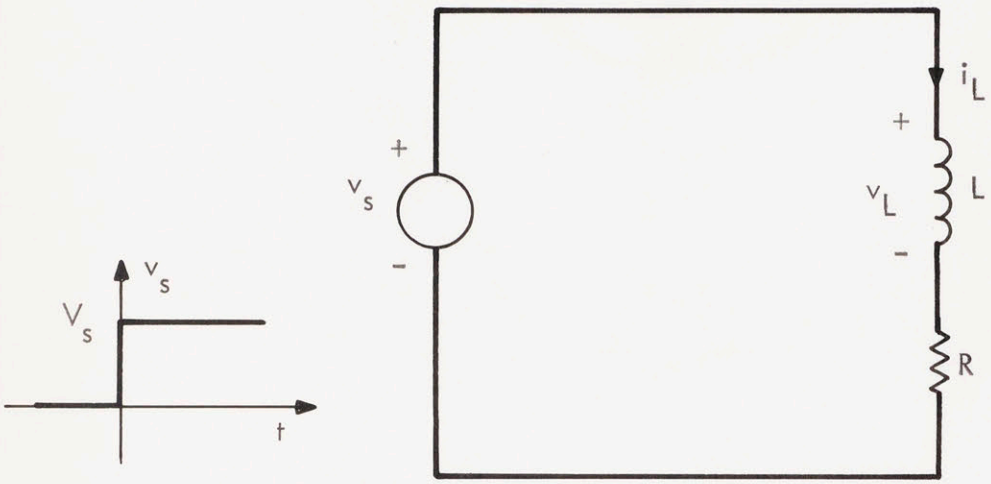


Fig. 3.9(a) LR Network with a Step Source

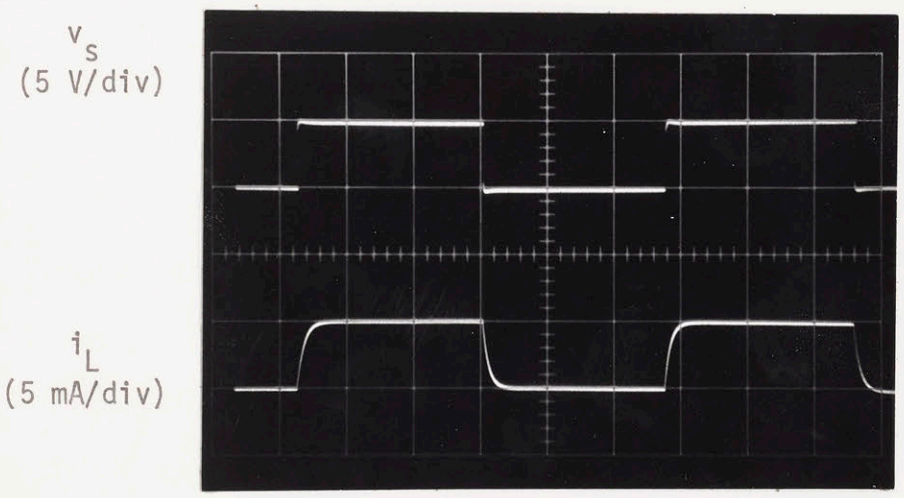


Fig. 3.9(b) Time Dependence of i_L for Simulated Inductor

and

$$i_{L_{2\ max}} = \frac{V}{R_2} \frac{1 - e^{-t/\tau_2}}{1 - e^{-2t/\tau_2}}$$

Also from Fig. 3.9d

$$i_{L_{2\ max}} = .002 = .0032 \frac{1 - e^{-\frac{5.5 \times 10^{-3}}{\tau_2}}}{1 - e^{-2 \cdot \frac{5.5 \times 10^{-3}}{\tau_2}}}$$

giving τ_2 = 10.1 msec.

As the calculated value of τ_2 = 10/1K = 10 msec, this agrees well with the experimental result.

Figure 3.9e shows a "blown-up" view of the inductor voltage and from the same figure

$$v_{L\ (0)} = 4 \text{ volts}$$

and

$$e^{-1} \cdot v_{L\ (0)} = 1.47 \text{ volts}$$

Hence one time constant has elapsed when the voltage has dropped to 1.47 volts. This occurs at 1.8 msec which is the time constant obtained experimentally. Calculations indicate a time constant of 1.79 msec, which agrees well with the experimental data.

3.12.2 Variation of Impedance with Frequency

The simulated inductor has a high frequency limitation, above which the impedance ceases to be reactive; this occurs when the closed loop gain of the integrator equals the open loop gain of the integrator

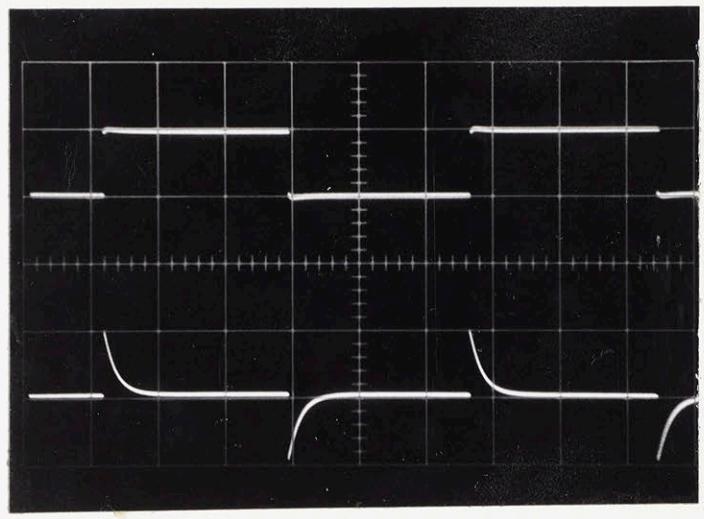


Fig. 3.9(c) Time Dependence of v_L for the Simulated Inductor

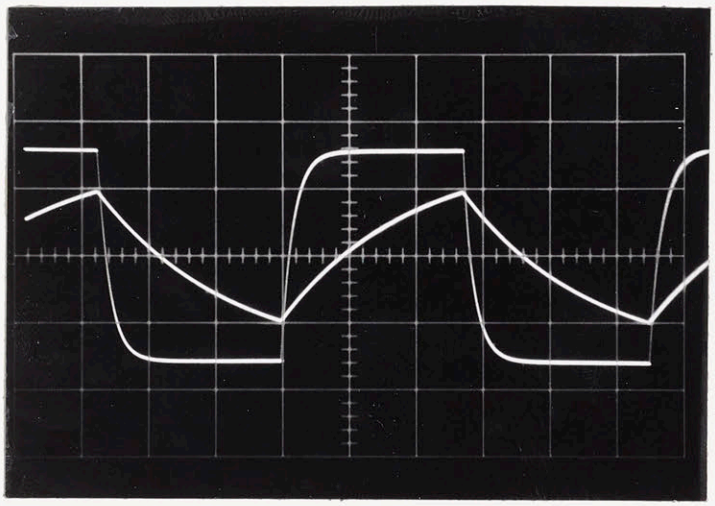


Fig. 3.9(d) Double Exposure Showing Inductor Current for Two Different Time-Constants

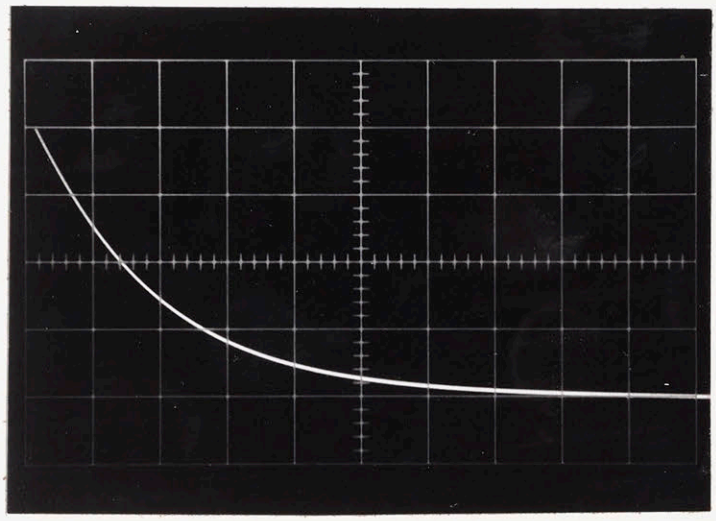


Fig. 3.9(e) Exponential Decay of the Inductor Voltage

op-amp. To find the module's bandwidth, the impedance of the simulated inductor was plotted as a function of frequency. Figure 3.10 illustrates the graphical data presentation of the variation of impedance as a function of input frequency. Clearly the impedance is inductive up to 1 kHz which is the required bandwidth of the Parity Simulator.

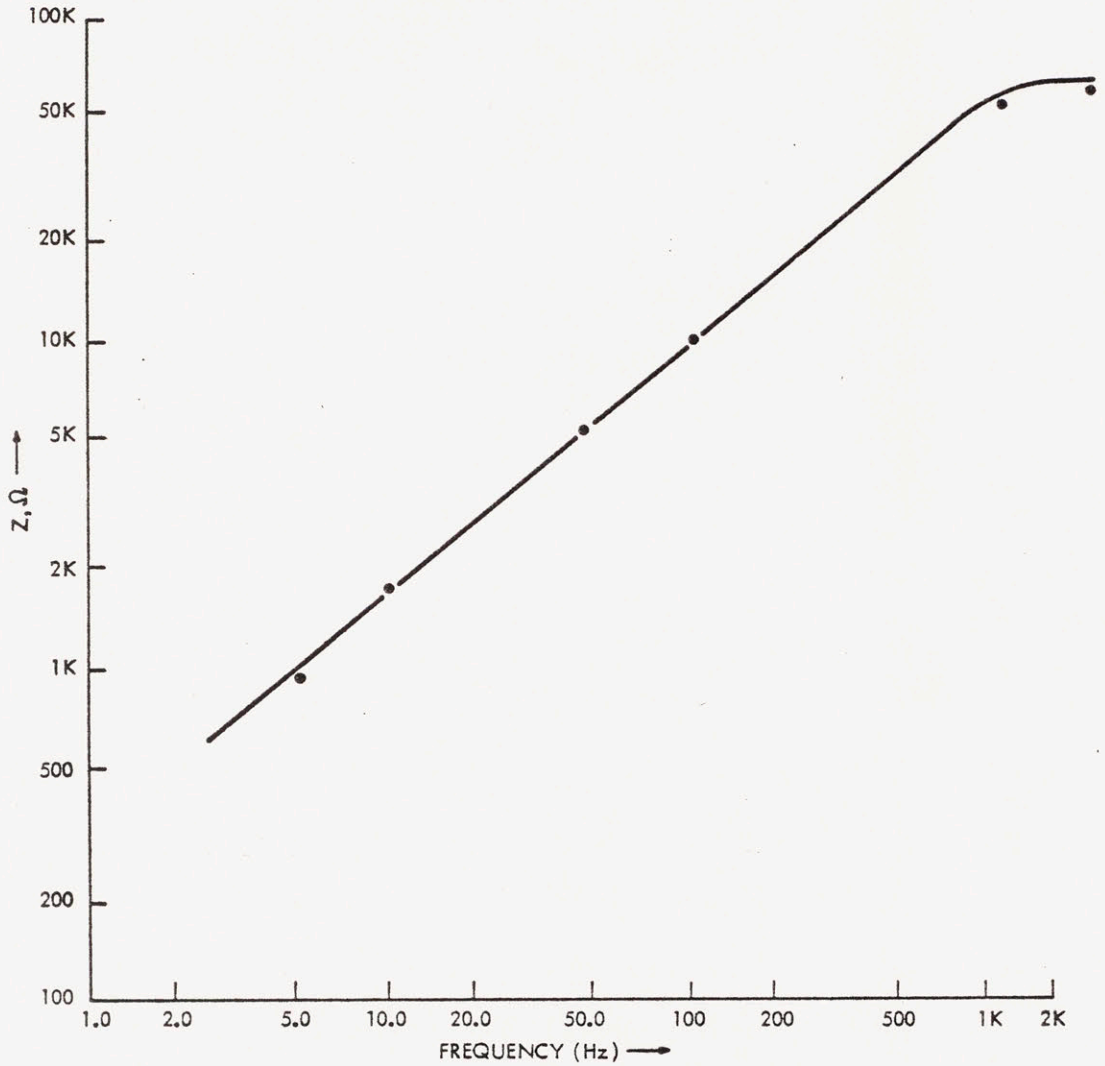


Fig. 3.10 Impedance of the Simulated Inductor as a Function of Frequency

CHAPTER 4

CAPACITANCE SIMULATOR

The capacitor is a two-terminal circuit element in which the current flowing through the element is proportional to the time rate of change of the terminal voltage across it.

4.1 Ideal Capacitor

For the ideal capacitor constructed from linear dielectric material, the terminal relations in terms of capacitance C are

$$v_c = \frac{1}{C}\int_0^t i_c\,dt + v_c(0)\ ;\ i_c = C\frac{dv_c}{dt} \qquad (4.1)$$

The ideal capacitor is a lossless element and is capable of energy storage. This energy is stored in the electric field and consequently is termed electric stored energy.

In practice, the ideal volt-ampere relationship of a capacitor can only be approximated. However, as compared to an inductor, a capacitor can be much more accurately approximated over a fairly wide range of frequencies by either a pure capacitance, or a capacitance in parallel with a large resistance corresponding to the leakage resistance of the dielectric.

4.2 Loss Mechanisms in Capacitors

In an ideal capacitor the dielectric material separating the conducting plates is a perfect insulator. That is, there is no energy dissipated in the dielectric as a result of an applied electric field.

Actual dielectrics never realise this ideal perfectly, but rather, dissipate some of the energy delivered to them. Moreover, at very high frequencies, skin effect causes an appreciable loss to occur in the capacitor leads and electrodes. At very high voltages corona may occur and contribute to the loss.

The merit of a capacitor from the point of view of freedom from losses is usually expressed in terms of the phase angle of the capacitor. The tangent of the phase angle is termed the dissipation factor D. With ordinary dielectrics, the dissipation D is so small, that for all practical purposes, it is equal to the phase angle expressed in radians. The dissipation can also be defined as the ratio of the conductance G(w) to capacitive impedance B(w), or

$$D = \frac{G(w)}{B(w)} \tag{4.2}$$

Although the dissipation of a capacitor is determined largely by the type of dielectric used in the capacitor, it is also affected by the conditions under which the dielectric operates. Consequently, the frequency characteristics of an actual capacitor is rather complex and represents a variety of phenomena which affect the value of capacitance and D over a wide frequency range.

4.3 Equivalent Circuit of a Lossy Capacitor

One possible circuit model which can represent the dissipation in an actual capacitor is shown in Fig. 4.1. This circuit model represents a variety of phenomena which affect the value of capacitance and

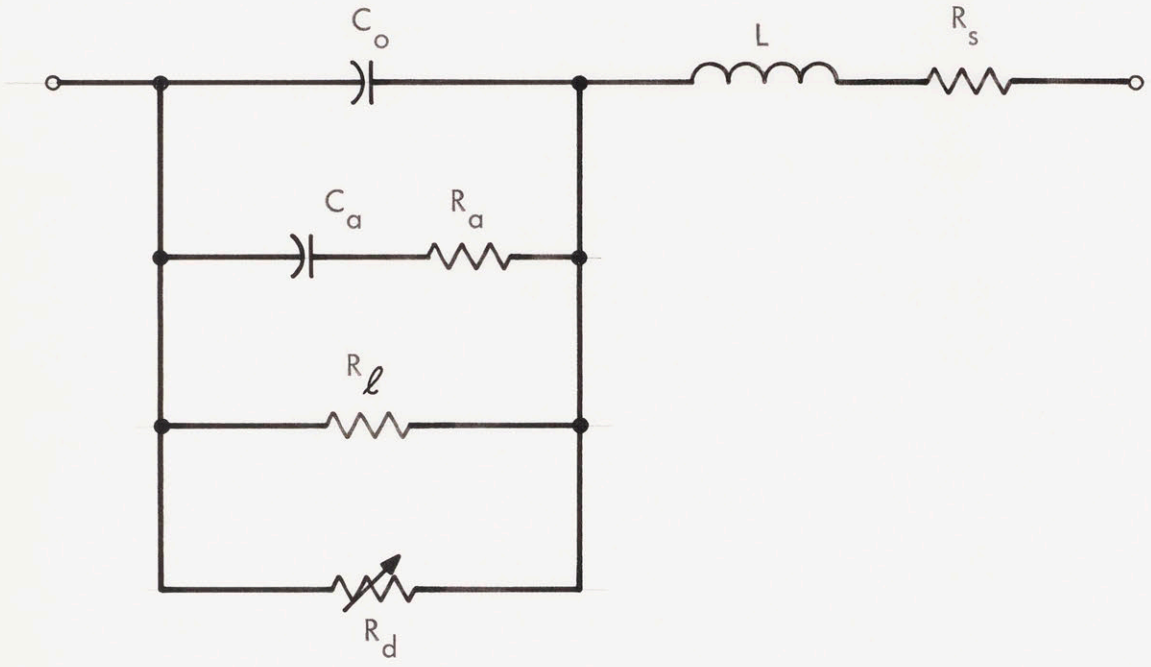


Fig. 4.1 An Equivalent Circuit of a Lossy Capacitor

the dissipation factor over a wide frequency range.

The electrostatic, or dc value of capacitance is C_o plus the relatively small capacitance C_a, which represents the increase in effective dc capacitance over its audio-frequency value resulting from interfacial polarization. This effect can be considered to be a gradual redistribution of charge through the dielectric. This effect causes dielectric absorption, characterized by the additional charging current flowing long after an ideal capacitor would have been charged, and the gradual recovery of the voltage after the capacitor has been momentarily discharged. The $R_a C_a$ time constant is due to the dielectric absorption property. At high frequencies, the series inductance L and resistance R_s change the effective value of the capacitance, especially as series resonance is approached.

There are several causes of energy loss in capacitors. At dc all capacitors have a finite leakage resistance known as the insulation resistance R_ℓ. At high frequencies the major part of the dissipation is in the dielectric itself and is caused by polarization effects in the dielectric material. As a result of non-homogeneity in the dielectric structure and in the applied electric field, this effect is varying and consequently is represented by the variable resistor R_d.

4.4 Capacitance Simulation

In Parity Simulation, the actual capacitance is replaced by a two terminal device in which the current flowing through the element is proportional to the time rate of change of the terminal voltage. In other words, this two terminal device behaves as a capacitor and has a

precisely controlled driving point impedance.

Two different schemes of simulating capacitors using op-amps were considered. Both circuits provide simulated capacitive reactances, which are relatively frequency independent and can be varied over a large range of values.

4.5 Capacitance Simulator by Impedance Multiplier

It is possible to simulate capacitive reactance using a capacitor in the feedback loop of an impedance multiplier. The variable capacitance multiplier is shown in Fig. 4.2, where the high gain of op-amp A_2 is used to multiply capacitance. The circuit equations are:

$$i_{1N} = \frac{e_{1N} - e_2}{1/sC_1} \tag{4.3}$$

$$e_2 = \frac{R_b}{R_a} e_{1N} \tag{4.4}$$

Combining Eqs. (4.3) and (4.4) and solving for the transfer relationship e_{1N}/i_{1N} gives

$$Z_{1N} = \frac{e_{1N}}{i_{1N}} = \frac{1}{s\, C_1(1 + \frac{R_b}{R_a})} \tag{4.5}$$

Equation (4.5) shows that the effective capacitance seen between point Z_{1N} and ground in Fig. 4.2 is

$$C_{1N} = C_1 (1 + \frac{R_b}{R_a}) \tag{4.6}$$

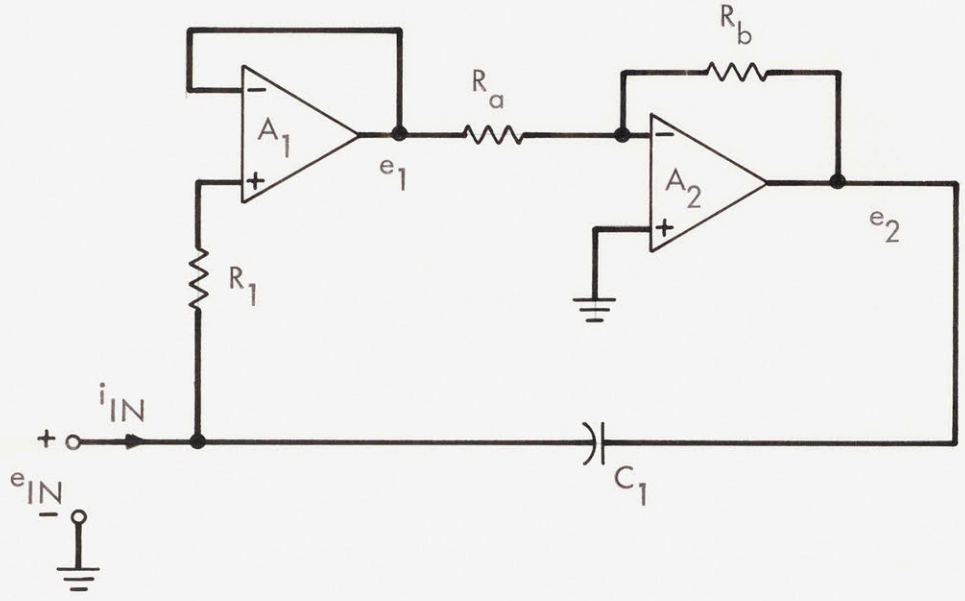


Fig. 4.2 Capacitance Simulator by Impedance Multiplier

Hence this circuit can be effectively used as a capacitance simulator. However, this circuit has a fundamental drawback - the maximum input voltage swing is reduced from the supply voltage V_{cc} , to $V_{cc}/1 + \frac{R_b}{R_a}$ where $\frac{R_b}{R_a}$ is the absolute value of the closed loop transfer function of A_2.

Hence another circuit is presented which simulates a variable capacitor and yet does not have the above-mentioned input voltage limitations.

4.6 Capacitance Simulator using an Integrator

Equation (4.1) states that the capacitor voltage is given by the integral of the current through the device. Hence a current-to-voltage transformation circuit in series with an integrator can be effectively used to model a capacitor. The transformation is implemented using a current-to-voltage converter and a differential amplifier, and this network together with the integrator forms the capacitance simulator.

The chosen circuit is illustrated in Fig. 4.3(a). Amplifier A_1 is a current-to-voltage converter; A_2 is a differential amplifier giving an output V_3 which is the difference between V_2 and V_5 scaled by their corresponding resistor values, as will be shown later (Eq. (4.21)). A_D represents a gain stage obtained from the multiplying DAC's (Digital-to-Analog Converters) which are used as gain programmable amplifiers, allowing the operator to change the capacitor values in 0.5% increments. The output of A_D (V_4) is integrated and fed back to close the loop. V_D represents a noise voltage fed in by the DAC's, which has a significant effect on loop stability especially when resistor values are matched.

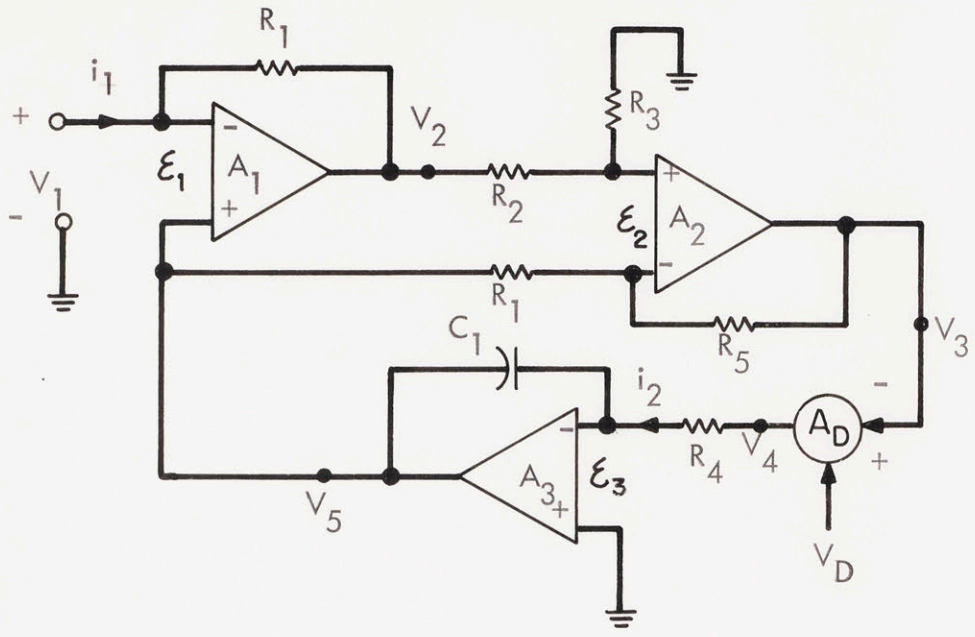


Fig. 4.3(a) Simulated Capacitor Circuit

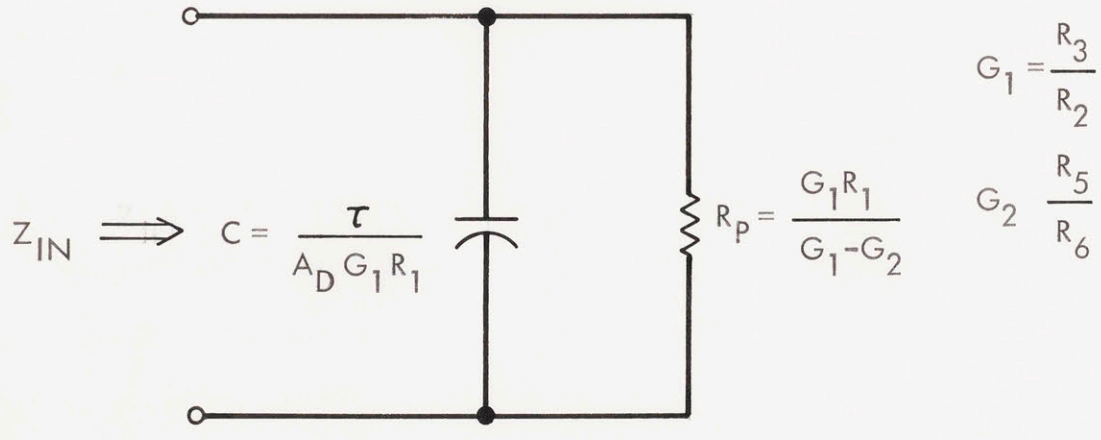


Fig. 4.3(b) Equivalent Circuit of the Simulated Capacitor

This aspect of stability is discussed at length in the succeeding sections.

4.6.1 Explanation of Operation

In order to illustrate the operation of the capacitor circuit it is necessary to find its closed loop transfer function. This may be obtained in the following manner:

4.6.1.1 Transfer Characteristic Equations

An analysis for the circuit of Fig. 4.3(a) yields the following equations:

$$V_2 = V_1 - i_1 R \tag{4.7}$$

$$V_4 = V_3 A_D + V_D \tag{4.8}$$

$$V_5 = V_1 = \varepsilon_1 \tag{4.9}$$

$$V_3 = G_1 V_1 - G_2 V_5 + \varepsilon_2 (1 + G_1) \tag{4.10}$$

$$V_5 = -\frac{V_4}{\tau s} + \varepsilon_3 \left(1 + \frac{1}{\tau s}\right) \tag{4.11}$$

where G_1 and G_2 are the ratio of resistors R_3 to R_2 and R_5 to R_6, respectively, ε_n the offset of amplifier n, and τ, the integrator time constant given by $R_4 C_1$. Combining these equations gives the resulting equation for input voltage,

$$V_1 = \frac{(\varepsilon_3 - \varepsilon_1)\,\tau s + [\varepsilon_3 - V_D + A_D G_2 \varepsilon_1 - A_D(\varepsilon_2 + G_1)] + A_D G_1 R_1 i_1}{[\tau s + A_D(G_1 - G_2)]} \tag{4.12}$$

If $V_D = 0$ and the op-amp offsets are negligible, then

$$V_D = \varepsilon_1 = \varepsilon_2 = \varepsilon_3 = 0 \tag{4.13}$$

and the circuit yields the following equations to describe its operation:

$$V_1 = \frac{i_1}{\frac{\tau s}{A_D G_1 R_1} + \frac{(G_1 - G_2)}{R_1 G_1}} \tag{4.14}$$

Equation (4.14) implies a network having a capacitor of value C in parallel with a resistor R_p, as shown in Fig. 4.3(b). The effective capacitance C and the parallel resistance R_p are given by

$$C = \frac{\tau}{A_D G_1 R_1} \tag{4.15}$$

$$R_p = \frac{G_1 R_1}{G_1 - G_2} \tag{4.16}$$

Equation (4.15) states that to model an ideal capacitor, the series resistance R_p should be infinite. This clearly implies that

$$G_1 - G_2 = 0 \tag{4.17}$$

which results in

$$\frac{R_3}{R_2} = \frac{R_6}{R_5} \tag{4.18}$$

In addition, when the capacitor terminals are open-circuited the following two conditions must be fulfilled.

$$i_1 = 0$$

$$s = 0$$

The resulting output voltage is given by

$$V_1 = \frac{\varepsilon_3 - V_D + A_D [G_1 - (\varepsilon_1 - 1) - \varepsilon_2]}{A_D(G_1 - G_2)} \qquad (4.19)$$

Clearly as G_1 tends to G_2, the term in the denominator $A_D(G_1 - G_2)$ tends to zero, and therefore the slightest noise will saturate the op-amps. This is so even if all offsets are made zero, as can be seen from Eq. (4.19). Thus a compromise has to be effected between the magnitude of the parallel resistor R_p (Eq. (4.16)) and stability (Eq. (4.19)). At first glance this may imply a major defect in the circuit, however, judicious selection of R_2, R_3, R_5 and R_6 can give a relatively large R_p. In the capacitor model, the values of R_2, R_3, R_5 and R_6 were matched to 0.01%, making R_p = 1 MΩ which provided the necessary resistance without affecting loop stability. Values much greater than 1 MΩ cause unstability and are not recommended.

4.7 Digitally Programmable Capacitor

As discussed earlier, the simulated capacitor C is a direct function of the integrator time constant τ, and an inverse function of A_D, G_1 and R_1. To control the value of C requires varying some

combination of the above parameters. In the capacitor module, two network parameters are going to be changed - the digital gain of the DAC's (A_D) and the integrator time constant τ. A_D is changed by using a pair of multiplying DAC's as a programmable attenuator. The time constant of the integrator τ is changed by varying C_1 in decades by switching in decade increment capacitors using computer controlled reed-relays.

Figure 4.4 illustrates the functional block diagram of the digitally programmable capacitor model. The current-to-voltage converter presents almost zero load impedance to ground and provides an output voltage proportional to the input current. The purpose of the current booster is to increase the operating current range of the module. The differential amplifier and the integrator are identical to Fig. 4.3(a). The DAC's which are programmed by the computer produce an output current which is transformed to a voltage by the differential current-to-voltage converter.

To appreciate the operation of this module, each of the fundamental decision blocks are discussed in the sections which follow.

4.7.1 Current-to-Voltage Converters

The analog integrator is basically a voltage operated device. Hence a current-to-voltage converter (also called transimpedance amplifier) is used to convert the capacitor current to an output voltage. The transimpedance amplifier provides an output voltage which is proportional to input current. The proportionality constant is the feedback resistor R_F such that $v_2 = - i_F R_F$. This circuit is characterized by zero input resistance and zero output resistance if the op-amp

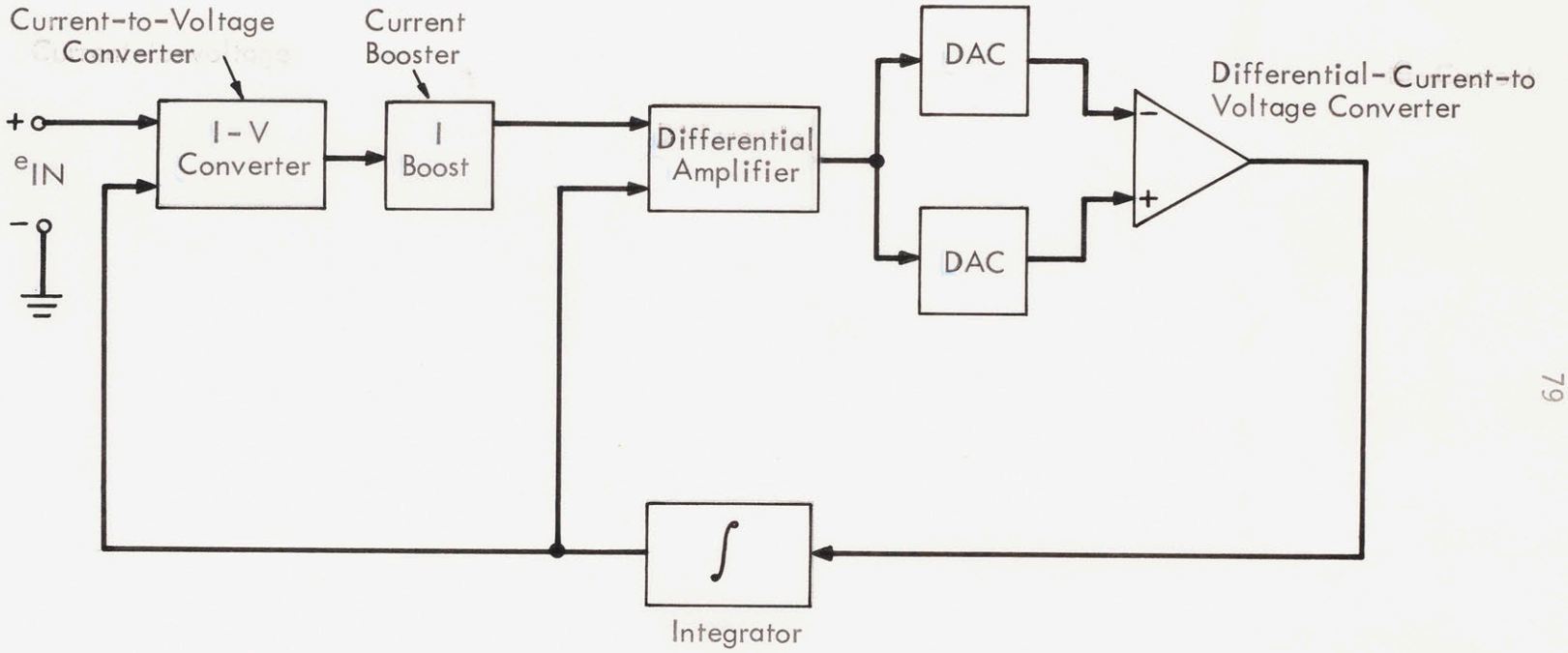


Fig. 4.4 Functional Block Diagram of the Capacitor Module

is ideal. Only one resistor (R_F) is required for the operation of this circuit. Input protection resistor R_p limits the input current during a step change in the incoming signal. This protection resistor prevents the possibility of extremely large input signal transients from forcing a signal through the op-amp input protection network and thus adversely affecting the operation of the converter.

The actual input impedance of the current-to-voltage converter assuming a finite open-loop voltage gain A, is given by

$$Z_{in} = \frac{R_F}{1 + A} \tag{4.20}$$

With R_F = 100Ω and A = 4500 at the maximum operating frequency of 1 kHz, Z_{in} = 0.022Ω, which is small compared to the typical resistor values used in the simulation (100Ω - 100 kΩ). Figure 4.5 illustrates the current-to-voltage converter with the current booster in its feedback loop.

4.7.2 Current Booster

Most op-amps are low-level devices with optimized input characteristics. To increase the power level, it is sometimes advisable to combine an op-amp having excellent input characteristics with a high power output circuit. This additional circuit can be tailored to have a maximum output current capability beyond the capability of the op-amp.

The simplest way to boost output current is to add an output emitter follower. To efficiently increase both polarities of current, a complimentary emitter stage is required. Class B biasing is used in the the current booster, with cross-over distortion being minimized by

enclosing the booster in the amplifier feedback loop so that the cross-over distortion is divided by the open-loop gain of the op-amp. Figure 4.5 shows the current booster within the feedback loop of the current-to-voltage converter. The maximum output current in the circuit is 150 mA, using the 2N3904-2N3906 complimentary transistor pair. The 100Ω precision resistor (R_F) provides the necessary feedback path for the input current.

4.7.3 Differential Amplifier

Differential DC amplifiers are circuits that amplify the difference between two signals and whose inputs are direct-coupled. They are easily realized through the use of one operational amplifier with linear feedback. The circuit of Fig. 4.6 functions as a difference circuit, using only one operational amplifier and four matched resistors, R_1, R_2, R_3 and R_4. If the resistors are perfectly matched, (i.e., $R_1 = R_2 = R_3 = R_4$), then the output is given by

$$v_3 = (v_2 - v_5) \tag{4.21}$$

Careful matching of resistors is essential to ensure high common mode rejection ratio. Potentiometer P_1 is used to achieve resistor matching to within 0.05%. Input offset voltages cause dc errors which are amplified by the factor $(R_3 + R_4)/R_3$. Potentiometer P_3 is used to nullify these errors at the output of the differential amplifier circuit.

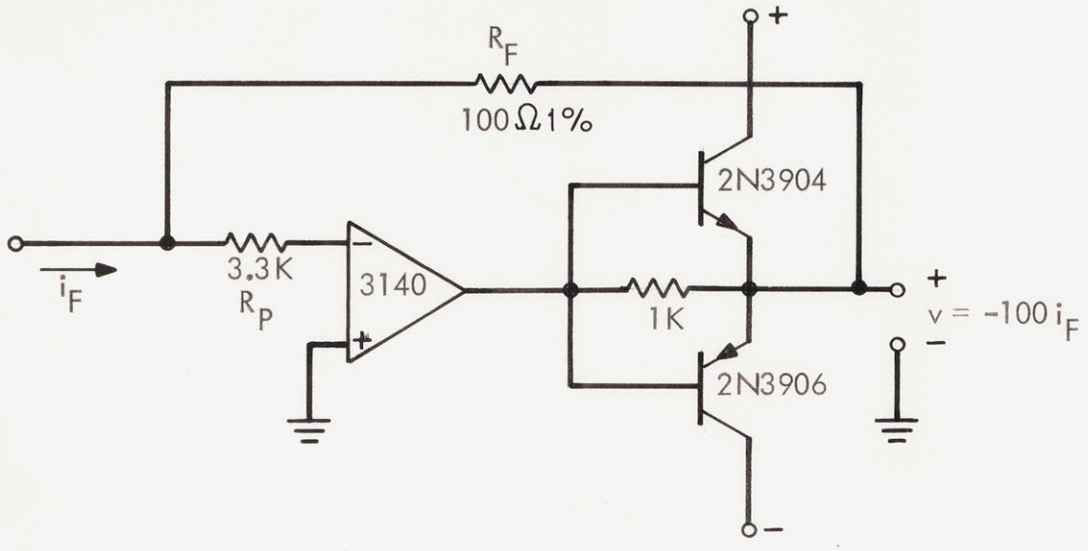


Fig. 4.5(a) Current-to-Voltage Converter

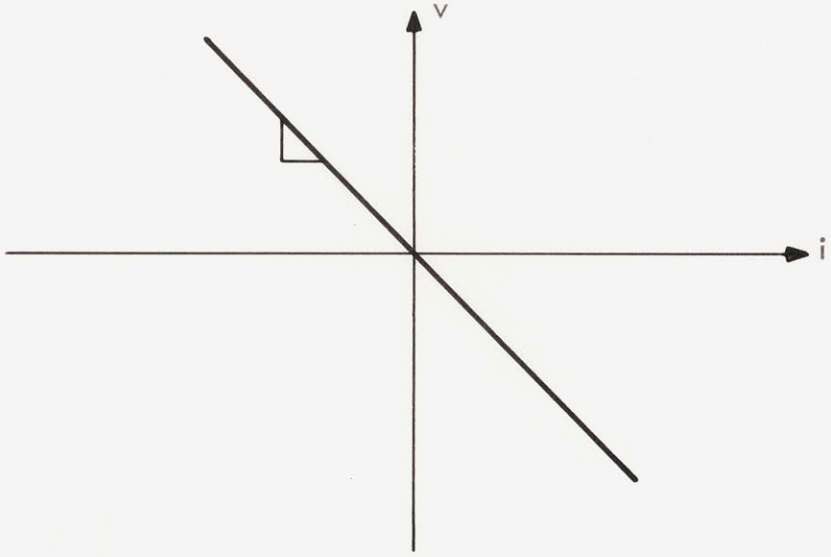


Fig. 4.5(b) Transfer Function of the Current-to-Voltage Converter

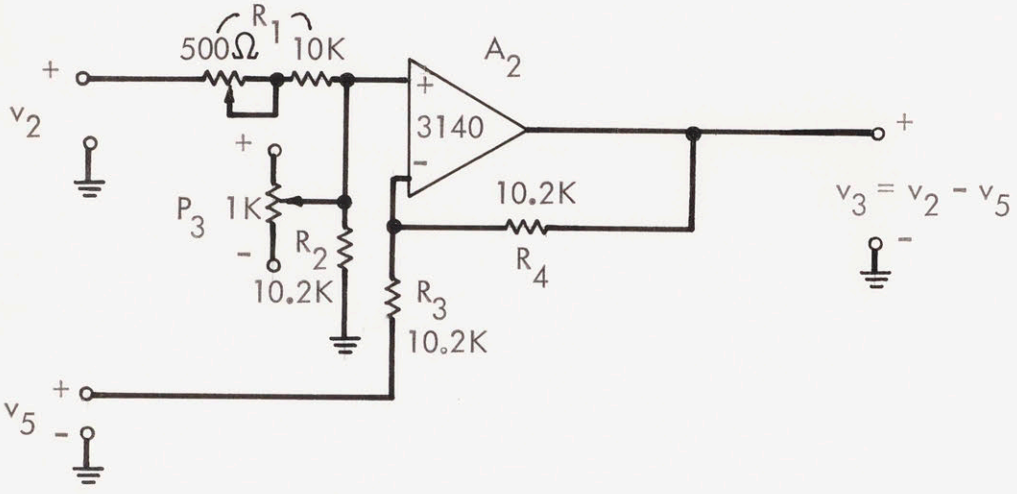


Fig. 4.6 Differential Amplifier

4.7.4 Digital-to-Analog Converters (DAC's)

The DAC's have basically the same network connections in the capacitor as in the inductor (Section 3.9.2). The transfer function of the DAC's is

$$v_4 = \frac{v_3}{[A]} \tag{4.22}$$

4.7.5 Analog Integrator

The output of the DAC's (v_4) is integrated by the analog integrator whose transfer function is given by

$$v_5 = - \frac{1}{R_4 C_1} \int v_4 \, dt \tag{4.23}$$

Potentiometer P_4 is used to zero the integrator offset, which also nulls the offset of the capacitor module.

Combining the individual transfer functions of the various decision blocks discussed, the overall transfer function of Fig. 4.8 is obtained. From the transfer function, the effective capacitance C and resistance R_p are found to be

$$C = \frac{1000 \, C_1}{[A]} \tag{4.24}$$

$$R_p = \frac{G_1 \, R_1}{G_1 - G_2} \tag{4.25}$$

where C_1 is the integrator capacitor.

Figure 4.7 illustrates the completed capacitor model and Fig. 4.8 shows the model capacitor on a printed circuit board. Prudent selection of the values of C_1 and [A] shows that the module can simulate any value of capacitance lying between 1-100,000 μF.

4.8 Frequency Limitations

The finite bandwidth of the multiplying DAC's sets an upper limit on the maximum operating frequency of the capacitor module. Above this frequency, the input impedance of the capacitor no longer looks capacitive. This is because the transfer function of the DAC's departs from the ideal transfer function at the upper frequency limit which is about 2 kHz. Since the upper frequency limit established for the Parity Simulator is set at 1 kHz, the simulated capacitor's bandwidth of twice this value was considered adequate for the purpose.

4.9 Electrical Characteristics of the Simulated Capacitor

These specifications apply for $V_s = \pm 15$ V, $T_A = 25°C$ unless otherwise specified.

4.10 Experimental Results

With the described capacitor model, the significant electrical parameters were accurately determined and recorded. Among the measured quantities are:

1) Step response of a simulated R-C circuit.
2) Self-discharge measurement.
3) Variation of impedance with frequency.

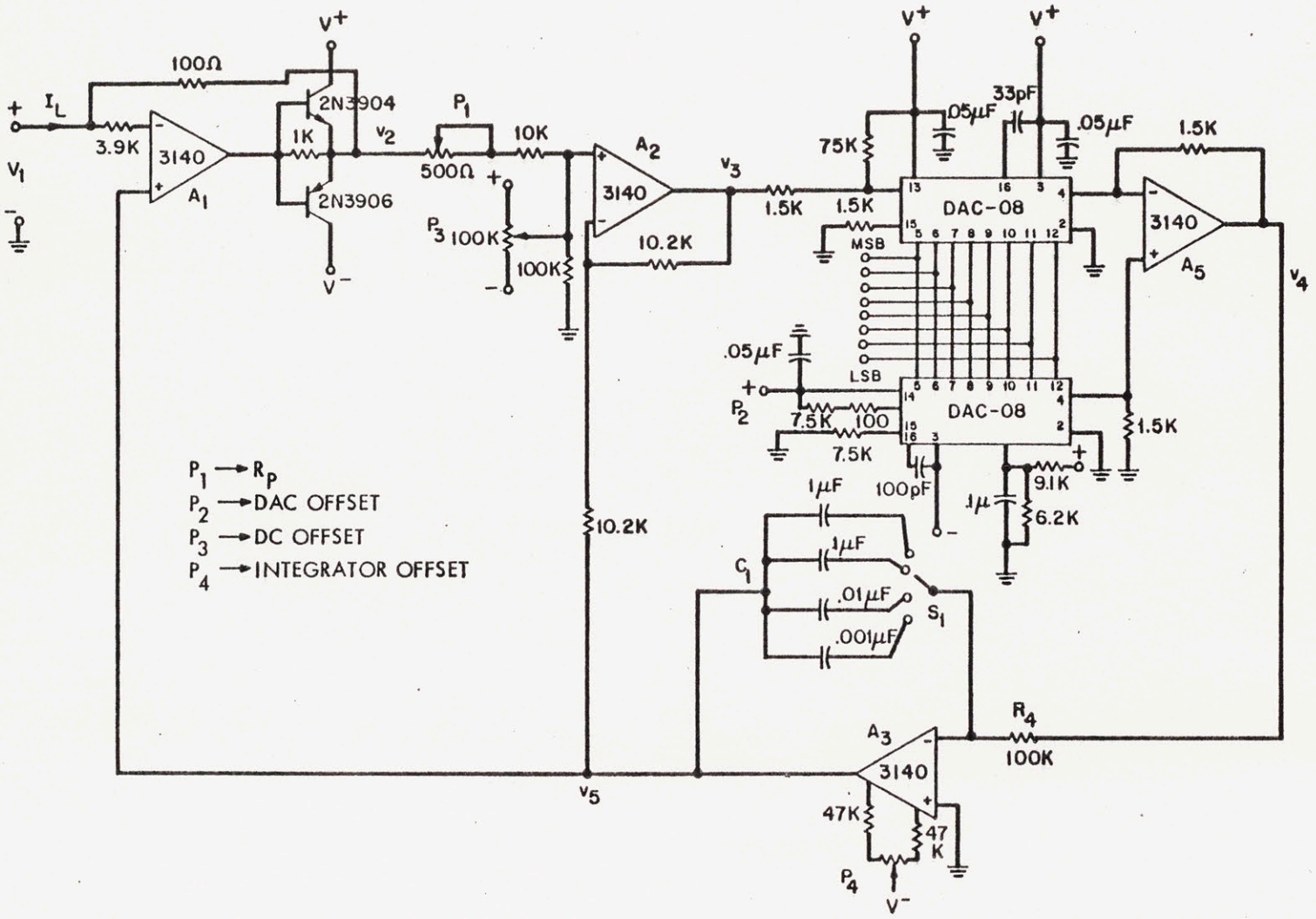


Fig. 4.7 Simulated Capacitor Circuit

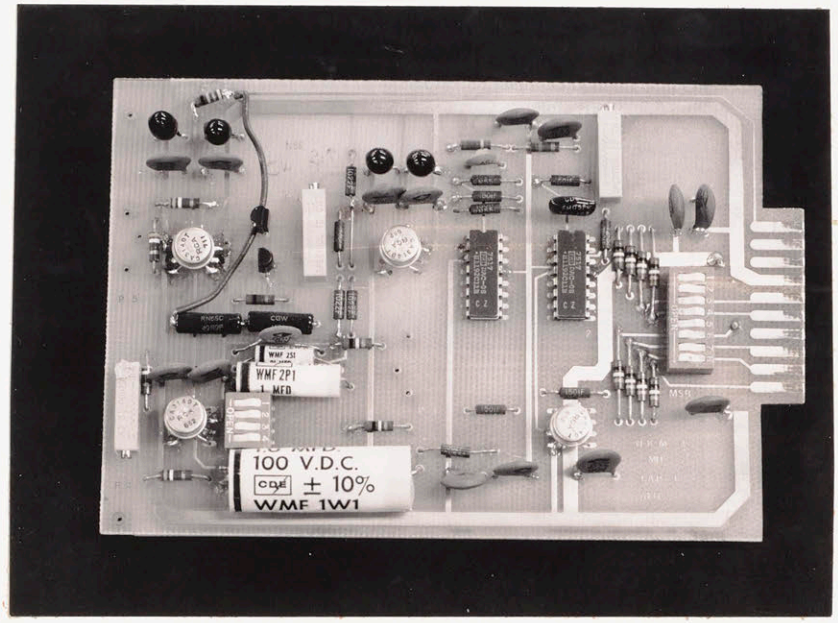


Fig. 4.8 Simulated Capacitor on a PC Board

Table 4.1

Parameter	Symbol	Numerical Value
Capacitance	C	$C = \frac{1000\ C_1}{[A]}$ μF
Maximum resolution		$\frac{1}{256}$ of maximum inductance for a particular C_1
Range of simulated capacitance values for $.00\|<C_1<\|$ μF	C_{max} (C_1 = 1 μF)	128,000 μF
	C_{min} (C_1 = .001 μF)	1 μF
Dissipation factor D for 10 μF simulated capacitor at 10 Hz (for similar mylar capacitor D = 0.00001)	D	0.002
Terminal voltage range	V_{OC}	±10 V
Terminal current range	I_L	±120 mA
Maximum operating frequency	f_u	1 kHz

These quantities were measured for various capacitor values and various operating frequencies.

4.10.1 Step Response of a Simulated RC Circuit

Single time constant networks all have energy storage elements (either an inductor or a capacitor) along with a combination of sources and dissipators. The numerical solution of such networks involves linear differential equations with constant coefficients which in the case of an RC circuit is of the form:

$$v_c = u_{-1}(t)\, V_s(1 - e^{-t/\tau}) \qquad (4.26a)$$

and

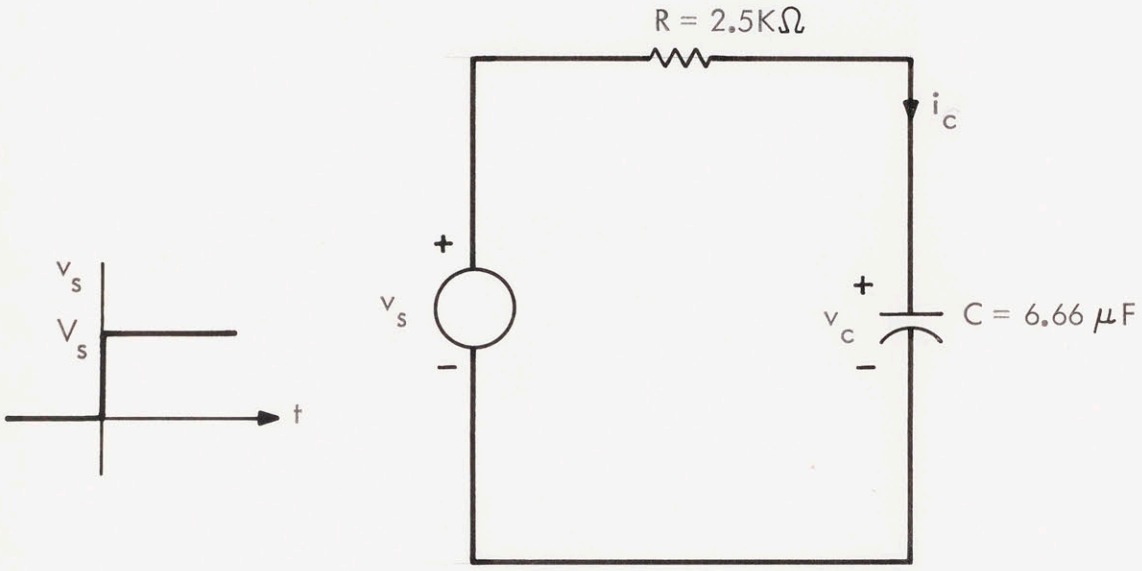
$$i_c = u_{-1}(t)\, \frac{V_s}{R}\, e^{-t/\tau} \qquad (4.26b)$$

where τ, the time-constant is given by RC. Figure 4.9 shows a general RC circuit in series with a step cource V_s. The circuit was constructed using the simulated capacitor.

Figure 4.10(a) and (b) illustrates the observed current and voltage variables. Figure 4.10(c) shows an expanded view of the capacitor current i_c from which the actual time constant is obtained. From the figure, it is observed that the device current has decayed to 1/e of its actual value in 16 msec which compares favorably well with the calculated circuit time constant of 16.25 msec.

4.10.2 Self-Discharge Measurement

From the terminals, the simulated capacitor module looks like an ideal capacitor C, in parallel with a resistor R_p. Measurement of R_p involves charging the capacitor to a known voltage V_s, and then allowing it to self-discharge. Then by measuring the discharge rate, the

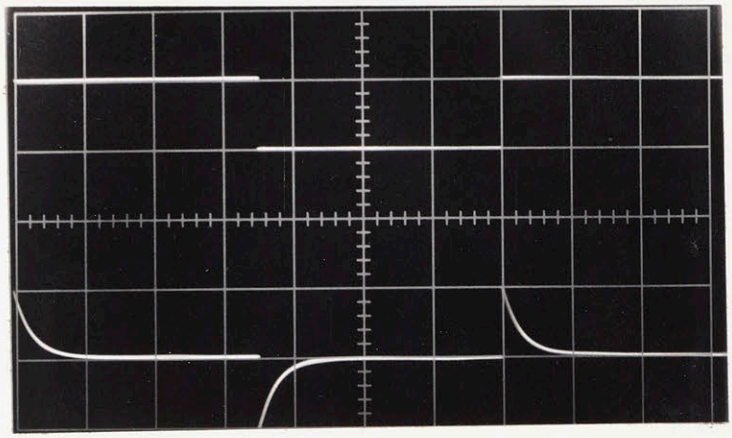


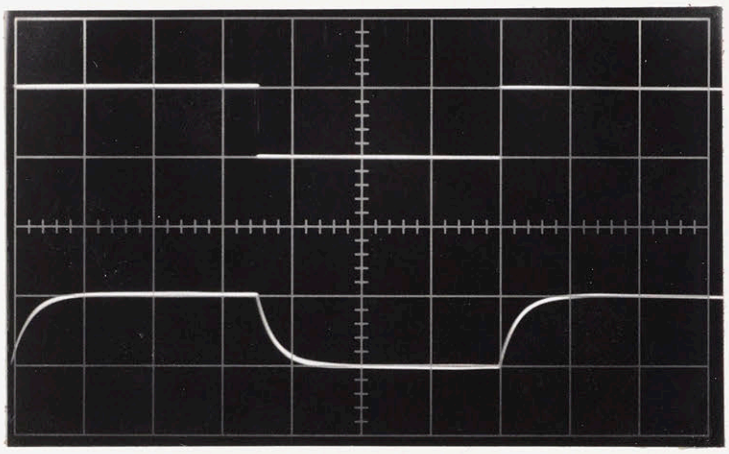
$$v_c = U_{-1}(t)\ V_s\ (1 - e^{-t/\tau})$$

$$i_c = U_{-1}(t)\ \frac{V_s}{R}\ (1 - e^{-t/\tau})$$

$$\tau = RC$$

Fig. 4.9 RC Network with a Step Source





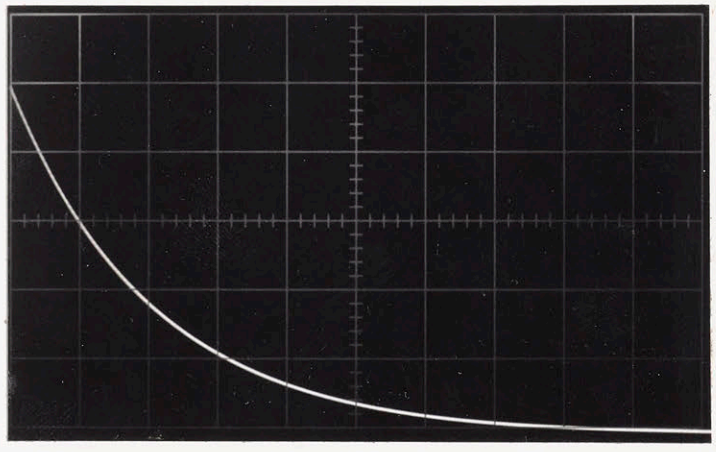


Fig. 4.10 Step Response of a Simulated RC Circuit

self time-constant τ_s, and hence R_p can be determined. From Fig. 4.11, the self time-constant τ_s is found to be 0.9 seconds. As the capacitor value is 1.0 μF, the parallel resistance R_p is 900 KΩ which compares favorably with the calculated value of 1 MΩ

4.10.3 Variation of Impedance with Frequency

Due to device limitations, the capacitor module has a maximum frequency limitation beyond which the impedance ceases to be reactive. To determine the bandwidth of the module, the impedance of the simulated capacitor was plotted as a function of frequency. Figure 4.12 shows the variation of impedance with input frequency. Clearly the impedance is capacitive up to 1 kHz which is the maximum operating frequency for the simulations.

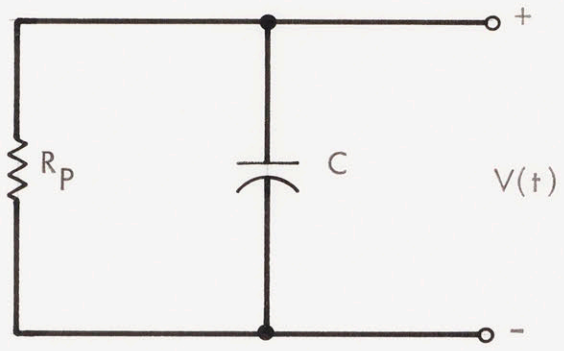


Fig. 4.11(a) Equivalent Circuit of the Capacitor Module

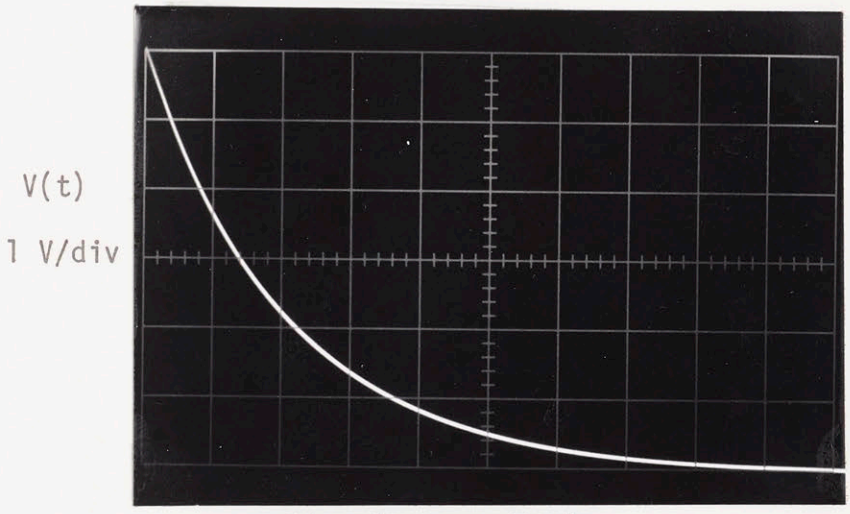


Fig. 4.11(b) Response of the Simulated Capacitor Initially Charged to 6 Volts

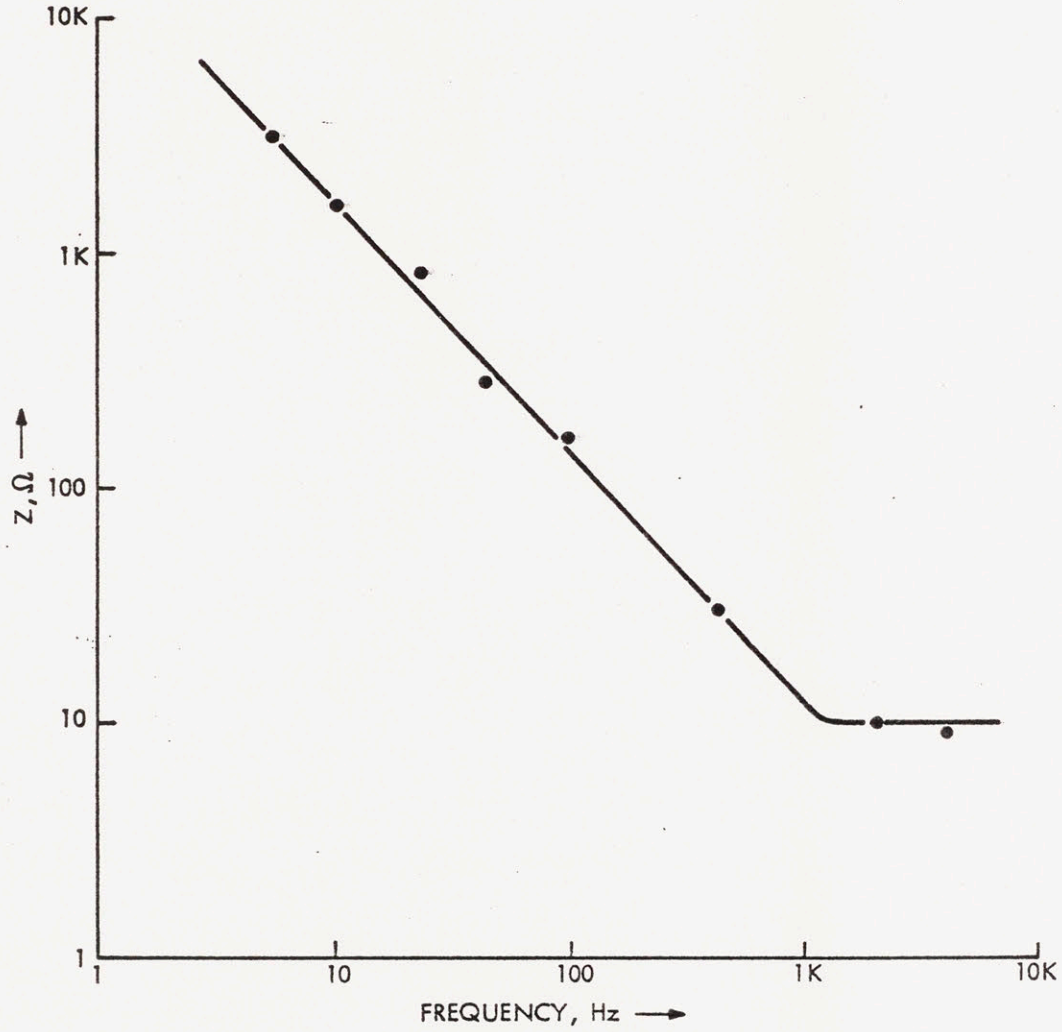


Fig. 4.12 Input Impedance of the Simulated Capacitor as a Function of Frequency

CHAPTER 5

RECTIFIER DIODE SIMULATION

Silicon rectifiers essentially contain a single p-n junction. They have low on resistance to current flow in one direction, but high resistance to the current flow in the opposite (reverse) direction. They can be operated at ambient temperature up to 200°C, current levels of a few thousand amperes and voltage levels greater than 3000 volts. In addition, they can be used in parallel or series arrangements to provide higher current or voltage capabilities.

5.1 Flow Chart for the Ideal Diode Model

All, but the simplest static power conversion systems utilize diodes in their high power circuits. Hence diode modules are invariably necessary in Parity Simulation techniques. A real diode, however, would not suffice, having numerous sources of error associated with it if used singly in the Parity Simulation. The major source of error would be the relatively high forward conduction voltage drop which is of the order of 0.6 to 0.8 volts for a typical silicon device. This magnitude of the forward drop disqualifies the real device from being used in the simulation, because voltage scaling is impossible to achieve. However, the combination of a diode with an operational amplifier results in a circuit with a much lower forward drop. This op-amp diode network results in a diode model which closely approximates an ideal diode in the forward conduction region.

The logic flow chart for the ideal diode is shown in Fig. 5.1. The logic state of the switching device is indicated by the binary variable D. This variable can be either "1" or "0" depending on whether a particular

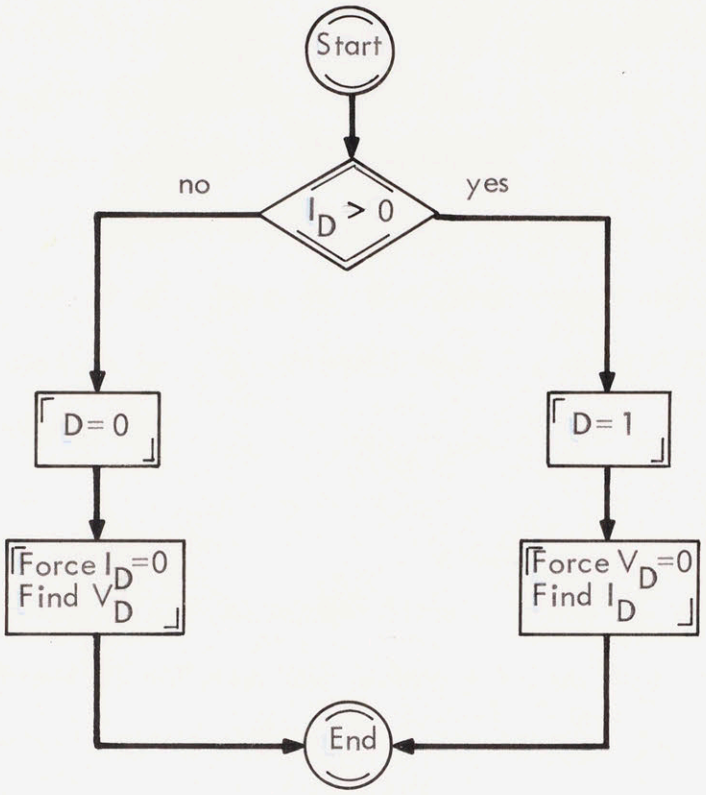


Fig. 5.1 Logic Flow Chart for the Ideal Diode Model

device is on or off. This variable is used to force the device current and device voltage as demanded by the device conditions. Obviously the flow chart simulates an ideal diode - one which completely blocks a voltage of one polarity, but allows full current flow when a voltage of an opposite polarity is applied, and has no power loss. Moreover, it (ideal diode model) has no reactive flows, no voltage breakdown, and no charge storage. Obviously such a device does not exist. However, the chief requirement for the diode module in Parity Simulation is a low forward drop - a condition which is achieved in the ideal diode model.

5.2 Diode Characterization

The characterization of the silicon diode is greatly simplified by the close correlation between the theoretical and the actual parameters. The d.c. characteristic deals with the forward voltage drop, dynamic on-resistance, breakdown voltage,reverse leakage current, etc. while the a.c. characteristic deals with the diode capacitance, forward recovery time, reverse recovery time, charge storage, etc.

5.2.1 Forward Voltage Drop

A silicon rectifier usually requires a forward voltage of 0.6 - 0.8 volts, depending upon the temperature and impurity concentration of the p-n junction, before a significant amount of current flows through the device. As shown in Fig. 5.2, a slight increase in forward voltage beyond this point causes a sharp increase in forward current.

From the analysis of an asymmetric p-n junction structure, the minority carrier distribution and flow can be expressed in terms of minority carrier concentration. From these equations, and the effect of the

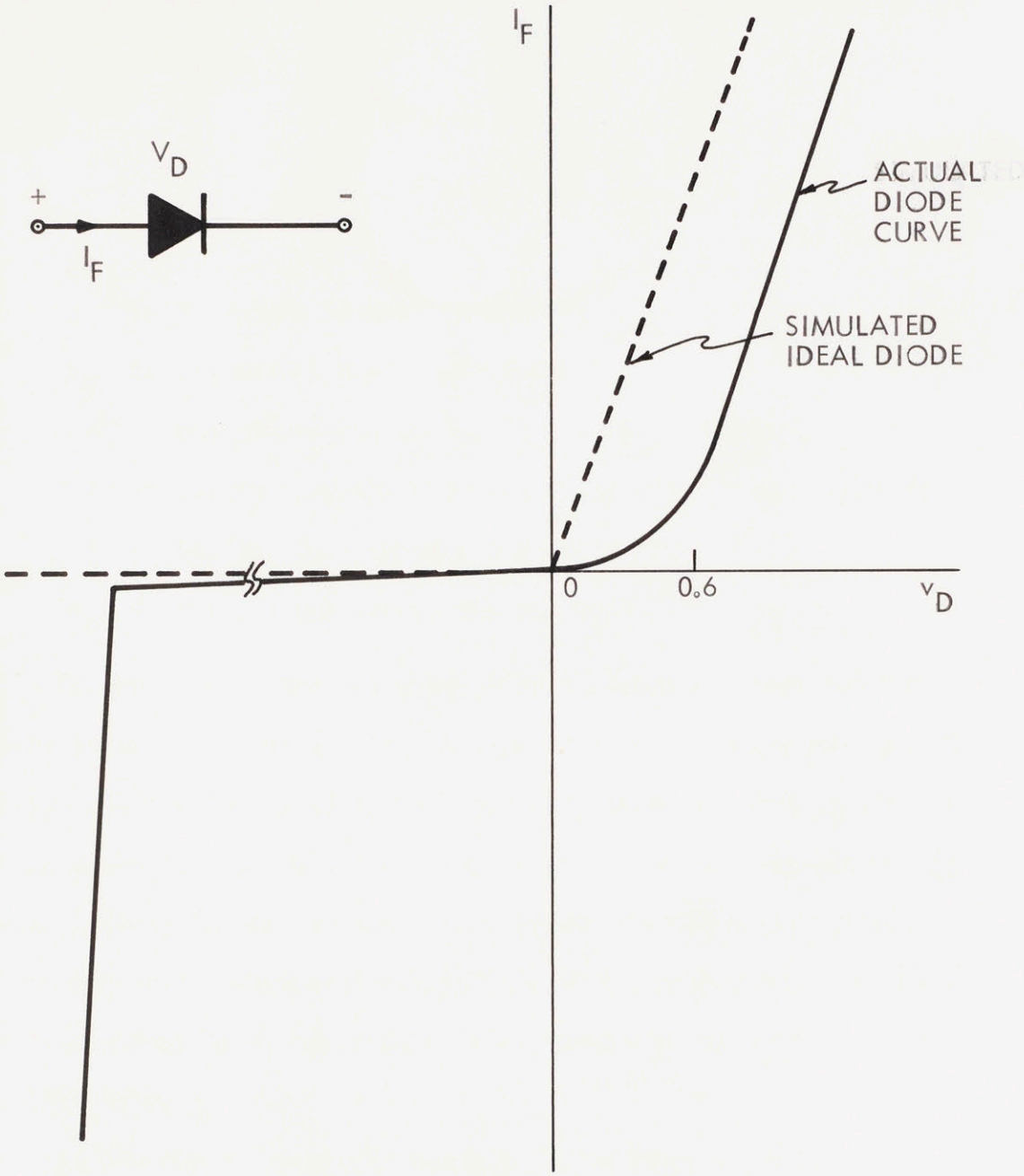


Fig. 5.2 Diode Characteristics

temperature dependence of the intrinsic carrier concentration the static electrical behavior of the p-n junction diode can be summarized by the theoretical equation:

$$I_F = I_S \left[\exp \frac{q\,V_D - I_F\,R_S}{\eta\,K\,T} - 1\right] \qquad (5.1)$$

where I_S is the diode saturation current

R_S is the series ohmic resistance

q is the electronic charge (1.6×10^{-19} coulomb)

K is the Boltzmann's Constant (1.38×10^{-23} watt sec/°K)

T is the absolute temperature in °K

V_D is the voltage across the junction

Parameter η in the above equation is dependent upon the impurity gradient in the junction and the carrier lifetime in the semi-conductor material. At low values of forward current, carrier recombination in the junction depletion layer is the predominant factor in determining the relationship between forward voltage and current and so $\eta = 2$. At high values of forward current, the relationship between forward current and voltage is determined primarily by minority carrier diffusion and $\eta = 1$. For high level injection, $\eta = 2$.

At low forward current, where $I_F\,R_S$ is negligible compared to V_D, and with the exponential term much larger than 1, Eq. (5.1) becomes

$$I_F = I_S \left[\exp \frac{q\,V_D}{\eta\,K\,T}\right.$$

or

$$V_D = \frac{\eta K T}{q} \ln \left(\frac{I_F}{I_S}\right) \tag{5.2}$$

A plot of the semiconductor diode characteristics is shown in Fig. 5.2. The graph shows that any reverse voltage in excess of a few tenths of a volt produces a small reverse current which remains constant. When a forward voltage ($V_D = + V_F$) is applied, the forward current increases exponentially. At forward voltages above the threshold voltage, (0.6 V) the slope of the voltage-current characteristic represents the dynamic resistance of the rectifier diode. This dynamic resistance r_D at a forward current I_F is obtained from Eq. (5.1) and is expressed by the equation:

$$r_D = \frac{\eta K T}{q I_F} + R_S \tag{5.3a}$$

5.2.2 Diode Capacitance

The capacitance normally specified for a diode is the total capacitance which is equal to the sum of the junction capacitance and the fixed capacitance of the leads and the package. The junction capacitance is inversely proportional to the square root of the reverse voltage and increases linearly with temperature.

5.2.3 Charge Storage

Another important mechanism in real p-n junction diodes is charge storage. When a forward current is flowing, a carrier gradient in the high resistivity side of the junction results in an apparent storage of charge. If the source of a forward bias is suddenly changed to a reverse bias, the

stored charge maintains a current flow, (now a reverse current) until the charge is depleted by a combination of reverse current flow and internal recombination. Thus the phenomenon of storage or reverse recovery time is another departure from an ideal diode. The recovery time is a strong function of the forward current and the commutation $\frac{di}{dt}$, where commutation di/dt is the rate of change of current from the forward current level to the reverse current peak.

5.2.4 Leakage Current

Whenever a semiconductor p-n junction is reverse biased, a reverse or leakage current (I_R) flows through the junction. This reverse current is the sum of three currents: I_D due to diffusion, I_G due to charge and I_S due to surface leakage. Therefore

$$I_R = I_D + I_G + I_S \tag{5.3b}$$

5.2.5 Forward Recovery

A final undesirable property of real diodes is forward recovery time t_{fr}. Forward recovery time is defined as the time required for the voltage across the diode to reach a steady state value after a forward pulse is applied. When a current step (pulse) is applied to a diode, the diode cannot build the carrier gradient immediately; an overshoot voltage is observed and the diode appears to be inductive; however, transit time and conductivity modulation, not inductance are responsible for the effect.

5.3 Actual Diode Model

The various properties of real diodes (resistance, capacitance, charge storage, etc.) can be added to the ideal diode model of Fig. 5.1 as

external elements to get the equivalent circuit shown in Fig. 5.3.

The diode, which follows Eq. (5.1) is given the zener symbol as it has a voltage limit V_B, where V_B is the avalanche breakdown voltage. The series resistance, r_F is shown as variable to partly account for forward recovery time, it also accounts for forward voltage drop. The resistor r_S accounts for the surface component of the reverse current and is also generally used to account for changes in bulk current. I_G is the charge generation current generator.

Capacitor C_T represents the transition capacitance. The diffusion capacitance C_D partially accounts for the forward recovery effect because it is a measure of carrier transit time. L is also generally required to account for t_{fr}. C_D also accounts for storage and turn-off time. C_D does not behave like a normal capacitor, in that its value is proportional to forward current.

5.4 Ideal Behavior

In Parity Simulation, the real diode is replaced by an analog model which evaluates terminal conditions and makes a decision regarding the "operating region" of an op-amp - linear or saturation region.

Modeling of the ideal diode is done using an op-amp, a real diode and a handful of other components. A few of the characteristics of the real diode mentioned in the preceding sections, for example the junction capacitance, have not been implemented. This is simply because such characteristics are of little significance in most power rectifier applications. The characteristics of particular significance in Parity Simulation are the forward voltage characteristic, the stored charge and the reverse recovery

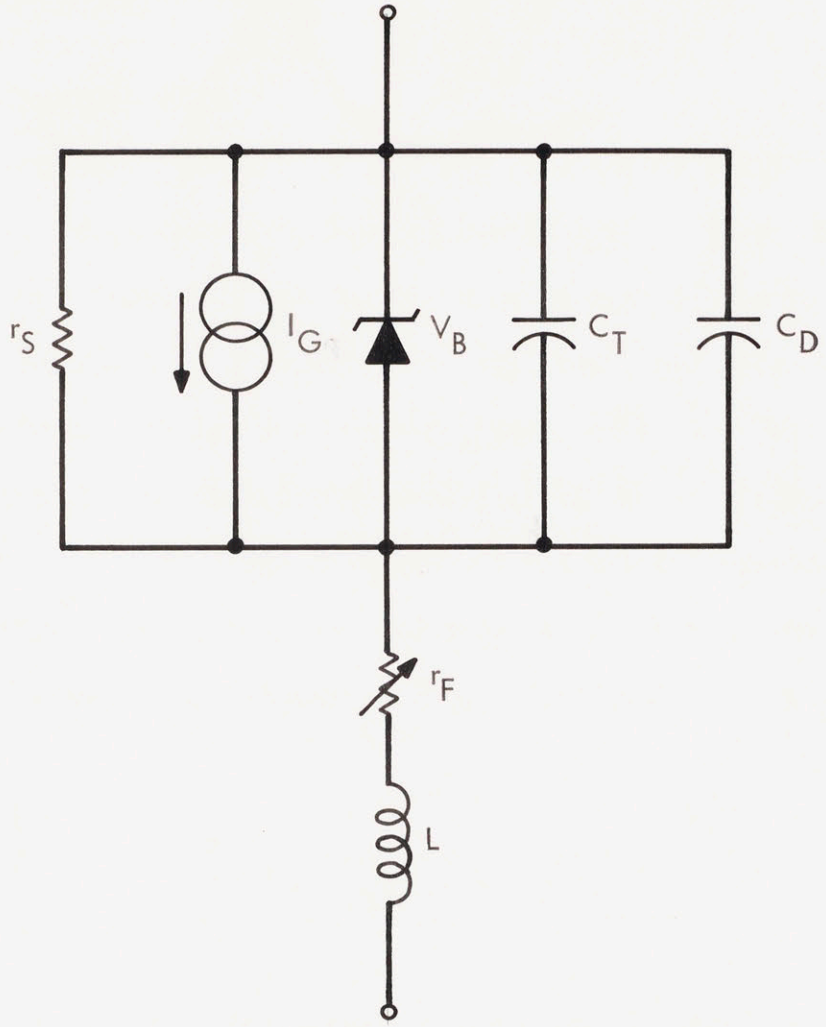


Fig. 5.3 Equivalent Circuit of a Diode

characteristic. Particular attention has been paid to the latter as this is one of the most important characteristics in power rectifier applications.

5.5 Ideal Diode Model

As discussed in earlier sections, the actual rectifier diode has finite resistance and nonlinear switching characteristics. These characteristics contribute to a "rounding" of the break point area of the rectifier characteristic as illustrated in Fig. 5.2. Ideally, the break point would be sharp and well-defined. In the precision rectifier circuit of Fig. 5.4(a) the high open-loop gain of the operational amplifier is used to reduce the effect of the diode nonlinearity. The operation of the circuit can be analyzed by the usual techniques except that the relationship of current and voltage in the diode must be taken into account. This relationship is given by Eq. (5.2) as:

$$V_D = \frac{1\ K\ T}{q}\ \ell n\ \left(\frac{I_F}{I_S}\right)$$

Figure 5.4(a) illustrates a circuit where a real exponential diode is used as a negative feedback element around an operational amplifier. When $v_i > 0$, the diode is turned on and consequently the feedback loop is closed resulting in the op-amp operating in the linear region. Linear region operation implies that the voltage at the inverting input is negligibly small, hence the diode current i_D which equals the input forward current i_i is of the form:

$$i_i = I_F = \frac{v_i}{R} \qquad V_I > 0 \tag{5.4}$$

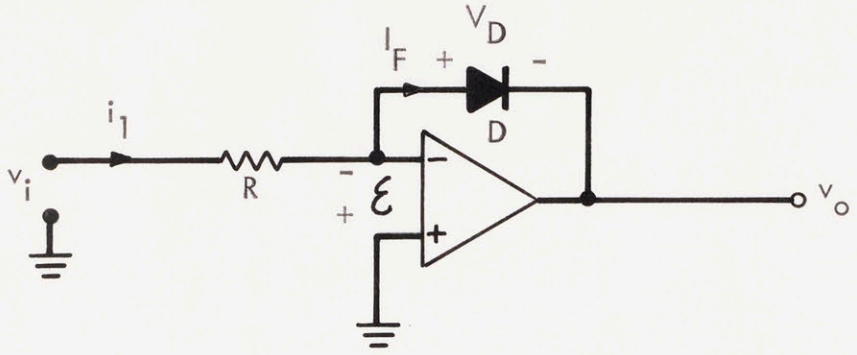


Fig. 5.4(a) Precision Rectifier

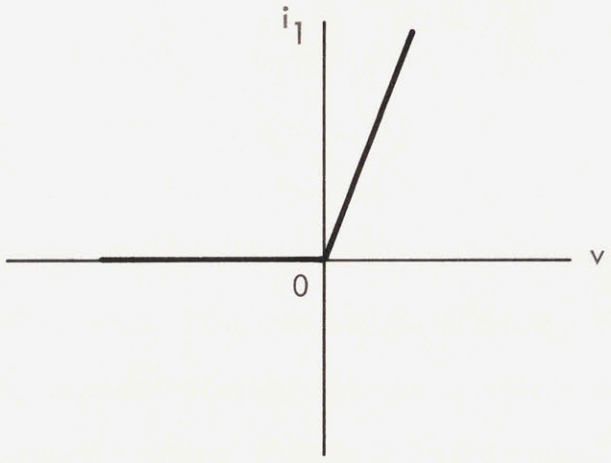


Fig. 5.4 (b) Transfer Characteristics of the Precision Rectifier

where R is the external circuit resistance. Combining Eqs. (5.2) and (5.4), the result is

$$i_i = \frac{v_i}{R} = I_s \exp \frac{q V_D}{\eta K T} \qquad (5.5)$$

with

$$v_o = - V_D$$

Taking the finite amplifier gain A, and the diode nonlinearities into account, the expression for the forward drop of the ideal diode becomes:

$$\varepsilon = \frac{-v_o}{A} = \frac{V_D}{A}$$

$$\therefore \varepsilon + \frac{0.6}{A}$$

This is an extremely small voltage, certainly much less than the forward drop of an actual diode. Thus the ideal diode provides a good approximation of the idealistic characteristics one would expect in reducing diode nonlinearity and forward voltage drop by a factor equal to the loop gain of the amplifier.

5.6 Explanation of Operation

Precision rectifiers alter the input signal depending on its instantaneous polarity. A half wave rectifier can be made to remove either the positive or the negative portions of a waveform. It performs very closely to the expected response of an ideal diode. The ideal diode possesses several advantages relative to the silicon diode. First the ideal diode can rectify signals down to approximately zero volts amplitude. Second, the forward conduction region is linear.

In the inverting half-wave precision rectifier circuit shown in Fig. 5.4(a) the two ideal properties discussed above can be approached with nearly zero error. The circuit will rectify low-level signals with peak voltages of only 0.6/A volts. The circuit operates in the following way. For small instantaneous positive voltages, (less than 0.6 volts) the amplifier is practically open-loop and so a relatively large positive voltage appears at the output end of the feedback elements, forcing the diode into forward conduction. The gain of the operational amplifier automatically adjusts itself to keep the summing voltage at virtual ground.

For negative input voltages, the current i becomes negative with a limitation of $-I_s$. If v_i/R is less than $-I_s$ as it invariably is, the current through the reverse biased diode cannot balance the current I_o. Accordingly, the amplifier output voltage is forced negative until the amplifier saturates. When this occurs the feedback loop cannot keep the voltage at the inverting amplifier input negligible small because of the limited current ($-I_s$) the diode can conduct in the reverse direction. This constraint necessitates the use of an operational amplifier which does not have input protection diodes, such as the μA 741C.

5.7 Simulated Diode Circuit Model

Figure 5.5(a) shows the circuit configuration of the simulated diode model. The buffer stage which is a complimentary transistor pair gives a current gain to the model. An interesting addition is the offset potentiometer P_1, which enables the operator to have some control of the threshold voltage (break point). This control of the break point allows the operator to scale the forward voltage drop of the simulated diode. Obviously in the

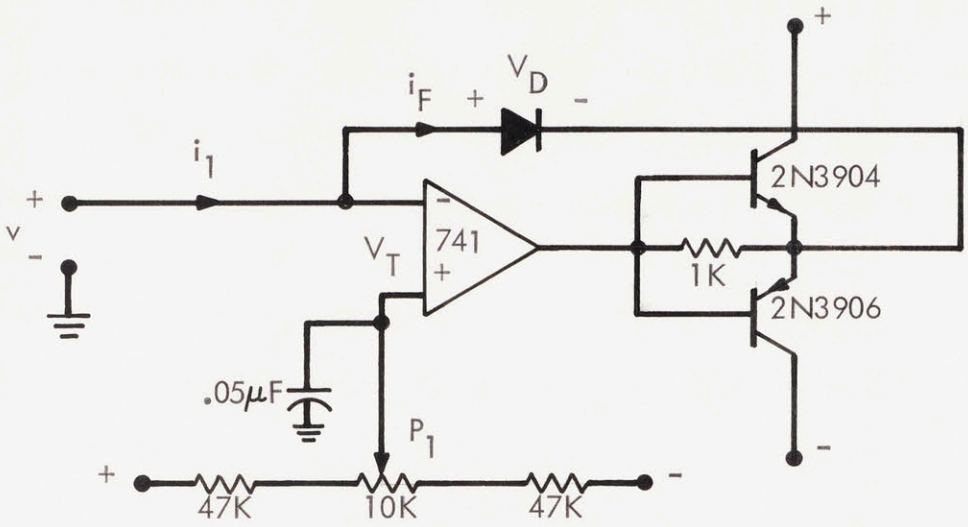


Fig. 5.5(a) Simulated Diode Circuit Model

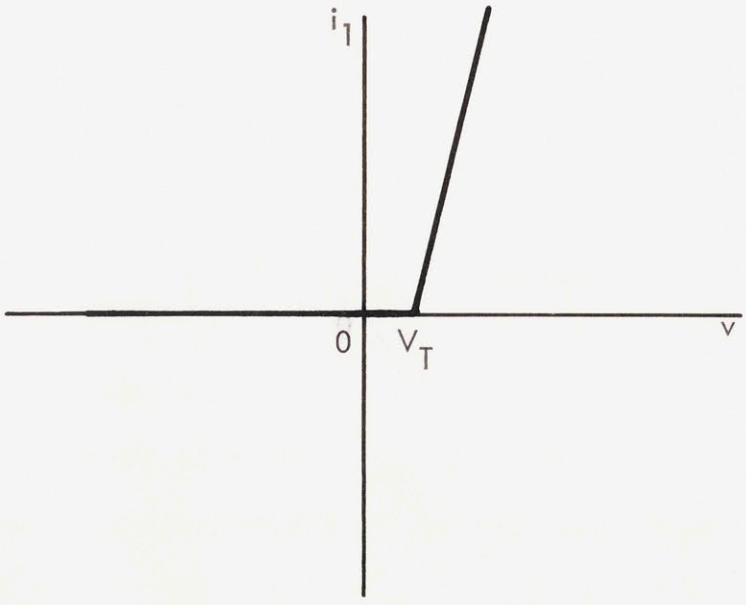


Fig. 5.5 (b) Transfer Characteristics of the Simulated Diode Model

simulated diode circuit model, the threshold voltage is dependent on the bias voltage applied to the operational amplifier. This bias voltage is determined by the setting of potentiometer P_1. The simulated diode suffers from one disadvantage: non-availability of a terminal which would give a voltage signal proportional to the current flowing. A solution would be to incorporate a floating input current-to-voltage converter in the model.

5.8 Electrical Characteristics

These specifications apply for $V_S = \pm 15V$ $T_A = 25°C$ unless otherwise specified.

Table 5.1

Parameter	Symbol	Numerical Value
Peak repetitive reverse voltage	V_{RRM}	10 volts
Average rectified forward current	I_o	120 mA
DC forward voltage drop	V_F	Can be adjusted from 0-600 mV

5.9 Experimental Results

With the described diode model, the significant electrical design parameters were accurately determined and recorded. Among the measured quantities are:-

1. Peak rectifier current
2. Reverse recovery current
3. Transfer characteristics on a transistor curve tracer.

5.9.1 Test Results and Waveforms

Current waveforms

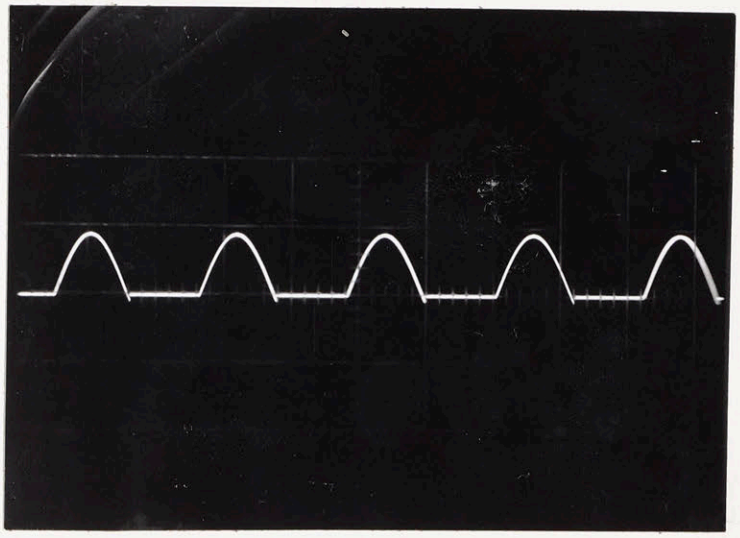
Figures 5.6(a), (b) and (c) illustrate the forward and reverse recovery currents of the simulated device. Clearly the device acts as a rectifier with a high forward-to-reverse current ratio. This reverse recovery characteristic was not built into the simulated diode model, but it is due to the slew rate limitation of the operational amplifier. Figures 5.7(a), (b) and (c) show the effects of peak forward current variations and circuit limited rate of fall of the initially high anode current (di/dt) of the device. In Fig. 5.7(c) the reverse recovery current is much higher than in either 5.7(a) or (b) clearly indicating that reverse current I_R is a strong function of the peak forward current and the circuit limited di/dt. Figure 5.8 illustrates the test set-up used for the measurement of the simulated diode parameters.

Transfer characteristics

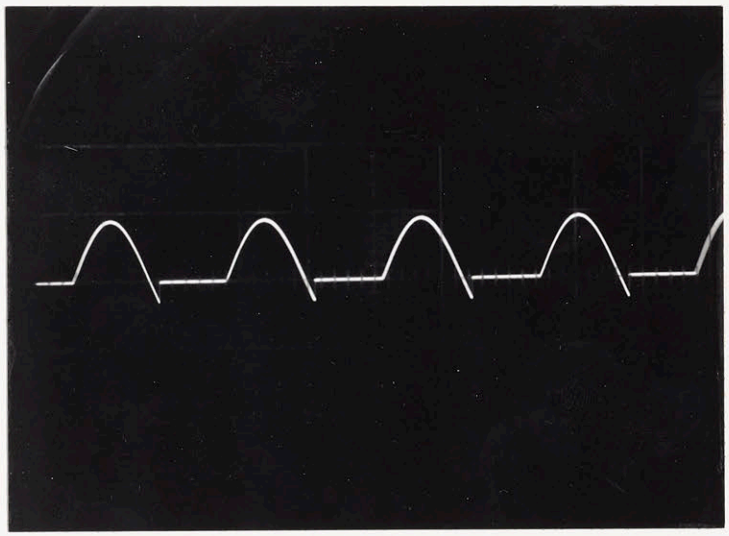
Reverse and forward volt-ampere curves of the simulated rectifier diode are shown in Fig. 5.8. The two areas - forward and reverse will be separately examined.

Forward DC characteristics

The forward characteristics of the simulated rectifier diode very closely approaches an ideal diode. The volt-ampere curve is linear and the break point (threshold voltage) is sharp and well-defined. This threshold voltage is clearly illustrated in Figs. 5.9(a) and (b). For "ordinary" silicon diodes, the break point occurs at approximately 0.6 volts, and the diode attains full conduction at voltages greater than the above value.

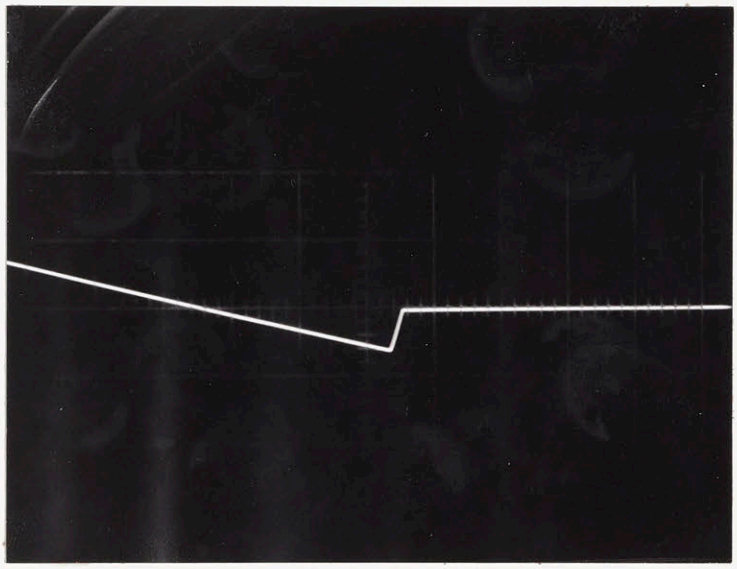


(a) Scales: Horizontal : 2 mA/div
Vertical : 2.5 msec/div



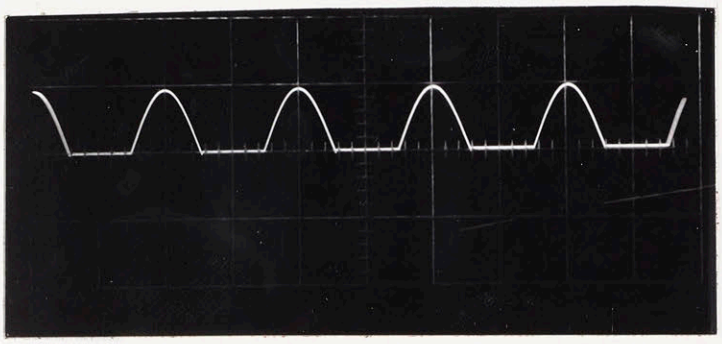
(b) Scales: Horizontal : 2 mA/div
Vertical : 1 msec/div

Fig. 5.6 Rectified Forward Current in Simulated Diode Model



Scales: Horizontal : 0.5 mA/div
Vertical : 20 μsec/div

Fig. 5.6(c) Reverse Recovery Current in Simulated Diode Model

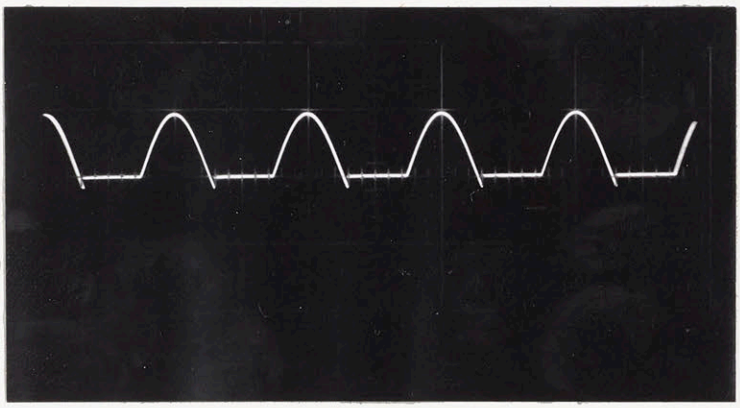


Diode Current (2 mA/div)

(a)

$\frac{di}{dt}$ = 0.4 mA/ms

Time (5.0 msec/div)

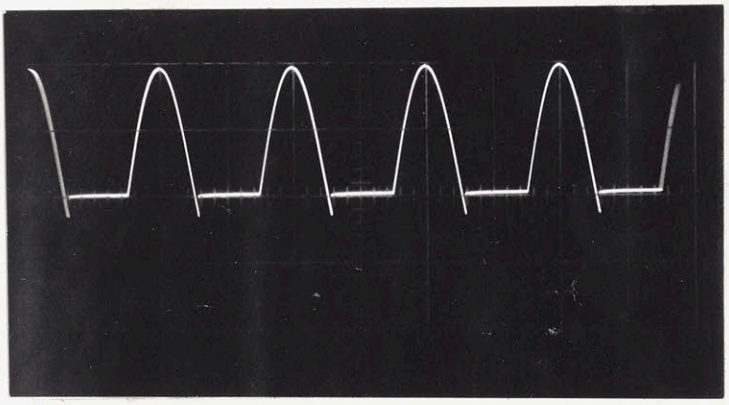


Diode Current (2 mA/div)

(b)

$\frac{di}{dt}$ = 4 mA/ms

Time (0.5 msec/div)



Diode Current (2 mA/div)

(c)

$\frac{di}{dt}$ = 4 mA/ms

Time (1.0 msec/div)

Fig. 5.7 Reverse Recovery Characteristics

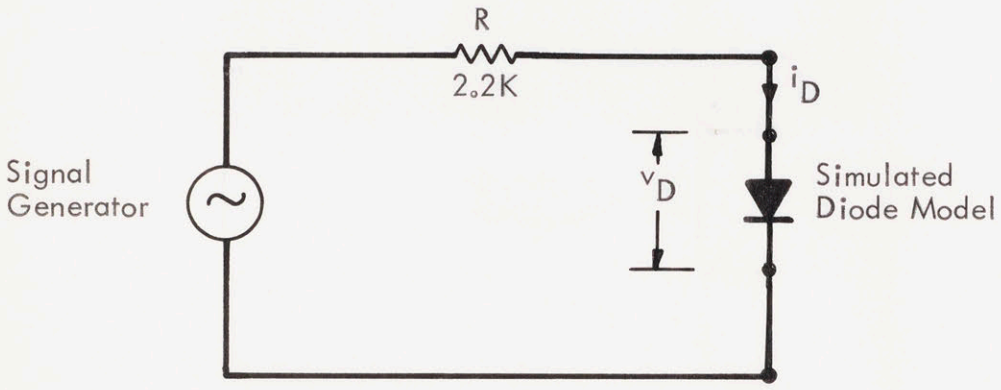
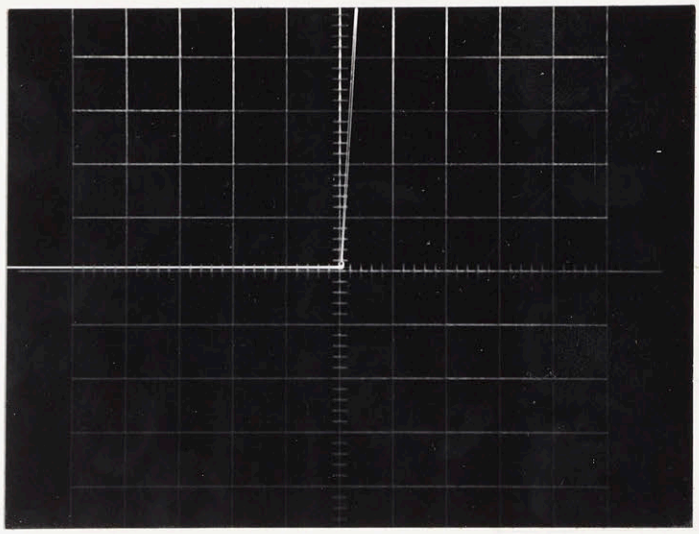


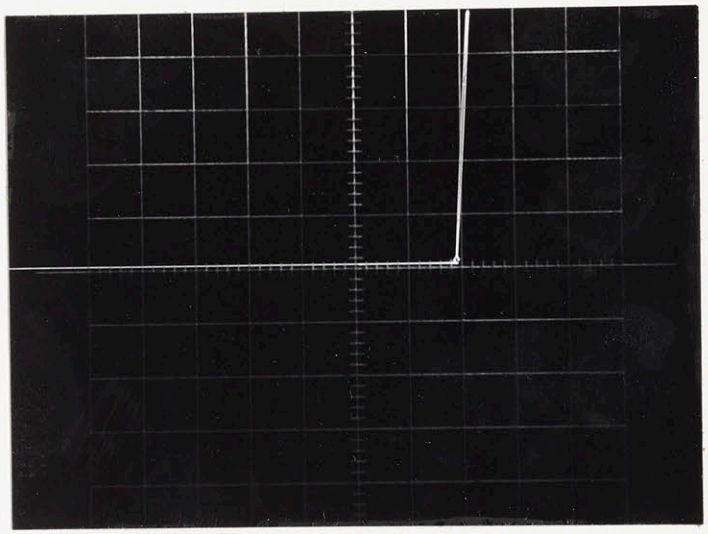
Fig. 5.8 Test Circuit for Measurement of Simulated Diode Parameters

(a)



Scales: Horizontal : 10 mV/div
Vertical : 2 mA/div

(b)



Scales: Horizontal : 10 mV/div
Vertical : 2 mA/div

Fig. 5.9 Simulated Diode Transfer Characteristics
(a) Threshold = 0 V
(b) Threshold = 20 mV

Figure 5.9(a) shows the break point at the origin, and Fig. 5.9(b) shows the break point at 20 mV. By varying the setting of potentiometer P_1, the break point can be set to any predetermined value.

Reverse characteristics

When reverse voltage less than the supply voltage is applied to the simulated diode model, the behavior of the current is similar to any back-biased silicon p-n junction. The typical volt-ampere curve has almost zero slope as seen in Figs. 5.9(a) and (b).

At some definite reverse voltage greater than the power supply voltage the simulated diode no longer operates as a diode. However, in actual practice the maximum peak voltages are less than or equal to 10 volts; hence the so called "break down" area is never encountered in the simulation.

CHAPTER 6

ANALOG-DIGITAL MODEL OF A THYRISTOR

The silicon controlled rectifier (SCR) is a solid state semiconductor four layer N-P-N-P device. The SCR, in its normal state will block an applied voltage in either direction; but when a trigger pulse is applied to the gate electrode, current will flow from the anode to the cathode, thus completing the load circuit. On removal of the applied voltage, the device will block again, but it cannot be turned on. It is therefore equivalent to a rectifier, except that conduction is initiated by the gate, at a predetermined time. Once conduction starts, the gate exercises no further control. The SCR is therefore the solid state equivalent of a thyratron.

6.1 Behavior of the Thyristor as a Switch

The thyristor has essentially two states: a blocking state in which it behaves in the same manner as a reverse-biased diode, and a conducting state, in which it operates in the same manner as a forward biased diode. The diode and thyristor differ in that only the latter can block forward voltage. As an ideal thyristor is either "off" or "on" only two values are required to indicate its state and a Boolean variable is the obvious choice.

Before the switch can replace the thyristor, it must possess a number of attributes as follows:

a) Switch closure can occur only for positive values of the simulated device voltage.

b) Currents greater than zero maintain the switch in the closed position.

c) The switch allows only positive-current flow. It is not the magnitudes, but the polarities of the voltage and current which are important and so these are represented by Boolean variables.

6.2 Flow Chart for the Thyristor Model

The basic flow chart for the digital thyristor model is shown in Fig. 6.1. The logic state of the device is shown by the binary variable C. The variable C can be either 1 or 0, depending on whether a particular device is on or off, respectively. These variables are used to force the device current I_{AK} and the device voltage V_{AK} as demanded by the device conditions. For consistent triggering of the thyristor, the magnitude of the gate drive must be greater than a specified value if the thyristor is to be consistently triggered. In normal design practice, it is ensured that the gate drive achieves this value, so the presence of a gate signal can be equated to the conduction of the thyristor, provided, of course, that the device voltage is of the correct polarity. A Boolean variable "T" indicates the presence or absence of a gate drive, T being equal to 1 when the trigger is present, and being equal to 0 when the gate pulse is absent.

6.3 Digital Modeling of a Thyristor

In Parity Simulation, the thyristor is replaced (simulated) by an analog-digital model. This model evaluates terminal conditions, and makes a decision regarding the state of a reed relay, which is the actual switching element. The analog model is built round a digital functional block, the latter having regenerative feedback so essential for actual thyristor simulation. Different digital models were considered and the optimum selected on the basis of simplicity, number of terminal connections and the

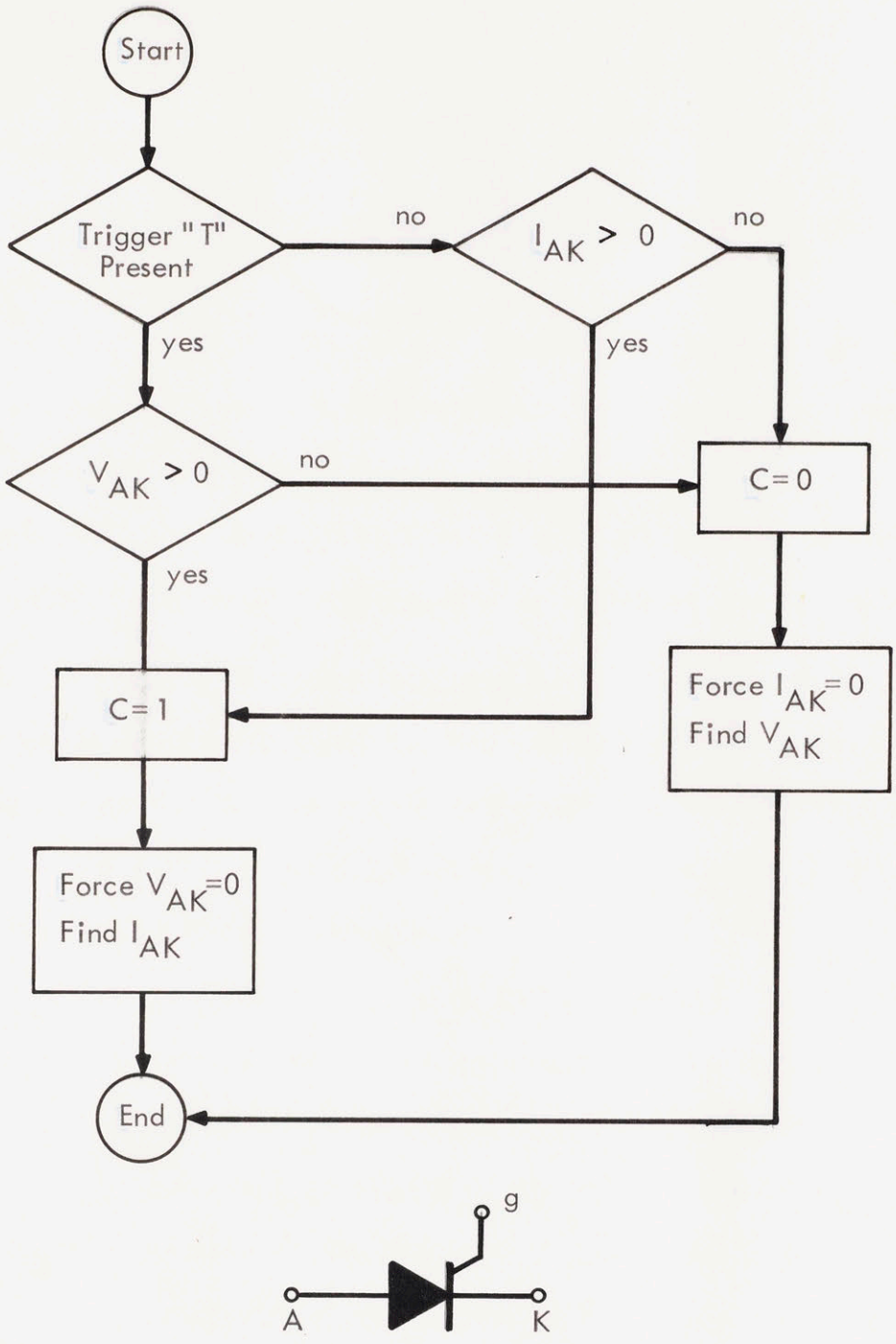


Fig. 6.1 Flow Chart of a Digital SCR

presence or absence of "hazards" in the logical model.

6.3.1 Principle of Model Operation

The state of the SCR can be easily deduced if the following information is known:

a) whether the device is reverse biased or forward biased

b) whether the device is forward biased and there is a trigger signal at the gate

c) whether there is neither forward nor reverse bias on the device after it has been triggered during a forward bias period.

State (a) clearly indicates that the device is off, (b) indicates the state at which the device turns on, and (c) indicates that the device is on. This type of device characteristic indicates a basic flip-flop operation. Figure 6.2 is a schematic of the logical model. The behavior of the model is indicated using the following information:

i) $T = 1$ corresponds to a gate signal present

ii) $T = 0$ corresponds to the absence of a gate signal

iii) $V_{AK} = 1$ indicates the presence of a positive anode cathode potential greater than the forward conducting voltage

iv) $V_{KA} = 1$ represents the presence of a cathode anode voltage greater than zero. Clearly V_{AK} is not the logical inverse of V_{KA} since when the device is on, $V_{AK} = V_{KA} = 0$, though when the device is off, $V_{AK} = \overline{V_{KA}}$. This is illustrated in Fig. 6.3.

v) The state indicator C indicates the state of the SCR; $C = 0$ when the SCR is off and $C = 1$ when the device is on.

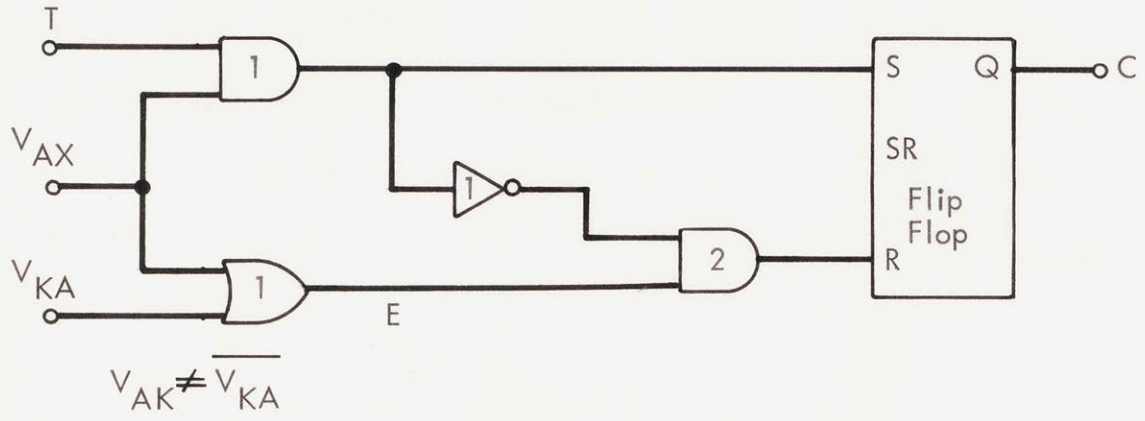
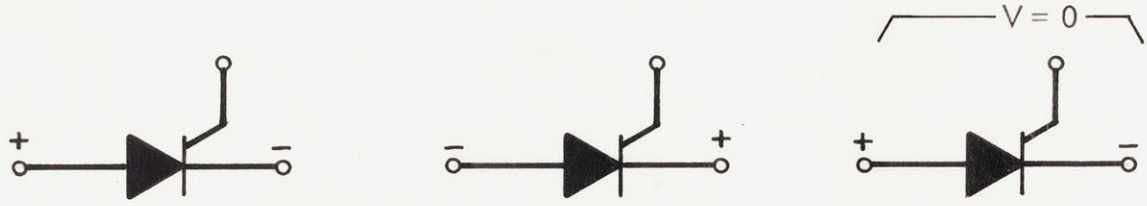


Fig. 6.2 Basic SCR Model



$V_{AK} = 1$
$V_{KA} = 0$
Device is OFF

$V_{AK} = 0$
$V_{KA} = 1$
Device is OFF

$V_{AK} = 0$
$V_{KA} = 0$
Device is ON

Fig. 6.3 Illustrating the Significance of V_{AK} and V_{KA}

The following sequence is used to illustrate the operation of the model. All inputs are logic states which are obtained from the external circuit and converted to logic levels. The conduction state C, basically depends on the trigger pulse T, V_{AK}, and V_{KA}; the memory or latching device being the Set-Reset flip-flop indicated as S/R F-F in Fig. 6.2. Four logic gates have been employed, and for the present it is assumed that all four gates have equal gate delays. From the figure it is seen that the "S" and "R" inputs are defined as follows:

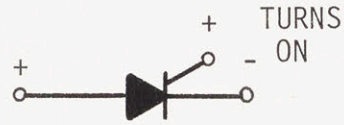
$$S = V_{AK} \cdot T$$

$$R = (V_{AK} + V_{KA})(\overline{V_{AK} \cdot T})$$

Obviously the Set-Reset flip-flop defines the state of its output as a function of the state of its inputs; both outputs being uniquely determined by the inputs S and R, except when both these inputs are 1. The latter case (S = R = 1) is an undefined state as in this case both Q and $\overline{Q}$ become high.

Now if there is a forward bias on the device but no trigger signal, V_{AK} = 1 and T = 0, and the S-R flip-flop is reset. The state indicator C indicates that the output is 0 and that the device is off. If the device is now triggered, T becomes 1 with V_{AK} = 1, the set terminal S is 1 and C = 1, implying that the device is now on. Removal of the trigger pulses has no effect on the output C and the model will continue to indicate on until V_{AK} or V_{KA} appears, when the device is reset, indicating C = 0. The Truth Table 6.1 describes the operation of the device.

Table 6.1

State	T	V_{AK}	V_{KA}	S	R	C
	Φ	0	1	0	1	0
	0	1	0	0	1	0
	1	1	0	1	0	1
	Φ	0	0	0	0	1
	Φ	0	1	0	1	0

Φ = don't care

Although the model thus emulates the state of the device, it has the following drawbacks:

1. The model has 4 terminals making it topologically different from a real thyristor. Interconnections between devices is also more difficult due to an additional terminal.
2. The model does not consider one of the basic properties of the SCR - holding current. In fact, there is no provision for a logical input to indicate the presence of a forward current or reverse recovery current.
3. As the forward conducting voltage V_{AK} is not the inverse of V_{KA}, two logical voltage monitors are required, one for each of the above inputs (V_{AK}, V_{KA}).

4. The model is a combinational logic without actual positive feedback from the output "C" to either of the three inputs "V_{AK}", "V_{KA}" and "T". Actual regeneration can be manifested by the elimination of the "V_{KA}" terminal.

Hence another model is presented, which simulates the thyristor in such a way that it not only has the same number of terminals, but also includes the internal feedback property; yet has one less logic gate and no flip-flops. This model is the basic functional block around which the SCR module is built.

6.4. Regenerative Feedback in a Thyristor

An understanding of the positive feedback action that results when a thyristor is triggered can be obtained using the two transistor analogy This can best be visualized by connecting two transistors, a p-n-p and an n-p-n, to form a regenerative feedback pair as shown in Fig. 6.4. When the gate current circulates, this initiates a current flow in the collector of transistor T_1 providing base drive for T_2. Similarly, the collector of T_2 supplies base drive for T_1. Thus a regeneration situation occurs driving both transistors to saturation. Once in saturation, the total potential drop across the device approximates that of a single p-n junction, and the anode current now is limited only by the external circuit. This implies that the thyristor is logically a sequential switch, and may be represented by an equivalent logic block diagram, shown in Fig. 6.5. In this block diagram, at $t = t_0$, assume that there is no gate signal and no positive bias on the anode of the thyristor, thus the state indicator F indicates that the SCR is off (F = 0). At time $t = t_1$ a trigger pulse is applied to terminal g, giving a logic equivalence of $I_g = 1$, but again the output F is low as there

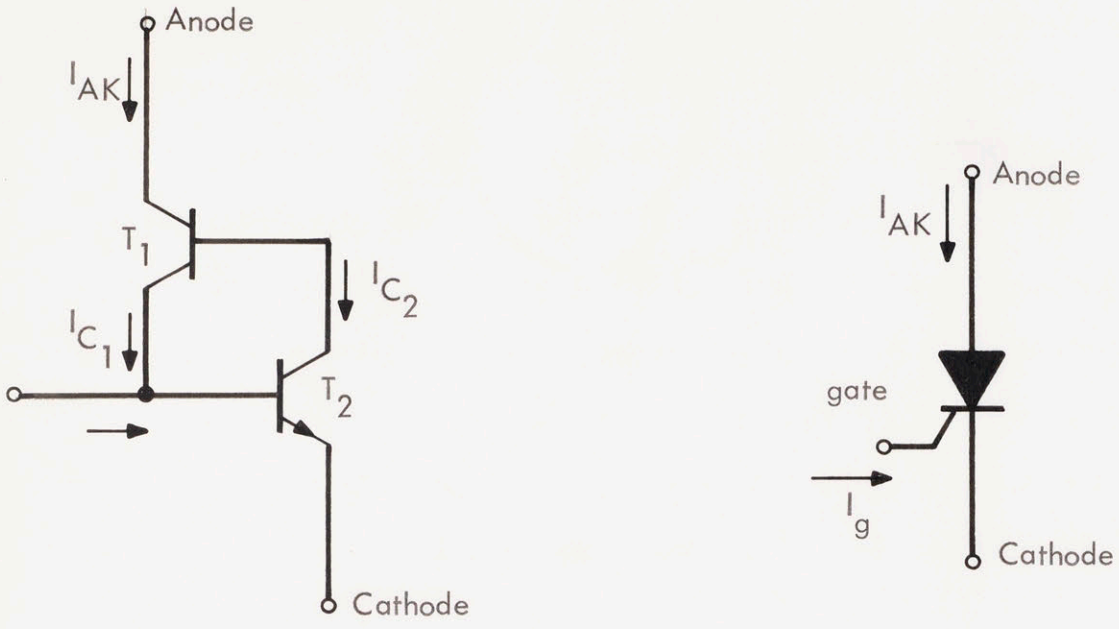


Fig. 6.4 Two Transistor Analogy of a Thyristor

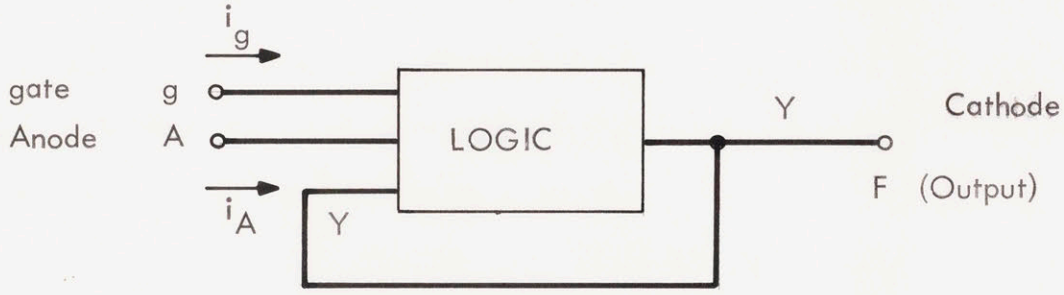


Fig. 6.5 Thyristor Logic Block Diagram

is no positive bias on the thyristor. When terminal g returns to zero, there is still no change in the state of the thyristor. However, when the anode terminal 'A' goes high, and the gate terminal g is triggered, the output F goes high, indicating that the thyristor is now switched on. At this point a response to output "F" appears at terminal 'y', and the thyristor latches on. Now the gate trigger pulse is no longer required to maintain the device in its on-condition. Hence when terminal 'g' returns to zero at time t_4 there is no change in output F. At time t_5 the anode "A" goes low and the thyristor is turned off; the output F returns to zero and is back at the starting condition.

6.4.1 Functional Representation of the Thyristor

From the preceding discussion, the thyristor state F is known to depend on the polarity of the terminal 'A' and the existence of the gate signal at 'g'. As has already been stated, all these variables are of the Boolean type and the problem is to derive a Boolean-functional representation of the thyristor in terms of these variables.

The first step in finding the functional representation of the thyristor state on the aforementioned variables is to define its output by a flow table and hence to derive a Karnaugh map. These are tabulated in tables 2 and 3.

Table 6.2
Flow Table

g / F \ A	00	01	11	10
0	1		3	2
1	1	4	3	

Table 6.3
Karnaugh Map of Modes of Operation

F \ g A	00	01	11	10
0	0	0	1	0
1	0	1	1	0

The method of prime implicants is then employed to obtain the equation for the excitation and the output. Equation (6.1) gives the functional representation of the thyristor in Boolean form:

$$F_{n+1} = \overline{\overline{A \cdot g} + \overline{A \cdot y_n}} \qquad (6.1)$$

where F_{n+1} is the next state in terms of present state y_n and input states A, and g; A and g being used to test the circuit equivalence to the thyristor in logical operation. Thus the relationship of Eq. (6.1) predicts that the thyristor is in the 'on' state when the thyristor is forward biased, i.e., when terminal A = 1, and when the trigger pulse is applied to the thyristor, i.e., when g = 1. If terminal A was now made low, i.e., the logical equivalence of anode current being less than the holding current, then the resulting state equation shown below (6.2) indicates that the thyristor recovers its blocking condition.

$$F_{n+2} = \overline{\overline{A \cdot g} + \overline{A \cdot y_{n+1}}} = 0 \qquad (6.2)$$

where $A = 0$

$y_{n+1} = F_n = 1$

$g = \phi$ ϕ signifies a "don't care"

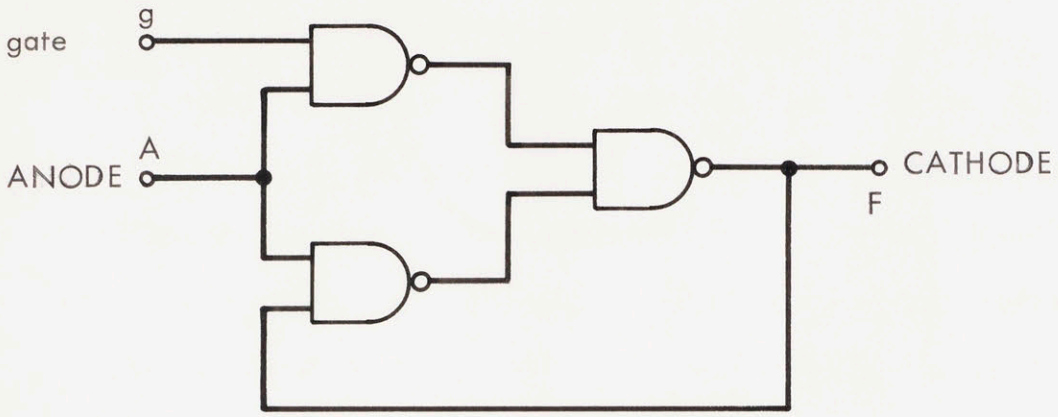
The model thus accurately emulates the state of the device. It is a relatively simple digital model which employs a minimum of input functions, and it does not require any new variable to be defined and monitored in the previous model.

6.4.2 SCR Digital Module

The circuit shown in Fig. 6.6 is a practical realization of the logical model given by Eq. (6.1). The figure also illustrates the operating waveforms of the SCR models for a typical 'turn-on', and it is clear that proper operation of the model results, without hazards or oscillations. Due to the desirable features of this digital model, it is selected for modeling the SCR; however, any model of the SCR must emulate the basic characteristics of the device. As this is purely a digital model, specific analog circuits are built around it to enable the completed model to respond directly to analog as well as digital signals.

6.5 Analog-Digital SCR Model

The family of thyristor devices has in common a switching capability in one or two quadrants of its V-I characteristics. Thyristor devices are switched into the on-state by applying a trigger signal to the gate, the anode-to-cathode voltage having been positive. The SCR remains on, after removal of the gate pulse, if the anode-cathode current is greater than the holding current of the device. If the device is on, the state of the trigger is irrelevant. After the SCR has been turned on, it remains so until the anode current returns to a value less than the holding current. Another important feature is that SCR conduction is unilateral, i.e., negative-anode current is not possible, except for the reverse recovery current. The



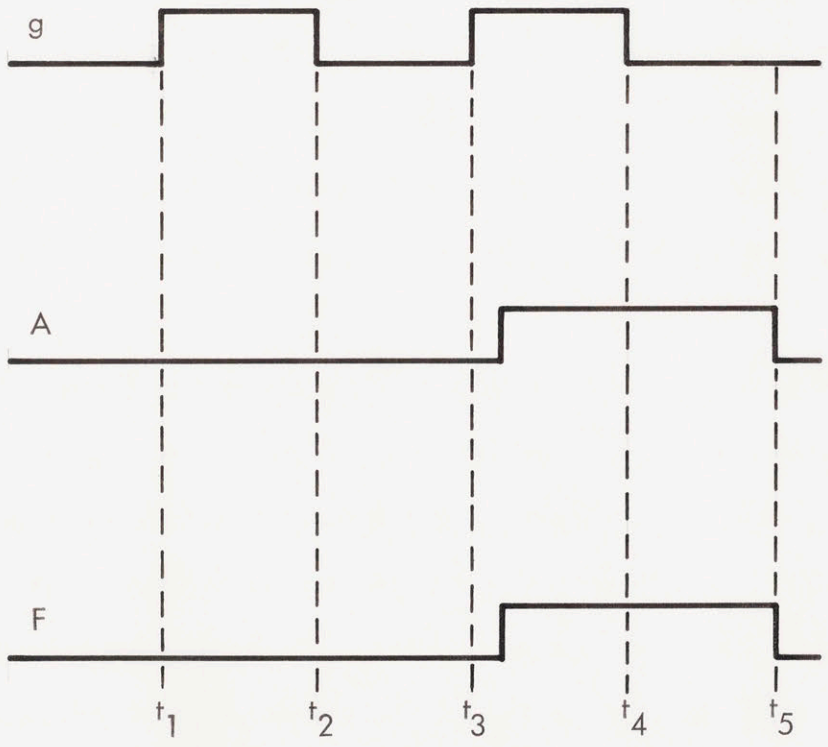


Fig. 6.6 SCR Logic Model and its Associated Timing Diagram

latter characteristic (reverse recovery current) is of considerable importance and plays an important role in selection of other circuit elements. In spite of this fact, the reverse recovery characteristic is rarely incorporated in conventional SCR models. Reverse recovery current and recovered charge are both specified, due to their strong application orientation. Specifically, where the voltage across the device must be limited by an R-C snubber network, the size of the capacitor required is determined by the SCR's recovered charge characteristics.

6.5.1 Implemented Characteristics

The previous logic model is the foundation block around which the SCR simulation model is built. Specific electrical characteristics of the SCR implemented in the 3-terminal model are:

1) Holding Current (I_H) which is analogous to the operating current of an electromechanical relay. If the anode current drops below this minimum level, the SCR reverts to the forward blocking state.

2) Reverse Recovery Characteristics. During commutation, SCR's display a transient recovery current that far exceeds the maximum blocking current. This reverse current is called the reverse recovery current, and its time integral is termed recovered charge, Q_R. After forward conduction, the reverse current in the circuit will continue to flow through the SCR, until a depletion layer has developed across the reverse blocking junction. The reverse current reaches a peak value and then starts to decay to zero. During decay, the reverse voltage increases across the cathode-anode terminals until

the full reverse blocking voltage impressed on the SCR by the circuit is achieved. This time interval is known as the reverse recovery time t_{rr}. This time, t_{rr}, depends on both the peak on-state current ($I_{F\ MAX}$) prior to commutation, and the commutation di/dt.

3) Low on Resistance and High Off Resistance. When the SCR is in the 'on state', the voltage drop across the SCR abruptly decreases to a very low value referred to as the forward on-state voltage. When the SCR is in the on-state, the forward current is limited primarily by the impedance of the external circuit. Increases in forward current are accompanied by only a slight increase in forward voltage when the SCR is in the forward conduction state. However, the dependence of forward voltage on forward current has not been included, though provision has been made for its incorporation.

A relatively high resistance is in parallel with the relay contacts. This is to supply bias current to the input comparator. (Section 6.6.3). This minimum value of bias current sets the limit on the maximum off state resistance which can be used. It turns out that this is 20 MΩ which was considered to be large, compared to the actual resistances used in the simulation circuits (typically 100Ω-100kΩ). Hence for all practical purposes the off resistance is very large and the SCR can be considered an open circuit when it is off. Though the model does not incorporate gate trigger characteristics such as turn-on delay, etc., provision has been made to incorporate them if necessary.

6.5.2 Principle of Model Operation

The thyristor model evaluates terminal conditions and makes a decision regarding the state of a reed relay. Figure 6.7 illustrates the functional block diagram of the thyristor. The relay contacts R_{1a} are in series with a current-to-voltage converter (I-V converter) which outputs a voltage v_F proportional to the input current, but with a polarity reversal. This output signal (v_F), is now transmitted to the analyzing section which determines if the holding current value of the SCR is reached. Reverse recovery current and its associated time t_{rr} is also modeled. Provision is also made to bring this signal (v_F) on to the front panel for indirect measurement of the SCR current. Each of the analog decision networks (V_{AK} evaluator, holding current detector and the reverse recovery section) have a digital filter on their output terminals for increasing noise immunity during the switching operations. The state evaluator is a specialized digital filter which determines if a specific digital signal has legally changed state, or if the state change was caused by noise. The output of the state evaluator is connected to the "A" input of the basic logic model; the output of the latter after being debounced and buffered is supplied to the relay coil.

6.6 Analog-Digital Thyristor Model: Circuit Analysis

Figure 6.7 illustrates the functional block diagram of the thyristor simulation model. To appreciate the operation of this model, each of the fundamental "decision blocks" will be analyzed, with special emphasis being on the reverse recovery section.

6.6.1 Current-to-Voltage Converter

The holding current in the thyristor model is of the order of 50 μA. This low value of holding current is determined by the current scale factor

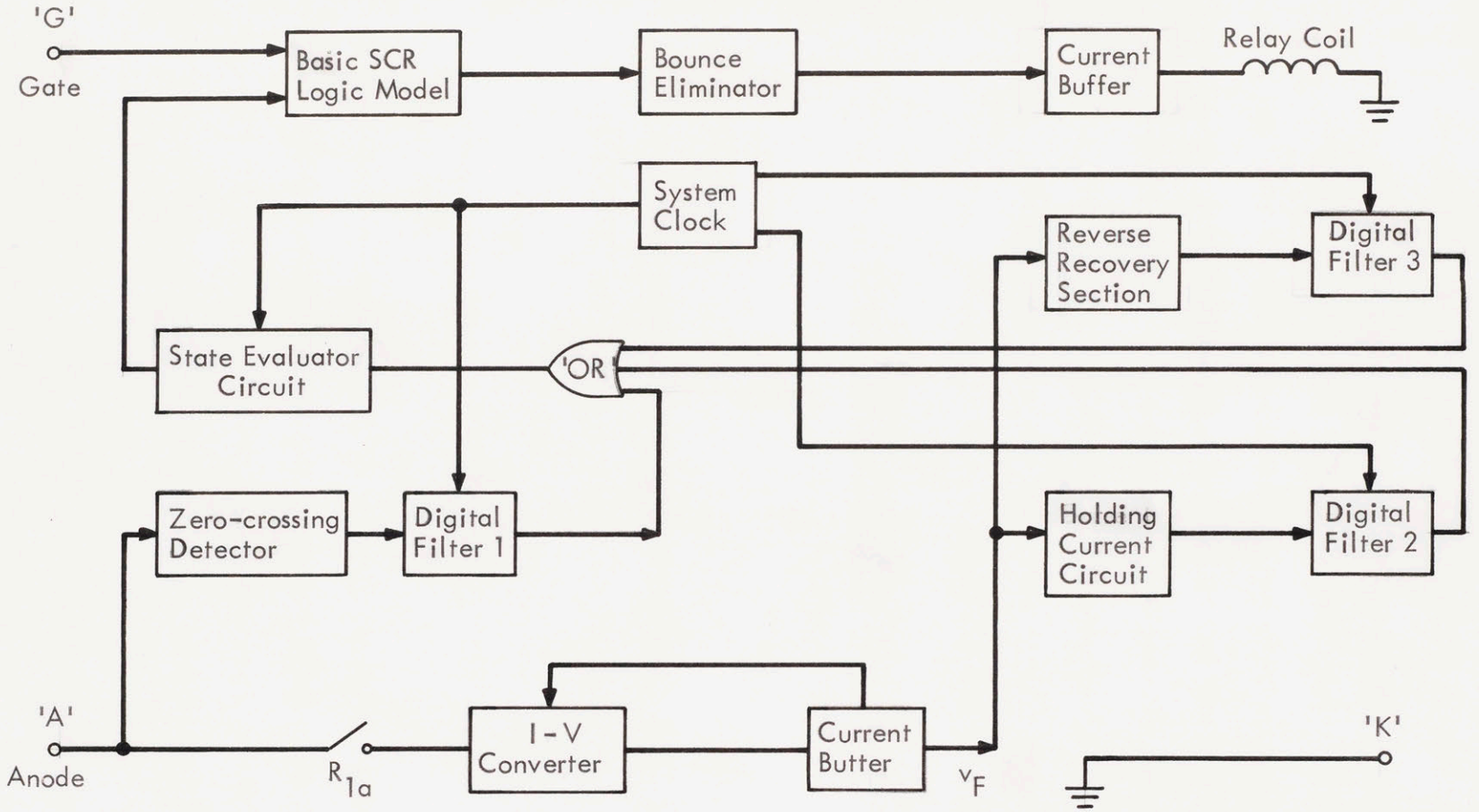


Fig. 6.7 SCR Functional Block Diagram

used in the simulation. Such small current values create a number of obvious problems - susceptibility to noise, difficulty in measurements, necessity of using high gain stages in the reverse recovery section, giving rise to serious offset problems. To minimize these problems (especially the latter), a current-to-voltage converter (also called transresistance amplifier) was used as the principal current element. This converter basically behaves as if it were a resistor with a power gain. It provides an output voltage which is proportional to the input current. The converter presents almost zero load impedance to ground, because the inverting input appears as a virtual ground. The input current, however, flows through the feedback resistor generating an output voltage

$$v = - i_F R_F \tag{6.3}$$

as shown in Fig. 6.8.

The actual impedance of the I-V converter, Z_m, taking into account the finite gain A, and differential input impedance Z_{id} is given by

$$Z_{in} = \frac{Z_{id}}{1 + (Z_{id}/R_F)(1 + A)} \approx \frac{R_F}{1 + A} \tag{6.4}$$

The lower limit on measurement of current input is determined by the offset voltages and bias currents of the inverting input. To minimize the latter error, the FET input RCA CA 3140 op-amp was used, which has bias currents of 30 pA, small enough to be neglected (as compared to 50 μA). The offset voltage is of the order of 2 mV, hence from Eq. (6.3) with R_F = 100Ω a forward current of 50 μA is the minimum which can be accurately measured. Figure 6.8 shows the voltage-to-current converter with a current booster,

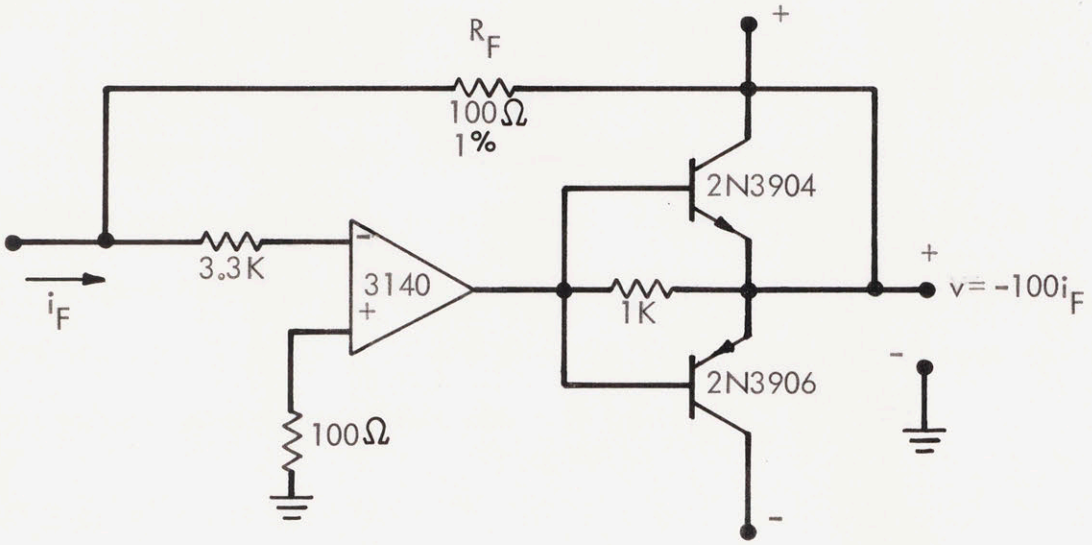
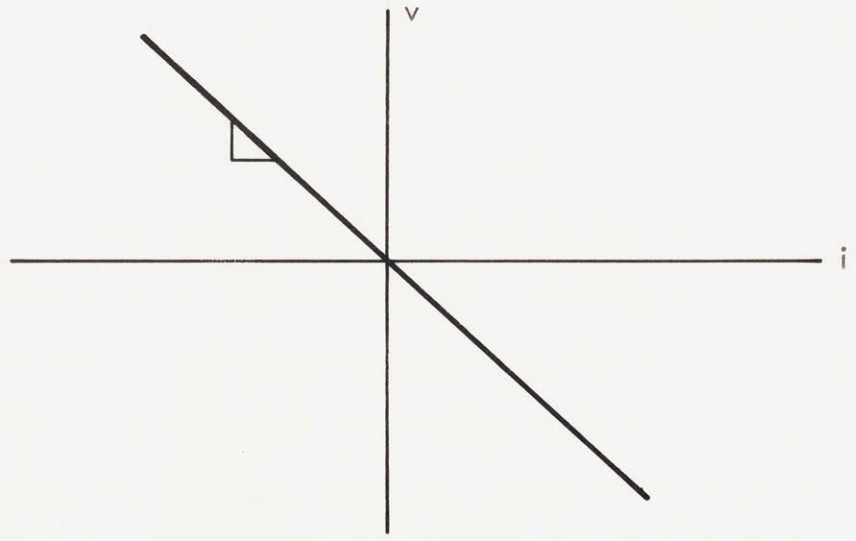


Fig. 6.8 Current-to-Voltage Converter



Transfer Function of the Current-to-Voltage Converter

for operating at higher current levels. The 3.3 kΩ protection resistor is to limit the input current during a step change in the incoming signal. This prevents the possibility of extremely large input signal transients from forcing a signal through the input protection network and thus adversely affacting the constant current source internal to the op-amp.

As mentioned before, the circuit is characterized by almost zero input resistance. Using Eq. (6.4), with R_F = 100Ω and A = 4500 at the maximum frequency of 1 kHz, Z_{in} = 0.022Ω which is very small compared to the typical values used in the simulation (100Ω-100kΩ).

6.6.2 Current Booster

Most operational amplifiers lack the output current capability needed for many common applications, and a variety of circuits have been developed to boost the current to acceptable levels.

Complementary emitter followers provide the simplest bipoler current boosting for an operational amplifier. The current booster used in the SCR model has basically class B bias; so there is no quiescent drain from the booster. However, the circuit is connected for continuous supply of output current through the zero crossing as shown in Fig. 6.8. Near the output zero crossing, both transistors are off, but output current continues to be supplied through R_1 from the operational amplifier. No current boosting is then available, but it is not required as the voltage is small. As the output moves away from its zero crossing, load current is drawn through R_1 whose voltage gradually turns on one of the transistors to provide additional output current. The maximum output current in the thyristor current booster is 150 mA, using the complimentary transistor pair - 2N3904 and 2N3906. The 100Ω precision resistor (R_F) provides the necessary feedback path for the

input current.

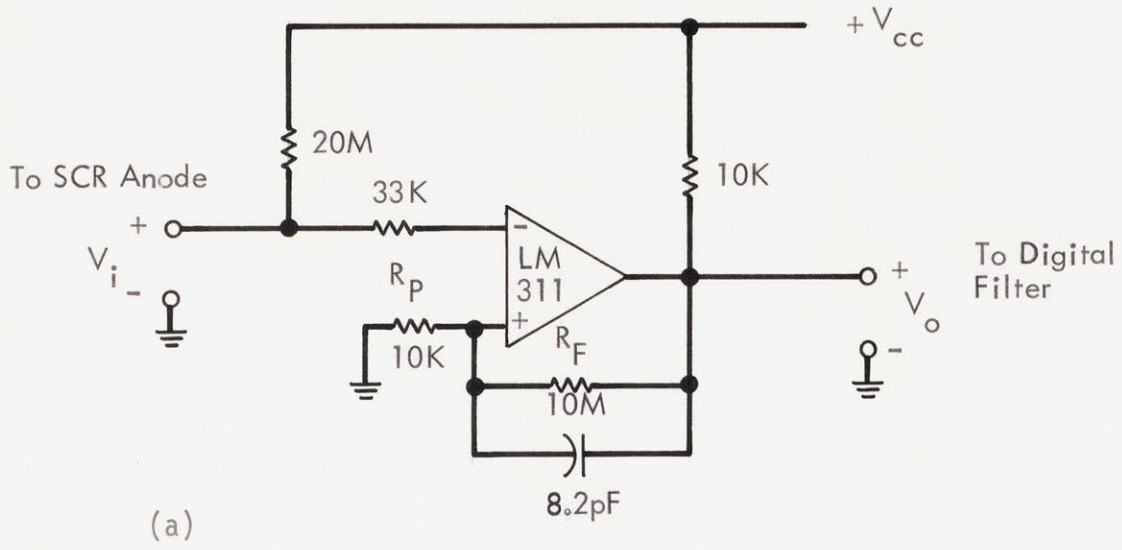
6.6.3 Zero-crossing Detector

For a simple switch to act as a thyristor, it has to possess a number of attributes, one of them being that the switch closure can occur only for positive voltages on the simulated device. The block diagram (Fig. 6.7) illustrates this decision module as the "V_{AK} Evaluator". Here, it is necessary to convert analog signals into bilevel signals. This is done by comparing an input signal with a reference voltage being, in this particular case, the cathode voltage. Whenever the signal changes from less than the reference to greater than the reference (or vice versa), the output voltage of the comparator abruptly changes state. Figure 6.9(a) shows the inverting zero-crossing detector and Fig. 6.9(b) illustrates its transfer function. Hysteresis is provided by R_F and R_p. The window width of the hysteresis loop is given by

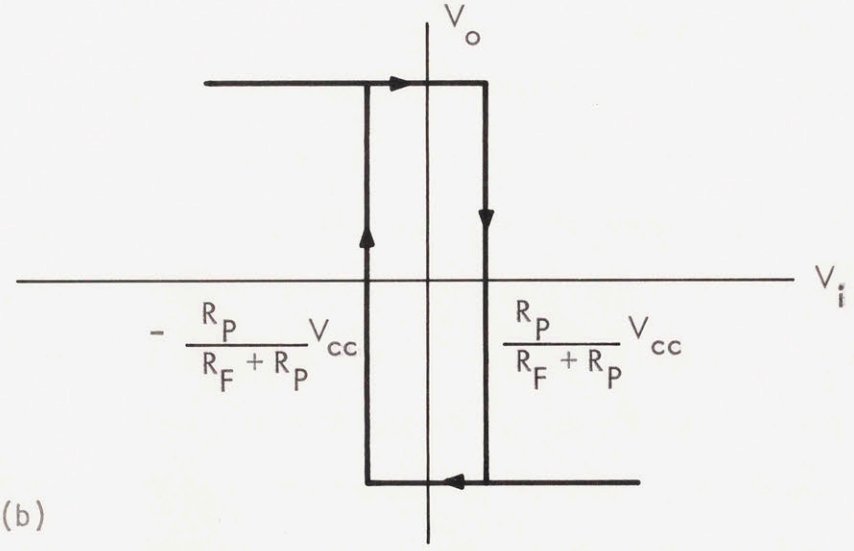
$$v_i = \frac{R_p}{R_p + R_f} \cdot V_{cc} \qquad (6.5)$$

where V_{cc} is the supply voltage.

The hysteresis circuit therefore provides noise immunity and prevents the output from oscillating during transitions. The window width for the thyristor model zero-crossing detector is obtained from Eq. (6.5) by substituting values of 10 kΩ, 10 MΩ and 15 V for R_p, R_f and V_{cc} respectively. This allows a window width of 15 mV, which is adequate for providing noise immunity and for preventing oscillations during the switching operation. As the comparator is CMOS compatible, the output is directly connected to the CMOS digital filter. A 20 MΩ resistor is connected to the inverting input solely for



(a)



(b)

Fig. 6.9 Zero Crossing Detector (a) and its Transfer Function (b)

providing bias current to the LM 311 comparator. The absence of bias current may, in certain circuit connections, cause the comparator to saturate.

6.6.4 Reverse Recovery Circuit

When a thyristor is in the forward conduction mode, charge Q is stored in the base region; this charge is a function of the forward current I_F. When the thyristor is turned off, a certain amount of this stored charge is recovered as reverse anode current. The magnitude of this recovered charge Q_R is dependent on the initial charge stored, the minority carrier life-time τ_b in the base region, and the circuit limited rate of fall of the initially high anode current $(\frac{di_R}{dt})$. Figure 6.10 illustrates the practical circuit which models the reverse recovery current dynamics. Op-Amp A_1 is the voltage-to-charge amplifier. This converts a change of voltage to a transfer of charge on capacitor C_1. The minority carrier life-time τ_b is modeled by potentiometer P_1 through which the charge on C_1 is allowed to decay. Amplifier A_2 is connected as a differentiator which models the circuit limited rate of fall of the forward current. The differentiator has a small signal transistor in its (op-amp A_2's) feedback loop. The transistor (2N3904) is connected in the reverse breakdown mode, to prevent saturation of A_2. The input signal v is obtained from the current-to-voltage converter (Section 7.6.1) which delivers an output voltage linearly dependent on the forward current i_F. The outputs of A_1 and A_2 are compared by a high speed comparator (LM311). The comparator output is low as long as the differentiator voltage is greater than the charge amplifier's output. During this variable length of time the digital filter output is high, allowing the reverse current to flow, changing state only when the charge on C_1 has decayed to where $v_{a_2} = v_{c_1}$.

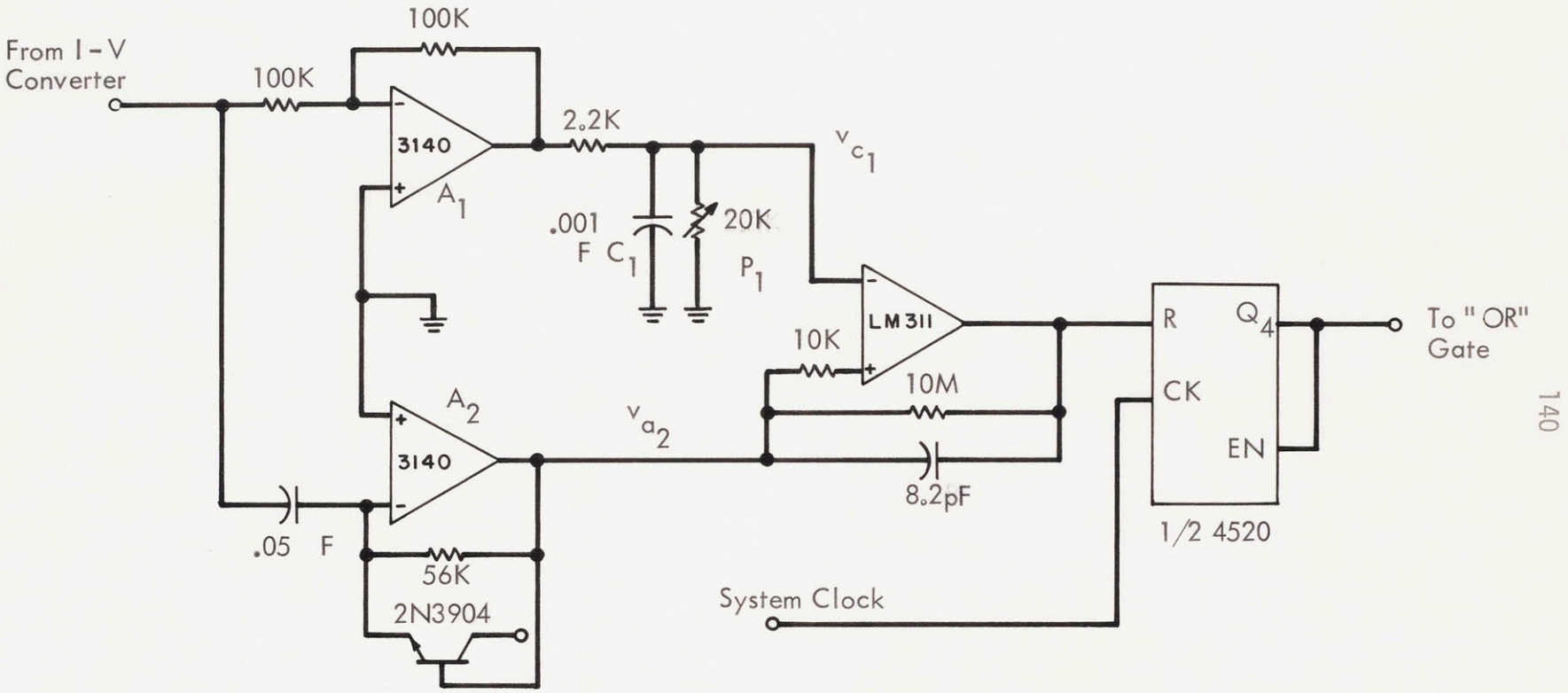


Fig. 6.10 Reverse Recovery Circuit

6.6.5 Holding Current Simulation

After a thyristor has been switched to the on-state condition a certain minimum value of anode current is required to maintain the thyristor in this low-impedance state. This minimum principal current is known as the holding current I_H. To model this parameter, a comparator circuit similar to the Zero-crossing detector of Section 6.6.3 is used, the only difference being that the detector is non-inverting. The hysteresis level sets the comparator trip point and consequently the holding current value. Figure 6.11 shows the holding current circuit, and for the values shown, the hysteresis value is 5 mV. From Eq. (6.3) this voltage corresponds to a forward current of 50 μA - the holding current of the device.

6.6.6 Digital Filtering

Basically, an active filter is a device that passes signals of a certain frequency and rejects those of other frequencies. The frequencies that pass constitute the pass band and those that are attenuated make up the stop bands. Most complex circuits, whether analog or digital, use filters to attenuate the undesired frequencies. Though analog "Active Filters" are more commonly used, the SCR simulation model utilizes digital filters since they are smaller, require fewer components, and yet perform their function as well as, or even better than, their analog counterparts.

As illustrated in Fig. 6.12(a), the digital filter is basically a binary up counter (CD 4520) driven by a system clock. The counter consists of an internally synchronous 4-state counter. The counter stages are D-type flip-flops and are incremented on the positive going transition. The counters are cleared by high levels on their reset lines. A CMOS compatible output obtained from one of the 3 comparators is fed into the reset terminal

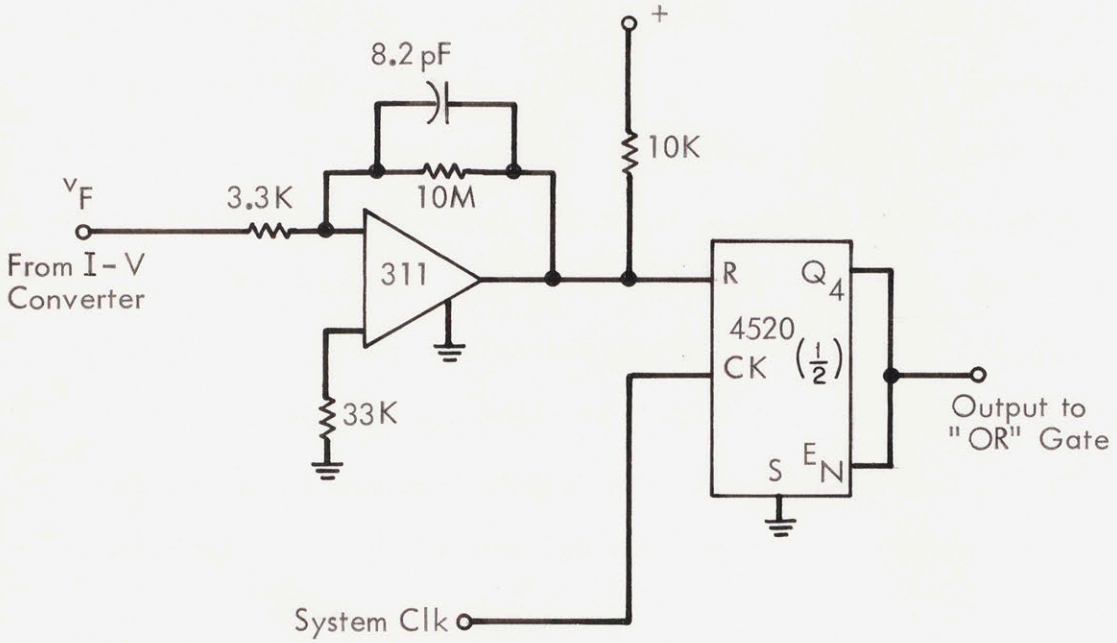
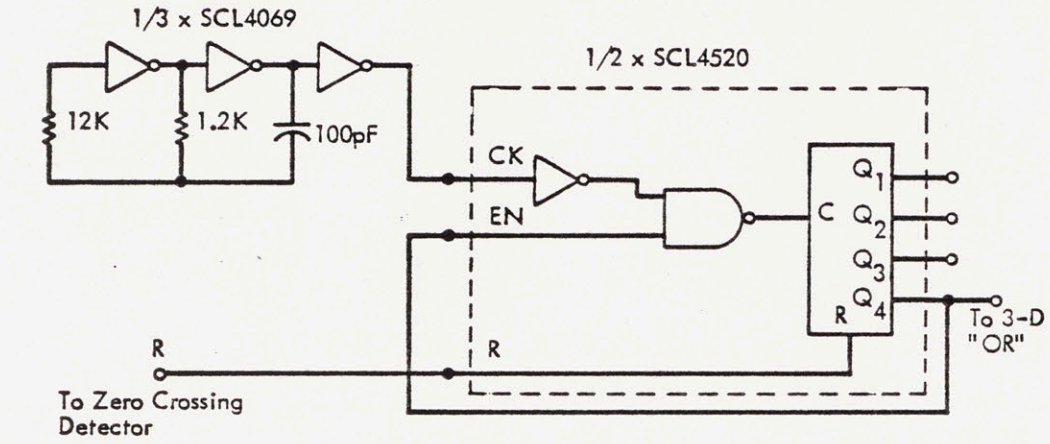


Fig. 6.11 Holding Current Circuit

of the counter, the output being obtained on Q_4. Q_4 is also fed back to the 'enable' input, which can disable the counter if it (enable) goes high. Figure 6.12(b) shows the timing diagram of the digital filter and is useful in visualizing how the circuit operates. When the reset goes low, the counter starts advancing one step in binary order, on the positive-going transitions of the clock. Q_1, Q_2, Q_3 and Q_4 are divide-by-N buffered outputs where N = 2, 4, 8, and 16 respectively. On the arrival of a pulse on Q_4, the counter is disabled and the output remains high, until initialized by a 'high' on the reset terminal. For Q_4 to go 'high' the reset should be low for at least 8 clock pulses. Hence a noise spike less than 8 clock pulses wide is digitally filtered out. Each thyristor model uses three such digital filters, one at each comparator output of the holding current circuit, reverse recovery circuit, and the zero-crossing detector circuit.

6.6.7 State Evaluator Circuit

The inherent noise in a circuit is generated internally by resistors and opamps, and externally by switching of inductive loads, 60 Hz interference, etc. The generated noise is random and has a variety of spectral characteristics depending on the active elements used in the circuit, coupling between adjoining lines, switching speed, etc. The bandwidth of a closed loop amplifier determines the amount of noise transmitted to the next stage - the greater the closed loop bandwidth, the greater will be the noise. To reduce such noise in digital circuits, special filtering techniques have to be used. Section 7.6.6 discussed a binary counter type digital filter. This section discusses a special type of digital filter which determines if a specific digital signal has legally changed state, or if the state change was caused by noise.



(a)

(b)

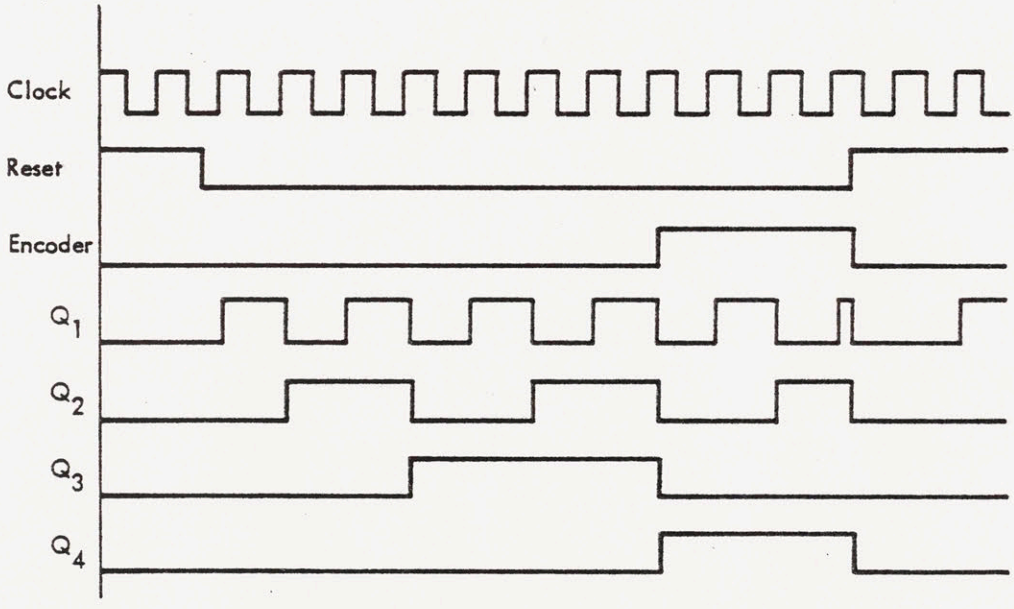


Fig. 6.12 'Low-pass' Digital Filter (a) and its Timing Diagram (b)

As shown in Fig. 6.13(a) the state evaluator consists of two identical, independent, four stage, serial-input parallel-output shift registers. Each register has independent clock (CK) and reset (R) inputs as well as a single data input (D) which is tied high. All register stages are D-type master-slave flip-flops. The logic level present at the data input is transferred into the first register stage and shifted over one stage at each positive going clock transition. The outputs Q_1, Q_2, Q_3 and Q_4 of each shift register are connected to a quad input AND gate (CD4082) whose output is transmitted to the J, K inputs of a J K flip-flop. Synchronism is achieved by operating the entire network from the system clock.

From the timing diagram of the state evaluator (Fig. 6.13(b), it is evident that the output $\bar{Q}$ of the J-K flip-flop is delayed from the input waveform (at reset R') by five clock pulses. Hence the circuit operates as a digital delay, delaying a change of state by five clock pulses.

During this delay period, the reset R' maintains its previous state. Arrival of a noise pulse (less than five clock pulses wide), would change the reset (R') state; however, for the input signal to filter through, five clock pulses are required. If the duration of the noise pulse is less than this interval (5 clock pulses), the circuit assumes that the reset (R') was influenced by noise and so the output $\bar{Q}$ remains in its original state.

Because of internal circuit construction, there is no guarantee as to what d.c. level will be present on the output at Q when power is first turned on. Since the condition Q = 0 must be guaranteed, a system-power on pulse input to reset R of the J-K flip-flop can be made to assure that Q will be at a low logic level. The pulse is generated by the R_1C_1 circuit in Fig. 6.13(a).

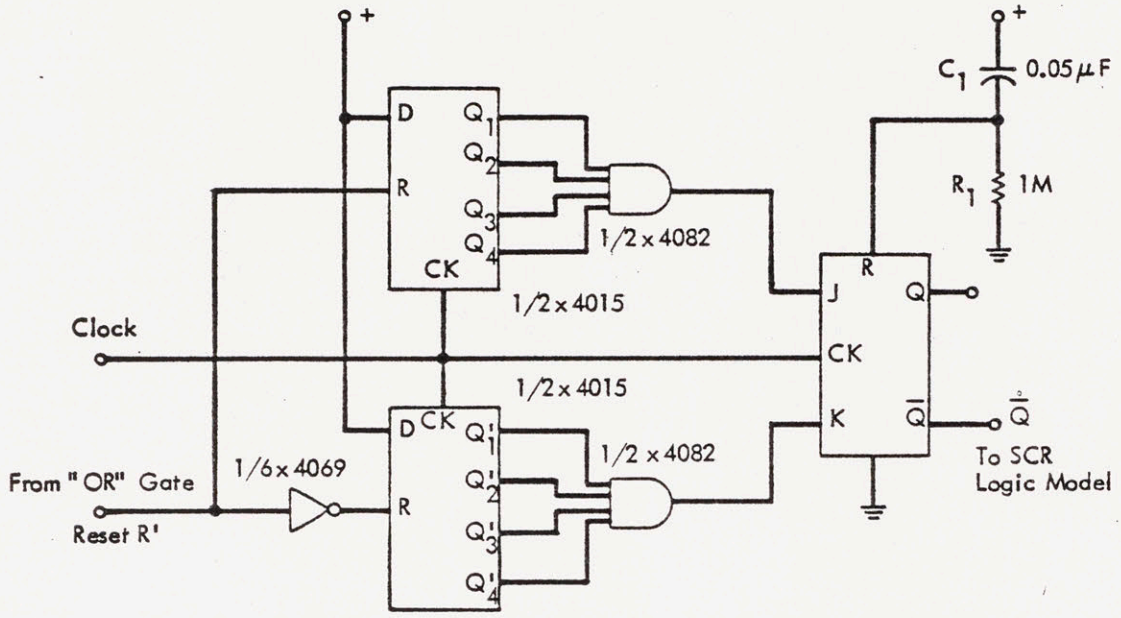


Fig. 6.13(a) State Evaluator Circuit

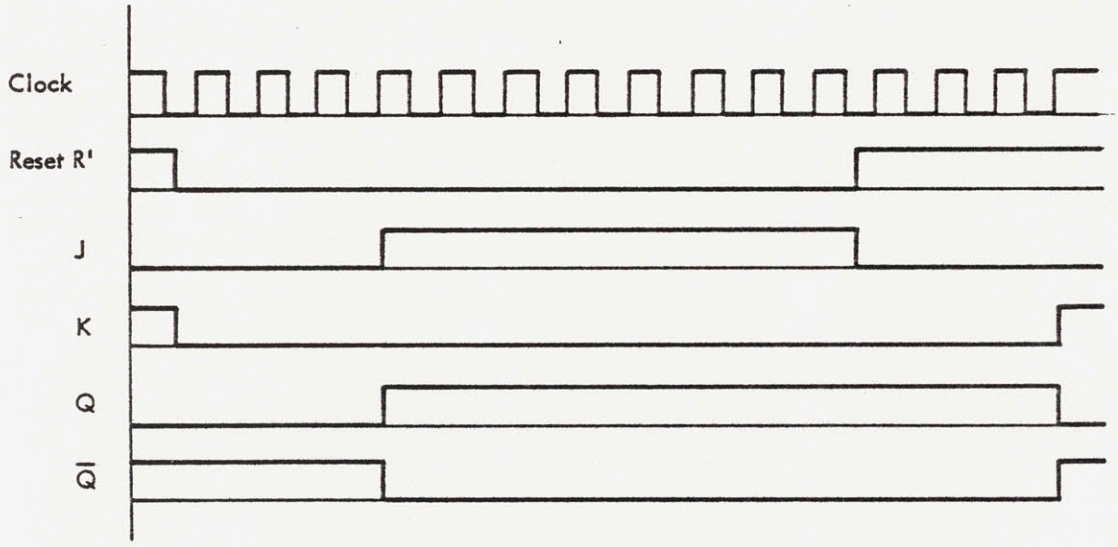


Fig. 6.13(b) Timing Diagram of the State Evaluator Circuit

6.6.8 Bounce Eliminator Circuit

Monostables are often used as bounce eliminators for electromechanical relays. Contact bounce is a transient phenomena that occurs when the movable contact repeatedly strikes and bounces off one of the fixed contacts. This happens each time the switch is thrown and may last for several milliseconds. This is undesirable for the simulated thyristor module, and unreliable operation may result due to the random number of "bounce transitions".

Figure 6.14 shows the digital bounce eliminator circuit. This is used with a SPDT reed relay. The bounce eliminator circuit is built around a CD4528 monstable multi-vibrator which has stable, resettable one-shot operation for any fixed voltage timing application. An external resistor R and an external capacitor C control the timing for the circuit. Basically the circuit delivers a pulse of a certain minimum length on the rising and falling edge of the input pulse.

6.6.9 Switching Element

Thyristors are basically solid-state devices that have characteristics similar to an electromechanical switch. A theoretically perfect switch is a device which has no power loss when used for the purpose of interrupting current through a load and one which can change its state, say from the on to the off condition, in zero time. This simple definition has far-reaching implications. It requires that in the closed position the switch must have no voltage drop across its terminals. In the open position, the switch must cut off all current flow through the load, and finally, the repetitive cycling speed must be infinite, corresponding to zero time delay between one switch setting and the other. The perfect switch, of course, can never be implemented; however, switching devices closely approaching the ideal are on the market. Transistors represent the best available components for switching

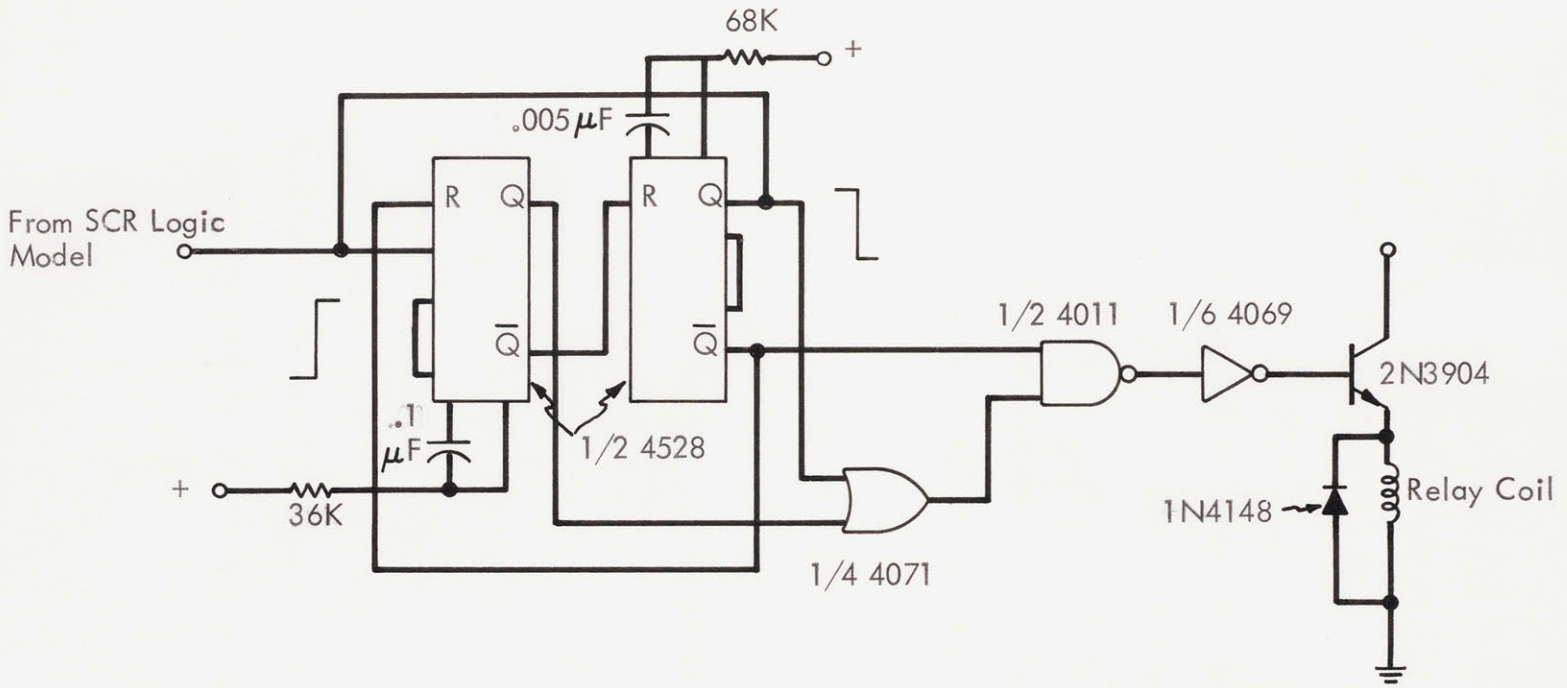


Fig. 6.14 Debouncing Circuit

applications, especially in high-speed equipment. Field-effect transistors (F.E.T.'s), while they approach the ideal in the off position, and can operate at relatively high repetition rates, are severely limited by a high voltage drop in the on-condition. This loss limits the usefulness of these devices in the SCR model application. As low forward drop is the crucial issue in the SCR model, the optimum switching element is the reed relay.

Reed relays are constructed of two magnetic members plated with special metals to form switch contacts. These contacts are protected by a glass enclosure and a dry inert gas atmosphere, making this relay an extremely sensitive magnetic device with high quality and reliability. Certain parameters of the thyristor model are specified by the reed relay considerations. For example, the "operate time" of the reed relay gives the model SCR its corresponding "turn-on" delay. The maximum repetition rate determined the upper limit of the model SCR's switching speed. For the relay under consideration, the maximum switching speed is approximately 1 kHz.

The necessary drive for the relay is obtained from a Darlington transistor (MJE 802), used in the common collector configuration. This transistor amplifier configuration, although not producing a voltage gain, produces a current gain of magnitude β_F, where β_F is the short-circuit common emitter current gain. The output drive is now capable of operating the reed relay. A free-wheeling diode is placed across the relay as a protection device, to prevent excessive switching transients from destroying the transistor.

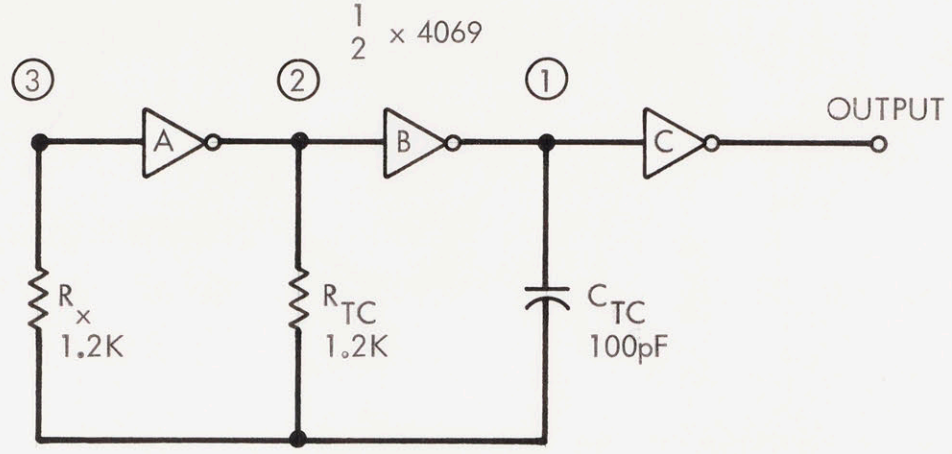
6.6.10 System Clock

The system clock is the basic timing unit for any synchronous circuit. The system clock must provide a periodic waveform which can be used as a

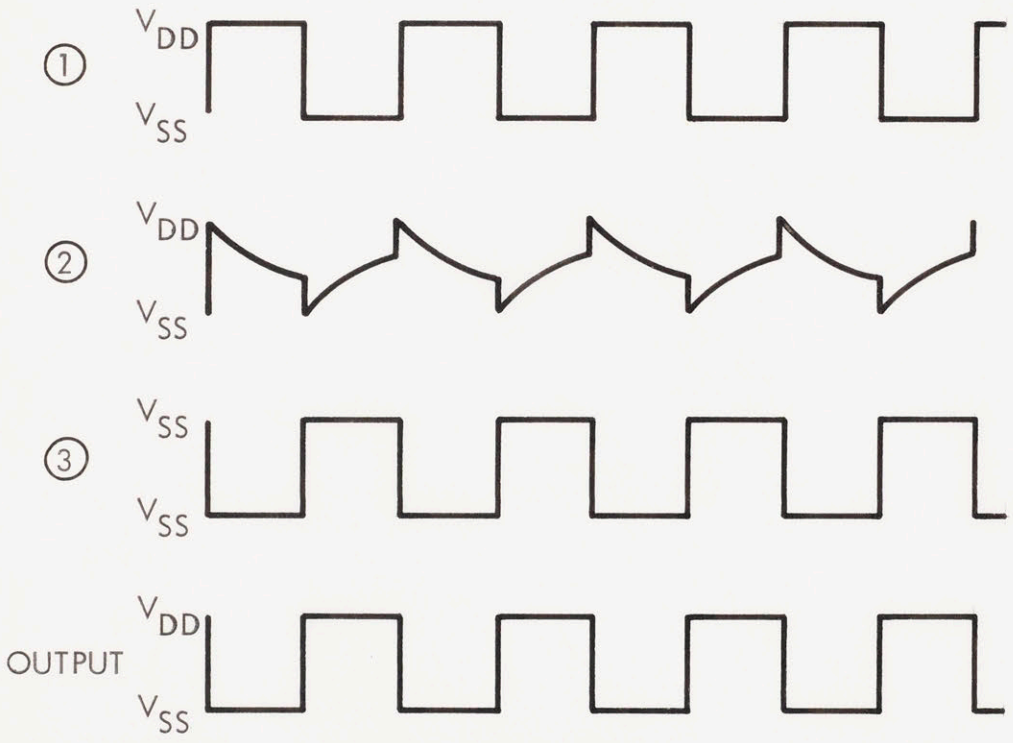
synchronizing signal. A square wave is used as a clock waveform in most digital systems; the main requirement being simply that it be perfectly periodic. Figure 6.15(a) shows an astable multivibrator which uses 3 COS/MOS inverters and Fig. 6.15(b) shows the related waveforms. This simple circuit requires only two resistors and one capacitor and operates in the following manner. When the waveform 1 at the output of inverter B is in a high or "1" state capacitor C_{tc} becomes charged positive. As a result, the input to inverter A is high and its output is low or "zero". Resistor R_{tc} is returned to the output of inverter A to provide a path to ground for discharge of capacitor C_{tc}. As long as the output of A is low, the output of inverter B is high. As capacitor C_{tc} discharges, however, the voltage generated in waveform 2 approaches and passes through the transfer voltage point of inverter A. At the instant that this crossover occurs, the output of A becomes high; as a result the output of B becomes low and the capacitor C_{tc} is charged negative. The resistor R_{tc} connected to the output of A then provides a charge path to a supply voltage. Capacitor C_{tc} begins to charge to this voltage, and again the voltage approaches and passes through the transfer voltage point of inverter A. At that instant, the circuit again changes state and the cycle repeats. Inverter C is used as an inverting buffer to prevent loading of capacitor C_{tc}.

The oscillator is made independent of supply voltage variations by use of a large resistor in series with the input load to inverter A. This resistor should be at least twice as large as resistor R_{tc} to minimize frequency dependence on supply voltage. The time period τ for one cycle can be computed by the following equation:

$$\tau = 2.2\ R_{tc}\ C_{tc}$$



(a)



(b)

Fig. 6.15 Circuit Diagram (a) and Voltage Waveforms (b) for the Astable Multivibrator

For the desired period of 1.4 μsec the values of C_{tc} and R_{tc} come to be 100 pF and 1.2 KΩ respectively.

6.7 Electrical Characteristics of the Simulated SCR

These specifications apply for $V_s = \pm 15V$ and $T_A = 25°C$ unless otherwise specified.

Table 6.4

Parameter	Symbol	Value	Units
Instantaneous On-state Voltage (offset voltage of V-I converter)	v_T	6	mV
Maximum On-state Current	$I_{T\ (0\text{-}Peak)}$	120	mA
Instantaneous Holding Current (gate open)	I_{HO}	40	μA
Turn-on Time	t_{on}	0.4	msec
Maximum Switching Speed	f_s	1.0	kHz

Figure 6.16 illustrates the completed SCR model and Fig. 6.17 shows the model SCR on a PC board.

6.8 Experimental Results

With the described SCR model, the significant electrical design parameters were accurately determined and recorded. Among the measured

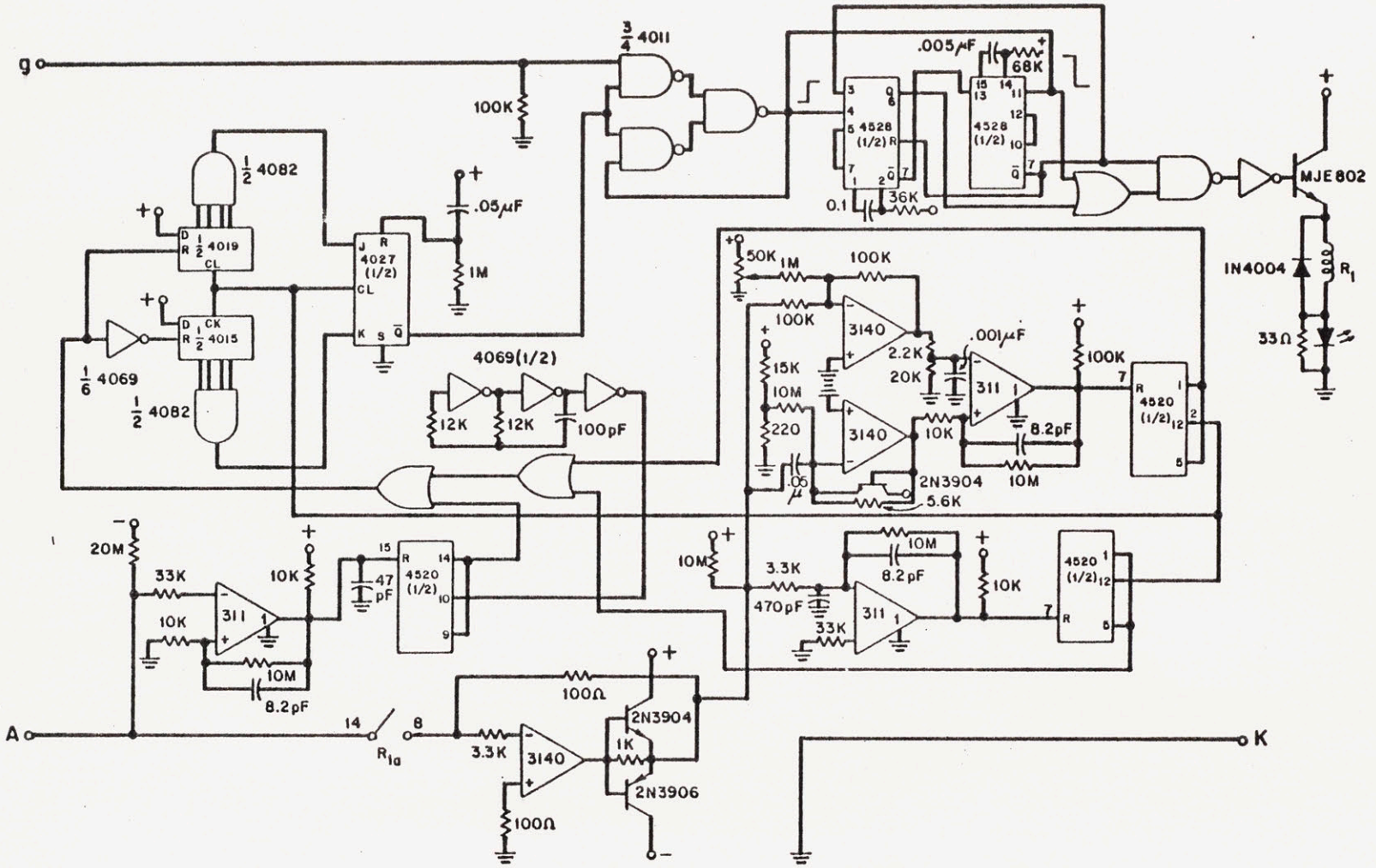


Fig. 6.16 Analog-Digital SCR Model

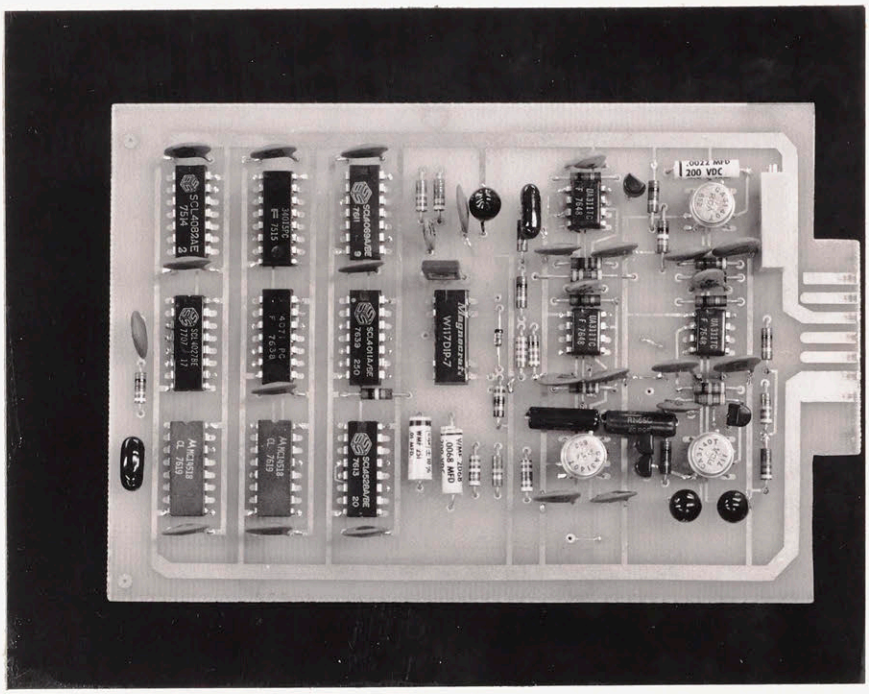


Fig. 6.17 Analog-Digital SCR Model on a PC Board

quantities are:

1. Peak thyristor current and peak inverse voltages.
2. Reverse recovery current
3. Holding current

These quantities were measured under various load conditions and various operating frequencies.

6.8.1 Test Results and Waveforms

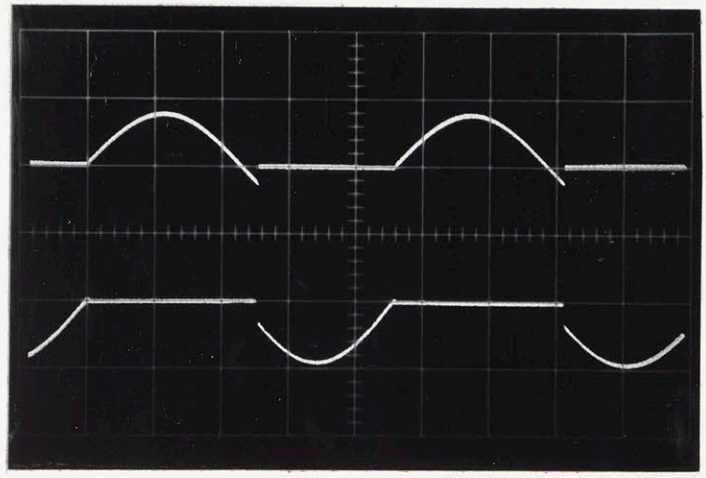
1. Current and voltage waveforms

Figure 6.18(a) and 6.18(b) illustrate the current and voltage variables of the SCR. The effect of the reverse recovery current on the voltage variable is clearly noticeable. This effect of creating large values of dV/dt is of special significance in circuits where it is imposed in the forward direction across some device elsewhere in the network. Clearly this maximum dV/dt is imposed when the SCR just turns off. Figure 6.18(c) shows the test circuit used for the measurement.

2. Reverse recovery characteristics

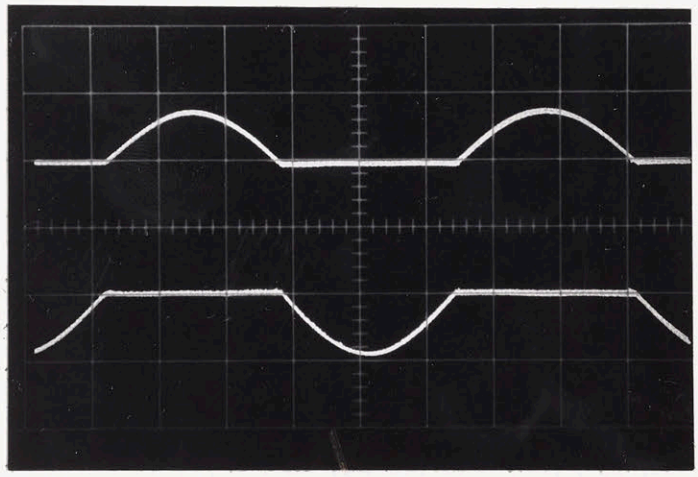
Figure 6.19(a), 6.19(b) and 6.19(c) clearly illustrate the effects of peak forward current variations and circuit limited rate of fall of the initially high anode current (di/dt) on the reverse recovery current of the device. In Fig. 6.19(b) the reverse recovery current of the device is much higher than either (a) or (c) clearly verifying that reverse current I_R is a strong function of the peak forward current and the circuit limited di/dt.

Figure 6.20 illustrates an expanded view of the reverse recovery current of the device. To obtain a more meaningful output, graphical measurements of recovered charge were made for different values of reverse



Time (2 msec/div)

(a)



Time (50 msec/div)

(b)

Fig. 6.18 SCR Current and Voltage Variables

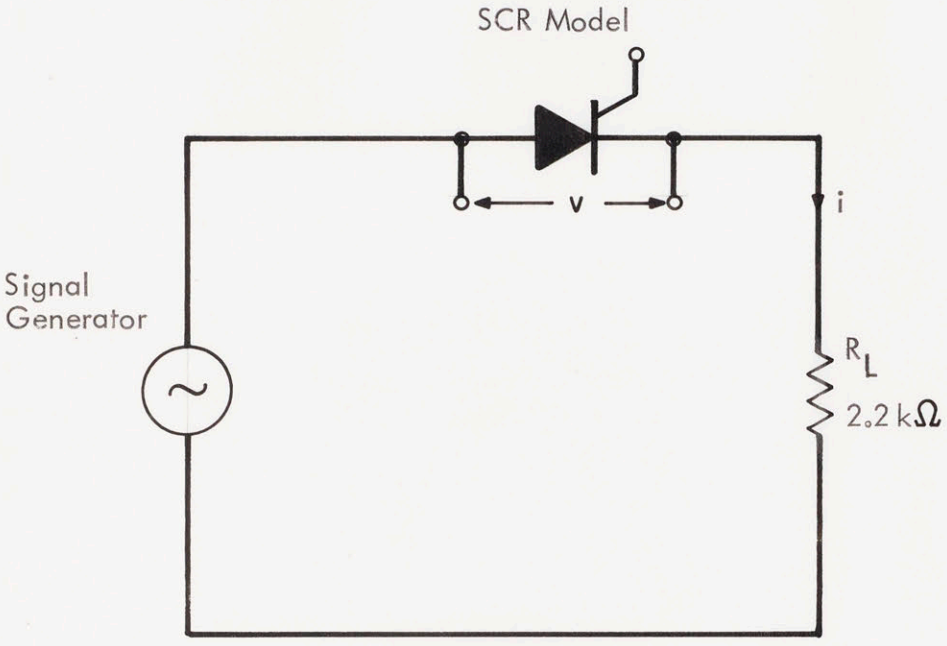
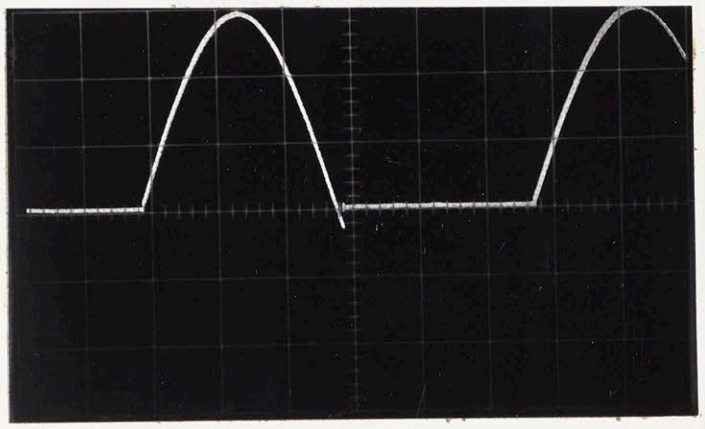


Fig. 6.18(c) Test Circuit for the Measurement of Current and Voltage Variables

SCR Current
(2.5 mA/div)

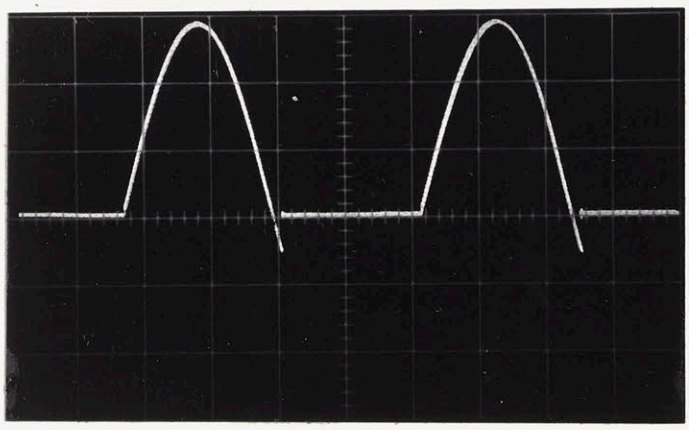


$\frac{di}{dt}$ = 1.2 mA/msec

(a)

Time (2.0 msec/div)

SCR Current
(2.5 mA/div)

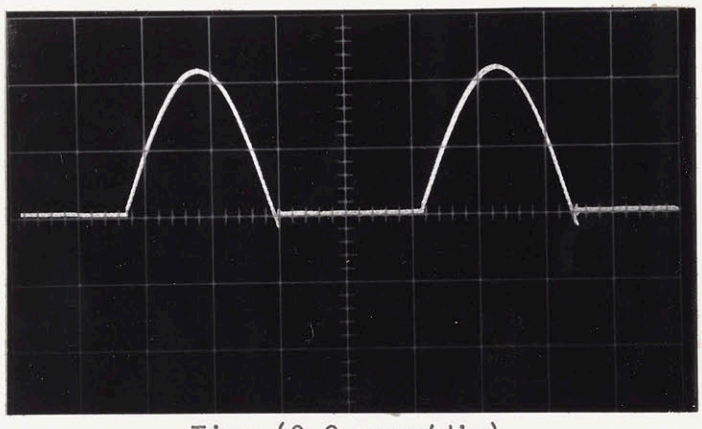


$\frac{di}{dt}$ = 2.5 mA/msec

(b)

Time (1.0 msec/div)

SCR Current
(0.5 mA/div)



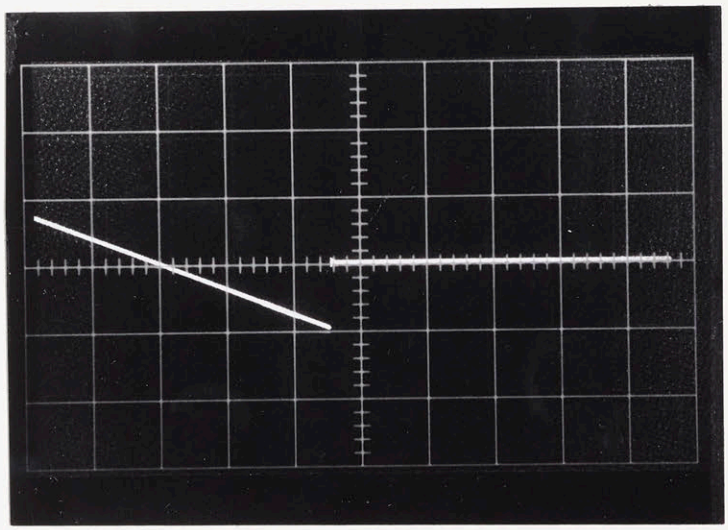
$\frac{di}{dt}$ = 2.5 mA/msec

(c)

Time (0.2 msec/div)

Fig. 6.19 Reverse Recovery Characteristics

SCR Current
(2 mA/div)



Time (0.5 msec/div)

Fig. 6.20 Reverse Recovery Current

di/dt applied. Figure 6.21 shows the recovered charge data for the model, and for a typical SCR.

3. Holding current

Figure 6.22 illustrates the thyristor holding current. At the discontinuity in the waveform, the forward device current is less than the holding current and consequently the thyristor turns off resulting in the "break" in the forward current trace. Clearly the holding current is extremely small (40 μA), and to achieve a "clean" (noise free) waveform an I-V converter (Section 7.6.1) which is a low impedance circuit is used in the model. This is because the gain of the I-V converter for DC noise voltage is approximately unity, whereas the gain for DC current is 100, giving a signal-to-noise ratio of 100.

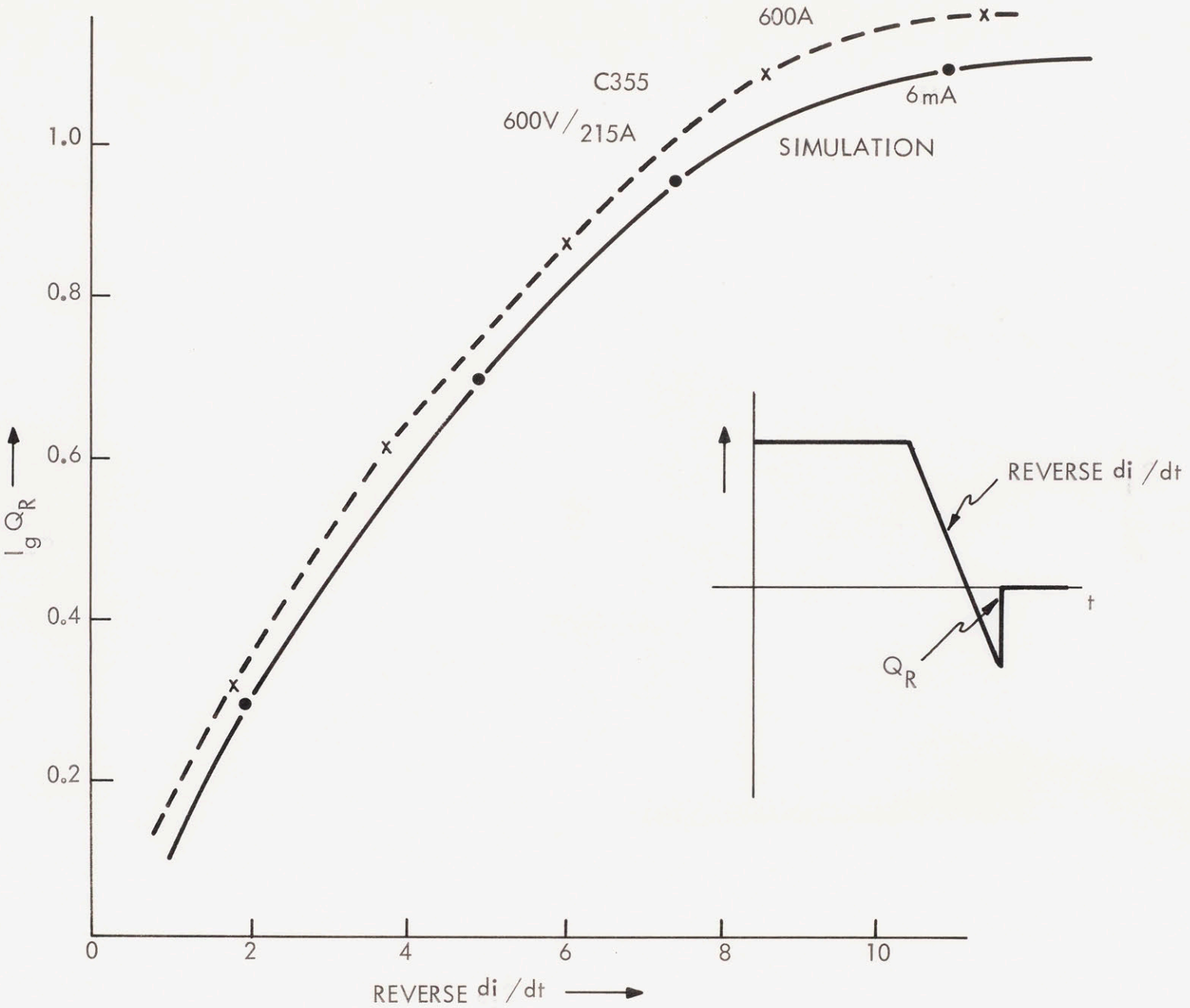
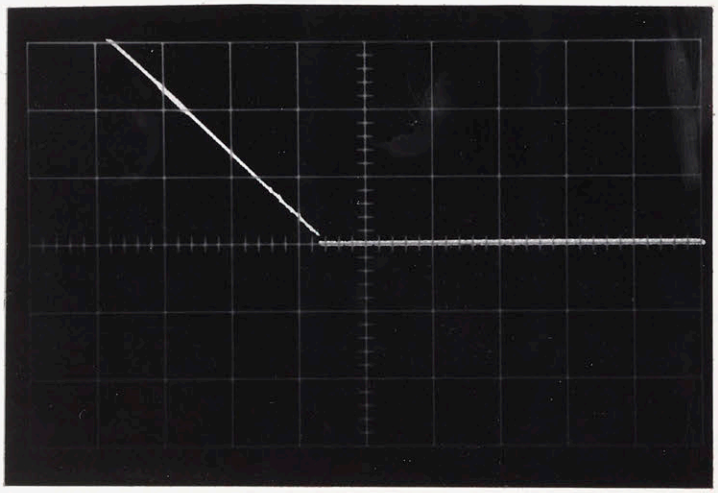


Fig. 6.21 Recovered Charge Data

SCR Current
(200 μA/div)

(I_H = 40 μA)



Time (100 msec/div)

Fig. 6.22 Holding Current Waveform

CHAPTER 7

EXPERIMENTAL VERIFICATION

Parity Simulation technique employs a high degree of correspondence between the topology of the model and the topology of the actual system. The existence of such a topological isomorphism allows a true "bread-board" approach to simulation. Three circuits have been used to illustrate the concept of Parity Simulation.

1) A Parallel RLC Ringing Circuit
2) Current Commutated Chopper
3) 10 kHz Series Inverter

These are dealt with at length in the succeeding sections.

7.1 "Q" of a Simulated RLC Circuit

Series and parallel RLC circuits are relatively common in electronics owing to their frequency selective properties. They are band pass or band-rejection networks which pass or reject signals in a relatively narrow band of frequencies.

For the parallel resonant circuit of Fig. 7.1.1, the system function can be written in the form:

$$H_{(s)} = \frac{V_2}{V_1} = \frac{Ls}{LCs^2 + \frac{L}{R}s + 1} \qquad (7.1.1)$$

From the system function of Eq. (7.1.1) the quality factor Q can be expressed simply in terms of C, L and R.

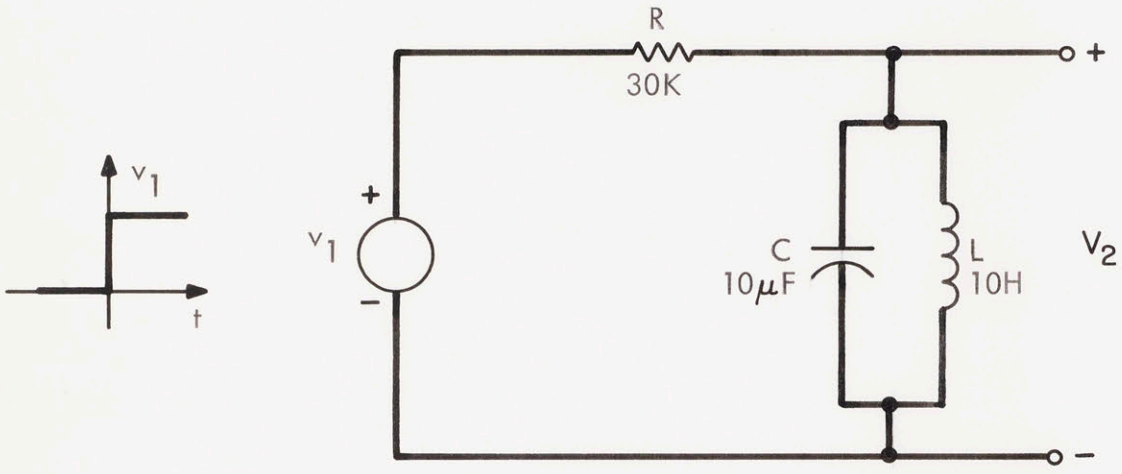


Fig. 7.1.1(a) Parallel Resonant RLC Circuit

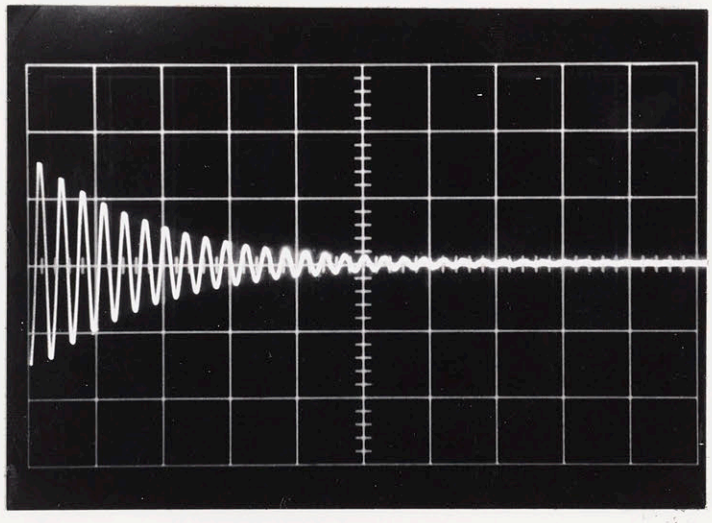


Fig. 7.1.1(b) Response of the Simulated Parallel RLC Circuit

$$Q = R\sqrt{\frac{C}{L}} \qquad (7.1.2)$$

Figure 7.1.1(a) illustrates the test circuit used to determine the step response of the simulated RLC circuit. Both energy storage elements have been simulated in the network. Implementing Eq. (7.1.2) in the circuit of Fig. 7.1.1(a) gives the value of the quality factor Q.

$$Q = 30K\sqrt{\frac{10\mu}{10}} = 30 \qquad (7.1.3)$$

Figure 7.1.1(b) illustrates the response of the simulated RLC circuit. The circuit oscillates for at least 25 cycles indicating a minimum of damping. The number of oscillatory cycles also gives a measure of the overall Q of the circuit. The value of the Q obtained from the exponential decay of the envelope in Fig. 7.1.1(b) can be expressed as:

$$Q = [\text{no. of cycles whose amplitude} \geq \frac{1}{e} \cdot V_m] \qquad (7.1.4)$$

where V_m is the peak amplitude of the first cycle. As the legitimate number of cycles in Fig. 7.1.1(b) is 10, Q turns out to be 31.4, which agrees remarkably well with the calculated value of Q in Eq. (7.1.3)

From Eq. (7.1.1), the ringing frequency f_c can be obtained as:

$$f_c = \frac{1}{2\pi\sqrt{LC}} \qquad (7.1.5)$$

and for the values given in Fig. 7.1.1(a) f_c is calculated to be 15.9 Hz. From Fig. 7.1.1(b) f_c is found to be 15 Hz which indicates good correlation between simulated and calculated values.

7.2 Simulation of a Current Commutated Chopper

A current commutated thyristor chopper is used to illustrate the concept of Parity Simulation. Results of the Parity Simulation are discussed along with a brief theoretical analysis of the current commutated chopper, and illustrations of the various circuit variables.

7.2.1 Function of DC Choppers

DC-dc converters basically consist of some kind of a chopper which is used to vary the average DC voltage applied across the load circuit. The average voltage is varied by alternate on and off switching so as to permit a train of constant voltage pulses to be delivered to the load circuit. The magnitude of the average load voltage can be altered by 1) frequency modulation, 2) pulse width modulation 3) Combination of frequency and pulse-width modulation. In the first case conduction time is maintained constant, and the repetition rate is varied, whereas in the second case the pulse repetition rate is kept constant and the conduction time per cycle is varied. Generally speaking, all three approaches are applicable to DC switching circuits, with cycling rates varying from a few Hertz to 20 kHz. The upper frequency limit is determined by the total cycling time of the solid state switch. In the case of thyristor choppers, the turn-off time is the prime switching parameter, determining the maximum operating frequency.

DC choppers are extensively employed in variable speed drives

where rheostats or series parallel switching of batteries is considered unsatisfactory; the former due to excessive power loss, and the latter due to the lack of smooth acceleration. In separately excited DC motors choppers may be employed in the field circuits to achieve a greater range of speed control, this method being extensively used by the "Green Line" in the M.B.T.A. Rapid Transit System.

Within the last few years the economical availability of large thyristors has led to the highly efficient use of power pulse controlled DC motors with corresponding influx of numerous chopper circuits. In general, they all employ resonant circuits for reversal of voltage polarity on the turn-off capacitor. They may vary in the type of commutation employed (voltage or current commutation), capability of regeneration, and load voltage reversal, but they all have a high operating efficiency under varying load conditions, and the unique ability to impose a current limit on the load circuit.

Selection of the Current Commutated Chopper, as one of the two circuits constructed to illustrate the Parity Simulation concept was based on a number of criteria: This circuit yields to an uncomplicated theoretical analysis and exhibits interesting behavior of certain variables during the commutation interval. Since it contains 5 switching elements, the circuit has $2^5 = 32$ possible states which must be considered, although in this case, many of these states can be eliminated a priori. Last but not the least, was the fact that an actual chopper circuit with conventional components was readily available to verify the Parity Simulation results.

7.2.2 Current Commutated Chopper

Figure 7.2.1 illustrates the basic principle of a current commutated chopper. Q_1 is the load thyristor which may be turned on by being triggered with a gate pulse. Commutation is achieved by means of external circuit elements not shown in the diagram. Diode D_1 is a freewheeling diode which permits the load current to circulate after the thyristor (Q_1) has been commutated off. A typical load current diagram is illustrated in Fig. 7.2.1(b), under the assumption that the switching time can be neglected, since this interval, compared to the switching frequency, is small. Using superposition and assuming steady-state, the condition of periodicity results in:

$$0 < t < T/2 \quad i_o(t) = \frac{V_o}{R} \frac{2}{1 + e^{-\tau/2T}} e^{-t/\tau} \qquad (7.2.1)$$

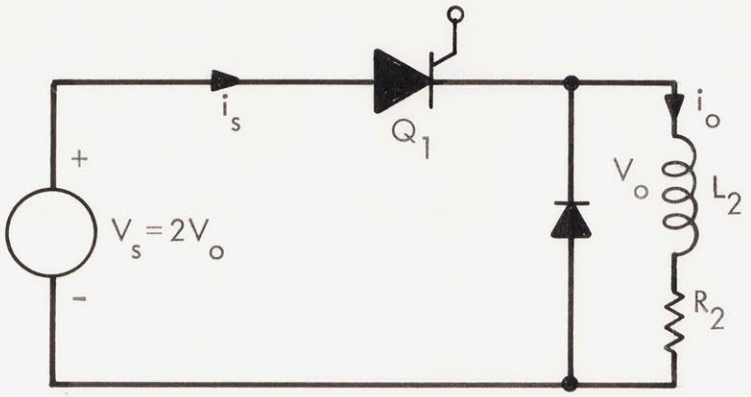
and

$$T/2 < t < T \quad i_o(t) = \frac{2\,V_o}{R} \frac{1 - e^{-(t-\tau/2)/\tau}}{1 + e^{-\tau/2\,T}} e^{-t/\tau} \qquad (7.2.2)$$

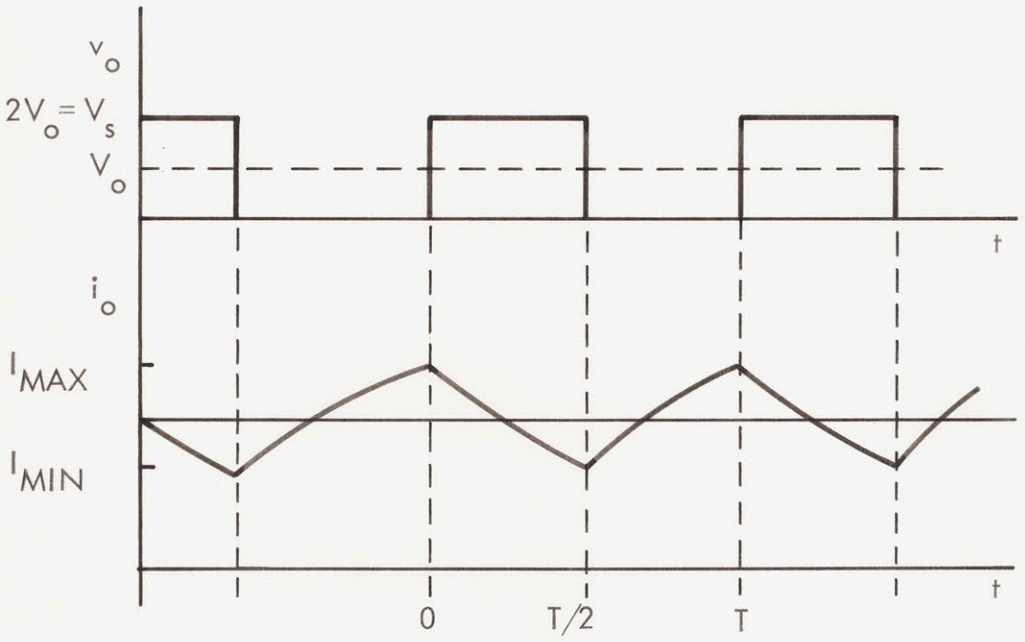
where $\tau = L_2/R_2$

Equation (7.2.2) implies that for a fifty percent duty cycle, and continuous current conditions, the ratio T/τ should be less than ten. Accordingly, for 50 Hertz τ should be greater than 2 milliseconds. For a load resistance R_2 of 300Ω, this suggests a load inductance value greater than 0.6 Henry. A 4 Henry inductor, which was readily available was utilized for this purpose.

The next step is to add the components required for the



(a)



(b)

Fig. 7.2.1 Basic Principle of a Current Commutated Chopper

commutation of load thyristor Q_1. The complete chopper circuit including the commutation circuitry is shown in Fig. 7.2.2. Selection of the specific component values is based on calculations done beforehand. As the commutation circuitry determined the numerical values of the key parameters in the chopper, its sequence of operation will be briefly discussed as follows:

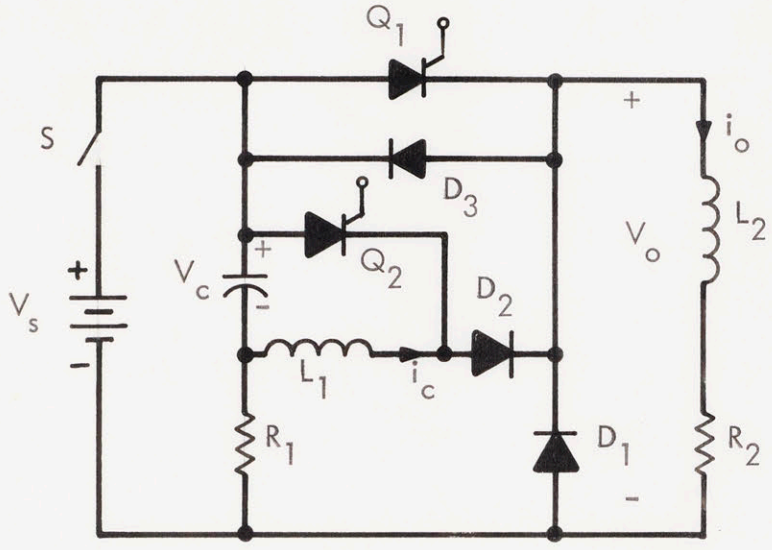
1) At $t = t < 0$, switch S is closed. The capacitor voltage increases exponentially to supply voltage V_s with a time constant of R_1 C.

2) At $t = 0$ thyristor Q_1 is triggered. Current now flows from the supply, through Q_1 to the load, increasing exponentially to its maximum value.

3) $0 < t < t_1$. Commutating thyristor Q_2 is turned on. An oscillatory current i_c starts to flow as capacitor C discharges, reaching a maximum when the voltage across L_1 reaches zero.

4) $t_1 < t < t_2$. The oscillatory current i_c, which initially was negative now becomes positive. Diode D_2 turns on, and commutating thyristor Q_2 turns off. Since the load current i_o is constant for the relatively short commutation interval, the appearance of the oscillatory current i_c reduces the forward current of thyristor Q_1 (i_{q_1}) which eventually becomes zero.

5) $t_2 < t < t_3$. Diode D_3 turns on; as it is in inverse parallel with thyristor Q_1, Q_1 is reverse biased and rapidly



C = 2 μF
L_1 = 10 mH
L_2 = 4 H
R_1 = 1.5 kΩ
R_2 = 300 Ω
V_s = 22 V

Q_1, Q_2 - C220D
D_1, D_2 - 1N34A

All Resistors = 1/2 W

Fig. 7.2.2 Current Commutated Chopper Circuit.
Element Values Shown are for the Actual Circuit.

turns off.

6) $t_3 < t < t_4$. Diode D_3 turns off and D_2 turns on. Thyristor Q_1 has already been commutated off.

7) $t_4 < t < t_5$. The load voltage V_o goes to zero and the free-wheeling diode (D_1) turns on. Oscillatory current flows until all the energy stored in the commutating inductance L_1 has been transferred to capacitor C, and consequently the capacitor voltage v_c increases above V_s.

8) $t_5 < t$. Capacitor current i_c reverses polarity and becomes negative. Consequently diode D_2 turns off, and capacitor C now discharges through resistor R_1 to the supply voltage V_s. During this brief interval, the load current is decaying exponentially to its minimum value.

9) $t = T$. At the end of the cycle, load current i_o has reached its minimum value $i_{o\ min.}$ Thyristor Q_1 is once again turned on, and the cycle is repeated.

7.2.3 Component Values of the Actual Circuit

To verify the simulation, an actual circuit was constructed using actual components whose designed values are indicated in Fig. 7.2.2. Phase control thyristors (C220B) having a relatively large turn-off time (50μ seconds) were used. The chopping frequency was 50 Hz. Operating at comparatively low supply voltages (22 volts) made snubbers unnecessary, the dV/dt being well within the maximum rating of the devices. Hence the waveforms do not have the expected

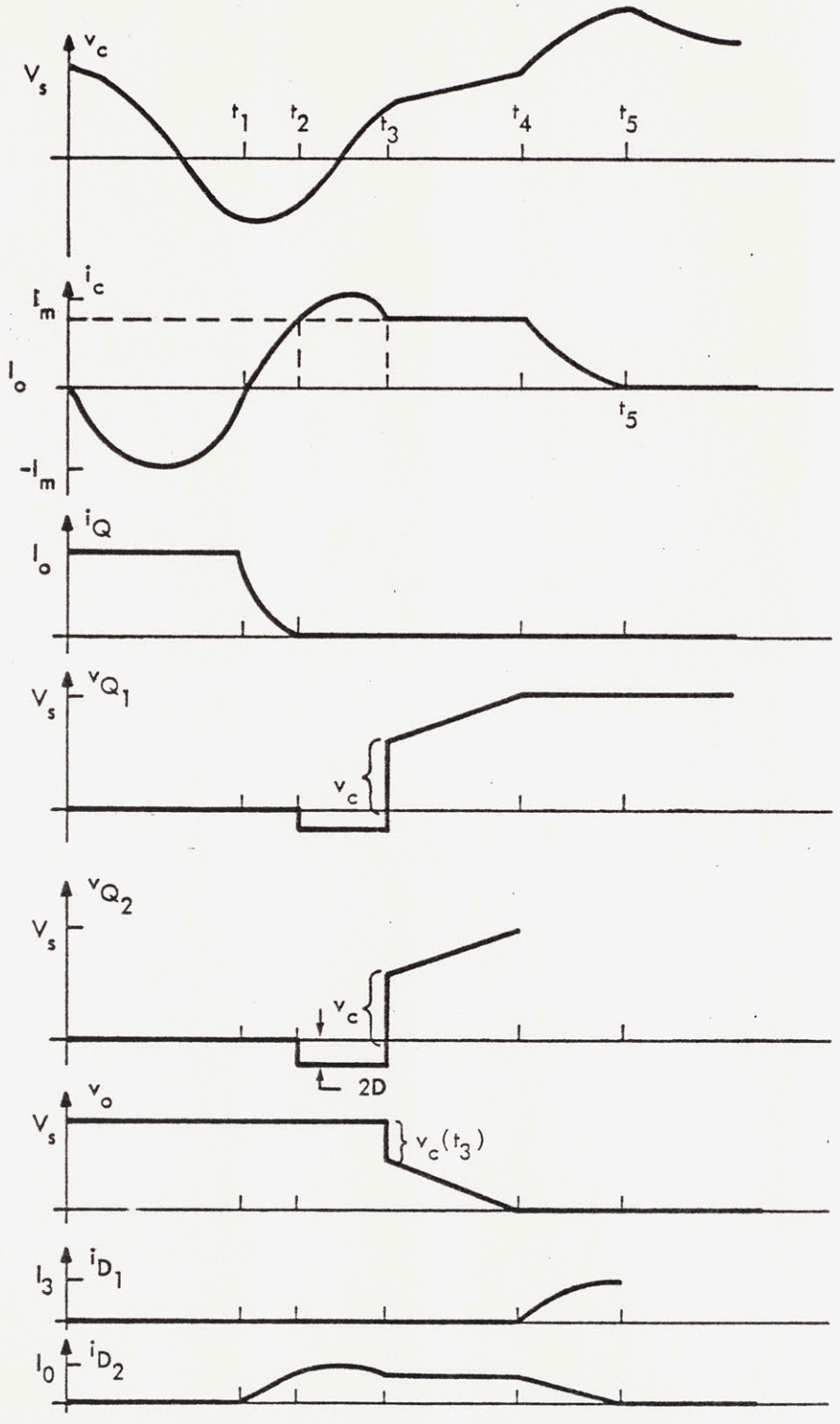


Fig. 7.2.3 Time Variations of Currents and Voltages in The Circuit

snubber oscillations superimposed on them.

A Power Device Controller[13] was used to obtain synchronized but optically isolated gate firing pulses for the two thyristors, the firing frequency was set at 50 Hertz and the gate current limited to 50 mA. Load inductor L_2 was a general purpose inductor with a relatively low Q of 12.6 at 50 Hertz. Commutating inductor L_1 was a precision linear inductor with a quality factor of 20 at 50 Hz. The winding capacitance was such that the ringing frequency was underdamped; however, connecting a 2.2 kΩ damping resistor in parallel, greatly helped matters. Diodes D_1, D_2 and D_3 were medium curent devices of the type IN4961. Due to the limited current carrying capacity of the load inductor L_2, the chopper could not be operated anywhere close to the maximum rating of the circuit components.

Measurements were made using a Tektronix 454 Oscilloscope and a P-6430 DC current probe. Figure 7.2.4(a) illustrates the various circuit variables in the actual circuit.

7.2.4 Parity Simulation

The simulated chopper uses five types of synthetic element modules: inductor, capacitor, resistor, thyristor and diode. Moreover it (chopper) uses five switching devices giving 32 possible states. These states correspond to various combinations of conducting and non-conducting devices. Under normal operation the circuit exhibits only 7 of these states. These are stated below. The variables refer to Fig. 7.2.2.

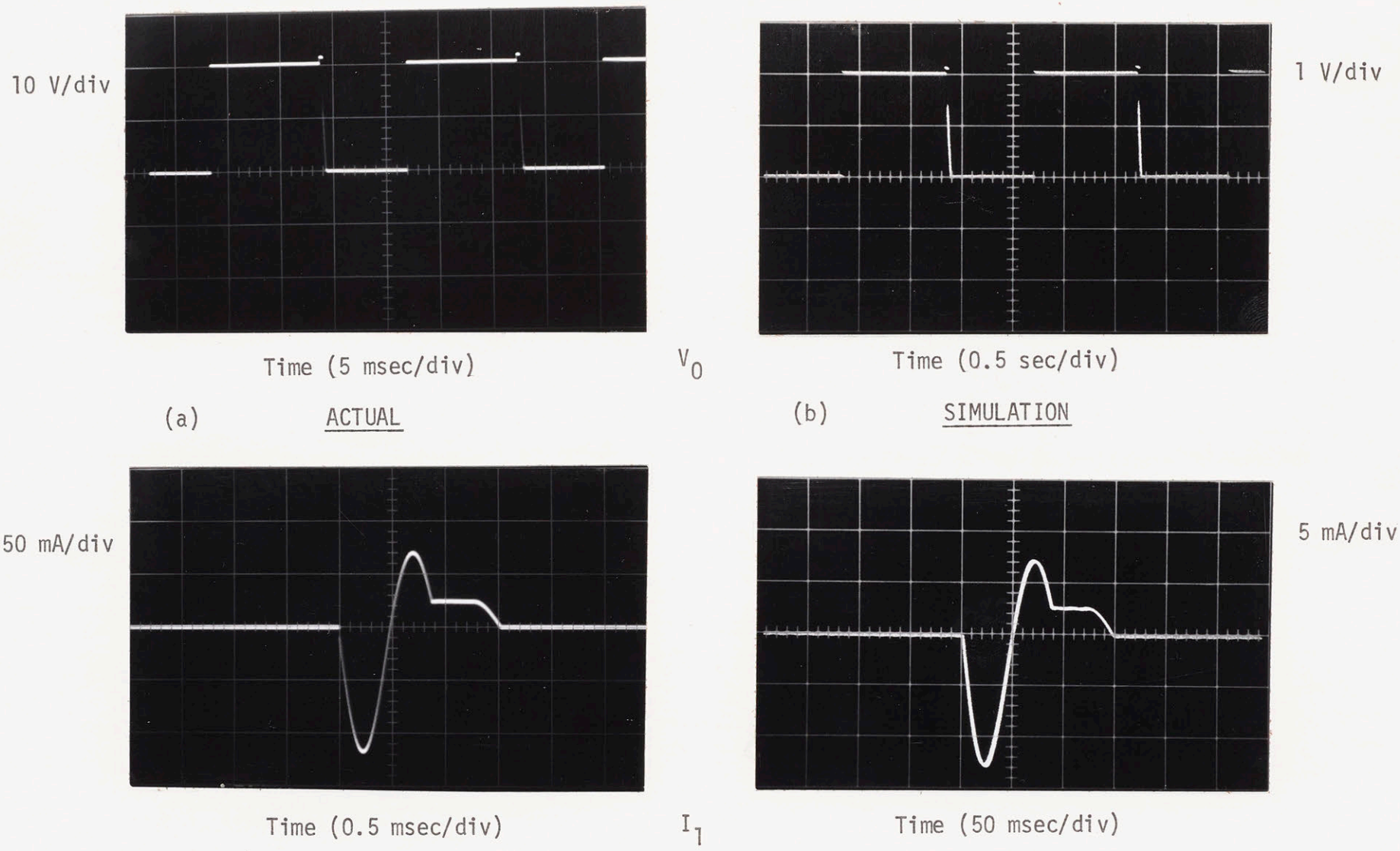
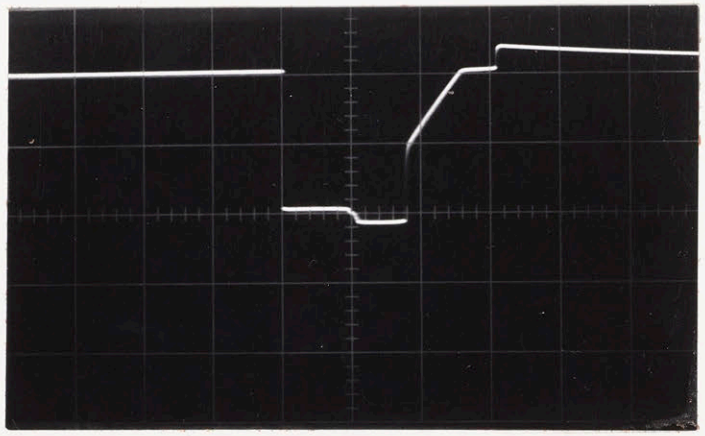


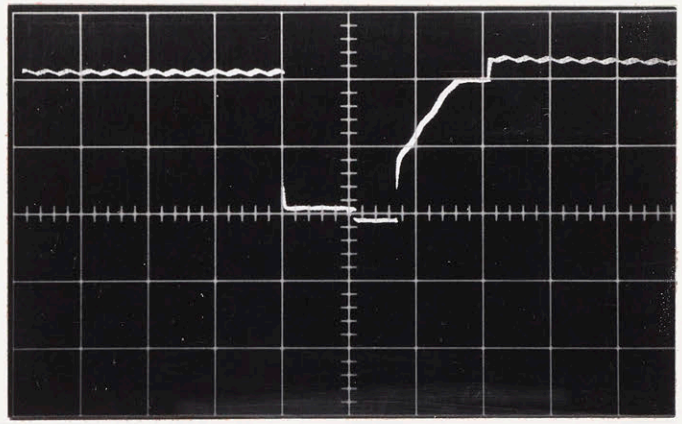
Fig. 7.2.4 Waveforms of the Current Commutated Chopper of Fig. 7.2.2

10 V/div



Time (0.5 msec/div)

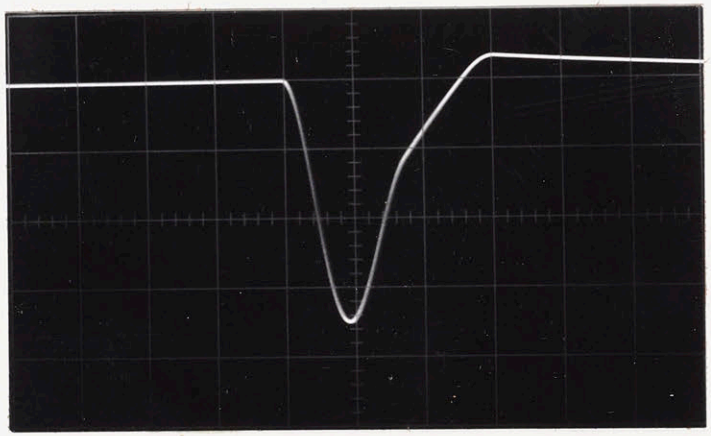
V_{Q_2}



1 V/div

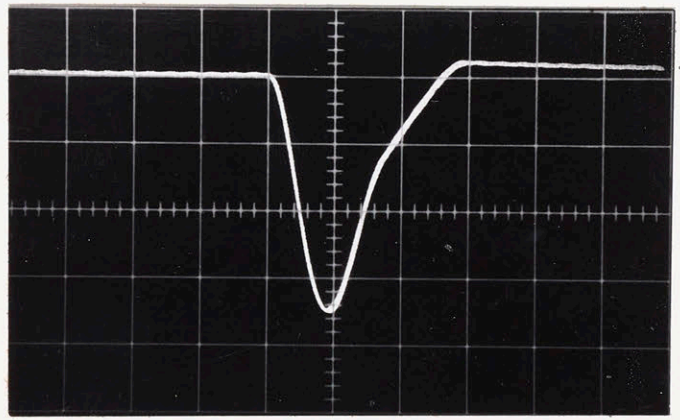
Time (50 msec/div)

10 V/div



Time (0.5 msec/div)

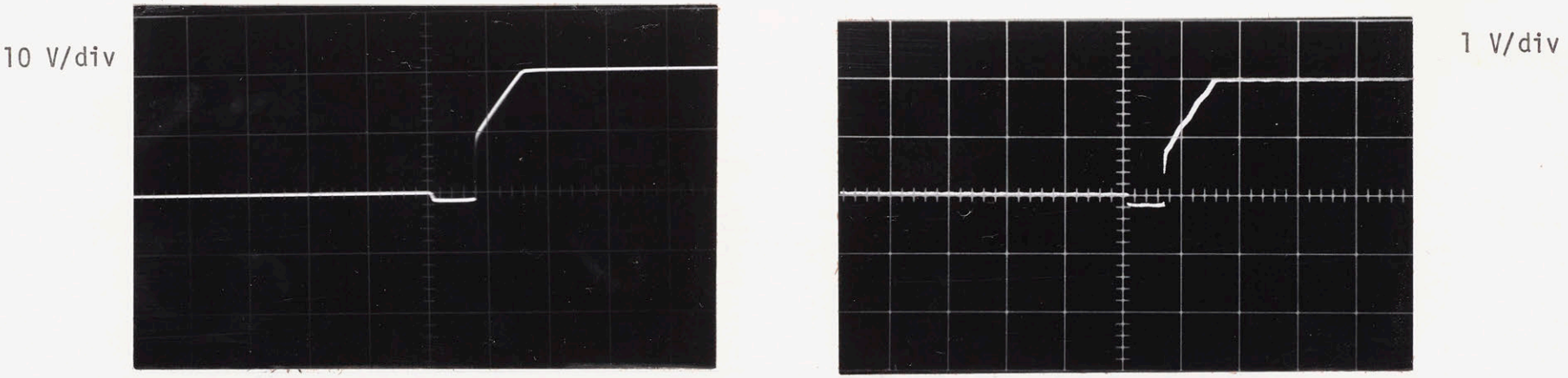
V_c



1 V/div

Time (50 msec/div)

Fig. 7.2.4 (Continued) Waveforms of the Current Commutated Chopper of Fig. 7.2.2



(a) ACTUAL

(b) SIMULATION

Fig. 7.2.4 (continued) Waveforms of the Current Commutated Chopper of Fig. 7.2.2

$$\begin{bmatrix} \dot{v}_C \\ \dot{i}_1 \\ \dot{i}_2 \end{bmatrix} = [A] \begin{bmatrix} v_C \\ i_1 \\ i_2 \end{bmatrix} + [B][V_s]$$

I (00100)

$$[A_I] \quad \begin{bmatrix} -\frac{1}{R_1 C} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{R_L}{L_2} \end{bmatrix} \qquad [B_I] = \begin{bmatrix} \frac{1}{R_1 C} \\ 0 \\ 0 \end{bmatrix}$$

Q_1 gate pulse

II (10000)

$$[A_{II}] = \begin{bmatrix} -\frac{1}{R_1 C} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{R_2}{L_2} \end{bmatrix} \qquad [B_{II}] = \begin{bmatrix} \frac{1}{R_1 C} \\ 0 \\ \frac{1}{L_2} \end{bmatrix}$$

Q_2 gate pulse

III (11000)

$$[A_{III}] = \begin{bmatrix} -\frac{1}{R_1 C} & -\frac{1}{L_1} & 0 \\ 1\frac{1}{L_1} & 0 & 0 \\ 0 & 0 & -\frac{R_2}{L_2} \end{bmatrix} \qquad [B_{III}] = \begin{bmatrix} \frac{1}{R_1 C} \\ 0 \\ \frac{1}{L_2} \end{bmatrix}$$

$i_1 = 0$

IV (10010)

$$[A_{IV}] = [A_{III}] \qquad [B_{IV}] = [B_{III}]$$

$$i_1 \geq i_2$$

V (00011)

$$[A_V] = [B_{IV}] \qquad [B_V] = [B_{IV}]$$

$$i_1 \leq i_2$$

VI (00010)

$$[A_{VI}] = \begin{bmatrix} -\frac{1}{R_1C} & -\frac{1}{C} & 0 \\ \frac{1}{L_1+L_2} & -\frac{R}{L_1+L_2} & 0 \\ 0 & 0 & 0 \end{bmatrix} \quad [B_{VI}] = \begin{bmatrix} \frac{1}{R_1C} \\ \frac{1}{L_1+L_2} \\ 0 \end{bmatrix}$$

$$v_o = 0$$

VII (00110)

$$[A_{VII}] = \begin{bmatrix} -\frac{1}{R_1C} & -\frac{1}{C} & 0 \\ \frac{1}{L} & 0 & 0 \\ 0 & 0 & -\frac{R_2}{L_2} \end{bmatrix} \quad [B_{VII}] = \begin{bmatrix} \frac{1}{R_1C} \\ \frac{1}{L} \\ 0 \end{bmatrix}$$

In the case of the Parity Simulation, these states need not be determined, since the synthesized switching elements will automatically establish the circuit states as do their counterparts in the actual

network. Figure 7.2.5 shows the Parity Simulator programmed for all existing states. On the other hand, although the analog computer operates this way in principle, the user must first guarantee that his analog topology is algebraically explicit for each state. Hence for each individual state he must make preliminary calculations, determine the individual state of each element in the network prior to every "state run", and patch changes in the network inbetween runs. Particularly he has to be certain to avoid undefined or non-existent states, which in power circuits is certainly not a trivial matter.

Figure 7.2.6(a) shows the chopper in state 11000. The differential equations for this state are:

$$\frac{d\,V_c}{dt} = -\frac{1}{R_1 C} V_c - \frac{1}{C} i_1 + \frac{1}{R_1 C} V_s \qquad (7.2.3)$$

$$\frac{di_1}{dt} = \frac{1}{L} V_c \qquad (7.2.4)$$

$$\frac{di_2}{dt} = -\frac{R_2}{L_2} i_2 + \frac{1}{L_2} \qquad (7.2.5)$$

Figure 7.2.6(b) illustrates the patching required for the solution to the above differential equations. The analog computer uses an appropriate interconnection of amplifiers, integrators and summers - this interconnection changing when the circuit changes state, but bearing no topological relationship to the system being modeled. This changing interconnection pattern is one of the major obstacles to the analog computers' use for the study of circuits employing semiconductor switching

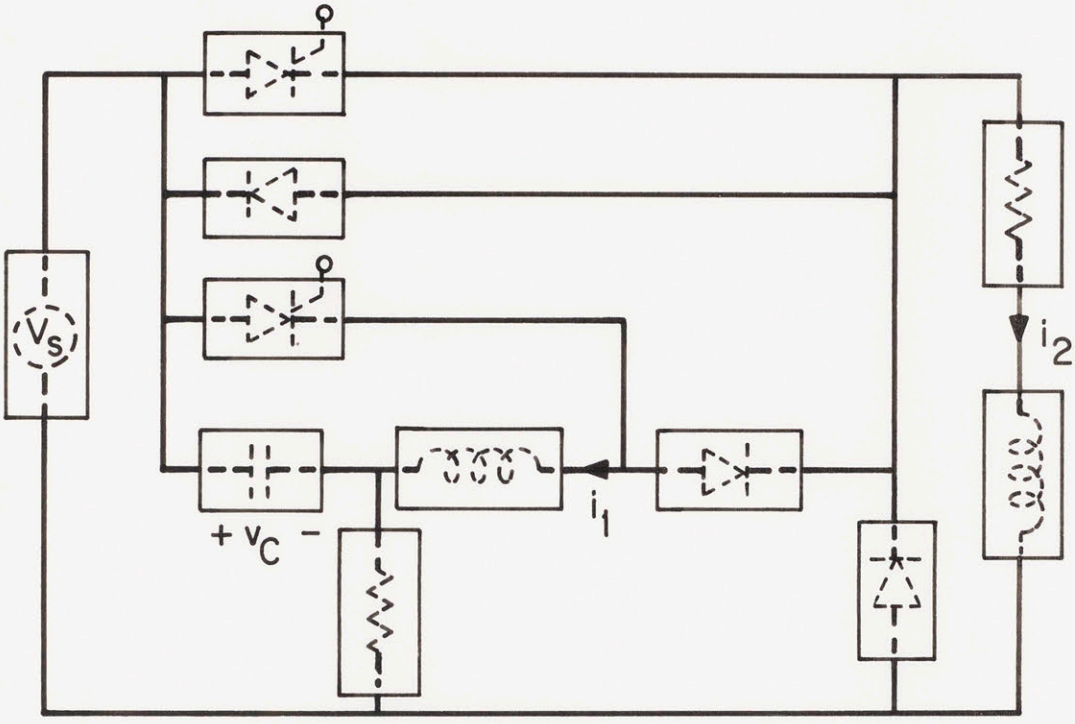


Fig. 7.2.5 Parity Simulator "Programmed" for all States
(Boxes Correspond to Synthetic Elements)

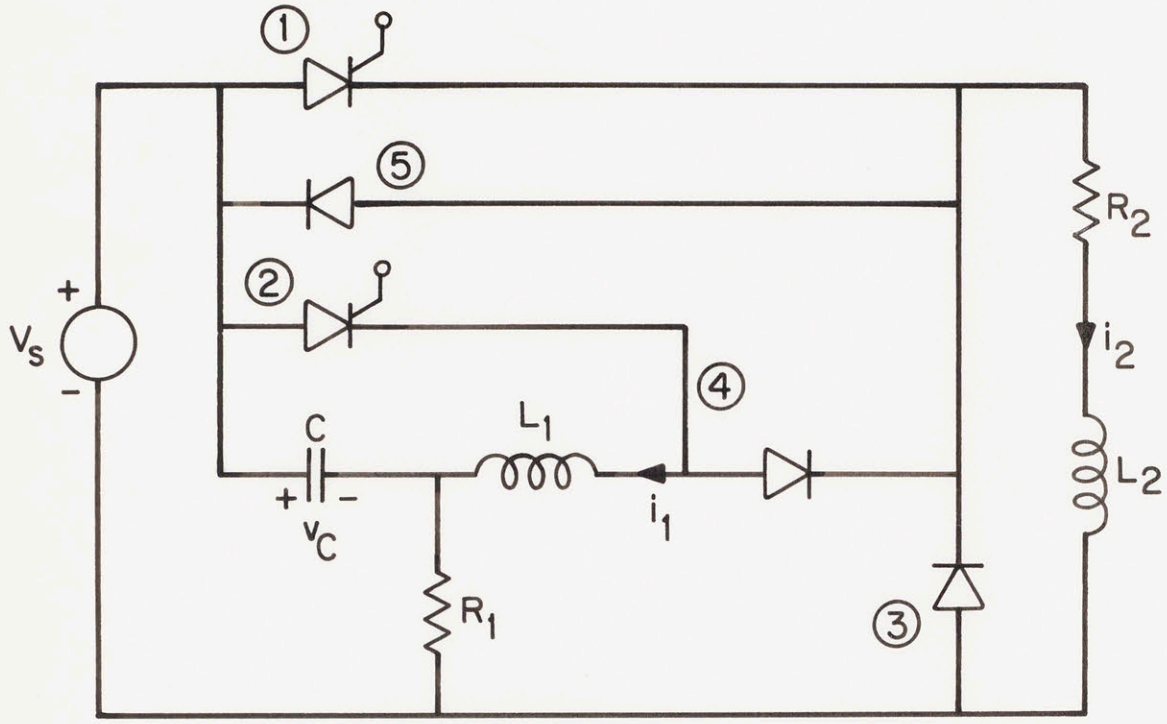


Fig. 7.2.6(a) Current Commutated Chopper in State 11000

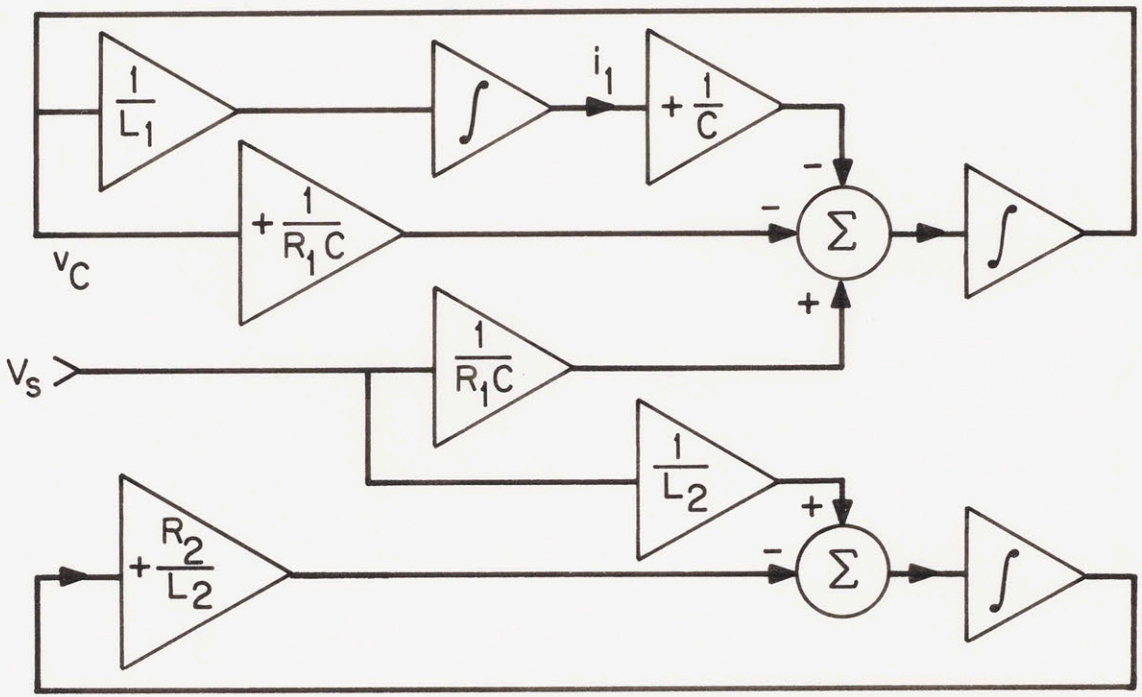


Fig. 7.2.6(b) Analog Computer Programmed for State 11000

elements.

As mentioned earlier, in the Parity Simulation there is no need to first represent the network by a set of state equations. Faults, shoot-throughs, etc., can all be studied without modifying the Parity Simulator. Also, unlike the Analog Computer, the Parity Simulator makes all network variables available at all times.

7.2.5 Scale Factor Requirements for the Parity Simulator

The element values in the simulation are chosen by scaling the maximum voltage and current values to within the maximum values allowed by the element modules which are $\pm$ 12 volts and 120 mA respectively. The time scale is chosen such that the maximum frequency in the model is within the bandwidth of the modules. In the case of the chopper, the voltage and currents were both scaled down by a factor of 10, and the time scale was expanded by a factor of one hundred. Obviously the impedance scaling depends on the scale chosen for voltage, current and frequency. In the above case, the impedance scale factor is unity, giving a scale factor of a hundred for the simulated inductance and capacitance values. Thus the numerical values of the simulated resistance, inductance and capacitance in Fig. 7.2.2 are R_2 = 300Ω, R_1 = 1.5 kΩ, L_1 = 1 H, L_2 = 400 H, and C = 200 μF. The frequency of the triggering pulses was 0.5 Hz, obtained from a phase-locked loop based optically isolated firing circuit. Measurements were made on a Tektronix 545 storage Oscilloscope.

7.2.6 Simulation Results

Figure 7.2.4(b) illustrates the various circuit variables as

measured in the Parity Simulation. Although both current and voltage variables are shown, in the simulation they all result from voltage measurements, since somewhere in each synthetic element there is a voltage proportional to the current flowing through the element. This is particularly convenient for instrumentation purposes. Of course the parity concept also permits the use of a current probe, if desired.

The detailed correspondence of the waveforms is impressive. Not only the shapes, but the relative amplitudes and frequency are identical. There is a slight ripple on voltage V_{q2}; this was found to be caused by the magnetic field emanating from the power supply transformers mounted directly beneath the circuit boards. Mounting the power supplies in a remote location will elminate this 60 Hz interference.

7.2.7 Correlation of Results

The simulated and actual chopper circuits were operated at a fundamental frequency of 50 Hz. The standard equations[12] were used to calculate results for comparison with experimental values. These results, both experimental and calculated are summarized in Table 7.2.1. The time intervals t_1 to t_5 are defined in Fig. 7.2.3. Correlation between the calculated, actual and simulated time intervals is quite good. In fact there is fair agreement between the calculated, simulated and actual values of the different individual parameters. These results give a high degree of assurance of the validity of the simulation technique used.

7.3 Simulation of a 2 kW, 10 kHz Series Inverter

Inverter design is one of the most demanding tasks that

Table 7.2.1

Parameter	Calculated Values	Actual Values	Simulated Values $\times 10^2$
t_1	0.44 msec	0.48 msec	0.49 msec
t_2	0.46 msec	0.50 msec	0.51 msec
t_3	0.90 msec	0.88 msec	0.88 msec
t_4	1.37 msec	1.30 msec	1.28 msec
t_5	1.69 msec	1.60 msec	1.58 msec
t_{q1} (Turn-off Time Presented to Q_1	0.42 msec	0.4 msec	0.38 msec
t_{q2} (Turn-off Time Presented to Q_2	0.44 msec	0.41 msec	0.39 msec
Peak Capacitor Voltage	23.77 volts	24.0 volts	23.5 volts (Scale Factor = 10^{-1})

currently face the circuit designer. Early experience in "thyratron tube days" served as an introduction to some of the more complex considerations that have emerged, as the time domain and instrumentation have progressed to the present micro-second level. This progress has led to new techniques of design, and a much wider application acceptance.

7.3.1 Inverter Circuits

Many prime sources of electrical energy today produce direct current. In the future, many of the new conversion methods for direct conversion of thermal to electrical energy will also produce direct current. For example, thermoelectric, thermionic, and magnetohydro-

dynamic devices, as well as fuel cells, all have a common demoninator - they are direct current generators. While direct current is useful for a number of applications, the majority, especially where large amounts of power are involved, require alternating current. This calls for an efficient and reliable method for converting direct current to alternating current at some desired output voltage and frequency. An inverter is invariably used for this purpose, mainly because of its high reliability, good output waveform and low switching losses.

Semiconductor devices used in inverters are of two types, thyristors and transistors. (Some special designs, of course, use both devices.) However, the thyristor very definitely has the greatest potential for very high power operation.

SCR inverters can be conveniently categorized by identifying the method used to commutate or switch off the devices. Series commutated inverters make use of a charged capacitor which is connected in series with the load to bring the load current to zero and turn-off the appropriate SCR. When the capacitor is in parallel with the load, it is for reversing the anode voltage on an SCR to turn the device off. This arrangement is called parallel commutation. Lastly there is the impulse commutation which uses an auxiliary LC tank which stores energy, which is used to commutate the SCR's. Each inverter circuit has its own unique characteristics which make them desirable for specific applications. One circuit may have high efficiency while another may give excellent frequency regulations. However, they all have certain specified characteristics which are 1) input voltage, 2) output voltage, 3) output power, 4) frequency stability, 5) load regulation, 6) overall

efficiency, and 7) harmonic distortion of the output waveform. The last characteristic is a major issue in some applications, and so a great deal of emphasis has been placed on it. The output voltage (in most cases) is non-sinusoidal, and the harmonic voltages have a significant effect on the overall system performance. Elaborate inverter circuits can be devised to reduce the harmonics, making cost prohibitive and an economic decision must be made, on the basis of cost versus harmonic distortion.

Present day thyristor inverters typically work at an input voltage range of 50 - 4000 volts, and an input current of 1 - 1000 amps. The normal range of output power is from 50-watts to 4 MW, though 20 MW units have been designed and tested. Typical operating frequencies are from 60 Hz to 20 kHz, with efficiencies approaching 90% in most cases.

Applications of inverters include uninterruptible power supplies, variable speed AC motor drives, aircraft power supplies, induction heating, output of DC transmission lines, ultrasonic cleaning, cycloconverter supplies and DC-DC converters, where the advantages of light weight, small size, low cost, and fast response time due to the high frequency link are very apparent. They are also used in sonar transmitters operating in the VLF (Very-Low Frequency) band. Recently inverters have also found applications in high-frequency fluorescent lighting supplies. Because of the high frequency of the inverter circuits, the size and weight of the magnetics is considerably reduced; moreover, low cost capacitors can be used to maintain a unity power factor in the overall circuit. The overall efficiency can be substantially improved, which also means a decrease in power dissipation.

This decrease in power dissipation in a large industrial complex can mean less burden on the air-conditioning system, resulting in a substantial saving in energy requirements.

7.3.2 Classification of Inverter Circuits

The basic classification of inverter circuits is by methods of turn-off. They are divided into six classes:

i Class A. These inverters are commutated by resonating the load. They are most suitable for high frequency operation with sinusoidal output.

ii Class B. Inverters in this class are self-commutated by an LC circuit. They are relatively simple circuits, with regulation by time-ratio control.

iii Class C. LC switched by a load carrying SCR. An example of this class of inverters is the well known McMurray-Bedford inverter.

iv Class D. LC switched by an auxiliary SCR. This type of inverter has both pulse-width and time-ratio regulation. The commutation energy may readily be transferred to the load and so high efficiencies are possible.

v Class E. External pulse source for commutation. It is capable of very high efficiencies.

vi Class F. This class of inverters is line commutated. Obviously it requires a source of alternating power; however, efficiencies are very high.

A self-commutating series inverter was selected as the final circuit to illustrate and verify the Parity Simulation concept. This

selection was not arbitrary, but was based on the underlying criteria:

1) Sine wave output, unlike the chopper simulation, (Section 7.2) which has a square wave output.

2) Exhibits very interesting behavior of certain key parameters during the commutation interval.

3) Non-trivial number of switching components used.

4) Relatively high frequency of operation (10 kHz as compared to 50 Hz for the chopper).

5) Ease of availability of the actual 10 kHz series inverter circuit, to be used for parameter comparison purposes.

7.3.3 Operational Description of the Series Inverter

The operation of the power circuit of the Series Inverter is first discussed, and this is followed by component value selection.

7.3.3.1 Power Circuit for the Series Inverter

Figure 7.3.1 illustrates the circuit of the series inverter. The 60 Hz AC supply is rectified using a center tapped transformer and a half wave bridge rectifier. The rectifier output is filtered, and applied to a center-tapped capacitor bank creating a split supply for the inverter. The operation of the inverter is as follows: When thyristor Q_1 is fired, current flows from the top capacitor to load capacitor C, charging it to a voltage approaching 2 V_s. The current then reverses, and flows back to the supply via diode D_1, and the load capacitor discharges. Diode D1, connected in inverse-parallel to thyristor Q_1 presents the necessary turn-off time to Q_1. Thyristor Q_2 is triggered

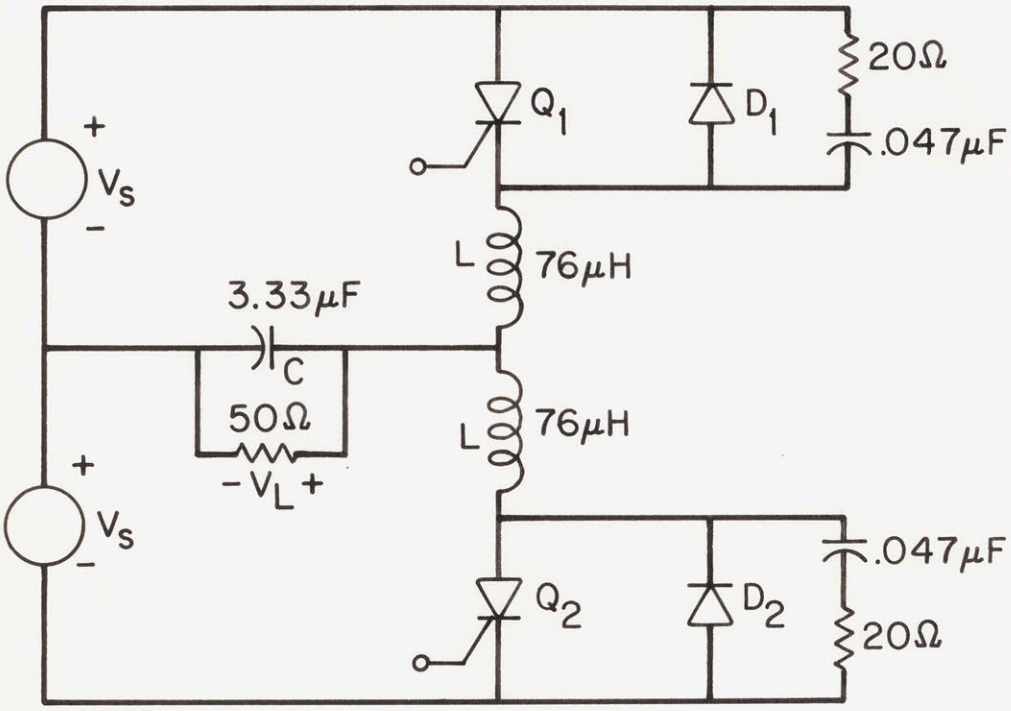


Fig. 7.3.1 2 kW, 10 kHz Series Inverter

next and a similar cycle occurs for the lower half of the center-tapped capacitor. Thyristor Q_1 is retriggered and the complete cycle repeats itself.

7.3.3.2 Selection of Component Values

The circuit of Fig. 7.3.1, using a pair of General Electric C 149-S10 high speed thyristors, and two A28D fast recovery diodes was constructed in order to verify the simulation. A couple of 5500 μF 200 volt Sprague capacitors were used to obtain the necessary split supply. A transient voltage supression network was needed to limit the rate of change of forward voltage applied to the thyristors. Because of this transient, a snubber circuit, consisting of a series-connected resistor and capacitor was placed in shunt with the SCR. The snubber in conjunction with the circuit effective series inductance controls the maximum rate of change of voltage across the device when a stepped forward voltage is applied to it. Calculations indicated the RC snubber network to have numerical values of 20Ω and 0.047 μF respectively.

The LC ringing circuit consists of the 76 μH commutating inductors (L) and the series resonant capacitor C. The commutating inductors were wound on Arnold cores A12 6040-2 with 41 turns each. Analysis of the resonant circuit indicated the resonant capacitor value to lie between 3.2 - 3.4 μF. Selection of the type of capacitor for the LC resonant circuit is not a trivial problem, as the high peak currents would cause appreciable heating in the dielectric, specially at the high frequencies involved. In view of this fact, Mylar capacitors were used, and to minimize peak currents within the capacitors, a

parallel network was used. 0.1 μF was considered to be the optimum value for the individual capacitors in the network, and 32 of these capacitors were combined together to form a single capacitor of 3.33 μF. The circuit is basically a series resonant circuit, with the resonating capacitor in series with the resonating inductor. For optimum operation, the quality factor of the resonating circuit should be as large as possible; this can be accomplished by increasing the commutating capacitor C. Choice of C is based on ensuring that the maximum thyristor voltage is within the device ratings, while maintaining underdamped oscillations in the circuit.

The firing pulses were obtained from a Power Device Controller[13] which was set to operate at 10 kHz. The optically isolated 1 amp current limited output pulses were used to trigger thyristors Q_1 and Q_2.

Measurements were made using a Tektronix 454 Oscilloscope and a P-6042 DC current probe. Figure 7.3.2(a) illustrates the various circuit waveforms of the network variables in the actual circuit.

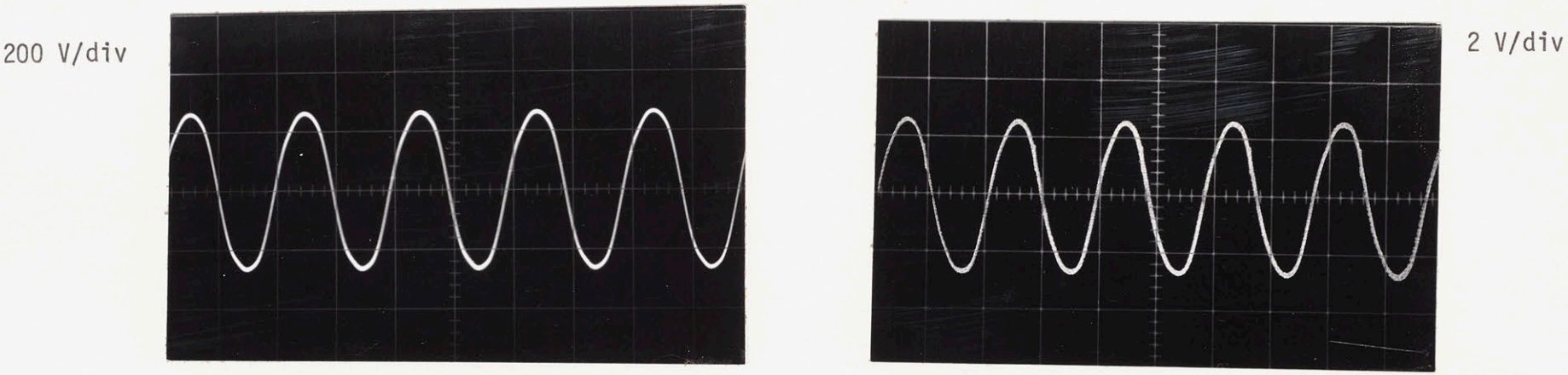
7.3.4 Analog Computer Simulation of the Series Inverter

In an analog computer simulation, circuits are analyzed by numerically solving the network differential equations (Ref. Chapter 2). In the case of the series inverter the network equations are

$$V_S - V_L = L \frac{d I_1}{dt} \tag{7.3.1}$$

$$V_S + V_L = L \frac{d I_2}{dt} \tag{7.3.2}$$

$$\frac{d V_L}{dt} = (I_1 - I_2 - I_3)/C \tag{7.3.4}$$



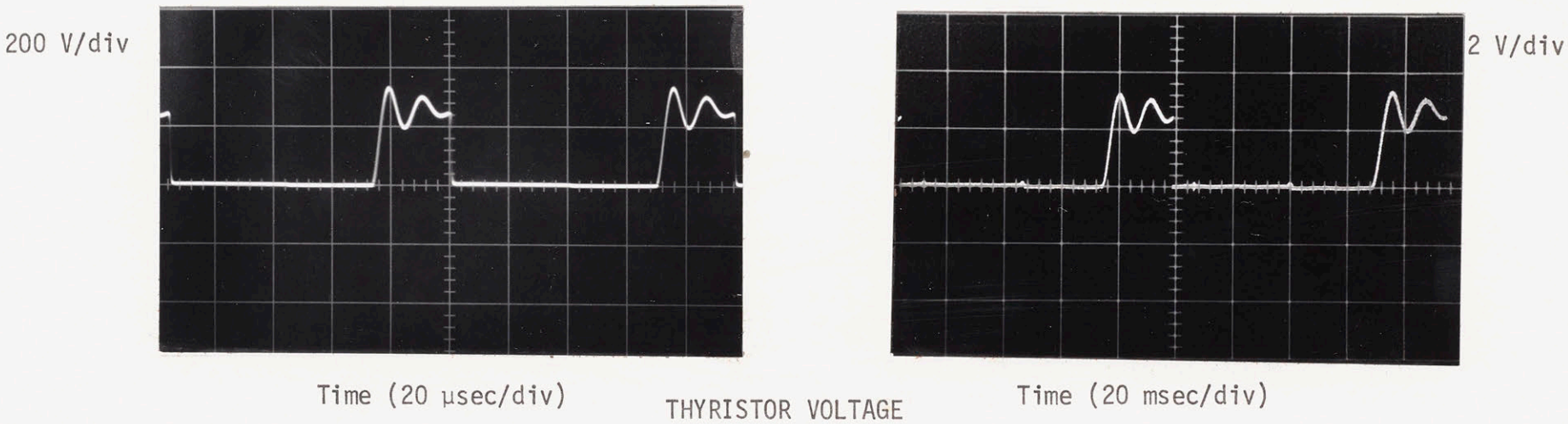
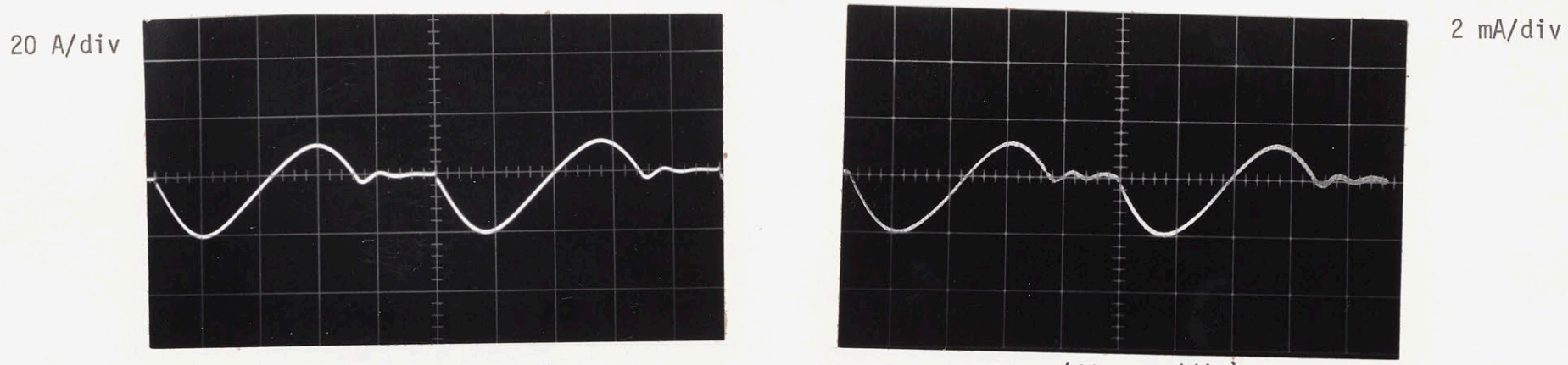


Fig. 7.3.2 Waveforms of the 2 kW, 10 kHz Series Inverter



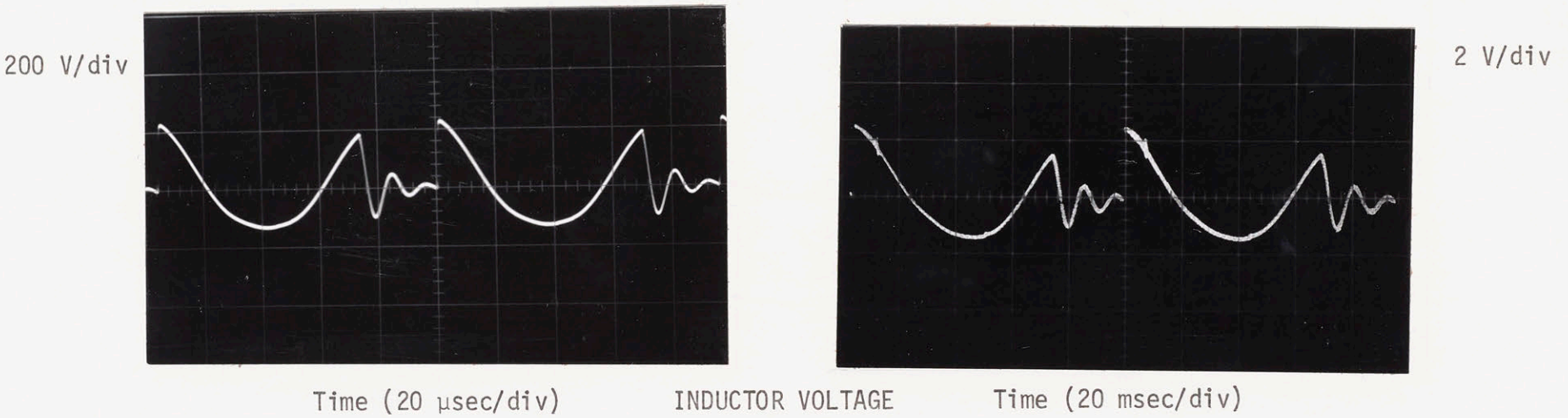
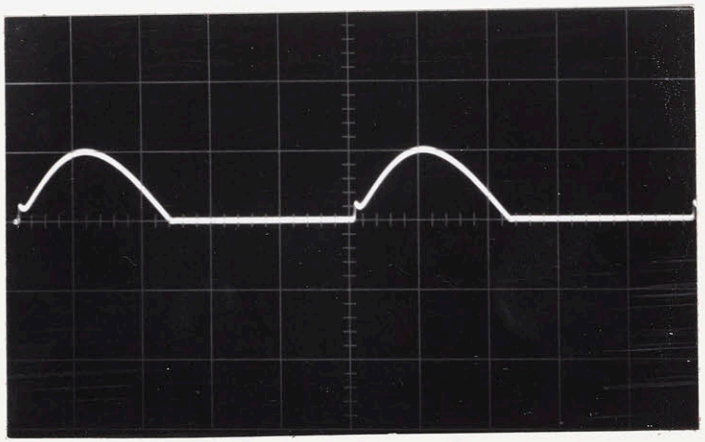
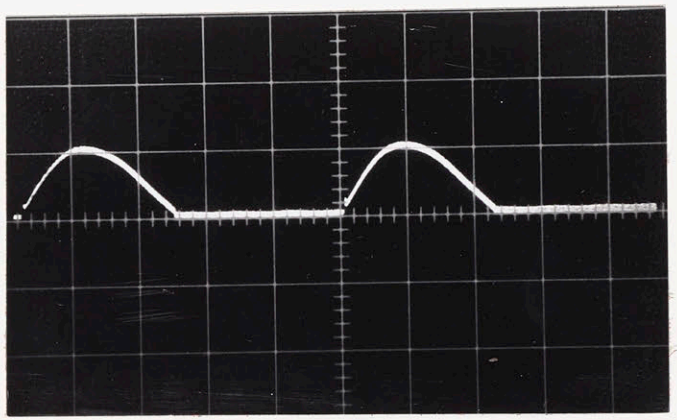


Fig. 7.3.2 (continued) Waveforms of the 2 kW, 10 kHz Series Inverter

20 A/div





2 mA/div

Time (20 sec/div) THYRISTOR CURRENT Time (20 msec/div)

(a) ACTUAL (b) SIMULATION

Fig. 7.3.2 (continued) Waveforms of the 2 kW, 10 kHz Series Inverter

$$V_L = I_3 R_L \qquad (7.3.4)$$

The switching elements (diodes and thyristors) are represented by current-zero switches, and the output is obtained as a set of variables, usually in a normalized form.

7.3.5 Parity Simulation of the Series Inverter

Currently the Parity Simulator has five types of synthetic element modules; inductor, capacitor, resistor, thyristor and diode. As mentioned earlier, all except the thyristor are two terminal modules through which an actual current can flow. The thyristor is obviously a three terminal device. Since the series inverter contains 4 switching elements, the circuit has 16 possible states. No state determination is necessary as the synthetic modules automatically establish the circuit states just like the actual elements. Consequently no "pre-programming" is needed, and the operator simply needs to patch the modules together topologically the same as in Fig. 7.3.1.

7.3.6 Scale Factor Requirements

As in the chopper simulation, the element values are chosen by scaling the maximum voltages and currents to within the maximum allowed by the Parity Simulator. Choice of the time scale is such that not only is the maximum frequency of the simulation within the bandwidth of the element modules, but that the scaled values of the inductance, capacitance and resistance are within the range of the simulated element modules. With the above constraints in mind, the scaling factors were chosen, 100:1 for voltage, 10^4:1 for current and 10^3:1 for

frequency, all simulated values being scaled down. The simulated element values are inductance L = 7.6 H, capacitance C = 33.3 μF and load resistance R_L being 5 kΩ. The triggering pulses were obtained from an optically isolated firing circuit, the repetition rate being 10 Hz. The various voltage and current measurements were made using a Tektronix 549 Storage Oscilloscope. Figure 7.3.3 shows the test set-up for comparing the simulated and actual circuit waveforms.

7.3.7 Simulation Results

Using the synthetic element modules, the series inverter was assembled, and the various circuit variables recorded. Figure 7.3.2(b) illustrates the waveforms of the currents and voltages as measured in the Parity Simulation. The accuracy of the simulation is evident in the comparison between the simulation results and the oscilloscope photographs taken from the actual operating circuit. Note the extremely close correlation between the response of the actual load voltage and the simulation. A similar correlation has been obtained between the other variables. Using the above results, the prime electrical characteristics are determined. They are discussed at length in the following sections.

7.3.7.1 Harmonic Analysis of the Load Voltage

Comparison of the load voltage waveforms was done using a 1900-A wave analyzer. The tabulated results show a high degree of similarity between the lower harmonics in the simulated and actual circuits. In the case of the fourth and fifth harmonics, there seems to be an appreciable difference between the simulated and actual values; however,

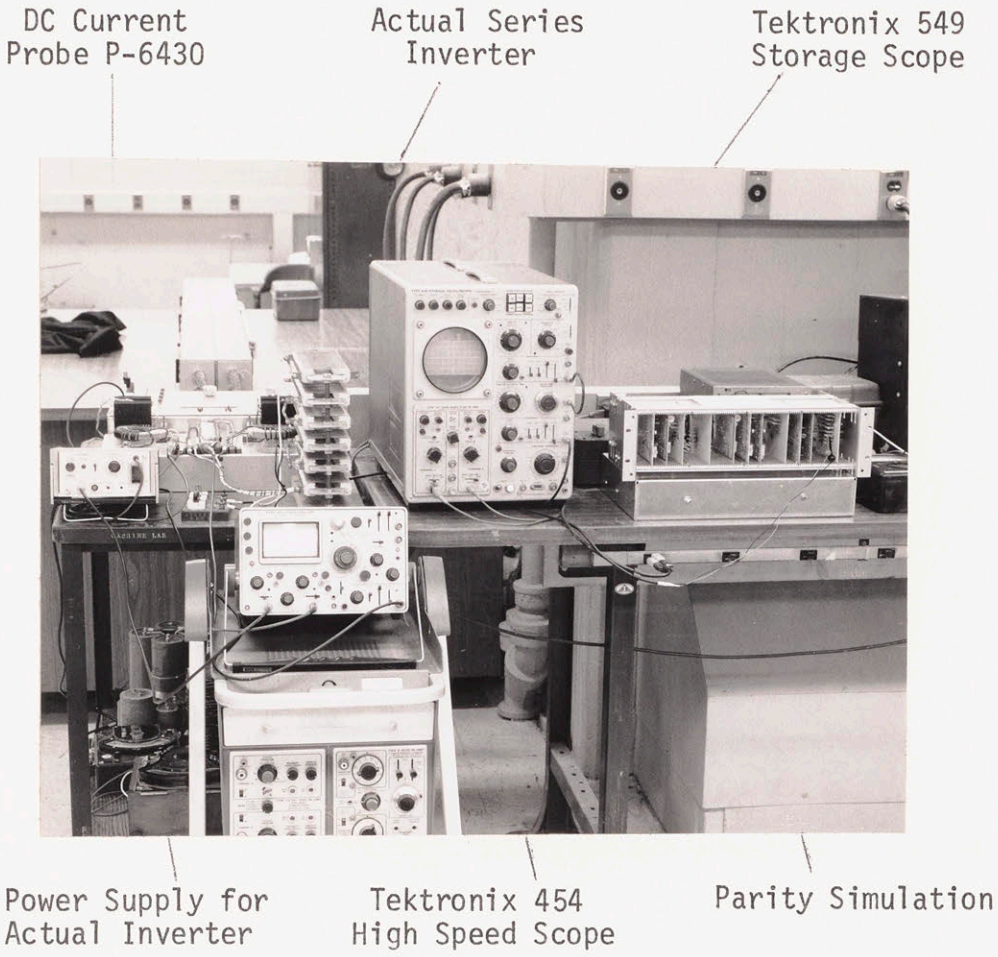


Fig. 7.3.3 Test Set-up for the Simulated and Actual Series Inverter Circuit

a large part of this difference is attributed to experimental error due to the extremely small amplitudes involved. Table 7.3.1 shows the percentage error in the harmonic content of the simulated output voltage as compared to the actual.

Table 7.3.1

Harmonic Analysis of Load Voltage

Harmonic	Actual	Simulation	% Error Compared to Fundamental
Fundamental	100%	100%	-
2nd Harmonic	1.5%	1.5%	0.0%
3rd Harmonic	6.0%	6.1%	-0.1%
4th Harmonic	0.7%	0.2%	0.5%
5th Harmonic	0.42%	0.96%	-0.54%

7.3.7.2 Comparison between the Simulated and Actual Results

The circuit of Fig. 7.3.1 using actual components was constructed, in order to verify the Parity Simulation results.

Table 7.3.2 compares the actual and simulation results for the resistive load case.

7.3.7.2.1 Glossary for Table 7.3.2

The parameters are arbitrarily defined as:

R_L = Load resistance placed across capacitor C in Fig. 7.3.1

$V_{load\ (0\text{-}Peak)}$ = Peak voltage across load resistance R_L

Turn-off time = Circuit commutated turn-off time presented to the SCR's.

Peak inductor current = Maximum current in inductor L_1

The sub-headings in the columns (in Table 7.3.2) "Sim." and "Act." refer to simulated and actual circuit values, respectively.

Table 7.3.2

Comparison of Simulated and Actual Results

R_L		V_{load} 0-Peak		Turn-off Time		Peak Inductor Current	
Sim. R x 100	Act. Ω	Sim. $x10^{-2}$	Act. Volts	Sim. mS	Act. μS	Sim. mA	Act. 10 x I
18	18	59.0	56.2	18.0	17.0	1.3	1.3
20	20	61.1	58.1	19.0	18.1	1.3	1.3
25	25	66.1	63.0	22.5	22.5	1.3	1.3
30	30	67.2	66.0	23.5	25.1	1.3	1.3
35	35	69.0	69.1	25.2	26.0	1.3	1.3
40	40	71.1	70.3	25.7	26.5	1.35	1.35
50	50	73.0	74.1	26.8	27.5	1.39	1.37
100	100	80.2	82.2	30.1	30.0	1.39	1.40

Table 7.3.2 shows the close correlation between the response of the actual inverter circuit and the Parity Simulation. This close agreement inspires confidence in the Parity Simulator's ability as a tool for equipment design.

Figures 7.3.4(a), (b) and (c) vividly compares the simulated

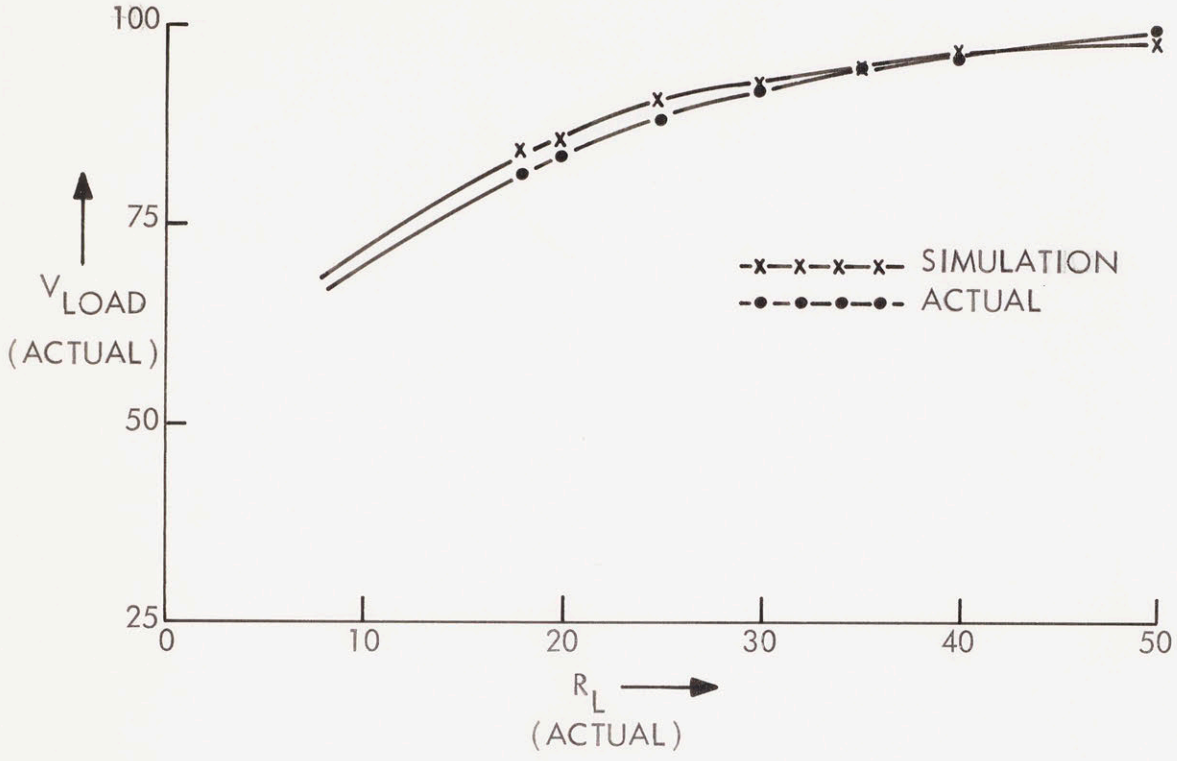


Fig. 7.3.4(a) Load Voltage versus Load Resistance

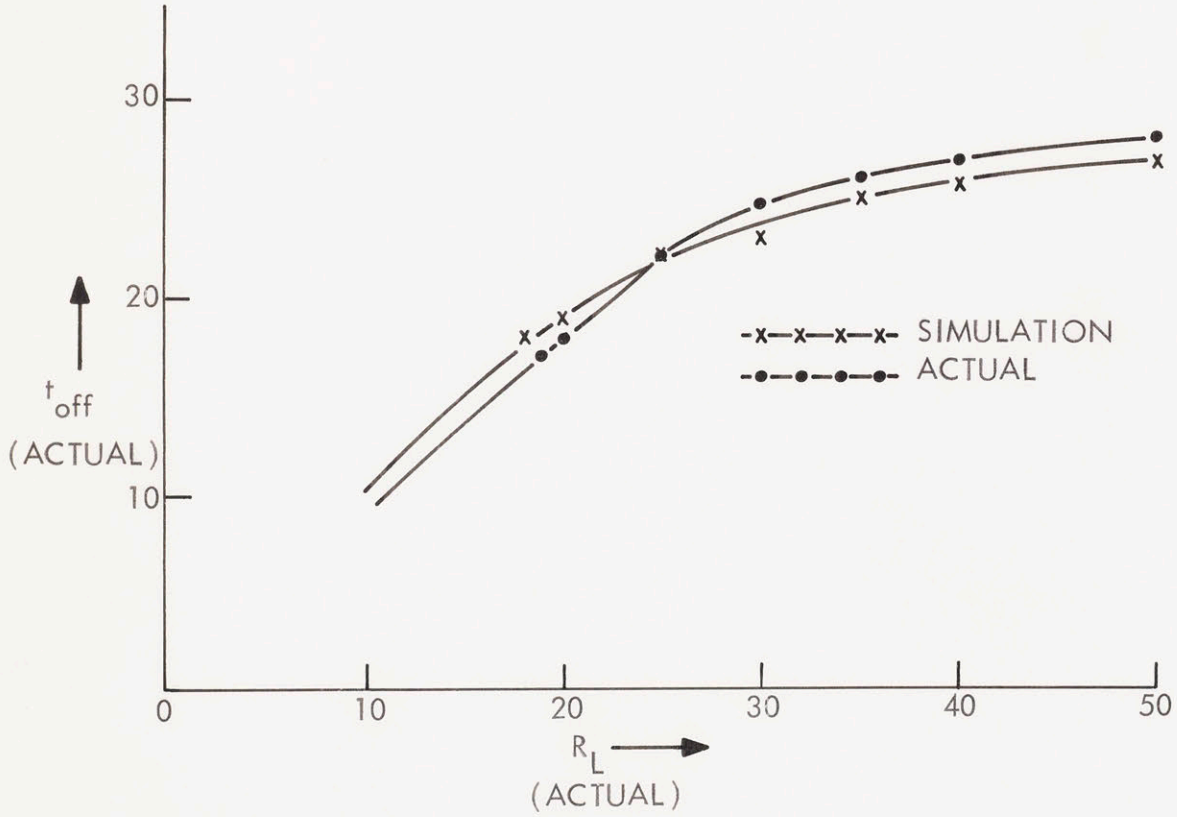


Fig. 7.3.4(b) Turn-off Time versus Load Resistance

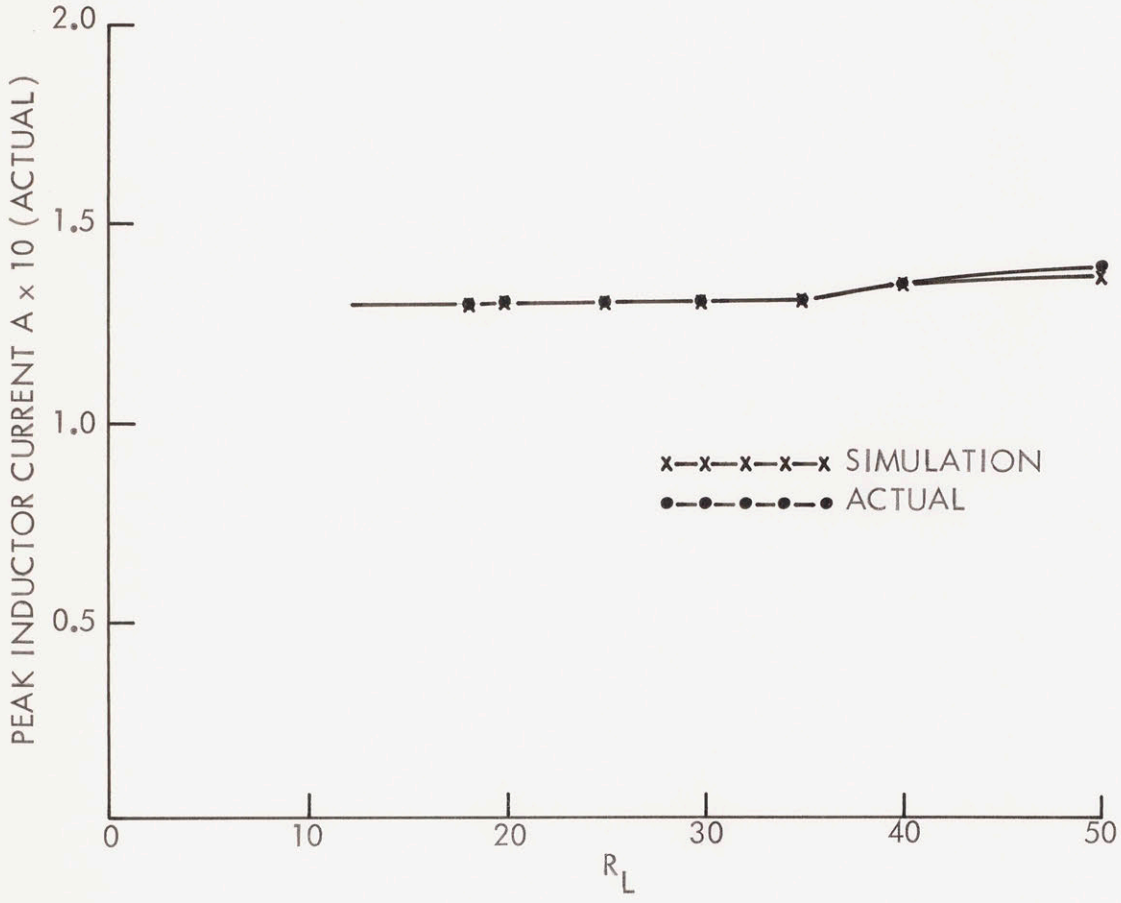


Fig. 7.3.4(c) Peak Inductor Current versus Load Resistance

and actual circuit performance.

7.3.7.3 Sensitivity Analysis

The series inverter was operated at various values of load resistance; the load being varied from infinity down to a relatively low value of 13Ω, where the inverter ceased operation. It was decided to investigate the mechanism of operation for low values of load resistance on the simulation, and hence to empirically determine the new values of inductance and capacitance so that the circuit would operate consistently with a load resistance of 5Ω.

For the purpose of analysis, the circuit is represented by a parallel resonant circuit (Fig. 7.3.5) excited by a unit step, whose response is calculated. On going through the equations, the current i_1 (Fig. 7.3.5) is given by:

$$i_1 = e^{-t/2\,R_L C} \sin \omega_o t \qquad (7.3.5a)$$

$$\text{where} \quad \omega_o = \sqrt{\frac{1}{LC} - \left(\frac{1}{2\,R_L\,C}\right)^2} \qquad (7.3.5b)$$

A Wang #600 Computer and its associated plotter were used to solve the above equations and obtain plots for various values of R_L. (The Subroutines for the solution is given in Appendix 1.) Of course, this is for the ideal case, assuming no losses in the energy storage elements. Figure 7.3.6 illustrates the response for various values of load resistance. Low values of the load resistance R_L destroy the Q (Quality Factor) of the circuit and create a finite DC offset. This results in

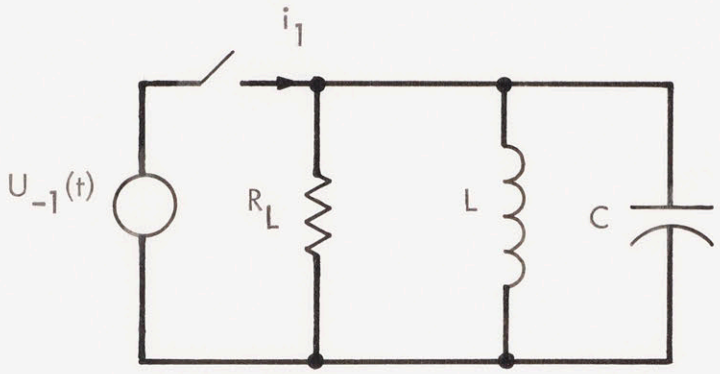


Fig. 7.3.5 Parallel Resonant Circuit

$L = 7.6$ Henries

$C = 33.3\ \mu F$

$250 < R_L < \infty$

$$i_1 = e^{-t/2R_L C} \sin \omega_o t$$

$$\omega_o = \sqrt{\frac{1}{LC} - \left(\frac{1}{2 R_L C}\right)^2}$$

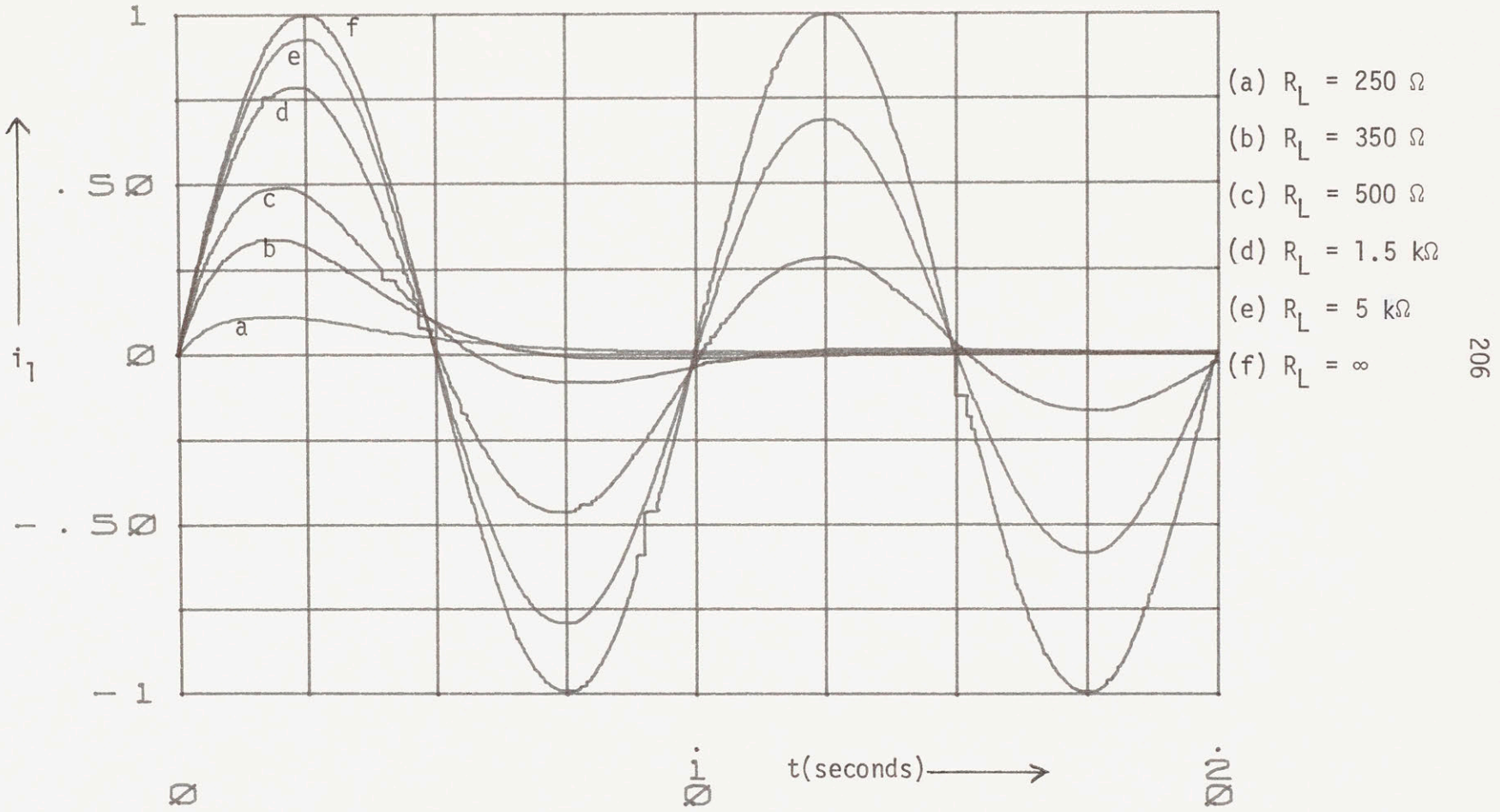


Fig. 7.3.6 Response of a Parallel RLC Circuit for Variations in Load Resistance R_L

the oscillatory current ringing about an average DC value given by $\frac{V}{R_L}$ (Fig. 7.3.7) which ultimately becomes large enough to prevent the thyristor current from ever crossing zero. This prevents the flow of reverse recovery current in the thyristor which consequently does not turn off. In other words, decreasing the load resistance decreases the diode current, which finally cease to flow, at which point the circuit ceases to function. Figure 7.3.8 illustrates the inductor current (thyristor + diode current) in the simulation, for a load resistance of 12Ω (1200Ω), where the resistance in paranthesis denotes the simulated value. The diode current is now extremely small, as the circuit is almost critically damped. Any further increase in load will cause commutation failure due to the above reason. The small ripple in Fig. 7.3.8 is due to the snubber current, which is now comparable to the diode current. Figure 7.3.9 graphically shows the variation of diode current with load resistance. At the value of 12Ω (1200Ω), it is seen that the diode current is a mere 50 μA; projection of the locus indicates that at 11.5Ω (1150Ω), the diode current is essentially zero indicating the absolute minimum load resistance for consistent operation. In the actual circuit, the minimum value for consistent operation is 13Ω (1300Ω), below which the circuit is relatively unstable; commutation failure positively occurs below 12Ω (1200Ω). Thus for consistent operation, the minimum load resistance as obtained from the simulation is 12Ω (1200Ω) which is in close agreement with the value of 13Ω (1300Ω) obtained from the actual hardware.

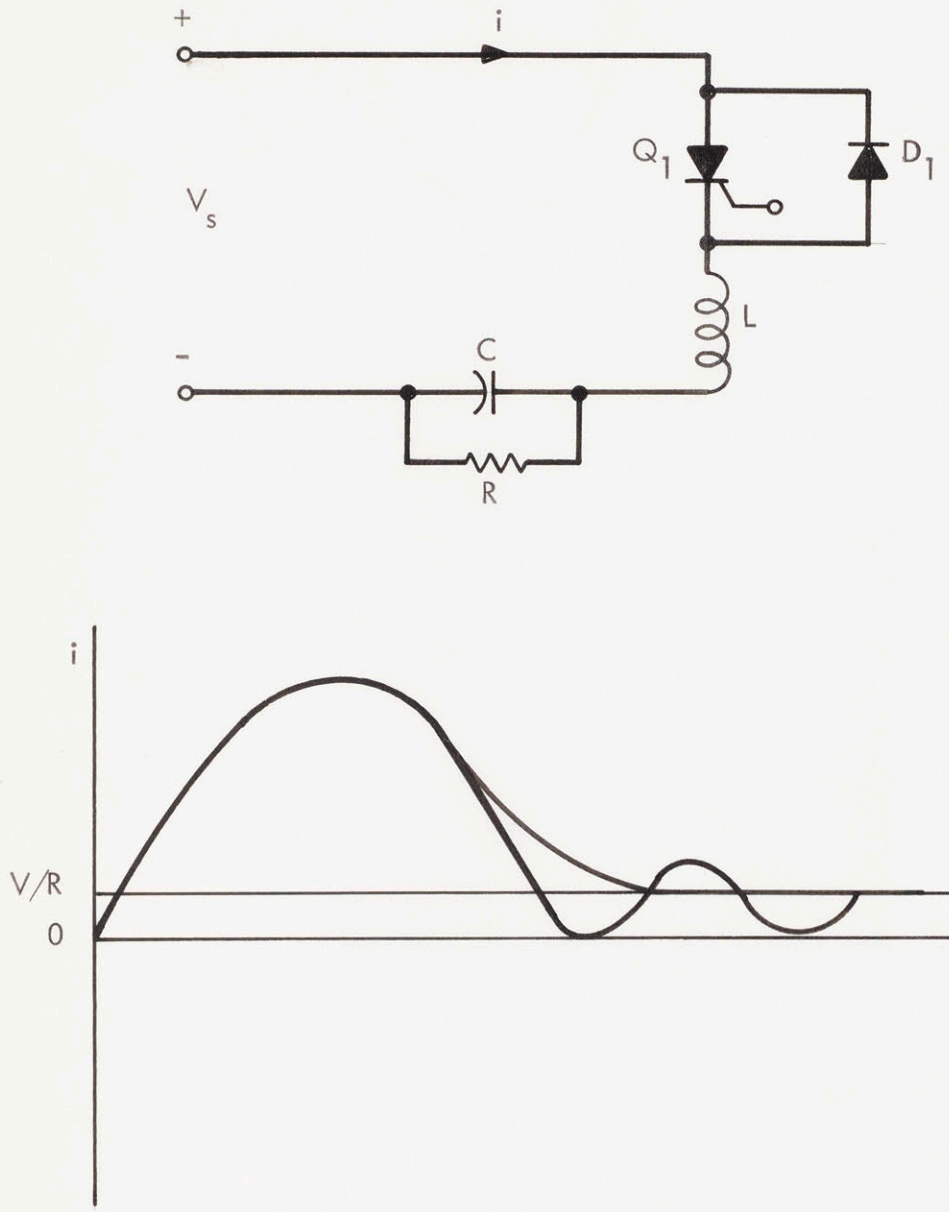


Fig. 7.3.7 Simplified Circuit and its Response for Very Heavy Loads

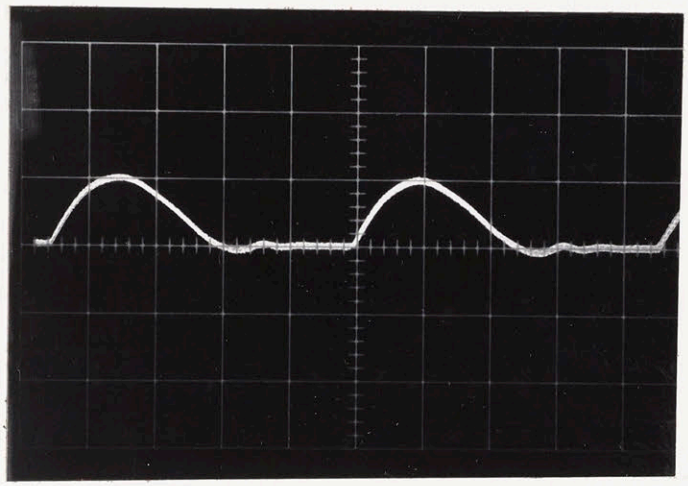


Fig. 7.3.8 Inductor Current in the Simulated Circuit for a Load Resistance of 1200 Ω.

Fig. 7.3.9 Diode Current versus Load Resistance in the Simulation

7.3.7.4 Inverter Operation with a 5Ω Load

The commutating inductance and capacitance were empirically changed in the simulation, such that the circuit would have the same resonant frequency, but would now accommodate a load resistance of 5Ω (500Ω). The final circuit values of L and C were 2.53 μH and 100 μF in the simulated network, which correspond to 10 μF and 25.3 μH in the actual circuit.

7.3.7.5 Snubber Circuits

The snubber circuit basically consists of a series connected resistor and capacitor placed in shunt with a switching device. The snubber circuit, in conjunction with the commutating inductance controls the maximum rate of change of voltage across the switching element when a voltage step is applied to it. In an analog computer simulation, incorporation of the snubber creates a stiff system which is not easily represented; however, the stiffness of a system is of no consequence to the Parity Simulator, as long as the frequency of oscillation is within the bandwidth of the element modules.

Snubbers were incorporated in the series inverter simulation. This was found to be responsible for the ringing seen in the inductor voltage and current waveforms in Fig. 7.3.2(b). The snubber capacitor is also responsible for the maximum rate of change of forward current $(\frac{di}{dt})$ that the thyristor is subjected to, and this occurs when the device just turns on. From the waveforms of Fig. 7.3.2(b) the various snubber circuit parameters are deduced as under:

$$\frac{dV}{dt} = 80 \text{ V/}\mu\text{sec}$$

$di/dt = 4.0$ A/μsec (with snubbers)

On removal of the snubbers from the Parity Simulation, a maximum di/dt of 1.3 A/μsec was obtained; this is only a third of the snubber di/dt. This shows the importance of incorporating the snubbers, since the snubber characteristics determine the maximum di/dt applied to the switching device, and the circuit designer has to make sure that this "snubber installed" di/dt is within the thyristor ratings.

CHAPTER 8

CONCLUSIONS

The primary purpose of this thesis was to demonstrate a totally new concept in the simulation of static energy conversion systems. Conventional simulation techniques have not been very effective in such system analysis. However, the Parity Simulation technique has demonstrated itself quite capable of accurately predicting such a system's performance. The outlook for the Parity Simulation technique looks very promising, and the future should see the gradual phasing out of the relative limited analog simulation approach, specially as the Parity Simulation concept is developed and explored further. Motivation will come from the end user, who has been continually demanding a "high performance" tool for detailed design studies of high power converter systems.

This chapter summarizes the key results of the study and also proposes the research that needs to be done for the system to be developed into a general purpose facility.

8.1 Summarized Results of the Parity Simulator

The advantages of the Parity Simulation technique have been discussed in Chapter 2, and it was shown that this technique provides a high degree of correspondence between the topology of the model and the topology of the actual system. Section 7.2 illustrated the difficulty of using an analog computer for simulation purposes and clearly showed the superiority of the Parity Simulation technique. Rapid "programming", ease of incorporating topological changes, and relatively lower costs

all helped to demonstrate the superiority of the Parity Simulation technique over its counterpart.

In Section 7.3, the sensitivity analysis of the series inverter clearly indicated the close correlation between the response of the actual circuit and the Parity Simulation. The critical parameters such as load voltage, turn-off time and peak inductor current all correspond closely to the actual values. Harmonic analysis of the load voltage also indicated the high degree of similarity between the simulated and actual circuit waveforms, the maximum error being a fraction of a percent when referred to the fundamental. Critical eccentricities such as snubber circuits have also been simulated and their effects have matched the actual snubber circuit effects.

8.2 Future Trends

Parity Simulation has already been demonstrated as a feasible concept for simulating static power conversion systems. However, to develop a general purpose Parity Simulation facility, extensive work needs to be done in several different areas. Foremost is the development of modules to model other types of elements; specifically models for rotating machines, coupled inductors, nonlinear reactors, etc. User interface is another area where some effort should be devoted. Input-output format, implementation of fault conditions, and determination of necessary protection equipment all require additional work. However, such a uniquely outstanding facility would certainly help to develop, enlarge and expand the capabilities of the existing system into a powerful tool for studying power conversion systems.

APPENDIX 1
WANG #600 Computer Subroutine

The following is the subroutine for the Wang #600 Computer and is used to solve equations (7.3.5a) and (7.3.5b) and returns a value of i_1 for a given value of R_L

```
0818   09 00     *     M
0819   06 04     f 4
0820   06 00     ST10
0821   06 15     ST15
0822   00 01     E1
0823   00 05     E5
0824   00 00     E0
0825   00 01     E1
0826   00 05     E5
0827   04 15     x15
0828   08 01     *  RE
0829   01 09     T9
0830   05 15     ÷15
0831   00 12     E12
0832   08 11     *  e^x
0833   06 02     ST2
0834   08 01     *  RE
0835   01 09     T9
0836   06 14     ST14
0837   08 15     *  1/x
0838   06 14     ST14
0839   00 01     E1
0840   00 05     E5
0841   00 00     E0
0842   00 01     E1
0843   00 05     E5
0844   04 14     x14
0845   08 12     *  x^2
0846   00 12     E12
0847   06 14     ST14
0848   00 03     E3
0849   00 09     E9
0850   00 05     E5
0851   00 01     E1
0852   00 10     E10
0853   00 03     E3
0854   00 02     E2
0855   02 14     +14
0856   08 13     *  √x
0857   06 14     ST14
0858   07 00     RE 0
0859   04 14     x14
0860   00 06     E6
0861   00 10     E10
0862   00 02     E2
0863   00 08     E8
0864   00 03     E3
0865   00 02     E2
0866   03 14     -14
0867   08 06     *  SN
0868   06 14     ST14
0869   07 02     RE 2
0870   04 14     x14
0871   09 15     *  RT
```

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