Peak Current Mode Driver for Thermoelectric Cooler

by

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S.B. in Electrical Engineering and Computer Science, Massachusetts Institute of Technology (2020)

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Abstract

Thermoelectric coolers (TECs) are solid state devices that use the Peltier effect to provide heating or cooling for an enclosed area when a voltage is applied. In order to both heat and cool, a bidirectional current must be supplied to the TEC. Therefore, a driver circuit is needed to supply the TEC with this bidirectional input. This thesis explores a design for an ultra-compact driver for a TEC that allows the system to quickly respond to disturbances, and efficiently maintain a precise temperature. Existing integrated TEC driver products currently do not meet the design targets set in this thesis. The products only operate up to 2 MHz frequency, are less than 90 % efficient, and are quite large. This motivates the design of an improved TEC driver. This thesis provides an investigation into a peak current mode controlled TEC driver architecture that operates at 5 MHz with a 2.7-5.5 V input, and supplies ± 1.5 A to the TEC. This TEC driver was targeted to achieve a 95 % efficiency, and will be incorporated with other circuity as part of an ultra-compact integrated circuit (IC) package design. After exploring various architectures, a peak current mode dual buck H-bridge TEC driver comprising the architectural blocks of a gate drive circuit, outer voltage loop, and inner current loop was designed. This design ensures that the targets of small size, high efficiency and stability are met. The experimental results, along with analysis and simulation of the design presented in this thesis demonstrate that this architecture can be used in TEC driver applications, and shows great promise for use in other applications due to its size and efficiency.

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Chapter 1

Introduction

Thermoelectric coolers are solid state devices used in applications where temperature stabilization, temperature cycling, or cooling below ambient temperature are required [5, 11, 6]. TECs can be used in either heating or cooling applications, depending on the polarity of the applied voltage (V). A TEC needs to be supplied with a bidirectional current (I) to be able to both heat and cool an enclosed area. As such, an electric circuit must be integrated into any TEC system to drive and control the TEC. The TEC driver architecture needs to operate efficiently to minimize power (P) losses, as well as quickly respond to any disturbances, to ensure a precise temperature (T) can be maintained. This thesis aims to develop a very efficient, high frequency driver for a TEC that will be integrated into a small IC package. The TEC driver is designed and simulated using Cadence Virtuoso, LTSpice and MATLAB, and is intended to operate as a temperature controller to heat and cool a laser system.

1.1 Background

Uses of TECs

Single stage thermoelectric coolers can produce a maximum temperature difference of about 70 °C, and historically have low thermo-electrical energy conversion efficiency due to inherent parasitic conduction losses [49]. The main drawbacks of TEC technology is thus the inadequate performance for high temperatures ranges [16]. For smaller temperature differentials however, the TEC efficiency is much higher [46]. TECs are therefore desirable for several applications such as photonics systems (e.g. industrial laser diode cooling, and laser transceiver modules), food & beverage cooling, and clinical diagnostic systems [42] where the required temperature range is small.

TECs are solid-state cooling devices and hence have the benefit of being lightweight and small - on the order of a few millimetres. They are flexible in design and thus can be easily integrated into systems or configured for many different applications [22]. Additionally, TECs have no moving parts - this lack of mechanical wear increases the lifespan of the system and lowers the maintenance requirements. TECs are thus highly reliable devices that have long lifetimes, and rarely experience failure due to mechanical vibration or stresses [6]. Another major advantage is that TECs are highly controllable. This means that they can respond quickly and achieve a precise temperature.

A further reason for using TECs is its environmental benefit. Many conventional cooling systems utilize hydrochloroflourocarbons which contributes to global warming and detrimentally impacts the environment [13]. TECs are much more environmentally safe than other cooling units in the market. Therefore, there is a need for research into and development of more efficient TEC driver architectures to ensure the diversification into more environmentally-friendly cooling/heating technologies.

Operation of TECs

A TEC is a thermoelectric device that consists of an array of alternating p-type and n-type semiconductor materials situated between two thermally conducting plates (usually ceramics) [49]. These p-type and n-type materials are joined electrically in series, and thermally in parallel, to form semiconductor couples, as shown in Figure 1-1 below.

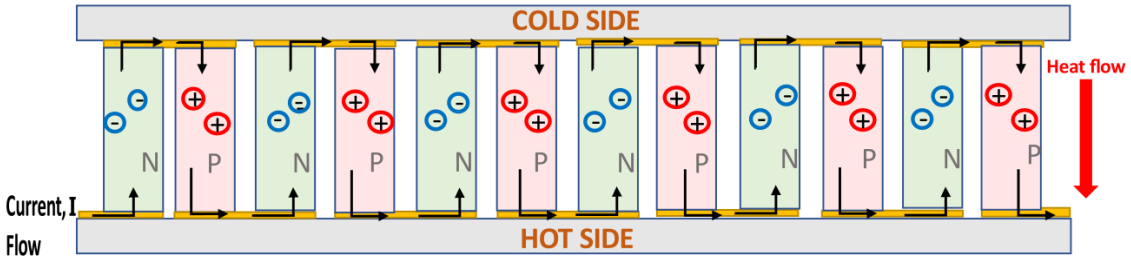

Figure 1-1: Array of p-type and n-type semiconductor couples of a TEC connected thermally in parallel and electrically in series, which allows current and heat to flow through the device.

The junctions of the TEC comprise dissimilar semiconductor materials. Therefore, when a direct current (DC) voltage is applied across the TEC terminals, a current flows across the contacts of the dissimilar conductors, and a temperature differential results. Heat is evolved at one junction and absorbed at the other. This phenomenon where heat is absorbed or dissipated when a current folows across a junction between dissimilar materials is known as the Peltier effect [16]. Figure 1-2 illustrates the Peltier effect phenomenon in an n-type material.

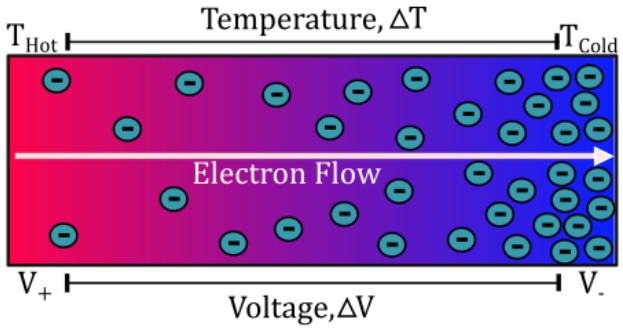

Figure 1-2: Peltier effect in an n-type material. When a voltage is applied, the electrons diffuse from the positive to the negative side, developing a temperature differential.

The Peltier effect creates a temperature difference by transferring heat between the two electrical junctions. The electric current due to the applied DC voltage drives charge carriers in the p-type and n-type materials. This carrier movement transports heat and results in a temperature difference across the ends of the TEC.

The Peltier coefficient (P_c) of a material represents how much heat is carried per unit charge (q) that passes through the junction. The different semiconductor materials in the TEC have complementary Peltier coefficients. Due to the different P_cs of the materials, the TEC acts like a heat pump and one surface of the TEC absorbs heat while the other gets heat deposited. The Peltier heat (Q_P) varies as a linear function of I.

$Q_P = P_c \cdot$ q, where:-

- q = I $\cdot$ time (t)
- $P_c = \alpha \cdot$ T where:-
  - The Seebeck coefficient (α) is the voltage generated per degree of temperature difference over a material.
  - T is the junction temperature in Kelvin [22].

When a DC voltage is applied across the TEC, a current is produced which drives the carriers in the p- and n-type materials. Heat flows in the same direction as the carrier flow. Thus, cooling occurs when a current is directed from n- to p-type material, while heating occurs when a current flows from p- to n-type material, as illustrated in Figure 1-3.

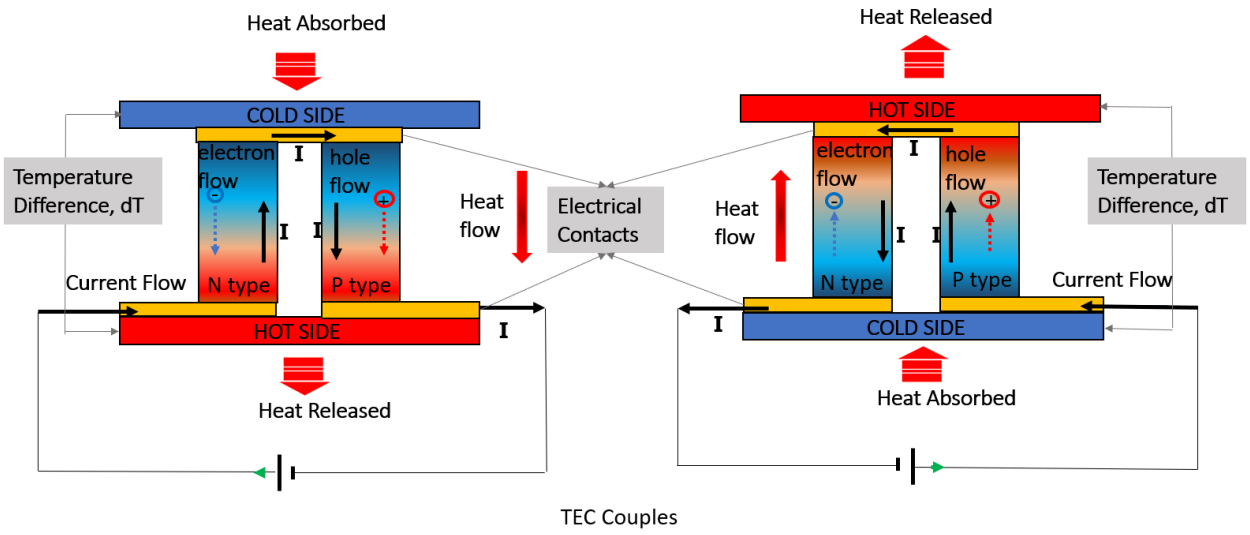

Figure 1-3: Bidirectional current, heat, and carrier flow in the semiconductor couples. Depending on the polarity of the applied voltage, the current drives the charge carriers which either carry or deposit heat from the top side to the bottom side of the TEC.

By exploring the energy bands of the semiconductor materials, the mechanisms for heat transfer in the TEC system can be better understood. According to Bohr's atomic model, each shell in an atom includes separate quantities of energy, at dissimilar levels. There are three main energy levels, the valence band, conduction band, and inner band. Semiconductors have fully occupied valence bands, and unoccupied conduction bands, with a small band gap between the two energy levels. This causes semiconductors to have conductivity levels in-between that of insulators and conductors. The valence band contains valence electrons which are held at the highest molecular orbital while the conduction band, has electrons that are loosely held by the atom. The conduction band electrons are referred to as mobile carriers as they can move around more freely. There is a band gap between conduction and valence energy levels, and for a semiconductor to conduct, the valence electrons require a certain amount of energy to be excited and move from the valence to conduction band.

In n-type materials, the conduction energy band lies above the hypothetical energy level of an electron i.e. the Fermi energy level. The Fermi level is usually found at the center between the valence and conduction bands. Hence, for an electron to leave, it must absorb energy. At one junction of the TEC, heat is absorbed from the environment. This heat is carried by electron transport to the other side of the TEC, where electrons are now at an energy level above the Fermi level. As the electrons move from a high- to low-energy state, they emit energy [5, 33]. Therefore, there is a decrease in temperature on the side where heat was absorbed, and a temperature increase on the side where heat is released. This allows

the TEC to heat/cool, as shown in Figure 1-4.

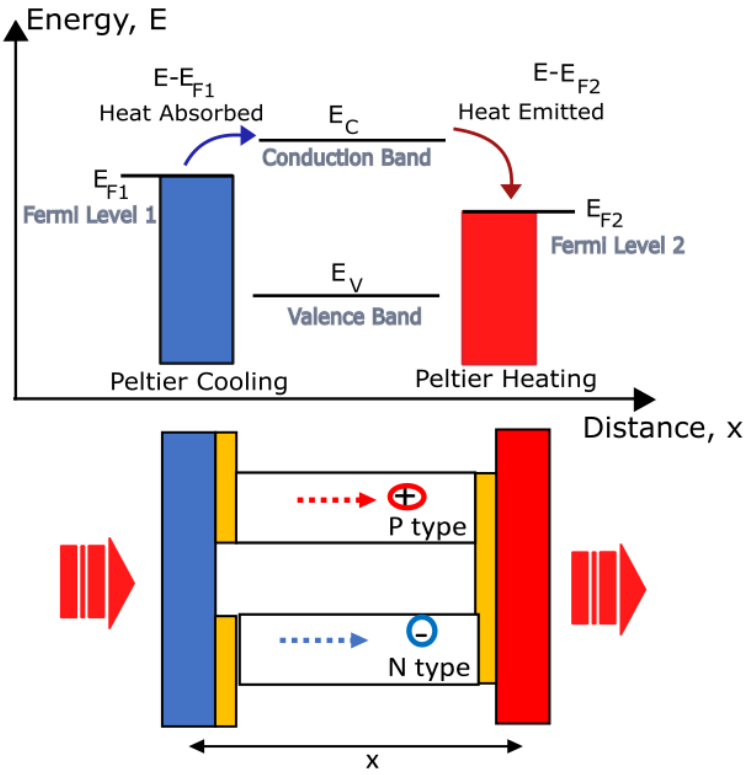

Figure 1-4: Electron movement across different energy levels as heat is absorbed/emitted in the TEC. Electrons absorb energy, and move from the left contact to the right contact, where they emit energy to the contact.

The complex device physics of the TEC can be modelled by an equivalent thermoelectric circuit model which separates the electronic domain (V,I), and the thermal domain (P,T), into two circuits [5, 50], which influence each other through I and V dependent sources.

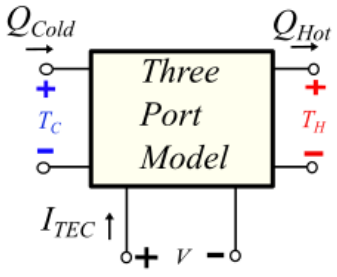

Figure 1-5: High level three port model of the TEC.

Figure 1-5 shows the three port model of the TEC where the bottom port connects to an electric circuit, and the left and right ports are the thermal connections to the cold and hot sides showing the Peltier heating (Q_{Hot}) and Peltier cooling (Q_{Cold}).

Table 1.1 summarizes the analogous meanings of each thermal and electrical component used in the thermoelectric and electric model of the TEC shown in Figures 1-6 and 1-7.

Table 1.1: Thermal and electric circuit analogs.

Thermal Variable	Electrical Variable
Heat Flow [W]	Current [A]
Temperature [C]	Voltage [V]
Thermal Resistance [K/W]	Resistor [Ω]
Thermal Mass [J/K]	Capacitor [F]

The thermoelectric model shown in Figure 1-6 shows the the Peltier cooling current source (Q_{PC}), Peltier heating current source (Q_{PH}), and Joule heating (Q_J), which is given by the formula $Q_J = I^2 \cdot R$ as dependent sources, It also shows the thermal capacitance (C_{TH}), and thermal resistance (R_{TH}) which model the thermal impedance across the TEC couples.

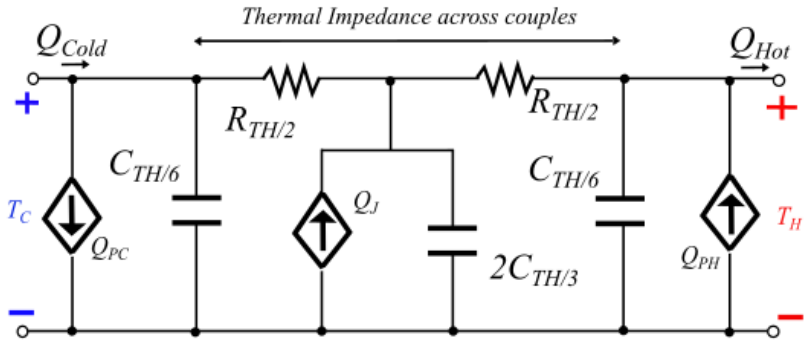

Figure 1-6: Equivalent thermal model of the TEC showing heat flow from left to the right.

The equivalent electric circuit model in Figure 1-7, shows that the voltage applied at the electrical port experiences the TEC resistance (R_{TEC}) in series with a voltage source which represents the Seebeck voltage that arises from the temperature difference across the TEC. The TEC's I-V characteristic is dominated by the resistive element and consequently, power varies with the square of I across the TEC.

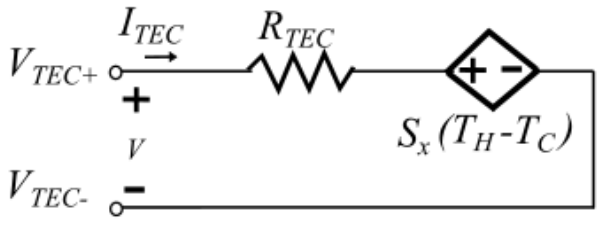

Figure 1-7: Equivalent electric circuit model of the TEC. A voltage applied across the terminals produces a temperature differential due the the Peltier effect.

1.2 Project Motivation

This thesis aims to develop a novel, high-performance TEC driver. This driver will aid in making TECs a more popular heating/cooling technique as opposed to conventional cooling techniques that negatively impact the environment. The main motivations for designing a new TEC driver are simplicity, power savings, and size reduction. This new driver architecture strives to create a highly efficient, controllable, system in a small package size.

The driver will operate off an input voltage (V_{in}) ranging from 2.7 to 5.5 V and supply a output voltage (V_{out}) ranging from -0.95V_{in} to +0.95V_{in}, producing maximum output current (I_{out}) of ± 1.5 A. It will run at a switching frequency (f_{sw}) of **5 MHz**, to allow smaller component sizing, and ensure fast system response. It further aims to provide greater than 95 % efficiency (η), by reducing power losses, and minimizing current ripple (ΔI).

The driver must provide bipolar voltage and current capability so that the TEC can be used to both heat and cool. In order to ensure the TEC can heat/cool to a precise temperature, the driver must also ensure that the system can respond quickly to any disturbances and input changes. The TEC product must also be of a small form factor so that it can be easily incorporated into the desired laser photonics application system [51]. The TEC driver will eventually be a part of an ultra-compact IC, as illustrated in Figure 1-8 below.

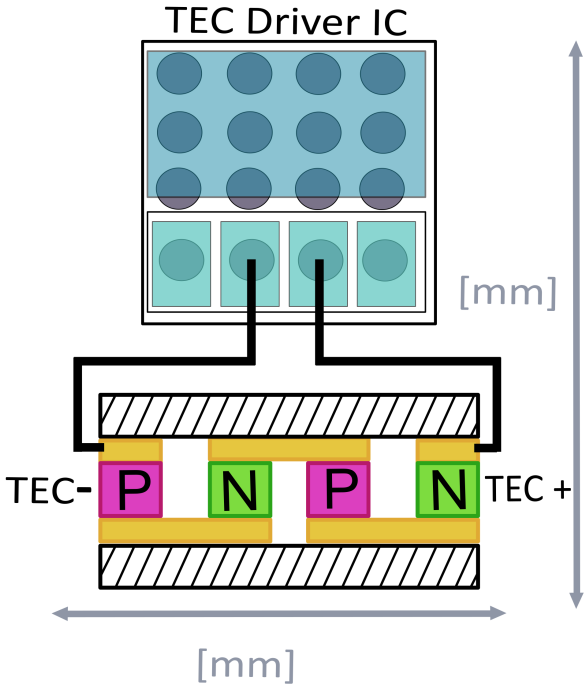

Figure 1-8: Ultra-compact IC package containing the TEC driver circuitry at the top, with the TEC device connected at the bottom.

1.3 Literature Review

A number of integrated TEC products have been developed commercially. However, each product was designed for a different application and hence has varying specifications, operating conditions, and design architectures. Table 1.2 below compares existing TEC drivers with the design targets for the TEC driver in this thesis.

Table 1.2: Comparison of existing TEC driver products.

Product	**V_{in}** (V)	**I_{Out}** (A)	**f_{sw}** (MHz)	**Package Size** (mm^2)	**Driver Design**	η (%)
LTC1923 (2001) [47]	2.7 - 5.0	1.0	0.26	5.0 x 5.0	Dual PWM H-bridge 2 external H-bridges 2 external inductors Voltage mode control	-
ADN8831 (2019) [7]	3.0 - 5.0	2.0	1.0	5.0 x 5.0	Linear & PWM drive 1 external H-bridge & 1 external inductor	≈ 90
ADN8833 (2018) [8]	2.7 - 5.5	1.0	2.0	4.0 x 4.0	Linear & PWM drive 1 external inductor	-
ADN8834 (2018) [9]	2.7 - 5.5	1.5	2.0	4.0 x 4.0	Linear & PWM drive 1 external inductor	-
ADN8835 (2018) [10]	2.7 - 5.5	3.5	2.0	6.0 x 6.0	Linear & PWM drive 1 external inductor	-
LTM4463 (2020) [48]	2.7 - 5.5	1.5	1.0	3.5 x 4.0	Linear & PWM drive 1 external inductor	≈ 90
MP8833 (2018) [36]	2.7 - 5.5	1.5	1.0	2.0 x 3.0	Linear & PWM drive 1 internal inductor Current mode control	≈ 90
Thesis (2021)	2.7 - 5.5	1.5	5.0	ultra-compact	Dual buck PWM coupled internal inductor Current mode control	> 95

The existing TEC drivers vary in size, operating frequency, employ different architectures and as such have different efficiencies.

The MP8833 [36] device has a small footprint, however it is only able to operate at a frequency of 1 MHz. Currently, the integrated TEC products on the market can only operate up to a maximum frequency of 2 MHz [8, 9, 10]. With this low f_{sw}, in order to limit the output ripple across the TEC and reduce power losses, these designs use large passive components (inductors and capacitors) to sufficiently filter and smoothen the output ripple. This causes the TEC products to have large footprints and package sizes.

In order to facilitate both heating and cooling, some of the different driver architectures used to supply the bidirectional voltage are: constant current drive, pulse width modulation (PWM) drive, and linear regulator drive. An H-bridge TEC driver circuitry is commonly utilized to provide the bidirectional current flow through the TEC. However, there is a wide variation in how the H-bridge circuitry is driven. In the ADN8833 and LTC1923 products [8, 47], the H-bridge circuitry is external to the IC package. This means that the actual footprint of the TEC driver is in fact larger than the dimensions stated in Table 1.2. Further, the user is forced to source the external components separately, which adds to the cost as well as impacts the system efficiency.

The LTC1923 [47] uses a dual PWM drive and a voltage mode controlled feedback scheme. However, this results in the need for a complicated type III compensation network to stabilize the system. The compensation network is also external to the IC package which again increases the footprint of the system. The dual PWM drive is implemented as two separate buck stages. This doubles the components needed, and increases the IC size.

Generally, linear regulators are less efficient than switching regulators. However, Analog Devices (ADI) uses a patented (US6486643B2) high gain linear regulator (LDR) stage [29] in the ADN8833, ADN8834 and ADN8835 [8, 9, 10] which is very efficient. Therefore, many of the new TEC products from ADI utilize a driver design that involves linear drive on one side and PWM drive on the other. Utilizing a linear regulator reduces the component count and makes the product smaller. However, in order to make the linear regulators with comparable efficiency to that of a switching regulator, the design becomes very complicated.

In addition to the bidirectional voltage supply, a feedback system is usually incorporated to improve the system stability. For the PWM driver side architecture, there have been many different designs for the feedback system. The LTC1923 [47] uses a voltage mode control scheme, while others used current mode control schemes. Each method has different advantages and drawbacks, so depending on the intended application for the TEC product, different control schemes were used.

None of the existing TEC drivers can operate at switching frequencies as high as 5 MHz, the package sizes are large, and efficiencies can be improved. There is thus a need for innovation to create a TEC driver that has higher efficiency levels, simpler design architectures, smaller package sizes, lower output ripple currents, and faster speed of operation. This thesis project aims to develop a TEC driver circuit that can overcome the shortcomings in existing TEC products.

1.4 Thesis RoadMap

This thesis is organized into ten chapters.

Chapter 1 introduces the background of TECs, presents a summary of previous work, and explains the motivation for the new driver design.

Chapter 2 outlines the target design goals/specifications for this novel TEC driver and highlights the potential challenges in achieving these design goals.

Chapter 3 describes the methodology used in selecting and designing this novel driver architecture. It provides an analysis of the trade-offs of different approaches, and explains the rationale behind, and operation of the major components of the new TEC driver designed in this thesis.

Chapters 4 - 10 analyze the design of each major subsystem in the **new TEC driver**. Simulation results illustrating the TEC driver's performance are presented for each block.

Chapter 4 provides mathematical modelling along with simulation data of the model for the new TEC driver architecture.

Chapter 5 describes the design, including components sizing and selection, for the buck power stage of this new TEC driver.

Chapter 6 describes the gate drive circuitry for this TEC driver architecture. It details the path of the PWM signal from the inner current loop to the power metal oxide semiconductor field effect transistor (MOSFET).

Chapter 7 describes the design and operation of the outer voltage loop of the novel TEC driver design. It analyzes the compensation network, error amplifier and voltage divider needed to stabilize the system.

Chapter 8 describes the inner current loop with emphasis on the current sensing architecture, comparator, and SR latch.

Chapter 9 evaluates the system, detailing the efficiency calculations, timing analysis, and stability analysis for the complete TEC driver system.

Chapter 10 concludes with a summary of the novel TEC driver architecture that was developed as well as the design targets that were set forth in the project. Recommendations for the further development of TEC driver circuits are also offered.

Chapter 2

System Design Requirements

2.1 Design Targets

The main design targets of the TEC driver developed in this thesis are:

1. 5 MHz speed of operation
2. $>$ 95 percent efficiency
3. Low current ripple (ΔI) through the TEC
4. Small package size and simple design
5. Large dynamic range for the differential voltage across the TEC
6. Good stability and fast transient response

By achieving the above targets, the new TEC driver will have good stability, improved simplicity, power savings, and size reduction.

This thesis aims to design a driver for a TEC that supports current sourcing and sinking to provide a bidirectional V_{out} up to $\pm$ 0.95V_{in}, and I_{out} up to $\pm$ 1.5 A from a V_{in} supply ranging from 2.7 – 5.5 V. This driver will then be part of an ultra-compact package-integrated design built in 0.18 μm process technology with an in-package inductor.

The core architectural decisions for designing a TEC driver that satisfies the above specifications involve macro-model decisions and transistor level design. At the macro-scale, the main decisions include control architecture design, stability analysis of the feedback system,

current sensing architecture design, and design of gate drivers. At the transistor level, each macro-block must be translated into 0.18 μm process technology so that sizing, transistor matching, timing analysis, as well as system efficiency and power losses can be evaluated.

2.2 Design Specifications

Table 2.1 below provides a summary of the specifications that this new TEC driver was designed to meet in this thesis project.

Table 2.1: Specifications for the TEC driver designed in this thesis.

Specification	Description	Value
V_{out}	TEC Output Voltage	$\pm 0.95 \cdot V_{in}$ V
V_{in}	Input Voltage	+2.75 to 5.5 V
f_{sw}	Switching Frequency	5 MHz
I_{out}	Output Current	$\pm$ 1.5 A
Package Size	Footprint of IC	ultra-compact
R_{TEC}	Effective TEC Resistance	3 Ω
D	Duty Cycle Range	95 % to 5 %
Process Technology	Semiconductor Technology	0.18 μm
μ	Target Efficiency	95 %
P_{out}	Output Power	8.25 W
Δ V_{out}	Output Ripple Voltage	30 mV
Δ I_{out}	Output Ripple Current	30 % max current

2.3 Potential Challenges

The design targets and specifications discussed in Sections 2.1 and 2.2 above pose several challenges that were carefully considered when creating the TEC driver architecture.

Firstly, TECs inherently have low efficiencies. Therefore, to achieve the high levels of efficiency needed to make TEC technology viable, all power losses must be minimized. For TEC applications, it is also necessary to minimize the ΔI and ΔV. The inductor current

ripple (ΔI_L) is given by the formula $\Delta I_L = \frac{D(V_{IN}-V_{OUT})}{f_{sw}L}$. Therefore, to reduce ΔI, either the inductor (L) or switching frequency (f_{sw}) must be increased. Increasing L allows for better filtering, but it increases the device footprint which conflicts with the design goal of minimizing the package size.

Consequently, a high operating frequency of 5 MHz was selected to reduce ΔI across the TEC. Reduced ΔI helps the inductor to not saturate as easily, and reduces devices stresses. This high frequency reduces the ripple while using smaller filtering components. Reduction in component size is very beneficial since it allows for a massive decrease in the area of the IC package. The smaller the package size, the larger the market demand for the product, since many applications which require precise temperature control but have limited space can now easily incorporate this IC.

Unfortunately, there are potential limitations for such a high frequency of operation. At high frequencies, parasitic inductive and capacitive effects become more pronounced and have a larger impact on the operation of the system. Another challenge is the duty cycle (D) limitations. A fast operating frequency means that the system has shorter times to settle and operate. However, the system has inherent limits on how quickly it can operate, that result from:

- the non-overlapping time between the turn on of the high and low-side MOSFETs
- the blanking time needed to avoid false triggering on switching transitions
- current sensing delays

These delays limit the range of achievable D and hence the dynamic range of the system. Therefore, the TEC driver must be designed to minimize the system's minimum on/off times.

In terms of package size, there are limitations on component sizing. Power electronics historically leverages the use of magnetics, in the form of inductors and transformers, to convert energy effectively [12, 21, 37]. However, in order make sure the driver fits into a small package size, these components need to be minimized. Reduction of the size of power MOSFETs further impacts the delay and power losses of the system. The small package size also places a limit on the number of pins that the IC package can have. Therefore, several tradeoffs are required to balance these metrics and achieve the desired system performance.

Chapter 3

Design Choices & Trade-offs

The TEC demands adjustable bidirectional current in order to heat/cool by varying degrees and maintain a precise system temperature. Due to ambient temperature variation and laser operation uncertainties, the TEC driver must be capable of either sourcing or removing heat and must therefore have a four quadrant operation as shown in Figure 3-1 below.

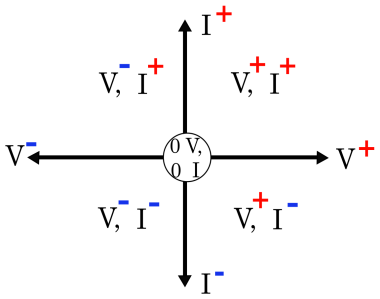

Figure 3-1: Four quadrant operation required to source and remove heat from the TEC.

The integrated TEC system must run from a fixed-range V_{in} (2.7 V - 5.5 V) and modulate this V_{in} to produce a variable bidirectional differential voltage across the TEC. A high dynamic range and output power are vital to allow the TEC to heat/cool across a wide temperature range. It is also imperative for power losses to be minimized since any difference in energy input to the system and energy output from the system is dissipated as heat. This excess heat combats the cooling process and hence results in a low efficiency.

The core components that need to be designed in the TEC driver architecture are:

- bidirectional current generation (Section 3.1)
- stabilization of the system (Section 3.2)

3.1 Bidirectional Current Generation

Voltage regulators are circuits that provide a variable output voltage from a fixed input source [12, 21, 37]. There are two major classes of regulator circuits that can produce variable output voltages:

- Linear regulators
- Switching regulators

These regulators are explored in Sections 3.1.1 and 3.1.2, while the different configurations of these regulators are investigated as methods of providing bidirectional current in Sections 3.1.3 to 3.1.4.

3.1.1 Linear Regulators

Linear regulators [21] use linear techniques to modulate the input supply to produce an output voltage. A transistor operating in the linear regime is placed in series between the input supply and output load. The transistor acts as a variable resistor- its resistance varies according to the load, and produces a constant output voltage. When creating a desired output voltage, the transistor drops the excess voltage across itself. Linear regulators therefore require the input voltage to be higher than the output voltage.

Though linear regulators are a simple and cheap solution to step-down the input voltage, they are normally inefficient. Power is continuously dissipated as heat since the difference between the input and output voltages, and the output current, are constant. This continuous power dissipation constitutes a significant portion of the power output, leading to massive inefficiency. Linear regulators can be designed to have a high gain so that the time during which current and voltage are both flowing through the device is reduced. This decreases the power dissipation, but adds to the complexity of the design.

3.1.2 Switching Regulators

DC-DC switching converters [12, 21, 37] convert a DC input voltage to a DC output voltage. They can generate output voltages that have opposite polarity or larger/smaller magnitudes from the input, unlike linear regulators. Switching converters use transistors, however, they are not held in a perpetually partially conducting (and therefore dissipative) mode. Instead, they are switched (turned on and off). The switches store the input energy temporarily and then release it to the output at a different voltage level. The fraction of the switching cycle for which the switch is on, the switch's D, therefore sets the amount of charge transferred

to the load. These converters are highly efficient since the switching element is either fully conducting with small on resistance or switched off having near infinite impedance [21].

Switching produces harmonics which cause electromagnetic interference (EMI) [12]. Filtering is needed to get rid of these harmful harmonics. However, this adds additional components and thus increases the device size. Fortunately, by increasing the f_{sw}, - the rate at which the switches are turned on and off, the size of the packets of energy being stored and distributed can be reduced. As a result, components' energy storage requirements can be made smaller.

Linear regulators provide benefits in size and cost, but switching regulators are more versatile and have higher efficiency.

The Buck Converter

The buck converter shown in Figure 3-2 is a step-down switching DC-DC regulator.

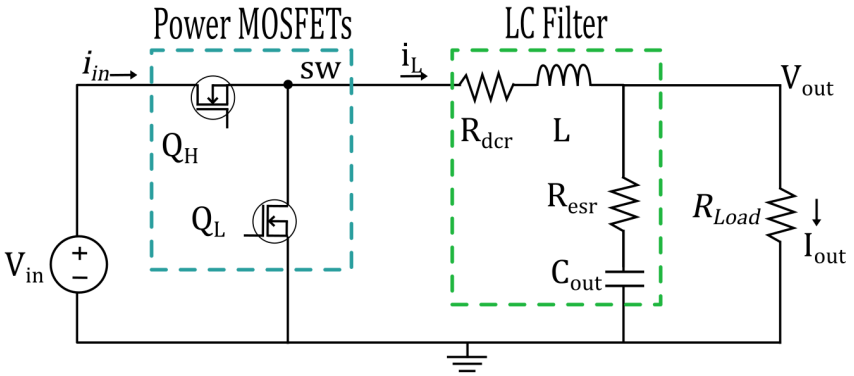

Figure 3-2: Step-down synchronous buck regulator circuit with an input voltage source, a pair of power MOSFETs which act as a pulse generator, a passive LC filter, and a load.

The switches are alternatingly turned on and off to produce a stepped-down output voltage across the load. The passive LC output filter removes harmonics and smoothens the output voltage across the load. This technique of using the pulse source and a reactive (non-dissipative) output filter allows the energy to be efficiently transferred.

In a simple open-loop case, for a given V_{in} and load, the $V_{out} = DV_{in}$. Therefore, the output is a function of the D and V_{in}. In order to able to heat/cool to a set temperature, the magnitude and polarity of the load current through the TEC must also be regulated. The duty cycle must therefore be a function of the load current. Closing the loop with a feedback scheme makes D dependent on the current flowing through the load and hence makes the TEC current/voltage controllable.

3.1.2.1 PWM Schemes

In order for DC-DC converters to produce variable outputs, the pulses applied to the switches must be controllable through pulse width modulation (PWM) techniques [18]. Therefore, the best method of generating the control pulses for the switching transistors is investigated in this section.

One of the the simplest ways to generate a PWM signal is the triangle-intercept [12], as shown in Figure 3-3 below. A ramp or triangular waveform, generated using an oscillator, and an input reference signal are passed to a comparator. When the value of the reference signal is greater than the ramp waveform, the output is pulsed high, else it stays low. The input signal is thus converted to variable-width pulses that adjust the on-time of the switches, with the percentage of on-time proportional to the ratio of the input waveform to the peak of the triangle waveform. The PWM technique impacts the common mode, noise, operating frequency, and ripple.

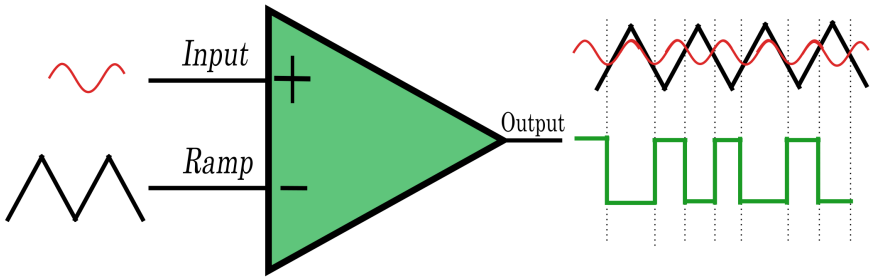

Figure 3-3: PWM generation using a comparator, input (red) and ramp modulation waveform (black) to produce a square-wave PWM signal (green).

The major categories of modulation techniques investigated in determining the best control waveform for the TEC driver included pure pulse width modulation (double-sided modulation with balanced triangle ramps) [12, 21, 37], and a combination of pulse-width modulation "class D" and linear modulation (classes A and B) [19].

Class D Modulation

The class D amplifier architecture explored [14] involves two half-bridge switching circuits that supply pulses of opposing polarities to the filter, as shown in Figure 3-4 (i.e., a full-bridge converter). The filter, which is connected to the TEC load, comprises two inductors and two capacitors. Each half-bridge contains two output transistors: a high-side transistor connected to the positive power supply, and a low-side transistor connected to the negative supply. The class D amplifier explored therefore operates like a dual buck converter.

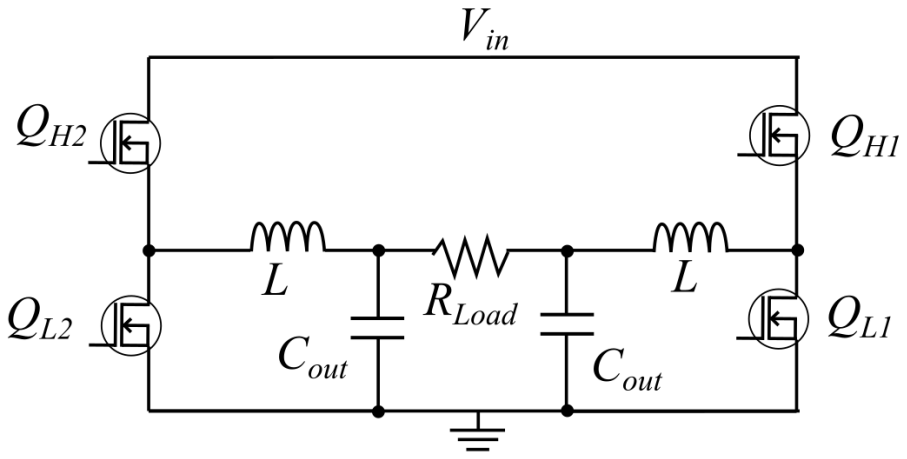

Figure 3-4: Class-D amplifier circuit showing the two half-bridge circuits with the TEC connected across the output of the two LC filters.

The PWM drive signals for the class D amplifiers encode information about a signal into a stream of pulses, and are produced using one of two modulation techniques, AD (traditional) or BD modulation.

Two Levelled Modulation (AD)

The AD modulation technique [14, 19] varies the duty cycle of the PWM input to the MOSFET gates such that its average content corresponds to the input analog signal. The input and modulating waveforms are passed into a comparator. The output of the comparator is then split, with one leg fed through an inverter and the other fed through a buffer. As shown in Figure 3-5, this creates two PWM signals, the A and B leg, which are the inverse of each other. These waveforms control the opposite sides of the H-bridge high-side MOSFETs. Because the switching waveform is nearly fully differential, a load across the A-leg and B-leg sees the entire switching waveform [19]. At nominal operation, the amplifier switches with 50 % duty cycle - causing significant current flow and power dissipation into the load. An LC filter is therefore necessary to reduce the current to a small residual ripple, to achieve high efficiency.

AD modulation has no significant common-mode switching content in its output. However, there is a common-mode DC voltage, equal to half of the supply voltage, due to the average value of the PWM switching. Since both sides of the load see this DC voltage level, it does not contribute to power dissipation across the load. Because this technique does not take advantage of the zero state voltage across the load network that is possible with a full-bridge topology, one gets higher ripple than is achievable for a given switching frequency. Consequently, this operating mode was not selected.

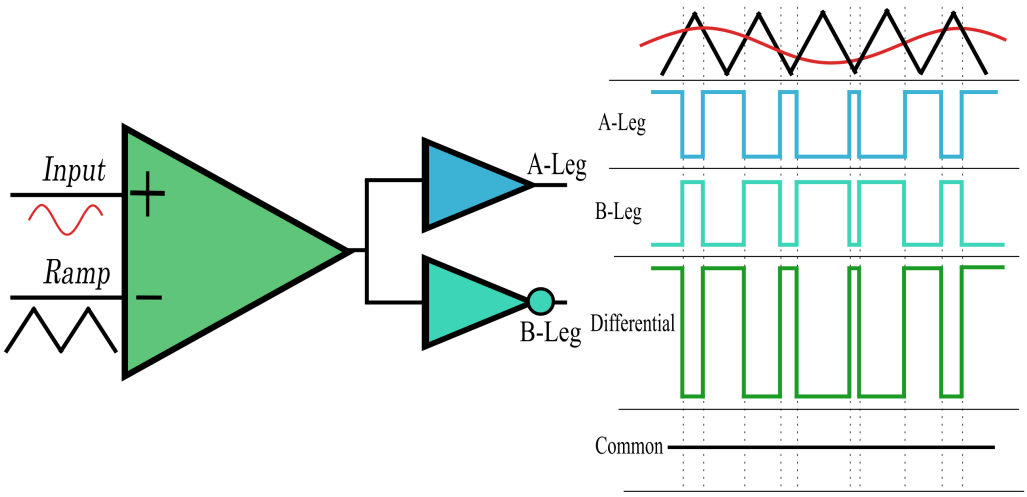

Figure 3-5: AD modulation circuit and resultant two-levelled ($+V_{in}$, 0) PWM waveform.

Three Levelled Modulation (BD)

This BD technique [14] modulates the duty cycle of the difference of the output signals such that its average content corresponds to the input analog signal. BD modulation creates a three levelled voltage ($+V_{in}$, 0, $-V_{in}$). The differential voltage that appears across the TEC is now double the frequency of the original input. This effective doubling of switching frequency is very beneficial as it reduces the current ripple across the TEC while allowing the filter components to be reduced [19]. Unlike AD Modulation, BD modulation has significant common mode content, as shown in Figure 3-6.

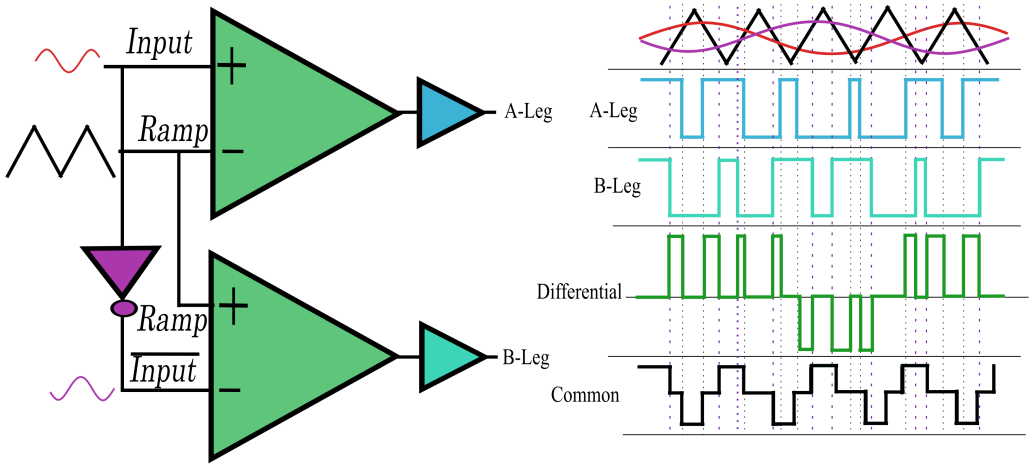

Figure 3-6: BD modulation circuit and resultant three-levelled ($+V_{in}$, 0, $-V_{in}$) waveform.

The resultant rail-rail common mode which varies as the PWM duty cycle varies, is a major issue. It causes the voltage across the load connected across the A and B leg to be sinusoidal- oscillating at the resonant frequency of the LC filter, $f_{LC} = \frac{1}{2\pi\sqrt{LC}}$. This

significant common mode content causes high EMI which produces undesirable noise in the system.

Figure 3-7 below shows a comparison of the AD and BD modulation schemes.

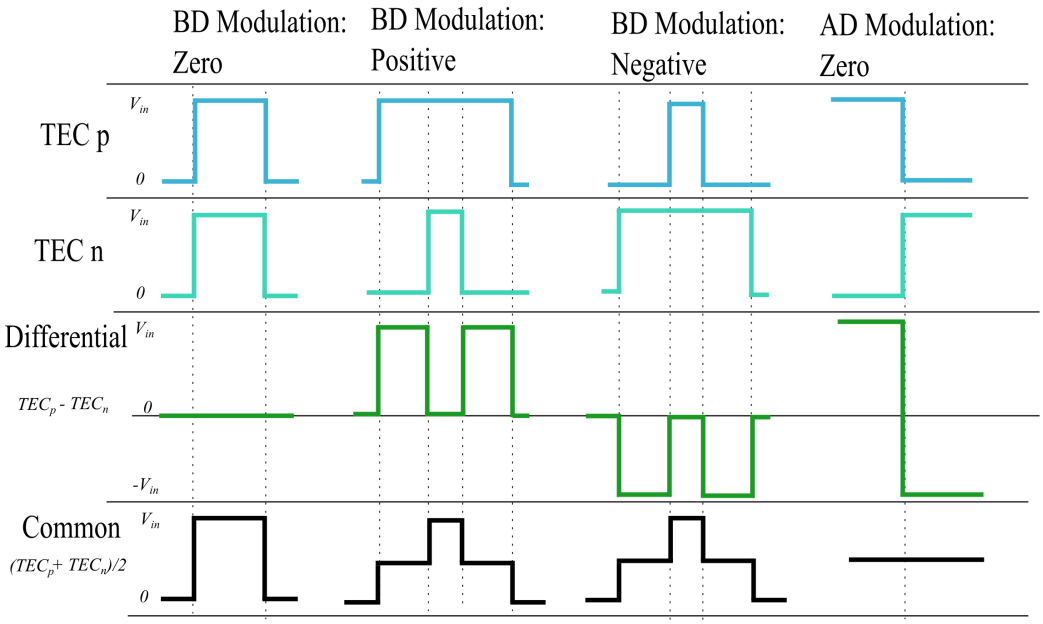

Figure 3-7: Comparison of AD and BD modulation PWM waveforms. They key differences are the common mode and differential waveforms.

AD modulation allows control over the common mode, while BD modulation has a doubling of the frequency but causes a sinusoidal oscillation because of the common mode swinging.

Another popular PWM technique involves using double-sided modulation with balanced triangle ramps and feeding the output of the comparator to a latch to produce the gate drive signal [12, 21, 37]. A clock signal set at the desired operating frequency, either sets or resets the latch. If the switch turns off, this PWM technique is referred to as "trailing edge modulation" whereas if the switch turns on, it is called "leading edge modulation".

Double-sided modulation based on clock trailing edge

When the control waveform exceeds the modulating ramp, the comparator output is pulsed high and the high-side MOSFET is turned off [12, 18]. A turn-on command is activated when the clock edge sets the latch, and when the PWM output of the comparator pulses high, it resets the latch, the high-side MOSFET turns off. The high-side MOSFET therefore turns on after the trailing edge of the clock, as shown in Figure 3-8.

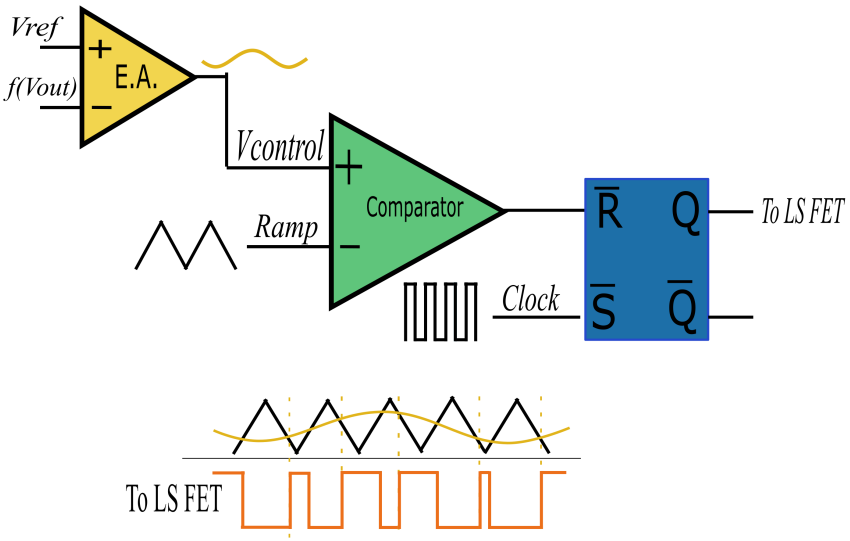

Figure 3-8: Trailing edge modulation operation and resultant PWM waveform (orange).

Double-sided modulation based on clock leading edge

If the control waveform exceeds the modulating ramp, the comparator output is pulsed high and the high-side MOSFET is turned on [12, 18]. A turn-off command is activated when the clock edge resets the latch, and when the output of the comparator pulses high, it sets the latch, and the high-side MOSFET turns on. The high-side MOSFET therefore turns off at the leading edge of the clock, as shown in Figure 3-9.

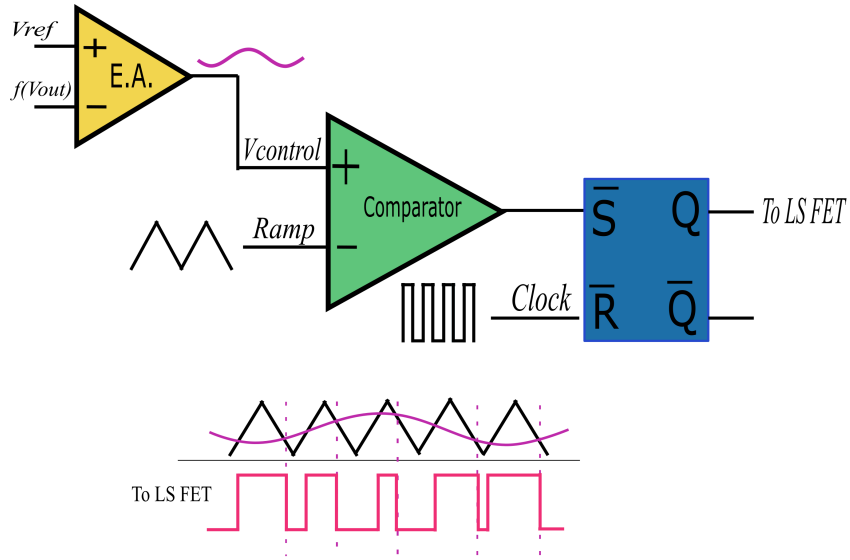

Figure 3-9: Leading edge modulation operation and resultant PWM waveform (pink).

This double-sided modulation with balanced triangle ramps results in better harmonic content for synthesized AC waveforms.

3.1.3 Buck-Linear Regulator Architecture

To provide bidirectional current to the TEC, a modified H-bridge driver circuit was designed where one side is driven by a high gain linear power stage and the other side is driven by a PWM-controlled buck converter.

Operation of Circuit:

A digital to analog converter (DAC) voltage is used as DAC reference voltage (V_{ref}) input to the system. It sets the duty cycle of, and hence output voltage for the buck, as well as the output of the linear regulator. We want the voltage across the TEC to have as large a dynamic range as possible in order to maximize the temperature range of the system. Therefore, the output voltage across the TEC was designed to span as close to rail-rail (V_{in} to -V_{in}) as possible. Since the V_{ref} is used to set V_{out}, it must be well mapped to the output voltage range. V_{ref} varies from 0.25 to 2.25 V, therefore, the midpoint of V_{ref} range, 1.25 V, was mapped to the midpoint of the V_{out} range to maximize the output voltage range.

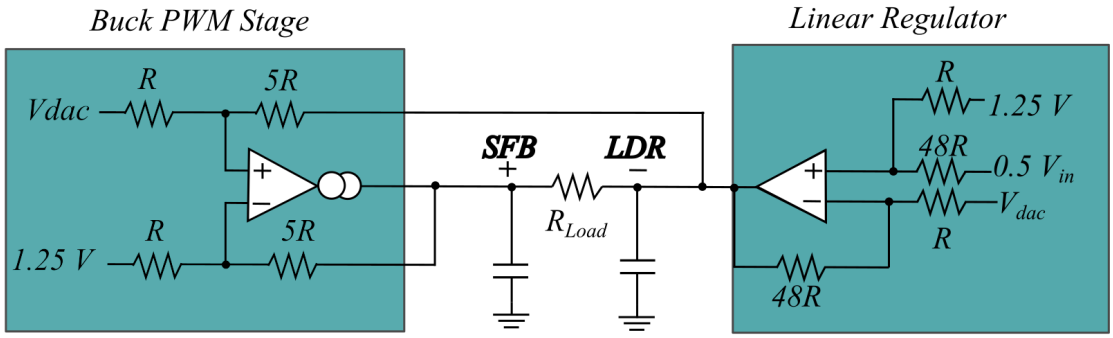

Figure 3-10: Single-ended buck-linear regulator architecture used to generate bidirectional current across the TEC. The voltage across the TEC is the difference of the buck stage output, SFB, and the high-gain linear regulator output, LDR.

In Figure 3-10 above, the buck stage is modelled by a voltage controlled voltage source and the linear regulator by an operational amplifier (op-amp). In the diagram above:

- The buck output (SFB) = D $\cdot$ V_{in}
- LDR is the output voltage from the linear regulator stage
- V_{ref} is the input reference voltage (0.25 to 2.25 V)
- V_{in} is the input supply (2.7 to 5.5 V)
- f_{sw} is the switching frequency, 5 MHz

In order to maximize the range of the current flow and achieve high temperature ranges, a large voltage differential across the TEC is required. The maximum current through the TEC occurs when there is ± V_{in} across the TEC. However, due to duty cycle limitations and minimum on/off times for the buck stage, a full swing of $+V_{in}$ to -V_{in} cannot be achieved. Instead, a voltage range across the TEC of ± 0.95· V_{in} was targeted.

The voltage difference across the TEC (V_{TEC}) = LDR-SFB. To achieve a large positive voltage, the buck stage's output, SFB, must be maximized, while to achieve a large negative voltage, SFB must be minimized. This means that in order to obtain a large dynamic range, high and low duty cycles must be achieved. Linear regulator and buck stage gains (S_{gain}, L_{gain}) were calculated in Appendix A to ensure that the maximum voltage swing of LDR-SFB can be achieved for the V_{ref} range.

The higher the gain of the LDR side, the faster the LDR side of the TEC output node traverses from high to low, minimizing the power dissipation. However, the maximum achievable gain is determined by the minimum on and off limits of the buck stage. L_{gain} was selected to be 48 while S_{gain} was set to V_{in}, to ensure the full range of duty cycles is traversed for the DAC range as shown in Figure 3-11.

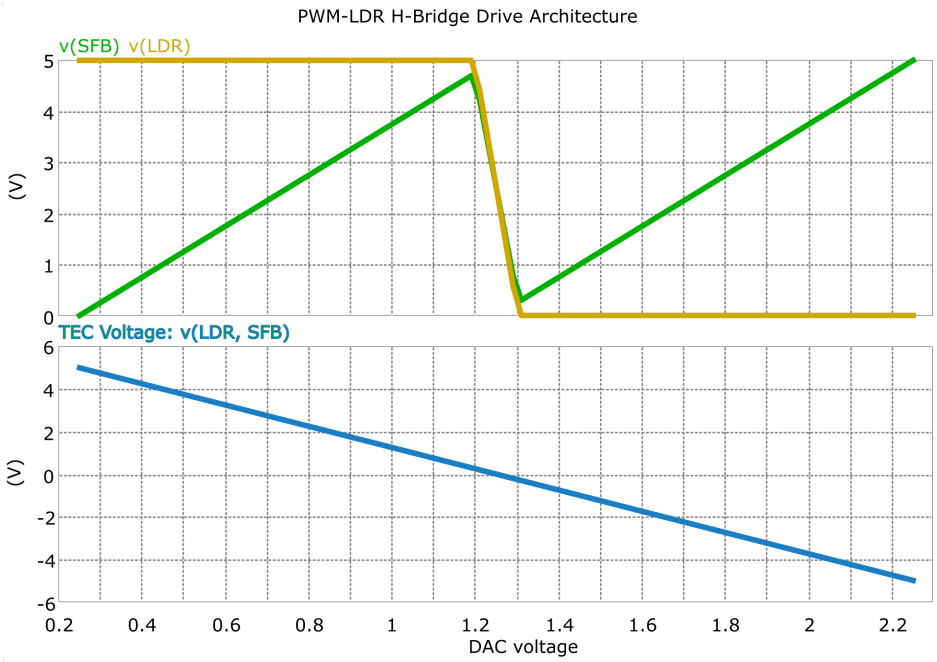

Figure 3-11: DC sweep of DAC voltage showing the resultant output TEC voltage range for the buck-linear regulator architecture. The ranges of the LDR (yellow) and the buck output, SFB, (green) are shown as the DAC reference voltage is swept from 0.25 to 2.25 V. The blue graph shows that the output voltage seen across the TEC spans the full ±V_{in} range.

3.1.4 Dual Buck H-Bridge Architecture

Figure 3-12 shows the dual buck H-bridge architecture. This circuit is highly efficient, since it is composed of switching DC-DC converters. However, it has a higher component count than the hybrid buck-linear regulator design. The voltage seen across the TEC is the difference between the outputs of two buck stages, hence the output is a fully differential signal. Usually, in a buck converter with a load-current step, the output capacitor supplies (or sinks) the immediate difference in current while the inductor current is ramped up or down to match the new load current. In this bidirectional circuit, the buck stage must now act as both a current source and sink, to achieve the desired four quadrant operation.

To allow the output voltage range of $\pm\ V_{in}$, the outputs of the two buck stages, V_{tec}^{+} and V_{tec}^{-}, must be 180 degrees out of phase. The PWM gate drive waveforms must therefore be inverted - when buck 1's high-side MOSFET is on, buck 2's high-side MOSFET is off and vice versa for the low-side MOSFETs. The symmetry of this architecture allows for the feedback/control process to be simplified. Since the bucks are complementary, current monitoring is only required on one side of the system and then an inverted copy can be created to act as the control for the other buck stage. With this design, the output common mode will be centred about $V_{in}/2$ ensuring that a wide dynamic range can be achieved.

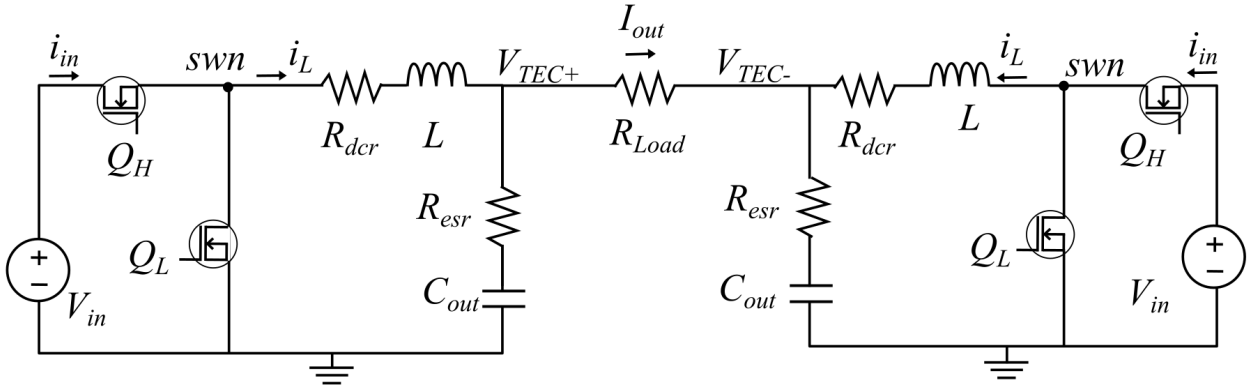

Figure 3-12: High-level block diagram for the dual H-bridge buck architecture used to generate bidirectional current in the TEC. The TEC is connected across the outputs of the two buck stages.

The hybrid linear regulator-buck circuit has lower efficiency and higher complexity. Therefore, this dual H-bridge buck concept was selected as the core of the bidirectional current generation block in the novel TEC driver designed in this thesis because of its high efficiency and simple design.

3.2 System Stabilization: Feedback Architectures

High accuracy and precision are at the centre of creating a stable TEC driver. A common and inexpensive way to ensure good system performance is to apply feedback and "close the loop". A closed-loop system feeds the output of the system back to the input to better control the system. It ensures high levels of stability, disturbance rejection, and good transient response.

There are many methods that can be used to design and implement feedback-controlled DC-DC switching converters. Linear analog control is the most widely used method, and is effective and economical. Digital control methods are good in principle, but impractical for high frequency systems because of the computation power required. Therefore, linear analog control methods were exclusively investigated for this high frequency application.

The two main PWM feedback control schemes that were investigated are:

1. Voltage mode control (VMC)

2. Current mode control (CMC)

Voltage mode control [12, 31], which was invented in 1976, revolutionized the power supply industry since its inception. Current mode control [12, 31, 39], which was introduced a couple of years later, has been widely used in switching converter stabilization. Each feedback scheme is operated based on different control variables - and their different implementations yield different advantages/shortcomings, as illustrated in the Sections 3.2.1 and 3.2.2.

3.2.1 Voltage Mode Control

VMC [32] is one of the most popular control methods due to its simplicity and effectiveness in regulating an output voltage given any changes in the load. It is based upon trailing edge modulation, where a turn-on command is activated at the clock edge, and a turn-off command is imposed when the output of the error amplifier intersects the ramp voltage, as shown in Figure 3-13.

A scaled-down version of the buck-stage output voltage is compared with a reference voltage through an error amplifier. The difference between the actual V_{out} and the desired output voltage is then used as an input to a controller. The output of the controller, a compensated error signal, is compared to against a large amplitude voltage ramp, which generates the PWM signal. An increase in the control voltage leads to a commensurate increase in duty cycle command. The control voltage thus directly controls D.

3.2.2 Current Mode Control

In CMC, the output voltage is compared to a reference voltage through an error amplifier, just like in voltage mode control. The output of the error amplifier is then compared with the peak current, and summed with a compensating ramp. An oscillator is used as a fixed-frequency clock, and the ramp waveform of VMC is replaced with the output inductor current. CMC is based upon the idea of creating a voltage-controlled current source that is programmed to ensure a constant voltage regardless of load changes. CMC is implemented using two feedback control loops. An inner current control loop that monitors the inductor current and creates this voltage-controlled current source, while an outer voltage loop monitors the converter's output voltage [25]. It constantly programs the controlled current source by providing a control voltage to the inner current loop. The control voltage therefore regulates the output voltage to a desired set point. A high-level block diagram of CMC operation is shown in Figure 3-13 below.

The current loop forces the inductor current to follow the error amplifier's output voltage. This converts the inductor into a quasi-ideal voltage controlled current source which removes its dynamics from the outer voltage loop. The complex double pole from the buck's LC filter can thus be approximated out - transforming the system to a first order system. Stabilization of the outer voltage loop is then drastically simplified since the complex poles become a single capacitive pole.

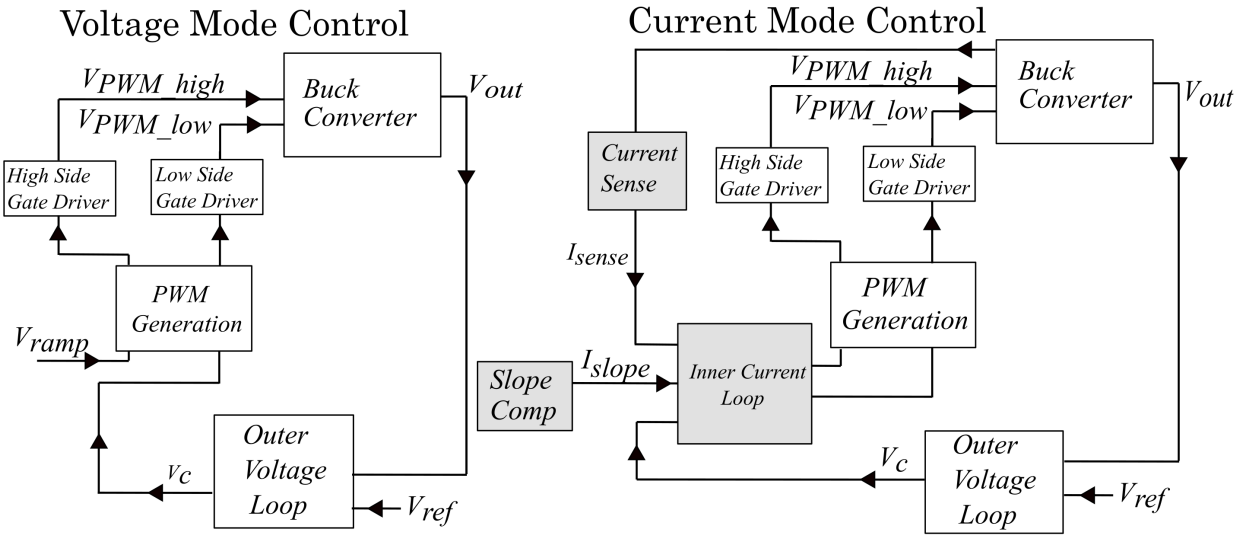

Figure 3-13: Comparison of current mode control and voltage mode control's high level block diagrams. The CMC block diagram has a more complex feedback loop but has inherent current-limiting capabilities.

CMC was was preferentially selected over VMC because despite its extra complexity, it resolves many of the issues that VMC faces, as illustrated in Table 3.1 below.

Table 3.1: Comparison of VMC and CMC's advantages and disadvantages.

Feature	**Voltage Mode Control**	**Current Mode Control**
Summary	PWM signal generated by comparing the voltage error signal with a constant ramp waveform	PWM is generated by comparing the voltage error signal with an inductor current waveform
Control Variable	Output voltage which is easily measured	Inductor current - additional circuitry is required to sense current
Feedback	One feedback loop - since only the output voltage is needed to stabilize the system, the design is simple and easy to analyse	Two feedback loops: Outer voltage loop and inner voltage loop. This makes the analysis more complicated.
Compensation	Requires complex Type III compensation to stabilize the complex poles from the buck output filter	Requires simpler Type II compensation. CMC eliminates the complex pole dynamics
Subharmonic instability	None	Yes - requires slope compensation to stabilize the system
Minimum On/Off Limits	None	Yes - due to blanking time needed to avoid ringing and current sensing time
Noise Margin	A large amplitude ramp is used which makes the system robust to noise	The small sense current generates the voltage ramp

Table 3.1: Comparison of VMC and CMC's advantages and disadvantages.

Feature	Voltage Mode Control	Current Mode Control
Current Limiting	Must be separately integrated	Has inherent cycle-by-cycle current limits
Dynamic response	Slower than CMC	Fast
Line Rejection	Bad/Slow - Line variations are sensed in the output voltage and are then corrected in the feedback loop. Therefore, there is a delay between the line variation and the duty cycle being adjusted. A feedforward term must be added to fix this.	Good - The inductor current which rises with a slope proportional to V_{in} - V_{out} adjusts quickly to line varations. CMC has automatic input-voltage feedforward.
Load Regulation	Good - it can significantly step-down the voltage and maintain good regulation for small-to-no loads	Load regulation is worse than VMC since the control loop is forcing a current drive.

The main types of current mode control schemes investigated were:

1. Peak current mode control (PCMC)

2. Valley current mode control (VCMC)

Peak Current Mode Control

PCMC [44], as shown in Figure 3-14 below, uses trailing edge modulation. The outer voltage loop's error amplifier forces the output voltage to be equal to the reference voltage. The error amplifier's output is then compared with the sensed inductor current. When the high-side MOSFET is on, the inductor current ramps up. When this current level exceeds the error amplifier's output voltage, the comparator outputs a high pulse. This high PWM pulse

resets the flip flop and terminates the charge phase by turning off the high-side MOSFET. It then initiates a discharge phase, turning the low-side driver on. The discharge phase continues until the next clock pulse sets the flip flop and then a new charging phase is initiated.

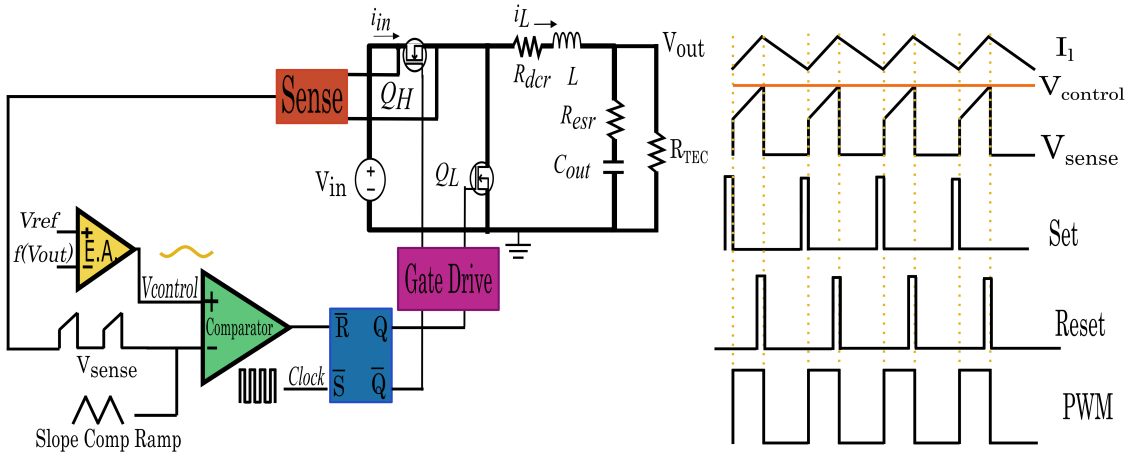

Figure 3-14: PCMC block diagram and resultant PWM control waveforms that are produced.

Valley Current Mode Control

VCMC [44], as shown in Figure 3-15, uses leading edge modulation. When the sensed inductor current falls below the error amplifier's output voltage, the PWM signal goes high. This sets the flip flop, initiating the charge phase by turning on the high-side MOSFET and stops the discharge phase by turning off the low-side MOSFET. The charge phase continues until the next clock pulse resets the flip flop, thus initiating a new discharge phase.

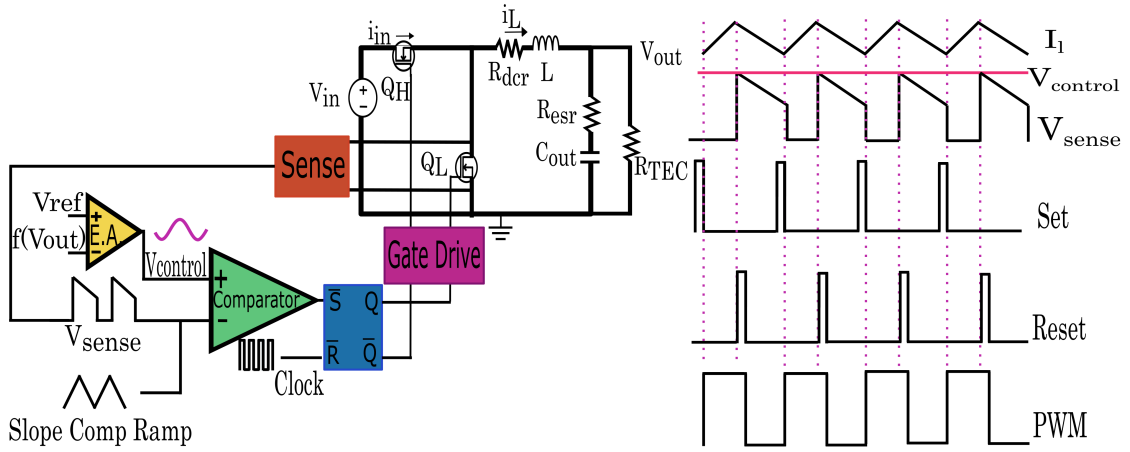

Figure 3-15: VCMC block diagram and resultant PWM control waveforms that are produced.

Peak current mode control was chosen as the feedback method for the TEC driver architecture because it provides inherent cycle-by cycle over-current limiting, short circuit

protection, good transient response, and simple feedback compensation as illustrated in Table 3.2 below. The instabilities that occur at duty cycles greater that 50 % can be overcome by slope compensation, and careful timing analysis will minimize duty cycle limitations [41].

Table 3.2: Comparison of PCMC and VCMC closed loop techniques.

Feature	**PCMC**	**VCMC**
Control Variable	High-side MOSFET current measured	Low-side MOSFET current measured
Subharmonic instability	Needs slope compensation for duty cycles > 50 %	Needs slope compensation for duty cycles < 50 %
Blanking time	Needs blanking time to avoid ringing on switching transitions of the high-side MOSFET	None needed since current is sensed during the off time of the high-side MOSFET
Duty Cycle Limit	Has a minimum on time, can operate at high duty cycles but cannot operate at low duty cycles	Has a minimum off time, can operate at low duty cycles but cannot operate at high duty cycles
Overcurrent protection	Yes	No
Line Variation	Fast	Slower

3.3 Novel TEC Driver Architecture Design Summary

After exploring various architectures, the TEC driver designed in this thesis will incorporate a modified dual buck H-bridge backbone with peak current mode control.

Figure 3-16, and the following list, describe the main blocks that were designed in this new TEC driver architecture in order to create a TEC driver that met the design targets and product specifications set in Chapter 2:

1. Buck Power Stage
    - Filter Components
    - Power MOSFETs
2. Gate Drive
    - Gate Driver
    - Bootstrap Circuit
    - Level Shifter
    - Non-overlap Timing Block
3. Outer Voltage Loop
    - Voltage Divider
    - Error Amplifier
    - Compensator Network
4. Inner Current Loop
    - Comparator
    - Current Sense
    - Slope Compensation
    - Set-reset (SR) Latch

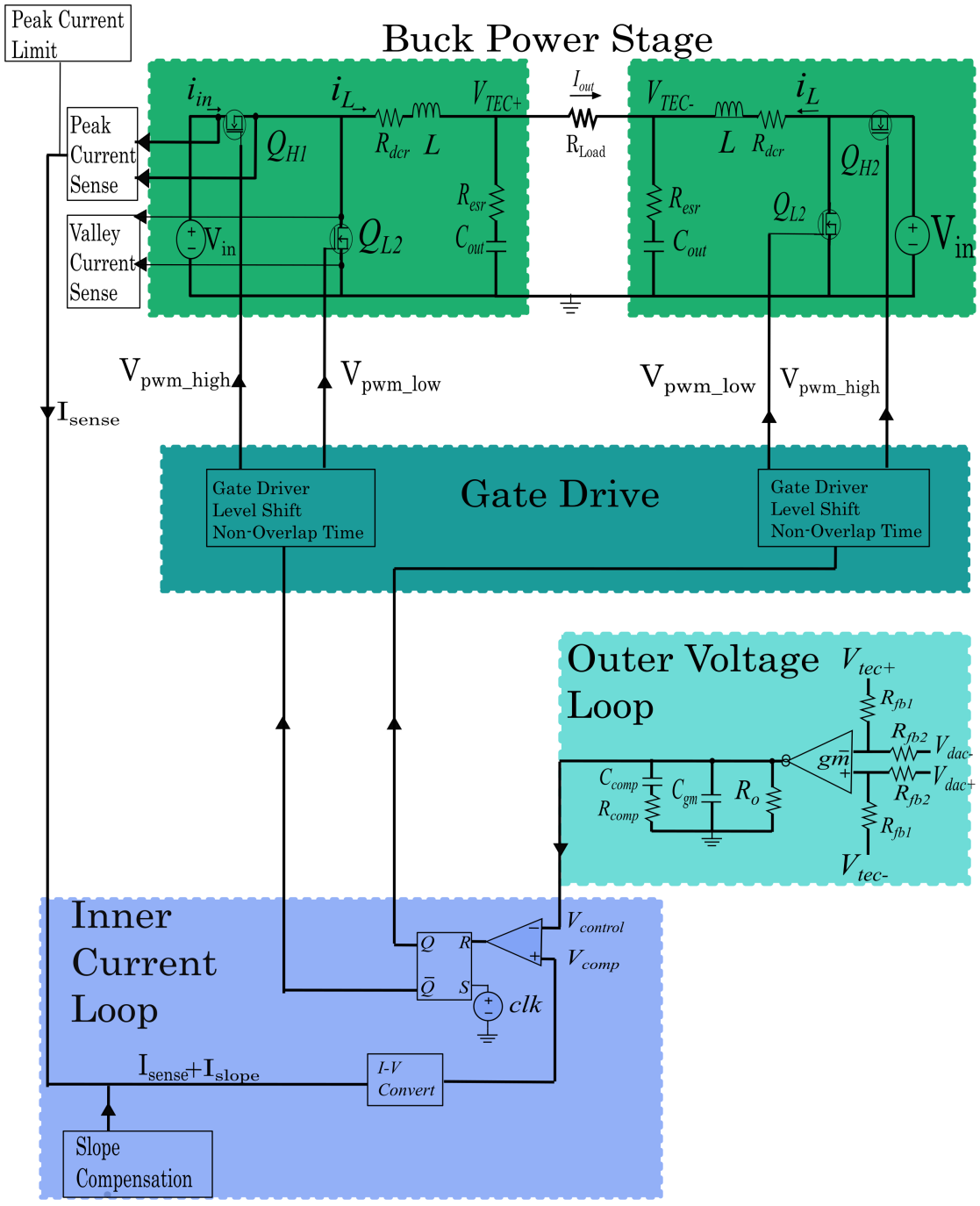

Figure 3-16: Novel TEC driver high-level block diagram. This diagram shows the 4 major blocks of the peak current mode TEC driver: the buck power stage, the gate drive circuitry, the outer voltage loop, and the inner current loop and describes how the blocks are interconnected.

Chapter 4

Peak Current Mode TEC Driver Model

Linear control theory [45] provides valuable tools for studying the dynamic performance of a converter. It enables the design of closed-loop feedback systems that compensate for any perturbations, and hence ensures fast, stable performance. DC-DC switching converters are non-linear time-varying systems [3]. The magnetic components have non-linearities [24] and the operating mode depends on the on/off state of the power MOSFET switches. Therefore, the supply is time-varying.

In order to apply conventional linear control theory, a linear time invariant (LTI) model must be developed. An averaged small-signal linear model, created by applying linearization techniques around an operating point, can then be used to characterize the behaviour of a control system for any deviations caused by dynamic transients in the system [53].

A DC-DC switching converter system is essentially a sampled-data system in the small-signal limit [24]. Hence, modelling of the open-loop and closed-loop PWM DC-DC converter system is necessary for dynamic and stability analysis [23]. Appendix B provides a detailed derivation for the transfer functions.

4.1 Open Loop Analysis

In order to analyze and design a stable, controllable system, the time-varying, non-linear system must be converted to a LTI model.

Step 1: Convert to Time Variant System

The buck converter has a three terminal PWM switching cell which includes an active

terminal (a), passive terminal (p), and common terminal (c). Terminals a and p are always connected to a voltage source while c is connected to the current source/inductor. During one switching cycle, there are two operating modes, when the high-side switch is on and when the high-side switch is off, as demonstrated in Figure 4-1 below.

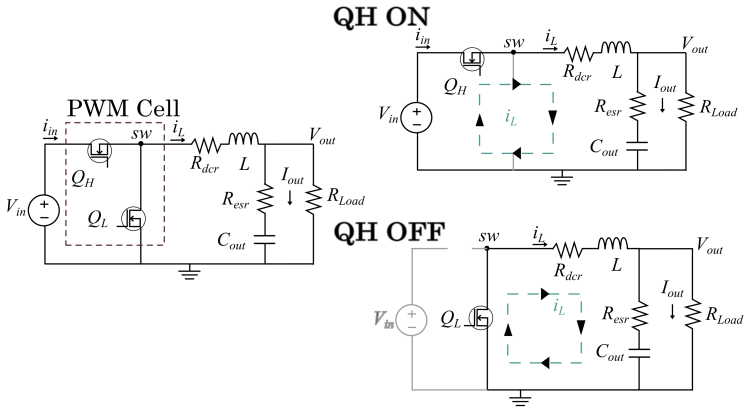

Figure 4-1: Operating modes of the buck converter. The high-side/low-side MOSFETs are alternatingly turned on/off, creating two operating modes.

The three terminal PWM cell can be averaged over one switching cycle, with the average switch current $= d \cdot i_L$ and the average switch voltage $= d \cdot V_{ap}$ as shown in Figure 4-2 below.

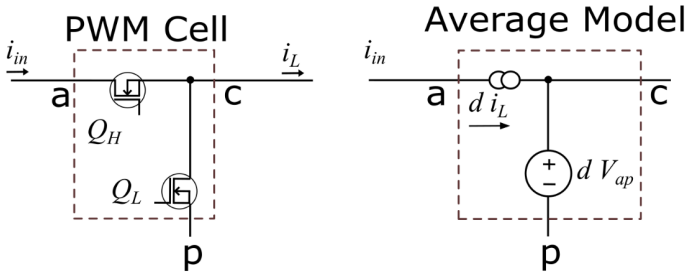

Figure 4-2: Conversion of the three terminal PWM cell to a time-averaged model.

Step 2: Linearize Model

The small signal model then needs to be linearized around a DC steady state operating point. Each signal, $x = \mathrm{X} + \hat{x}$, has a DC component, (X), and a small signal variation around that point, ($\hat{x}$). When two signals are multiplied, the steady state and alternating current (AC) quantities can be separated, and the higher order products of AC quantities can be ignored, since its contribution is negligible. $x \cdot y = (X + \hat{x}) \cdot (Y + \hat{y}) = X \cdot Y + \hat{x} \cdot Y + \underline{\hat{y} \cdot X + \hat{x} \cdot \hat{y}}$

Therefore,

$d \cdot i_L = \hat{d} \cdot I_L + \hat{i}_L \cdot D + D \cdot I_L$

$d \cdot v_{ap} = \hat{d} \cdot V_{ap} + \hat{v}_{ap} \cdot D + D \cdot V_{ap}$

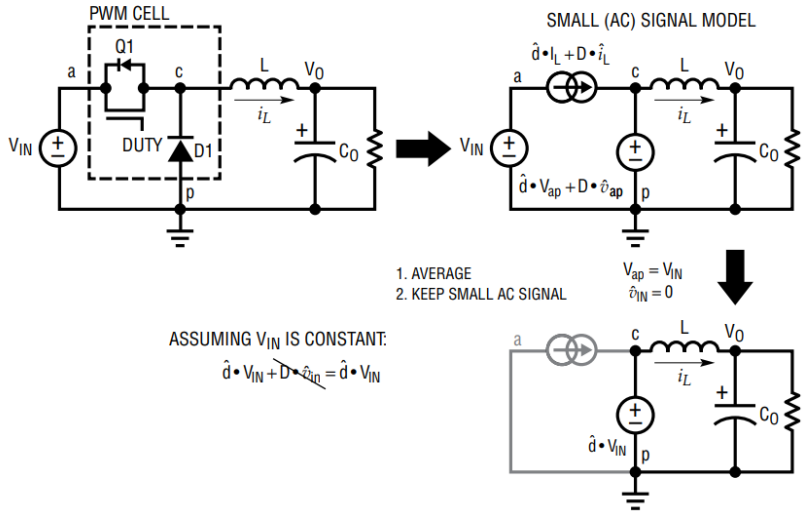

Figure 4-3: LTI model of the buck converter. Adapted from [53]. This linearized model is needed to design a closed loop feedback system.

As illustrated in 4-3 above, the buck converter can be modelled as a voltage source, $\hat{d} \cdot V_{in}$, connected to a LC output filter network. The outputs are inductor current and output voltage, and are affected by changes in duty cycle, input voltage and output current. Figure 4-4 below shows the block diagram representation of the system, highlighting the inputs and outputs of the system.

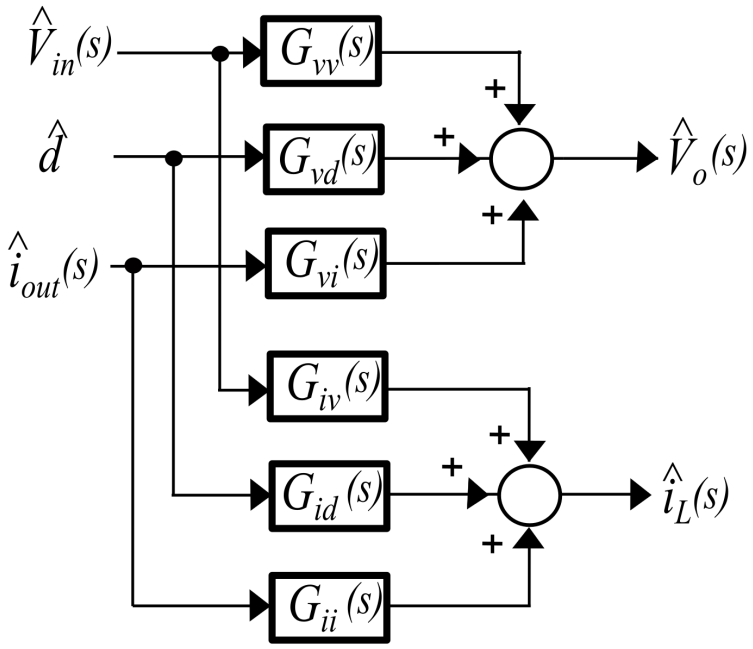

Figure 4-4: High-level block diagram for the buck converter.

Table 4.1 summarizes the transfer functions for the buck open loop system. The detailed derivation for these transfer functions is presented in Appendix B.

Table 4.1: Open loop transfer functions.

	Name	Description	Formula	Expression
1.	$G_{filter}(s)$	Buck Power Stage Output Filter	$\frac{\hat{V}_{out}(s)}{\hat{V}_{in}(s)}\Big\|_{\hat{V}_i=d=\hat{i}_o=0}$	$K_{filter}\frac{(s+\omega_z)}{s^2+2\xi\omega_0 s+\omega_0^2}$
2.	$G_{id}(s)$	Duty Cycle - Inductor Current	$\frac{\hat{I}_L(s)}{\hat{d}(s)}\Big\|_{\hat{V}_i=\hat{i}_o=0}$	$K_{id}\frac{(s+\omega_{z1})}{s^2+2\xi\omega_0 s+\omega_0^2}$
3.	$G_{vd}(s)$	Duty Cycle - Output Voltage	$\frac{\hat{V}_{out}(s)}{\hat{d}(s)}\Big\|_{\hat{V}_i=\hat{i}_o=0}$	$V_{IN}G_{filter}(s)$
4.	$G_{vv}(s)$	Input Voltage - Output Voltage	$\frac{\hat{V}_{out}(s)}{\hat{V}_{in}(s)}\Big\|_{\hat{V}_i=d=\hat{i}_o=0}$	$dG_{filter}(s)$
5.	$Z_o(s)$	Output Current - Output Voltage (Output Impedance)	$\frac{\hat{V}_{out}(s)}{-\hat{i}_{out}(s)}\Big\|_{\hat{V}_i=d=0}$	$K_{zo}(s+\omega r_l)\frac{(s+\omega_z)}{(s+\omega_{z1})}$
6.	$G_{vi}(s)$	Input Current - Input Voltage (Input Impedance)	$\frac{\hat{V}_{in}(s)}{\hat{i}_{in}(s)}\Big\|_{\hat{i}_{oi}=d=0}$	$K_{zin}\frac{s^2+2\xi\omega_0 s+\omega_0^2}{(s+\omega_{z1})}$
7.	$G_{iv}(s)$	Input Voltage - Inductor Current	$\frac{\hat{I}_L(s)}{\hat{V}_{in}(s)}\Big\|_{\hat{i}_{oi}=d=0}$	$K_{iv}\frac{(s+\omega_{z1})}{s^2+2\xi\omega_0 s+\omega_0^2}$
8.	$G_{ii}(s)$	Input Current - Inductor Current	$\frac{\hat{I}_L(s)}{\hat{I}_O(s)}\Big\|_{\hat{i}_{oi}=d=0}$	$G_{filter}(s)$

4.2 Closed Loop Analysis

The open loop system was stabilized by using feedback from PCMC to close the loop. Figure 4-5 below shows a high-level circuit diagram of the PCMC dual H-bridge buck TEC driver architecture.

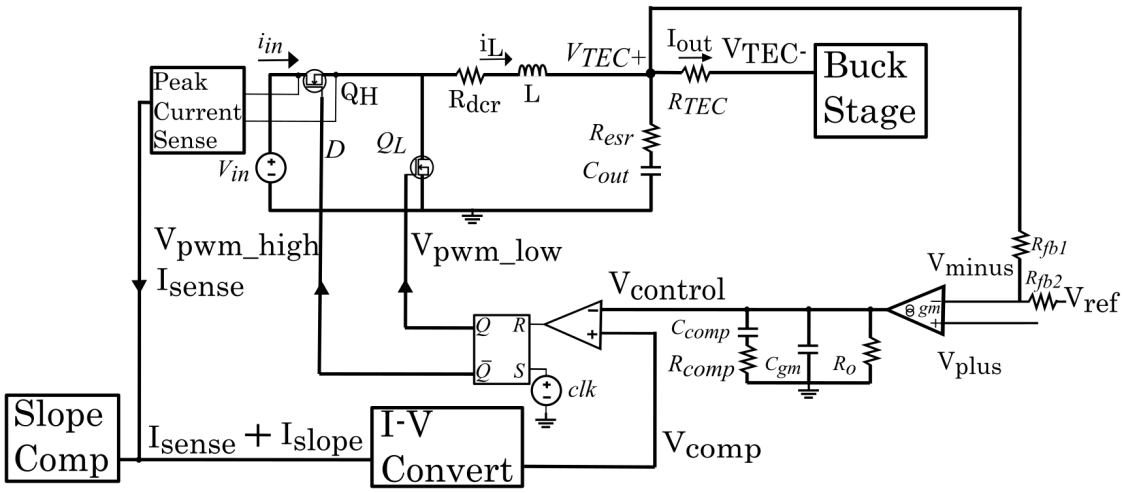

Figure 4-5: PCMC TEC driver control circuit diagram showing the closed loop system.

The circuit diagram shown in Figure 4-5 above can be modelled as the block diagram shown in Figure 4-6 below. The transfer functions were then derived from the block diagram.

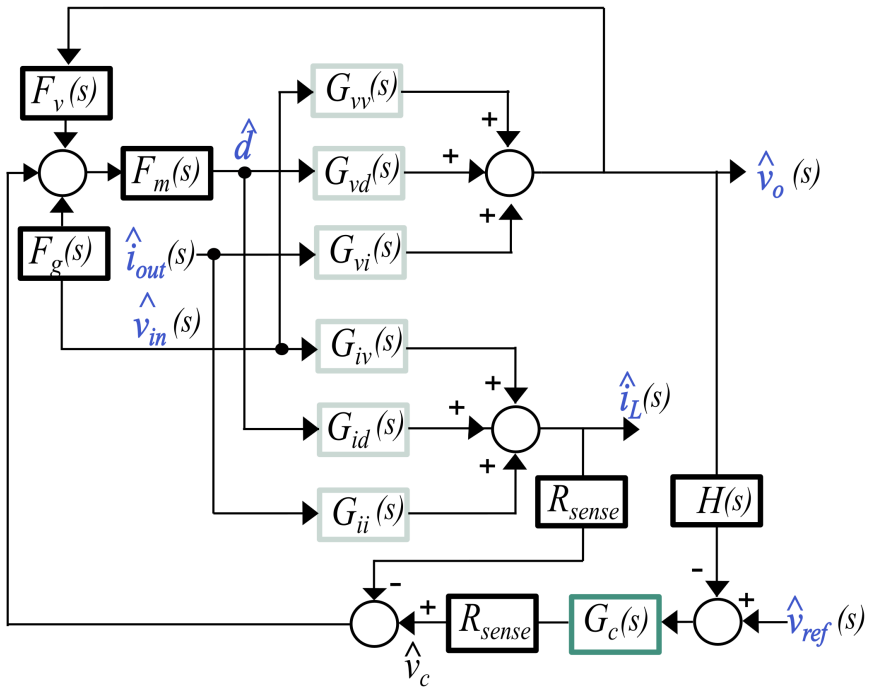

Figure 4-6: PCMC TEC driver control block diagram for the closed loop system.

Table 4.2: Closed loop transfer functions for the TEC driver.

	Name	Description	Formula	Expression
1.	$G_{vc}(s)$	Output Impedance	$\frac{\hat{V}_{out}(s)}{\hat{v}_c(s)}\Big\vert_{\hat{V}_i=\hat{i}_o=0}$	$\frac{F_m}{1+F_m G_{id}(s) R_{sense}} G_{vd}(s)$
2.	T(s)	Open Loop Gain		$G_{vc}(s) * G_c(s) * R_{sense}$
3.	$V_{ref,cl}(s)$	Closed Loop Reference-Output Voltage	$\frac{\hat{V}_{out}(s)}{\hat{V}_{ref}(s)}\Big\vert_{\hat{V}_i=\hat{i}_o=0}$	$\frac{G_{vc}(s)*G_c(s)*R_{sense}}{1+T(s)}$
4.	$Z_{o,open}(s)$	Open Loop Output Impedance	$\frac{\hat{v}_{out}(s)}{\hat{i}_{out}(s)}\Big\vert_{\hat{V}_i=\hat{v}_{ref}=0}$	$\frac{G_{vi}+R_{sense}F_m G_{id}(G_{vi}-\frac{G_{ii}G_{vd}}{G_{id}})}{(1+R_{sense}F_m G_{id})}$
5.	$Z_{o,close}(s)$	Closed Loop Output Impedance		$\frac{Z_{o,open}(s))}{(1+T(s)}$
6.	$V_{in,cl}(s)$	Closed Loop Line-Output Voltage	$\frac{\hat{v}_{out}(s)}{\hat{V}_{in}(s)}\Big\vert_{\hat{i}_{out}=0}$	$\frac{G_{vv}+F_m(G_{iv}H_e R_s G_{vv}+F_g G_{vd})}{(1+F_m(G_{id}R_s H_e-F_v G_{vd})+G_c R_m G_{vd})}$ $\frac{-G_{iv}R_s H_e * G_{id}F_m * G_{vd}}{(1+F_m(G_{id}R_s H_e-F_v G_{vd})+G_c R_m G_{vd})}$

The three closed loop transfer functions described in Table 4.2 are used to ensure that the system is stable in the face of any disturbances. The control-output transfer function, $G_{vc}(s)$, is needed to design the compensator of the outer voltage loop. This transfer function represents the "plant" for the system. By analyzing the open-loop crossover frequency and phase margin, a suitable controller was designed to stabilize the system.

The controller that is presented in Chapter 7 uses the information provided from bode plots of this transfer function to determine the phase boost required to develop a responsive, stable closed-loop TEC driver architecture.

The step responses which demonstrate the stability of the system are provided in Section 9.3.

Chapter 5

Buck Power Stage

The buck power stage comprises a pair of power MOSFETs, Q_H and Q_L, an LC filtering circuit, and a load, as shown in Figure 5-1 below.

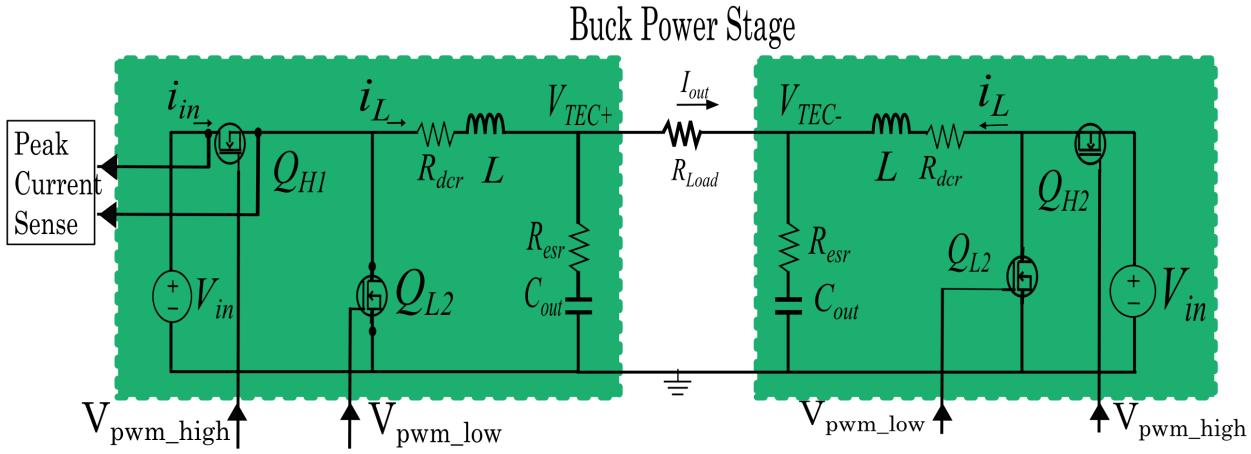

Figure 5-1: Buck converter power stage. Each buck stage (green) contains a pair of power MOSFETs that are controlled by PWM signals. The TEC is connected across the output of the LC filter from each buck stage.

These components were sized to ensure that the current density of the device was achievable and ensure that the following design targets were met:

1. Package size: ultra-compact design (on the order of mm)

2. Efficiency: low power dissipation (on the order of mW)

5.1 MOSFET Selection

In the TEC driver architecture, there are two buck stages and hence four power MOSFET devices that need to be sized. Each MOSFET is used in a buck stage, and hence these devices can be identical.

Electrons have higher mobilities than holes and as such, n-channel metal oxide semiconductor (NMOS) devices with the same performance, can be made smaller than p-channel metal oxide semiconductor (PMOS) devices [15]. Since this design aims to minimize the footprint of the IC, NMOS devices were selected as the switches.

When selecting the sizing of the MOSFET, the following tradeoffs were analyzed. Larger NMOS devices have:

+ more space for pillars and vias to facilitate current flow and heat dissipation in the IC package.

+ better current density which ensure the devices experiences less stress.

+ smaller on resistances which reduces the conduction losses and hence power dissipation.

− higher gate and output capacitance which increases the switching power losses.

− slower slew rates. These larger devices require larger gate driver circuitry to get fast slew rates for the switching transitions.

− a larger footprint which decreases the available space on the IC for other components.

The MOSFET, designed in 0.18 bipolar CMOS-DMOS (BCD) technology, was carefully sized to minimize power loss, whilst ensuring fast switching.

Package Size

The IC package for the TEC system was targeted to be much smaller than existing TEC driver products, hence all the system components must fit into a reduced area. The largest components are the magnetics, which sit atop the footprint, and the power MOSFETs.

The physical layout of the MOSFETs was determined using a model of a 16 pin wafer-level chip scale packaging (WLCSP) package, shown in Figure 5-2.

In order to manufacture the IC, a border on each side of the package is required. This further reduces the available dimensions. Additionally, the other system blocks require space.

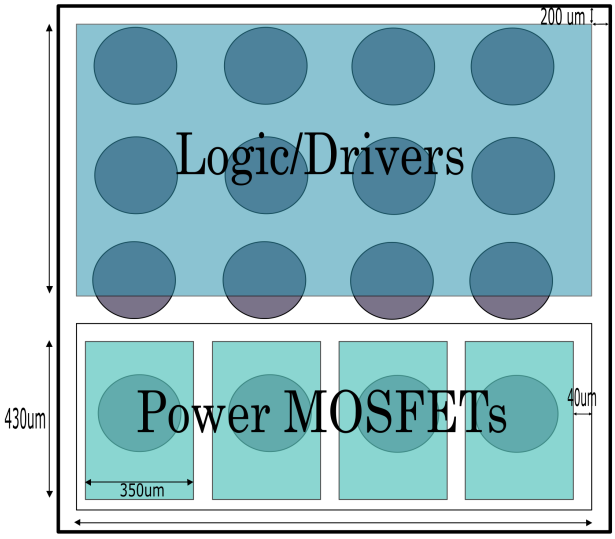

Figure 5-2: Package layout for ultra-compact TEC driver IC. The black circles represent the pins of the WLCSP IC package and the physical dimensions of the power MOSFETs must fit into the bottom section of the package since the upper portion is reserved for other driver circuitry.

Based on existing TEC products, an upper block was designated for the other architectural elements. Allowing for at least 40 μm of spacing between each MOSFET for interconnects and wiring, this further reduces the maximum MOSFET size to 430 μm x 350 μm, as shown in Figure 5-3 below.

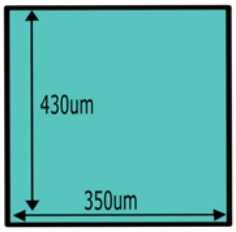

Figure 5-3: Maximum dimensions allocated for the power MOSFET footprint.

These physical dimensions provide a maximum limit on the MOSFET size. The MOSFET has four main parameters which were then adjusted to achieve the desired performance:

- NMOS channel width (W_n); NMOS channel length (L_n)
- fingers (f): Number of poly gates used; multiplier (m): Number of parallel devices

The X dimension is set by the number of fingers (f) of the device and the channel length (L_n). The more fingers, the more source terminals are shared, and hence the parasitic

capacitance of the MOSFET decreases. Using a minimum device L_n of 600 nm, a maximum finger size, (f) of 290 was selected.

The Y dimension is set by the channel width, (W_n), and the multiplier (m). The multiplier stacks m copies of the MOSFET vertically. These parallel MOSFETs split the current flow in each device and improves the current density. With a Y dimension of 430 μm and each width being 40 μm, the maximum number of multipliers was found to be 10.

Current Density

The MOSFETs have pillars and vias between the metal layers of the printed circuit board which brings current between layers. Assuming the current is evenly distributed, the current flow mainly runs vertically from the pad through the MOSFET. Therefore, we need to ensure that the device can withstand the maximum current required by the TEC without experiencing electron migration/breakdown. The current density (J) is given by the equation J = $\frac{I_{max}}{(m*f*W_n)}$. Maximizing the number of fingers, width, and multiplier creates a device that can tolerate higher currents.

For these selected parameters: W_n = **40 μm,** L_n = **600 nm, m= 10, f = 290**

The current density of the MOSFET devices was found to be:

J = $\frac{1.5e^3}{40*10*290}$ = 0.013 mA/ μm.

This current density ensures that the MOSFETs are not unduly stressed during operation when the maximum current flows, and will not experience any device failures.

Efficiency Analysis

The main sources of power loss in MOSFETs are:

- **Conduction Losses**
  - from the MOSFET drain-source on resistance ($R_{ds,on}$)
- **Switching Losses**
  - from the MOSFET's gate charge
  - from the MOSFET during switching transitions
  - from the low-side MOSFET's body diode

In designing the MOSFET, these losses were minimized to achieve a high efficiency.

When the MOSFET is conducting, power is lost as the current flows through the $R_{ds,on}$. This $R_{ds,on}$ of the power MOSFET varies with temperature (T), gate-source voltage (V_{gs}), and device size (W_n, L_n). Therefore, several simulations were run varying the temperature and device size to ensure the worst-case operating condition was still well within the power budget to ensure $>$ 95 % efficiency.

Figure 5-4 below shows the effect of increasing the multiplier and number of fingers on the $R_{ds,on}$. As the multiplier increases, and the number of fingers decrease, the resistance decreases. Therefore, the larger the multiplier, the lower the resistance.

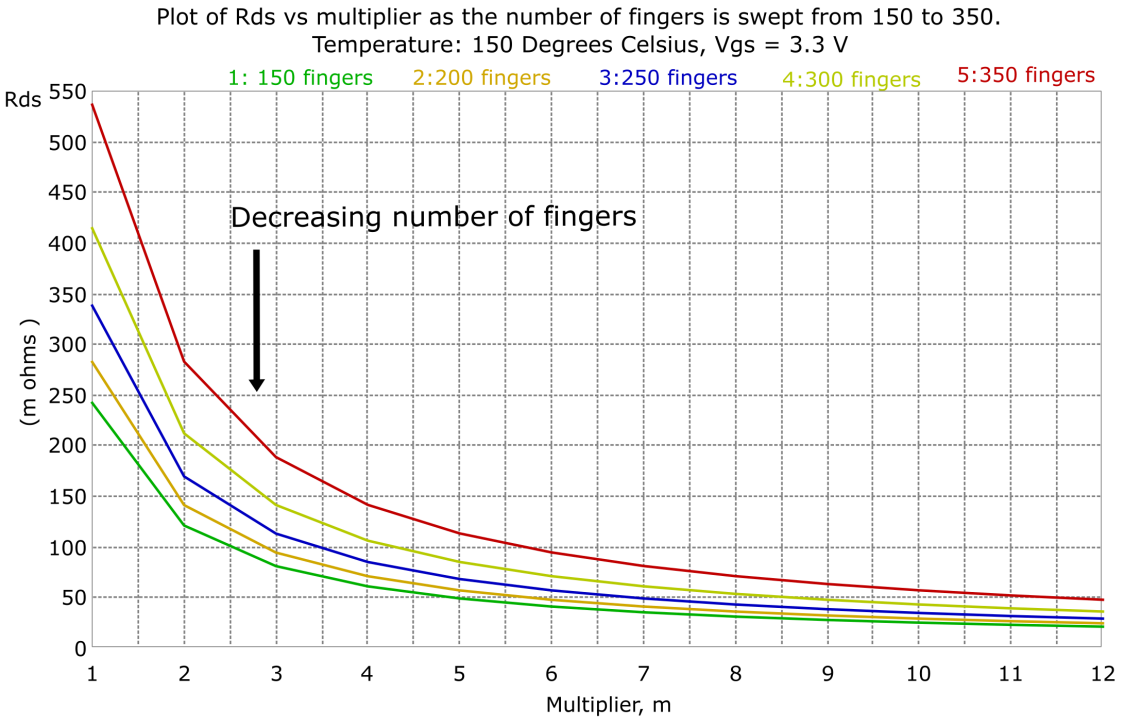

Figure 5-4: Impact of multipliers and fingers on conduction loss. As the number of copies of stacked devices (m) increases, the $R_{ds,on}$ of the device decreases. As the number of fingers decreases, the MOSFET's $R_{ds,on}$ resistance decreases.

Figure 5-5 shows the impact of temperature, (T), and gate-source voltage, (V_{gs}) on the resistance of the MOSFET. As temperature increases, the $R_{ds,on}$ increases, while increasing V_{gs} reduces the $R_{ds,on}$. For the device of fixed W_n = 40u, f = 290, L_n = 0.6 μm, m = 10, the worst-case (largest) $R_{ds,on}$ occurred when the V_{gs} = 2.7 V, T = 150 °C. This resultant $R_{ds,on}$ was 34 mΩ.

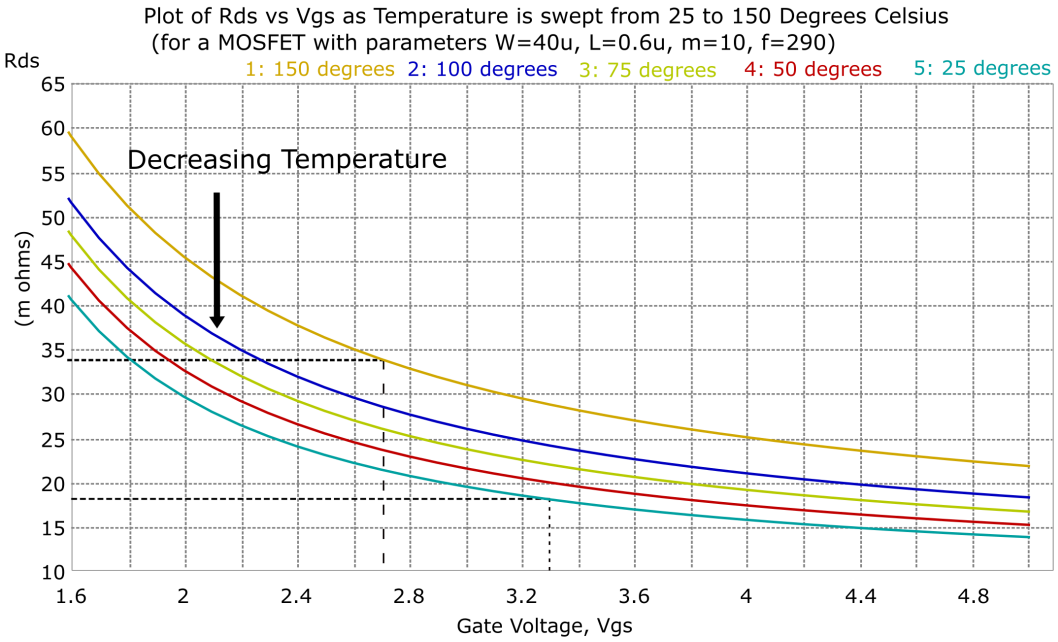

Figure 5-5: Impact of temperature, (T) and V_{gs} on conduction loss. Increasing the temperature increases the $R_{ds,on}$ while increasing the V_{gs} decreases the $R_{ds,on}$.

Based on conduction, $I^2 \cdot R_{ds,on}$, and switching losses, this maximum $R_{ds,on}$, (34 mΩ), was found to ensure an efficiency > 95 % whilst ensuring the MOSFET still remained within the physical size limits and had a good current density.

5.2 Inductor Selection

In order to remain in continuous conduction mode (CCM), the inductor current (I_L) must never hit zero. Therefore, once I_{out} is greater than half the peak to peak current ripple (ΔI_{pp}) the system will remain in CCM.

$$\begin{aligned} \Delta I_{pp} &< \frac{I_{OUT}}{2} \\ L &> \frac{V_{out}^2(1-D) * T}{2P_{min}} \end{aligned} \tag{5.1}$$

Therefore, from Equation 5.1 above, it can be seen that the constraint on the minimum inductance to ensure CCM operation is: $L > \frac{V_o ut(1-D)TR}{2}$

Another design specification identified in Chapter 2 imposes the constraint that the maximum tolerable current ripple is 30 % of the maximum peak current (1.5 A).

We want to minimize ΔI because:

- large ΔI impose stresses on components, requiring devices to be sized up to withstand stresses.
- large ΔI cause heat losses in TEC and increase the steady-state output voltage ripple.

For this TEC driver, the maximum tolerable current ripple, as outlined in the design targets is: $\Delta I_{pp} = 0.9$ A. This sets a constraint on the minimum inductance, as shown in Equation 5.2.

$$\begin{aligned} \Delta I_{pp} &= \frac{V_{out}(1-D)}{f_{sw} * L} \\ L &> \frac{V_{out}(1-D)}{f_{sw} * \Delta I_{pp}} > 75nH \end{aligned} \tag{5.2}$$

A small inductor allows the current to quickly ramp, however it also leads to large ripple current since ripple current is inversely proportional to inductance. The IC footprint limits the physical size and hence achievable inductance.

Coupled Inductors

Instead of having two separate inductors for each buck channel, the inductors can be coupled together to minimize ΔI, voltage ripple (ΔV), power losses, and reduce the overall IC package size [20, 26, 35, 54]. Figure 5-6 below shows the implementation of coupled inductors in the TEC driver circuit.

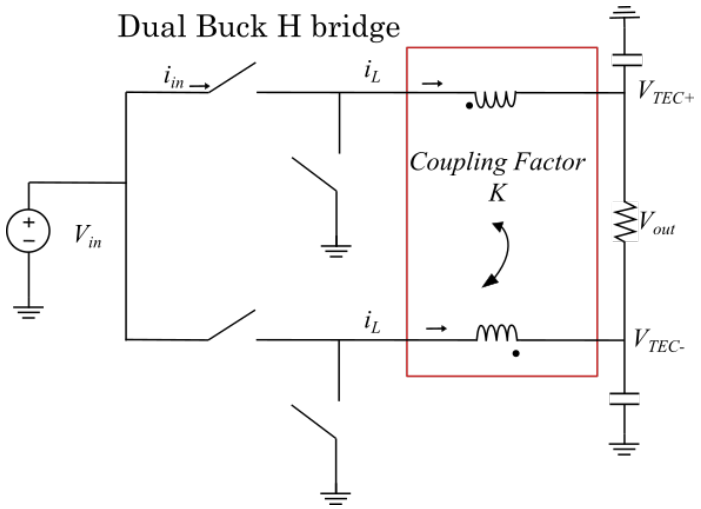

Figure 5-6: High level model of the TEC driver architecture using coupled inductors.

Each leg of the H-bridge driver has currents that are 180° out of phase which allows for additional ripple cancellation. As shown in Figure 5-7, this halves the output current ripple. The average current remains the same, however, the ripple is reduced, and the fundamental ripple frequency is doubled [35].

Even harmonic ripple currents in the inductors reinforce into the output capacitors, while the odd harmonics cancel at the output. The polarity of the coupling of the inductors can therefore give a lower ripple by suppressing differential currents and allowing common mode current to the output. The larger the magnetising inductance, the better the suppression of the odd harmonic ripple current while the leakage inductance must be set to give a desired slew rate capability. With high permeability core material, at low duty cycles the coupling approximately halves the ripple current for the same transient response.

Figure 5-7 below shows that coupling results in a 2X ΔI and ΔV reduction.

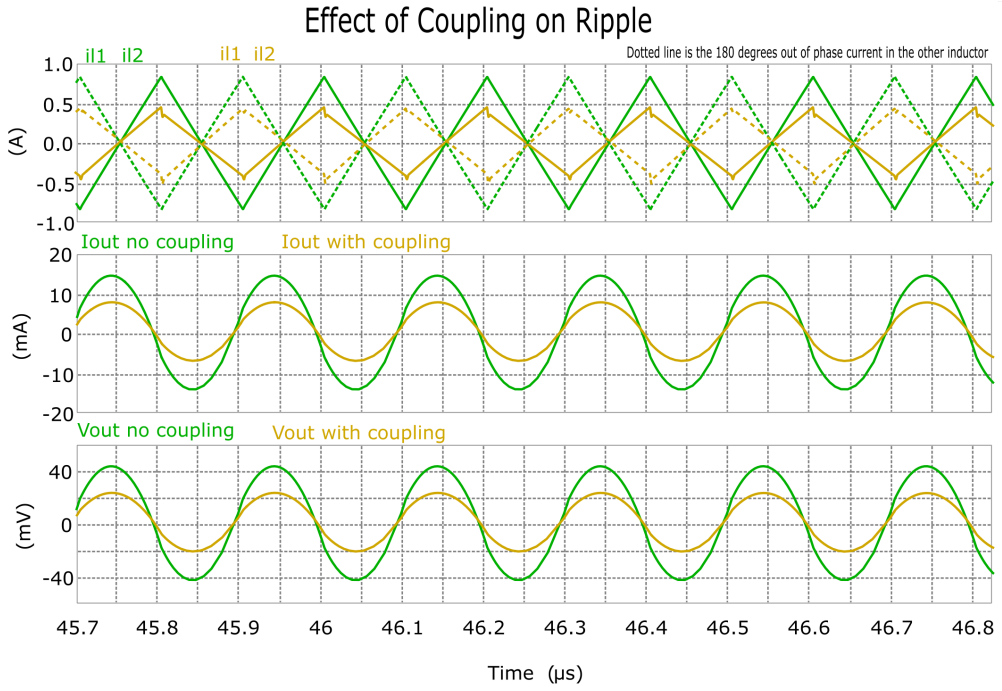

Figure 5-7: Effect of using coupled inductors on the ripple current and voltage. The green graphs are the waveforms without coupling while the yellow graphs are with a K of 0.94 and have reduced ripple.

Coupling the inductors reduces the component count and improves both the steady-state and dynamic performances. Therefore, in order to maximize the inductance and current ripple reduction, the inductors from the two buck stages were coupled to achieve a larger effective inductance while remaining within the physical device limits.

5.3 Capacitor Selection

The inductor current has a DC value and an AC ripple, however, since in periodic steady state the average capacitor current is zero, only the AC ripple goes through the capacitor. This fraction of current causes the voltage ripple. This ripple is a triangular wave with an average value of zero, therefore, it is positive for half the cycle and negative for the other half of the cycle. The peak to peak voltage ripple is found by integrating the wave over half the period, which is the area of a triangle with base T/2 and height 1/2, as derived in Equations 5.1 and 5.4 below.

$$\begin{aligned} i &= C\frac{dV_C}{dt} \\ \Delta q &= C\Delta V_C \\ \Delta V_C &= \frac{\Delta q}{C} \end{aligned} \tag{5.3}$$

Δq is the area of the triangular waveform, therefore,

$$\begin{aligned} \Delta q &= \frac{1}{2}\frac{T}{2}\Delta I_{pp} \\ C &> \frac{\Delta I_{pp} T}{4\Delta V_{spec}} \\ C &> 0.8\mu F \end{aligned} \tag{5.4}$$

The effect of parasitic effective series resistance (esr) of the capacitor reduces the resonant peak (i.e. damps the system) as well as affects the efficiency of the circuit, since power is lost through the resistance. Therefore, a capacitor with low esr was selected.

Another design consideration imposed was that the cutoff of this filter should be sufficiently far from the resonance of the switching frequency. As shown in Equation 5.5 below, the resonant frequency is inversely proportional to the square root of the capacitance.

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{5.5}$$

The breakpoint frequency was therefore set at least a factor of 10 below f_{sw} to ensure the resonance of the system was not hit. Therefore, the output capacitance (C_{Out}) value was selected to be 1 μF.

Chapter 6

Gate Drive

Figure 6-1 below shows a high-level view of the major blocks involved in the path of the signal from the output of the inner current loop to the gate of the MOSFETs.

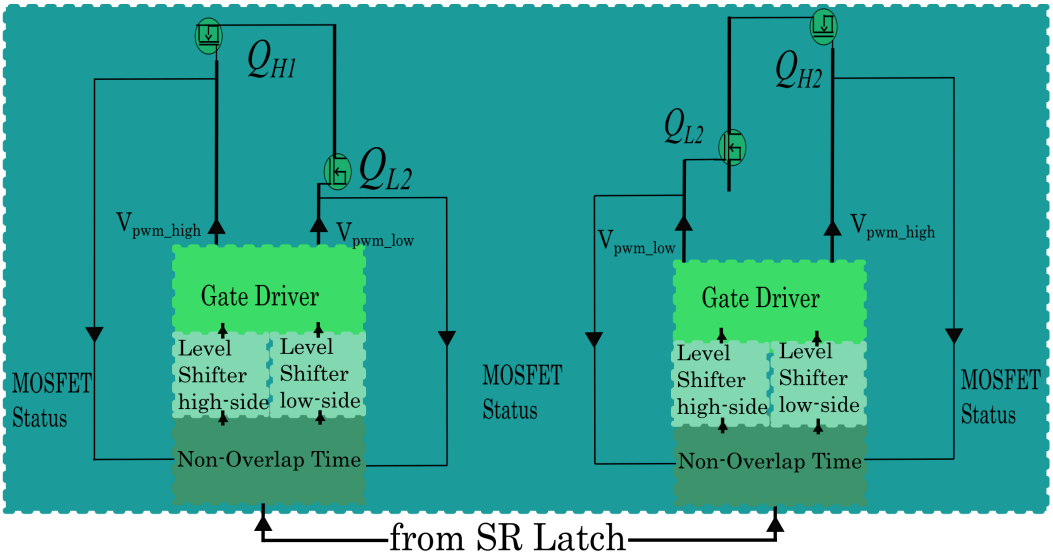

Figure 6-1: Gate drive high level block diagram showing the path of the signal to the power MOSFET, which involves the gate driver, level shifter and non-overlap blocks.

6.1 Non-overlap Timing

Ideally, the high-side and low-side MOSFETs would be driven by fully inverted signals. Unfortunately, due to the slew rate of the rising and falling edges of the PWM waveforms, if the PWM gate signals were simply the inverse of each other, there would be a period of time when both MOSFETs are on. This would create a shoot-through current, causing massive

power losses. Therefore, dead-time or non-overlapping control is imposed on these PWM gate control signals. A specially designed circuit ensures that during switching transitions, only one MOSFET is on at any time. This delay between the turn on instants of the high-side and low-side PWM signals causes both the power switches to be off for a short interval due to the dead-time circuitry. This dead-time however needs to be minimized since any extended period of time when both MOSFETs are off leads to reverse-recovery losses from the low-side MOSFETs' body diode. Therefore, in order to balance the two power losses, the non-overlap interval was made as small as possible to ensure there is no shoot through current, and minimize the reverse-recovery losses.

The circuit shown in Figure 6-2 below, takes the output of the SR latch from the inner current loop as an input as well as HS on and LS on, which are signals that tell the state of the MOSFETs. This circuit generates $Force_{HSOn}$ and $Force_{LSOn}$ as output signals, which ensure that there is sufficient non-overlap/dead time (T_{dead}) before either gate driver is turned on. However, before these signals can be fed to the power MOSFET, more circuitry is needed.

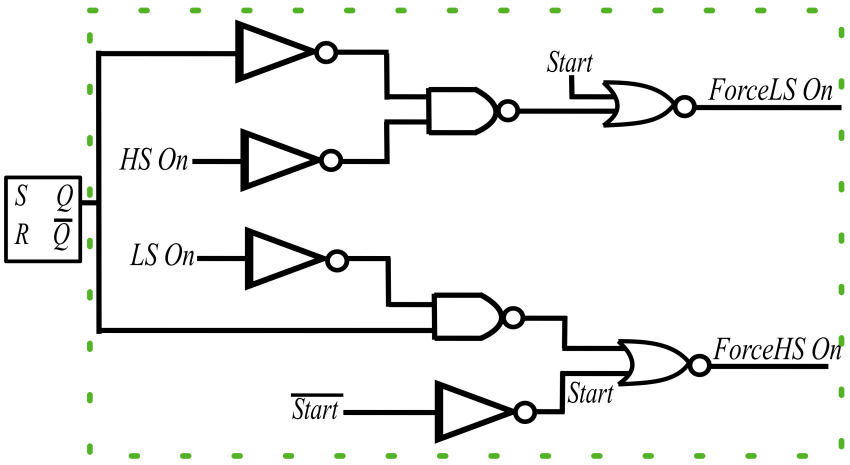

Figure 6-2: Non-overlap timing generation circuitry which ensures that the high-side and low-side MOSFETs are not on at the same time, to reduce power losses.

In the buck converter, the high-side MOSFET is connected across the input voltage node and a switch node, while the low-side MOSFET is connected across the switch node and ground, as shown in Figure 6-3. Since the high-side and low-side MOSFETs have different reference potentials, the gate drives for the MOSFETs must also be at different voltage levels.

To turn an NMOS device on, its V_{gs} must be greater than the threshold voltage (V_t). To minimize power losses, the V_{gs} for the MOSFETs was selected to be 3.3 V for nominal

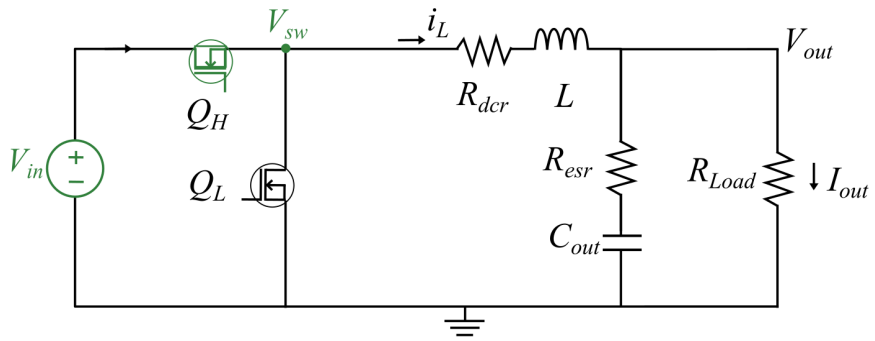

Figure 6-3: Buck converter circuit diagram showing the different reference potentials; V_{sw} for the high-side MOSFET, and ground for the low-side MOSFET.

operation. The input voltage to the system however, can vary from 5.5 to 2.7 V. Therefore, as the supply drops, the V_{gs} can drop to 2.7 V. Since the high-side MOSFET is referenced to the switch node, V_{gs} must be $> V_{in} + V_{gs}$ to turn on. A boosted voltage (BST) provided by the bootstrap circuitry must therefore be at this potential to allow the high-side MOSFET to turn on. BST must be V_{gs} higher than the switch node potential (V_{sw}).

6.2 Bootstrap Gate Drive

A bootstrap circuit is used to supply a bias to the high-side MOSFET. During the buck operation, when the low-side MOSFET is on, the high-side MOSFET is off. This causes the switch node to be pulled to ground. By placing a capacitor, diode, and resistor, the input voltage supply can be used to charge this bootstrap capacitor through the bootstrap diode and resistor.

When the low-side MOSFET is turned off, the high-side MOSFET turns on, and the switch node is pulled up to the high voltage bus. The bootstrap capacitor then discharges some of the stored voltage that was accumulated during the charging sequence, to the high-side MOSFET.

This capacitor provides a low impedance path to source the high peak currents needed to charge the high-side switch. In general, it is sized to have enough energy to drive the gate of the high-side MOSFET without being depleted by more than 10 %. Therefore, it should be at least 10 times greater than the gate capacitance of the high-side MOSFET. It was selected to be 100 nF. In order to minimize losses associated with the diode's reverse recovery, a transistor is used instead of a bootstrap diode. This ensures the device will only turn on and provide a conduction path for the capacitor when necessary. This controls the power losses and reduces the voltage drop, ensuring that BST is sufficiently high.

6.3 Level Shifter

As shown in Figure 6-3, the reference potential of high-side MOSFET's source terminal is not the system ground. Therefore, the reference potential of the input gate-driving pulse must get level shifted to match the reference voltage of the switch node. The interface between the low-voltage logic PWM inputs and the new switch-node referenced PWM pulse was implemented via a level shifting circuit, shown in Figure 6-4 below.

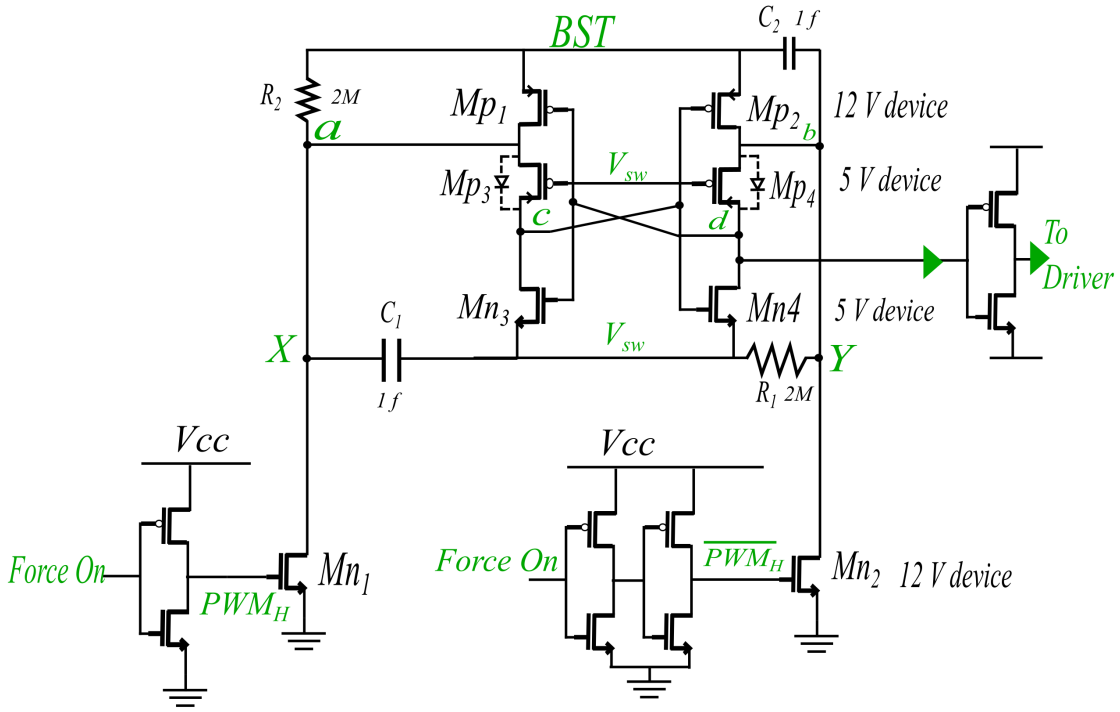

Figure 6-4: Level shifter circuit diagram used the raise the potential of the high-side MOSFET's gate drive signal.

Circuit Operation

This level shifter circuit changes the input voltage level from V_{sw}-gnd to BST-gnd. The NMOS devices, MN1 and MN2, receive a ground referenced PWM and inverted PWM input from the non-overlap timing block, described in Section 6.1. MN3 and MN4 are low V_t devices that act as voltage limiters when MN2 and MN1 are off. They ensure that the source nodes of MN3 and MN4 do not exceed V_{sw} - V_t. Therefore, MN3 and MN4 only need to be 5 V rated devices.

The drains of MN1, MN2 and MP1, MP2 can be pulled to ground if MN1 or MN2 are on, resulting in a drain-source voltage (V_{ds}) of BST across MP1 or MP2. Their drains can also be pulled up to BST if MN1 or MN2 are off, causing a V_{ds} of BST across the MN1 or

MN2. Therefore, MN1, MN2, MP1, and MP2 need to be devices that can withstand BST V. As a safety factor, 12 V rated devices are used.

MP3 and MP4 are PMOS devices that limit the drain voltage of MP3 and MP4, nodes a and b, as shown in Figure 6-4, to voltages higher than BST + V_t. They also help to decouple the signals, and speed up the transitions of the level-shifter output signal. The R2 resistor helps to set the latch while the R1 resets the latch and the capacitors act as decoupling capacitors.

The level shifter produces a PWM level-shifted pulse that is the inverse of the input, and hence needs to pass through one more inverter stage before it is the correct polarity.

Figure 6-5 shows the input PWM wave (green) and the boosted voltage (yellow) that is supplied to the high-side MOSFET.

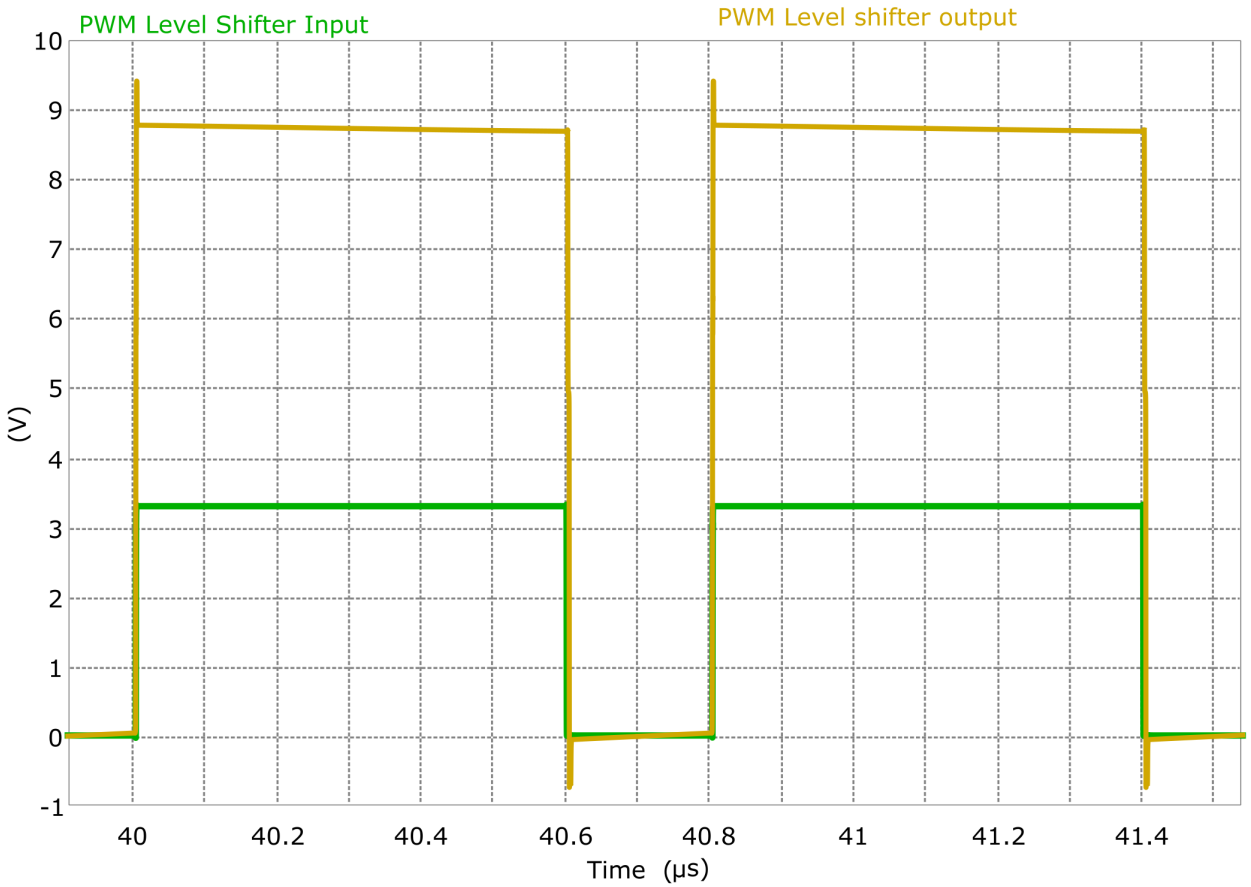

Figure 6-5: Level shifter simulation results demonstrating that the 0-3.3 V input PWM signal (green) has been boosted in voltage to the 0-8.8 V (yellow waveform), so that the high-side MOSFET can be driven.

Table 6.1 provides a summary of the operation of the MOSFETs in the level shifter circuit.

Table 6.1: Level shifter MOSFET operation.

MOSFET	$PWM_H = \mathbf{1}$ **&** $\overline{PWM_H} = \mathbf{0}$	$PWM_H = \mathbf{0}$ **&** $\overline{PWM_H} = \mathbf{1}$
MN1	$V_{gs} > 0$ MOSFET ON Nodes X & a pulled to ground	$V_{gs} < 0$ MOSFET OFF Nodes X & a set by node a
MN2	$V_{gs} < 0$ MOSFET OFF Node Y set by nodes b & d	$V_{gs} > 0$ MOSFET ON Nodes Y & b pulled to ground
MN3	Driven by d $V_{ds} < 0$ MOSFET OFF	Driven by d $V_{ds} > 0$ MOSFET ON
MN4	Gated by c $V_{gs} > 0$ MOSFET ON Node d pulled to BST	Gated by c $V_{gs} < 0$ MOSFET OFF Node d pulled to ground
MP1	Driven by d $V_{gs} > 0$ MOSFET OFF	Driven by d $V_{gs} < 0$ MOSFET ON
MP2	Gated by c $V_{gs} < 0$ MOSFET ON Node b pulled high	Gated by c $V_{gs} > 0$ MOSFET OFF Node b pulled low
MP3	Provides path from node a to c Node c pulled low	Provides path from node a to c Node c pulled high
MP4	Provides path from node d to d Node d pulled high	Provides path from node a to c Node d pulled low

6.4 Gate Driver

The power switches in the buck converter are designed to be large, in order to minimize their $R_{ds,on}$ and hence reduce conduction losses. However, these large devices now have large capacitances [40]. Charging the gate capacitor turns the device on and allows current to flow between the drain and source terminals, while discharging it turns the device off, and stops the flow of current [1]. During switching, the device is in a high current and high voltage state, which results in power dissipation. Thus, transitions between states must be minimized to reduce the time during which the device is in a dissipative state. The gate capacitor however cannot change its voltage instantaneously.

The $R_{ds,on}$ of the switches determines how much current can be sources/sunk. It is therefore a gauge of the maximum drive strength rating of a driver, since it limits the gate current that can be provided. A gate driver that can source/sink high gate current for a longer time will lower switching times and hence reduce switching power loss.

Since fast operation is paramount to the TEC driver, a special gate driver circuit was designed to minimize the rising and falling edge propagation delays, known as the slew rate. Minimizing the system delays allows higher duty cycles to be achieved, creates a large dynamic range, and ensures efficient operation. Figure 6-6 below shows the delays associated with the gate input PWM waveform where:

- on-time (T_{on}) is the time during which the MOSFET is conducting
- fall time (T_f) and rise time (T_r) are the slew rates of the falling and rising edges
- T_{dead} is the dead time interval between the high and low-side MOSFETs

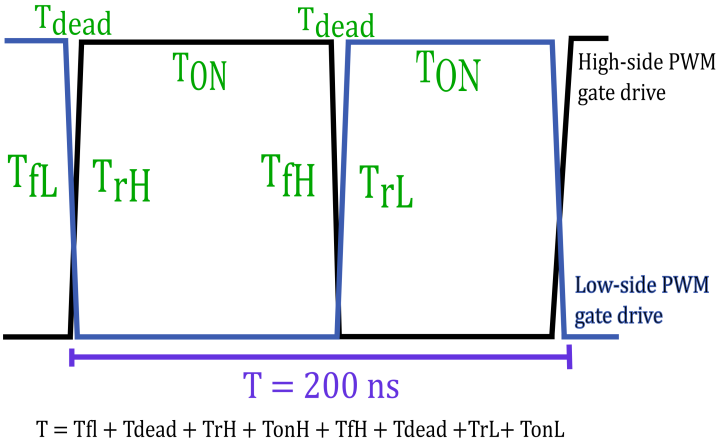

Figure 6-6: Timing analysis of the input PWM to the power MOSFETs. The period comprises the dead-time delay, the rise and fall times, and the on-times.

As MOSFETs increase in size, their capacitance increases. Therefore, the gate driver consists of a string of inverters that are progressively scaled up, as shown in Figure 6-7. This ensures that each inverter is able to quickly drive its load (the gate capacitance of the next inverter stage).

A gate drive slew rate of 1.5 μs was selected to balance minimizing the slew rate and system delays, with minimizing device sizes. The final buffer stage was designed to ensure the power MOSFETs had a slew rate of 1.5 μs. This outer stage was designed to have the largest, and hence strongest inverter pair in order to drive the large power MOSFET. The previous stages of inverters were then incrementally scaled down, dividing the $\frac{W \cdot fingers \cdot multiplier}{L}$ ratio by three for each earlier stage. This ratio ensures that the drive strength increases as the chain progresses, and that each inverter can drive the following stage.

An inverter consists of a PMOS and an NMOS device. PMOS and NMOS devices have different majority carriers in their channels and hence have different mobilities which impact their drive strengths. In order ensure the inverter is balanced, the rise times and fall times must be matched. The rise time is determined by the strength of the PMOS device as this pulls the signal up to the supply, while the fall time is dictated by the NMOS device which pulls the signal to ground.

$$\begin{aligned} \beta &= \frac{2(I_D)}{(V_{gs} - V_t)^2} \\ &= \frac{\mu C_{ox} W}{L} \\ \beta_p &= \frac{\mu_p C_{ox} W}{L} \\ \beta_n &= \frac{\mu_n C_{ox} W}{L} \\ \frac{\beta_n}{\beta_p} &= \frac{\mu_n}{\mu_p} \\ &= 64.7/14.4 \approx 4.5 \end{aligned} \tag{6.1}$$

Equation 6.1 shows that NMOS mobility (μ_n) is 4.5x stronger than PMOS mobility (μ_p). The PMOS channel Widths (W_ps) were scaled up from the NMOS devices by a factor of 4.5 to account for the difference in carrier mobility, and ensure a symmetric inverter.

Figure 6-7 below shows the scaled string of inverters used to achieve the desired gate input slew rate.

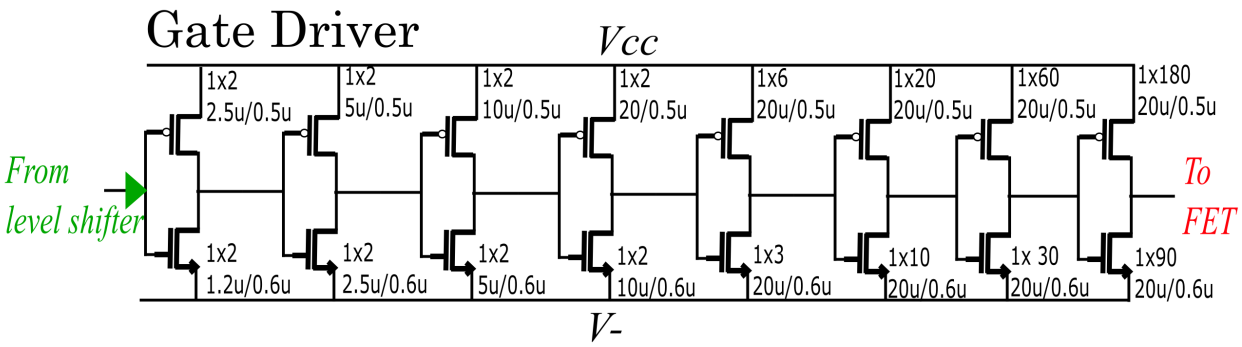

Figure 6-7: Gate driver circuit showing the scaled inverter chain used to achieve the desired input slew rate to drive the power MOSFET PWM.

Figure 6-8 below shows simulation results of the slew rate for the high-side MOSFET, that results from the driver chain.

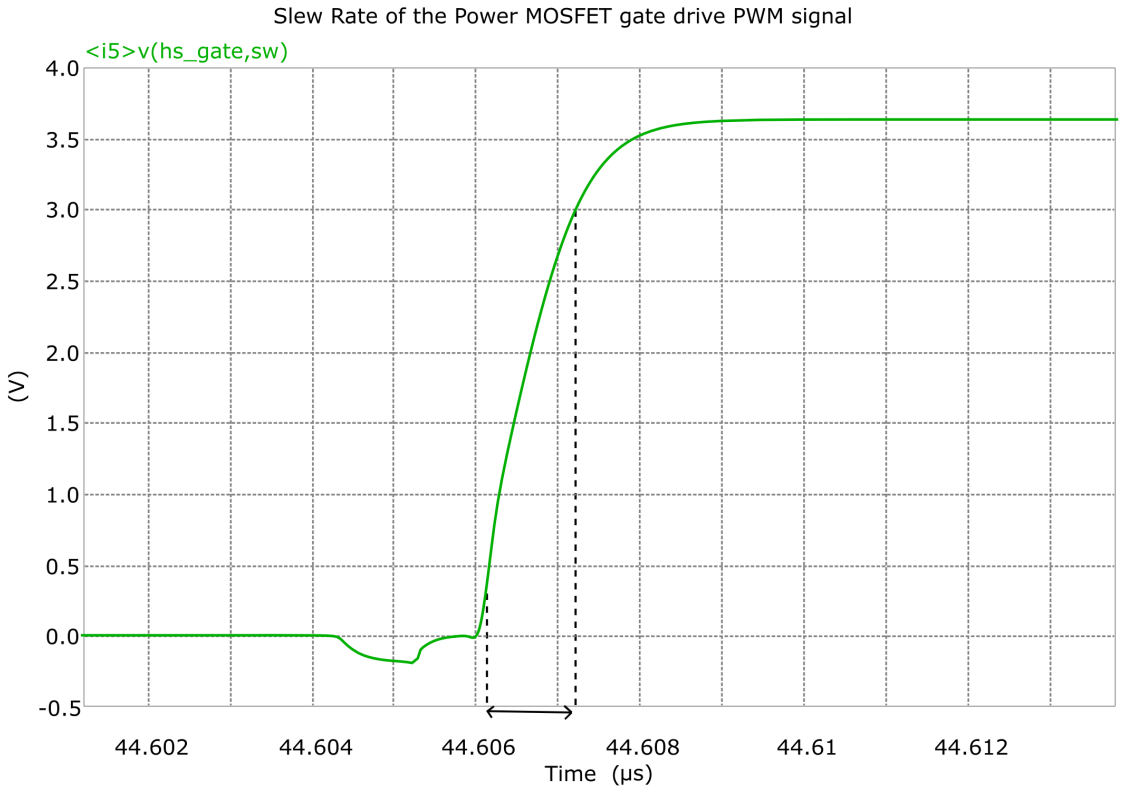

Figure 6-8: Waveform showing rise time slew rate of the high-side gate drive for the positive side of the TEC.

Chapter 7

Outer Voltage Loop

The outer voltage loop monitors the output voltage and constantly programs the controlled current source [28]. It provides a control voltage to the inner current loop, which limits the peak inductor current and sets the output voltage. Due to dynamic load and line fluctuations in a system, a controller is needed to ensure stability.

7.1 Outer Voltage Loop Macromodel Design

The outer voltage loop, as shown in Figure 7-1, comprises the:

- voltage divider
- compensator network
- error amplifier

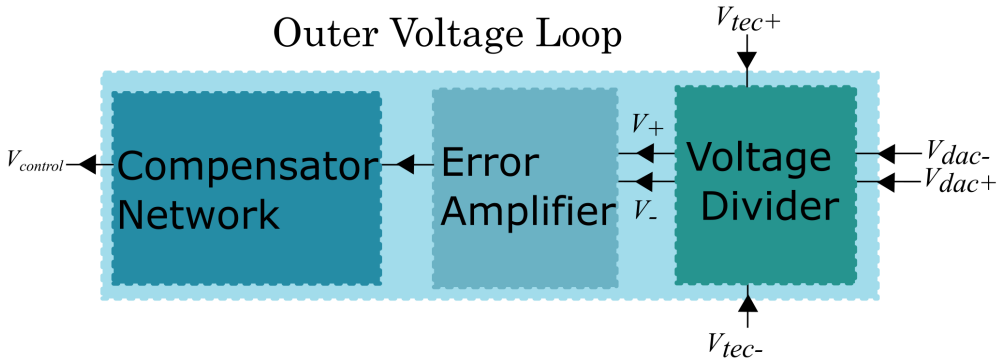

Figure 7-1: High level block diagram showing the outer voltage loop design.

7.1.1 Voltage Divider

The voltage divider block produces a scaled down version of the buck output voltage, centred about an input common mode, and sets the output common mode of the system.

Output Common Mode

The system was designed to have an output common mode level that ensured a large dynamic range. This output common mode was chosen to be around $\frac{V_{in}}{2}$, the 50 % duty cycle point. This allowed both the positive and negative current cases to be centred about the same point to maximize the range of the system.

Input Common Mode

The input common mode voltage (V_{cm}) level was set to ensure that any large disturbances in the common mode level would not significantly impact the bias currents for the differential pair transistors of the error amplifier. Input common mode variation would impact both the transconductance (gm), which sets the system gain, as well as the output common mode level. If the input common mode were too high/low, the output voltage swing would be reduced. A variable input common mode results in incorrectly biasing causing the MOSFETs to enter the triode region, where they will no longer amplify.

The gain ratio of the voltage divider block sets the input common mode. Additionally, the gain ratio was set to ensure that V_{ref} was well mapped to the output voltage range. V_{ref} is a differential signal that has a 2 V swing centred about 1.25 V. The maximum output voltage for each buck stage output ranges from V_{in} to 0 (nominally a 5 V swing). Using a gain ratio of $\frac{V_{ref}}{V_{out}}$, the gain ratio scale factor was set to be 2.5. The V_{cm}, was therefore selected to be 1.607 at nominal operation, as calculated in Equation 7.1 below.

$$\begin{aligned} \frac{\frac{V_{in}}{2} - V_{cm}}{2.5} &= -\frac{1.25 - V_x}{1} \\ \frac{V_{in}}{2} - V_{cm} &= 2.5(1.25 - V_{cm}) \\ V_{cm} &= \frac{\frac{V_{in}}{2} + 2.5(1.25)}{6} \approx 1.607 \end{aligned} \tag{7.1}$$

Values for feedback resistors (R_{fb1}, R_{fb2}) were selected to be 25 KΩ and 10 KΩ respectively to satisfy the desired scaling factor. This gain ratio maps the reference voltage range to the output voltage range to ensure a large dynamic range and sets an input common mode to ensure the transistors have sufficient headroom to operate in the saturation regime. The output of the voltage divider block, shown in Figure 7-2 below, has resistors R_{fb1}, R_{fb2}

to set the input common mode, while the input V_{dac-} is paired with V_{tec+}, and V_{dac+} is paired with V_{tec-} to create the output common mode. The output of each of the resistor divider networks is then passed to the error amplifier and compensator network blocks which eventually outputs a control voltage ($V_{control}$).

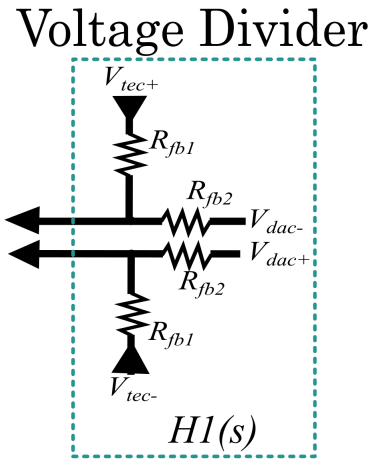

Figure 7-2: Voltage divider block diagram showing the feedback resistors, R_{fb1}, R_{fb2}, which were selected to achieve the desired scaling factor.

7.1.2 Error Amplifier

The error amplifier magnifies the difference between the two inputs and through the feedback loop, the inputs are stabilizing to a common value. The error amplifier for frequency compensation can be a simple voltage-to-voltage amplification device, the traditional op-amp, or can be a voltage-to-current amplification device, the operational transconductance amplifier (OTA). The traditional amplifier amplifies the error detected between a fixed reference level and a state variable. It requires local feedback between its output and inputs to make it stable. The values of resistors in the feedback network affects the gain-phase of the system. The OTA amplifier however is an open-loop amplifier stage with no local feedback. Only the ratio of the feedback resistors is important, not the actual values. The OTA design was utilized because the simplicity of its design facilitates the ease of analysis.

7.1.3 Compensator Network

The compensator network block ensures stability of the system in response to any disturbances. It consists of an resistor and capacitor (RC) network and is designed to counteract the gains and phases of the system's control-to-output transfer function that negatively impacts stability [28]. Due to the difficulty in measuring the small-signal time domain responses of a DC-DC converter system, frequency response is the most convenient metric to use to

design the compensator. The controller tailors the frequency response to create a stable closed loop.

The ultimate goal is to make the system's closed-loop-transfer function, shown in Figure 7-3, satisfy the stability criteria.

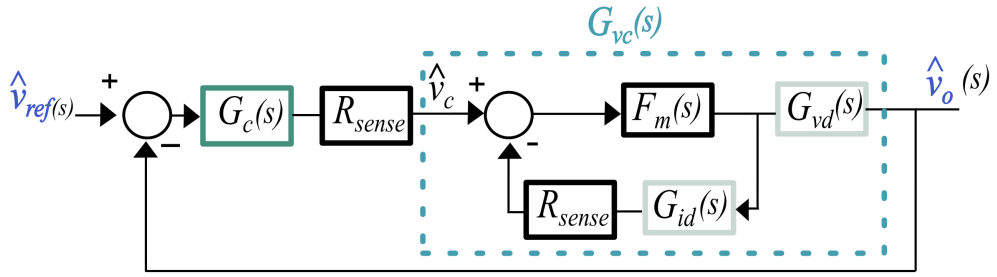

Figure 7-3: Block diagram showing the outer voltage loop with the controller ($G_c(s)$) and plant ($G_{vd}(s)$).

The system was designed to have:

1. Minimized peaking. This can be achieved by moving the compensator zeros to coincide with LC resonant frequency to minimize phase shift.

2. Good phase margin (pm) and gain margin ($> 70°$, $>$ -10 dB). This prevents oscillations by providing a large damping factor to ensure a well-damped transient load response.

3. A high crossover frequency (f_c), (1/5 - 1/10 f_{sw}), to maximize bandwidth and ensure fast transient response.

4. Attenuation at f_{sw} for good noise immunity and jitter minimization.

5. A -20 dB/dec slope at the gain crossover point. This maximizes the gain margin and ensures stability since it negates the chance of the gain turning positive at a higher frequency where the phase crosses 0.

6. Large DC gain to minimize the DC regulation/steady state error, and ensure high accuracy.

Compensation Network Design

The following steps outline the process that was involved in designing the compensation network that stabilized the system.

1. **Unity gain crossover frequency selection**

The f_c determines the bandwidth of the system. A low bandwidth results in slow transient behaviour, bad disturbance rejection, and the propagation of errors through the system. A higher bandwidth causes faster transient response, however, reduces the stability margin and makes the control loop more sensitive to switching noise. Therefore, a balance must be struck between the bandwidth (transient response) and stability margin.

From the modelling of the system as discussed in Chapter 4, it can be seen that the closed loop model introduces an undesirable phase delay at $\frac{f_{sw}}{2}$, due to a pair of double poles that are caused by the sampling effect of the current signal. In order to achieve a good phase margin and noise attenuation,f_c was selected to be $1/10^{\,th}$ f_{sw}.

2. **Phase boost calculation**

   The frequency response of the system plant, was investigated to determine the current phase at the desired crossover frequency. The phase margin determines the transient response of the system. If the pm is too high, the system will have a slow response, whereas if pm is too low instability, manifested as oscillations in step responses results [45]. Therefore, a target phase margin of 60° was set to ensure a fast, well-damped response. Based on the current system phase and desired phase margin, the phase boost (pb) needed was determined to be $pb = (x - 90) + pm$.

3. **Compensation scheme selection**

   The larger the pb required, the more complicated the compensation architecture becomes. The buck output filter has complex poles which require a pb of 180° to stabilize the system. This would requires type III compensation [27], which has:

   - two zeros placed at the location of the complex conjugate of poles of the LC filter. It provides a notch that will eliminate the resonant peak.
   - a pole at the origin for high DC gain
   - a high frequency pole to cancel the zero caused by the capacitor's esr
   - a high frequency pole to attenuate switching noise

   However, due to the inner loop of peak current mode feedback, the inductor dynamics are removed from the system, and, only maximum of 90° phase boost in needed. Type II compensation [27], which has two poles, and one zero, is able to provide up to 90° of phase boost and therefore was selected.

The compensator can be therefore be thought of as three cascaded transfer functions, as shown in Figure 7-4.

1. H1(s) is the voltage divider ratio (β_{vdiv}) which impacts the DC gain of the system.
2. H2(s) is the transfer function of gm. This also impacts the DC gain of the system.
3. H3(s) is the impedance of the compensator network at the amplifier output, $V_{control}$. It determines the crossover frequency and hence bandwidth, as well as the phase/gain margins of the system.

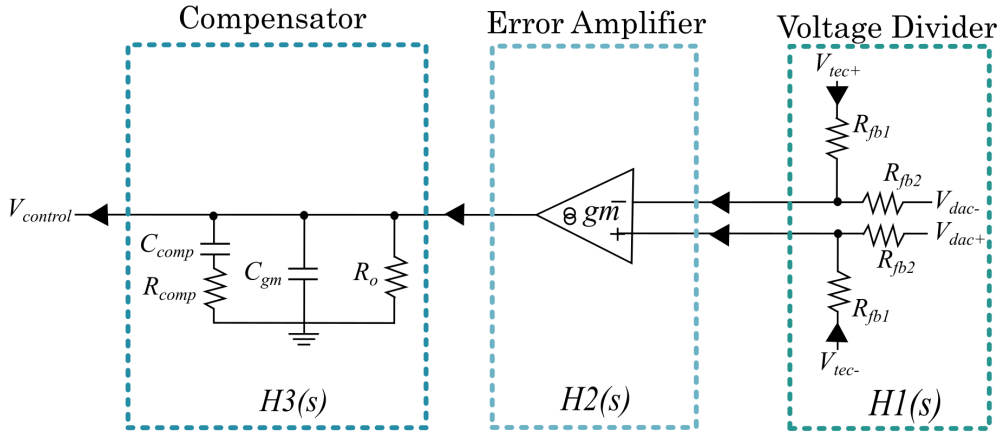

Figure 7-4: Macromodel design of the compensation network of the outer voltage loop.

- R_o**:** The transconductance amplifier does not have an infinite output impedance, therefore, the error amplifier internal output resistance (R_o) term is added to account for the finite output impedance.

- C_{Comp}**:** In order to minimize the steady state error, high DC gain is achieved by placing a compensator capacitance (C_{Comp}) capacitor at the amplifier output. The capacitor has an impedance of $\frac{1}{sC_{Comp}}$. This capacitor forms an integrator, adding a pole at the origin, and hence providing infinite DC gain and -90 degrees of phase shift.

  The parallel R_o, C_{Comp} branch now creates a low frequency pole, $P_o = \frac{1}{R_o C_{Comp}}$. The transfer function then becomes: $H3(s) = \frac{1}{1+\frac{s}{P_o}}$

- R_{Comp}**:** To increase the phase at the crossover frequency, a compensator resistance (R_{Comp}) is added in series with C_{Comp}. This creates a zero, z_o, and adds +90 degrees phase boost. This zero needs to be placed before the crossover frequency to increase the phase of the compensator and hence increase the phase margin of the system. $z_o = \frac{1}{R_{Comp}C_{Comp}}$

The transfer function then becomes: $H3(s) = R_o * \frac{1+\frac{s}{z_o}}{1+\frac{s}{p_o}}$

- C_{gm}**:** This R_{Comp} zero causes a gain slope increase which causes an increase in gain at high frequencies above the crossover frequency. In order to attenuate the high frequency switching noise, a small ceramic compensator capacitance (C_{gm}) is added in parallel. This introduces a high frequency pole, $p_1 = \frac{1}{R_{Comp}\frac{C_{Comp}C_{gm}}{C_{Comp}+C_{gm}}}$.

  since $C_{gm} << C_{Comp}$, $p_1 \approx \frac{1}{R_{Comp}C_{Comp}}$

  The location of this pole is a tradeoff between noise immunity and phase margin. In order to sufficiently attenuate the high frequency noise, it must be placed as close to f_c as possible. However, the closer the pole is to f_c, the lower the phase margin of the system will be due to the -90 phase of the pole.

The final transfer function then becomes: $H3(s) = R_o * \frac{(1+\frac{s}{z_o})}{(1+\frac{s}{p_o})(1+\frac{s}{p_1})} = \beta gm R_0 \frac{(1+\frac{s}{z_o})}{(1+\frac{s}{p_o})(1+\frac{s}{p_1})}$

Effect of Controller Parameters

- **Impact of** C_{Comp}

C_{Comp} affects the location of the low frequency pole (f_{p0}), and the low frequency zero (f_z). A smaller C_{Comp} can increase the low to-mid frequency gain of transfer function, as well as reduce the load transient response settling time without much impact on the V_{out} undershoot (or overshoot) amplitude. On the other hand, a smaller C_{Comp} means higher f_z frequency which may reduce the phase boost at the targeted crossover frequency.

- **Impact of** R_{Comp}

R_{Comp} impacts the location of the zero and the high frequency pole (f_{p1}). Larger R_{Comp} increases the gain between f_z and f_{p1}, and directly increases the supply bandwidth f_c. It therefore reduces the V_{out} undershoot/overshoot at the load transient. However, if R_{Comp} is too large, the supply bandwidth f_c can have insufficient phase margin, affecting the stability of the system.

- **Impact of** C_{gm}

C_{gm} affects the location of the 2^{nd} high frequency pole. It is used as a decoupling capacitor to reduce switching noise. If $f_c > f_{p1}$, C_{gm} does not impact the load transient response.

However if $f_c < f_{p1}$, C_{gm}, can reduce the bandwidth and phase margin, resulting in an increased transient.

- **Impact of β_{vdiv} R_o, gm**

β_{vdiv}, R_o and gm affect the DC gain of the system. The DC gain is given by R_o x β_{vdiv} x gm.

Component values and pole/zero placement

The component values for the resistors and capacitors were selected to ensure the poles, zeros and DC gain created a stable system. The component values chosen were: $\beta_{vdiv} = 0.4$, $R_o = 90$ MΩ, gm = 100 $\mu\Omega^{-1}$, $C_{Comp} = 20$ pF , $R_{Comp} = 60$ KΩ , $C_{gm} = 400$ fF

DC Gain: $90e^6$ x $100e^{-6}$ x $\frac{1}{2.5} = 3600 \approx 72$ dB

The following equations show the placement of the poles and zeros for the compensator.

Low Frequency Zero: $f_z = \frac{1}{R_{Comp}C_{Comp}}$
In order to ensure the system has sufficient bandwidth, the zero frequency is made to be less than the targeted crossover frequency. This sets a limit on the values of R_{Comp}, C_{Comp}, as shown in Equation 7.2 below

$$\begin{aligned} f_z &< f_c \\ f_z &< 5e^6 \\ \frac{1}{R_{Comp}C_{Comp}} &< 5e^6 \end{aligned} \tag{7.2}$$

High Frequency Pole $f_{p1} = \frac{1}{R_{Comp}C_{gm}}$
The location of this pole is a trade-off between noise immunity and phase margin. Therefore, the pole frequency was set between the crossover frequency and the switching frequency as shown in Equation 7.3 below:

$$\begin{aligned} f_c < f_{p1} < f_{sw} \\ \text{Assuming } C_{gm} << C_{Comp} \\ \frac{5}{6}e^6 < f_{p2} < 5e^6 \end{aligned} \tag{7.3}$$

Low Frequency Pole: $f_{p0} = \frac{1}{R_o C_{Comp}}$

This pole was placed before the zero and second pole, in order to create the high DC gain of the system. This allows a value for R_o to be calculated, as shown in Equation refeq:7.4.

$$\begin{aligned} f_{po} &< f_z < f_{p1} \\ f_{p0} &< fz < \frac{5}{6}e^6 < f_{p1} < 5e^6 \\ \text{Assuming } C_{gm} &<< C_{Comp} \\ \frac{1}{R_o C_{Comp}} &< \frac{1}{R_{Comp} C_{Comp}} < 0.8e^6 < \frac{1}{R_{Comp} C_{gm}} < 5e^6 \\ R_o &\approx 90e^6 \end{aligned} \tag{7.4}$$

Figure 7-5 and the bode plot, Figure 7-6, show the placement of the poles and zeros for the compensator that were used to stabilize the system.

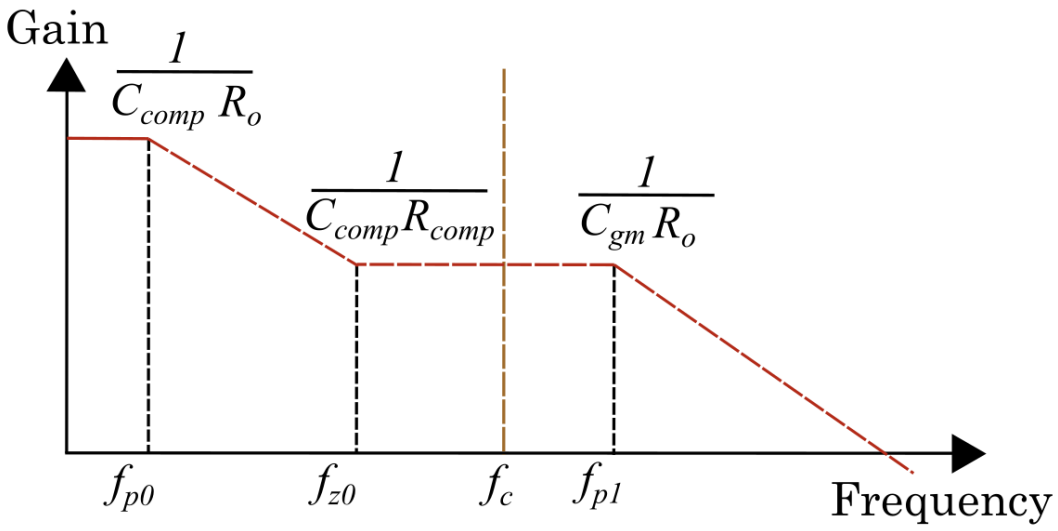

Figure 7-5: Gain-frequency plot showing the poles and zeros of the controller that was designed to stabilize the system.

The compensator was designed to add a phase boost to the system to stabilize the closed loop system. As shown in Figure 7-6, the peak in the phase bump was made to occur at the crossover frequency of the open loop system to mitigate against instability in the system whilst ensuring the system has a fast response.

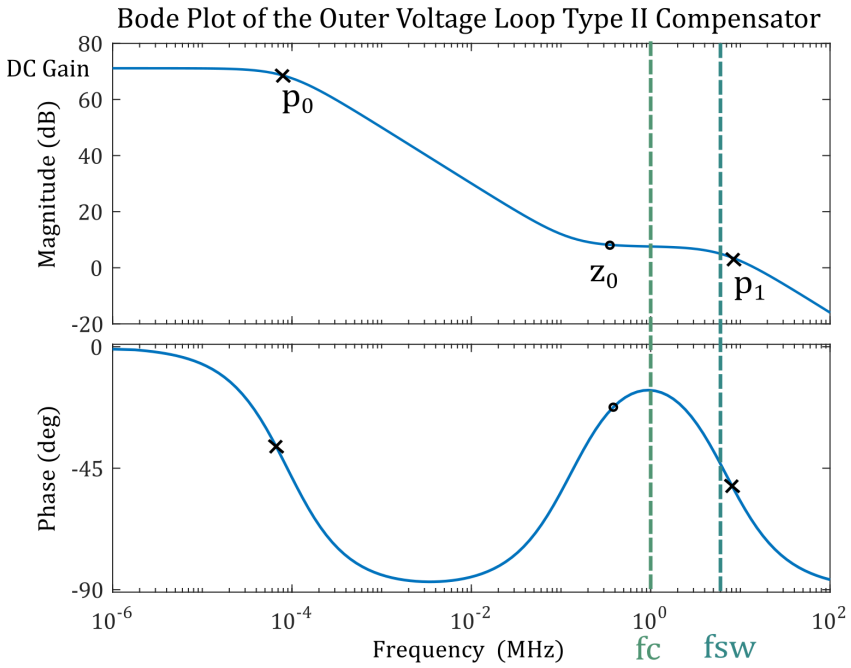

Figure 7-6: Bode plot of the Type II OTA compensator that was designed to stabilized the open loop system.

Figure 7-7 shows the bode plot of the unstable open loop and the stabilized closed loop.

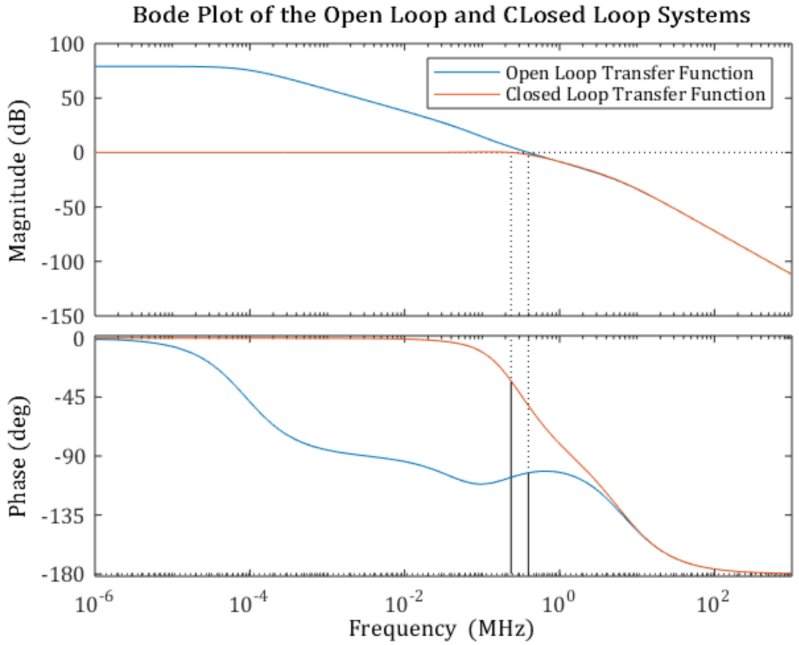

Figure 7-7: Bode plot of the open loop (blue) and closed loop (orange) systems. The closed loop system has a higher phase margin and is more robust against disturbances.

7.2 Outer Voltage Loop Transistor Level Design

The error amplifier was selected to be an OTA gm amplifier. Its macromodel behaviour was set when designing the control loop dynamics in Section 7.1. The following design targets were realised through transistor-level design:

- R_o of 90 MΩ
- gm of 100 $\mu\Omega^{-1}$
- common mode noise rejection

7.2.1 Error Amplifier

Figure 7-8 below shows a diagram of the error amplifier which was constructed using a backbone of a differential pair, and a cascode current mirror [4, 15, 38]. It amplifies the difference between the output voltages from the buck stages, and ensures the signals are centred about a set input common mode level.

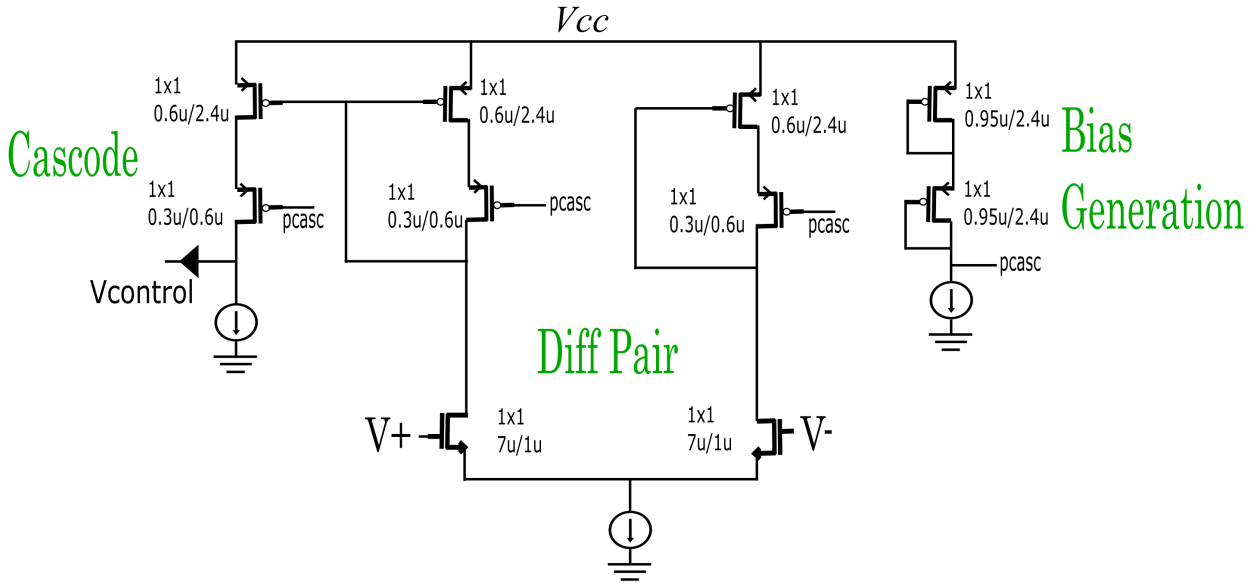

Figure 7-8: Transistor level design of the error amplifier showing the current mirror, differential pair, and biasing of MOSFETs.

Transistor Matching

In complementary metal oxide semiconductor (CMOS) IC design, any two MOSFET devices, with the same $\frac{Width}{Length}$ ratio, made in the same process technology, and even laid out next to each other are not identical. They differ in a myriad of ways, and generally,

these differences stem from random offsets that were caused during the manufacturing of the devices [34]. Theses random mismatches [2] follow a Gaussian profile, about a mean with variance (σ) and standard deviation (Δ) as shown in Figure 7-9.

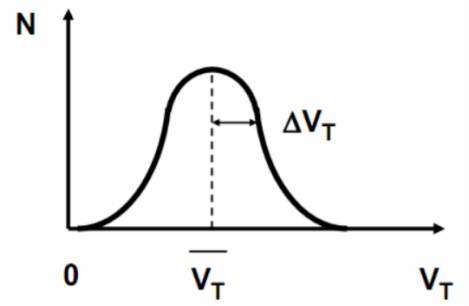

Figure 7-9: Threshold mismatch for the device spread shown as a Gaussian distribution.

The drain current (I_D) of a MOSFET is a function of threshold voltage, gate-source voltage, device geometry (W, L), and intrinsic parameters (channel mobility (μ_c), MOSFET oxide capacitance (C_{ox})), given by device property (β_p, β_n)). Therefore, any variation in these parameters will impact the device operation. These device mismatch parameters are provided in the TSMC process technology library for the devices. The transistors were thus carefully sized to mitigate the threshold voltage mismatch (δV_t), beta mismatch ($\delta\beta$), gate-source voltage mismatch (δV_{gs}).

$$\begin{aligned}
\frac{\delta I_d}{\delta\beta} &= +(1)\frac{1}{2}(V_{gs}-V_t)^2 \\
\frac{\delta I_d}{\delta V_t} &= -(2)\beta\frac{1}{2}(V_{gs}-V_t) \\
\frac{\delta I_d}{\delta V_{gs}} &= +(2)\beta\frac{1}{2}(V_{gs}-V_t) \\
\Delta I_D &= \frac{1}{2}(V_{gs}-V_t)^2\Delta\beta - \beta(V_{gs}-V_t)\Delta V_t + \beta(V_{gs}-V_t)\Delta V_{gs}
\end{aligned} \tag{7.5}$$

Equation 7.5 above demonstrates effect of the mismatch on the drain current.

7.2.1.1 Differential Pair

The differential pair, shown in Figure 7-8, has input signals V^+ and V^-. These signals are scaled versions of each buck stage's output and are differential, centred around an input common mode level. These differential signals along with the tail current source of the differential pair suppresses the effect of the input common mode level variations. This ensures that the I_D is largely independent of the V_{cm} deviations. This fixes the operation

regime of the differential pair MOSFETs and the output level, as a fixed drain current flows through the devices. The differential amplifier then uses negative feedback to steer current through the branches and ensure that the currents in two branches are balanced [4, 15, 38].

The gm of the NMOS devices of the differential pair sets the gain of the system. Thus, in order to achieve the desired transient response, the transistors were sized to have gm of 100 $\mu\Omega^{-1}$. The gm of a device is the rate of change of I_D, to the rate of change of the V_{gs}. I_D is given by the equation: $I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_gs - V_t)^2$. Therefore, $g_m = \frac{\delta I_D}{\delta V_{gs}} = \beta(V_{gs} - V_t)$ where β is defined as $\frac{\mu C_{ox} W}{L}$.

$$gm = \sqrt{2\beta I_D} = \sqrt{2\mu C_{ox}\frac{W}{L}I_D} \tag{7.6}$$

From Equation 7.6 above, the gm of the transistor is a function of β and I_D. Since all the transistors have constant drain current, the drain current mismatch (ΔI_D) must be 0. Equation 7.7 below shows the derivation of the ΔV_{gs} mismatch.

$$\begin{aligned} 0 &= \frac{1}{2}(V_{gs} - V_t)^2\Delta\beta - \beta(V_{gs} - V_t)\Delta V_t + \beta(V_{gs} - V_t)\Delta V_{gs} \\ 0 &= \frac{(V_{gs} - V_t)}{2}\frac{\Delta\beta}{\beta} - \Delta V_t + \Delta V_{gs} \\ \Delta V_{gs} &= -\frac{(V_{gs} - V_t)}{2}\frac{\Delta\beta}{\beta} + \Delta V_t \\ &= -\frac{\Delta\beta}{\beta}\frac{I_D}{g_m} + \Delta V_t \end{aligned} \tag{7.7}$$

To minimize the ΔV_{gs} mismatch for the differential pair NMOS devices, we need:

- a high $\frac{g_m}{I_D}$ ratio
- to minimize the overdrive for the differential pair, by having a large $\frac{W}{L}$ratio: i.e. maximize the g_m for the differential pair

In order to obtain a gm of 100 $\mu\Omega^{-1}$, using the device parameter information obtained in the TSMC datasheet, $\frac{W}{L} = \frac{g_m^2}{2\mu C_{ox} I_D} = 7$. Therefore, a W/L ratio of ≈ 7 was used.

The root mean square (rms) variation in the differential pair, ($\sigma(\Delta V_{gs,total})$), is given by: $\sigma_{mirror}(\Delta V_{gs}), = \sigma(\frac{\Delta I_d}{I_D}) * \frac{I_D}{gm_N}$ The mismatch from the differential pair, $\sigma(\Delta V_{gs,total}), = \sqrt{(\sigma_{nmos}(\Delta V_{gs}))^2 + (\sigma_{mirror}(\Delta V_{gs}))^2}$

The current error mismatch from the current mirror reflected through the gm of the

NMOS devices, $\sigma_{nmos}(\Delta V_{gs}) = \sqrt{(\frac{\Delta\beta}{\beta}\frac{I_D}{g_m})^2 + (\Delta V_t)^2}$

By balancing the minimization of the ΔV_t mismatch and ensuring the device was not too small, $\sigma(\Delta V_{gs,total})$ was found to be 5.76 mV. This mismatch was tolerable for the system and hence for the NMOS differential pair, a W/L ratio of 7 μm /1μm was selected.

7.2.1.2 Current Mirror

The PMOS current mirror circuitry copies a desired load reference current for the differential pair. The circuit has a modified cascode connection to increase the R_o of the system, while minimizing voltage headroom required when using the traditionally diode connected PMOS devices in a cascode architecture. This cascode current mirror helps to set the desired output resistance for the system and ensures a high output voltage swing [4, 15, 38].

For the current mirror, the fractional error in currents being mirrored is the key factor to be determined in order to minimize mismatch. Since all the transistors in the current mirror have the same V_{gs}, the $\Delta V_{gs} = 0$. Therefore, the fractional error in the currents being mirrored in the 1:1 ratio current mirror is determined by Equation 7.8:

$$\begin{aligned}\frac{\Delta I_d}{I_D} &= \frac{\frac{1}{2}(V_{gs}-V_t)^2\Delta\beta}{\frac{\beta}{2}(V_gs-V_t)^2} - \frac{\beta(V_{gs}-V_t)\Delta V_t}{\frac{\beta}{2}(V_{gs}-V_t)^2} \\ &= \frac{\Delta\beta}{\beta} - \frac{2\Delta V_t}{(V_{gs}-V_t)} \\ &= \frac{\Delta\beta}{\beta} - \frac{g_m}{I_D}\Delta V_t\end{aligned} \tag{7.8}$$

The offset can be mitigated by:

- minimizing $\frac{g_m}{I_D}$. This can be achieved by maximizing the overdrive voltage by having a small $\frac{W}{L}$
- increasing the device size since the $\sigma_{\Delta V_t} = \frac{A_{V_t}}{\sqrt{WL}}$.

For the current mirror, 1% matching was targeted. With $I_D = 10\ \mu$ A, $\sigma(\frac{\Delta I_d}{I_D}) = \frac{0.01}{\sqrt{2}}$

The total rms variation due to the random error is shown in Equation 7.9 below:

$$\sigma(\frac{\Delta I_d}{I_D}) = \sqrt{(\frac{\Delta\beta}{\beta})^2 + (-\frac{g_m}{I_D}\Delta V_t)^2} \tag{7.9}$$

The impact of $\Delta\beta$ is negligible, therefore Equation 7.10 was used to find the length.

$$\begin{aligned}
\sigma(\frac{\Delta I_d}{I_D}) &\approx \frac{g_m}{I_D}\Delta V_t; (\frac{g_m}{I_D} = \sqrt{\frac{2\mu c_{ox}}{I_D}\frac{W}{L}}) \\
\sigma(\frac{\Delta I_d}{I_D}) &= \sqrt{\frac{2\mu c_{ox}}{I_D}\frac{W}{L}}\sigma\Delta V_t; (\sigma\Delta V_t = \frac{A_{v_t}}{\sqrt{WL}}) \\
\frac{0.01}{\sqrt{2}} &= \sqrt{\frac{2\mu C_{ox}}{I_D}\frac{W}{L}}\frac{A_{v_t}}{\sqrt{WL}} = \sqrt{\frac{2\mu C_{ox}}{I_D}}\frac{A_{v_t}}{L} \\
L &= \sqrt{\frac{2\mu C_{ox}}{I_D}}A_{v_t}\frac{\sqrt{2}}{0.01} = \sqrt{\frac{2(14.4e^{-6})}{10e^{-6}}}(8.0971e^{-3})\frac{\sqrt{2}}{0.01} = 2.36\mu
\end{aligned} \tag{7.10}$$

For 1% matching: $L_{max} = 2.32$ μm. In order to minimize mismatch, a low gm/ID ratio is desirable, therefore, W was set to 600 nm.

For a W/L ratio of **600 nm/2 μm**:

- $\sigma(\frac{\Delta I_d}{I_D}) = \sqrt{(\frac{0.648}{100})^2 + (\frac{9.29e^{-6}}{10e^{-6}}7.39e^{-3})^2} \approx 9.38e^{-3}$. This mismatch was acceptable for the system.
- R_o of the cascode current mirror, given by the product of the output resistance of MP4 and the intrinsic gain of MP6, was found to be $\frac{1}{g_{ds_{MP4}}}\frac{1}{g_{ds_{MP6}}}g_{m_{MP6}} \approx 100M\Omega$, which is within the range of values required for the compensator dynamics.

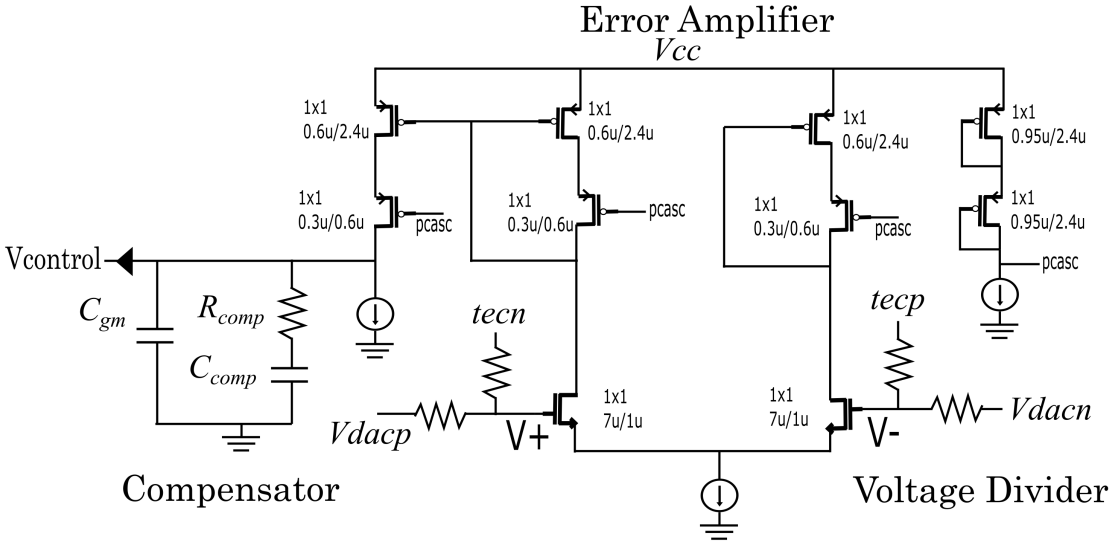

Figure 7-10: Transistor-level design of the outer voltage loop.

Figure 7-10 above, shows the complete outer voltage loop block. The simulation results, analyzing the stability for this system are presented in Section 9.3.

Chapter 8

Inner Current Loop

The current loop senses the inductor current signal and compares it to the control voltage from the outer voltage loop to modulate the PWM pulse width [30]. It comprises the following major blocks shown in Figure 8-1:

- Set-Reset (SR) latch
- Current sense
- Slope compensation
- Comparator

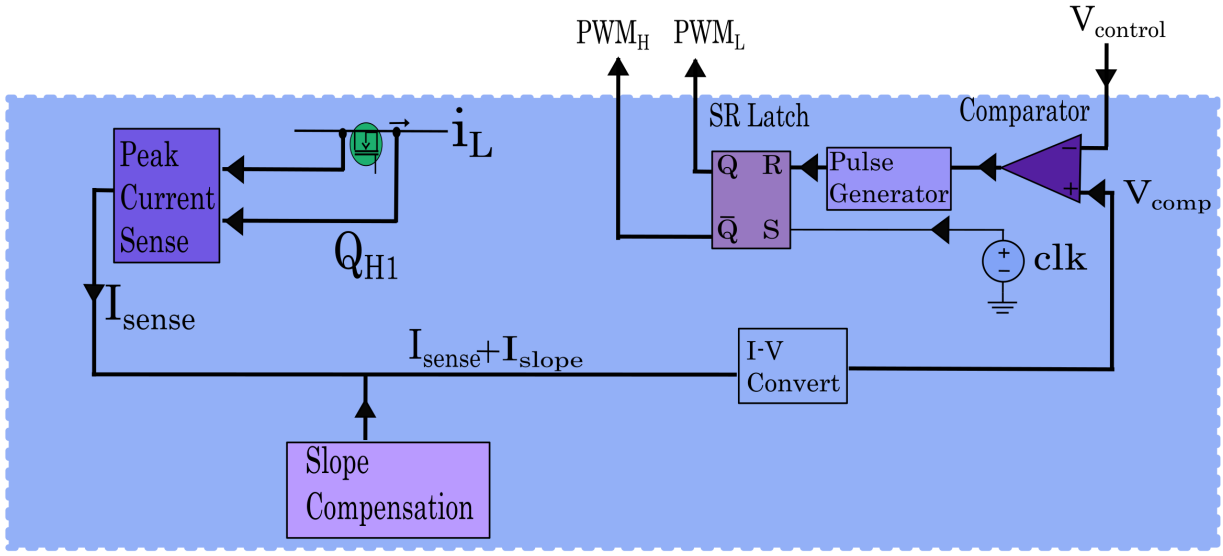

Figure 8-1: High level diagram showing the main blocks in the inner current loop.

A clock pulse is used to set the latch while the output of the comparator provides a reset signal. When the high-side MOSFET is on, the inductor is energized, and the inductor current increases. The current sensor measures this inductor current, and generates sensed current signal (I_{sense}), which is converted to sensed voltage signal (V_{sense}). An artificial ramp signal is then added to the sense voltage, V_{sense}, to compensate for sub-harmonic oscillations. When the sum of V_{sense} and the slope compensation ramp signal (V_{ramp}) exceeds the control voltage from the outer voltage loop, the comparator output pulses high. This initiates the discharge phase and the high-side MOSFET is turned off, the inductor is de-energized and the inductor current is decreased [17].

8.1 SR Latch

The SR latch takes the output from the current comparator (Reset) and a clock pulse of frequency f_{sw} (Set) and produces the PWM waveforms for the power MOSFETs. The latch output is used to determine when to turn the high-side MOSFET on/off.

The low-side MOSFET should turn on when:

- the voltage on the bootstrap capacitor is not high enough to provide a sufficienctly large boosted voltage. The low-side MOSFET therefore needs to turn on to provide a charging path for the capacitor to ensure this boosted voltage is high enough.
- the current comparator pulse is high. This means that the inductor current is higher than the limit and hence the high-side MOSFET must be turned off and the low-side MOSFET turned on.

The corresponding high-side MOSFET does the opposite of the low-side MOSFET. When a high input is applied to the set line of the SR latch, the Q output goes high, while $\overline{Q}$ goes low. The cross-coupled nand gate creates a feedback mechanism. Thus Q output will remain high, even when the S input goes low again. This is how the latch serves as a memory device. Conversely, a high input on the reset line will drive the Q output low and the $\overline{Q}$ high effectively resetting the latch's "memory". When both inputs are low, the system "latches" and it remains in its previously set or reset state. This circuitry includes a path that checks the level of the bootstrap capacitor voltage, in order to know when there is sufficient voltage before the high-side MOSFET can be turned on. It also includes a start signal which allows initial start up time for the system to settle before PWM pulses are output.

The system was designed to have blanking time so that when the high-side MOSFET transitions from off to on and ringing happens, these pulses do not cause false triggering and

resultant incorrect duty cycles on the PWM gate inputs. At the transistor level, the devices were designed to minimize any delays and are hence specified as minimum length devices. The SR latch circuit diagram that was designed is shown in Figure 8-2 below.

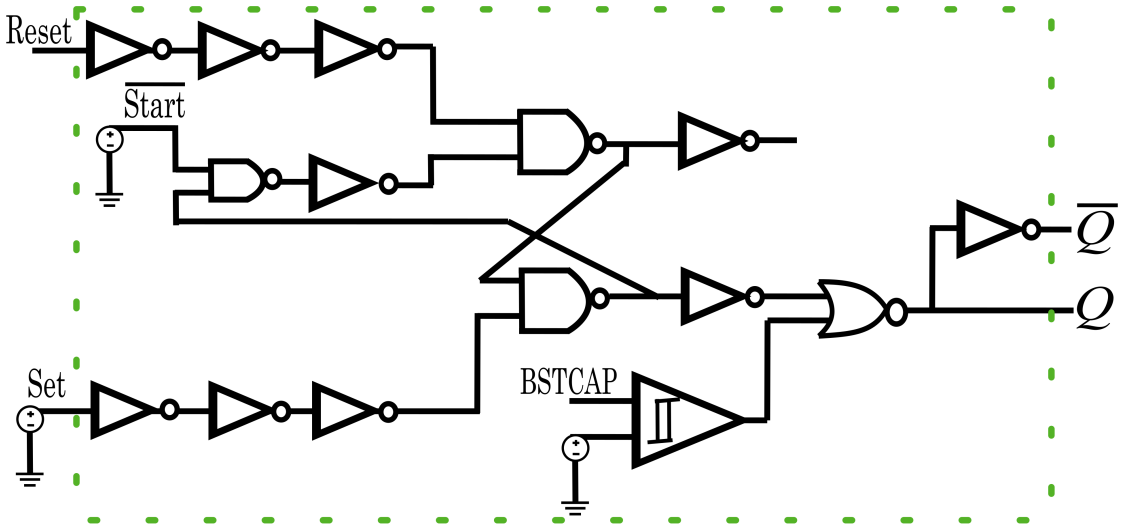

Figure 8-2: SR latch circuit diagram which produces a square wave pulse (Q) and an inverted copy (Qbar). These signals are fed to the gate drive block to produce the gate drive PWM signal for the two buck stages.

8.2 Current Sense

The sensed inductor current is compared with the control signal to generate reset pulses which control the turn-off of the power MOSFETs. Inductor current sensing must therefore be efficient, accurate, fast and immune to switching node noise. The main sensing methods [52] that were investigated include:

External Sense Resistor

In order to measure the inductor current, sense resistors can be placed in series with the inductor or load. By measuring the voltage drop across the resistor and using Ohm's law, the current flowing can be determined. This method has the disadvantage of requiring extra pins in the package just to sense current. It also causes extra power loss in the circuit, no matter how small the sense resistor is, since another dissipative element is added. Another drawback of this method is the cost, since highly accurate current sense resistors are prohibitively expensive.

Inductor Voltage

The voltage across the inductor is equal to the inductance times the change in current over

time. By integrating the voltage and knowing the inductor value, the current flowing through the inductor can be determined. This method however involves a complicated calculation and hence is not desirable as current needs to be sensed quickly.

MOSFET On-Resistance

Expanding on the idea of a sense resistor is the approach of using the power MOSFET's on-resistance was considered. The voltage can be measured across the transistor and the current flowing can therefore be determined. This method has the benefit of not requiring extra components, and not adding extra power losses into the system.

Sense-MOSFET

This last method uses a transistor, sized much smaller than the power MOSFET, by a ratio of approximately 1000:1. By forcing the same V_{ds} as the power MOSFET across the Sense-MOSFET, the current flowing through it is proportionally smaller by the same ratio. One issue of this approach is that the Sense-MOSFET must be designed to have extremely high matching, which can be difficult to achieve, as well as the sensing device must be located on chip, which can increase the footprint of the device [25].

High efficiency and fast sensing are crucial for this application, hence the Sense-MOSFET current sensing architecture was chosen. Since the TEC driver architecture employs feedback, any mismatches in the devices can be stabilized by the outer voltage loop's compensation. The fast current sensing will ensure that any over-currenting can be detected quickly, as well as minimize the minimum off time needed for the system which will allow the system to achieve high duty cycles.

8.3 Slope Compensation

The difference between the average inductor current and the DC value of the sampled inductor current can cause instability for certain operating conditions. This instability is the result of the sampled nature of the PCMC system, and is known as sub-harmonic oscillation [25, 44]. It occurs when the inductor ripple current does not return to its initial value by the start of next switching cycle. This causes alternating wide and narrow pulses at the switch node [44].

Slope compensation is a well-known and widely used technique of adding a ramp to the sensed inductor current to obviate the risk of subharmonic oscillation [41]. By adding a compensating ramp equal to the down-slope of the inductor current, any tendency toward

sub-harmonic oscillation is damped within one switching cycle as shown in Figure 8-3. Since the inductor value and input voltage are known, a ramp waveform of the inductor's down-slope was added to the sensed current to mitigate against any sub-harmonic oscillations.

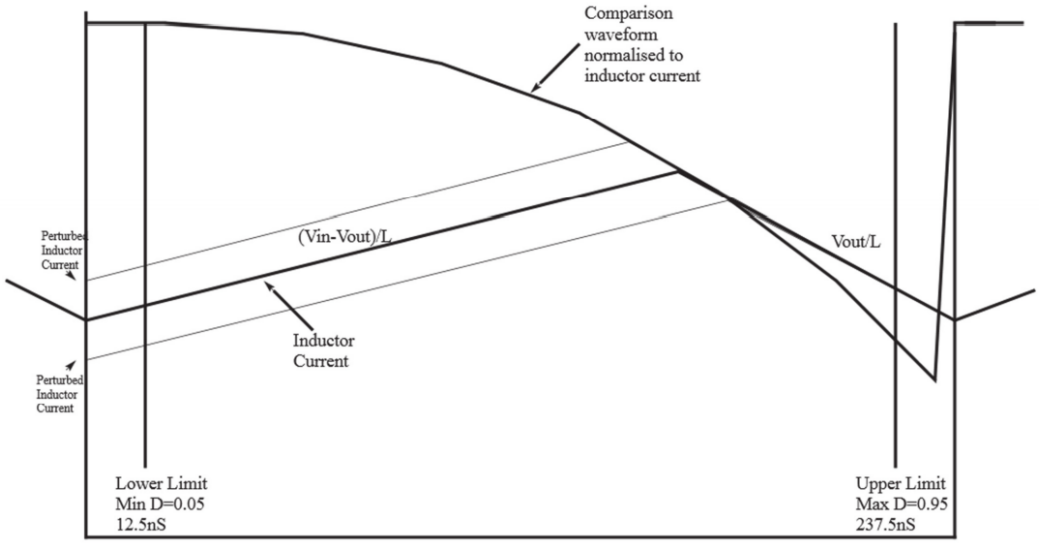

Figure 8-3: Non-linear slope compensation waveform used to prevent sub-harmonic oscillations when the system is run at duty cycles > 50 %.

8.4 Comparator

The state of the inductor current is naturally sampled by the PWM comparator. The comparator is needed to generate the pulse which tells the system when the high-side MOSFET current exceeds the limit (provided by the outer voltage loop). Any delays in the current comparator producing its output, therefore, impact the entire system. In order to achieve very high and very low duty cycles, the delay of the comparator must be minimized. Therefore, the comparator was designed at the transistor level to have very little delay and fast slew rates.

Chapter 9

System Evaluation

Chapters 6 - 8 detailed the following major architectural blocks:

- Gate Drive
- Outer Voltage Loop
- Inner Current Loop

These blocks constitute the new TEC driver architecture that was designed in this thesis project. This chapter summarizes the power, timing, and stability analysis of the complete TEC driver architecture, demonstrating how the following design targets were met:

- Efficiency
- Output voltage dynamic range
- Stability

Figure 9-1 below summarises the high-level TEC driver that was designed in this thesis.

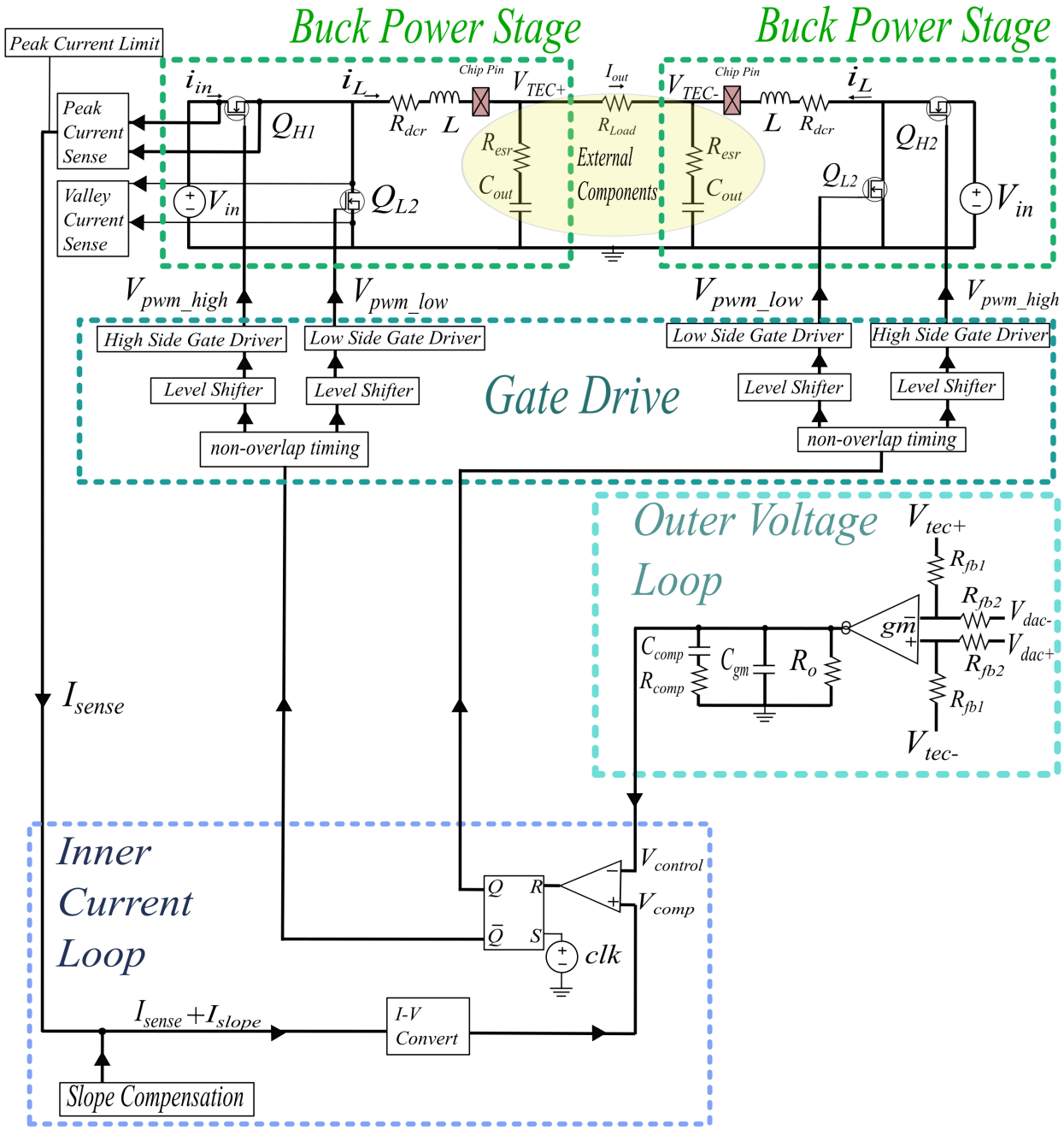

Figure 9-1: Diagram summarizing the major components that were designed and analyzed in the novel peak current mode TEC driver architecture.

9.1 Power Analysis

Efficiency [43] was a key metric in the design of the TEC driver. The difference in energy into the system and energy out is converted to heat. Generating excess heat when trying to cool negatively impacts the TEC operation. This excess heat further requires the system to integrate complex heat removal schemes. High efficiency is critical for achieving high power density. The lower the efficiency, the less useful the product is. Therefore, high efficiency is imperative.

A maximum output power (P_{Out}) budget was calculated assuming maximum power intake and worst-case scenarios for each component to ensure the overall system η was > 95 %.

Worst Case Operating Condition

- $V_{gs} = 2.7$, T = 150°. This corresponds to $R_{ds,on} = 34$ mΩ.
- I_{out} at ± 1.5 A. This corresponds to the maximum duty cycles, D = 0.95 for one buck stage, and D = 0.05 for the other buck stage.

As outlined in Chapter 2, the target η of this novel peak current mode TEC driver architecture is 95 %. For a nominal input voltage of 5 V, and with duty cycle limitations, the maximum achievable output swing for the system is 4.75 to - 4.75 V. This provides ± 1.5 A current to the TEC.

For an η of 95:

$$\begin{aligned} \eta &= \frac{P_{out}}{P_{out} + P_{loss}} * 100 \\ \mu &= \frac{V_{out} I_{out}}{V_{out} I_{out} + P_{loss}} \\ P_{loss} &= V_{out} I_{out} \frac{(1-\mu)}{\mu} \\ &\approx 4.75 * 1.5 * \frac{(1-0.95)}{0.95} \\ &= 0.375 \text{ W} \end{aligned} \tag{9.1}$$

Therefore, as calculated in Equation 9.1 above, the maximum power loss budget is **375 mW**.

The following list presents the main avenues for power losses in this dual buck TEC driver architecture.

1. Power loss due to MOSFET (P_{FET})
    - Power loss due to conduction (P_{cond}) from the MOSFETs $R_{ds,on}$
    - Power loss due to MOSFET switching (P_{sw})
    - Power loss due to gate charge (P_{GateQ})
    - Power loss due to the low-side MOSFET's body diode (P_{LS})
2. Power loss due to inductor (P_{ind})
3. Power loss due to capacitor (P_{cap})

These losses are discussed in Sections 9.1.1 to 9.1.3.

9.1.1 MOSFET Losses

Power MOSFETs are voltage controlled four terminal semiconductor devices that are used as switches. In a NMOS device, when a positive voltage is applied to the gate terminal, holes in the p-type substrate are driven away and an n-type inversion layer forms between the source and drain. This electrically connects the drain and source, and causes a current to conduct through the channel [4, 15, 38]. Therefore, the gate voltage modulates the conductivity of the channel. The devices are either fully conducting, with a small on resistance, or switched off, with a very high impedance. Since their voltage is nearly zero when on and the current is nearly zero when off, power dissipation is minimized.

In the NMOS, charge is stored in the gate electrode, conducting channel, depletion layers as well as parasitic capacitance. The following parasitic resistances and capacitances determine the turn-on times and hence affect power loss in the device:

- Overlap capacitance (C_{os}, C_{od}) between the gate electrode and highly doped source and drain region
- Junction capacitance (C_{js}, C_{jd}) between the substrate and source and drain
- Capacitances between the metal electrodes and the source, drain, and gate

Conduction Loss

Conduction losses in MOSFETs are due to the power dissipated through the $R_{ds,on}$ of the channel as current flows when the device is on. P_{cond} is inversely proportional to the

MOSFET size, the larger the MOSFET, the lower the $R_{ds,on}$, and hence the lower the conduction loss. In the buck converter, while the high side MOSFET is on, the bottom is off and vice versa. Figure 9-2 below shows the current flow in the MOSFET device.

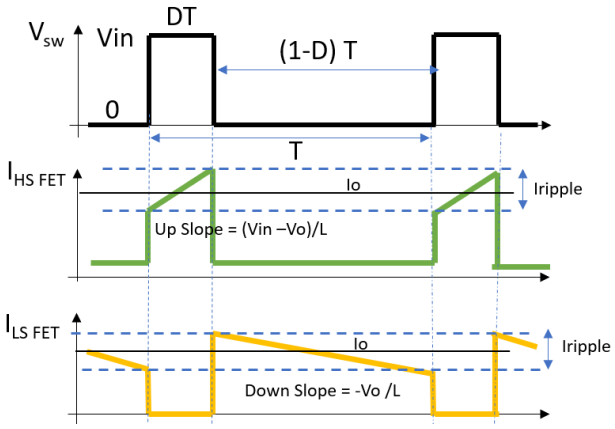

Figure 9-2: Waveforms showing the current flow in the buck converter.

The total conduction loss is therefore the sum of the high-side and low-side MOSFET conduction losses, illustrated in Equation 9.2 below.

$$\begin{aligned} P_{cond_{Total}} &= P_{cond_{HS}} + P_{cond_{LS}} \\ P_{cond_{HS}} &= D I^2_{rms_{HS}} * R_{ds,on_{HS}} \\ P_{cond_{LS}} &= (1-D) I^2_{rms_{LS}} * R_{ds,on_{LS}} \end{aligned} \tag{9.2}$$

In the worst case scenario, the maximum root mean square current (I_{rms}) occurs when the maximum output current, 1.5 A, flows.

$$\begin{aligned} I^2_{rms} &= I^2_o + \frac{\Delta I^2}{12} \\ \Delta I &= \frac{(V_{IN} - V_{Out})}{L} DT = 30\% \cdot I_{out} \\ I_{rms} &= I_o * 1.00375 \text{ A} \end{aligned} \tag{9.3}$$

As shown in Equation 9.3 above, since the ripple has been made very small due to all the design choices made in the TEC driver, its impact is negligible.

For the dual buck architecture, when one leg's high-side MOSFET is on and the low-side MOSFET is off, the other leg's low-side MOSFET is on and the high-side MOSFET is off.

Therefore, when 1.5 A flows, one buck will have a 95 % high-side duty cycle and 5 % low-side duty cycle, while the other buck has 5 % high-side duty cycle and 95 % low-side duty cycle. The maximum conduction loss is given in Equation 9.4 below.

$$\begin{aligned} P_{cond} &= DI_o^2 R_{ds,on} + (1-D)I_o^2 R_{ds,on} + DI_o^2 R_{ds,on} + (1-D)I_o^2 R_{ds,on} \\ &= 2I_o^2 R_{ds,on} \\ &= (1.5)^2 * 2 * 34e^{-3} \\ &= 153 \text{ mW} \end{aligned} \tag{9.4}$$

Switching Losses

When a MOSFET is either on or off, the power it dissipates is small. During a transition between the two states, however, both a large current and a large voltage exist simultaneously. The intrinsic capacitance of the devices stores and dissipates energy during the transitions. As such, switching losses are caused by the dynamic voltages and currents during the turn on/off times and are proportional to f_{sw} and parasitics.

- **Turn On and Turn Off Transitions**

  When a switch is turned off, the current does not instantly fall to zero, the channel still conducts, and an increasing drain to source voltage develops across the channel. This crossover loss is a function of the switching speed of the MOSFET (gate resistance, gate-source capacitance, and gate-drain capacitance).

  The stages of the device turn on and turn off are illustrated in Figure 9-3. The turn on sequence, as shown in the bottom graph of the figure involves the following states:

  1. t_0: $V_{gs} < 0$. Therefore the NMOS is off.
  2. t_1: V_{ds} reaches the threshold voltage, V_t.
  3. t_2: The MOSFET begins to turn on, I_{ds} increases from zero.
  4. t_3: The MOSFET keeps turning on, I_{ds} and V_{gs} reach steady state while V_{ds} decreases from V_{In} to 0.
  5. $> t_3$: Device is fully on.

  The P_{sw} occurs when I_D and V_{ds} are both non-zero, corresponding to period t_2 and t_3.

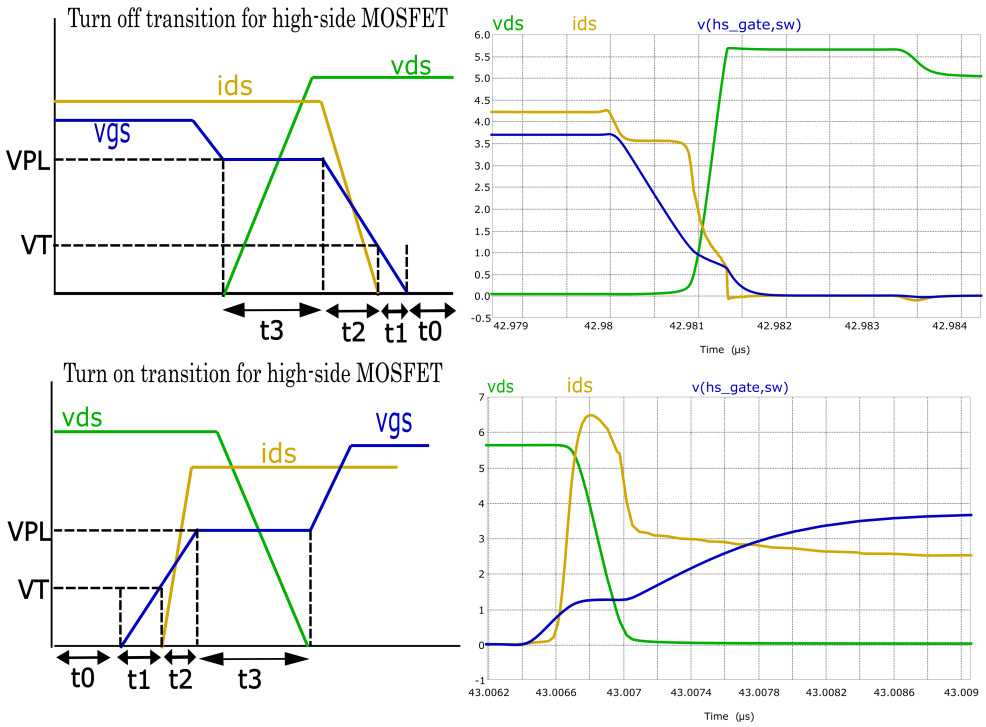

Figure 9-3: Waveforms showing how the current and voltage change during the high-side MOSFET's switching transitions.

Both of the low-side MOSFET's turn-on and turn-off are soft switching at normal operations. The load current continues to flow through the body diode after it is turned off, thus the drain voltage equals the forward direction voltage and stays low, hence the losses are very small and can be neglected.

Therefore, the P_{sw} losses are due to the high-side MOSFET's switching transitions.

The integral of the power dissipated in the transistor during both the turn-on and the turn-off transition is the switching energy lost per cycle, as shown in Equation 9.5 below. This energy, multiplied by the f_{sw} represents the switching component of the dissipated power, as illustrated in Figure 9-4.

$$\begin{aligned} P_{sw} &= \int (P_{sw,rise} * f_{sw}) + \int (P_{sw,fall} * f_{sw}) \\ &= (1.2266 - 1.2254)\mu J \cdot 5\text{MHz} + (1.248 - 1.2466)\mu J \cdot 5\text{MHz} \\ &\approx 14 \text{ mW per buck stage} \\ P_{sw,total} &= 28 \text{ mW} \end{aligned} \tag{9.5}$$

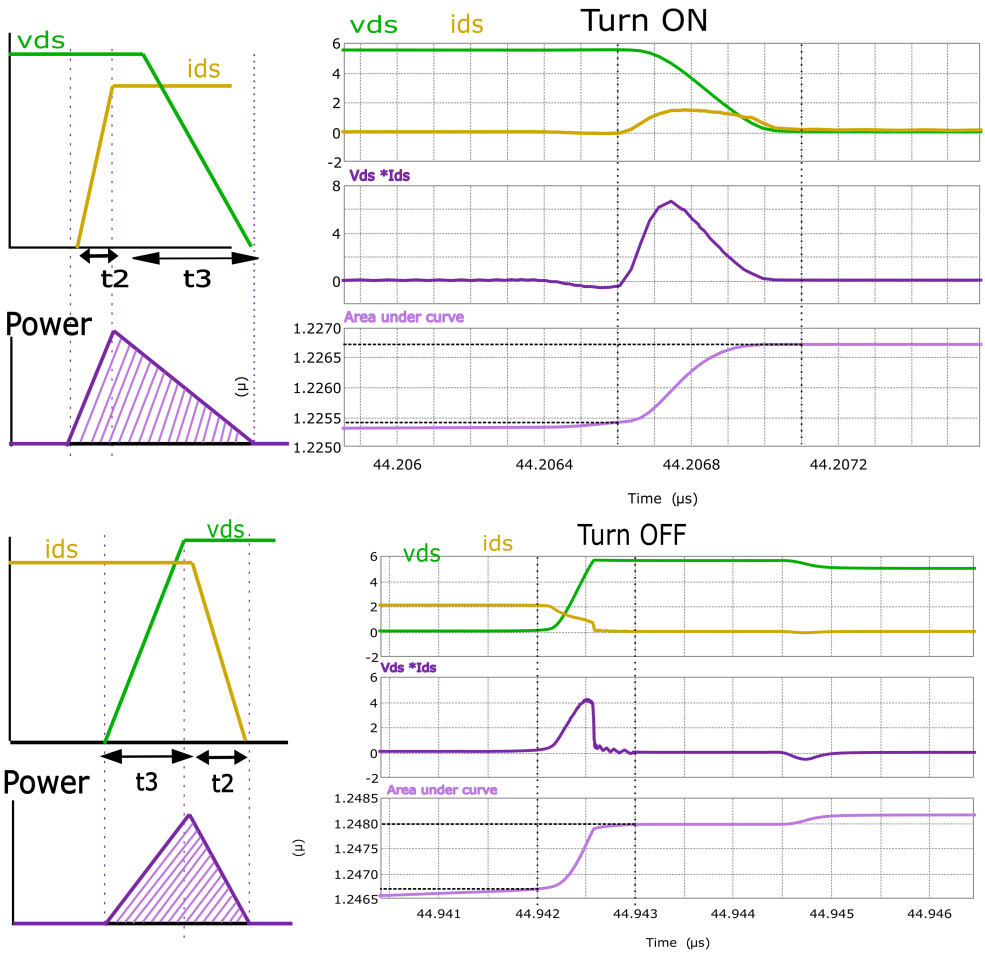

Figure 9-4: Power loss during the high-side MOSFET's switching transitions.

- **Gate Charge Loss**

  P_{GateQ} is due to periodic charging and discharging of the MOSFET's gate capacitance. During the turn on or turn off phase, output capacitance must be charged/discharged. When a voltage across a capacitor changes, a certain amount of charge must be transferred. P_{GateQ} is therefore caused by the energy required to charge/discharge the MOSFET's gate capacitance, as calculated in Equations 9.6 and 9.7. The average bias current required to drive the gate $= Q_{gate} \cdot f_{sw}$.

$$\begin{aligned} Q &= CV = It \\ E &= QV = Pt \\ P &= \frac{E}{t} = CV^2 f_{sw} = (C_{G,H} + C_{G-L}) * V_{drive}^2 * f_{sw} \end{aligned} \tag{9.6}$$

Figure 9-5 below shows the simulation results used to calculate the gate charge losses.

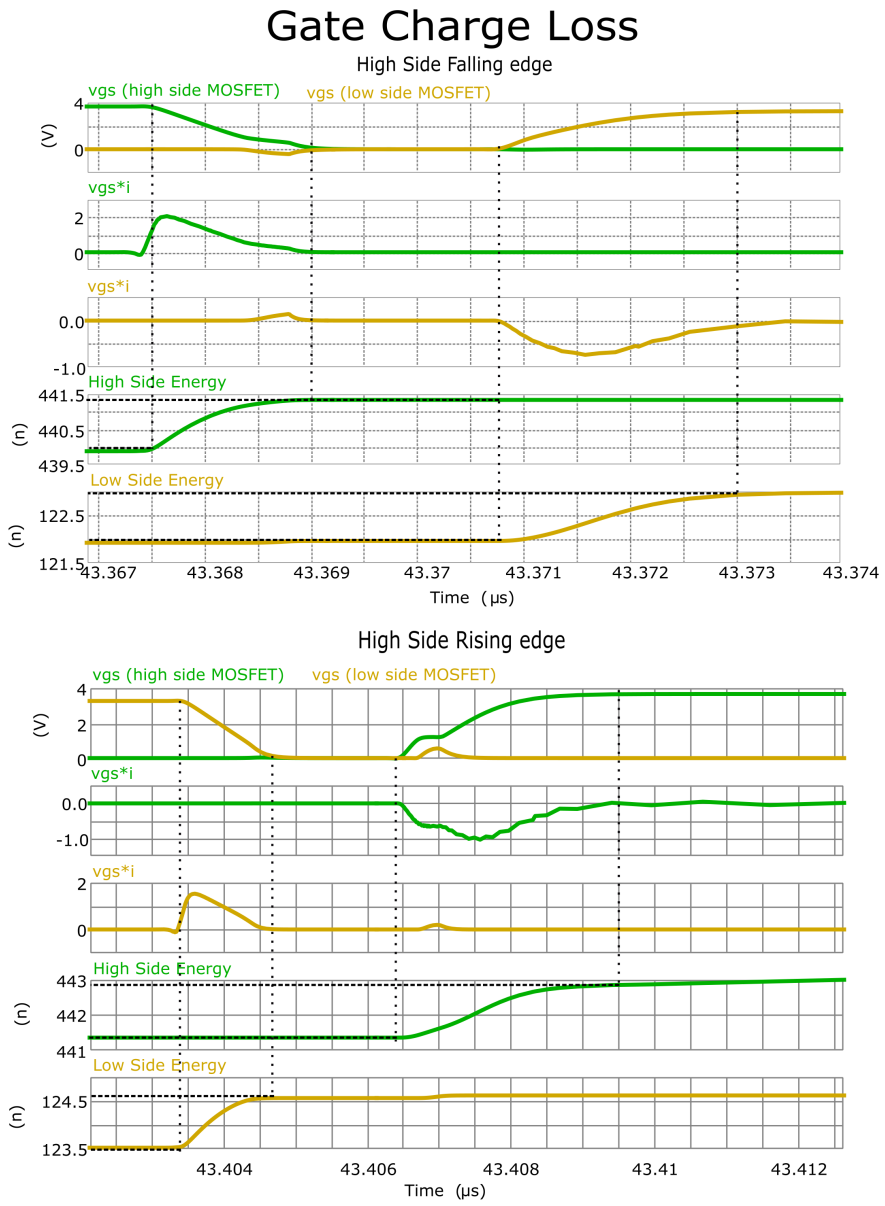

Figure 9-5: Simulation results showing the gate drive losses.

$$
\begin{aligned}
P_{GateQ} &= (4.4136e^{-7} - 4.4227e^{-7}) * 5e^{6} + (1.235e^{-7} - 1.2457e^{-7}) * 5e^{6} \\
&\quad + (4.3897e^{-7} - 4.4135e^{-7}) * 5e^{6} + (1.2196e^{-7} - 1.2295e^{-7}) * 5e^{6} \\
&\approx 24.6 \text{ mW per buck stage} \\
P_{Qgate,total} &= 49 \text{ mW}
\end{aligned}
\tag{9.7}
$$

- **Low-side Body-Diode Loss**

  The P_{LS} introduces two power losses into the system: dead-time loss (diode conduction loss) and diode reverse-recovery loss. When the high-side MOSFET is turned on, the transition of the body diode of the low-side MOSFET from the forward direction to the reverse bias state causes a diode recovery, which generates a reverse recovery loss in the body diode. In order to prevent the cross-conduction of the high-side MOSFET and low-side MOSFET, a rise edge dead-time between low-side MOSFET turnoff and high-side MOSFET turn on, and fall edge dead-time between high-side MOSFET turnoff and low-side MOSFET turn on are added. During these two dead-time intervals, both the high-side and the low-side MOSFETs are off preventing current spikes, while the inductor current flows through the low-side MOSFET's body-diode. Figure 9-6 below shows the dead time delays for the system.

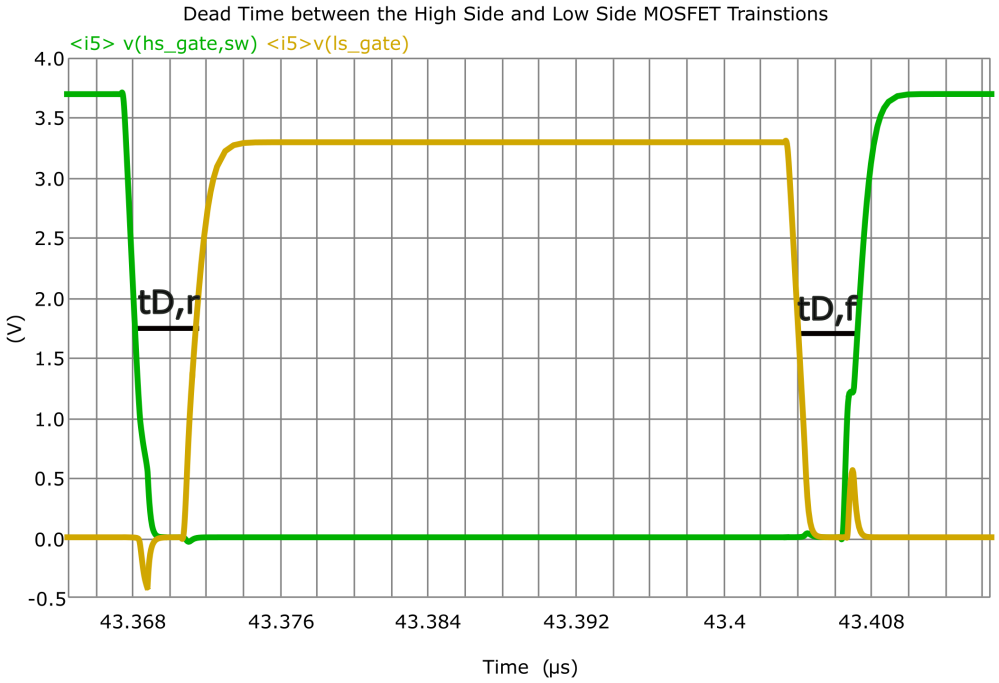

Figure 9-6: Power losses due to the non-overlapping time.

The power loss due to the low-side MOSFET is calculated in Equation 9.8.

$P_{LS} = V_D * I_o + (tD_r + tD_f) * f_{sw}$ where:

- V_D is the low-side MOSFET's body-diode forward voltage 0.4 V
- I_o is the output current 1.5 A
- tD_r is the dead time at the rising edge 3.26 ns

– tD_f is the dead time at the falling edge 3.2 ns

– f_{sw} is 5 MHz

$$\begin{aligned} P_{LS} &= 0.4 * 1.5 + 6.46e^{-9} * 5e^{6} \approx 30 \text{ mW} \\ P_{LS,total} &= 60 \text{ mW} \end{aligned} \tag{9.8}$$

9.1.2 Inductor Losses

An inductor is a reactive component that acts as an energy storage device and ideally is lossless, however, due to parasitics, power is dissipated.

DC Resistance Losses

The current that flows though the inductor during the operation of the TEC driver is shown in Figure 9-7 below.

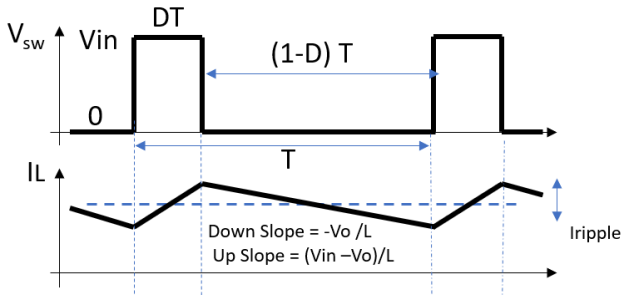

Figure 9-7: Inductor current ripple as the current ramps up when the inductor is energized and then ramps down when off.

Power is lost through the inductor DC resistance (R_{dcr}) and the core losses. The P_{ind} is generated by the R_{dcr} of the winding that forms the inductor. The R_{dcr} increases as the wire length increases; but decreases as the wire cross-section increases. Since the power loss is proportional to the square of the current, a higher output current results in a greater loss. Equation 9.9 shows the calculated power losses due to the inductor.

$$\begin{aligned} P_{cond_{ind}} &= DI^2_{rms_{HS}} * R_{L_{dcr}} \\ &= (1.5)^2 \cdot 30 \\ &= 67.5 \text{ mW} \end{aligned} \tag{9.9}$$

9.1.3 Capacitor Losses

There are several losses generated in the capacitor—including series resistance, leakage, and dielectric loss. These losses are simplified into a general loss model as the esr. P_{cap} is calculated by multiplying the esr by the square of the rms value of the AC current flowing through the capacitor. Equation 9.10 shows the power loss from the capacitor.

$$\begin{aligned} P_{cond_{HS}} &= I^2_{rms_{Cout}} * R_{esr} \\ I^2_{rms_{Cout}} &= \frac{\Delta I_o}{2\sqrt{3}} \\ &\approx 2(\frac{0.9}{2\sqrt{3}})^2 30 \approx 4.05 \text{ mW} \end{aligned} \tag{9.10}$$

Overall Efficiency Calculation

As calculated in Equation 9.1, the maximum tolerable power loss for the system to achieve 95 % efficiency was found to be 375 mW. This power loss comprises the losses from the MOSFETs, the inductor and capacitor. From the power losses of these components, the total power loss of this TEC driver system was calculated, as shown in Equation 9.11 below.

$$\begin{aligned} P_{total} &= P_{FET} + P_{ind} + P_{cap} \\ P_{FET} &= P_{Cond} + P_{sw} + P_{GateQ} + PLSBody \\ &= 153 \text{ mW} + 28 \text{ mW} + 49 \text{ mW} + 60 \text{ mW} \\ P_{ind} &= 67 \text{ mW} \\ P_{cap} &= 4 \text{ mW} \\ P_{total} &= 153 + 28 + 49 + 60 + 67 + 4 = 361 \text{ mW} \end{aligned} \tag{9.11}$$

Therefore, with a power loss of 361 mW, the overall system efficiency, evaluated at the worst case-operating conditions was found to be 95.1 %. This meets the design targets set forth for the TEC driver system.

9.2 Timing Analysis

In order to achieve a large temperature differential, the current flowing through the TEC must be maximized. Hence, a large voltage range across the TEC is required. The system must therefore be operable at very high and very low duty cycles. In order to maximize the duty cycle range, any system delays must be minimized. That is, the minimum time that the MOSFET switches must be on must be minimized to achieve low duty cycles and the minimum time that the switches must be off should be minimized to achieve very high duty cycles.

These system delays, are introduced by all the blocks that were designed in the previous sections. Figure 9-8 illustrates the delay path through the circuit. The main delays are introduced by time needed to sense currents, the non-overlapping timing block, and blanking time which is used to avoid false resetting of the PWM pulse when the high-side MOSFET rings on switching transitions. These limit the minimum output voltage that the converter can generate for a given input voltage and switching frequency.

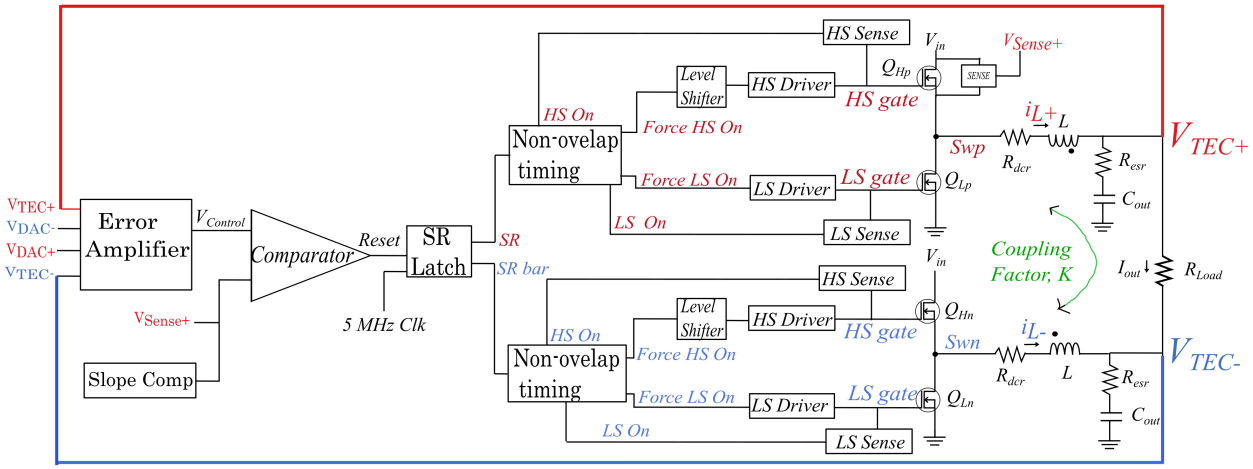

Figure 9-8: Delay path through the full TEC driver circuit showing why the system has minimum on and off time constraints.

Minimum On-time Calculation

The following cases detail the major delays that contribute to the system having minimum on-time constraints:

- **CASE 1: Positive Inductor Current**

  (Positive current flow is taken as current flowing from input voltage supply to output.)

  – Blanking time for the high-side MOSFET current comparator

- Current comparator delay
- Turn-off delay of high-side MOSFET driver

- **CASE 2: Negative Inductor current**
  - Blank time for high-side MOSFET current comparator
  - Current comparator delay
  - Turn off delay of high-side MOSFET driver
  - Dead time (delay from high-side MOSFET OFF - low-side MOSFET on)

Minimum Off-Time Calculation

The following cases detail the major delays that contribute to the system having minimum off-time constraints:

- **CASE 3: Positive Inductor current**
  - Dead time (delay from high-side MOSFET off - low-side MOSFET on)
  - Minimum on-time of low-side MOSFET
  - Turn off delay of low-side MOSFET driver
- **CASE 4: Negative Inductor current**
  - Minimum on-time of low-side MOSFET
  - Turn off delay of low-side MOSFET driver

With a f_{sw} of 5 MHz, this means that the period of one switching cycle is 200 ns.

Therefore, in order to achieve the required range of 95 % to 5 % duty cycles at a f_{sw} of 5 MHz, the required on-times are 0.95·200 ns and the off-times are 0.05·200 ns.

Therefore, all the system delays must be $<$ 10 ns.

9.3 Stability Analysis

The closed loop transfer functions described in Table 4.2 are used ensure that the system is stable in the face of any disturbances in V_{in}, V_{ref} and load current. The step response of the closed loop transfer functions of the macro-model system were modelled using MATLAB's Simulink models as shown in Figure 9-9. The step responses for the transistor-level driver circuit designed in Cadence-Virtuoso as shown in Figures 9-10 to 9-15 were also run, with the main metrics of overshoot, steady state error, and settling time analyzed.

Simulink Step Response for the macro-model design

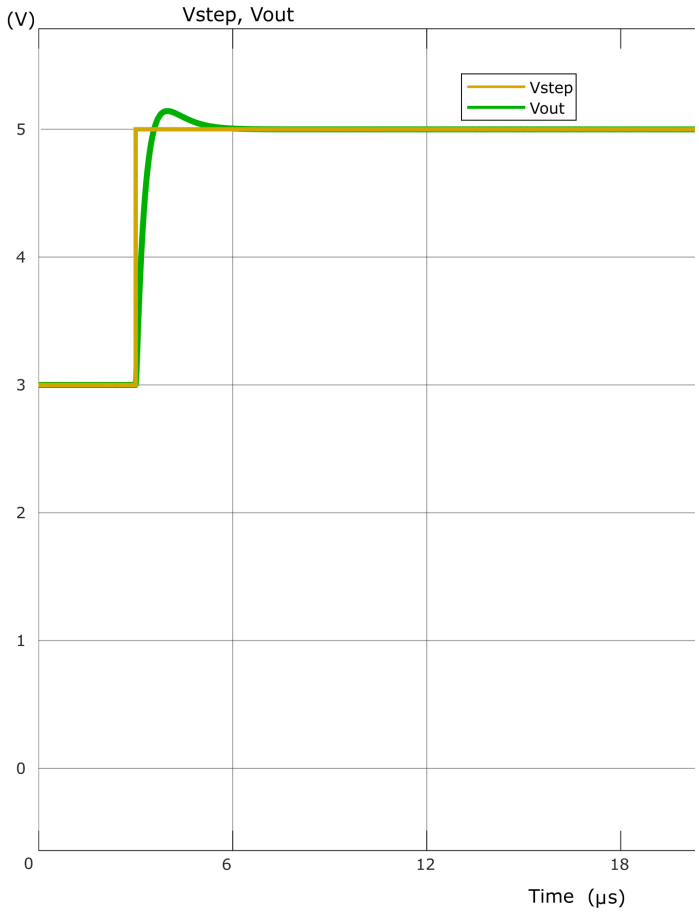

Figure 9-9: Transient simulation using MATLAB's Simulink program to simulate the block diagram for a voltage step and show the behaviour of the output voltage seen across the TEC. There is slight overshoot but the system settles back to its original value after 6 μs.

Cadence-Virtuoso step responses for the transistor-level TEC driver

V_{ref} Step Responses

Figures 9-10 and 9-11 below show the results when a transient step in the reference voltage, V_{ref} is applied to the system. Both responses show that the output voltage seen by the TEC has a well-damped response, with minimal oscillations and a settling time of 4 μs.

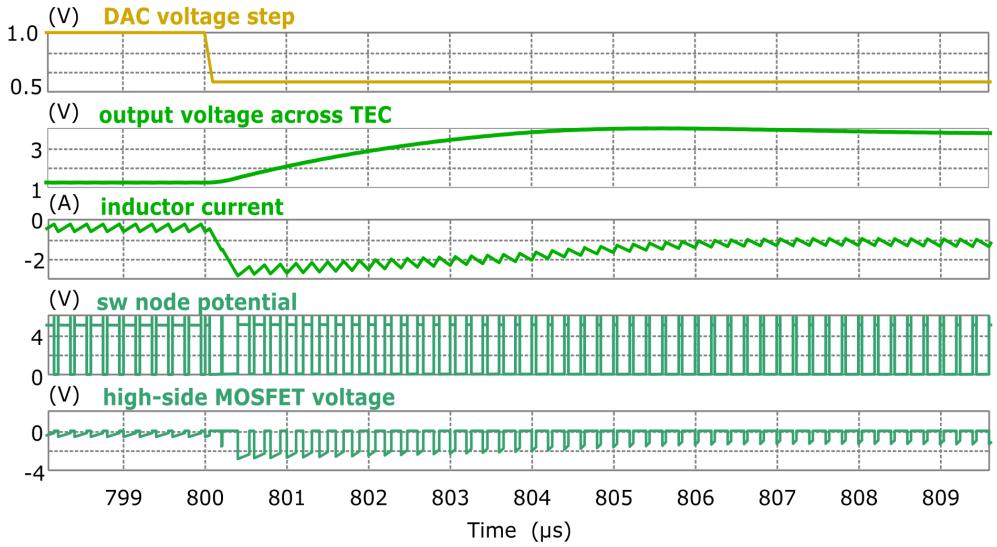

Figure 9-10: Transient simulation for a reference voltage (V_{ref}) step from 1 V to 0.5 V, for a nominal V_{in} of 5 V, showing the output voltage and output current seen across the TEC.

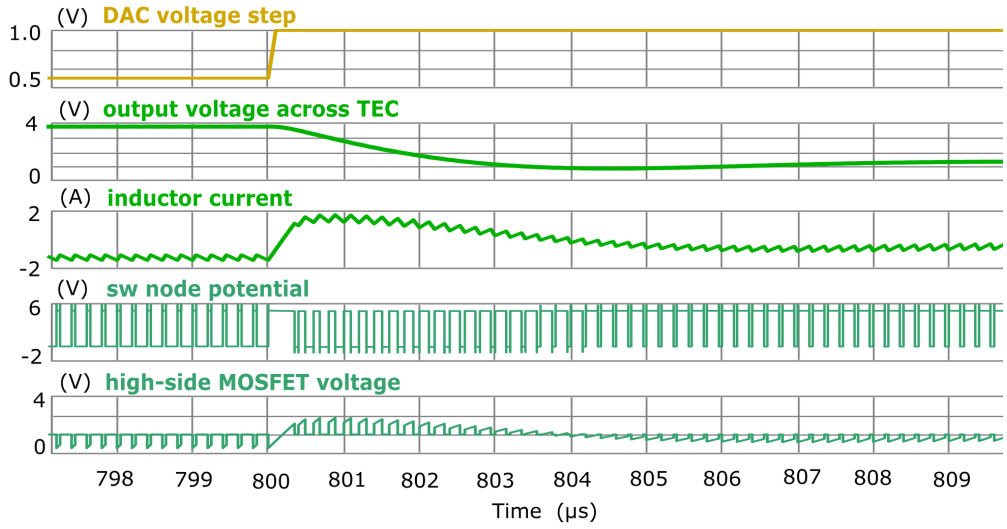

Figure 9-11: Transient simulation for a reference voltage (V_{ref}) step from 0.5 V to 1 V, for a nominal V_{in} of 5 V, showing the output voltage and output current seen across the TEC.

Figures 9-12 and 9-13 below show the results when a step in the input voltage, V_{in} is applied to the system. Both responses show that the output voltage seen by the TEC has a well-damped response, with minimal oscillations and overshoot, and a settling time of 6 μs.

V_{in} Step Responses

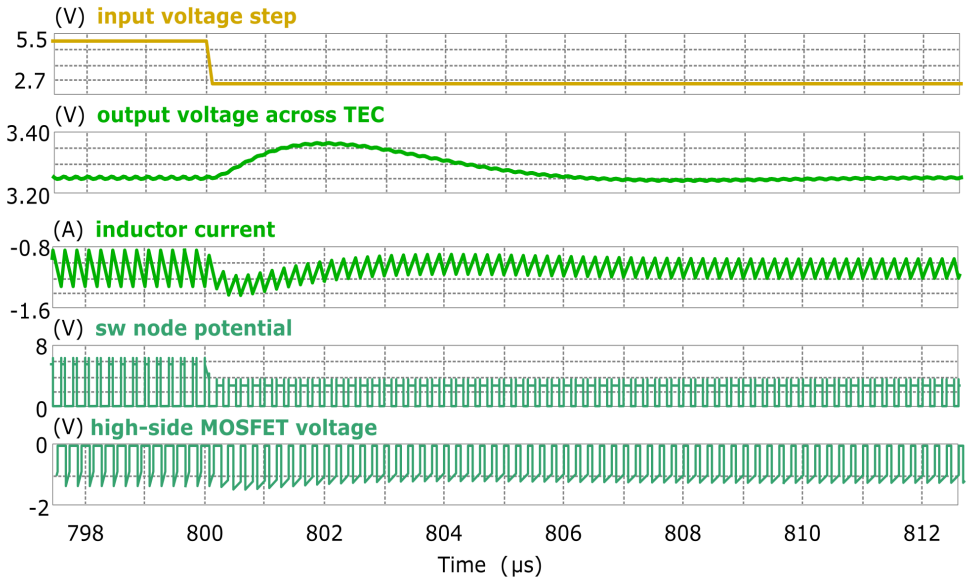

Figure 9-12: Transient simulation for an input voltage (V_{in}) step from 2.7 V to 5.5 V, showing the output voltage and output current seen across the TEC.

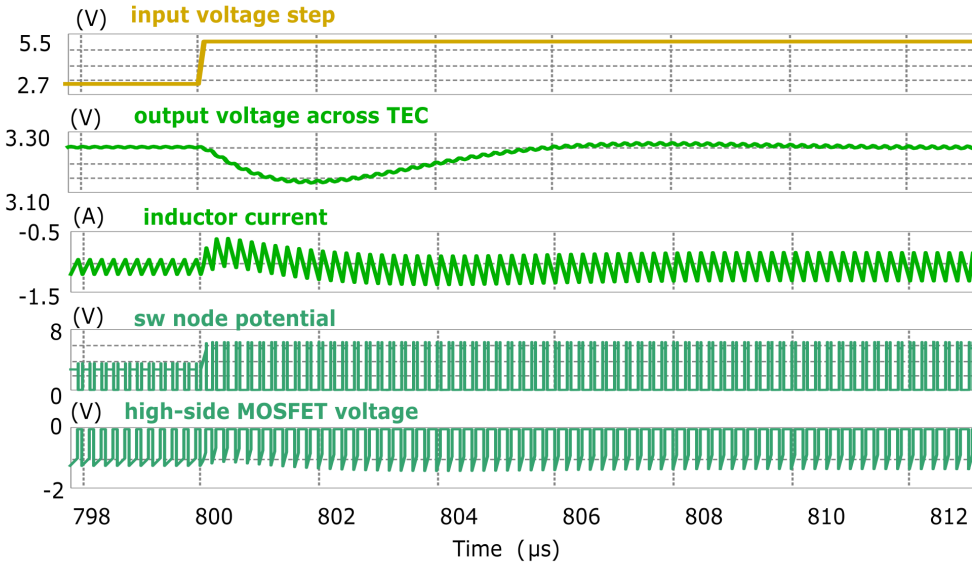

Figure 9-13: Transient simulation for an input voltage (V_{in}) step from 5.5 V to 2.7 V, showing the output voltage and output current seen across the TEC.

Load Current Step Responses

Figures 9-14 and 9-15 below show the results when a step in the load current through the TEC is applied to the system. Both responses show that the output voltage seen by the TEC has a well-damped response, with minimal oscillations (one lobe), slight overshoot, and a settling time of 6 μs.

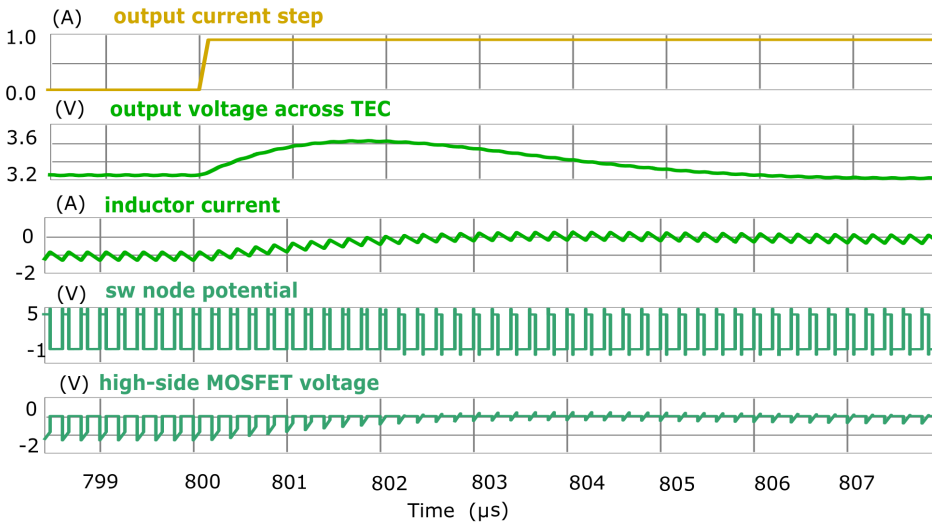

Figure 9-14: Transient simulation for a a load step from 1.35 A to 0.5 A, for a nominal V_{in} of 5 V, showing the output voltage and output current seen across the TEC.

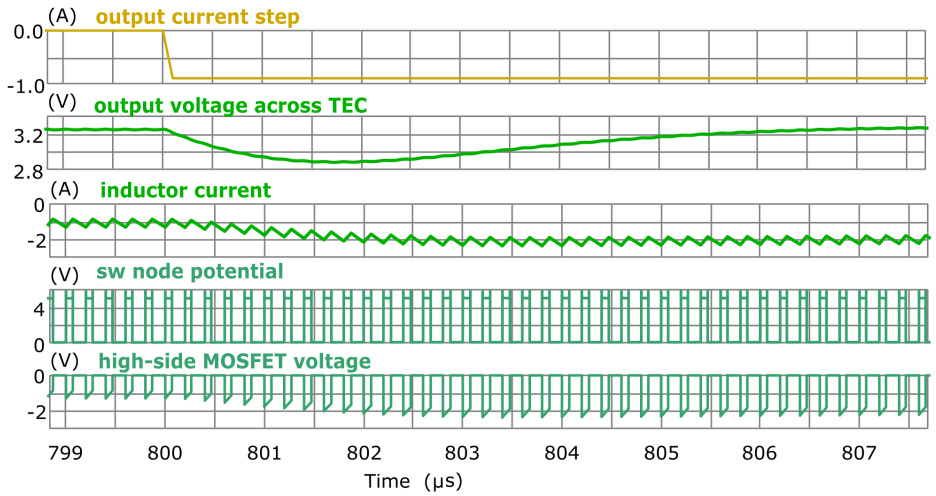

Figure 9-15: Transient simulation for a a load step from 0.5 A to 1.35 A, for a nominal V_{in} of 5 V, showing the output voltage and output current seen across the TEC.

These results confirm that the TEC driver has a stable, well-damped response to disturbances.

Chapter 10

Conclusion

This research project aimed to develop a new compact, very efficient, high frequency driver for a TEC designed to operate as a temperature controller to heat and cool a photonics laser system. There are currently no TEC driver products that meet all the specifications of this driver.

After exploring various architectures, a peak current mode dual buck H-bridge TEC driver was designed. This design involved three major blocks: a gate drive, outer voltage loop and inner current loop. This novel TEC driver was simulated and analyzed and provided promising outcomes. It ensured that the design targets of simple design, small size, high stability and fast transient response, 5 MHz speed of operation, $>$ 95 % efficiency, low ripple current, and large dynamic range for the differential voltage across the TEC were met.

The simulated design's behaviour matched well with the mathematical modelling of the system and thus provides valuable insight for TEC driver architectures. Although a full IC circuit for the TEC driver was not manufactured, the simulated results were able to demonstrate that this TEC driver architecture met the following targets.

- Allows TEC differential voltage range of $\pm$ 0.95V_{in}
- Provides a maximum output current of $\pm 1.5A$
- Has a maximum ripple current across the TEC of 30 % I_{out}
- Operates while the input voltage ranges from 2.7 V to 5.5 V
- Has a worst-case efficiency of 95 %

- Has an ultra-compact IC package with an integrated inductor
- Has a stable response to disturbances.

Future Work

The next steps in realising this novel TEC driver architecture design into a product include:

- integrating more protection systems to comply with safety regulations. Protections such as under-voltage protection, soft start-up, and static protection for the chip will be designed and integrated into the TEC driver architecture that was developed in this thesis.
- IC manufacture. The circuit-level TEC architecture schematics must be laid out, sent to a foundry to be manufactured and integrated with the inductor, which is being sourced by a third party company. The IC must then be be vigorously tested, to ensure that its behaviour complies with the outlined design targets.

Although this work provides a strong foundation for future iterations, limitations of this architecture that were identified though the design process muist be noted. With such a small package size, challenges may arise in the design of the magnetics for the system- which limits the size of the filter components that can be used. Furthermore, with the high frequency of operation, there are inherent duty cycle limitations. This peak current mode TEC driver will only be compatible with systems that require maximum output voltage ranges and duty cycles < 95 %.

Despite the identified limitations of this architecture, new applications were also realized. In addition to TEC driver applications, this peak current mode dual H-bridge architecture shows great promise to be used in several other applications due to its small size and high efficiency. This TEC driver circuit architecture can be modified in the future to be used in several applications where a small, highly efficient dual channel buck converter is needed.

Appendix A

Linear Regulator-Buck Architecture Gain Calculations

This section provides a detailed derivation of the gain parameters S_{gain} and L_{gain} for the linear regulator-buck architecture shown in Figure A-1 below.

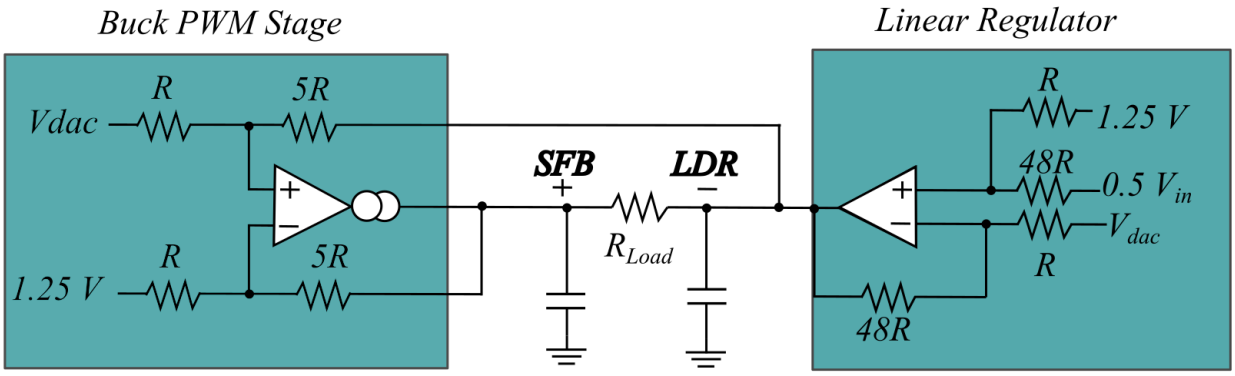

Figure A-1: Single-ended buck-linear regulator architecture.

Equations A.1 to A.8 provide the step-by-step analysis of how the gaind were derived.

- Using the Kirchhoff's Current Law: Current into node = current out of node
- Due to the high input impedance, no current flows into the V+ and V- op amp terminals
- For an op amp: V+ = V-

$$\begin{aligned} \frac{\frac{V_{in}}{2} - V^+}{L_{gain}R} &= \frac{V^+ - 1.25}{R} \frac{V_{in}}{2} - V^+ = L_{gain}(V^+ - 1.25) \\ V^+ &= \frac{\frac{V_{in}}{2} + L_{gain}1.25}{L_{gain} + 1} \end{aligned} \tag{A.1}$$

$$\begin{aligned} \frac{V_{DAC} - V^+}{R} = \frac{V^+ - V_{LDR}}{L_{gain}R} = L_{gain}(V_{DAC} - V^+) = V^+ - V_{LDR} \\ V_{LDR} = V^+(1 + L_{gain}) - L_{gain}V_{DAC} \end{aligned} \tag{A.2}$$

$$\begin{aligned} V_{LDR} &= \frac{\frac{V_{in}}{2} + L_{gain}1.25}{L_{gain} + 1}(1 + L_{gain}) - L_{gain}V_{DAC} \\ V_{LDR} &= \frac{V_{in}}{2} - L_{gain}(V_{DAC} - 1.25) \end{aligned} \tag{A.3}$$

$$\begin{aligned} \frac{V_{DAC} - V^+}{R} = \frac{V^+ - V_{LDR}}{S_{gain}R} S_{gain}(V_{DAC} - V^+) = (V^+ - V_{LDR}) \\ V^+ = \frac{S_{gain}V_{DAC} + V_{LDR}}{(1 + S_{gain})} \end{aligned} \tag{A.4}$$

$$\begin{aligned} \frac{1.25 - V^+}{R} = \frac{V^+ - V_{SFB}}{S_{gain}R} S_{gain}(1.25 - V^+) = (V^+ - V_{SFB}) \\ V_{SFB} = V^+(1 - S_{gain}) - S_{gain}(1.25) \end{aligned} \tag{A.5}$$

$$\begin{aligned} V_{SFB} &= \frac{S_{gain}V_{DAC} + V_{LDR}}{(1 + S_{gain})}(1 + S_{gain}) - S_{gain}1.25 \\ V_{SFB} &= V_{LDR} + S_{gain}(V_{DAC} - 1.25) \end{aligned} \tag{A.6}$$

S_{gain}:

$$\begin{aligned} V_{SFB} &= V_{LDR} + S_{gain}(V_{DAC} - 1.25) \\ V_{SFB} - V_{LDR} &= S_{gain}(V_{DAC} - 1.25) \\ S_{gain} &= \frac{V_{SFB} - V_{LDR}}{(V_{DAC} - 1.25)} \end{aligned} \tag{A.7}$$

If we want a full swing $S_{gain} = \mathrm{V_{in}}$

L_{gain}:

The higher the gain of the LDR side, the faster the LDR side of the TEC output node traverses from high to low, minimizing the power dissipation. However, the maximum gain is determined by the minimum on and off times that can be achieved by the buck side due to duty cycle limits.

$$\begin{aligned} V_{LDR} &= \frac{V_{in}}{2} - L_{gain}(V_{DAC} - 1.25) \\ L_{gain} &= \frac{\frac{V_{in}}{2} - V_{LDR}}{(V_{DAC} - 1.25)} \end{aligned} \tag{A.8}$$

L_{gain} was selected to be 48 to ensure the full range of duty cycles is traversed for the V_{ref} range.

Therefore, the optimal L_{gain} and S_{gain} values were found to be 48 and 5. For the circuit simulations, 48KΩ and 5 KΩ resistors were used to ensure high noise immunity in the system.

Appendix B

Transfer Function Derivations

This section provides a detailed analysis and derivation of the main closed loop and open loop TEC driver architecture transfer functions for the system.

Open Loop Transfer Function Derivation

- **Output Filter, Gfilter(s)**

  Figure B-1 shows a simplified block diagram for the buck-stage which was used to derive the transfer function of the output filter of the buck-stage, shown in Equation B.1.

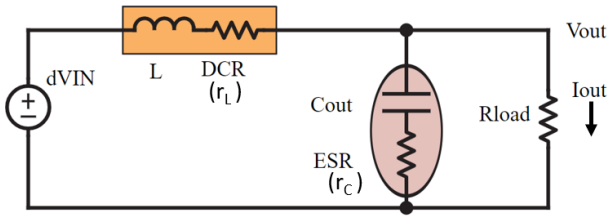

Figure B-1: Circuit diagram used in the derivation of the output filter transfer function.

Using the Voltage Divider Equation:

$$G_{filter}(s) = \frac{\hat{V}_{out}(s)}{\hat{V}_{in}(s)}\bigg|_{\hat{V}_i=d=\hat{i}_o=0} = \frac{(Z_C||R_{Load})}{Z_L+(Z_C||R_Load)} = \frac{Z_2(s)}{Z_{Total}(s)}$$

$$Z_c = \frac{1}{sC} + r_C \; ; \; Z_L = sL + r_L$$

$$
\begin{aligned}
Z_{Total} &= Z_L + (Z_C||R_{Load}) \\
&= \frac{R_{Load}(1+r_c sC)}{1+sC(R_{Load}+r_c)} + sL + r_L \\
&= \frac{R_{Load}(1+r_c sC) + [1+sC(R_{Load}+r_c)][sL+r_L]}{1+sC(R_{Load}+r_c)} \\
&= LC\frac{R_{Load}+r_c}{C(R_{Load}+R_c)} \frac{s^2 + s[\frac{C(r_L(R_{Load}+r_c)+r_{Load}r_c)+L}{LC(R_{Load}+r_c)}] + \frac{(R_{Load}+r_L)}{LC(R_{Load}+r_c)}}{\frac{1}{C(R_{Load}+r_c)}+s} \\
Z_{Total} &= L\frac{s^2+2\xi\omega_0 s+\omega_0^2}{(s+\omega_{z1})} \\
\omega_{z1} &= \frac{1}{C(r_c+R_{Load})} \\
2\xi\omega_0 &= \frac{C(R_{Load}r_L + r_c r_L + r_{Load}r_c) + L}{LC(R_{Load}+r_c)} \\
\omega_0^2 &= \frac{(R_{Load}+r_L)}{LC(R_{Load}+r_c)} \rightarrow \omega_0 = \sqrt{\frac{(R_{Load}+r_L)}{LC(R_{Load}+r_c)}} \\
\xi &= \frac{L + C[R_{Load}(r_c+r_L)+r_c r_L]}{2\sqrt{LC(R_{Load}+r_c)(R_{Load}r_L)}} \\
Z_2 &= (Z_C||R_{Load}) \\
&= \frac{R_{Load}(1+r_c sC)}{1+sC(R_{Load}+r_c)} \\
&= \frac{R_{Load}R_c}{(R_{Load}+R_c)} \frac{(s+\frac{1}{r_c C})}{(s+\frac{1}{C(R_{Load}+r_c)}} \\
Z_2 &= \frac{R_{Load}r_c}{R_{Load}+r_c} \frac{(s+\omega_z)}{(s+\omega_{z1})} \\
\omega_z &= \frac{1}{r_c C} \\
G_{filter} &= \frac{\frac{R_{Load}r_c}{R_{Load}+r_c}\frac{(s+\omega_z)}{(s+\omega_{z1})}}{L\frac{(s+\omega_z)}{s^2+2\xi\omega_0 s+\omega_0^2}} \\
&= \frac{R_{Load}r_c}{(R_{Load}+r_c)L} \frac{(s+\omega_z)}{s^2+2\xi\omega_0 s+\omega_0^2} \\
&= K_{filter}\frac{(s+\omega_z)}{s^2+2\xi\omega_0 s+\omega_0^2} where K_{filter} = \frac{R_{Load}r_C)}{L(R_{Load}+r_C)}
\end{aligned}
\tag{B.1}
$$

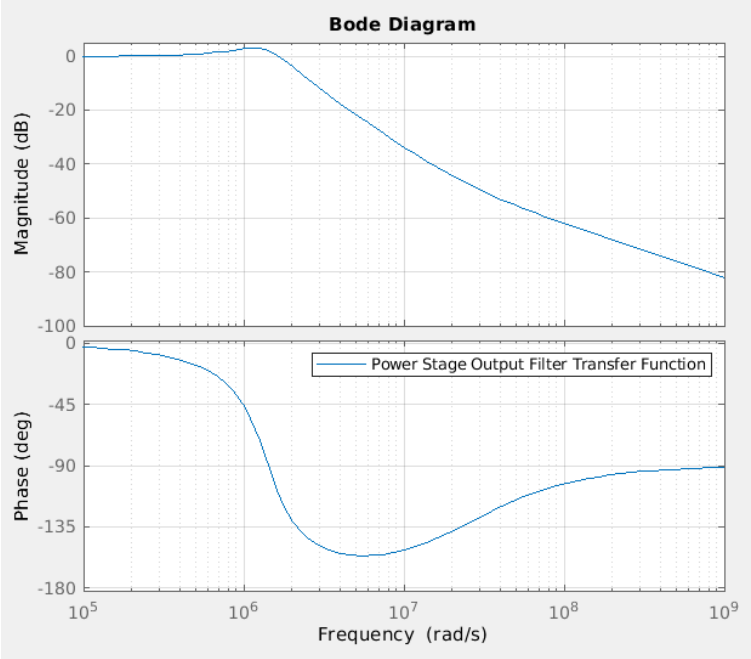

Figure B-2: Buck power stage output filter bode plot.

In the open loop system, the buck converter has a complex double pole due to the LC filter. The Q factor, or amount of peaking shown on the magnitude plot in Figure B-2 above, is affected by the capcitor esr and inductor's DC resistance (dcr). A high Q value is not desirable since it causes the system to have a very narrow bandwidth. As Q increases, the phase slope increases, i.e., the phase changes very quickly over narrow band of frequencies.

- **Duty Cycle-to-Inductor Current Transfer Function, Gid(s)**

  Figure B-3 below shows the circuit model that was used to derive the transfer function shown in Equation B.2. This transfer function shows the impact of the duty cycle variations on the output voltage.

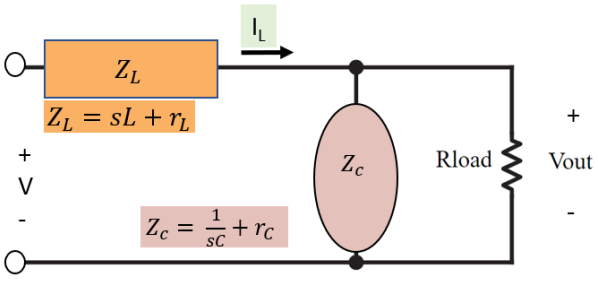

Figure B-3: Circuit diagram used in the derivation of the control-to-inductor current transfer function.

$$
\begin{aligned}
G_{id}(s) &= \frac{\hat{I}_L(s)}{\hat{d}(s)}\bigg|_{\hat{V}_i=\hat{i}_o=0} \\
i_L(s) &= \frac{d(s)V_{IN}}{Z_L + (Z_C||R_{Load})} = \frac{d(s)V_{IN}}{Z_{Total}} \\
&= \frac{d(s)V_{IN}}{L\frac{s^2+2\xi\omega_0 s+\omega_0^2}{(s+\omega_{z1})}} \\
\frac{i_L(s)}{d(s)} &= \frac{V_{IN}}{L}\frac{1}{\frac{s^2+2\xi\omega_0 s+\omega_0^2}{(s+\omega_{z1})}} \\
G_{id}(s) &= K_{id}\frac{(s+\omega_{z1})}{s^2+2\xi\omega_0 s+\omega_0^2} \text{ where } K_{id} = \frac{V_{IN}}{L}
\end{aligned}
\tag{B.2}
$$

- **3. Duty Cycle-to-Output Voltage Transfer Function, Gvd(s)**

  The control signal is the duty cycle and the output signal is the output voltage, V_{out}. Figure B-4 below shows the circuit model that was used to derive the transfer function, shown in Equation B.3.

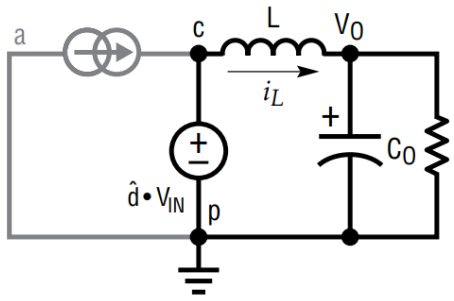

Figure B-4: Circuit diagram used in the derivation of the control-to-output transfer function.

$$
\begin{aligned}
\frac{V_{out(s)}}{d(s)} &= \frac{\hat{V}_{out}(s)}{\hat{d}(s)}\bigg|_{\hat{V}_i=\hat{i}_o=0} \\
V_{out}(s) &= V_{IN}d(s) = I_L(Z_C(s)||R_{Load}) \\
\frac{V_{out(s)}}{d(s)} &= G_{filter}V_{IN} \\
&= V_{IN}K_{filter}\frac{(s+\omega_z)}{s^2+2\xi\omega_0 s+\omega_0^2}
\end{aligned}
\tag{B.3}
$$

- **4. Input Voltage-to-Output Voltage Transfer Function, Gvv(d)**

  Figure B-5 below shows the circuit model that was used to derive the transfer function in Equation B.4.

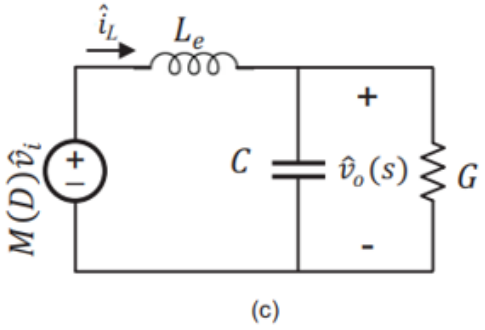

Figure B-5: Circuit diagram used in the derivation of the input voltage-to-output voltage transfer function.

$$G_{vv}(s) = \frac{\hat{V}_{out}(s)}{\hat{V}_{in}(s)}\bigg|_{\hat{V}_i=d=\hat{i}_o=0}$$
$$G_{vv}(s) = \frac{V_{Out}(s)}{V_{IN}(s)} K_{Filter} d \frac{(s+\omega_z)}{s^2 + 2\xi\omega_0 s + \omega_0^2} \tag{B.4}$$

- **5. Output Current-to-Output Voltage, i.e. Output Impedance Transfer Function, Zo(s)**

  The output impedance transfer function reflects the effect of output current ripple on the circuit performance. Figure B-6 below shows the circuit model that was used to derive the transfer function shown in Equation B.5.

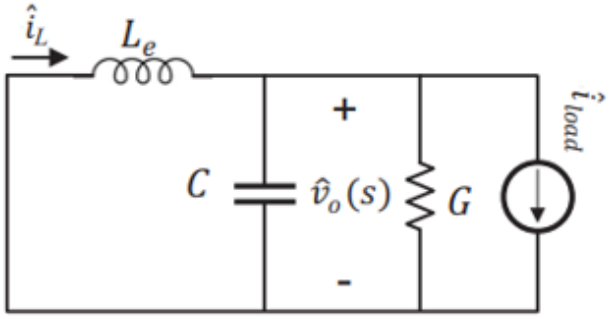

Figure B-6: Circuit diagram used in the derivation of the output current-to-output voltage transfer function.

$$
\begin{aligned}
Z_o(s) &= \frac{\hat{V}_{out}(s)}{-\hat{i}_{out}(s)}\Big|_{\hat{V}_i=d=0} \\
Z_o(s) &= -\frac{V_t}{i_t} \\
&= Z_L||(Z_C||RLoad) \\
&= \frac{R_{Load}(1+r_c sC}{1+sC(R_{Load}+r_c}||(sL+r) \\
&= \frac{1}{\frac{R_{Load}(1+R_c sC)}{1+sC(R_Load+r_c}+\frac{1}{sL+r}} \\
\frac{1}{\frac{R_{Load}(1+R_c sC)}{1+sC(R_Load+r_c}+\frac{1}{sL+r}} &= \frac{(sL+r)(1+sC(R_{Load}+r_c))}{R_{Load}(1+r_c sC)(sL+r)+1+sC(R_{Load}+r_c)} \\
&= \frac{R_{Load}r_c(s+\frac{1}{Cr_c}(s+(\frac{r}{L}}{(R_{Load}+r_c)[s^2]+(\frac{L+rC(R_{Load}r_c+R_{Load}Cr_c}{LC(R_{Load}+r_c)})s+\frac{R_{Load}+r}{LC(R_{Load}+r_c)}} \\
&= \frac{(s+\omega_z)}{(s^2+2\xi\omega_0 s+\omega_)^2}(s+\omega_{rl})K_{z0} \\
K_{zo} &= \frac{R_{Load}r_c}{R_{Load}+r_c} \\
\omega_z &= \frac{Cr_c}{} \\
\omega_{rl} &= -\frac{r}{L}
\end{aligned}
\tag{B.5}
$$

- **6. Input Current-to-Input Voltage Impedance Transfer Function, Zi(s)**

  Equation B.6 represents a ratio of perturbations in the input voltage when output current perturbations is zero.

$$
\begin{aligned}
i_L(s) &= \frac{dV_{IN}(s)}{Z_L+(Z_C||R_{Load})} \\
V_{IN}(s) &+ \frac{Z_L+(Z_C||R_{Load})}{di_L(s)} \\
&= \frac{Z_{Total}}{di_l(s)} \\
I_{in} &= \frac{1}{D}i_L \\
&= \frac{1}{D^2}(Di_L)
\end{aligned}
\tag{B.6}
$$

- **7. Inductor Current-to-Input Voltage ie Inductor Current-to-Line Voltage**
  This transfer function, as shown in EquationB.7, reflects the effect of input voltage ripple on the circuit performance.

$$\begin{aligned} G_{iv}(s) &= \frac{\hat{I}_L(s)}{\hat{V}_{in}(s)}\Big|_{\hat{i}_{oi}=d=0} \\ &= K_{iv}\frac{(s+\omega_{z1})}{s^2+2\xi\omega_0 s+\omega_0^2} \\ i_L(s) &= \frac{dV_{IN}(s)}{Z_L+(Z_C||R_{Load})} \\ V_{IN}(s) &+ \frac{Z_L+(Z_C||R_{Load})}{di_L(s)} \\ &= \frac{Z_{Total}}{di_l(s)} \\ I_{in} &= \frac{1}{D}i_L \\ &= \frac{1}{D^2}(Di_L) \end{aligned} \tag{B.7}$$

- **8. Inductor Current-to-Output Current Transfer Function Gii(s)**

  This transfer function, as shown in Equation B.8, reflects the effect of output current ripple on the circuit performance.

$$\begin{aligned} G_{ii}(s) &= \frac{\hat{I}_L(s)}{\hat{I}_O(s)}\Big|_{\hat{i}_{oi}=d=0} G_{filter}(s) \\ i_L(s) &= \frac{dV_{IN}(s)}{Z_L+(Z_C||R_{Load})} \\ V_{IN}(s) &+ \frac{Z_L+(Z_C||R_{Load})}{di_L(s)} \\ &= \frac{Z_{Total}}{di_l(s)} \\ I_{in} &= \frac{1}{D}i_L \\ &= \frac{1}{D^2}(Di_L) \end{aligned} \tag{B.8}$$

Closed Loop Transfer Function Derivation

The peak current mode controlled TEC driver architecture uses two feedback loops: an inner current and an outer voltage loop. The outer-voltage loop supplies the control voltage to the inner loop and the inner-current loop supplies the duty cycle to the power stage.

The control loop of the peak current mode buck converter includes the resistor divider network, the error amplifier with a compensation network, the current sampler and the duty cycle modulator.

F_g, F_v, F_m are gains due to the current modulation, and m_a is the slope of the external compensation ramp, as shown in Equation B.9.

$$\begin{aligned} F_g &= \frac{D^2}{f_{sw}2L} \\ f_g &= \frac{(1-2D)}{f_{sw}2L} \\ F_m &= \frac{f_{sw}}{m_a} \\ m_a &= -1.2 \\ R_{sense} &= Rds = 34m\Omega \\ H(s) &= \frac{1}{2.5+1} \end{aligned} \tag{B.9}$$

- **Open Loop Transfer Function**

  The inner current loop plus the power stage forms the plant for the outer voltage loop, as shown in Figure B-7 below. This transfer function is useful in determining what the phase of the system is and hence the phase boost that is required. It is therefore, vital in creating the compensator that will stabilize the system. Therefore, in order to design the compensator, the transfer function from $\hat{v}_c$ to $\hat{v}_o$ is needed. Assuming the current ripple is small, F_g, F_v are negligible and the block diagram can be reduced to Figure B-7.

  From the above block diagram, the transfer function were derived, as shown in Equations B.10 and B.11.

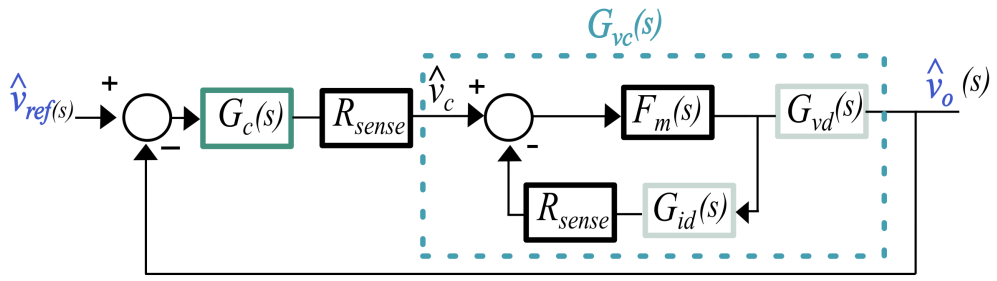

Figure B-7: Block diagram used in the derivation of the open loop transfer function.

$$
\begin{aligned}
G_{vc}(s) &= \left.\frac{\hat{V}_{out}(s)}{\hat{v}_c(s)}\right|_{\hat{V}_i=\hat{i}_o=0} \\
&= \frac{F_m}{1+F_m G_{id}(s) R_{sense}} G_{vd}(s)
\end{aligned}
\tag{B.10}
$$

The Open Loop Transfer Function: $T(s) = G_{vc}(s) \cdot G_c(s) \cdot R_{sense}$ where:

$$
G_c(s) = \beta g m R_0 \frac{(1+\frac{s}{z_o})}{(1+\frac{s}{p_o})(1+\frac{s}{p_1})} \tag{B.11}
$$

Low DC gain at low frequencies can cause steady-state errors. Therefore, we want high DC gain to minimize steady state errors.

The closed loop transfer functions described by Equations B.11 to B.15 were used to determine the stability of the system in the face of disturbances.

- **Closed Loop Transfer Function from V_{ref} to V_{out}**

  This transfer function is useful in describing how the system behaves in the face of any variations in the reference voltage.

$$
V_{ref,closed} = \frac{G_{vc}(s) * G_c(s) * R_{sense}}{1+T(s)} \tag{B.12}
$$

- **Closed Loop Output Impedance Transfer Function**

  Figure B-8 shows the block diagram of the TEC driver closed loop system that was used to derive the transfer function from the output voltage to the output current, shown in Equation B.13. This transfer function is useful in describing how the system

behaves in the face of any variations in the load current.

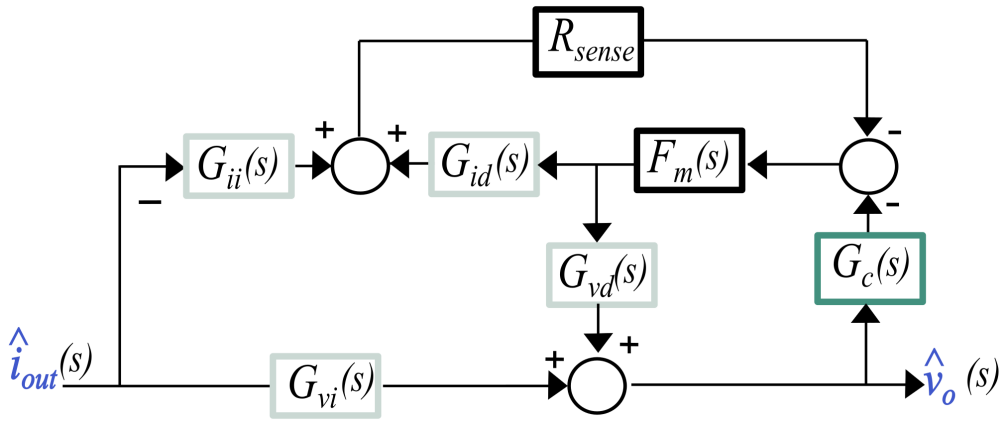

Figure B-8: Block diagram used in the derivation of the output impedance for the closed loop system.

$$
\begin{aligned}
Z_{o,open}(s) &= \frac{\hat{v}_{out}(s)}{\hat{i}_{out}(s)}\bigg|_{\hat{V}_i=\hat{v}_{ref}=0} \\
&= \frac{G_{vi}(s) + R_{sense}F_m G_{id}(s)(G_{vi}(s) - \frac{G_{ii}(s)G_{vd}(s)}{G_{id}(s)})}{(1 + R_{sense}F_m G_{id}(s))} \\
Z_{o,close}(s) &= \frac{Z_{o,open}(s))}{(1 + T(s)}
\end{aligned}
\tag{B.13}
$$

- **Closed Loop Line to Output Transfer Function**

$$
\begin{aligned}
V_{in,cl}(s) &= \frac{\hat{v}_{out}(s)}{\hat{V}_{in}(s)}\bigg|_{\hat{i}_{out}=0} \\
&= \frac{G_{vv} + G_{iv}H_e R_{sense}F_m G_{vv} + F_g * G_{vd}F_m - G_{iv}R_{sense}H_e * G_{id}F_m * G_{vd}}{(1 + G_{id}R_{sense}H_e F_m - F_v G_{vd}F_m + G_c R_m G_{vd})}
\end{aligned}
\tag{B.14}
$$

- **Closed Loop Input Impedance**

$$
\begin{aligned}
Z_{i,open}(s) &= \frac{\hat{v}_{in}(s)}{\hat{i}_{in}(s)}\bigg|_{\hat{i}_{out}=0} \\
&= \frac{G_{vi}(s) + R_{sense}F_m G_{id}(s)(G_{vi}(s) - \frac{G_{ii}(s)G_{vd}(s)}{G_{id}(s)})}{(1 + R_{sense}F_m G_{id}(s))}
\end{aligned}
\tag{B.15}
$$

Abbreviations and Symbols

a active terminal

AC alternating current

ADI Analog Devices

α seebeck coefficient

BCD bipolar CMOS-DMOS

BST boosted voltage

β_{vdiv} voltage divider ratio

β_p, β_n device property

c common terminal

C_{Comp} compensator capacitance

CCM continuous conduction mode

C_{gm} compensator capacitance

C_{js}, C_{jd} junction capacitance

C_{TH} thermal capacitance

CMC current mode control

CMOS complementary metal oxide semiconductor

C_{os}, C_{od} overlap capacitance

C_{ox} MOSFET oxide capacitance

C_{Out} output capacitance

D duty cycle

DAC digital to analog converter

DC direct current

dcr DC resistance

Δ standard deviation

$\delta\beta$ beta mismatch

ΔI current ripple

ΔI_D drain current mismatch

ΔI_L inductor current ripple

ΔI_{pp} peak to peak current ripple

ΔV voltage ripple

δV_{gs} gate-source voltage mismatch

δV_t threshold voltage mismatch

EMI electromagnetic interference

esr effective series resistance

f fingers

f_c crossover frequency

f_{p0} low frequency pole

f_{p1} high frequency pole

f_{sw} switching frequency

f_z low frequency zero

gm transconductance

I current

IC integrated circuit

I_D drain current

I_L inductor current

I_{out} output current

I_{rms} root mean square current

I_{sense} sensed current signal

J current density

K coupling factor

L inductor

L_n NMOS channel length

LC inductor and capacitor

LDR high gain linear regulator

LTI linear time invariant

m multiplier

MOSFET metal oxide semiconductor field effect transistor

η efficiency

NMOS n-channel metal oxide semiconductor

op-amp operational amplifier

OTA operational transconductance amplifier

p passive terminal

P power

P_c peltier coefficient

P_{cap} power loss due to capacitor

P_{cond} power loss due to conduction

P_{FET} power loss due to MOSFET

P_{GateQ} power loss due to gate charge

P_{ind} power loss due to inductor

P_{LS} power loss due to the low-side MOSFET's body diode

P_{Out} output power

P_{sw} power loss due to MOSFET switching

pb phase boost

PCMC peak current mode control

PMOS p-channel metal oxide semiconductor

pm phase margin

PWM pulse width modulation

q charge

Q_J joule heating

Q_{Cold} peltier cooling

Q_{Hot} peltier heating

Q_P peltier heat

Q_{PC} peltier cooling current source

Q_{PH} peltier heating current source

RC resistor and capacitor

R_{Comp} compensator resistance

R_{dcr} inductor DC resistance

$R_{ds,on}$ MOSFET drain-source on resistance

rms root mean square

R_o error amplifier internal output resistance

R_{fb1}, R_{fb2} feedback resistors

R_{TH} thermal resistance

R_{TEC} TEC resistance

S_{gain}, L_{gain} linear regulator and buck stage gains

SFB buck output

SR set-reset

σ variance

T temperature

t time

T_{dead} non-overlap/dead time

T_f fall time

T_{on} on-time

T_r rise time

TEC thermoelectric cooler

μ_c channel mobility

μ_n NMOS mobility

μ_p PMOS mobility

V voltage

V_{cm} input common mode voltage

$V_{control}$ control voltage

V_{ref} DAC reference voltage

V_{ds} drain-source voltage

V_{gs} gate-source voltage

V_{in} input voltage

V_{out} output voltage

V_{ramp} slope compensation ramp signal

V_{sense} sensed voltage signal

V_{sw} switch node potential

V_t threshold voltage

V_{TEC} voltage difference across the TEC

VCMC valley current mode control

VMC voltage mode control

W_n NMOS channel width

W_p PMOS channel Width

WLCSP wafer-level chip scale packaging

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