Design of a Bandgap-Less Temperature Sensor for Achieving High Untrimmed Accuracy

by

Vipasha Mittal

B. Tech, Indian Institute of Technology, Delhi (2018)

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Author

Department of Electrical Engineering and Computer Science

May 20, 2021

Certified by

Anantha P. Chandrakasan

Vannevar Bush Professor of Electrical Engineering and Computer Science

Thesis Supervisor

Certified by

Hae Seung Lee

ATSP Professor of Electrical Engineering

Thesis Supervisor

Accepted by

Leslie A. Kolodziejski

Professor of Electrical Engineering and Computer Science

Chair, Department Committee on Graduate Students
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Abstract

Temperature sensors are extensively used in measurement, instrumentation and control systems. CMOS based temperature sensors offer benefits of low cost and direct digital outputs over conventional sensors. However, they are limited in their absolute accuracy due to the non-ideal behaviour of the devices used to design them. Therefore, these sensors require either calibration or gain, offset and linearity adjustments to achieve desired accuracies. The latter process, also called trimming needs additional expensive test equipment, valuable production time and is a major contributor to the cost of the sensors. In order to enable high volume production of CMOS based temperature sensors at low cost, it is imperative to achieve high accuracies without trimming.

This work describes the design of an untrimmed, bandgap-less CMOS temperature sensor based on fundamental physical quantities resilient to process variations, package stress and manufacturing tolerances. Compared to previous art, this sensor employs high-thermal noise switched capacitor amplifiers, which are digitized by a bandgap-less successive approximation analog-to-digital converter. The flicker noise is attenuated through autozeroing, which also allows amplifying the thermal noise further. This work demonstrates the design of the first untrimmed closed-loop thermal noise temperature sensor. The chip is fabricated in TSMC 65 nm low-power process and simulation results show that the sensor achieves an untrimmed 3σ inaccuracy of less than 1°C.

Thesis Supervisor: Anantha P. Chandrakasan
Title: Vannevar Bush Professor of Electrical Engineering and Computer Science

Thesis Supervisor: Hae Seung Lee
Title: ATSP Professor of Electrical Engineering
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Chapter 1

Introduction

With the tremendous growth in the internet of things, smart systems and automation, integrated temperature sensors have become ubiquitous. They are used in automobiles and mobile phones for reliability monitoring, in thermostats at homes and for temperature compensation of frequency references [22]. With the increasing density of transistors, temperature sensors have also become crucial in microprocessors to monitor activity dependent hot-spots on chip [4]. Moreover, integrating temperature sensors with RFID tags opens up a plethora of opportunities- including environmental monitoring and monitoring in implantable devices [33]. Temperature sensors are generally a part of a bigger system which acts on the information that they provide. Therefore, for robustness and reliability, the sensors have to be closely integrated with the rest of the system. To enable robust system integration, smart temperature sensors are designed in complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) technology. Designing in CMOS technology also gives the benefit of high volume production at low cost [22].

1.1 Smart Temperature Sensors

A sensor that integrates the sensing element, analog-to-digital converter and other interface electronics on the same chip is referred to as a smart sensor [22]. The output of the sensing element is a weak analog signal which is converted to a digital form
using an analog-to-digital converter. Any further processing is then done in the digital domain. This makes the sensor robust, and since the output is in a standardized digital format, it is easily integrated with the rest of the system. A general block diagram of a smart temperature sensor is shown in Figure 1.

Figure 1-1: Architecture of a Smart Temperature Sensor [22]

Accuracy is of primal importance in applications that require sensors. A major disadvantage of using CMOS based sensors is their poor absolute accuracy, because of manufacturing tolerances, process variations, packaging stress and higher order temperature dependencies. In order to alleviate the impact of these factors, sensors typically have to be calibrated at one or more than one temperatures. In addition to calibration, gain, offset as well as linearity corrections are critical to achieve the desired accuracies in a wide range of temperatures. This process, called trimming, has to be done at one or more than one temperature points, and is the dominant contributor to the overall cost of the sensor.

In the existing literature, there are primarily four types of CMOS temperature sensors (depending on the sensing element used) - BJT based, resistor based, MOS based and thermal diffusivity based [19,34]. Except for thermal diffusivity based sensors, since the other sensors rely on temperature dependence of \( V_{BE} \) of a BJT, resistor values, or threshold voltages of MOSFETs, trimming is inevitable due to higher order temperature dependencies and process spread of these parameters. Sensors based on thermal diffusivity aim to solve the problem of trimming by exploiting the thermal diffusivity of silicon which is very well-defined. However, it is susceptible to self-heating due to the use of heaters in the design and its relatively large power consumption compared with other sensors.
From the recent survey of smart temperature sensors [19], it is clearly seen that the absolute inaccuracy increases as the trim points reduce. While the state of the art temperature sensors achieve $3\sigma$ inaccuracies as low as 0.1°C, they require at-least 1 trim point to do so. With 0 trimming points, the inaccuracies are still in the range of 1.6-3°C [19]. In this work, we aim to design CMOS smart temperature sensors that achieve fundamental linearity and offers possibility of no individual trimming point to achieve a $3\sigma$ inaccuracy of 1°C.

1.2 Previous Literature

The different temperature sensors differ in the type of sensing element used to generate the temperature dependent analog signal. An overview of existing temperature sensors is presented here.

1.2.1 BJT based

BJT based temperature sensors use the temperature dependent properties of a BJT to generate the temperature output. A block diagram is shown in Figure 1-4. The core philosophy of a BJT sensor consists of two vertical PNPs biased at different collector currents. The base emitter voltage of a BJT, $V_{BE}$ is equal to $\frac{kT}{q} \ln(I_c/I_s)$, where $I_c$ refers to the collector current and $I_s$ is the saturation current. The saturation current $I_s$ has a strong positive temperature dependence, and thus $V_{BE}$ has a negative temperature dependence.

The difference in two base-emitter voltages $\Delta V_{BE}$ is process independent, and equal to $\frac{kT}{q} \ln(p)$, where p is the ratio of collector currents. BJT based sensors achieve good inaccuracies after atleast one-point trims, and have a small form factor and time of conversion. They are widely used in thermal monitoring applications.
1.2.2 Resistor Based

Resistor based sensors use the temperature dependent properties of resistors to generate a temperature dependent signal by incorporating resistors in wien bridge or wheatstone bridge configurations. [3] These sensors achieve the best resolution and energy efficiency compared to other sensors, however at the cost of multiple-point trimming. An example of a wien bridge resistor sensor is shown in Figure 1-3.

1.2.3 Thermal Diffusivity Based

Thermal diffusivity sensors rely on measuring the thermal diffusivity of bulk silicon, which has a strong dependence on the absolute temperature, of the form $1/T^{0.8}$ [36]. The thermal diffusivity in such sensors can be measured by determining the amount of time it takes a small amount of heat to diffuse from a heater to a neighbouring temperature sensor, usually a thermopile. These sensors are increasingly being researched to develop untrimmed temperature sensors with high accuracy due to the fundamentally determined temperature dependence of thermal diffusivity of silicon.
1.2.4 MOSFET Based

When operated in the sub-threshold region, the drain current and the gate-to-source voltage of a MOSFET exhibit an exponential relationship.

\[ V_{GS} - V_{TH} = \left(\frac{n kT}{q}\right) \ln\left(\frac{I_D}{I_o}\right), \]

where, \( I_o \) is a process dependent parameter, and \( n \)
is the sub-threshold slope. Thus, they can be used in a similar way to BJT based sensors for low form-factor, and nanowatt power applications, that do not require high accuracies. Time-to-digital converters have also been proposed where the time taken by the sub-threshold current to charge a capacitor to a fixed threshold voltage is measured. These generally require an external timing reference.

1.2.5 Johnson Noise Based

Johnson Noise based temperature sensors use the temperature dependence of the thermal noise of an RC filter to generate a temperature dependent signal. These class of sensors are extensively explored in physics, however are in a nascent stage in integrated circuits. They offer possibilities of high untrimmed accuracy and absolute temperature measurement while using low resolution ADCs, with further research in the future. A few integrated circuit solutions have been proposed in [37] and [38].

\[ P_{\text{in},V} = \frac{KT}{C_{\text{in}}} \]
\[ P_{\text{s},V} = A^2 V_{n,\text{in}}^2 f_{\text{off}} + \Delta P \]

![Johnson Noise Based Sensor](image)

Figure 1-5: Johnson Noise Based Sensor [37]

1.3 Figures of Merit

Temperature Sensors are evaluated on a number of metrics, depending on their use case scenario. The various figures of merit are described below.

1.3.1 Worst case Inaccuracy

An important metric of evaluation is the worst-case inaccuracy (IA) over a specified temperature range. The values given are either max - min or 2x 3\( \sigma \) values. Since
inaccuracy is a statistical measure, measurements on a large number of samples (>10) are required to obtain realistic numbers. Inaccuracy is mainly a function of sensor type, readout architecture, process and the number of trimming points. [19]

The figure of merit corresponding to the inaccuracy is referred to as the Relative Inaccuracy. This corresponds to the slope of an imaginary box placed around the sensor’s error and is defined as $100 \times \frac{IA}{\text{Specified temperature range}}$. The inaccuracy for previous literature with respect to trim is shown in Figure 1-6.

Figure 1-6: Inaccuracy vs Trim Points [19]

1.3.2 Resolution

Resolution is a measure of the noise present in the sensor’s output. It is usually specified as an rms value in °C obtained after a particular conversion time. It should be noted that the resolution of most temperature sensors is limited by thermal and 1/f noise, rather than by quantization noise! As a result, sensor resolution can best be determined experimentally. [20]

The figure of merit corresponding to resolution is referred to as the Resolution FOM
which is defined as \( \frac{\text{Energy/Conversion}}{\text{Resolution}^2} \). The comparison of previous literature in terms of this figure of merit is shown in Figure 1-7.

1.3.3 Power Consumption and Time

Power consumption refers to the average power dissipated during the specified conversion time. Conversion time is reported by the time needed to achieve the reported resolution. The required time of conversion depends on the application, where latency critical applications such as thermal monitoring of processors require fast times of conversion, whereas industrial monitoring can tolerate upto seconds of time of conversion. The time constant of temperature changes is typically in the order of seconds, so in most applications, times upto a few seconds are tolerable.

Figure 1-7: Energy/Conversion vs Resolution [19]
1.4 Thesis Organization

In this chapter the basics of smart temperature sensors and previous literature was discussed. The rest of the thesis is organised in the following manner. Chapter 2 discusses the theory and system level architecture of the design proposed. In chapter 3, the details of the circuit level implementation and the layout are elaborated in detail. The simulation results are then presented in chapter 4. Finally, the thesis contributions are elucidated in chapter 5 along with a discussion on the future work.
Chapter 2

Theory and System Architecture

In this chapter, the concepts behind designing a fundamental zero-trim sensor are detailed. After discussing the theory required, we will then develop the system level description of the proposed idea.

2.1 Concepts of Fundamental Sensing

The output of a temperature sensor element is a weak analog signal, which is then amplified using analog signal conditioning blocks to generate the signal $V_{sig}$. An analog-to-digital converter (ADC) converts the given analog signal to its corresponding digital representation in order to transmit it in a standardised yet robust manner. It does so by comparing the signal against a known well-defined voltage reference $V_{ref}$.

For an N-bit ADC, the output digital bits are related to the original signal by the following equation [28]:

$$\frac{V_{sig}}{V_{ref}} = \frac{1}{2^N} (b_{N-1}2^{N-1} + b_{N-2}2^{N-2} + ... + b_0) \quad (2.1)$$

Hence the bits $b_0...b_{N-1}$ give a representation of $\frac{V_{sig}}{V_{ref}}$. The equation presents a key roadblock towards achieving high untrimmed accuracy. While the voltage signal $V_{sig}$
can be made very robust to process spread (for e.g., by using a PTAT $ΔV_{BE}$ of a BJT which just depends on the current ratios and boltzmann constant which are known accurately), the $V_{ref}$ needs to be perfectly temperature-independent in order to give a digital reading directly proportional to temperature.

In most designs, this voltage reference is designed using a bandgap reference, which uses an appropriate combination of a positive temperature coefficient voltage (generally, $ΔV_{BE}$ of a BJT) and a negative temperature coefficient voltage (generally, $V_{BE}$ of a BJT). The two voltages are combined in an appropriate ratio to generate the reference bandgap voltage $V_{REF} = V_{BE} + αΔV_{BE}$, where $α$ is chosen so that the positive temperature dependence of $ΔV_{BE}$ is balanced by the negative temperature dependence of $V_{BE}$. This is shown in Figure 2-1.

![Figure 2-1: Generation of a Bandgap Voltage](image)

In practice, the bandgap reference does not maintain a constant voltage with temperature. While the PTAT voltage $ΔV_{BE}$ demonstrates linear dependence on temperature, the $V_{BE}$ of the BJT deviates from the linear dependence on temperature. Moreover, it also varies across process corners [27]. The variation of $V_{BE}$ with temperature and process is shown in Figure 2-2, and is discussed in detail in Section 2.3.
In Figure 2-2, the effect of process and temperature changes on $V_{BE}$ is shown separately - the impact due to process and temperature is added to give a curvature across temperature as well as across process corners. As a result of this variation, the linear combination of $\Delta V_{BE}$ and $V_{BE}$ is not independent of temperature. This results in a curvature in the Voltage vs Temperature characteristic of the bandgap voltage, as shown in Figure 2-3.
To design a sensor free from individual trimming, the goal is to use signals that are either dependent on relative ratios or have precise dependencies on temperature. The concept of a individual trimming-free sensor is based on the use of two key ideas. By eliminating the bandgap reference from the entire signal chain (similar ideas used in [18]) and replacing that with a PTAT voltage instead, the reference becomes accurately known.

Since the reference voltage itself is directly proportional to temperature, in order to preserve temperature dependence of $\frac{V_{\text{sig}}}{V_{\text{ref}}}$, it is imperative that the temperature dependent analog signal $V_{\text{sig}}$ does not have a linear proportionality with temperature. In order to achieve this, we use the root-mean-squared (RMS) value of thermal noise for $V_{\text{sig}}$. The RMS value of thermal noise is a precisely determined function of the form $\sqrt{\frac{kT}{C}}$, where $C$ is the capacitance.

The temperature dependence of thermal noise is fundamentally governed by the thermal behaviour of motion of electrons, which makes the temperature dependence resilient to any variations. In modern CMOS processes, the capacitances fabricated are quite precise and do not exhibit a change in their value over temperature. Moreover, any spread in capacitance over process is reduced due to the $\sqrt{1/C}$ dependence in the thermal noise RMS voltage. Any gain error due to capacitance variation can be removed through batch calibration, and thus we do not require individual trimming. Since both the voltages $V_{\text{sig}}$ and $V_{\text{ref}}$ are precisely determined, we do not require any individual trimming to achieve the required temperature dependence. In the following sections, thermal noise and PTAT voltages are now described in detail.

2.2 Noise

Noise refers to the minute fluctuations observed irrespective of the presence or absence of external signals applied. Noise is a random process. This means that at any given instance of time, the instantaneous value of noise cannot be predicted, even if all the prior values are known. [29] Analog signals in integrated circuits are impacted
by two kinds of noise: Device noise and Environmental noise. Environmental noise refers to the random disturbances that the circuit experiences due to either the substrate, ground or supply lines. The impact of environmental noise is obfuscated by appropriate circuit design and bypass techniques. Here, we will be focusing on the study of device noise.

2.2.1 Thermal Noise of a Resistor

Consider a resistor with resistance $R$, such that both its terminals are open. One can imagine that the current flowing through this resistor would be zero. While it is true that the average current is zero, the random motion of electrons in this resistor produce random fluctuations in voltage. Intuitively, we can see that the variance of this voltage would increase with temperature and would also depend on the value of the resistance. These statistical fluctuations were experimentally shown in [14] and theoretically explained in [25] by Johnson and Nyquist respectively.

The one sided Power Spectral Density $S_v(f)$ for a resistor of resistance $R$ at a frequency $f$ and temperature $T$ is equal to $4kTR$. (where $k=1.38 \times 10^{-23}J/K$ is the Boltzmann’s constant). Since the power spectral density does not have a frequency dependence, this implies that the spectrum is white. (In reality, it is white roughly upto 100THz, but for practical purposes we can consider it to be white).

Effectively, the resistor is the source of the noise. To model this effect from a circuit designer’s perspective, we can replace the true, physical resistor with an artificial circuit. This circuit consists of an ‘artificial generator’ that is going to represent the noise, and now the resistor is otherwise ideal - no noise comes from it. [9] The circuit representation is shown in Figure 2-4 [29] Here, $V_n^2$ represents the frequency averaged value of the noise power.
2.2.2 Thermal Noise of an RC Circuit

Ideal lossless capacitors do not have a noise generator source. Let us consider this capacitor is connected to a noiseless voltage source or a short circuit to a resistor which has a resistance of $R$ (as shown in Figure 2-5). Clearly, we have a noise generator from the resistance. Let the output power across the capacitor due to this noise generator be $V_{n,\text{cap}}^2$. In this circuit, the power spectral density of the generator is $4kTR$ and the bandwidth is $1/(2\pi RC)$. The integrated output noise power $V_{n,\text{cap}}^2$ is equal to $\frac{kT}{C}$. This is independent of the value of the resistance. In case an ideal switch is connected to this capacitor, we can assume that when the switch is OFF, the RMS noise voltage stored on the capacitor gets frozen off from its previous value.
Thermal Noise of a Switched Capacitor

We can now understand the thermal noise of a switched capacitor. Consider a capacitor that is switched to the open and closed configuration through a switch as shown in Figure 2-6. When the switch is ON, the thermal noise power is equal to $kT/C_s$ as derived earlier. This corresponds to a noise charge $q^2 = kTC_s$ on the capacitor. When the switch is now open, this noise charge stays stored on the capacitor, as the capacitor is now in an open circuit. [24]

2.2.3 Noise of a MOSFET

The current through a MOSFET is governed by the motion of charge carriers. Random perturbations in the motion of the charge carriers leads to noise generation in a MOSFET. Depending upon the mechanism of generation, the major sources of noise in a MOSFET can be divided into thermal, flicker and shot noise. They also differ in terms of their frequency spectrum and their specific characteristic properties are further delineated below.

Thermal Noise

A MOSFET operating in strong inversion is accompanied by the formation of a channel between the drain and the source. The random thermal motion of the charge carriers in the channel results in thermal noise, similar to that in a resistor.
Flicker Noise

At low frequencies, the dominant source of noise in a MOSFET is the flicker noise. This noise is also called "1/f noise" because of the inverse proportionality of the power spectral density with frequency. The trapping and releasing of carriers by the traps located near the Si-SiO$_2$ interface results in the fluctuations in the surface potential. This results in random fluctuation in the number of carriers in the channel. The flicker noise theory considers the particle nature of the charge carriers, and thus at lower frequencies, the effect of the number of charge carriers is more visible.

Shot Noise

In the weak inversion region of operation, the current is primarily due to diffusion. However, it is highly probabilistic for an electron shooting out of the source to have enough energy to climb the energy barrier between the source and the channel. It is still possible for that electron to reach the channel through a number of randomizing collisions. Eventually, the electron would actually diffuse their way into the drain and contribute an impulse of charge. [30] Shot noise can thus be considered as the corollary to thermal noise in the weak inversion region. This process can be modelled as a Poisson process. The current noise density of shot noise can be modelled as $i_n^2 = 2qI_D$ where $I_D$ is the DC current through the MOSFET at the operating point.

2.2.4 Noise of an Amplifier

As we saw earlier, a number of sources in MOSFETs create noise. Since amplifiers consist of different MOSFETs, each of the MOSFETs contribute noise depending on their configuration in the circuit. In order to consider the equivalent impact of all of these transistors on the amplifier, each of the noise sources are referred to the input transistor of the amplifier.
Input Referred Noise

To calculate the total input referred noise from an amplifier, each of the noise source is considered to be an independent uncorrelated noise source. The total noise contribution is a sum of contributions from the flicker noise and thermal/shot noise in the strong/weak inversion region. [29] The equivalent input noise power is given by $v_{eq}^2$ where,

\[
v_{eq}^2 = \frac{8kT}{3g_m} \Delta f + \frac{K_f}{WLC_{ox}^2 f} \Delta f \quad (2.2)
\]
in the strong inversion region, and

\[
v_{eq}^2 = \frac{2nkT}{g_m} \Delta f + \frac{K_f}{WLC_{ox}^2 f} \Delta f \quad (2.3)
\]
in the weak inversion region, where $n$ is the sub-threshold slope.

To calculate the total input referred noise of an amplifier consisting of multiple transistors, each of these independent noise sources are individually considered. The overall noise power is the sum of the noise power from each of these sources. An equivalent circuit representation is considered where the entire noise contribution is from an equivalent noise voltage source at the input transistor. [17]

Consider a folded cascode opamp as shown in Figure 2-7. Since M6, M7, M8 and M9 are configured in a common gate configuration, their noise contributions are negligible. Let the contribution from M1 and M2 be equal to $v_{eq1}^2$ (both are equal since M1 and M2 are matched and biased similarly), from M4 and M5 be $v_{eq2}^2$ and from M10 and M11 be $v_{eq3}^2$. Through the process described earlier, we can now find the equivalent input noise power $v_{IT}^2$, where,

\[
v_{IT}^2 = 2(v_{eq1}^2 + \frac{g_{m4}}{g_{m1}} v_{eq2}^2 + \frac{g_{m10}}{g_{m1}} v_{eq3}^2) \quad (2.4)
\]

Here, $g_{m1}, g_{m4}, g_{m10}$ are the input transconductances of M1, M4 and M10 respectively.
Figure 2-7: Equivalent Input Referred Noise of a Folded Cascode Amplifier

Using formulae of $v_{eq}$ shown earlier, the input referred noise can be calculated. Let us consider the impact of thermal and shot noise alone. We can substitute $v_{eq2}$ and $v_{eq3}$ in terms of $v_{eq1}$ and find that

$$v_{IT}^2 = 2v_{eq1}^2 (1 + \frac{g_{m4}}{g_{m1}} + \frac{g_{m10}}{g_{m1}}) \quad (2.5)$$

Now, substituting $v_{eq1}^2$, we get $v_{IT}^2 = \frac{16kT}{3g_{m1}} (1 + \frac{g_{m4}}{g_{m1}} + \frac{g_{m10}}{g_{m1}})$ in the strong inversion region, and $v_{IT}^2 = \frac{4nkT}{g_{m1}} (1 + \frac{g_{m4}}{g_{m1}} + \frac{g_{m10}}{g_{m1}})$ in the weak inversion region.

The above equations can be simplified to be of the form $S_i(f) = \frac{MBkT}{g_{m1}}$, where $m$ reflects the noise contribution from other devices, $B$ is a constant that depends on the region of operation of the transistors, and $g_{m1}$ is the transconductance of the input transistor.

Output Referred Thermal/Shot Noise

If the unity gain frequency of the opamp is $f_u$ and the feedback ratio is $\beta$, then the closed loop -3 dB bandwidth is $\beta f_u$, and the output noise power spectral density is given by $S_o(f) = \frac{S_i(f)}{\beta^2}$.  

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We can employ a similar approach as in the case of an RC circuit to determine the total output referred noise of a closed loop amplifier. The total input referred noise of the amplifier is given by

\[ S_i(f) = \frac{mBkT}{g_{m1}} \]

From this, the total output referred noise of the amplifier can be determined by considering the bandwidth of the amplifier.

The mean square output noise is equal to

\[ v_{on}^2 = \frac{mBkT}{4B C_c} \]

where \( C_c \) is the dominant pole determining capacitance in the opamp, i.e. the compensation capacitance in case of a two stage opamp and the load capacitance in case of a single stage opamp.

Hence, the output referred shot noise power of an amplifier can be made proportional to temperature, by ensuring that the factor \( m \) is independent of temperature. Since \( m \) depends on the ratio of \( g_m \), the temperature dependence can be removed by biasing the transistors in weak inversion region. Further, the shot noise can be increased by decreasing the compensation capacitance.

### 2.3 PTAT Voltage

While thermal and shot noise is used as the temperature sensing voltage for the fundamental sensor, the reference voltage is based on PTAT (Proportional to Absolute Temperature) voltage. The temperature dependence of a BJT based PTAT voltage
is discussed in this section, to elucidate its resilience to variations.

As elaborated in BJT based temperature sensors in chapter 1, the difference in $V_{BE}$ between two BJTs with the same dimensions, and currents biased with a ratio of $p$, is directly proportional to temperature as shown in Figure 2-9.

$$\Delta V_{BE} = \frac{kT}{q} \ln(p)$$

In such a configuration, we have $\Delta V_{BE} = \frac{kT}{q} \ln(p)$. Alternately, we can also allow the same currents to go through both the BJTs, while maintaining a size ratio of $p$ to generate the temperature dependent voltage. Due to this ratio property used in the generation of a PTAT voltage from the $\Delta V_{BE}$ of BJTs, the resulting voltage is a highly accurate measure of temperature [21]. PTAT voltages generated in such a manner have a well defined temperature dependence, are tolerant to the package stress, process spread and any change across temperature. Hence PTAT voltage is an appropriate voltage reference that can be used as a reference in the ADC.

### 2.4 Global Architecture

In the previous section, we established the theory behind fundamental sensing. In this section we will go over the architecture and some requirements of the blocks used to implement these concepts. The circuit level details of these blocks will be elucidated in the next chapter. A block diagram of the overall architecture is shown in Figure 2-10.
2.4.1 Switched Capacitor Amplifiers

The thermal and shot noise generation and amplification is performed using switched capacitor amplifiers. In this subsection, the theory behind switched capacitor amplifiers is detailed, to understand their use in the global architecture.

Switched capacitor filters are an ideal consideration for implementing the thermal noise generators and amplifiers in this sensor. This is because they can be implemented using entirely capacitors and their amplification factor is determined by the ratios of capacitors. These are quite precise and the matching can be greatly improved by good layout techniques, and autozeroing can be easily implemented in these circuits for offset and flicker noise cancellation.

![Resettable Gain Switched Capacitor Circuit](figure)
Consider a Resettable Gain circuit as shown in Figure 2-12. In each phase $\phi_1$, the input voltage is sampled and amplified and in each phase $\phi_2$, the voltage across the integrating capacitor $C_2$ is cleared, and the offset voltage is stored. (This would be implemented differently had we wanted to design an integrator instead). To see the offset cancellation, we incorporate the effect of the input offset voltage by a voltage source $V_{\text{off}}$.

During the phase $\phi_2$, both the voltages across C1 and C2 are equal to the offset voltage $V_{\text{off}}$.

In phase $\phi_1$, the voltage across the capacitor $C_1$ is thus, $V_{C1}(n) = v_{\text{in}}(n) - V_{\text{off}}$, while for $C_2$ is given by $V_{C2}(n) = v_{\text{out}}(n) - V_{\text{off}}$.

The change in charge across $C_1$ is equal to $\Delta Q_{C1} = C_1(V_{C1}(n) - (-V_{\text{off}})) = C_1v_{\text{in}}(n)$

By conservation of charge, the change in charge across $C_1$ is equal to the change in charge across $C_2$.

Thus, $V_{C2}(n) = V_{C2}(n - 1/2) - \frac{\Delta Q_{C2}}{C_2}$

This gives us $V_{C2}(n) = -V_{\text{off}} - \frac{C_1v_{\text{in}}(n)}{C_2}$.

From this we can determine, $v_{\text{out}}(n) = V_{\text{off}} + V_{C2}(n)$.

Hence, $v_{\text{out}}(n) = -\frac{C_1}{C_2}v_{\text{in}}(n)$.

Thus the offset gets cancelled in the two phase operation and the output voltage is an amplified version of the input voltage by a factor that is decided by the ratio of the capacitances.

![Figure 2-12: Offset cancellation and Amplification in a Resettable gain circuit](image)
Noise Analysis

The overall noise of a switched capacitor amplifier consists of the noise due to the opamp (which was explained earlier) and the noise due to the specific implementation of the switched capacitor itself. The overall noise power is calculated by taking the sum of all the noise power contributions. Here, a brief discussion on the noise contribution due to the switched capacitor operation is explained.

For simplicity, assume that the amplifier is ideal, noiseless with no input parasitic capacitance. When the capacitor $C_s$ is switched, it stores a noise charge of $q_n = kT C_s$. In the next phase, since the capacitor is connected to the virtual ground of an opamp, there can be no charge stored at the node, hence the entire charge is transferred to the capacitor $C_i$, if the opamp is noiseless. Due to the charge, the squared noise voltage developed across the capacitor is equal to $q_n^2 C_i$. This is equal to $\frac{kT C_s}{C_i}$. In a fully differential configuration, the overall squared noise voltage developed will be twice, since the differential paths are considered to be independent of each other.

Therefore, the noise contribution depends on boltzmann constant, and values or ratios of the capacitances, which are quite precise in modern CMOS technologies. Hence, the switched noise is a good source of thermal noise in addition to the high thermal
Considering the impact of the opamp noise, it manifests in two ways. In the amplification phase, the output referred thermal/shot noise is $\frac{m \beta kT}{4 \beta C_c}$, as derived earlier. The opamp noise also manifests due to the autozeroing as well. The input referred noise power of the opamp is given by $\frac{m B kT}{g_m}$, due to which, the noise charge stored on the capacitor $C_s$ is $q^2 = C_s^2 \frac{m B kT}{g_m}$. Due to the feedback capacitor $C_i$ in the amplification phase, the output thermal/shot noise power due to the opamp is then equal to $\frac{C_i^2}{C_s^2} \frac{m B kT}{g_m}$. The net thermal/shot noise power at the output is the sum of thermal/shot noise powers from the switched capacitor action itself, opamp in the amplification phase, and opamp noise transferred from the autozeroing phase to the amplification phase.

If the opamp has input parasitics, they are represented by replacing $C_s$ by $C_s + C_p$ in the above analysis. Hence, it is important to reduce the input parasitics of the opamp.

### 2.4.2 ADC

The analog-to-digital converter (ADC) converts the analog voltage to digital bits. It does so by comparing the analog voltage against a known reference voltage. The considerations and requirements for the ADC in this design are detailed below.

**Quantization Noise and Comparator Noise**

The digitization of an analog voltage results in the conversion of an analog voltage to a series of discrete voltage. This results in the addition of quantization noise to the input signal. Assuming that the quantisation noise is white and uncorrelated to the input signal, the quantisation noise variance can be added to the signal variance to include the impact of the quantisation noise $Q$.

Any noise due to the comparator is directly added to the sampled signal. The effects of both the quantization noise and comparator noise to the output of the sensor are similar.
We can understand the behaviour of the quantization noise and comparator noise from a simple mathematical abstraction. Let \( X_1 \) be the random variable representing the input signal (i.e. the thermal noise and shot noise), \( X_2 \) represent the comparator and quantization noise and \( V_{\text{ref}} \) represents the PTAT reference of the form \( bT \), where \( b \) is a known constant.

We know that \( E(X_1^2) \) will be of the form \( aT \), where \( a \) is a known constant. Hence \( E((\frac{X_1}{V_{\text{ref}}})^2) \) will be ideally of the form \( \frac{aT}{b^2T^2} \). If the actual random variable is now \( (X_1 + X_2) \) due to the quantization noise and comparator’s noise and offset, we get

\[
E \left( \frac{X_1 + X_2}{V_{\text{ref}}} \right)^2 = E \left( \frac{X_1}{V_{\text{ref}}} \right)^2 + E \left( \frac{X_2}{bT} \right)^2
\]

(2.6)

This gives us an additional term of \( E(X_2)^2 \).

While the offset at one particular temperature can be found easily, in order to calibrate out the offset at different temperatures, we will need to do multi-point calibrations—which defeats the purpose of the fundamental sensor.

Hence, it is important that any noise and offset introduced by the comparator are kept to a minimum in the design process itself, and schemes for self-calibration of the offsets of the comparator are introduced at different temperatures. The maximum allowable offset and noise can be calculated through our required accuracy target.

Our target accuracy is 1°C for a range of 140°C, i.e. 0.7%. Assuming the RMS noise voltage of the signal after amplification to be around 40 mV, we obtain that the RMS voltage error floor for the quantization and comparator noise and offset is around 3.4 mV. The comparator in this work is designed to have an RMS noise of 700μVrms at 300 K and the residual offset is 0.25 mV.

Since the RMS quantization noise voltage is given by \( \frac{\text{LSB}}{\sqrt{12}} \), this gives us the LSB to be around 11 mV. We design the reference voltage close to \( 3\sigma \) value of the thermal and shot noise expected at -40°C which is close to 120 mV. Thus a 4 bit ADC suffices to satisfy the requirements. By ensuring that the combined effect of all of these sources of noise is less than 3.4 mVrms, we can ensure that we meet our target accuracy.
Reference Voltage Noise

The final output that we are interested in is of the form \( \frac{V_{in}}{V_{ref}} \). Let \( N_i \) and \( N_r \) be the undesired signals (offsets/ unwanted noise) in the input and reference voltages respectively. Thus we would effectively be getting \( \frac{V_{in} + N_i}{V_{ref} + N_r} \). This expression can equivalently be written as \( \frac{V_{in}}{V_{ref}} \left( \frac{1 + \frac{N_i}{V_{in}}}{1 + \frac{N_r}{V_{ref}}} \right) \). Now assuming \( N_r \ll V_{ref} \), using binomial theorem, we can simplify the above expression to \( \frac{V_{in}}{V_{ref}} \left( 1 + \frac{N_i}{V_{in}} \right) \left( 1 - \frac{N_r}{V_{ref}} \right) \) which equals \( \frac{V_{in}}{V_{ref}} \left( 1 + \frac{N_i}{V_{in}} - \frac{N_r}{V_{ref}} + \frac{N_r N_i}{V_{ref} V_{in}} \right) \). The +/- signs are inconsequential for this analysis, as for the worst case analysis, all the noise sources are added (by virtue of being uncorrelated). We can see that the noise introduced in the reference contributes a different dependence than \( A \frac{1}{\sqrt{T}} \) dependence that we desire. Hence, it becomes important to reduce noise introduced in the reference.

To understand the tolerable limit on the reference voltage noise, we will consider how the reference voltage noise actually manifests in the SAR ADC configuration.

Thus, the reference noise is added in a code dependent fashion to the final output. Considering our target variable to be \( X_1 \) and the reference noise to be \( X_2 \). The overall noise variance can thus be simplified to \( E(X_1^2) + E(X_2^2) \).

The RMS voltage is the square root of this value. Thus, similar to quantization noise of the ADC, the maximum limit on the allowable reference voltage noise is defined by the acceptable inaccuracy of the temperature sensor.
2.4.3 Variance Calculation

The noise analysis results presented in this chapter have been derived assuming we have infinite time samples of measurement available. However, in the practical implementation, we will have a certain finite number of samples we can take in order to calculate the variance to determine the temperature. The lower bound on the number of samples necessary to calculate variance is determined by the required accuracy from the sensor.

The sample variance calculated from the thermal noise and shot noise voltage, $V_{\text{sig}}$ and the PTAT reference voltage, $V_{\text{ref}}$ is equal to the variance of $\frac{V_{\text{sig}}}{V_{\text{ref}}}$, which is of the form $\frac{A}{T}$, where A is a known constant. The allowable error in temperature is $\pm 1^\circ C$, hence the error in variance would be $\frac{A}{T} - \frac{A}{T+1}$ that is approximately equal to $\frac{A}{T^2}$.

To determine the number of samples, we need to make sure that the $3\sigma$ value of the variance lies within $\frac{A}{T^2}$.

The number of samples can thus be found by finding the standard deviation of sample variance, which gives us a minimum bound on the number of samples required. The variance of a sample variance is given by the formula $\sqrt{\frac{2\sigma^4}{N}}$. From these results, we find that the minimum number of samples required is equal to $18T^2$, which comes to around 2.9E6 samples for $T=400K$.

Thus we need at least 2.9 million samples to be able to reach the targeted accuracy constraints.

2.5 Summary

In this chapter, the theory of fundamental sensing and underlying concepts were explained. The overall architecture was developed and the mathematical bounds and constraints on different components was elucidated. In the following chapter, we will go into the details of the circuit level implementation of the proposed architecture.
Chapter 3

Circuit Implementation

In order to demonstrate the idea, a proof-of-concept chip has been designed in TSMC 65nm Low Power technology and is currently being tested. In this chapter, the circuit design and layout of the proposed temperature sensor are described in detail.

3.1 Overall Structure

The overall design is shown in Figure 3-1. It consists of a thermal noise and shot noise generator with autozeroing. This is implemented using switched capacitor amplifier circuit. The generated thermal noise and shot noise voltage is then amplified by another switched capacitor amplifier. The thermal noise and shot noise voltage is then converted to digital bits using a 4 bit SAR ADC. A PTAT voltage reference with a reference buffer to drive the voltage source act as the voltage reference for the ADC. The reference voltage buffer also has autozeroing to eliminate any offsets that could be temperature dependent and affect the linearity of the reference. The details of implementation of each of these blocks is further delineated in the following sections.
3.2 Noise Generator and Amplifier

As explained in the previous chapter, we design switched capacitor amplifiers in the analog front-end to generate the temperature dependent noise signals and further amplify them. In order to reduce the impact of flicker noise as well as low-frequency offsets, we implement autozeroing in the switched capacitor circuits. The switches are implemented as NMOS switches, since the common mode voltage is 300 mV, and the maximum differential output voltage expected at the final output is of the order 200 mV. The circuit implementation of the analog front end is shown in Figure 3-2. The
switching is done in a different manner from that explained in the previous chapter - this is to make sure that the switching is parasitic insensitive. The rest of the operation is similar as described in the previous chapter. To illustrate the operation, time domain waveforms in the two phases of operation are shown in Figure 3-3 for a sinusoidal input. The two phases are shown by CLK1 and CLK2. In the actual implementation, there is no external input voltage source. Here, a sinusoidal input is used for illustration. Vin represents the input differential voltage and Vout represents the output differential voltage. In one of the phases, the output tracks the sinusoid and amplifies it, whereas in the other, it stores the opamp offset.

![Figure 3-3: Output Waveforms of the Amplifier for a Sinusoidal Input](image)

### 3.2.1 High Shot Noise Amplifier

The design uses a high shot noise amplifier, biased carefully such that the overall output referred noise voltage variance is linearly proportional to temperature. To enable this, the input transistors are of PMOS type and sized large to reduce the flicker noise contribution. A 2-stage operational amplifier is designed with a folded
cascode first stage and common source second stage. This is shown in Figure 3-4.

![High Shot Noise Amplifier](image)

**Figure 3-4: High Shot Noise Amplifier**

The first stage is designed such that the noise contributing transistors M2, M3, M10, M11, M14 and M15 are biased in deep weak inversion, thus producing shot noise. This is to ensure that the output referred shot noise of the closed loop amplifier does not have a temperature dependence.

To ensure that the maximum device frequency is at-least an order higher than the bandwidth requirement, close to minimum length transistors are chosen. Due to this, the gain from the amplifiers is low, and a second stage is also introduced. The noise contribution from the second stage is divided by the open loop gain of the first stage, which is temperature dependent. To reduce the contribution of the second stage noise, we thus introduce gain enhancement amplifiers in the first stage. This also gives an additional increase in the open loop gain of the amplifier. The open loop gain of the amplifier is 80 dB, to ensure that the closed loop gain is as close to ideal as possible.

Since amplifier noise also gets added during the autozeroing phase, we need to make sure that the amplifier stays stable, where the amplifier is connected in a unity gain feedback configuration in the closed loop. The compensation is switched during the amplification and offset storage phase such that $C_4 > C_2$ and $C_3 > C_1$. A fully differential configuration is designed to make the design more robust to any common mode voltage changes. Since the design is fully differential, a common mode feedback circuit is introduced to ensure stable common mode voltages.
3.3 Voltage Reference

As explained earlier, the analog to digital converter requires a voltage reference to compare the analog signal and generate the digital bits. In this work, a PTAT voltage reference was designed which is followed by a reference voltage buffer, as shown in Figure 3-5. The circuit designs of both of the components is delineated in this section.

![Figure 3-5: Voltage Reference](image)

3.3.1 PTAT Voltage

The PTAT Voltage is designed using BJTs as shown in Figure 3-5. The core principle of generating the PTAT voltage is based on the positive temperature coefficient of $\Delta V_{BE}$ as described in the previous chapter. In the actual implementation, the accurate difference of the two $V_{BE}$ voltages is implemented with the help of an opamp. Instead of using current ratios, here the same current flows through both the BJTs, and the sizes are ratioed instead. The current through the resistor $R_1$ is PTAT in nature and equal to $\frac{kT \ln(24)}{qR_1}$. The current is mirrored through current mirrors and the effect of channel length modulation is reduced by the use of cascode transistors. The resistances $R_1$ and $R_2$ are both of the same type, and thus vary similarly with temperature. The voltage across $R_2$ is the final PTAT voltage and is equal to $\frac{kT R_2}{q R_1} \ln(24)$. An additional transistor is also added for start-up.

To implement the opamp, a major consideration is the offset voltage, since there is no
offset cancellation scheme and any offsets in the opamp result in non-linearity of temperature dependence. Hence the opamp is implemented as a single stage amplifier, with one of the sides cascoded (to give an additional gain factor of 2). The number of transistors in this opamp is kept as low as possible to reduce the impact of any systematic and random offsets. The schematic of the opamp is shown in Figure 3-6.

![Opamp schematic](image)

Figure 3-6: Opamp designed in the PTAT Voltage Source

### 3.3.2 Reference Voltage Buffer

Depending on the SAR ADC switching, the load to the reference voltage will be switched. To ensure that the ADC gives a correct output, it is necessary to ensure that any kickback to the reference voltage settles before the next comparison. To ensure fast settling, it is also important for the reference to have a low output impedance. To ensure this, a reference buffer is added in the design. A 2 stage opamp is designed with a 2 pF capacitance at the output such that the second stage pole is the dominant pole. This is done to reduce the $g_m$ requirement on the input transistors, and thus reduce the current consumption.

Due to the large capacitance at the output of the buffer, the capacitance can store the reference voltage and provide the required voltage in switching. This approach does lead to a constant gain error in the output voltage due to capacitive dividing (1.6%), which can be corrected in the digital code.

Autozeroing of the reference buffer is done during the purging phase to reduce the
impact of any offsets (especially those that might be temperature dependent).

Figure 3-7: Low Power Reference Buffer

3.4 SAR ADC

Due to its energy efficient operation, a 4 bit SAR ADC was used for the analog-to-digital conversion. A conventional switching scheme and SAR logic was designed [6]. The overall SAR design is shown in Figure 3-8. A fully differential scheme is designed and the SAR logic (Figure 3-9) decides the state of switching in the purging and bit-cycling phases [2].
The autozeroing of the comparator happens during every purging phase of the ADC. The voltages VCM and VCM1 are different, as VCM1 is decided on the basis of the common mode voltage necessary for the self-calibration scheme used for the comparator offset calibration. The offset calibration scheme for the comparator is elucidated later in this section.
To ensure that the DAC is highly linear, besides careful layout, a calibration capacitor array and logic is also added similar to [12] to account for any non-linearity due to mismatch. The schematic is shown in Figure 3-10.

![Figure 3-10: Calibration Logic added to the DAC](image)

The critical component was the comparator which is required to have a low offset and low noise. The design of the comparator is elucidated below.

### 3.4.1 Comparator

As elucidated in chapter 2, the comparator needs to have a low noise and low offset, while consuming low power. While offset in a comparator can be calibrated, the noise cannot. A low-noise dynamic Miyahara comparator topology is used in this design to achieve the desired specifications [23]. This design is used since it is based on a double-latch type comparator topology, and thus has low noise, since the noise of the second latch stage is divided by the gain of the first stage. The offset is reduced by the use of a charge pump scheme explained later. The comparator is also dynamic, due to which it consumes very low power. The schematic is shown in Figure 3-11. In this design a PMOS input pair is designed.
The operation of the Miyahara comparator can be divided into four phases—reset, pre-amplification, regeneration and decision. During the reset phase, the CLK is high and the transistors M3 and M4 are switched on, due to which Di+ and Di- are pulled low. Since the PMOS transistors M6 and M9 have their gates connected to the ground voltage, they are switched ON, and thus the outputs Voutp and Voutn are both equal to VDD. This resets the comparator.

As the CLK goes low, the comparator enters the pre-amplification phase where M3 and M4 are switched off, and M5 starts to switch ON. The input transistors M1 and M2 start to charge Di+ and Di- (from initial zero voltage in reset) at different rates depending on the input differential voltage $\Delta V$.

If $Vinp > Vinn$, then $I_{M1} < I_{M2}$, thus Di+ < Di-. As the nodes Di+ and Di- begin to go high, they also start to switch off the transistors M6 and M9 which were pinning the output to VDD. Meanwhile, the NMOS transistors M8 and M11 also start to switch
As the common mode voltage between Di+ and Di- continues to rise, at one point, the transistors M6 and M9 cannot pin the output to VDD anymore and the comparator enters the regeneration phase. In the regeneration phase, the difference between Di+ and Di- is amplified because of positive feedback. As a result of this, Di+«Di-, M6 is switched ON, hence Voutp is pulled to VDD. Since Di-»Di+, M11 is switched on. Since Voutp is HIGH, M15 is turned on. Both M11 and M15 pull down Voutn to GND, thus generating the final decision. [16]

The design also incorporates a self-calibrating charge-pump based offset calibration scheme to reduce the offset introduced by the comparator. An additional set of transistors Mcal1 and Mcal2 are added to store the offset. During each autozeroing/purging phase, the comparator inputs are both connected to VCM1, and the outputs of the comparators are used to store the residual offset on the capacitor. The voltage on the capacitor is VC, and time domain waveforms for the offset cancellation scheme are shown in Figure 3-12.

![Offset Calibration (Time Domain Waveforms)](image)

Figure 3-12: Offset Calibration (Time Domain Waveforms)
Here, CAL represents if the comparator is in calibration mode and CLK represents the clock. A positive inout differential voltage of 1 mV is given to the comparator, and we can see that the comparator output COMP-OUT goes to VDD after calibration phase is over and the offset voltage is calibrated. Hence, in a few conversions of the SAR, the comparator starts giving the correct output. Since we are interested in around million samples, we can skip the initial few samples while calculating the variance.

3.5 Non-Overlapping Clock Generator

The switched-capacitor circuits and offset cancellation blocks require non-overlapping clocks. These are generated using the following circuit. [1] Appropriate delays are added to ensure correct timings and non-overlap. The circuit can be used to generate timing for signals that need to be switched off earlier ($\phi'_1, \phi'_2$) or later ($\phi_1, \phi_2$).

![Non-Overlapping Clock Generator](image)

Figure 3-13: Non-Overlapping Clock Generator

3.6 Layout

The chip was designed in a TSMC 65nm Low Power technology. Since the design is fully differential, the layout is carefully done in a symmetric fashion to avoid any systematic and random layout dependent offsets. A common centroid layout was separately employed for all the matching components, to reduce the effect of random
offsets due to fabrication. The resistors have been arranged in an interdigitated fashion. [10]

The ADC is also layouted in a fully symmetric fashion. The critical layout component is the DAC, which is designed in an interdigitated fashion [7]. The layout of the DAC is shown in Figure 3-14. Since the DAC is fully differential, there are two DACs that are placed symmetrical to each other. The layout of the BJTs is critical to ensure linearity of the PTAT reference. The BJTs were also arranged in a common centroid fashion for this purpose.

![Figure 3-14: DAC Layout](image)

### 3.7 Summary

In this chapter, a detailed circuit level implementation of the system was explained. The techniques used to maintain linearity of temperature dependence were also elucidated. In the next chapter, the simulation results are presented.
Chapter 4

Simulation Results

In this chapter, the simulation results of the prototype sensor are presented. The results are analyzed and proof-of-concept is validated through the simulation results.

4.1 Amplifier Noise Measurement

The closed loop noise of the amplifiers is evaluated using a small signal AC analysis to ensure that the shot noise characteristics of the amplifier with temperature are highly linear as expected. The results are shown in Figure 4-1. To evaluate linearity, the maximum deviation from the best-fit line was calculated and found to be 0.2°C.

Figure 4-1: Variance of the Amplifier with Temperature
4.2 PTAT Reference Voltage

To achieve a high untrimmed accuracy, the PTAT reference voltage needs to be highly linear with temperature. The simulated performance of the reference voltage with temperature is shown in Figure 4-2. To evaluate linearity, the maximum deviation from the best-fit line was calculated and found to be $0.4^\circ C$.

![Figure 4-2: PTAT Reference Voltage with Temperature](image)

4.3 Overall Noise Variance with Temperature

The overall voltage from the analog front end is simulated using transient noise simulations and the results are shown in Figure 4-3. In order to evaluate the linearity, the maximum deviation from the best fit line was calculated and found to be $0.6^\circ C$. 
4.4 Power Consumption

The overall power consumption of the temperature sensor is $77\mu$W. The breakdown of the power consumption by different blocks is shown in Figure 4-4. The power consumption from variance calculation is not taken in account here as it is implemented off-chip in this proof-of-concept chip.
4.5 Summary

In this chapter, we investigated the simulation results of the proof-of-concept chip. We will go into the comparison with the state of the art in detail in the next chapter, along with the contributions of the thesis and other future work.
Chapter 5

Conclusions and Future Work

In this chapter, the thesis is concluded with a comparison with the state of the art, summary of the thesis contributions and a discussion on the future possibilities this research paves avenues for.

5.1 Comparison with State-of-the-Art

The simulated results of the proposed sensor are compared with the state of the art temperature sensors in literature [19] and presented in table 5.1.

<table>
<thead>
<tr>
<th></th>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature range</td>
<td>-55 to 125</td>
<td>-40 to 125</td>
<td>-20 to 130</td>
<td>-25 to 125</td>
<td>-50 to 130</td>
<td>-50 to 130</td>
<td>-40 to 100</td>
</tr>
<tr>
<td>Principle</td>
<td>Resistor &amp; Thermal Diffusivity</td>
<td>BJT Based</td>
<td>Bulk Diodes</td>
<td>BJT</td>
<td>BJT</td>
<td>BJT</td>
<td>Noise and BJT</td>
</tr>
<tr>
<td>3σ Inaccuracy</td>
<td>±0.25</td>
<td>±1.7</td>
<td>±1.5±2</td>
<td>±1.85</td>
<td>±1.8</td>
<td>±2</td>
<td>±1</td>
</tr>
<tr>
<td>Trimming Points</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Conversion Time</td>
<td>10 ms + (1000 ms)</td>
<td>4.1 to 32.8 ms</td>
<td>12.8μs</td>
<td>8.2μs</td>
<td>0.27μs</td>
<td>0.03μs</td>
<td>375μs</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>66μW + (5.1 mW)</td>
<td>37μW</td>
<td>17.9μW</td>
<td>18.75μW</td>
<td>17.6μW</td>
<td>1210μW</td>
<td>77μW</td>
</tr>
<tr>
<td>Energy(nJ)</td>
<td>6.6E2 + (5.1E6)</td>
<td>1.2E3</td>
<td>2.3E-1</td>
<td>3.6E2</td>
<td>3.5E1</td>
<td>3.3E2</td>
<td>28.9E3</td>
</tr>
</tbody>
</table>

Table 5.1: Comparison with State of the Art Temperature Sensors

In [26], the accuracy is achieved by using the thermal diffusivity sensor for calibration. The relative inaccuracy figure of merit is calculated and shown in Figure 5-1 to compare with the current state of the art sensors.
5.2 Thesis Contribution

CMOS Temperature Sensors are increasingly becoming ubiquitous. However, in order to achieve high levels of accuracy, they require at-least a one-point temperature trim. Trimming is an expensive process and also results in substantially increased testing time in mass production; thus increasing the cost significantly. To tackle this problem, the use of thermal noise and shot noise amplifiers and PTAT voltage reference was presented in this work. The notion of solely relying on fundamental and ratioed quantities is a new paradigm introduced in the design of temperature sensors. The design can be used as a calibration source in conjunction with other types of sensors to achieve high performance. To compensate for any run-to-run variation of capacitance, a batch calibration of gain error can be performed, which is much more cost and time effective than individual trimming.

Fabricated in 65 nm TSMC Low Power Technology, the simulated untrimmed accuracy of the sensor achieves state-of-the-art performance. The proposed temperature
sensor has a simulated $3\sigma$ inaccuracy of $\pm 1^\circ$C, while consuming a power of $77\mu$W, a similar order of magnitude as other state-of-the-art sensors. Instead of individual trimming, a batch calibration is necessary to remove the effect of run to run capacitance variation.

5.3 Future Work

This work presents the first proof-of-concept chip, due to which not all metrics were optimized. This presents opportunities for further research and optimizations. One of the most useful directions with this work going forward is reducing the time of conversion. Since the goal is to find a huge set of uncorrelated samples, multiple analog sensors can be time multiplexed onto a single chip. For $N$ such sensors, the time of conversion reduces by a factor of $N$. Concepts from linear system modelling could also be exploited to model the specific use-case scenarios appropriately. This would enable only a one-time latency to measure the initial temperature, and on the basis of the system parameters, the problem can be simplified to deduce the real-time temperatures. Hence, the time of conversion would not be a problem.

Further ideas that can be explored are power and area optimizations along with higher clock rates. In this work, the digital back-end is implemented through an off-chip FPGA. This could further be integrated with the chip and variance can be computed on a sample-by-sample basis to avoid excessive memory on chip and efficient computation.

As the concepts of fundamental sensing were explored, besides being used as a calibration source with other sensors, this opens up avenues for cryogenic sensing. These sensors can be immensely useful for applications requiring integrated cryogenic temperature sensors (such as quantum processors). An exploration into this domain would enable integration of CMOS temperature sensors down to cryogenic scales and would be immensely useful for quantum processors and cryogenic equipment. [15]
Bibliography


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