# High performance $MoS_2$ transistors based on wafer-scale low-temperature MOCVD synthesis

by

Jiadi Zhu

B.S., Peking University (2018)

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

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## Abstract

Among all the possible back-end-of-line (BEOL) solutions to improve the integration density and functionality of conventional silicon circuits, two-dimensional (2D) material devices are believed to be very promising, due to their high mobility, relatively large band gaps, atom-level thickness, performance comparable to the one of silicon devices, and great potential in realizing 3D integration. However, wafer-scale growth of high-quality, continuous 2D materials thin film with BEOL compatible temperature (< 400 ºC) and good uniformity has always been difficult to realize. To achieve low contact resistance to these materials is also very challenging and hinders the development of 2D material devices and circuits.

In this thesis, we will demonstrate a novel 8-inch, BEOL-compatible metal organic chemical vapor deposition (MOCVD) method for the synthesis of 2D transition metal dichalcogenide materials with growth temperature lower than 400 ºC. Highly-scaled high-performance $MoS_2$ transistors will also be investigated with different contact engineering methods. These findings represent crucial steps for high performance power electronic circuits as well as realizing ultra-large scale BEOL integration with silicon circuits.

Thesis Supervisor: Tomás Palacios
Title: Professor of Electrical Engineering and Computer Science

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# Chapter 1

# Introduction

In the past seven decades, silicon technology has been rapidly developed to an unprecedented level, advancing people's lives and changing the world in ways people would have never imagined. Not only the size of the electronic devices has been scaled down from hundreds of microns to tens of nanometers, but the number of the devices in an integrated circuit has dramatically increased from less than ten [1] to more than 2.6 trillion [2]. However, such process has slowed down in the past 20 years due to the approaching of the physical limits at the nano-scale and the difficulties in realizing higher integration density [3]. Back-end-of-line (BEOL) integration [4] is proposed as a possible approach to continue to increase the integration density by stacking more layers of materials and devices on top of a silicon wafer where silicon devices and circuits are already fabricated. This could also increase the functionality of future silicon chips. Yet, more investigations are need to discover the most suitable material system for BEOL integration. Development on highly-scaled high-performance transistors are also needed as they would be the most basic building blocks for future electronics. In this thesis, we study different approaches to grow BEOL-compatible wafer-scale 2D materials. We also investigate the contact engineering methods that would reduce the contact resistance in 2D material transistors to make them more practical for BEOL integration. Finally, we will provide possible methods to scale the transistor dimensions further.

# 1.1 Emerging Materials for Back-End-of-Line Integration

To increase the integration density in future microsystems, researchers have proposed the concept of back-end-of-line integration (BEOL), which, instead of making microelectronic chips out of a single layer of silicon circuits, it stacks multilayers of semiconductor circuits on top of the silicon integrated circuit on the holding wafer. Such method could potentially increase the integration density and also enable the integrated circuit to have more and more functionalities. RF circuits, memory circuits, sensor arrays and many other circuits could be fabricated on top of the silicon logic circuit without causing performance degradation.

Among all the emerging material systems, there are several that have shown significant promise and have gone through relatively complete investigations (Figure 1.1). Some examples include carbon nanotubes [5-7], oxide semiconductors [8-10], and the 2D van de Waals materials [11-13]. All these material systems have been considered as potential materials for future electronics, especially for back-end-of-line integration.

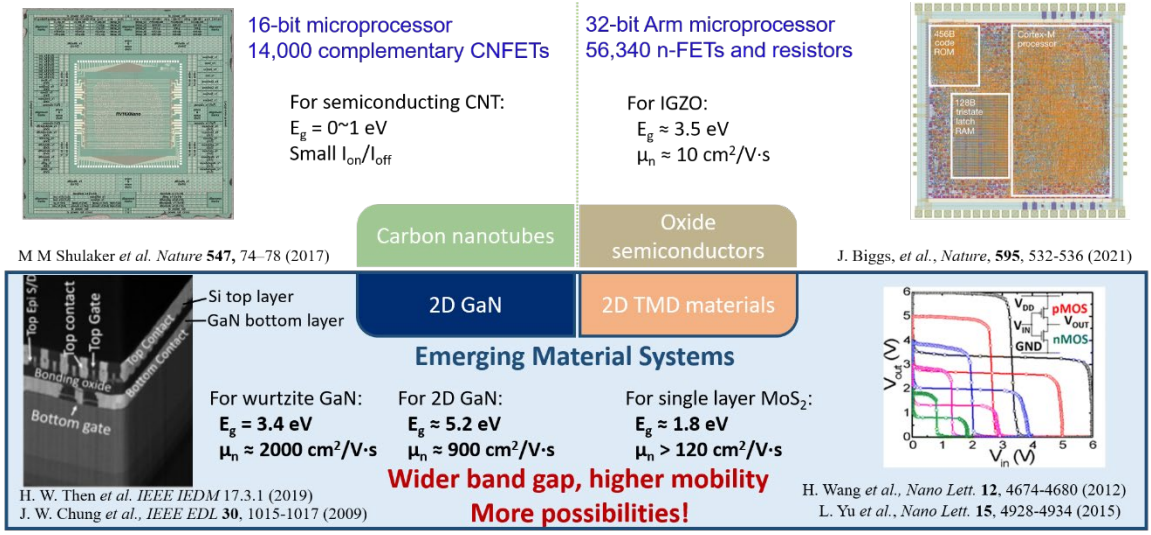


Figure 1.1 Circuit level demonstrations using novel material systems.

Carbon nanotubes (CNT) are one of the most matured low dimension materials. In the past two decades, researchers have done abundant work on improving the purity of CNT [14,15] and optimizing the device performance of semiconducting CNT field effect transistors [16,17]. State-of-the-art CNT transistors demonstrate high on-current of around 1.0 mA/μm [16], which is comparable to silicon transistors at the same operation voltage, but the on/off current ratio of CNT transistors (around 3 orders of magnitude) is still smaller than silicon transistors. From 2013 to now, S. Mitra, P. Wong and M. Shulaker et al. have also developed very-large-scale integrated circuit and corresponded BEOL technology based on high purity semiconducting CNT transistors and with a total transistor number of around 14,000 [6]. However, the small bandgap of semiconducting CNTs would lead to large leakage current in the off-state, which would eventually limit its applications for ultra-large-scale BEOL integrated circuits due to high power dissipation and severe short channel effect.

Oxide semiconductors, e.g. indium tin oxide (ITO) and indium gallium zinc oxide (IGZO), are also promising candidate for BEOL integration. Y. Wu et al. [8, 18] have demonstrated high performance IGZO transistors with 1.0 mA/μm current and high on/off current ratio up to 10 orders of magnitude, which could be even better than silicon devices at the same technology node. In 2021, Arm Ltd. also announced its flexible integrated circuits based on IGZO, which consists of more than 56,340 transistors and resistors [10]. However, since the IGZO channel is normally formed by sputtering, the channel carrier mobility would be normally around or lower than 10 $cm^2/Vs$, which is about 100 times lower than the value in silicon. It is also difficult to find a suitable material for p-type transistors among the various metal oxides, which hinders the fabrication of complementary metal-oxide-semiconductor (CMOS) logic in oxide semiconductor circuits [19]. Pure nMOS circuit design would lead to huge power consumption and may not be practical enough for future BEOL integration.

2D materials stand out as a very promising candidate among all these emerging materials due to their atom thin layer thickness, clean interface, and high mobility [20-22]. The 2D material system also provides rich choices from semi-metals, e.g. graphene, to semiconductors with a wide range of band gaps, to insulators as hexagonal boron nitrides and cubic boron nitrides. This enables complete BEOL integration purely with 2D

materials, as they could function not only as n-type and p-type semiconductors, but also metals and insulators.

$MoS_2$ and $WSe_2$ are often considered as two of the most mature 2D transition metal dichalcogenide (TMD) materials. Since 2011, our group has demonstrated the feasibility of using 2D materials to fabricate both nMOS [11] and CMOS [12] circuits based on many different 2D semiconducting channels. Compared with silicon and germanium, the relatively large band gaps in $MoS_2$ and $WSe_2$ allow them to efficiently reduce source-to-drain tunneling and corresponded large leakage current at extremely small channel length, which not only relieve the short channel effect to some extent, but also reduce the power consumption. Other 2D materials, such as monolayer 2D GaN [23], which has an even wider band gap (~5.2 eV) than the bulk GaN (3.4 eV), provide even more possibilities for power electronic circuits and radio frequency applications.

## 1.2 Low Temperature Synthesis of 2D Materials

2D materials are very promising for BEOL integration. However, a fundamental step to realize BEOL integration is to develop wafer-scale material synthesis methods. The previous work mostly demonstrated centimeter-scale synthesis of 2D TMD materials. Wafer-scale synthesis has also been shown on 4-inch [13] to 6-inch [24] wafers. However, most of these methods use chemical vapor deposition (CVD), which requires high growth temperature (>550 ºC). This would damage the silicon devices if we want to directly deposit the 2D materials on top of a BEOL wafer. Moreover, the solid precursors used in the CVD system need to be typically placed very close to the target substrate and the evaporation of the precursor fully depends on the local temperature, making it difficult to carefully control the growth rate and uniformity [25].

Accordingly, more advanced synthesis methods are needed to provide 2D materials with a synthesis temperature below 400 ºC, which is the highest temperature allowed by the BEOL integration [26]. Plasma enhanced systems are possible choices, as plasma could normally assist and accelerate the decomposition of precursors and allow the reaction to happen at a lower temperature. Plasma enhanced atom layer deposition (PEALD) and plasma enhanced chemical vapor deposition (PECVD) have been demonstrated as a

possible approach to realizing lower temperature synthesis compared with normal CVD methods. Yet the quality of the synthesized materials has always been problematic, as defects can easily be generated by the plasma, and the thickness of the synthesized materials is also challenging to be controlled accurately [27,28]. These deficiencies make it difficult to directly make integrated circuits based on PECVD or PEALD grown TMD materials.

Another possible way to realize low temperature integration is to use metal-organic chemical vapor deposition (MOCVD). The use of liquid precursors or low-melting point solid precursors could provide gas-type precursor flows in the reaction chamber. This will make it easier to control the reaction speed and lower reaction temperature can be realized. In 2015, J. Park et al. have demonstrated the MOCVD synthesis of uniform monolayer TMD materials on 4-inch substrates [13]. However, the growth temperature (550 $^{o}$C) is still much higher than what is required by BEOL integration. Alkali metal salts, e.g. NaCl, are often needed in this synthesis process to ensure large grain size of the TMD material. These compounds are however harmful for silicon circuits as the movable alkali metal ions could cause significant hysteresis in silicon transistors and eventually lead to device failures. Accordingly, more investigations are needed to ensure wafer-scale, low temperature synthesis for BEOL integration.

## 1.3 High-performance 2D Material Transistors

Once wafer-scale high-quality material is available, high performance 2D material transistors are needed for realizing BEOL integrations. A key requirement for these high-performance devices is the availability of ultra-low contact source and drain technologies [29,30]. Contrary to the bulk material transistors, in which covalent bonds could be easily formed between the metal contact and the heavily doped source/drain regions, as is shown in Figure 1.2a, a van de Waals interface is typically formed between the metal contacts and the source/drain regions in 2D material transistors (Figure 1.2c). This introduces a relatively large tunneling barrier and a wide Schottky barrier at the contact interface (Figure 1.2d) which reduces carrier injection and consequently induces a large contact resistance. Low work function materials, such as Ti and Sc, can be used to reduce the tunnel junction

height [31]. However, they are also easily affected by the defects inside the source/drain regions of the 2D material (Figure 1.2e). In these cases, strong Fermi pinning effects would be observed. Even if a low tunneling barrier is expected, the Fermi level of the low work function metal would be pinned in the middle or even the bottom part of the 2D material band gap, which still results in high tunneling barrier and large contact resistance. Accordingly, more research needs to be done to further understand the mechanism for metal contacts on 2D materials, and more improvements are needed to reduce the contact resistance in 2D material transistors.

Moreover, the scaling of 2D material transistors [32,33] is also important to achieve smaller device area and higher device performance. The relatively wide band gap of most monolayer 2D materials would be helpful in reducing the short channel effects at small channel length, compared with silicon transistors. The atomic thickness of 2D materials would also be useful to fabricate multilayer or multi-channel devices that would further enhance the device performance and integration density. These unique properties illustrate the great advantages of using 2D van de Waals materials for BEOL integration.

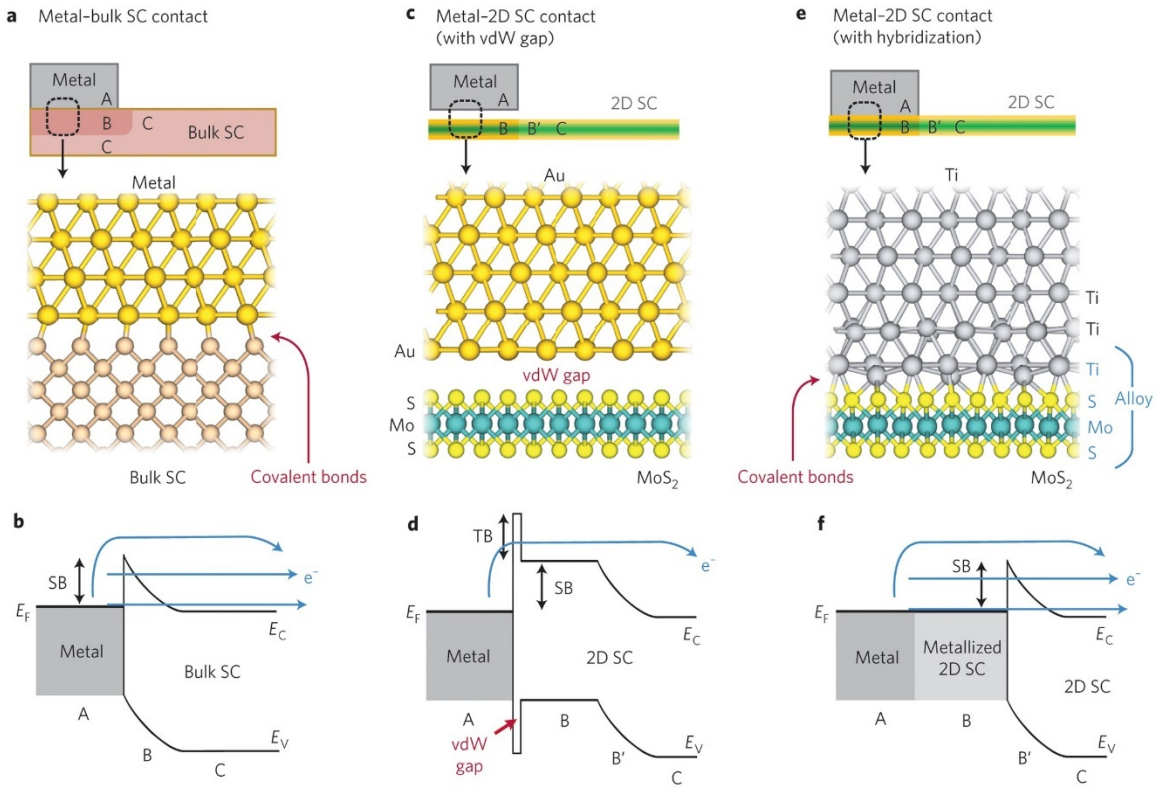


Figure 1.2 Different types of metal–semiconductor (SC) junction and their respective band diagrams. a,b, Schematic (a) and corresponding band diagram (b) of a typical metal/bulk

SC interface. c,d, Metal/2D SC interface with vdW gap (for example, Au–$MoS_2$ contact). e,f, Metal/2D SC interface with hybridization (for example, Ti–$MoS_2$ contact, where $MoS_2$ under the contact is metallized by Ti). EF, EC and EV represent the Fermi level of the metal, and the conduction and valence bands of the 2D SC, respectively. TB and SB indicate the tunnel and Schottky barrier heights, respectively. A, B, B' and C represent different regions in the current path from the metal to the SC. The blue arrows in b, d and f represent the different injection mechanisms. From top to bottom: thermionic emission, thermionic field emission and field emission (tunneling). In d, only thermionic emission is available. [29]

# 1.4 Thesis Goals and Outline

In this Thesis, we aim to develop a novel low-temperature, wafer-scale synthesis method that would efficiently provide high-quality, monolayer 2D material samples for device and circuit applications. We will also investigate the contact engineering methods which allows good ohmic contact to be formed between the metal contacts and the 2D material channels. Lastly, we will look into the potential scaling methods that would allow the ultimate scaling of electronic devices.

Chapter 2 will mainly focus on the material synthesis. Based on the metal-organic chemical vapor deposition method, we will study the growth mechanism in detail, trying to understand the crucial parameters for 2D material growth, and use these understandings to develop a novel synthesis method that would allow the 2D materials to be grown with the lowest growth temperature possible, good uniformity and large grain size. We will work on the design and setup of an 8-inch MOCVD system that would allow uniform 2D material growth on wafer scale. We will also pay special attention to making the growth method to be CMOS compatible and with minimum contamination.

Chapter 3 will investigate the different contact engineering methods that would allow lower source/drain contact resistance in n-type $MoS_2$ transistors. We will look into the methods of using clean van de Waals interface and phase transition/doping methods to experimentally reduce the contact resistance, which would provide valuable experience for high-performance 2D material transistor design and fabrication.

Chapter 4 will discuss the design and fabrication of highly-scaled high-performance transistors based on 2D materials and the aforementioned contact engineering methods. We will discuss the possible ways to realize the ultimate scaling of high-performance transistors based on the scaling of the channel length and the contact Length.

Finally, Chapter 5 will summarize the main findings of this work and give suggestions and possible directions for future work.

# Chapter 2

# Wafer-scale Low-temperature MOCVD Synthesis of 2D Materials

To develop wafer-scale (≥ 8-inch), low-temperature (< 400 ºC) synthesis methods of 2D materials is essential for BEOL integration. In this chapter, we will discuss the method to realize wafer-scale, low-temperature synthesis of $MoS_2$ with metal-organic chemical vapor deposition (MOCVD). We started from a 1-inch MOCVD system available in our group at the beginning of this project, to demonstrate the general growth method, the selection of seeding promoters, and the effect of material flow rate on material quality. From these understandings, we designed and built an MOCVD system based on a 10-inch hot wall tube furnace. By applying the knowledge that we learnt from the 1-inch MOCVD growth, we successfully realized wafer-scale $MoS_2$ growth on 8-inch wafers. The proposed method is compatible with silicon CMOS circuits and BEOL integration.

## 2.1 Metal-organic Chemical Vapor Deposition

### 2.1.1 Operation principle

The Metal-organic chemical vapor deposition (MOCVD) method can be used for the synthesis 2D TMD materials. By taking advantage of the relatively low melting points and decomposition temperature of the organic precursors, MOCVD method could realize a

synthesis temperature hundreds of degrees Celsius lower than the conventional CVD methods. Moreover, due to the low melting points, the organic precursors are in gas type when come into the reaction chamber, providing much better controllability over the growth process.

In our 1-inch MOCVD system for $MoS_2$ growth, we are using $Mo(CO)_6$ and $(C_2H_5)_2S$ as the precursors for molybdenum and sulfur, respectively. While the diethyl sulfide is liquid at room temperature, the molybdenum hexacarbonyl is a solid precursor. However, owning to its relatively low melting point (150 °C), it sublimates constantly in argon at room temperature, which provides relatively stable supply of the molybdenum atoms. Figure 2.1 shows the schematics of our 1-inch MOCVD system. The solid precursor of molybdenum is placed in two 90-degree elbows separated by a metal mesh. When the argon carrier gas is flowing through the solid bubbler, it can take away the sublimated molybdenum hexacarbonyl and bring it into the hot wall tubes. Same process also happens in the liquid bubbler, where diethyl sulfide evaporates and is brought into the reaction chamber by the carrier gas. The flow rate of the precursors is controlled by two mass flow controllers (MFCs) separately. Another MFC is used to introduce more argon into the system to accelerate the total gas flow to pump away the side products, e.g. hydrogen sulfide, sulfur powders and amorphous carbon. A separate line for hydrogen is also designed in the system for accelerating the decomposition of the sulfur precursor. However, it is not frequently used due to the potential etching effect of hydrogen to $MoS_2$.

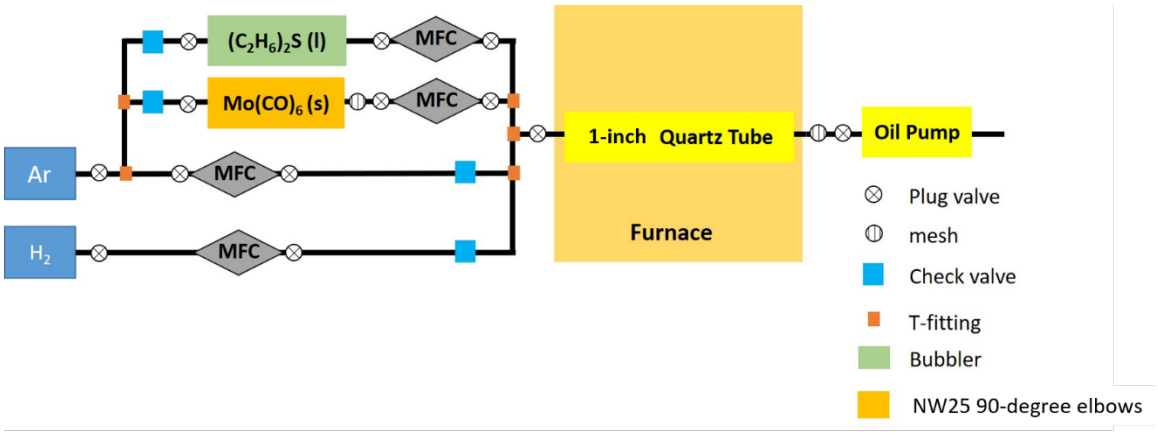


Figure 2.1 Schematics of the 1-inch MOCVD system.

The reaction chamber is connected to an oil pump to realize low-pressure environment (~ 7 Torr during growth). Seeding promotors would be needed during the growth process to ensure successful seeding process and large grain size of the synthesized material. The system is placed inside a fume hood due to the toxicity of the precursors and side products.

### 2.1.2 Growth of monolayer 2D materials

In the 1-inch MOCVD system, we use a single zone hot wall tube furnace as the reaction chamber. The temperature at the central part of the furnace is set to 800ºC. Considering the power dissipation at the two open ends of the tube furnace, a temperature gradient is formed. The 800 ºC central temperature would ensures a temperature of around 200ºC at the ends of the tube furnace (Figure 2.2). Such temperature gradient would allow hundreds of degrees Celsius of temperature changes within a distance of few centimeters. Yet this distance is not large enough to allow significant changes in the density of the precursors. Accordingly, we can study the growth condition at different temperature within one synthesis batch.

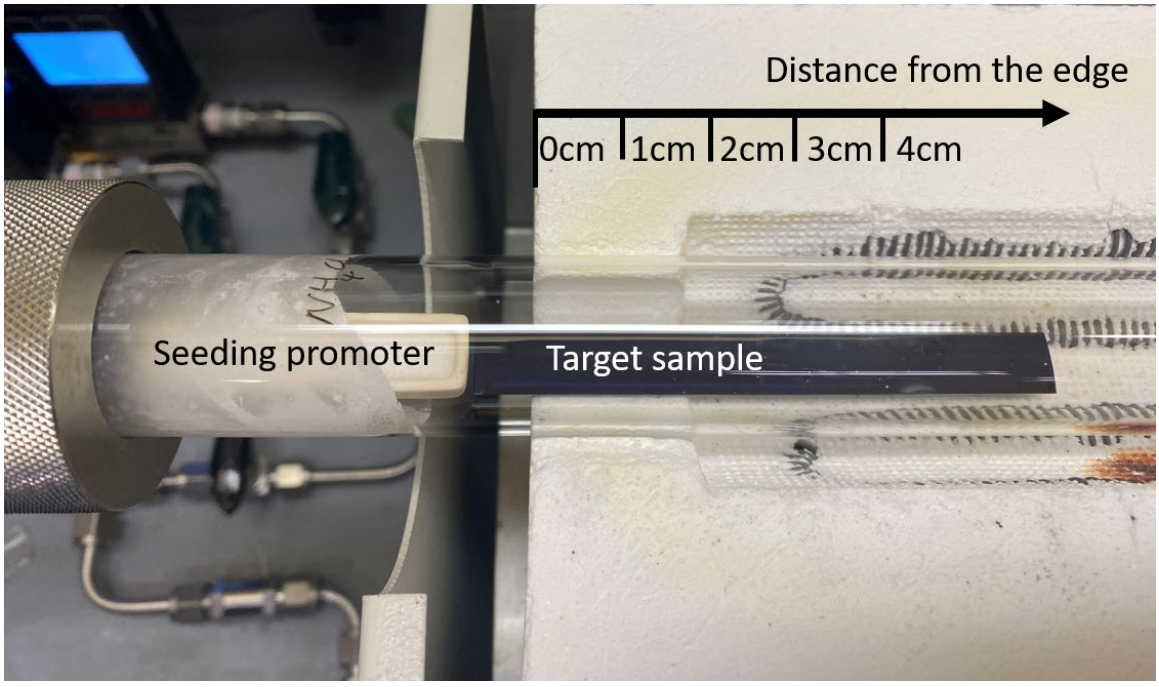


Figure 2.2 The setup of seeding promoter, laterally placed target sample inside the 1-inch MOCVD system. Left side is the upstream side.

Table 2.1 Temperature distribution as a function of the distance from the edge of the furnace.

| **Distance (cm)** | **0** | **1** | **2** | **3** | **Center of the furnace** |
|---|---|---|---|---|---|
| **Temperature (°C)** | 222 | 304 | 467 | 566 | 763 |

The seeding promoter is placed in a crucible at the upstream of the furnace. When gas flows from the top of the crucible, it would carry a small amount of the seeding promoters into the reaction region. By changing the position of the seeding promoter crucible, we can control the temperature of the crucible to manipulate the seeding promoter's sublimation rate and change its distance from the target sample. In this way, we can finely control the effect of the seeding promoter over the growth process.

During the growth process, a rectangular $SiO_2$/Si piece (~1 cm × 5 cm) would be placed laterally inside the tube furnace with one short edge at the end of the tube furnace on the upstream side (Fig. 2.2). The temperature changes as a function of distance and it is measured as what is shown in Table 2.1. During the growth, the crystal size and shape would change dramatically due to different temperature and different distance from the seeding promoter. This would help us to quickly find the most suitable growth condition for the 2D TMD materials.

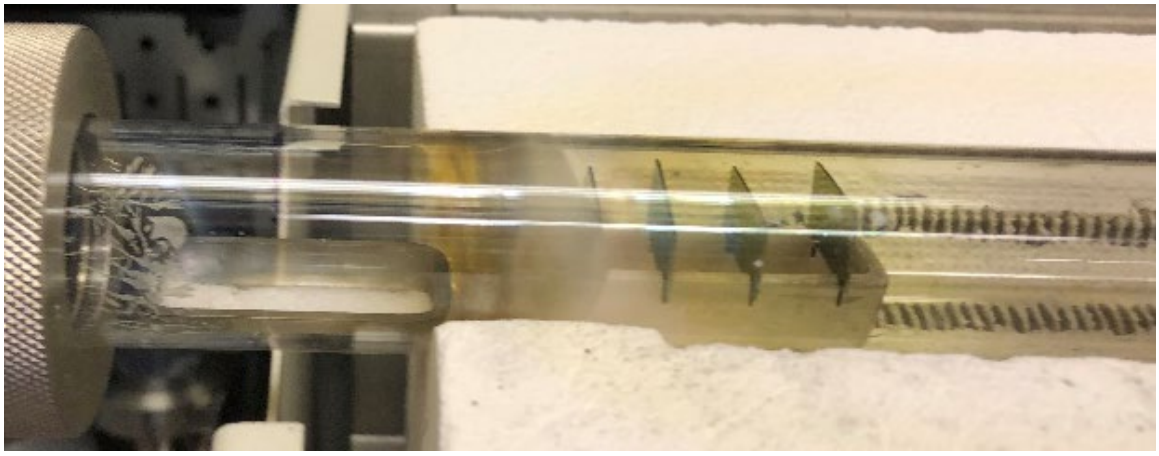

Figure 2.3 Vertical growth of monolayer $MoS_2$ film. Five $SiO_2$/Si pieces are placed vertically on an $Al_2O_3$ crucible (with trenches). Each piece is at a relatively stable

temperature during the whole growing process. The yellow color on the quartz tube comes from the coated $MoS_2$.

After the growth condition is confirmed, vertical growth can be done to improve the material uniformity. In this case, we cut trenches on an $Al_2O_3$ crucible (Figure 2.3), and place the $SiO_2$/Si pieces (~1 cm × 1.25 cm) vertically in the trenches. Based on the temperature-distance relationship we get in Table 2.1, the crucible is placed in the corresponded position to get the appropriate growth temperature for $MoS_2$ growth. Similar method is also used in the 8-inch MOCVD system, where we also first find the most suitable growth condition and then realize vertical, more uniform material growth as the second step.

# 2.2 Low-temperature MOCVD Synthesis of 2D Materials

As mentioned in chapter 1, the synthesis of TMD below 400 ºC is extremely important for BEOL integration. More importantly, alkali metal salts are fatal for silicon devices and thus need to be removed from the growth systems. This adds to the difficulties in realizing high quality growth and large material grain size. In this section, we will focus on the flow rate control and the selection of seeding promoters and their effect on the growth temperature and grain size of the synthesized TMD materials.

## 2.2.1 Seeding promotors

In CVD synthesis of 2D TMD materials, alkali metal salts are usually considered essential for seeding and realizing micrometer scale grain size [13]. It is believed that the alkali metal ions would help to fix the metal and chalcogenide precursors onto the target substrate and accelerate lateral growth. Many kinds of alkali metal salts have been investigated and applied to CVD and MOCVD synthesis in the past few decades as seeding promoter [34], which includes but not limited to sodium chloride, potassium chloride, potassium iodide, and perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt (PTAS).

By using sodium chloride as the seeding promoter in our one-inch MOCVD system, we could realize the growth of monolayer $MoS_2$ thin film with grain size of around 10 μm after an 18 hours growth. The optimized growth temperature in this case is only around 350-400 ºC, which is far below the limitation of BEOL integration. Figure 2.4 show the $MoS_2$ synthesized by lateral growth method. The $MoS_2$ grain size decreases in the higher temperature regions on the lateral growth sample as higher temperature accelerates the decomposition of precursors, which results in higher nucleation density.

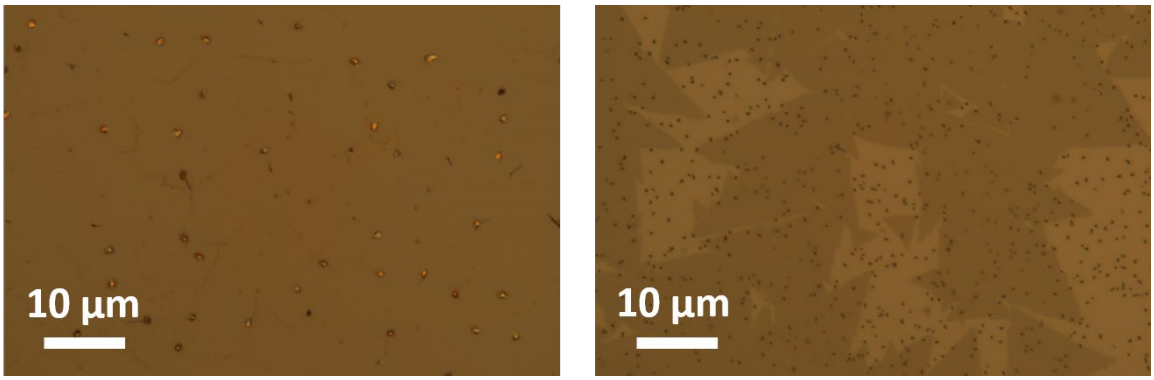


Figure 2.4 Optical micro scope image of the $MoS_2$ synthesized at different temperatures after 18 hours growth with NaCl as the seeding promoter. The left one is monolayer $MoS_2$ film grown at ~ 400 ºC, where grain size of around 10 μm can be observed. The white particles are NaCl residuals. The one on the right is $MoS_2$ flakes grown at ~350 ºC. The flake size would be slightly larger due to lower nucleation density. The black particles are mainly $MoO_x$ introduced by incomplete reaction of the exceeding molybdenum precursors at lower temperature region.

However, the sodium salt causes sodium contamination to the $MoS_2$ sample and the substrate, which would lead to fatal damage to the silicon circuits in the case of BEOL integration. Accordingly, we need a CMOS compatible seeding promoter to ensure *in situ* growth of $MoS_2$ on BEOL silicon wafers in the 8-inch system.

Among all the inorganic salts, ammonium halogens are considered among the most promising candidates as they decompose into gases when heated up and eventually flow out of the system without leaving any residual on the target sample. The halogen ions can be adsorbed onto the sample surface during the growth, which is helpful for the seeding process. Ammonium chloride is first applied as the seeding promoter in this work to replace the previous sodium chloride. Effective growth is observed from 350 ºC to 600 ºC. Yet the grain size is only around few hundreds of nanometers to few micrometers (Figure 2.5),

which is much smaller with the absence of the sodium ion. This can be attributed to the low melting point of ammonium salts. The halogen ions do not stay long enough on the sample surface to further increase the material grain size. Ammonium iodide has also been tried as seeding promoter, demonstrating similar trend (Figure 2.6) as the ammonium chloride. In this case the growth temperature is lower (~ 200 ºC) due to the lower reaction barrier required when iodine ions are presented [35]. This is therefore a useful method to realize lower growth temperature.

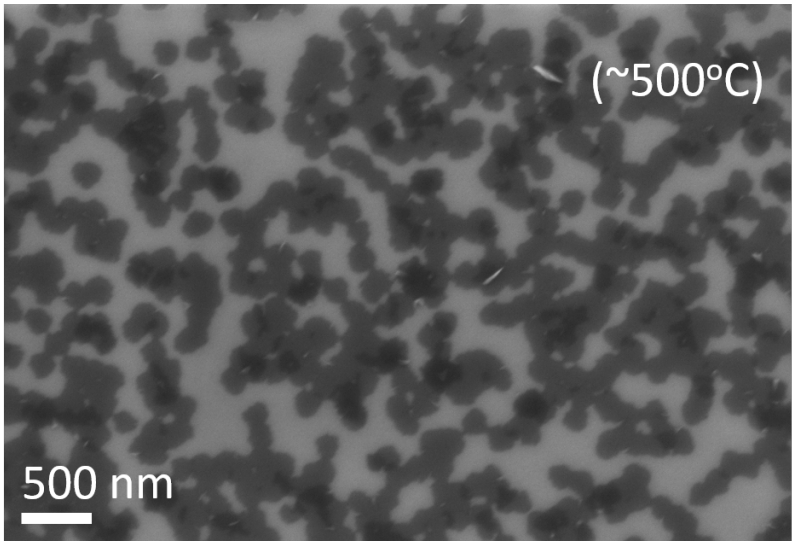

Figure 2.5 SEM image of $MoS_2$ flakes grown with $NH_4Cl$ as the seeding promoter.

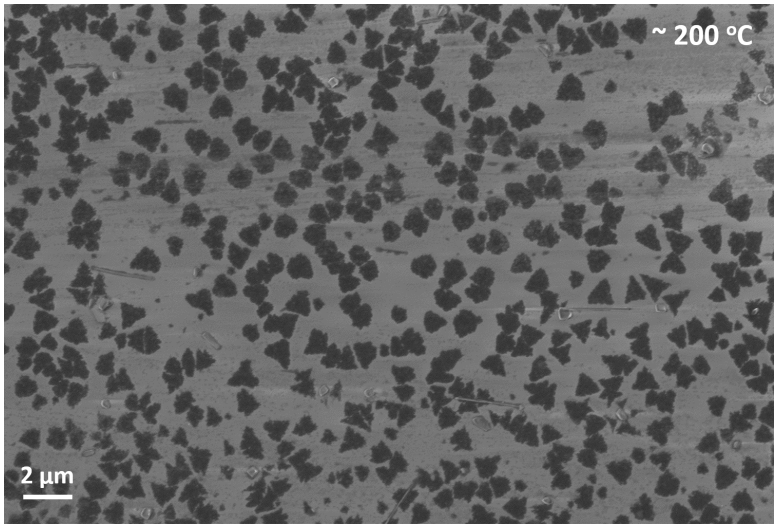

Figure 2.6 SEM image of $MoS_2$ flakes gown with $NH_4I$ as the seeding promoter.

Organic materials could also function as seeding promoters. In 2014, Ling et. al., demonstrated several inorganic and organic seeding promoters for CVD synthesis for $MoS_2$ [25]. Among them, crystal violet (CV) shows the largest material grain size under the same growth condition. Since crystal violet has an organic cation part ($C_{25}N_3H_{30}^+$) and $Cl^-$ as its anion, (not like PTAS that has potassium ions,) it will not leave any movable ions on the sample surface and would eventually evaporate. This makes the MOCVD sample clean and with relatively large grain size. Figure 2.7 shows the $MoS_2$ synthesized with CV as the seeding promoter after 10 hours growth time (the growth was interrupted to prevent the $MoS_2$ flakes from merging together). Grain size of around 10 μm is observed, which is comparable to the case when sodium chloride is used, while the optimum growth temperature is still around 350 ºC - 400 ºC. The shape of some of the $MoS_2$ flakes are not perfectly triangle or hexagonal, meaning the ratio of molybdenum and sulfur atoms inside these $MoS_2$ flakes is not close to (and may be far from) 1:2. Yet, this is only the first attempt of using CV as the seeding promoter. With carefully tuned flow rate, monolayer $MoS_2$ with larger grain size, better shape and uniformity is expected to be grown.

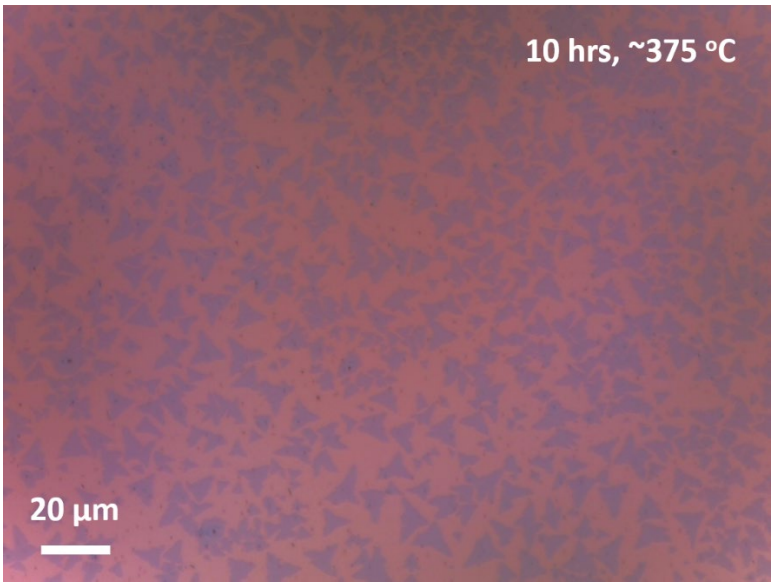


Figure 2.7 Optical microscope image of $MoS_2$ synthesized with CV as the seeding promoter.

Moreover, by using both $NH_4I$ and CV as the seeding promoter, we could obtain large grain size $MoS_2$ (~ 10μm) at even lower temperature. Figure 2.8 shows the $MoS_2$ grown at

around 200 ºC, which not only have large grain size, but also clean surface, showing this method would be very promising for wafer-scale growth and be silicon BEOL compatible.

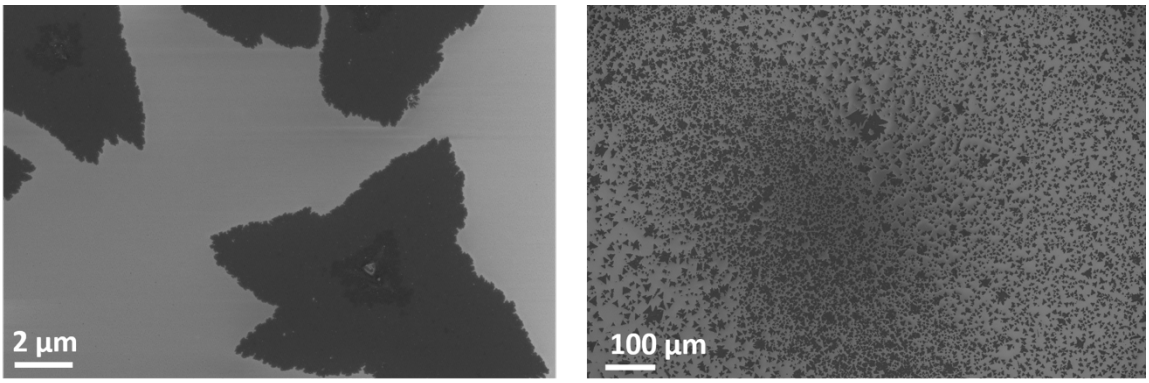


Figure 2.8 SEM image of $MoS_2$ synthesized with both CV and $NH_4I$ as the seeding promoter at ~200 ºC for 10 hours.

## 2.2.2 Flow rate control

The flow rate of the precursors and the ratio between them are important for the successful synthesis of the 2D TMD materials. In this section, we will study these parameters taking the synthesis of $MoS_2$ in the 1-inch MOCVD system as an example. Ammonium Chloride is used as the seeding promoter.

The starting point of the flow rate can be roughly determined by the previous growth condition when sodium chloride is used as the seeding promoter. In that case the flow rate for molybdenum, sulfur precursors and the carrier gas (Ar) are 0.07 sccm, 1.3 sccm, and 100 sccm respectively. After 12 hours of growth time and a growth temperature of around 500 ºC, $MoS_2$ flakes with grain size around 400 nm can be observed (Figure 2.9). When fixing the flow rate of molybdenum hexacarbonyl, the increase of the sulfur precursor flow rate from 1.3 sccm to 1.8 sccm increases the nucleation density as well as the grain size, as is shown in Figure 2.10. The flow rate of the molybdenum precursor tends to be more sensitive to the $MoS_2$ growth. When fixing the flow rate of the sulfur precursor at 1.3 sccm, the increase of the molybdenum precursor flow rate from 0.07 sccm to 1 sccm would only slightly increase the nucleation density of the synthesized $MoS_2$. However, if the molybdenum precursor is decreased to 0.04 sccm, no $MoS_2$ growth can be observed due to the lower molybdenum precursor density.

These trends are actually quite universal for the synthesis of $MoS_2$ using MOCVD method, regardless of which type of precursor is used and what size of the reaction chamber would be. Accordingly, these guidelines are very helpful for the synthesis of 2D materials, at larger scale, say 8-inch.

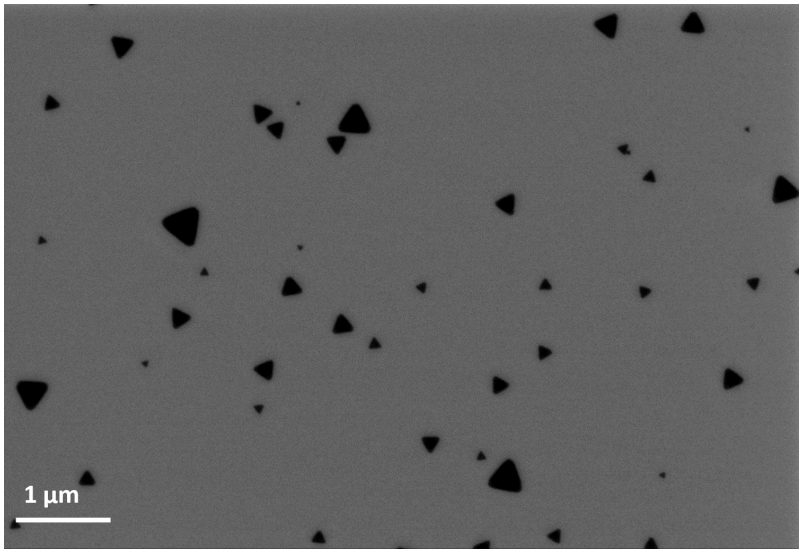


Figure 2.9 $MoS_2$ flakes grown at 500 ºC for 12 hours with $NH_4Cl$ as the seeding promoter. Molybdenum precursor flow rate is set as 0.07 sccm. Sulfur precursor flow rate is set as 1.3 sccm.

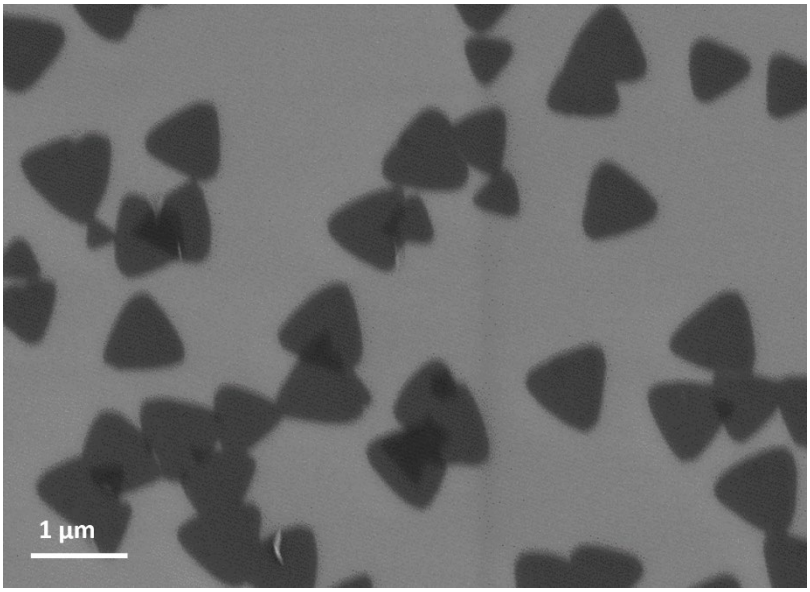


Figure 2.10 $MoS_2$ flakes grown at 500 ºC for 12 hours with $NH_4Cl$ as the seeding promoter. Molybdenum precursor flow rate is set as 0.07 sccm. Sulfur precursor flow rate is increased to 1.8 sccm.

# 2.3 8-inch MOCVD Synthesis of 2D Materials

Although the 1-inch MOCVD system provided important understanding for the MOCVD synthesis, things could be much different when it comes to larger scale. In this section, we would focus on the synthesis of $MoS_2$ at wafer scale, i.e. the MOCVD synthesis of $MoS_2$ on 8-inch $SiO_2$/Si wafers. We will start from the 1-inch MOCVD system to design the setup of the 8-inch MOCVD system, realizing the synthesis of monolayer MoS2 thin film with the large system and discuss the possible improvements that could be done in the near future.

## 2.3.1 System design

In order to grow 2D materials on an 8-inch wafer, we bought a 10-inch outer diameter (OD), double temperature zones hot wall tube furnace, which would have enough space for the gas flow even if there's an 8-inch wafer placed inside vertically. Due to the extremely-large volume of the furnace and the toxicity of the precursors and reaction products, we also designed and build an exhaustive enclosure cabinet to contain the MOCVD system. A powerful dry pump (Edwards iGx 600M model) is used to achieve the vacuum condition for the 2D material growth. An overlook of the 8-inch MOCVD system is shown in Figure 2.11.

The general structure of the 8-inch MOCVD system is similar as the 1-inch MOCVD system. However, several differences should be noticed due to the extremely large volume of the reaction chamber:

First, the temperature gradient in the reaction chamber is much smaller than in the 1-inch tube furnace. Instead of having ~500 $^{o}$C temperature change within around 4 cm, the large diameter of the 10-inch furnace makes the power dissipation much stronger and thus the temperature changes with a lateral gradient of 20-40 $^{o}$C/inch. This requires: 1) to have the material grown in the center region of one temperature zone, otherwise the temperature would vary across the diameter direction. 2) to use thermal blocks at the two ends of the furnace to prevent potential damage to the o-rings and fringes, and ensure relatively stable temperature distribution inside the furnace.

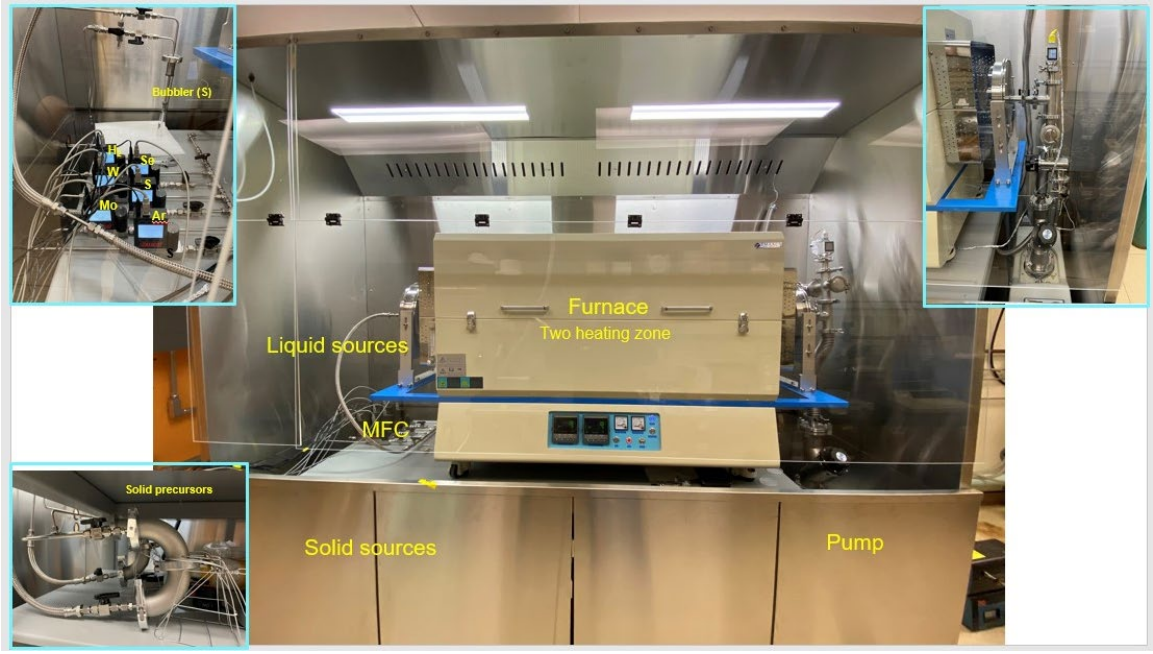


Figure 2.11 An overlook of the 8-inch MOCVD system.

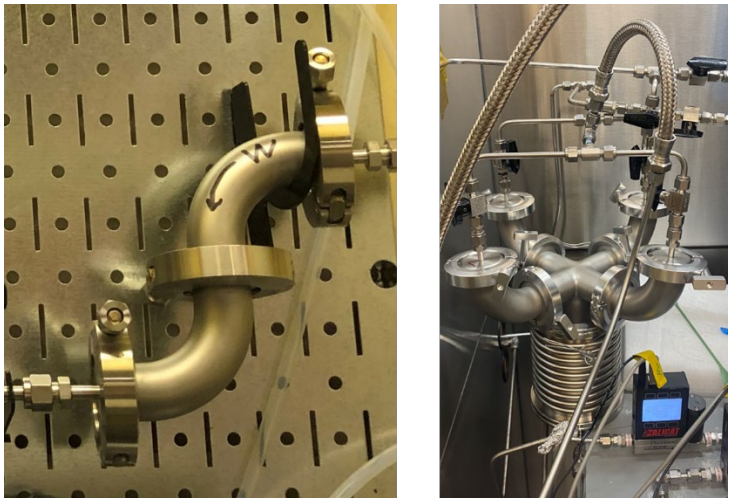

Figure 2.12 Changes in the solid bubbler. (Left) Solid bubbler for the 1-inch MOCVD system (size: NW25). (Right) Four paralleled solid bubbler for the 8-inch MOCVD system. The size for each bubbler is NW40.

Second, the flow rate of precursors required would dramatically increase in the 8-inch MOCVD system. Since the diameter is increased by 10 times, and the length of the tube is also increase by two times, the volume of precursors would also increase by around 200 times to make the localized precursor concentration to be relatively the same. This could be easily realized for the liquid precursor, as the saturation pressure is fixed, it is enough

to increase the flow rate in order to satisfy the requirement. However, since the sublimation of the solid precursor is slow, just increasing the flow rate won't be very efficient, as the concentration of $Mo(CO)_6$ would drop at higher flow rate due to the dwell time of argon is shorter than what is needed to reach saturation pressure. Accordingly, we are using 4 parallel solid bubblers, each of which has a diameter around 2 times larger than the one for the 1-inch system. This provides enough molybdenum atoms at a higher flow rate, even if the saturation pressure cannot be realized.

### 2.3.2 Uniformity of wafer-scale 2D materials

To realize highly uniform 2D material monolayer thin film on 8-inch wafers requires precise control over the flow rate, temperature distribution as well as seeding. Several attempts have been made to get a highly uniformed monolayer $MoS_2$ thin film grown on top of the $SiO_2$/Si wafer in the 8-inch MOCVD system. The images of the as grown sample and Raman spectra taken at random regions on the 8-inch sample are shown in Figure 2.13 and Figure 2.14. Ammonium chloride is used in these cases as the seeding promoter.

First, two 10-inch $Al_2O_3$ porous thermal blocks are placed on the two ends of the 10-inch quartz tube. Instead of simply keeping a stable temperature distribution inside the reaction chamber, they also block the direct gas flow from the gas inlet and cause significant flow turbulence in the left half of the reaction chamber. This helps with the mixing of the precursors. As a result, we could get a uniformly grown $MoS_2$ sample on the $SiO_2$/Si wafer. In some cases, due to the low concentration of molybdenum precursor, extra molybdenum can be introduced by electron beam evaporation. Pure molybdenum with density of 2~3 atoms/10,000 $nm^2$ can be deposited onto the surface of a bare $SiO_2$/Si wafer to function as the nucleation center and the solid precursor of $MoS_2$. During the growth, the MOCVD process is taking place along with a CVD process where molybdenum reacts with the sulfur precursor as well and form $MoS_2$ eventually. This seeding methods is also useful to realize uniform $MoS_2$ film when there's not enough gas type molybdenum precursor. However, the growth temperature is much higher than expected, which is around 625 $^oC$.

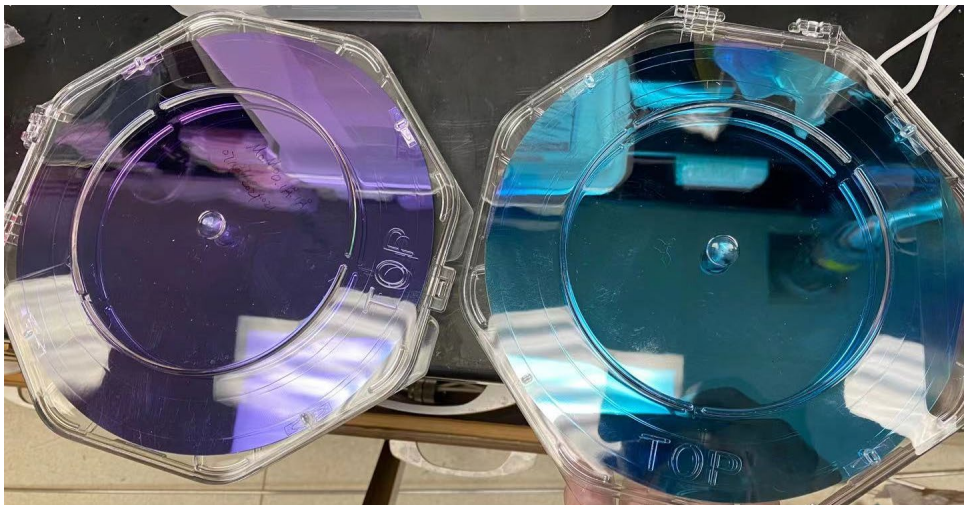


Figure 2.13 (Left) 8-inch bare 300nm $SiO_2$/Si wafer. (Right) 8-inch $MoS_2$ thin film grown on the $SiO_2$/Si wafer. Good uniformity can be roughly estimated based on the uniform color distribution.

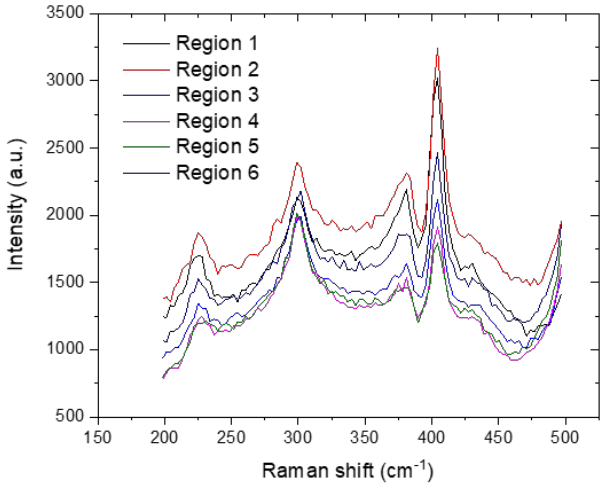


Figure 2.14 Raman spectra taken at different random regions on top of the 8-inch $MoS_2$ sample. Good uniformity can be observed.

## 2.3.3 CMOS compatibility

Conventional CVD and MOCVD methods would requires alkali metal salts to ensure large grain size of the synthesized 2D materials. However, these mobile alkali metal ions would be fatal to silicon devices as they would penetrate the insulting layers, e.g. spacers and gate dielectrics, and cause huge hysteresis in the CMOS devices and severe reliability problems and even device failure. Hence, our 8-inch MOCVD system is targeted to be a CMOS

compatible system without mobile cations. Furthermore, we are also trying to reduce potential contamination to the maximum we can, which means even inert metal atoms that could function as nucleation centers are unfavored in the system.

Based on these concerns, we are using a mixture of ammonium iodide and crystal violet as the seeding promoters. The iodine ions help to reduce the growth temperature significantly, allowing us to have a growth temperature lower than the 400 ºC limit. The crystal violet is a pure organic material which will not cause any ion contamination but help to increase the grain size of the synthesized 2D materials to tens of micrometers. All of these seeding promoters turn into gas form at a temperature higher than 205 ºC. Accordingly, with proper annealing and purging process, we could obtain a CMOS compatible or BEOL compatible wafer scale $MoS_2$ sample what is capable to be applied to ultra-large-scale circuit integration. This technology will be especially useful for future electronics.

## 2.4 Chapter Summary

In this chapter, we discussed the methods to synthesize $MoS_2$ below 400 ºC and at 8-inch wafer scale. Based on the knowledge we get from the one-inch MOCVD system, we successfully designed and set up an 8-inch MOCVD system. By finely tuning the flow rate of the precursors and careful design of the bubbler system, reaction chamber and system vacuum, we could realize uniform 2D material growth in the 8-inch MOCVD system. We also propose a new method to realize CMOS compatible growth of 2D materials, without introducing alkali metal ions that are normally presented in convention CVD or MOCVD samples. We expect these findings to be of significant impact to the future development of large scale 2D material devices and circuits, and also be useful for BEOL integration.

# Chapter 3

# Contact Engineering for Transistors based on 2D Materials

Contact engineering in 2D material transistors has always been a very important research topic. The clean interface of the 2D van de Waals materials improves the intralayer carrier transport property. It also prevents strong Fermi pinning between the 2D material and the contact metals. Moreover, due to the atomic thickness of the 2D materials, it is also difficult to realize efficient substitutional doping in 2D material systems, making it harder to form a good ohmic contact in 2D material devices than in bulk materials. In this chapter, we mostly focus on two different approaches to realize low contact resistance in 2D material systems, the formation of clean van de Waals contacts and the phase transition method.

## 3.1 Van de Waals Contacts

As discussed in section 1.3, instead of forming covalent bonds in the source/drain regions, which is the standard approach in bulk material devices, a clean van de Waals contact could provide stable and lower contact resistance due to the reduced Fermi pinning effect. In this section, we will focus on two different types of contacts, the conventional gold contact and novel metallic carbon nanotube (CNT) contact to discuss the effect of ultra clean interface on contact resistance.

### 3.1.1 Gold contact

As an inert metal, gold does not react with other materials at room temperature, and thus can form pure van de Waals contacts with 2D material layers. This unique property helps gold contacts to get rid of the severe Fermi pinning effect observed in most of the other low work function metals. Although gold has a relatively high work function and consequently higher energy barrier for electron injections, the uniformity from device to device, and between different test cycles is much better than for most of the other metal contacts in 2D material transistors. Here, we studied $MoS_2$ transistors with pure gold contacts and back gate structure to understand the crucial parameters in 2D material transistors. These parameters will be useful for future analysis when different contact material or device structures are used.

The structure of the global back gate $MoS_2$ transistor is shown in Figure 3.1. Starting from highly p-type doped silicon substrate, 285 nm silicon dioxide is grown through thermal oxidation. The heavily doped silicon wafer will be functioning as the global back gate in the $MoS_2$ transistors that are later fabricated. Monolayer MOCVD synthesized $MoS_2$ thin film is then coated with polystyrene and transferred onto the target substrate with the help of DI water. The polystyrene protection layer is removed by immerse in toluene for 40 minutes. Electron beam lithography is used to define the channel and active regions, which is covered by PMMA A8 950k after the development process. The exposed $MoS_2$ is etched away by oxygen plasma to form electrical isolation between devices. Another electron beam lithography is performed to expose the source/drain region, followed by the electron beam evaporation process to deposit 75 nm of Au. Lift-off is done to eventually form the source/drain patterns. The device is measured in a vacuum probe station with a semiconductor parameter analyzer (Agilent B1500A).

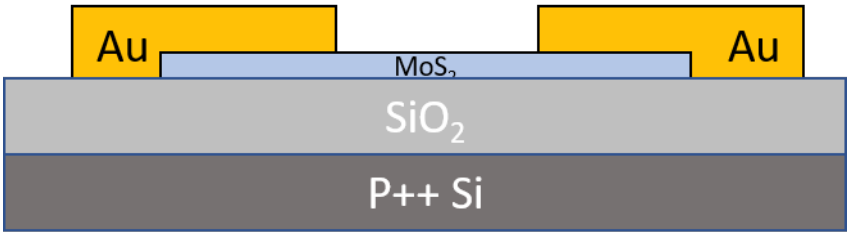


Figure 3.1 Schematics of the back gate $MoS_2$ transistor with gold contacts.

Figures 3.2 and 3.3 show the transfer characteristics and output characteristics of the back gated $MoS_2$ transistor with 1 µm channel length, under different drain and gate bias. Normalized on-state current of around 10 µA/µm can be measured in these devices, showing relatively good channel conductivity. This transistor also possesses on/off current ratio of around seven orders of magnitude, which demonstrates its good property as an electrical switch. Good linearity can also be observed from the output characteristics due to the clean van de Waals interface at the gold/$MoS_2$ contact.

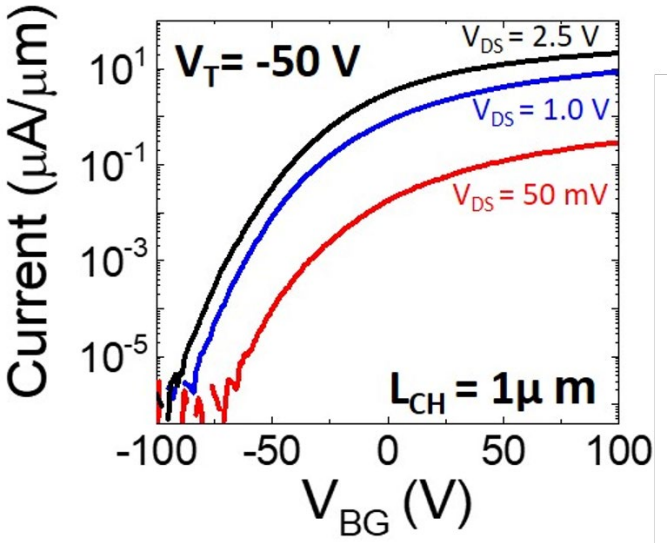


Figure 3.2 Transfer characteristics of the back gated $MoS_2$ transistor with 1 µm channel length.

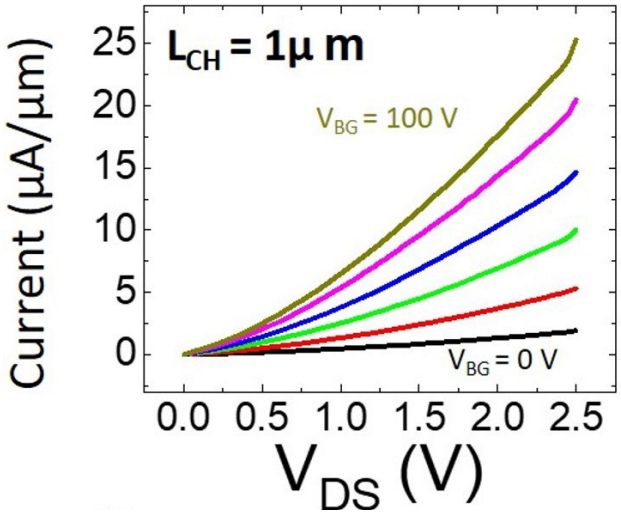


Figure 3.3 Output characteristics of the back gated $MoS_2$ transistor with 1 µm channel length.

For transistors with shorter channel length, higher on-state current can be observed due to the reduced channel resistance. Figure 3.4 shows the transfer characteristics of a 200 nm channel length transistor with the same structure. Higher on-current density can be observed without any degradation in the on/off current ratio. The threshold voltage also remains at around -50V since they are fabricated on the same substrate and are from the same piece of $MoS_2$ sample. Figure 3.5 illustrates the on-state resistance of transistors with different channel length. By extrapolating the data, we could get the on-state resistance when the channel length is approaching zero, which represents two times of the contact resistance in these $MoS_2$ transistors based on gold contacts. The extracted contact resistance is around 4.9 kΩ·μm, which is the normal value for gold contacts in $MoS_2$ transistors. We can also extract the sheet resistance of the MOCVD sample at the on-state to be ~15 kΩ/□. This also matches well with the on-state resistance data from the other MOCVD $MoS_2$ samples that we grow in the past few years.

Based on the result above, more information can be extracted. By using the "Y-function method" [36], we can calculate the carrier mobility inside the $MoS_2$ channel from the linear region data in Figure 4.2 ($V_{DS}$ = 50 mV), which is 3.5 $cm^2/V \cdot s$, and extract the contact resistance between the Au/$MoS_2$ contact to be around 5.0 kΩ·μm. This contact resistance value matches well with the data that we get from the transmission line model (TLM) in figure 3.5.

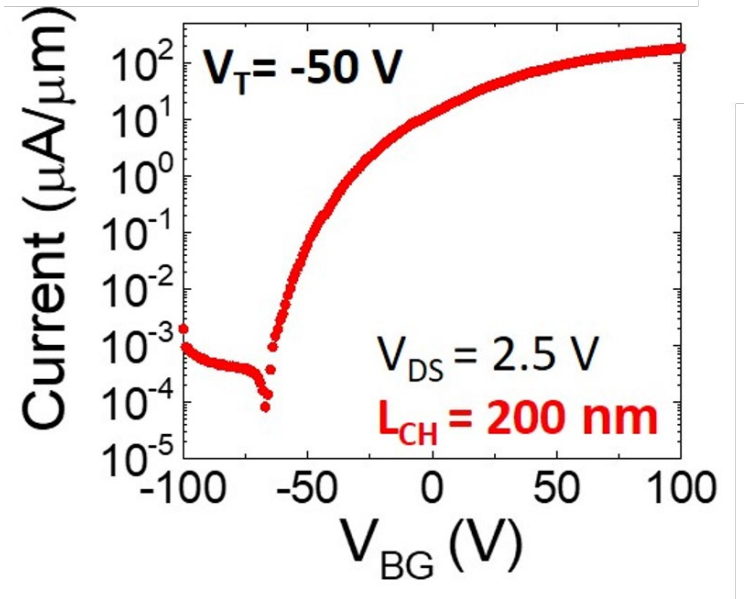


Figure 3.4 Transfer characteristics of a 200 nm channel length back gated $MoS_2$ transistor.

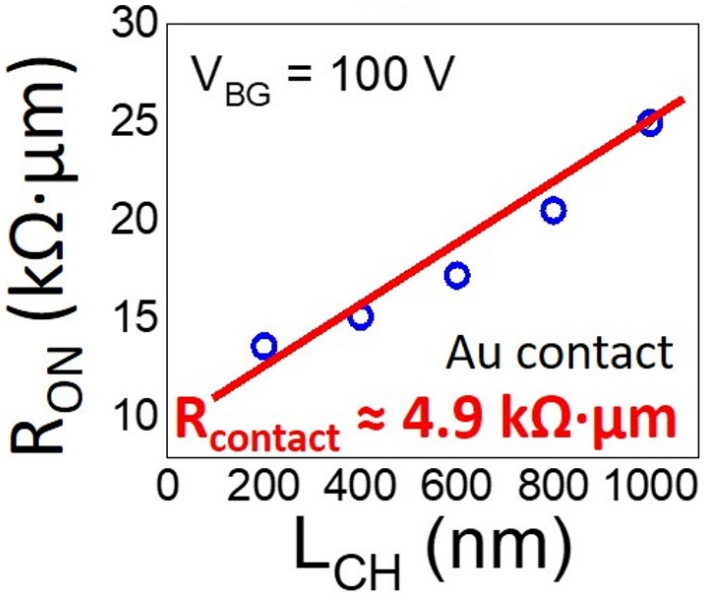


Figure 3.5 Extraction of contact resistance and the on-state $MoS_2$ sheet resistance of the MOCVD grown $MoS_2$ by TLM structure.

### 3.1.2 Metallic CNT contact

Apart from gold contacts, the contacts formed by $MoS_2$ and other 2D or 1D metallic materials are expected to also be clean van de Waals contact and should have good contact quality. Previous research has demonstrated the contacts formed by graphene on $MoS_2$, which shows the lowest contact resistance value among all the contacts when phase transition or doping methods are not applied. It should have similar effect when metallic carbon nanotubes (CNTs) are used as the contact material. There are also no dangling bonds on the outer wall of the CNTs, and the transfer process is also less likely to introduce defects and covalent bonds compared with the normal physical vapor deposition methods, e.g. electron beam evaporation and sputtering, which would have high energy metal atoms to be deposited onto the vulnerable surface of the 2D materials. Accordingly, the CNT contacts should also provide low contact resistance when contacting $MoS_2$.

Here, we made the first experimental demonstration of top gated monolayer $MoS_2$ transistors based on CNT nanoscale contacts. Figure 3.6 shows the schematic of the transistors. The MOCVD-grown monolayer $MoS_2$ film between two CNT bundles would act as the channel material once it is transferred on top of the CNT bundles. For the convenience of electrical measurement, we are also using Cr/Au assistive electrodes to connect the CNT bundles source/drain contacts with the measurement setups. These Cr/Au

assistive interconnects are not in touch with the $MoS_2$ channel and can be replaced by in-plane CNT bundles or vertical metal-filled via in larger scale integrated circuits. In these devices, the channel lengths are defined by the distance between two adjacent CNT bundles and is typically around or larger than 180 nm (Figure 3.7), while the channel width is designed as 2 μm by electron beam lithography.

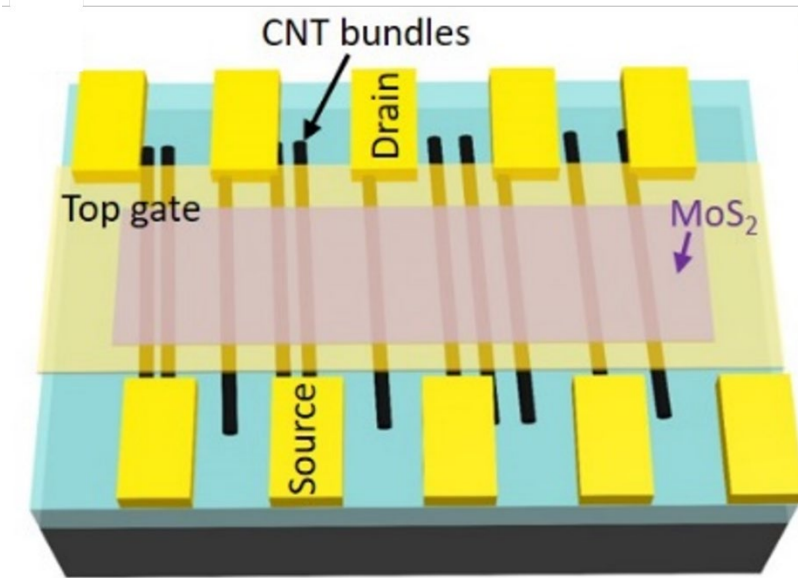


Figure 3.6 Schematic of top gate $MoS_2$ transistors with CNT bundles as the source/drain contacts.

The fabrication of the $MoS_2$ transistors with CNT bundle contacts starts from 285 nm $SiO_2$/Si substrates. CNT bundles are transferred and aligned on top of the substrate by soft-lock drawing method [37]. MOCVD-grown monolayer $MoS_2$ coated with polystyrene is transferred onto the substrates with DI water and later cleaned up with toluene. Electron beam lithography and reactive ion etching (RIE) with oxygen plasma were used to define the device area of interest by removing other additional CNT bundles and $MoS_2$ on the substrates. Electron beam lithography and e-beam evaporation followed by a lift-off process were used to pattern and deposit 0.2 nm Cr/75 nm Au stacks as the assistive electrical contacts to the CNT bundles. The sample is annealed at 250 ºC for 1 hour in $N_2$ atmosphere at 0.2 Torr to enhance the contacts and remove moistures. 50 nm $Al_2O_3$ dielectric layer is then deposited onto the surface with atomic layer deposition (ALD) method. Subsequently, EBL, e-beam evaporation and lift-off process were carried out to

pattern and deposit 0.2 nm Cr/75 nm Au stack as the top-gate electrode. The electrical measurements of top-gated $MoS_2$ FETs were carried out in atmosphere and room temperature using a semiconductor parameter analyzer (Agilent 4155C).

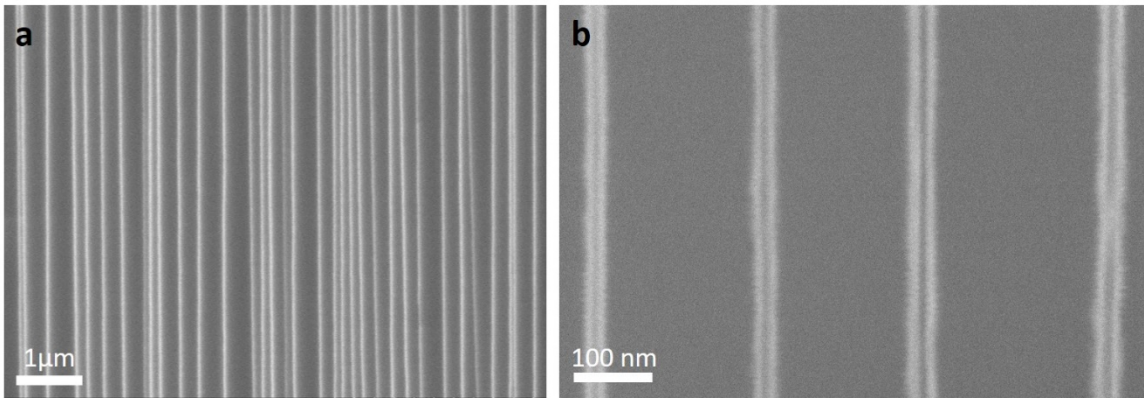

Figure 3.7 SEM images of the area where the $MoS_2$ transistor array can be fabricated. a, SEM image of the CNT bundles where $MoS_2$ transistor array can be fabricated. b, High-resolution SEM image of the CNT bundles for source/drain contacts, showing an average contact length ($L_c$) of 10-20 nm and a typical channel length (the distance between two adjacent CNT bundles) of around 180 nm.

From our observation, the adjacent CNT bundles usually have similar diameters, as shown in Figure 3.7. Hence, we can roughly estimate the contact resistance of the CNT/Au contact as well as the resistance of the CNT bundle by assuming the CNT bundles in a local region are of the similar size.

As shown in Figure 3.8, we can model the two branches into the following resistances:

1) $R_{probe}$ includes the resistance of probes, probe/Au contacts, the wire resistance of the Au assistive contact and other parasitic resistance related to the wires connected to the probes.

2) $R_{c,CNT}$ represents the contact resistance of the CNT contacts and the Au assistive contacts.

3) $R_{CNT}$ stands for the resistance of the metallic CNT bundle.

4) $R_{c,MoS2}$ corresponds to the contact resistance of the CNT contacts and the $MoS_2$ channel.

5) $R_{ON}$ is the on-state sheet resistance of the $MoS_2$ channel between the source/drain CNT bundles.

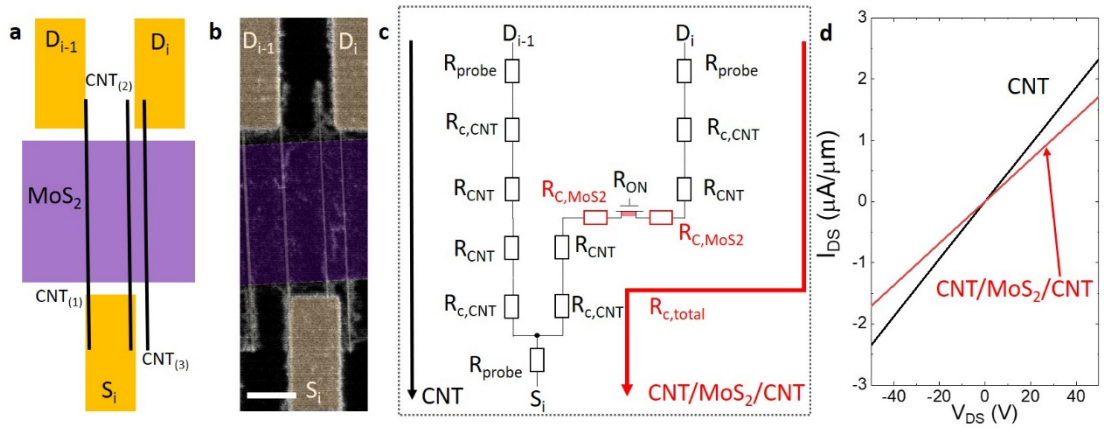


Figure 3.8 Contact resistance extraction from top-gated $MoS_2$ transistors with CNT bundle contacts. a, Schematic of one $MoS_2$ transistor with CNT bundle contacts (right) and one adjacent CNT bundle sharing the same source terminal (left). b, SEM image of the two devices before the top gate and gate dielectric were deposited. Scale bar: 500 nm. c, Schematic of the circuits formed by these two branches at the on-state. d, Measured on-state output characteristics of the two branches.

From the on-state output characteristics of the CNT branch and $MoS_2$ branch:

$$R_{CNT,total} = 2\left(R_{probe} + R_{c,CNT} + R_{CNT}/2\right) = 2 * 10.8\ k\Omega$$

$$R_{MoS2,total} = 2(R_{probe} + R_{c,CNT} + R_{CNT}/2 + R_{c,MoS2} + R_{ON}/2) = 2 * 14.6\ k\Omega$$

Subtracting the $R_{CNT,total}$ from $R_{MoS2,total}$:

$$R_{c,MoS2} + R_{ON}/2 = 3.8\ k\Omega$$

From Figure 3.8B, the $MoS_2$ transistor has a channel length of 184 nm, with a contact length (the width of the CNT bundle) of around 18 nm.

Using the sheet resistance extracted before from the transistors with gold contacts:

$$R_{ON}/2 = 1.4\ k\Omega$$

Actually, in order to assume that the on-state sheet resistance of the $MoS_2$ channel are the same, not only did we use the $MoS_2$ sample from the same batch of MOCVD synthesis in the fabrication of devices with CNT bundle and pure gold contacts. We can also calculate the carrier density in the back-gated $MoS_2$ transistor with Au contacts and the top-gated $MoS_2$ transistor with CNT bundle contacts. For the carrier density estimation, we can use the following formula:

$$n = C_{ox}(V_{BG} - V_T)/q,$$

The carrier density in the back-gated transistor is: $n = 1.3\times10^{13}$ $cm^{-3}$, while in the top-gate cases: $n = 1.9\times10^{13}$ $cm^{-3}$, which shows a similar carrier density level.

Accordingly, the contact resistance between the CNT bundles and the $MoS_2$ would be:

$$R_{c,MoS2} = 3.8\text{-}1.4 = 2.4\ k\Omega\cdot\mu m$$

Several devices are measured to further confirm the contact resistance between CNT bundles and the $MoS_2$ channel. Table 3.1 listed the other six devices we fabricated with critical parameters. The extracted contact resistances are all around 2.2 kΩ·μm, with the lowest one reaching 1.6 kΩ·μm, demonstrating much lower value than when gold contacts are used. These values represent the state-of-the-art performance in $MoS_2$ transistors when no high-vacuum deposition system or phase transition/doping methods are used. Figure 3.9 also listed the SEM images of the corresponded devices in Table 3.1.

Table 3.1 Contact resistance extracted from top-gated $MoS_2$ transistors with CNT bundle contacts.

| Device | 1# | 2# | 3# | 4# | 5# | 6# |
|---|---|---|---|---|---|---|
| $W_c$ (nm) | 15 | 25 | 15 | 8 | 10 | 20 |
| $R_{MoS2,total}$ (kΩ) | 34.0 | 27.8 | 68 | 28.8 | 29.2 | 35.3 |
| $R_{CNT,total}$ (kΩ) | 21.8 | 19.4 | 60.8 | 21.2 | 18 | 22.6 |
| $R_{c,MoS2}+R_{ON}/2$ (kΩ) | 6.1 | 4.2 | 3.6 | 3.8 | 5.6 | 6.4 |
| $L_{ch}$ (nm) | 609 | 328 | 187 | 187 | 406 | 547 |
| $R_{ON}/2$ (kΩ) | 4.50 | 2.64 | 1.41 | 1.41 | 3.05 | 4.11 |
| $R_{c,MoS2}$ (kΩ·μm) | 1.6 | 1.6 | 2.2 | 2.4 | 2.5 | 2.3 |

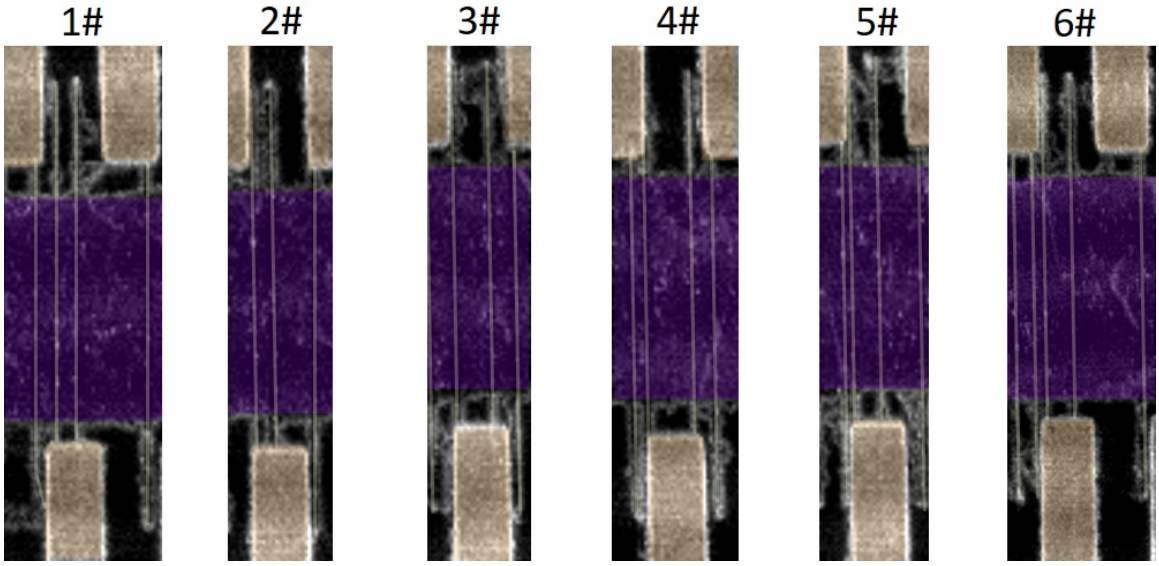

Figure 3.9 False color SEM images of the $MoS_2$ transistors with an adjacent CNT bundle sharing the source terminal. The width of the Au assistive electrodes is 500 nm. The purple regions are $MoS_2$ ribbons. The white lines are CNT bundles. The orange regions are Au assistive contacts.

# 3.2 Phase Transition and Doping

Phase transition and doping are useful methods to realize ohmic contact in 2D material devices. By changing the source/drain region from semiconducting to conducting, it is possible to effectively reduce the Schottky barrier and obtain quasi-zero electron barriers between the metal contacts and the source/drain materials. In this section, we discuss two different approaches, namely, the 2H/1T phase transition induced by lithium ions and the wave function hybridization obtained by bismuth coating.

## 3.2.1 2H/1T phase transition

The phase transition is a very powerful approach to change the electrical properties of the source/drain regions in 2D material transistors to reduce the contact resistance. In our study, we exposed the source/drain region of $MoS_2$ transistors to n-butyllithium solution for around seven hours, while keeping the channel region covered with PMMA A4 950k photo resist. The lithium ions inside the n-butyllithium solution have high enough energy to change the 2H phase semiconducting $MoS_2$ to 1T phase, which is in metallic form [38].

After the phase transition, we rinse the sample in hexane to remove the n-butyllithium residue and left the sample to dry up by itself. The aforementioned phase transition process is done in a nitrogen glovebox that has oxygen and moisture density lower than 2%.

After the sample is dried, we deposit 75 nm Au to form the contact to the 1T phase source/drain followed by a lift-off process. The sample is then measured under vacuum condition. A significant current increase of more than one order of magnitude compared with the 2H phase source/drain $MoS_2$ transistors with same device structure is observed in these samples.

Figure 3.10 shows the transfer characteristics of the back gated $MoS_2$ transistors when phase transition methods are used and not used. A large difference can be observed in terms of current density under the same gate voltage, demonstrating the effect of phase transition in source/drain region on device performance.

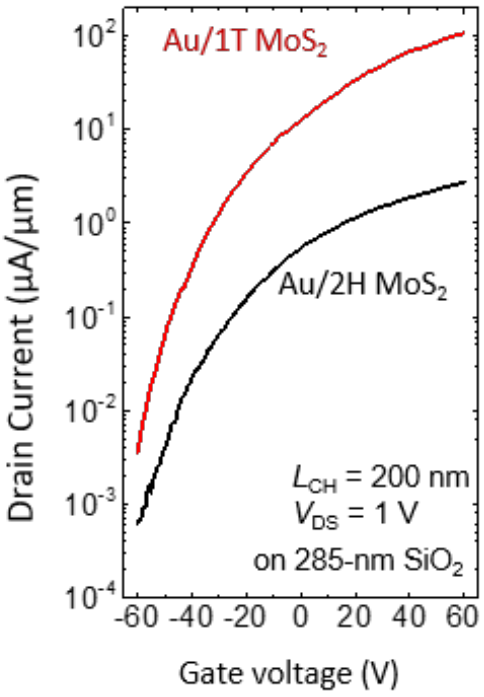


Figure 3.10 Transfer characteristics of back gate $MoS_2$ transistors with and without phase transition in source/drain regions.

Further measurements (Figure 3.11) also show the lithium phase transition method could reproducibly provide contact resistance of around 2 kΩ·μm with gold contacts, which is significantly lower than the cases when no phase transition is applied.

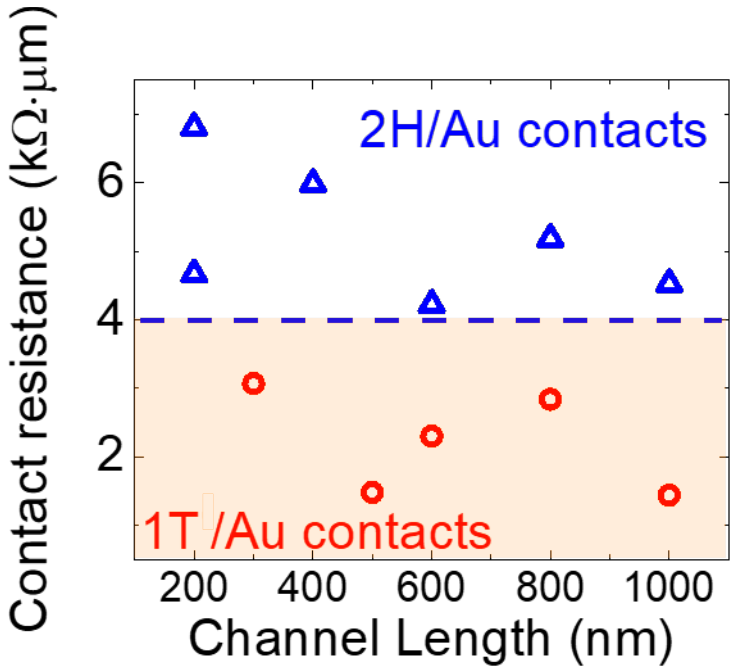


Figure 3.11 Benchmark of contact resistances in back gate $MoS_2$ transistors with and without phase transition in the source/drain regions under different channel lengths.

### 3.2.2 Bismuth contact

As a semi-metal, bismuth forms a crystallized structure on top of the $MoS_2$ and induces high electron density in the 2D material layer underneath. Previous research [39] shows that, due to wavefunction hybridization, the electron barrier between the bismuth electrode and the heavily doped $MoS_2$ underneath is almost zero, which ensures ohmic contact in the source/drain region of the $MoS_2$ transistors.

In this work, bismuth deposition in a thermal evaporation system was studied as contact metal to $MoS_2$ transistors. The transistor we fabricated has a global back gated structure similar to the schematic in Figure 3.1, which consists of a heavily p-type doped silicon substrate and 10 nm of PECVD grown $SiN_x$ back-gate dielectric. $MoS_2$ was transferred on top of the $SiN_x$ with polystyrene as the protection layer that was later removed by toluene. Mesa etch was done with oxygen plasma to define the channel region with 2 μm in width. PMMA A4 950k was used as the photo resist which covers the channel regions with a length ranging from 100 nm to 1 μm. Figure 3.12 and 3.13 shows the transfer and output characteristics of the $MoS_2$ transistors with 20 nm/ 30 nm Bi/Au contact.

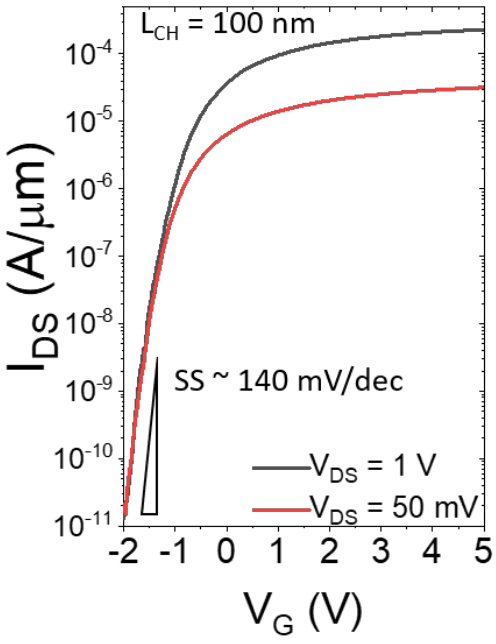


Figure 3.12 Transfer characteristics of the $MoS_2$ transistor with 10 nm $SiN_x$ back gate dielectric and Bi/Au source/drain contacts.

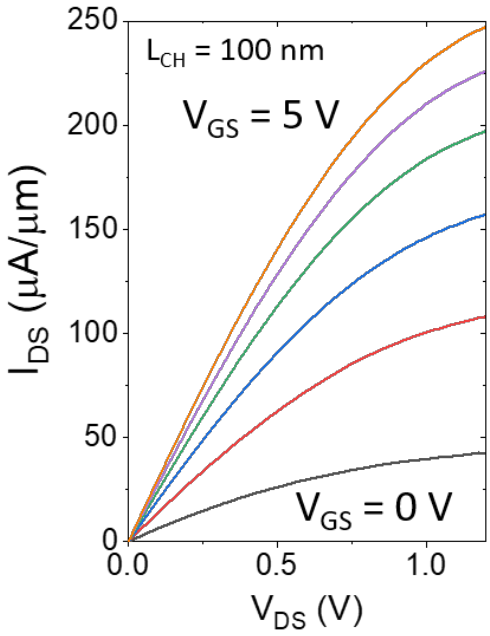


Figure 3.13 Output characteristics of the $MoS_2$ transistor with 10 nm $SiN_x$ back gate dielectric and Bi/Au source/drain contacts.

Figure 3.12 demonstrates the transfer characteristics of a back-gated $MoS_2$ transistor with under 100 nm channel length. Low drain-induced barrier lowering (DIBL) effect is observed due to the large band gap of $MoS_2$. Low subthreshold slope of around 140 mV/dec is also observed due to the thin and high quality $SiN_x$ back gate dielectric. Figure 3.13 shows linear output characteristics, demonstrating good ohmic contacts were formed between the source/drain region and the contact metals. The TLM structure also provide contact resistance of around 1.0 kΩ·μm, which is the lowest among the four ohmic contact technologies studied in this work. Actually, $MoS_2$ transistors with bismuth contacts also demonstrate the best overall performance and its fabrication process can also be very simple.

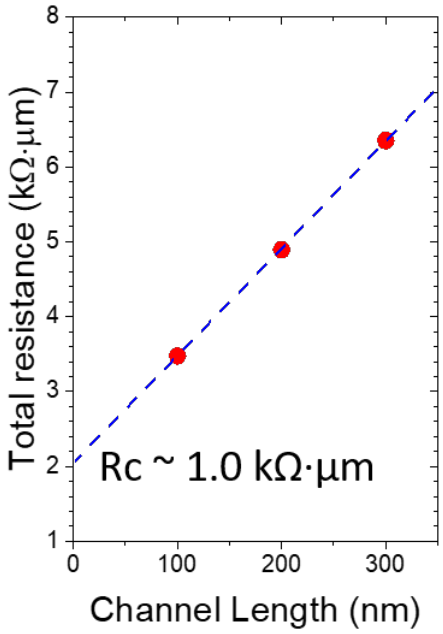


Figure 3.14 On-state resistance measured in transmission line model of the $MoS_2$ transistors with 10 nm $SiN_x$ back gate dielectric and Bi/Au contacts. 5V gate bias and 1V drain bias is applied in this case.

# 3.3 Chapter Summary

In this chapter, we demonstrated four different approaches to realize ohmic contacts in $MoS_2$ transistors. These methods can easily be integrated in a standard fabrication flow and

currently represent the state-of-the-art for low contact technology in 2D material transistors. As future directions, we can combine these methods together to further improve the contact quality. The optimization of contact quality to lower the contact resistance in 2D material transistors is essential and will determine whether the 2D material transistors would eventually be comparable to silicon transistors. For now, the state-of-the-art contact resistance in 2D material transistors is still about one order of magnitude higher than that in silicon devices. Hence, more efforts have to be made to further reduce the contact resistance in 2D material transistors in the future. Moreover, most of the contact engineering technologies are based on n-type devices. It would be of great interest to realize excellent ohmic contacts also in p-type 2D material devices.

# Chapter 4

# Highly-scaled High-performance Transistors based on 2D Materials

In the previous chapter, we discussed the contact engineering methods to realize good ohmic contacts in $MoS_2$ transistors. In this chapter, we will discuss possible approaches to fabricate high performance $MoS_2$ transistors at the limit of scaling. This would provide useful insights for the scaling of electronic devices, demonstrating the possible structure of the "ultimate" device that we could have by the scaling of device size.

## 4.1 Channel Length Scaling

In this section, we propose a novel self-aligned short channel double gate $MoS_2$ transistor, which could potentially have a channel length around or less than 10 nm and could possess excellent device performance after careful optimizations. The schematic of this novel device is shown in Figure 4.1. Instead of having a global gate structure, this device is designed to have two localized gate structure to reinforce the gate control over the channel material. The gate length is defined by electron beam lithography which can be scaled down to 2 nanometers (the smallest pattern size that could be fabricated with our EBL system, Elionix F-125). The source and drain are separated by the top gate terminal, which can be fabricated with a single step of metal deposition without further requirements on

EBL and pattern alignments. This self-aligned formation of source/drain terminals greatly reduces the fabrication challenges at the limit of scaling, as it spontaneously defines the channel length, and provides the possibility of realizing transistors with few-nanometer-long channel lengths.

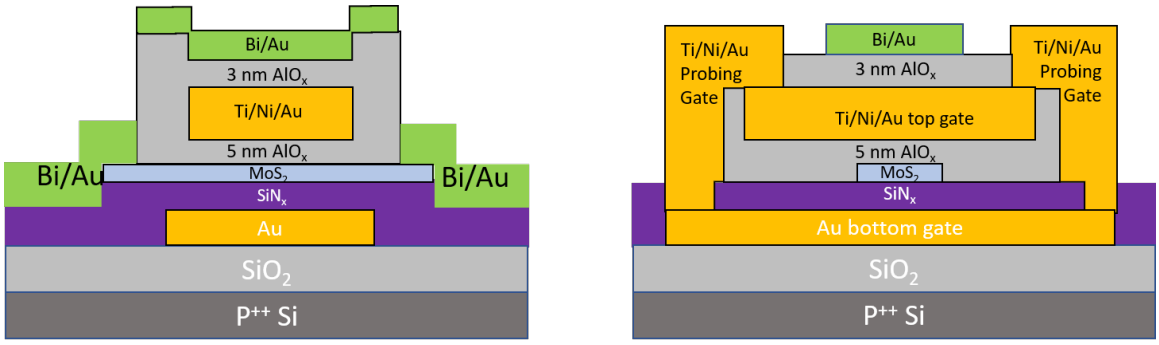


Figure 4.1 Schematics of the cross-sections (left) along the channel direction and (right) perpendicular to the channel direction, in the center of the channel of the self-aligned short channel double gate $MoS_2$ transistor

The fabrication process of the proposed self-aligned short channel double gate $MoS_2$ transistor is as follows:

0) **Substrate preparation**. The device is fabricated starting from a heavily p-type doped silicon wafer with 285nm $SiO_2$ on the surface. $O_2$ plasma cleaning was performed to ensure a clean sample surface.

1) **Local back gate.** Localized back-gate structures are fabricated with electron beam lithography with gate length from 20 to 110 nm. PMMA A4 950k was used as the photo resist. 20 nm gold was deposited followed by the lift-off process to from the back-gate electrode.

2) **Local back gate dielectric.** 5 nm $SiN_x$ thin film was deposited by PECVD method to form the back-gate dielectric. Electron beam lithography we then performed with reactive ion etching (RIE) process to make contact via through the $SiN_x$ layer, which would later connect the back gates to the top gates.

3) **Channel material.** Continuous monolayer $MoS_2$ film is then transferred on to the surface of the sample with polystyrene as the protection layer, which was later removed with toluene. Electron beam lithography combined with oxygen plasma etching are used to isolate the channel regions, which has a width of 2 μm.

4) **Local top gate and gate dielectric.** Electron beam lithography is carried out to define the top gate pattern, which have a gate length ranging from 10nm to 100 nm. A low temperature (80 ºC) ALD process is performed to grow 5 nm of $Al_2O_3$ as the top gate dielectric with the other regions still covered by the PMMA A4 950k. 1nm/ 60nm/ 40 nm Ti/Ni/Au layer is deposited as the top gate electrode followed by 3 nm of low temperature ALD $Al_2O_3$ to ensure the structure of the top gate electrode won't be broken during the lift-off process. The sample is then immersed in cold acetone for 30 hours for the lift-off process.

5) **Probing electrode for gate terminals**. Electron beam lithography is used to define the probing electrode for the top gate. PMMA A8 950k was used as the photo resist. RIE is performed to etch away part of the 3 nm $Al_2O_3$ on the two ends of the top gate electrode. 1nm/90nm/60nm Ti/Ni/Au metal stack is deposited followed by a lift-off process to form the probing pads.

6) **Source/drain formation**. Electron beam lithography is used to define the source drain pattern. There is no strict requirement on the accuracy of the exposure as the channel length is already determined by the top gate structure. A 20nm/30nm Bi/Au metal layer is then deposited, followed by a lift-off process to form the source/drain terminals.

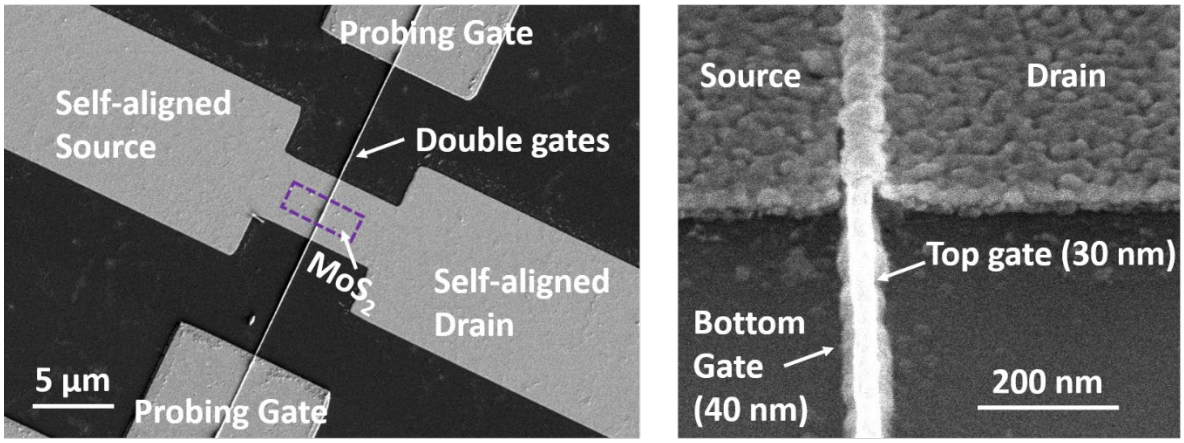


Figure 4.2 Top view SEM images of the fabricated self-aligned short channel double gate $MoS_2$ transistors with 30 nm top gate length and 40 nm bottom gate length.

The fabricated transistor is demonstrated in Figure 4.2 which has a channel length of around 30 nm. Excellent gate alignment is realized as the top gate is well overlapped with

the bottom electrode. The slightly oversized bottom electrode provides an exposure tolerance of ~ 5nm, which ensures the good alignment.

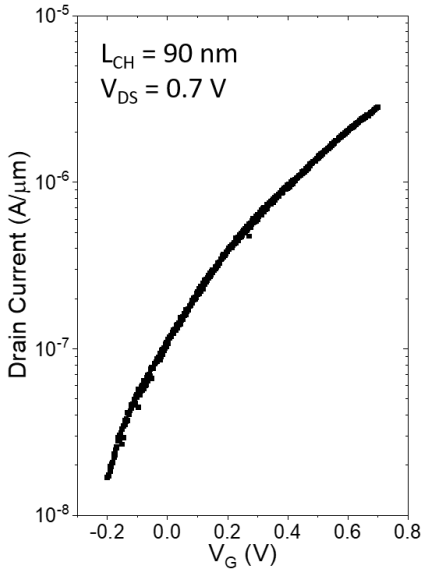


Figure 4.3 Transfer characteristic of a self-aligned short channel double gate $MoS_2$ transistors with 90 nm top gate length.

We measured the transfer characteristic of the prototype device (Figure 4.3). More optimizations have to be made to the source/drain contacts, the top gate dielectrics as well as other fabrication processes to further improve the performance of this self-aligned short channel double gate $MoS_2$ transistor. Yet, for now, it shows the feasibility of realizing short channel transistors with channel length less towards 10 nm and even shorter, which provides much insights for the design of future electronic devices.

# 4.2 Contact Length Scaling

Apart from the scaling of channel length, the scaling of contact length is also important. As feature size continues to scale down in transistors, conventional metal contacts will encounter higher resistance due to enhanced carrier scattering at metal grain boundaries and contact sidewalls [40-42]. However, CNT bundle nano electrodes do not suffer from these problems and the ultimate contact length can be as narrow as the diameter of a single-wall CNT. The previous demonstrated alignment uniformity, surface cleanness and excellent conductance of the CNT bundles all make them a promising contact material for

electronic devices. As shown in Figure 4.4, 25 individual top-gated devices are fabricated in an array, and cover an effective area of 25 µm × 3 µm. This fabrication method can be further extended for larger scale integrations, *e.g.* the 100-transistor array shown in Figure 4.5, or for smaller devices with higher integration density, e.g. the 4 × 3 transistor array with single device area of 300 nm × 200 nm in Figure 4.6.

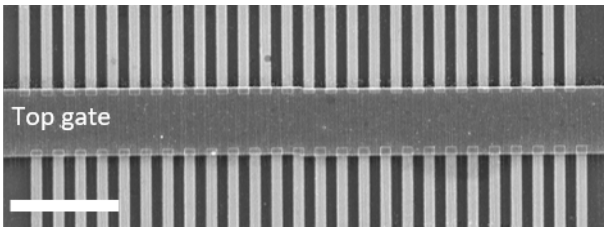


Figure 4.4 SEM image of 25 top-gated $MoS_2$ transistors in an array. Scale bar: 5 µm.

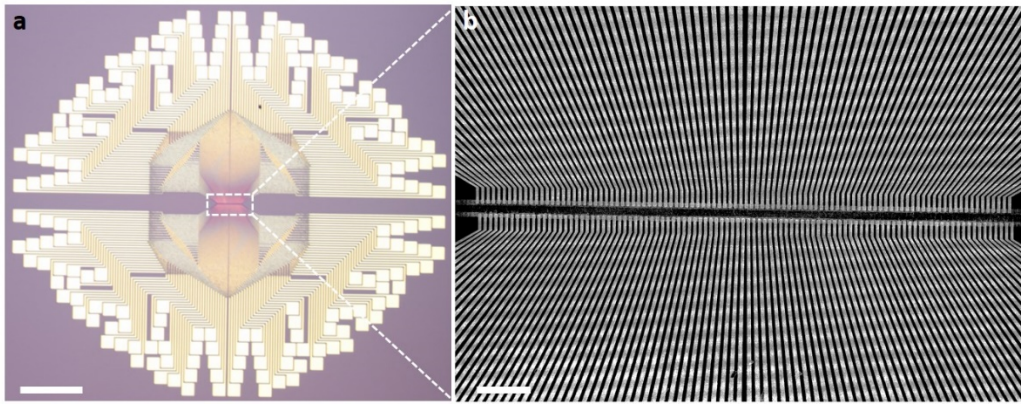


Figure 4.5 Images of the 100 $MoS_2$ transistor array with CNT bundles as source/drain contacts. a, Optical microscope image of the array. Scale bar: 250 µm. b, SEM image of the contact region inside the $MoS_2$ transistor array. Scale bar: 20 µm.

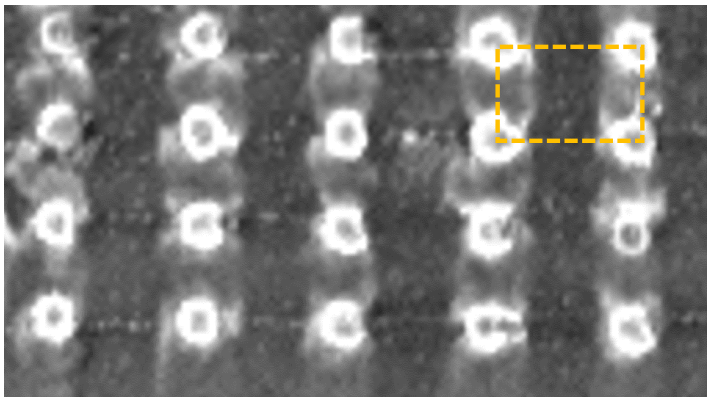

Figure 4.6 SEM image of a 4 × 3 back gate $MoS_2$ transistor array with shared CNT bundle contacts. The area of a single device (in the orange rectangle) is 300 nm × 200 nm.

In Figure 4.7, we demonstrated the transfer and output characteristic of 20 functional devices from the 25-device array. All these $MoS_2$ transistors exhibit *n*-type conduction with an on/off current ratio of ~ $10^5$ and the highest on-state current being 38 µA/µm. The extracted threshold voltage ($V_T$) is around -33 V, with a slight variation of 38.6 mV/V, demonstrating good device uniformity. The peak field-effect mobility estimated at the maximum transconductance was ~3.4 $cm^2\ V^{-1}\ s^{-1}$, which is comparable to the value (~3.5 $cm^2\ V^{-1}\ s^{-1}$) of using Au contacts.

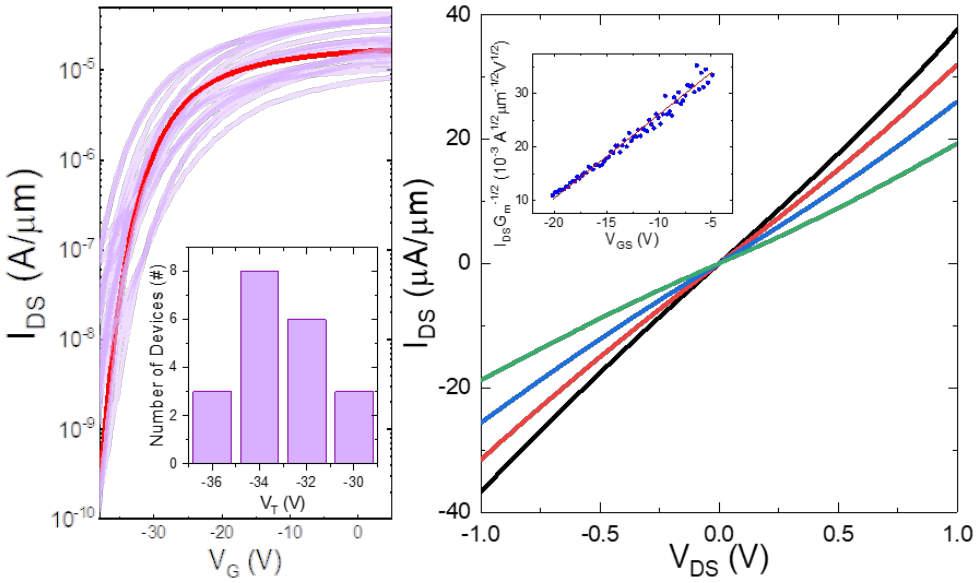


Figure 4.7 (Left) Measured transfer characteristics of 20 $MoS_2$ transistors inside the array at room-temperature and $V_{DS}$ = 1 V. The red line demonstrates the representative performance among the 20 devices, (inset) threshold voltage ($V_T$) distribution of the 20 devices. (Right) Measured output performance of the $MoS_2$ transistors, (inset) channel mobility extraction.

We also observed good device-to-device uniformity among different transistor arrays (Figure 4.8), demonstrating the possibility of larger scale integration by fabricating more devices in one large array or making more transistor arrays with few devices. The current density of the CNT bundle contact $MoS_2$ transistor is also higher than most of reported semiconducting $MoS_2$ devices and the semiconducting CNT (s-CNT) channel transistors, thanks to the small contact resistance and good conductance of the metallic CNT (m-CNT) bundles, and could be increased even further by scaling of channel length as well as changing of channel materials, showing its potential for high-performance logic circuits.

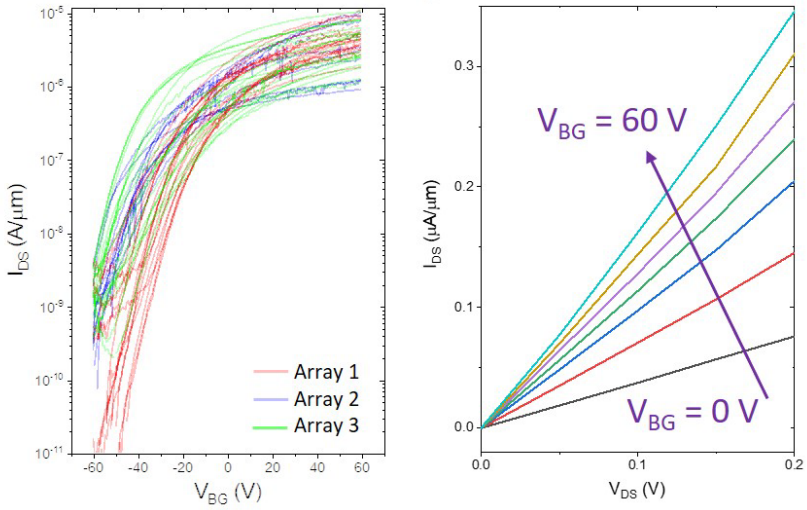


Figure 4.8 Electrical measurement of back-gated $MoS_2$ transistors with CNT bundle contacts from three different arrays, which also demonstrate good uniformity. (Left) Transfer characteristics of 43 functional devices from 3 different arrays. (Right) Output characteristics of a representative back-gate transistor, which also has relatively good output linearity.

# 4.3 Chapter Summary

In this chapter, we looked into the possible technologies that could help the further scaling of transistors. The proposed technologies based on self-aligned source/drain and the integration of metallic or semiconducting low-dimensional nanomaterials represent new paradigms for advanced devices at the limit of scaling. More investigations need to be done to optimize these prototype devices to improve their performance and uniformity. Multi-channel transistors based on 2D materials represent another interesting direction that should be studied further.

# Chapter 5

# Conclusions and Future Work

## 5.1 Conclusions

In this thesis, we focused on developing three important technologies for BEOL integration of 2D materials with state-of-the-art silicon wafers: the low-temperature synthesis of 2D TMD materials on wafer scale, contact engineering methods to realize low contact resistance in 2D $MoS_2$ transistors, and scaling approaches for 2D material devices. The main conclusions are summarized as below:

For wafer-scale low-temperature synthesis of 2D $MoS_2$ monolayer thin films:

1) We demonstrated a novel MOCVD method to grow 2D $MoS_2$ with synthesis temperature lower than 300$^{o}$C by using ammonium iodide and crystal violet together as the seeding promoter.

2) We illustrate a feasible approach to synthesize 2D TMD materials with CMOS-compatible process. Potential contamination, such as the alkali metal salts, was removed from the synthesis system without causing significant degradation in the grain size of the synthesized 2D material.

3) We successfully designed and build an 8-inch MOCVD system that is capable to grow wafer-scale 2D materials with good uniformity, low temperature and less contamination, which would be a promising method to realize BEOL integration as well as ultra-large-scale integration with 2D material devices and circuits in the near future.

For the contact engineering on 2D $MoS_2$ transistors:

1) We successfully demonstrated ohmic contacts in $MoS_2$ transistors by both phase transition and bismuth metal, which are useful for circuit level integration.

2) We demonstrated the use of carbon nanotube bundles as nanoscale contacts in $MoS_2$ transistors, which might be a promising technology for the further scaling of transistor contacts.

For the device level demonstrations:

1) We developed a novel technology to fabricate high performance 2D material transistors with gate length approaching tens of nanometers and self-aligned source/drain regions. This method would be a possible way to realize the ultimate high-performance transistors at the end of physical scaling.

2) We demonstrated array-level-integration of transistors based on CNT bundle contacts, and discussed the potential applications of this novel technology for BEOL integration.

# 5.2 Suggestions for Future Work

Based on the results presented in this thesis, future research directions can be identified in the flowing three directions:

**A. Wafer-scale, low-temperature synthesis of 2D materials**

1) Further synthesis could be done on annealed c-plane sapphire substrate to obtain 8-inch monolayer 2D materials with a uniform crystalline orientation. The use of c-sapphire substrates would also be useful for they synthesis of most 2D materials, including TMDs, graphene and hBN.

2) Expand the material system that can be synthesized with the 8-inch MOCVD system, which could be, but not limited to $WSe_2$, graphene, and hBN.

3) Reduce the synthesis temperature and total growth time, which decrease the defect density and decrease the total thermal budget.

4) Multilayer growth of 2D materials, which reduces the time that transfer process is needed. This could efficiently reduce the polymer contaminations and physical damage to

the 2D materials during the transfer process. Heterogenous integration is also promising, which allows different types of materials to be grown laterally or vertically next to each other, to form intralayer or interlayer heterojunctions.

5) Efficient wafer-scale transfer method that would allow us to transfer the 8-inch monolayer 2D materials onto any arbitrary substrate without causing damages or contaminations.

**B. Device design and optimizations**

1) Further synthesis could be done on novel methods or potential technologies that could reduce the contact resistance in 2D material devices to around or even less than 10 Ω•μm. In spite of all the recent progress, all the reported works still cannot demonstrate 2D material devices with a contact resistance better than in silicon devices. Further improvements on contact engineering methods are needed to allow 2D material devices to be fully accepted by the electronic device society.

2) The design and fabrication of high-performance 2D material transistors that could have current density more than 10 times higher than silicon transistors at the same operation voltage and technology node.

3) 2D material devices that could realize the ultimate scaling of transistors.

4) P-type transistors based on 2D materials is very important for both the device and circuit society. However, little knowledge exists on how to efficiently fabricate a high-performance p-type 2D material transistor. Namely, how to obtain low-resistance p-type contacts and which material could be used as the semiconducting channel. $WSe_2$ may be useful in this case, yet more investigations are still needed.

5) Potential applications for 2D material devices, which may include but not limited to RF rectifiers, high-density memories, and low-power neuromorphic device.

6) Possible methods that could improve the stability and reproducibility of 2D material devices from device level.

7) Methods that would be useful for BEOL technology, e.g. selective/controllable etching of monolayer 2D materials without damaging the other 2D materials underneath, effective gating technology, multi-channel transistor structure.

8) Improve the quality of gate dielectric in 2D material transistors. More investigation could be done on the doping effect from the dielectric layers, the possible selection of gate dielectric materials, and the possibility of realizing devices purely with 2D materials, i.e. with 2D metal contact and 2D insulators.
9) Investigate the contacting methods for ultra-wide bandgap materials, e.g. 2D GaN and 2D hBN, which would be useful for power electronic circuits.

**C. Circuit level integration**

1) The fabrication technology of 2D material devices and circuits on 8-inch wafers. More detailed analysis on device variations could be carried out. Standard cell library for 2D material transistors could be prepared as the basis for circuit level integrations.
2) Design ULSI circuits based on wafer scale 2D materials, devices, 2D material transistor standard cell library.
3) Flexible electronics based on 2D materials and flexible substrates.
4) Power electronic circuit based on ultra-wide bandgap 2D material devices.
5) BEOL integration with multiple device/circuit layers.

In summary, there are many interesting opportunities and projects to be worked on in the next few years and decades to come. It is a truly exciting time to be working on the 8-inch low-temperature synthesis technology, and its combination with advanced fabrication technologies will allow hybrid systems with unique performance. The future for 2D material devices and circuits is extremely promising, and it will help provide people dreams and a bright future in the way that science always does.

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