CMOS THz-ID: A 1.6mm^2 Package-Less Identification Tag Using 260-GHz Far-Field Backscatter Communication

by

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Abstract

Radio Frequency Identification (RFID) tags have been widely used for counterfeit mitigation, authentication and supply chain management. Small form factor, power efficiency and cost are the important requirements of these tags which are often limited by off-chip antenna and packaging. Operating at Terahertz (THz) frequency removes these limitations by enabling on-chip antenna array within mm-size with sufficient gain. In this thesis, I presents an ultra-small identification tag that is entirely built in a CMOS chip without external components. The usage of backscatter communications at 260 GHz enables full integration of a 2×2 patch antenna array. For chip compactness and minimum interference caused by direct wave reflection, the backscatter signal is frequency-shifted by 2 MHz and radiated with cross-polarization from the same antenna array. Such a configuration also, for the first time for RF tags, enables beam-steering for enhanced link budget. The presented tag has a peak power consumption of 21 μW and can be powered by a chip-wide array of photodiodes. Using a low-cost 65-nm bulk CMOS technology, the THz-ID chip has an area of only 1.6 mm^2 and demonstrates measured downlink speed of 100 kbps and upload speed of 2 kbps across 5 cm distance from the reader. The tag-reader authentication/communication protocol is fully demonstrated using external tag power and partially demonstrated using the tag-integrated photo-voltaic powering. The tag size is the smallest among all prior RFIDs using far-field communications.

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I am grateful for the technical advises and contributions from Rabia Yazicigil and Wanyeong Jung in this project. Furthermore, thanks for the technical discussions with my labmates including but not limited to: Cheng Wang, Xiang Yi and Zhi Hu.

Last but not least, I would like to thank my family and friends. Specially, my parents and my wife for their patience, love and care, and support during my studies and research. There are no words that can express my appreciation towards them.

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Chapter 1

Introduction

1.1 Motivation

Radio-frequency identification (RFID) tags have been widely adopted in tracking, authentication, localization, supply-chain management, health care and so on [31]. They are filling the information gap between the physical world and the digital world, maximizing efficiency and improving quality of life. For example, inside a hospital, a fine-grained localization and authentication technology can help doctors and nurses keep track of assets and medicines, and thus, reduces operational costs while increasing the quality of patient care [5, 10]. In retail, locating items on shelves and tracking the movement of goods improves customer experience and provides valuable analytics for store owners [19, 25]. In the supply chain, such capability can optimize the pallet loading and quality control processes, in which a lot is done manually today [6, 20].

At present, commercial RFID chips rely on external antenna or inductor packaging to facilitate efficient coupling of the RF waves. That, however, significantly increases the overall size of the tag, making it impossible to be attached to small objects such as medical pills, tooth implants and semiconductor chips. The associated authentication and recording of manufacturing data, therefore, can only be realized indirectly through special treatments (e.g. holographic patterns) on the goods packages, which leave loopholes for counterfeiting. Another barrier for RFID applications is the additional cost associated with the chip packaging, which takes up to two thirds of the

total tag cost [24, 26]. That makes RFID technologies much less competitive than optical identification systems (based on barcodes or QR-codes), for example, printed barcodes for low-cost products (e.g. a 50-cent candy bar) [31]. Lastly, it is noteworthy that pervasive electronic tagging raises serious privacy concerns related to inadvertent and malicious tracking of the tagged assets. Other sensitive data related to, for example, finance and personal health, are also increasingly generated by RFIDs. However, encryption and authentication protocols normally require intensive computing, making reliable data protection difficult to realize in power/hardware-constraint RFID operation environments.

1.2 Related Works

In order to enable secure and ubiquitous asset tagging, fully-passive, particle-sized identification chips without external packaging are highly desired. However, the recently demonstrated prototypes [3,4,14,23,28,33] that took the above path face either size, energy, communication or security limitations. In [4], a 9-mm^2 sensor node (volume=27 mm^3) is implemented at 915MHz out of a stacked packaging of multiple functionality layers for photo-voltaic powering, battery, antenna, etc. This increases the overall size and cost of the sensor node. In [33], a 116×116 μm^2 monolithic radio chip is demonstrated, that relies on near-field inductive coupling at 5.8 GHz with on-chip coil antenna, which severely limits the operation range to ∼1 mm. In comparison, far-field tag interrogation using resonant antennas effectively increases the range. Using this principle, a pad-less chip with 24-GHz downlink and 60-GHz uplink boosts the range to 50 cm [27, 28], but the chip-integrated transmitter (Tx) and receiver (Rx) antennas at two different frequencies also increase the chip size to 3.7×1.2 mm^2. While this is already an impressive form factor, to fully enable the applications described previously, a further miniaturization is desired. In [23], a mm-Wave power-harvesting RFID tag is presented where the chip size is 1.3×0.95 mm^2 without including the antenna. The off-chip 60GHz antenna increases the size and requires special packaging. A bidirectional 0.32 THz radio is presented in [3] with a

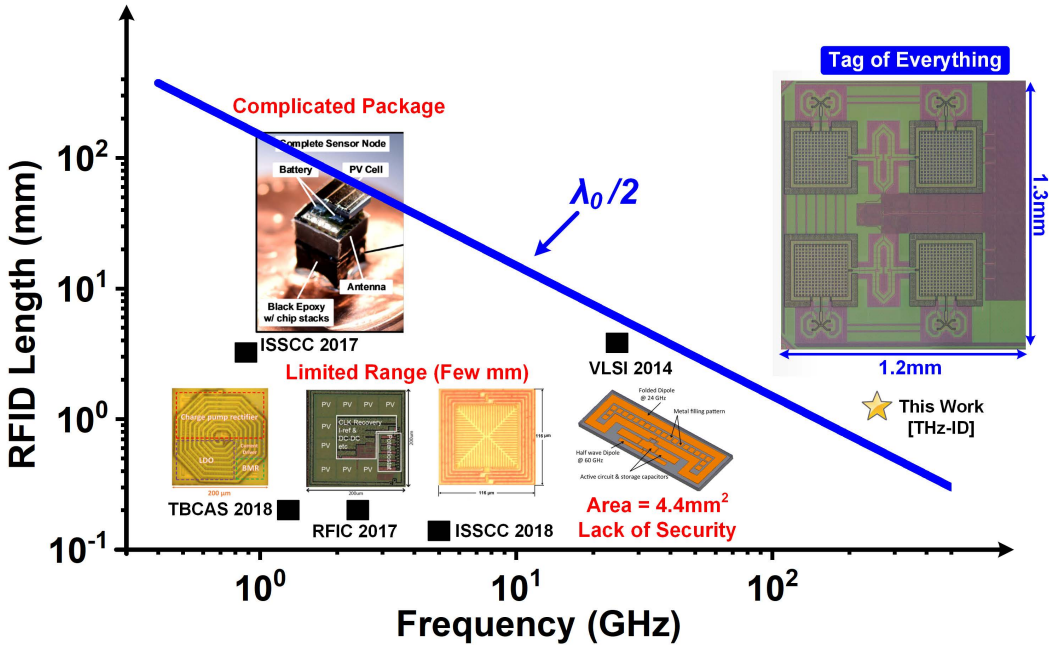


Figure 1-1: Size comparison of previous works. Blue line indicates the reduction in the size of resonant antenna with frequency.

size of 0.57 mm^2 because of on-chip Tx and Rx antennas. However, this work doesn't involve power-harvesting and requires a separate battery for its 49.3 mW peak DC power consumption. The additional battery increases the size of the whole package. It is also noteworthy that all the above works [3, 4, 23, 28, 33] also do not support secure identification. To this end, [14] demonstrates a secure authentication tag, but the chip requires an 8-mm^2 433MHz external antenna and works by inductive coupling which limits its operation range.

1.3 Innovations

The major challenge of tags' physical size is dominated by the size of resonant antenna which is important for efficient far-field communication. The size of a resonant antenna is of the order of $\sim \lambda_o/2$ where λ_o is the wavelength. This indicates that operating at THz frequency will drastically reduce the antenna size enabling mm-size form-factor for the tags. Fig. 1-1 compares the size of previously reported work with the proposed THz-ID emphasizing size scaling with frequency. The aggressive CMOS

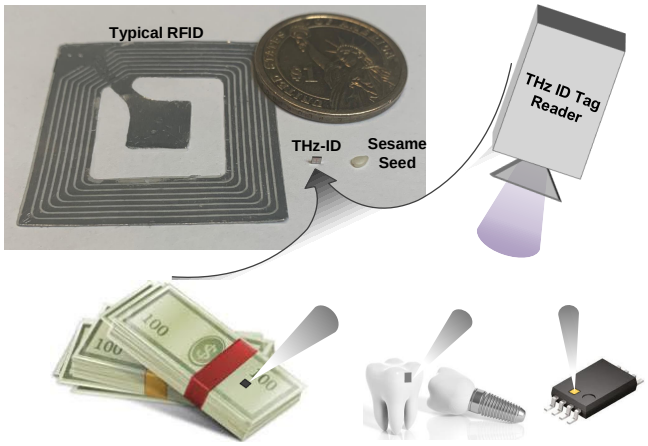


Figure 1-2: THz-ID tag: a size comparison and its potential applications.

scaling allows for THz tags but THz circuits (e.g: oscillators) consumes a large DC power making them incompatible with field-deployable applications. This hurdle is overcome through photovoltaic energy-harvesting and back-scattered communication in the proposed design.

In this thesis, I present a package-less, monolithic tag chip in CMOS, that has a size of 1.2×1.3 mm^2 (shown in Fig. 1-2) [13, 15]. To enable far-field operation with such small form factor, the downlink/uplink carrier frequency is pushed into the low THz regime (260 GHz). That, along with a Tx-Rx antenna sharing technique, allow for an on-chip integration of a 2×2 antenna array and a tag-side, beam-steering capability. An operation range of 5 cm is demonstrated, which makes barcode-reader-like applications possible. A frequency-shifted back-scattering technique with orthogonal radiation polarization is employed which helps in distinguishing weak back-scattered signal from strong reflection of incident wave. The whole chip consumes a peak power of 21 μW, which is provided by an array of chip-integrated photodiodes.

The details of the system architecture of the first prototype of THz-ID is presented in chapter 2 while the design of the circuit blocks is presented in chapter 3. The measurements setup and results are given in chapter 4. Finally, chapter 5 provides a conclusion for this work while pointing out potential improvements and perspectives for future work.

Chapter 2

THz-ID System Architecture

2.1 Hardware Architecture

The architecture of the tag chip is shown in Fig. 2-1. The incident 260-GHz wave (red) from the reader is coupled to a 2×2 array of on-chip patch antennas. The THz signal with a particular linear polarization received by each antenna is extracted from two sets of antenna feeds with a power-splitting ratio of ∼1:1. Half of this power, used for the downlink, is rectified to baseband via four THz square-law detectors. The other half of the input power is used for the back-scatter uplink communication. It is noteworthy that a strong, direct reflection of the incident downlink wave, due to the large surface of the object to be tagged, is inevitable. It is, therefore, critical to eliminate the interference of such reflected waves to the actual data-modulated signal, which is back-scattered by the chip. To this end, single-sideband (SSB) frequency mixing is added to the back-scattering process, so that the final carrier frequency for the uplink (f_{UL}) is ∼2 MHz below that for the downlink (f_{DL}). Meanwhile, the chip is designed so that the polarization of the back-scattered wave (blue in Fig. 2-1) is also rotated by 90°, so that the tag reader's receiver antenna with a linear polarization aligned with the back-scattered wave can further suppress the directly reflected wave by >20 dB. The cross-polarization scheme also allows for re-using the downlink antennas for uplink antennas, which reduces the tag area by ∼2x. More details of the antennas will be given in chapter 3.

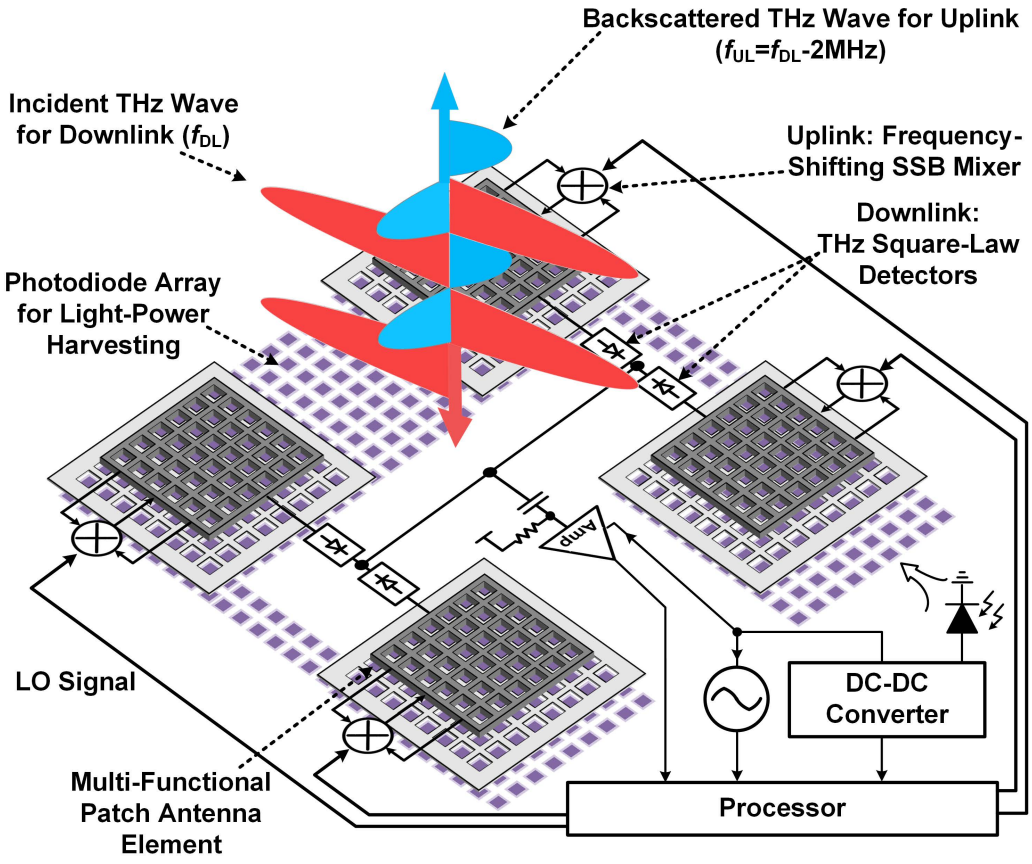


Figure 2-1: Overall architecture of the THz-ID tag.

Both the downlink and the uplink utilize ON/OFF-shift-keying (OOK) modulation, and offer data rates at 100 kbps and 2 kbps, respectively. The THz SSB mixers for the frequency shifting of the uplink carrier are driven by four 2-MHz local-oscillator (LO) signals generated by an integrated processor. With independent, digital control of the phase in each LO, beam-steering for the THz uplink wave is achieved. That enhances the link budget when the tag is not perpendicularly facing the tag reader. Moreover, without the beam-steering capability, the tag would act like a mirror and make the back-scatter communication more prone to eavesdropping.

In the protocol, the processor first sweeps the uplink beam direction until reliable communication is established. Then it will work with the reader to perform an identification protocol. The photo-voltaic powering of the tag is realized through a large array of P-N photodiodes placed under and beside the antennas. To allow the incident light to reach the photodiodes, the patch and the ground plane of the antenna possess a fishnet pattern (Fig. 2-1). A DC-DC converter is implemented in order to boost the photodiode output voltage to $\sim$1 V. A 8-MHz oscillator is integrated to provide the LO signal for the THz SSB mixers, as well as the clock signals for the DC-DC converter and the processor. The photodiodes, DC-DC converter and processor were implemented by my collaborators.

2.2 Chip Micrograph

The tag chip is fabricated using a TSMC 65-nm bulk CMOS process. The micrograph of the chip is shown in Fig. 2-2. The chip has an area of 1.3×1.2 mm^2. The two rows of pads, which can be cut, are for debugging purpose only.

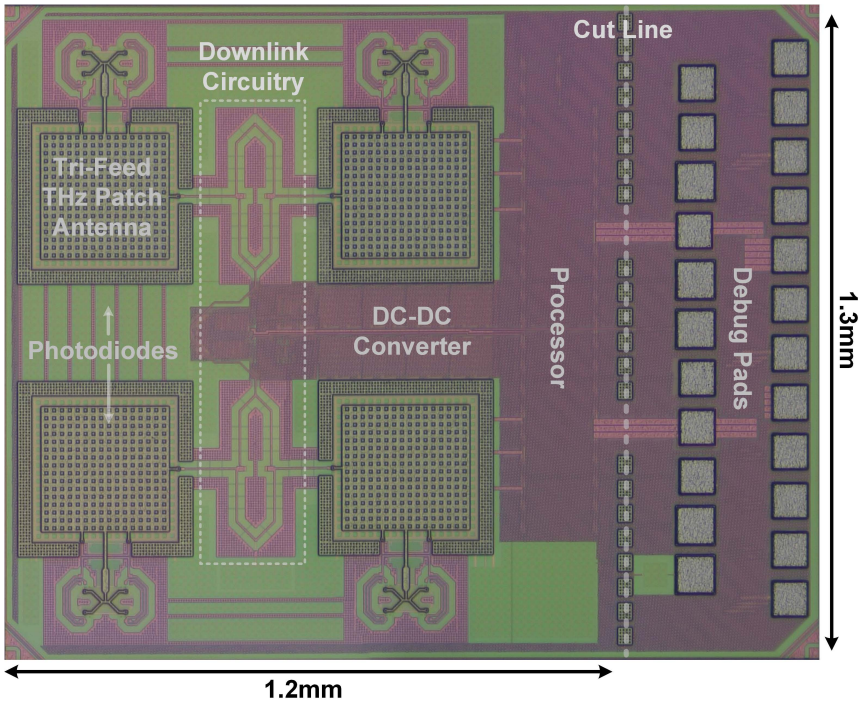


Figure 2-2: Chip micrograph

Chapter 3

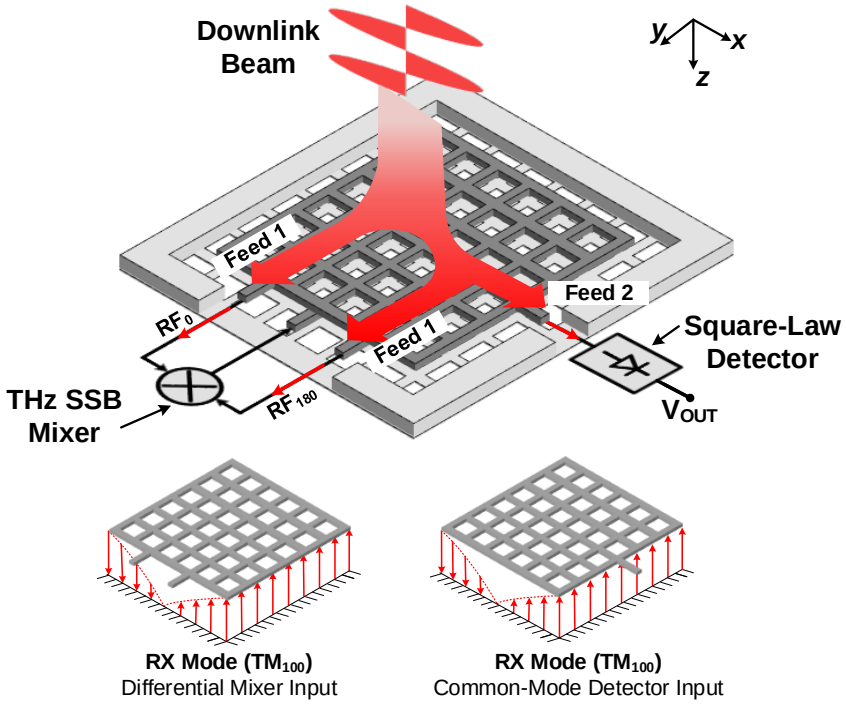
THz Downlink and Uplink

In this chapter, I describe the design of various tag components that enable 260-GHz communication with very small power consumption and chip area.

3.1 Multi-Functional On-Chip Patch Antenna

To enable front-side radiation, the tag integrates 2×2 patch antennas that are shared between the downlink and uplink. To realize such sharing, a near-square shape is adopted for the patch, so that its two dominant excitation modes i.e. TM_{100} and TM_{010} with orthogonal polarizations have the same resonance frequency (∼260 GHz). As Fig. 3-1a indicates, to excite a certain mode (TM_{100} in this case), we can either use a differential feed symmetrically connected to the patch edge along the x-direction (i.e. Feed 1), or a single-ended feed connected to the center of the patch edge along the y-direction (i.e. Feed 2). Therefore, when both feeds are used and the downlink wave aligns with the TM_{100} mode of antenna, the received power is split into the two feeds for back-scatter (Feed 1) and downlink demodulation (Feed 2), respectively. Accordingly, the THz SSB mixer has a differential input, while the THz square-law detector for the OOK de-modulation of downlink has a single-ended input (Fig. 3-1a).

Next, to radiate the uplink signal with orthogonal polarization, the TM_{010} mode of the same antenna is used (Fig. 3-1b) and is excited by a single-ended feed (Feed 3) at the center of the patch edge along the x-direction. Accordingly, the THz SSB



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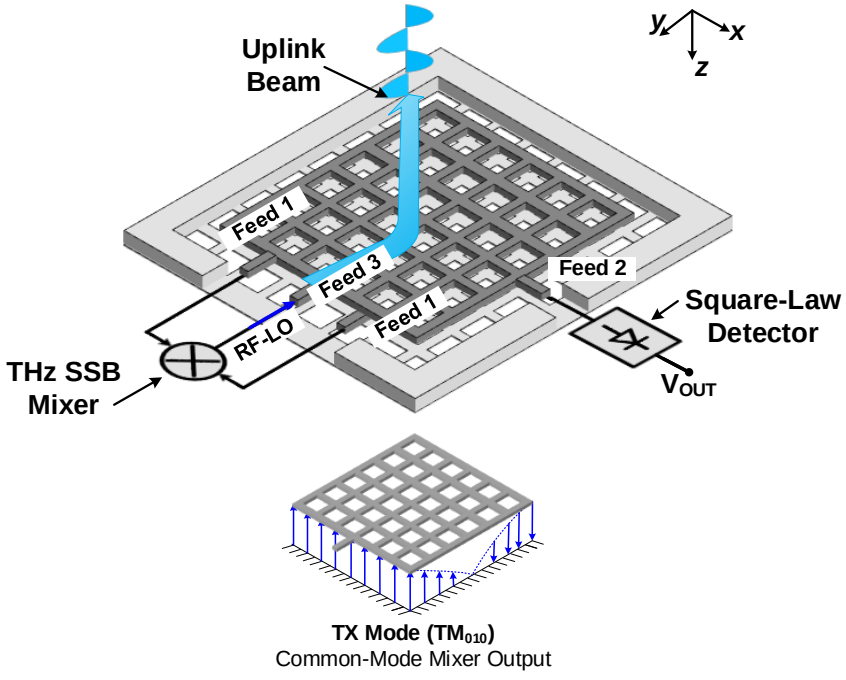
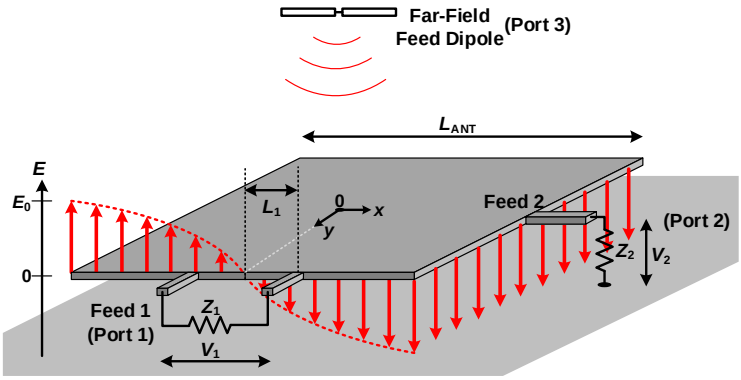
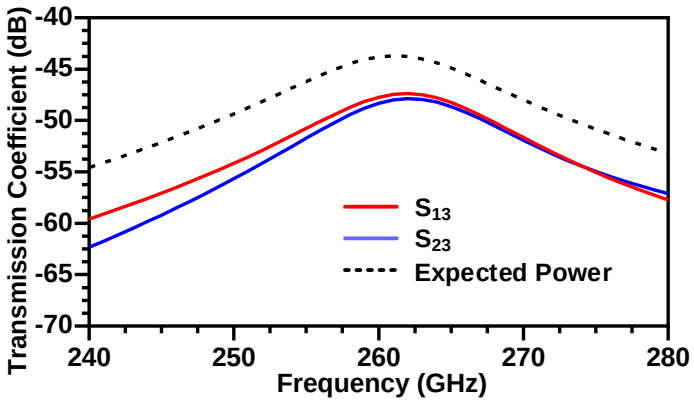


(b)

Figure 3-1: Schematic of the multi-port patch antenna with excited (a) TM_{100} for downlink and (b) TM_{010} for uplink.



(a)



(b)

Figure 3-2: (a) The electrical-field distribution of the TM_{100} mode in the multi-port antenna. (b) The simulated power transmission coefficients from a far-field feed dipole (2 cm away) to the two ports associated with the downlink, when they are terminated by Z_1=150 Ω and Z_2=450 Ω, respectively. The dotted line shows the expected total received power, which includes the free-space propagation loss and the gains of two antennas. Ideally, it should be 3-dB higher than S_{13} and S_{23} when the power transmissions to Port 1 and 2 are equal and maximized.

mixer provides a single-ended output, as described later in Section 3.2. Note that the electrical field distribution of the associated TM_{010} mode has a null at Feed 2, so the leakage of the uplink signal to the THz square-law detector is very small. Similarly, the received downlink signal does not leak into the SSB mixer output either (Fig. 3-2a)[1].

To ensure the reliability of both the downlink de-modulation and the backscattering, the power splitting ratio in Fig. 3-1a is set to about 1:1. The value of the ratio

[1]Note that the uplink signal injected at Feed 3 can *couple back* to the SSB mixer through a *common-mode* leakage in Feed 1. Techniques to prevent such leakage are described in Section 3.2.

is controlled by the termination impedances at Feed 1 and Feed 2 (i.e. Z_1 and Z_2 in Fig. 3-2a). To determine the optimal values of Z_1 and Z_2, we first derive the desired ratio of K=Z_2/Z_1. Note that for the TM_{100} resonance mode, the distribution of the electrical field (hence the local voltage with respect to ground) along x-direction approximately follows an anti-symmetric sinusoidal pattern (Fig. 3-2a), and can be expressed as [2]:

$$V(x) = V_0 \cdot \sin \frac{\pi x}{2L_{ANT}}, \tag{3.1}$$

where V_0 is the maximum RMS voltage at the edge of the antenna, and L_{ANT} is the dimension of the antenna. Therefore, the power injected into Z_1 and Z_2, respectively, is:

$$P_1 = \frac{4V_0^2}{Z_1}(\sin \frac{\pi L_1}{2L_{ANT}})^2 \quad and \quad P_2 = \frac{V_0^2}{Z_2}, \tag{3.2}$$

where L_1 is the distance of each Feed 1 wire from the antenna edge center (Fig. 3-2a). For equal power splitting (i.e. P_1=P_2), the required ratio K is derived:

$$K = \frac{Z_2}{Z_1} = \frac{1}{4(\sin \frac{\pi L_1}{2L_{ANT}})^2}. \tag{3.3}$$

In our design, the value of L_1/L_{ANT}, limited by the circuit floorplan, is about 0.18, which leads to K≈3. Next, to further determine Z_1 and Z_2, we note that their optimal values should provide matching between the entire downlink structure and the incident plane wave. This scenario is emulated in a full-wave electromagnetic simulator, HFSS [1], with a far-field half-wave dipole antenna (Port 3 in Fig. 3-2a). The dipole has a gain of 2 dB and is located at 2 cm from the on-chip patch antenna. The absolute values of Z_1 and Z_2 are then swept (while keeping their ratio of K=3). When Z_1=150 Ω and Z_2=450 Ω, maximum total power transfer from the feed dipole to the two patch antenna ports (S_{13} and S_{23} in Fig. 3-2) is obtained, meaning that the wave reflection on the antenna is minimum. Fig. 3-2b shows the simulated power transmission co-efficient (including free-space propagation loss) when the above optimal impedance values are applied.

Regarding the implementation of the patch antenna, its radiator uses the top

aluminium (Al-pad) layer of the CMOS process, and has a size of 271 μm in the x-direction and 235 μm in the y-direction. These dimensions, along with the additional feed ports, lead to the same resonant frequency for both TM_{100} and TM_{010} modes. The patch would have a square shape if only Feed 2 and Feed 3 were present but the differential Feed 1 necessitates a non-square shape. The patch radiators and the ground planes of the antennas are implemented with a fishnet pattern to allow transmission of light through them for photovoltaic harvesting. The ground plane of the antenna is made out of M3 layer. The antenna is also enclosed by a ground wall (M3 to top aluminum layer), which is 20-μm away from the patch at all sides. That reduces the coupling with neighboring electronics and antennas while its effect on the antenna performance is negligible. Using HFSS the peak directivity and radiation efficiency of the antenna in the simulation are 6.7 dBi and 27%, respectively, in both resonant modes.

3.2 THz Frequency-Shifting Backscatter Module

Instead of using a dedicated Tx signal source on a tag [28], which is too power hungry to be practical for THz IDs, our uplink adopts an energy-efficient backscatter scheme for the incident wave. As described in chapter 2, the backscatter module applies a frequency shifting to the THz signal. Shown in Fig. 3-3, the backscatter module consists of a passive single-side (SSB) band mixer, two 90° Lange couplers and a balun. It takes the differential RF signal from the antenna, generates its quadrature phases, and then mixes it with a set of 2-MHz quadrature LO signals. The mixer output is finally injected back to the antenna. Next, details of the components in the backscatter module are given.

3.2.1 Input Balun

In Fig. 3-1b, the TM_{010} mode excited by the SSB mixer output presents a common-mode electrical field at the two wires of Feed 1. As a result, the mixer output will be fed back to the mixer and undergoes an extra down-shift by f_{LO} in each round

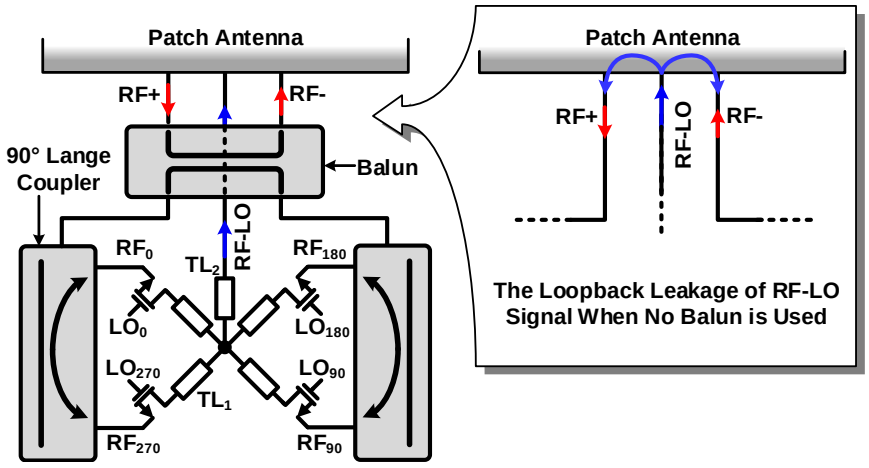
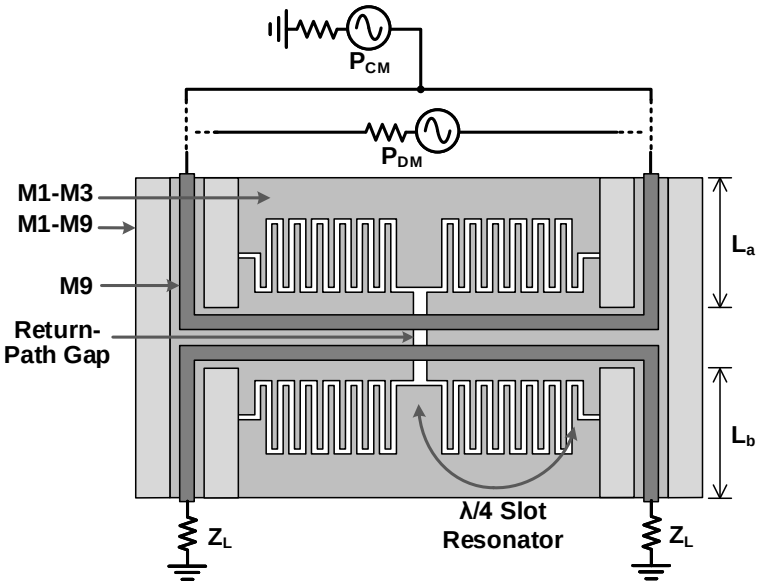
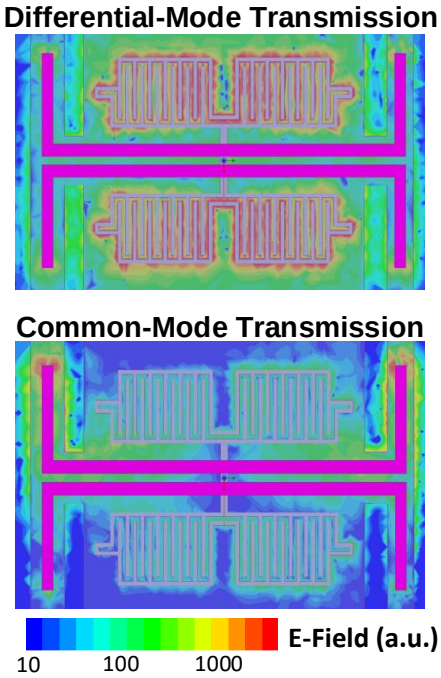


Figure 3-3: Schematic of the backscattering module consisting of a passive SSB mixer, a balun, and two 90° Lange couplers. The loopback effect with the absence of the input balun is also shown.

trip. Such loopbacks therefore cause excessive signal loss and undesired LO harmonic spurs. To avoid it, between Feed 1 of the antenna and the SSB mixer input, a balun is inserted, which only allows the transmission of differential signal from the antenna, and blocks the common-mode leakage from the mixer output. A return-path-gap-based balun introduced in [30] is used, which consists of two microstrip lines coupled via a slot in the ground plane (i.e. return-path gap or RPG, see Fig. 3-4a). The RPG slot, closed by four quarter-wavelength slot resonators in the ground plane, only allows transmission (hence input-output coupling) of quasi-TE-mode wave, which is excited by a differential signal in the input microstrip lines. That is illustrated in the electromagnetic simulation shown in Fig. 3-4b, and we can see that the common-mode signal is effectively rejected. The simulated insertion loss for the differential mode is $\sim$1 dB and the rejection for the common mode is >10 dB from 240 to 280 GHz. The balun is implemented using 2-μm-wide M9 microstrip lines and slots in a shunted M1-M3 ground. Note that a wire placed along the central line of the balun connects the SSB mixer output (f_{RF}-f_{LO}) and the antenna (Fig. 3-3); since the balun central line can be treated as the virtual ground for the differential-mode transmission, the above wire does not interfere with the balun operation.



(a)



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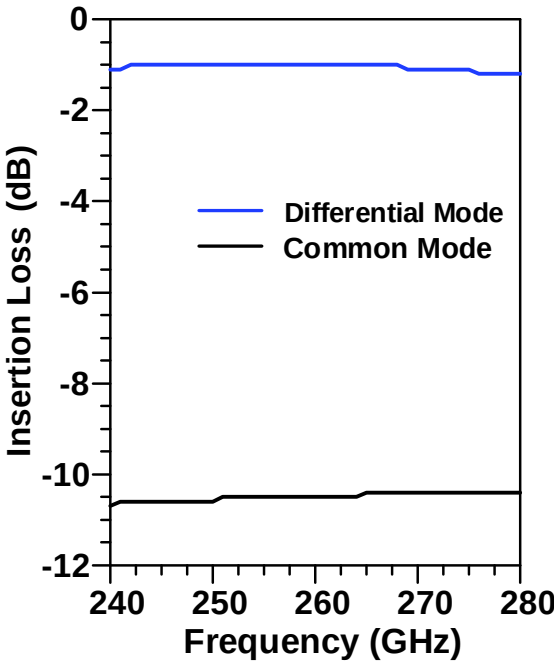


(c)

Figure 3-4: 260-GHz balun based on a return-path gap: (a) structure, (b) simulated electrical-field distribution, and (c) simulated insertion loss from the input to one load Z_L.

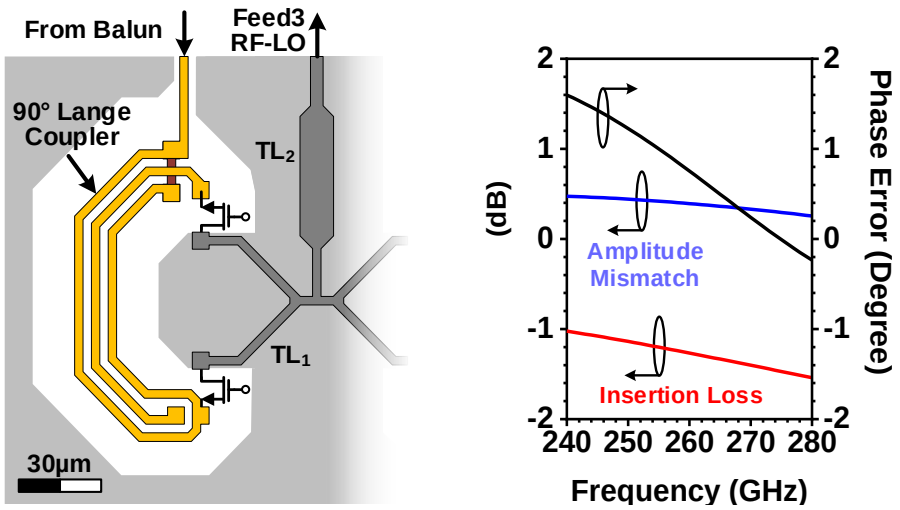


Figure 3-5: (a) The structure of the 260-GHz Lange coupler in the backscatter module. (b) Simulated insertion loss and output mismatch of the coupler.

3.2.2 Coupler

The Lange coupler that generates the quadrature phases for the input 260-GHz signal is shown in Fig. 3-5a. The electromagnetic simulation results are shown in Fig. 3-5b; at 260 GHz, the simulated insertion loss excluding the ideal 3-dB power splitting factor is 1.2 dB, and the amplitude/phase mismatches at the two output ports are 0.5 dB and 0.5°, respectively. The couplers are implemented using the M9 layer, with 3-μm-wide lines and 3-μm spacing among the lines. The couplers are also enclosed by a ground plane (with a spacing of 15 μm) to provide the signal's return path and to minimize the coupling to surrounding structures.

3.2.3 Passive Single-Sideband Mixer

Although a double-sideband (DSB) mixer involves simpler hardware implementation, we note that the generated upper and lower sidebands are applied with opposite phases from the LO; in our tag, therefore, their associated uplink beams would point to different directions in the beam-steering. That lowers the security and causes signal loss and interference. In our design, a SSB mixer based on passive quad switches is adopted to not only suppress the upper-sideband of the output, but also to minimize

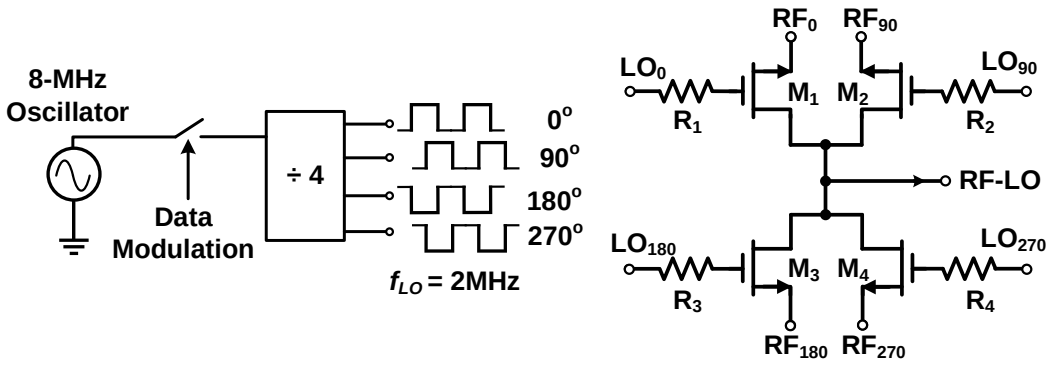


Figure 3-6: Schematic of the 260-GHz passive SSB mixer.

the power consumption. Shown in Fig. 3-6, the 2-MHz quadrature LO signals of the mixer are from an 8-MHz on-chip oscillator cascaded by a divide-by-4 static frequency divider[2]. The phases of the RF and LO signals of the MOSFETs are arranged in the way that at the central current-summing node, the lower-sidebands of all branches add up constructively, while the upper-sidebands cancel. MOSFETs in 65-nm bulk CMOS process have poor switching performance at THz; although wider channel provides smaller ON-resistance, there is also stronger coupling of THz signal from the channel to the LO wire through the gate-channel capacitance. To block such coupling, a set of 1.5-kΩ resistors ($R_1 \sim R_4$ in Fig. 3-6) are added in series with the transistor gates, which improves the mixer insertion loss from 15.5 dB to 13.5 dB in the simulation. Lastly, the OOK uplink modulation is realized by a data-controlled gating of the LO signals.

Shown in Fig. 3-5a, microstrip TL_1 lines combine the drain nodes of the MOSFETs and TL_2 is used to assist the impedance matching to Feed 3 of the antenna. But TL_2 falls short to provide ideal transformation and the limited space (due to the presence of the balun) hinders the placement of additional matching network components. This impedance mismatch leads to an insertion loss of 2 dB from the mixer to antenna Feed 3.

The simulated differential impedance of the whole backscattered module is very

[2]Although a divide-by-2 operation for a 4-MHz signal also provides the 2-MHz quadrature LO signal, the additional availability of LO phases (e.g. 45°, 135°, 225°, 315° in Fig. 3-6) provided in our divide-by-4 scheme is utilized to demonstrate the beam-steering of uplink wave.

close to the desired 150 Ω (see Section 3.1) without any additional matching network. If necessary, the impedance matching can be fine tuned by controlling the lengths (L_a and L_b, see Fig. 3-4a) of the transmission lines connecting the balun to the antenna and coupler, respectively. The simulated common-mode impedance of the backscattering module is largely capacitive (4.2-347.4j Ω). The small real impedance ensures that the radiation efficiency for uplink signal is not affected by the loading at Feed 1.

In Fig. 3-7, we show the eletromagnetic-circuit co-simulation results of the entire backscatter module. An overall conversion loss of 18 dB (including the 2-dB impedance mismatch loss) is achieved at f_{RF}=260 GHz, at the expense of zero static DC power. The conversion loss should be improved with more advanced CMOS technologies. The module also effectively suppresses the components at $f_{RF}+f_{LO}$ and $f_{RF}\pm 2f_{LO}$. The component at $f_{RF}+3f_{LO}$, due to its constructive summation at the mixer output node, appears at the output spectrum, with 10-dB rejection ratio. In the future, this may be improved by adopting a polyphase N-path mixer structure. Also note that the phase noise of the backscattered signal, being the sum of the RF and LO phase noise, is not deteriorated by the ultra-low-power tag LO; because the simulated tag LO phase noise is still smaller than that of the RF signal, due to the large difference between the two signal frequencies (i.e. 2 MHz versus 260 GHz).

3.3 THz Downlink Circuits

For the de-modulation of the 260-GHz OOK downlink signal, a THz square-law detector is used to first rectify the input to baseband, then a low-power amplifier is used to boost the baseband signal to a few hundred mV, so that the subsequent digital circuits can operate reliably (Fig. 2-1).

3.3.1 THz Square-Law Detector

To achieve zero DC power and low flicker noise, our 260-GHz square-law detector is based on a 2.4μm/65nm NMOS device with zero drain bias. Similar to other FET-

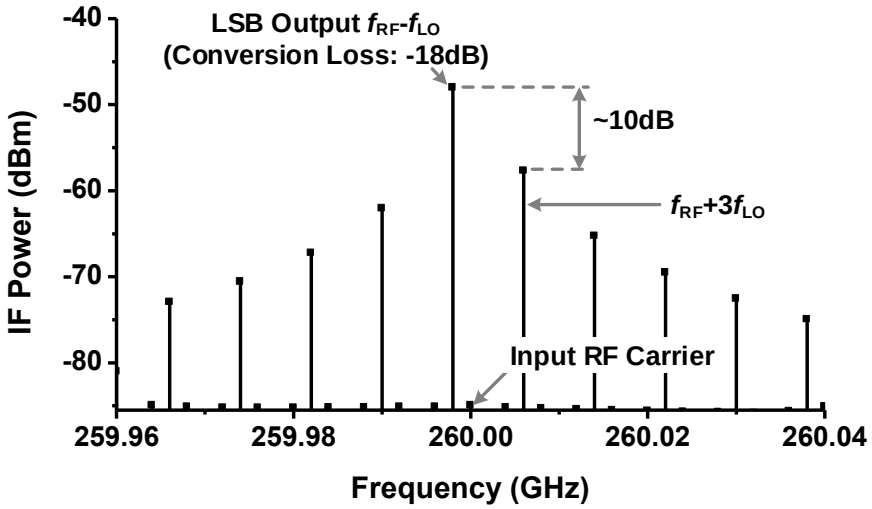


Figure 3-7: Simulated output spectrum of the THz backscatter module with a -30-dBm RF input (f_{RF}=260 GHz) and quadrature LO signals at f_{LO}=2 MHz.

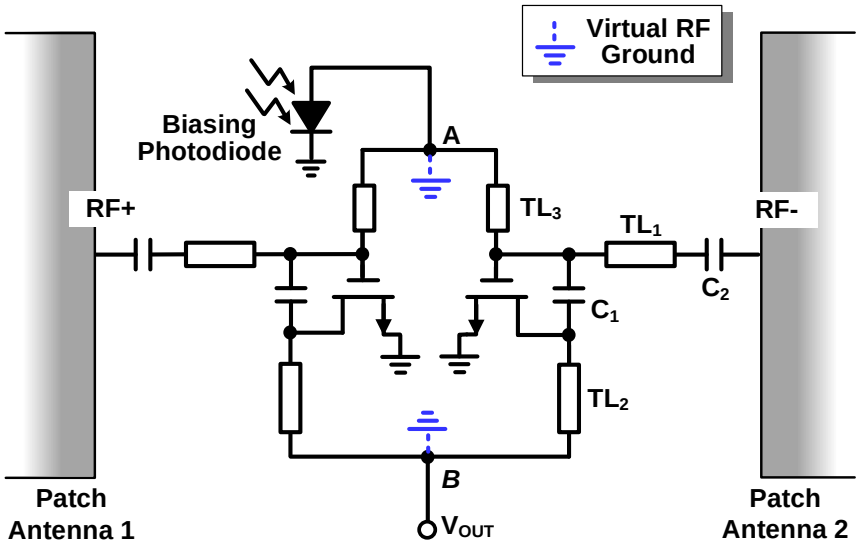
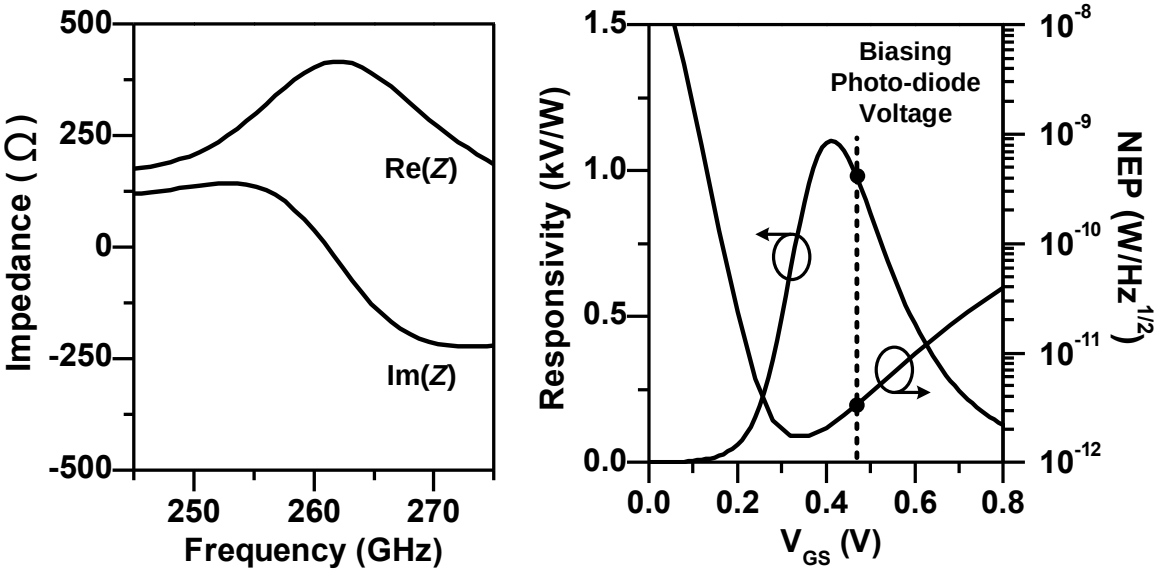


Figure 3-8: Schematic of a photovoltaically-biased THz square-law detector pair.

based THz detectors [16, 21], the optimal responsivity and noise-equivalent power (NEP) occur at a gate bias around the threshold voltage V_T of the transistor. Conventional VDD-powered circuits, due to the tag's energy harvesting operation, has large bias voltage fluctuation. Fortunately, in our CMOS process, the threshold voltage ($V_T \approx 0.4$ V) is close to the light-insensitive, open-circuit voltage of a P-N photodiode ($V_{PD} \approx 0.47$ V). Therefore, a simple photovoltaic-biasing circuit shown in Fig. 3-8 is adopted. Next, I note that any THz-power leakage to the biasing photodiode and detector baseband output should be avoided. To this end, a dual-detector scheme shown in Fig. 3-8 is used, which utilizes the property that the THz downlink signals extracted respectively from the adjacent edges of two patch antennas (see Fig. 2-1) are differential. As a result, in the symmetric circuit topology in Fig. 3-8, virtual RF grounds are formed at Node A and B. Furthermore, TL_2 and TL_3 are quarter-wavelength transmission lines; they transform the virtual ground to high impedances at the drain and gate of the MOSFET and therefore, highly confine the THz wave within the device. It is noteworthy that since the two differential THz inputs carry the identical OOK envelope, the baseband output from the two MOSFETs is in-phase, and is therefore combined and extracted at Node B.

In Fig. 3-8, C_1 ($\sim$50 fF) creates an AC short and therefore facilitates THz self-mixing in the diode-connected MOSFET. C_2 ($\sim$15 fF) provides DC isolation from the uplink backscatter module, and together with TL_1 (0.35λ) forms a matching network to present an impedance that is derived in Section 3.1 for equal power splitting. The insertion loss of matching network is 1 dB. $TL_1 \sim TL_3$ are 75 Ω coplanar-waveguide (CPW) transmission lines implemented using M9 layer. As shown in Fig. 3-9a, the simulated overall impedance of the detector circuit is close to the desired impedance value of 450 Ω. Lastly, Fig. 3-9b shows that, at the photodiode bias voltage of $\sim$470 mV, the simulated responsivity and noise equivalent power (NEP) are 1 kV/W and 32 pW/Hz$^{1/2}$, respectively. Note that the NEP is limited by the channel thermal noise of the transistor. The noise voltage from the photodiode, calculated in Appendix, is small, and does not transfer to the transistor output, given that the transistor is in the triode mode.



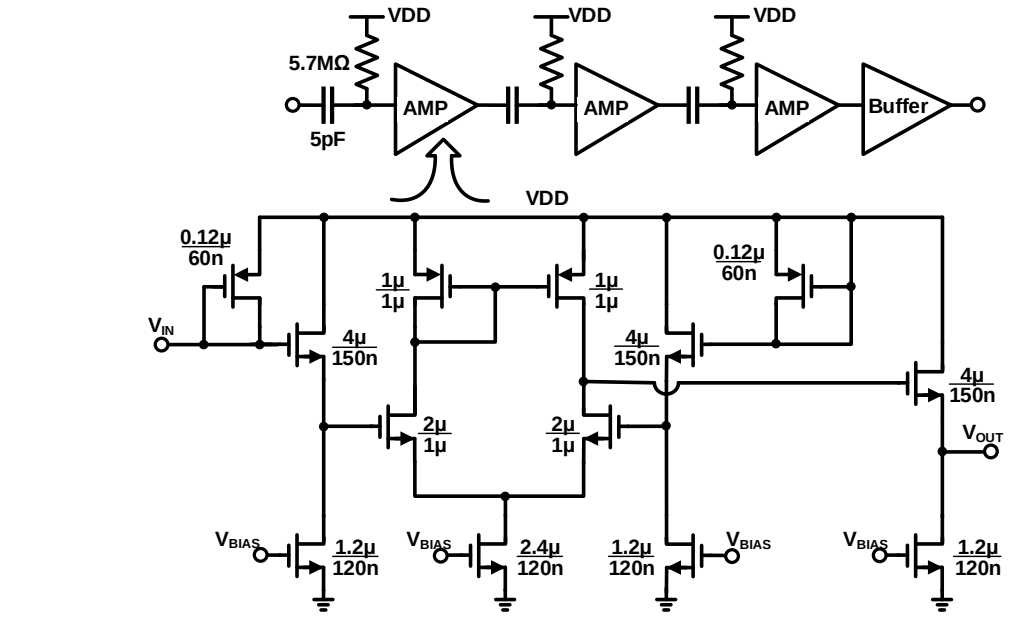
(a) (b)

Figure 3-9: (a) Simulated impedance of the detector presented to Feed 2 of the antenna. (b) Simulated responsivity and NEP of the detector.

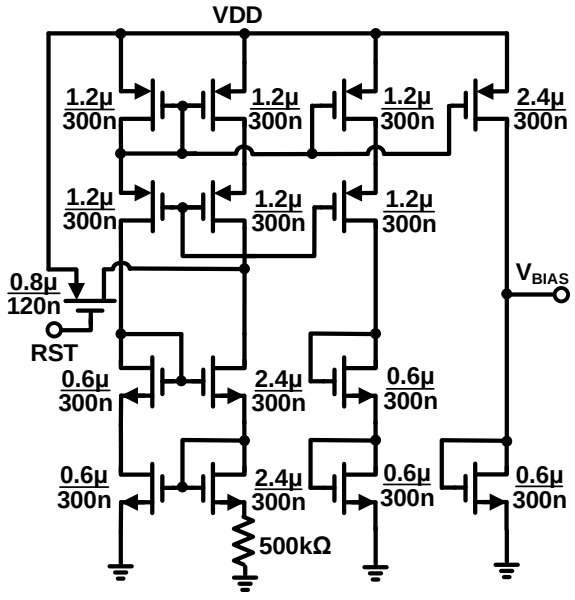
3.3.2 Ultra-Low-Power Amplifier

Shown in Fig. 3-10a, the demodulated signal from the detector is injected into a chain of amplifiers through a high pass filter. The filter, consisting of a 5 pF capacitor and a 5.7 MΩ resistor, has a low cut-off at 5 kHz, and provides not only the input bias of the amplifier but also DC isolation from the THz detector. The amplifier consists of three stages and two inverting buffers, and are separated by the same high-pass filters; this way the inevitable amplifier offset due to PVT variations and layout asymmetry is not amplified and saturate the circuits near the amplifier output.

Each amplifier stage consists of an input NMOS differential pair, which is preceded and followed by source-follower stages acting as voltage shifters. To save power, all amplifier stages are biased in the sub-threshold regime. The bias voltage V_{BIAS} in Fig. 3-10a is generated from a cascode constant-g_m circuit (Fig. 3-10b). A reset signal *RST* from the tag's DC-DC converter is used to ensure that the biasing circuit jumps from an undesired meta-stable state to the normal state, when *VDD* ramps up to ∼1 V. As shown in Fig. 3-10c, the simulated gain and the input-referred noise of the amplifier chain are 80 dB and 21 nV/Hz$^{1/2}$, respectively. The whole amplifier-buffer



(a)



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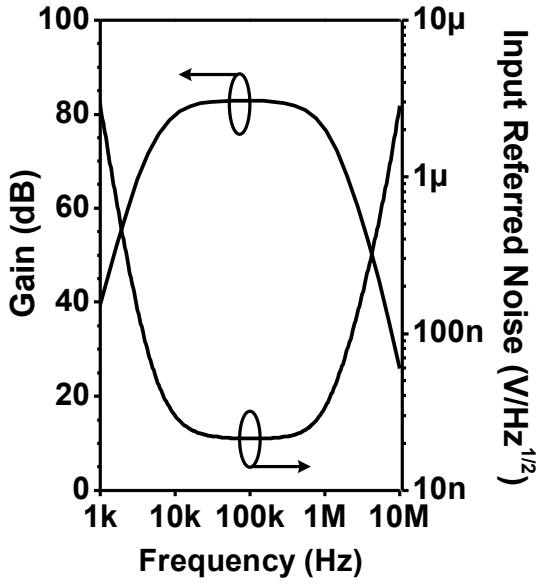


(c)

Figure 3-10: The ultra-low-power amplifier in the tag downlink: (a) the schematic of the main amplifier chain, (b) the cascode constant-g_m bias generation circuit, and (c) the simulated voltage gain.

chain, including the biasing circuit, consumes only 1.5 μW.

The high gain is to ensure reliable toggling of subsequent digital circuits. It, however, also amplifies the noise, so when the THz detector is idle, the amplifier output has a low but non-zero probability of falsely toggling the succeeding digital buffer. To mitigate its impact, before taking any downlink message, the on-chip processor always first validates a 16-bit preamble in front of the message. When the THz detector outputs normal data in the downlink mode, the amplifier output level is sufficiently far away from the digital trigger threshold, and the noise impact is suppressed.

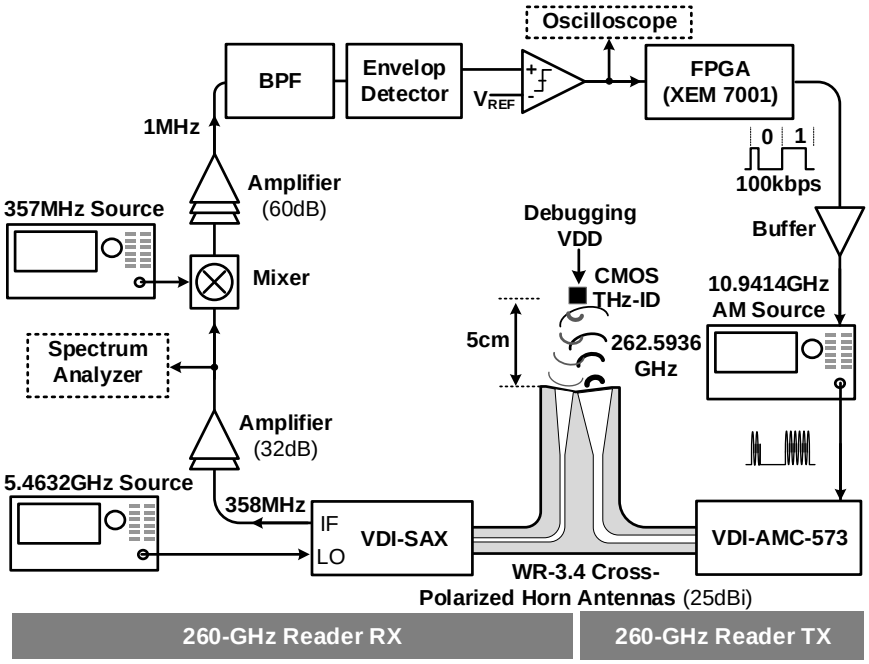
Chapter 4

Experimental Results

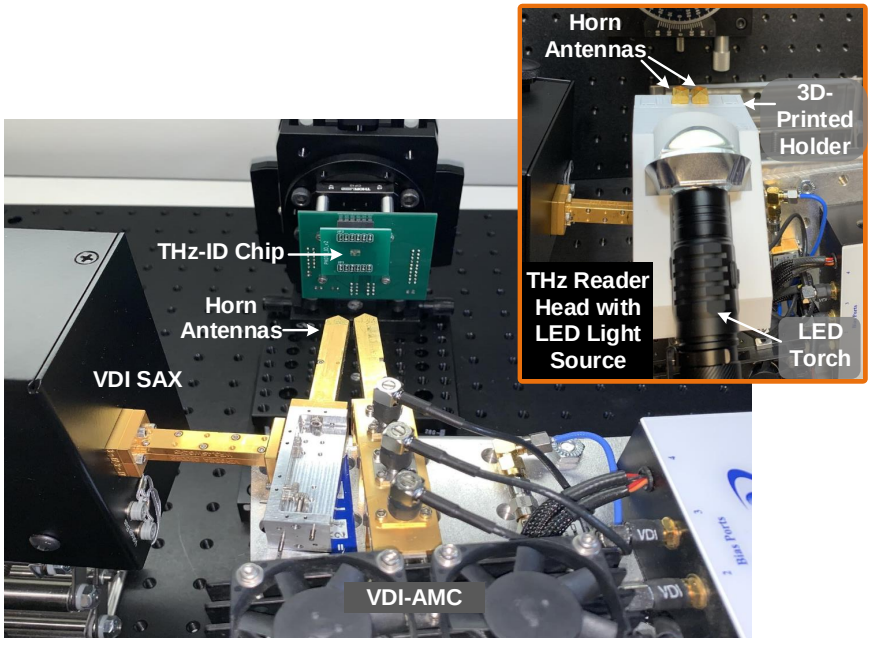
4.1 Measurement Setup

A custom-designed THz-ID reader is constructed, as shown in Fig. 4-1a. It communicates with the chip at a distance of 5 cm using two WR-3.4 horn antennas. The antennas are placed in the way that their *E*-planes are orthogonal to each other, in order to match the cross-polarizations of the THz-ID antennas (Fig. 3-1). For the reader-to-tag downlink, an amplifier-multiplier chain (AMC) from Virginia Diodes Inc. (VDI) is used, which converts a 10.9414-GHz input signal to a 20-dBm output at 262.5936 GHz. The input of the VDI AMC is OOK modulated by the 100-kbps data generated from a FPGA board (XEM 7001). According to the Friis formula [8], the power impinging on the THz-ID chip is about -5 dBm.

For the tag-to-reader uplink, a VDI spectrum analyzer extender (SAX) mixes the tag-backscattered signal with the 48^{th} harmonic of its 5.4632-GHz LO, and downconverts to 358 MHz. The signal is then amplified by 32 dB and observed on a spectrum analyzer. To close the communication loop, the signal is also further downconverted to 1 MHz, amplified by 60 dB and bandpass filtered. Finally, an envelop detector cascaded by a comparator recovers the 2-kbps data and feeds to the FPGA (Fig. 4-1a). Fig. 4-1b shows the photograph of the setup. The THz-ID reader head also includes an illumination source, which consists of a CREE XP-L-V6 LED and a lens that converge the light to $\sim$1 cm^2 spot on the PCB. The chip PCB is mounted on



(a)



(b)

Figure 4-1: (a) Diagram of the testing setup. Note that when light powering is used, the debugging VDD is disconnected. (b) Photos of the testing up with and without a LED torch for photovoltaic powering of the CMOS chip. The power electronics inside the LED torch, which generates large switching noise, is by-passed in the setup.

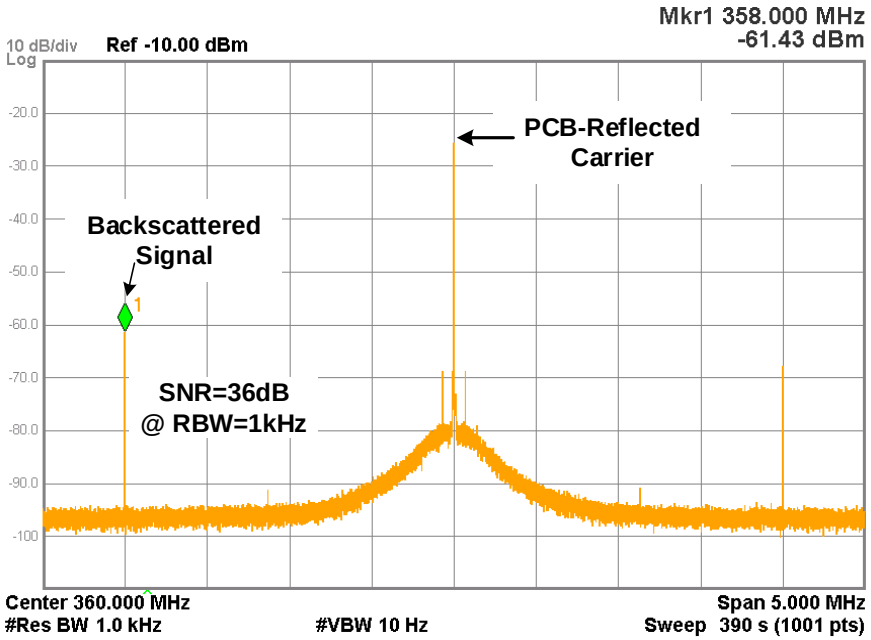


Figure 4-2: Measured spectrum of the backscattered signal

a rotational stage, which is used for the beam-steering measurement. In the uplink and downlink modes, the tag consumes 13 μW of power; that includes 4 μW of static leakage power of the digital circuits. In the most power-hungry security mode, the power consumption rises to 21 μW.

4.2 Characterization of the Circuits

4.2.1 Back-scatter Module

To characterize the 260-GHz backscatter module in a basic continuous-wave mode, the chip is externally powered and clocked (at f_{LO}=2 MHz) via the debugging pads. With the incident wave generated by the VDI AMC, a down-converted spectrum shown in Fig. 4-2 is obtained from the VDI SAX. The tone at 358 MHz is the expected signal backscattered by the THz-ID. It has a *SNR* of 36 dB at 1-kHz bandwidth, indicating the feasibility of an uplink with the designed 2-kbps data rate. The tone at 362 MHz is the upper-sideband image due to the limited image rejection (∼10 dB) of the SSB mixer in the tag. The central tone at 360 MHz is the reader-generated 262.5-GHz

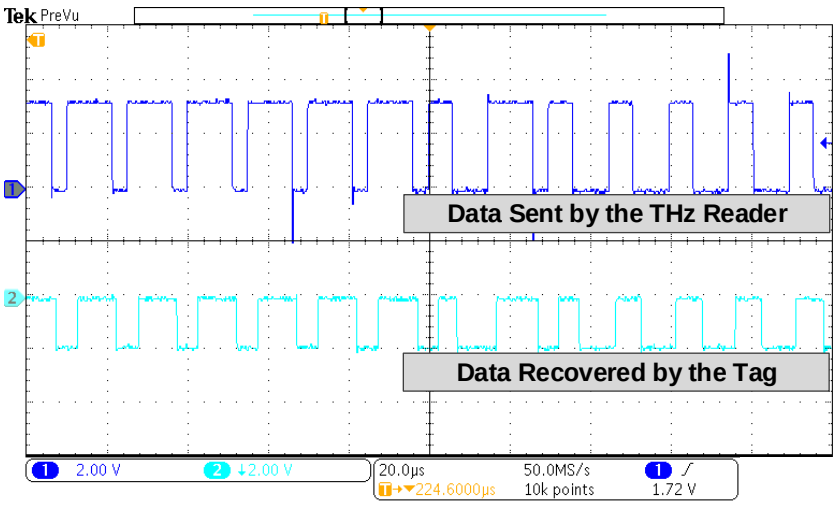


Figure 4-3: Measured downlink wavefrom from the tag.

signal directly reflected from the chip and its surroundings. Note that although this signal is already attenuated by ∼>20 dB due to the cross-polarization of the reader antennas, it is still >30 dB higher than the tag-backscattered signal in Fig. 4-2. That in turn justifies our backscatter scheme using cross-polarization and frequency shifting. The scheme ensures that the phase noise of the directly-reflected signal is below the reader's thermal noise floor, hence does not degrade the uplink *SNR*. The scheme also avoids the saturation of the reader's baseband amplifier caused by the undesired reflected tone with large power.

4.2.2 Downlink circuits

With OOK modulation to the VDI AMC, the tag downlink output is measured via a debugging pad. Pulse-width modulation is adopted for the encoding of the system, where duty cycle <45% represents bit 0 and >55% represents bit 1. In our measurement setup, the reader uses 40% duty cycle for bit 0 and 75% for bit 1. The results in Fig. 4-3 indicate that the tag downlink correctly recovers the original data created by the FPGA in the THz reader (Fig. 4-1a). To achieve the gate bias of the downlink MOSFET detector, ambient lighting is found to be sufficient in the testing.

4.2.3 Tag's beam-steering

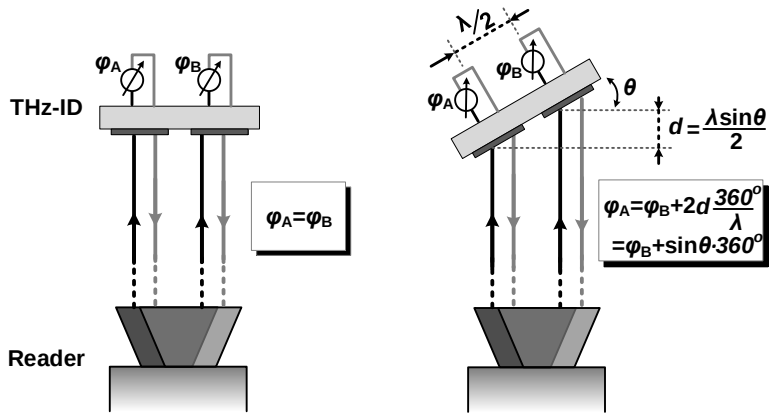
Next, we test the beam-steering capability of the THz-ID chip. Note that it is different from conventional beam-steering of phased arrays, due to the unique back-scattering operation of the chip, and the co-location of the reader's transmitter and receiver. Shown in Fig. 4-4a, the goal of the beam-steering of this tag is to ensure that when the chip does not face the reader perpendicularly, its backscattered wave can still be re-directed towards the reader. Fig. 4-4a indicates that, with a chip tilting angle of θ and on-chip antenna spacing of $\lambda/2$, the following phase gradient (in degree) should be applied in order to compensate the total propagation-path difference related to the waves handled by the two patch antennas:

$$\varphi_A - \varphi_B = 2 \cdot (\frac{\lambda}{2} \sin\theta) \cdot \frac{360^\circ}{\lambda} = (\sin\theta) \cdot 360^\circ \tag{4.1}$$

This is verified in our experiment, where the LO phase of each THz SSB mixer is digitally controlled by the on-chip processor. Fig. 4-4b shows the backscatter-wave power, which is received by the reader in the measurement, at varying chip tilting angle θ. Two tag phase-gradient settings requested by the reader, φ_A=φ_B and φ_A-φ_B=180°, are tested. The measured peak responses of the reader occur at θ=0° and θ=30°, respectively, which well agree with (4.1). This also shows that the maximum beam-steering angle (in both azimuth and elevation directions) is ±30°. It should be noted here that, when an antenna is tilted, the effective aperture decreases by a factor of $\cos\theta$. At θ=30°, ∼1.2 dB two-way power loss should occur. However, in the measurements we received almost the same peak power in both settings. This can be attributed to either a better alignment in Setting 2 or measurement error.

4.2.4 Protocol and Energy-Harvesting

I also verified the protocol with an external power and the tag internal clock (Fig. 4-5a). When the reader receives the tag's beacon message, the FPGA starts a feedback loop to request a change of uplink beam angle until the *SNR* is maximized. The measured waveforms associated with this operation are shown in Fig. 4-5b. Then the



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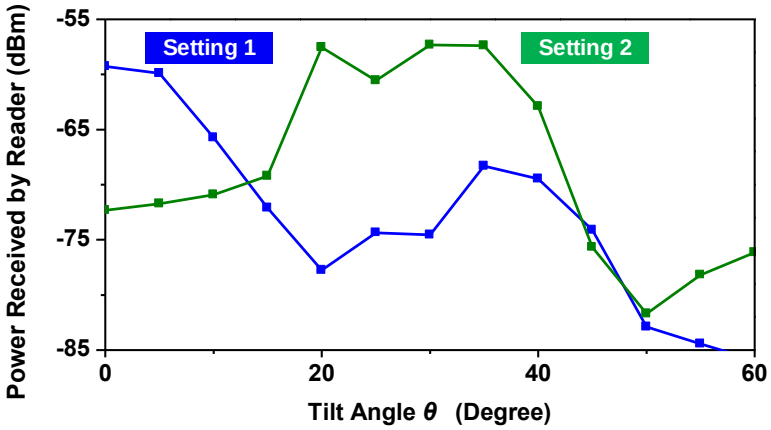
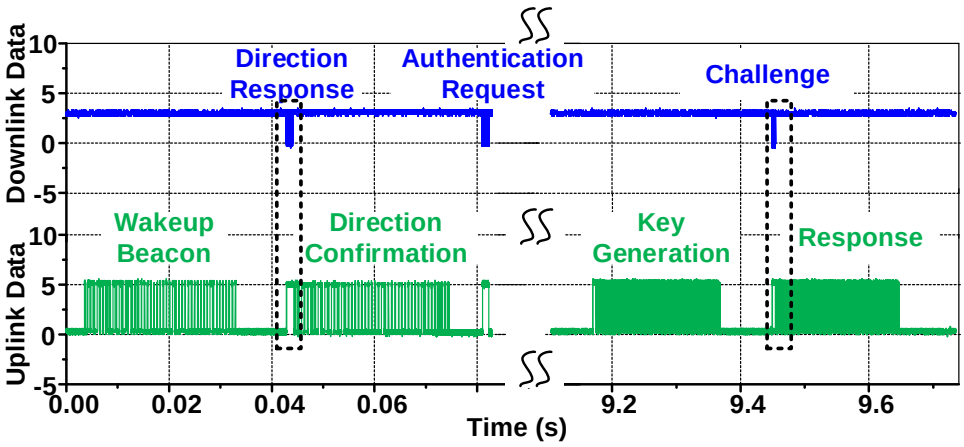
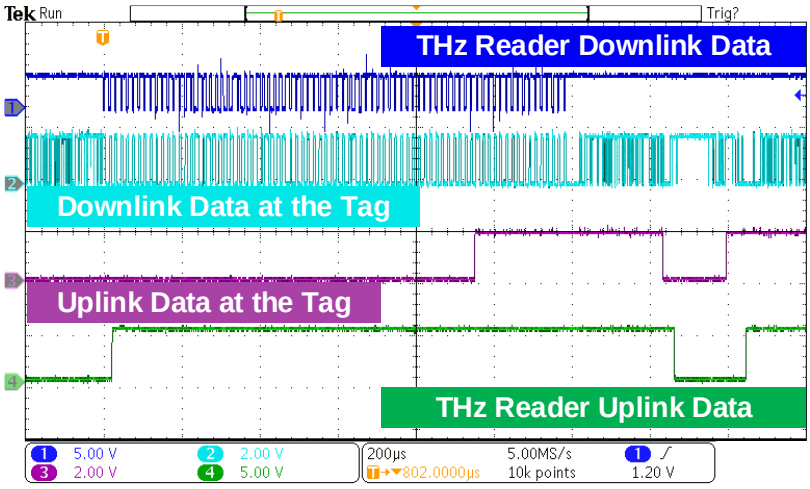


(b)

Figure 4-4: (a) Phase-shifting (φ_A-φ_B) conditions in the tag to ensure that the backscattered wave points to the reader when the tag is tilted by θ. (b) Measured backscattered-wave power, which is received by the reader, at different chip tilting angle θ. Here, two digital settings of φ_A-φ_B are applied.



(a)



(b)

Figure 4-5: (a) Measured downlink and uplink data in the protocol. Zoom-in views of dotted regions representing the phases of (b) direction response and confirmation.

reader sends a trigger to the chip to start the authentication process. In Fig. 4-5b, when THz reader is transmitting data, tag's downlink circuit recovers exact same data and during idle time random output pulses are observed, as explained in Section 3.3. Due to the preamble validation in the processor, those random pulses are rejected.

Lastly, with external LED illumination and photodiode powering, the time-domain behavior of tag, measured via the power supply pads, is shown in Fig. 4-6. The high-frequency fluctuations on V_{OUT} lines after the output voltage reaches $\sim$ 1 V indicates that the on-chip processor is activated. In Fig. 4-6, the chip is entirely power-autonomous and interrogated by the THz reader. It can be seen that, when

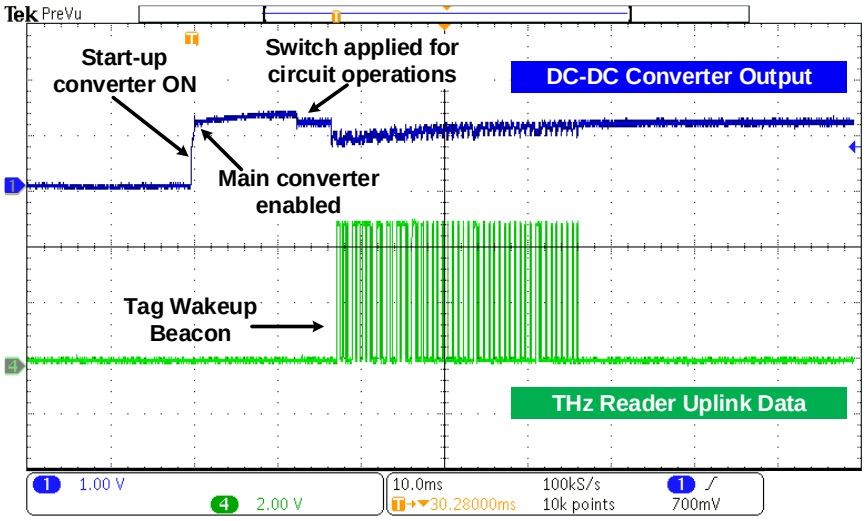


Figure 4-6: Measured startup behavior of THz-ID with optical powering.

the converter-startup is completed, the on-chip processor sends a tag-wakeup beacon signal through its 260-GHz backs-catter uplink, and the signal is successfully received and recovered by our reader. Since the downlink amplifier consists of transistors operating in the sub-threshold regime, the large photoelectric effect causes bias drift of the amplifier and excessive noise, which prevents the completion of the entire security protocol in the test. The static current of the processor also increases with the illumination. In the future development iterations, we should be able to optically power the complete protocol by enclosing the downlink and processor circuitry with a cover formed by the Al-pad layer and sidewalls formed by M1-to-Al stack.

Chapter 5

Conclusions and Future Works

In this thesis, I demonstrate a new application of THz CMOS electronics, which utilizes its advantages in compact size and packageless chip integration. It also show that silicon THz transceivers, which are long considered to be power hungry, can be applied in ultra-low-power systems, if a backscattering communication scheme is adopted. Our presented tag is built entirely on a low-cost CMOS chip, and is around 3× smaller than the smallest package-less, far-field chip reported previously [28]. It also offers multi-antenna beam-steering functionality for the first time in RFIDs. It uses pulse width modulation (PWM) and amplitude shift keying (ASK) with 100% modulation index. The uplink and downlink data rates are 2kbps and 100kbps, respectively and has been demonstrated at a distance of 5cm. The tag employees a security processor with peak power consumption of 21μW.

The presented work demonstrates the feasibility of ID tags with ultra-small size and cost, which is expected to empower a wide range of new applications in manufacturing, logistics, anti-counterfeiting, and so on. To fully make these applications practical, a few more technologies should be developed. For example, to allow for embedding of the tag inside opaque materials, energy harvesting directly from the THz wave is desired. That requires high-speed rectifier devices in CMOS process. To this end, the poly-gate-separate Schottky diodes in CMOS, which have ∼2-THz cutoff frequency and are used in THz imaging [11], could possibly meet the above needs. Secondly, although the size and cost requirements for the THz-ID reader, compared to

the tags, are much more relaxed, it is still highly preferred that the reader front-end is implemented using silicon integrated circuits. Rapid advances are being made in this area [32]. For example, in [7], the 200-to-255-GHz power amplifier using 130-nm SiGe BiCMOS process (f_{max} ≈500 GHz) is already capable of generating 20 mW of power, which is only 7 dB away from the VDI AMC used in our tag reader. In light of recent developments of high-speed and high-power SiGe and CMOS processes [12, 17, 18, 22] with up to 720-GHz f_{max} and up to 7.1-V breakdown voltage, achieving radiation power of 100 mW in the sub-THz regime is no longer unimaginable. These devices can also works as high-speed rectifier devices for efficient energy harvesting at THz band. Thus, in future a true THz-ID is realizable.

Appendix A

Noise Voltage of An Open-Circuit Photodiode Under Illumination

In the downlink THz MOSFET detector (Fig. 3-8), an open-circuit photodiode under illumination is used to provide the gate bias of the transistor. The net output current of the photodiode, although is zero, should be treated as the sum of two opposite current flows [29]. One is the photocurrent I_p generated by the illumination, and the other is the diffusion current I_d due to the forward bias of the diode:

$$I_d = -I_p = I_0(e^{\frac{V_0}{V_t}} - 1), \tag{A.1}$$

where I_0 is the reverse saturation current of the p-n junction, V_t is the thermal voltage (V_t=kT/q ≈26 mV at 300 K), and V_0 is the open-circuit photodiode voltage. The respective noise fluctuations associated with the above currents are uncorrelated, so the total equivalent noise current power spectral density of the device is [9, 29]:

$$\tilde{i_n^2}/\Delta f = 4q(|I_p| + I_0) \approx 4q|I_p|. \tag{A.2}$$

The open-circuit noise voltage of the photodiode is then considered to be the

product of (A.2) and the diode differential resistance at the bias (R_d=$V_t/|I_p|$):

$$\tilde{v_n^2} = \tilde{i_n^2} \cdot R_d^2 = 4q|I_p| \cdot \left(\frac{V_t}{|I_p|}\right)^2 \Delta f = 4q\frac{V_t^2}{|I_p|}\Delta f = 4kTR_d\Delta f \tag{A.3}$$

Interestingly, the generated noise is the same as thermal noise of a resistor equal to R_d of the photodiode, and decreases with larger illumination. Hence, its noise contribution to the output noise voltage of the MOSFET detector in Fig. 3-8 is:

$$\tilde{v}_{n,det}^2 = g_m^2 \cdot \tilde{v_n^2} \cdot r_{ds}^2 = g_m^2 r_{ds}^2 \cdot 4kTR_d\Delta f, \tag{A.4}$$

where g_m and r_{ds} are the transconductance and output resistance of the MOSFET. Note that (A.4) is much smaller than the MOSFET's own channel thermal noise ($\tilde{v}_{n,ch}^2 = 4kTr_{ds}\Delta f$): for the MOSFET biased in the triode mode (Fig. 3-8), the simulated g_m and r_{ds} are 1.4 μS and 7.7 kΩ, respectively, and I_p in normal tag operation is $\sim$0.1 μA (hence $R_d\approx$260 kΩ). Therefore, $\tilde{v}_{n,ch}$ is $\sim$11 nV/Hz$^{1/2}$, while $\tilde{v}_{n,det}$ in (A.4) is $\sim$0.7 nV/Hz$^{1/2}$.

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