Self-Align-Gated GaN Field Emitter Arrays Sharpened by a Digital Etching Process

Self-Align-Gated GaN Field Emitter Arrays Sharpened by A Digital Etching Process

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***Abstract*— Field emitters are attracting much attention recently because of their potential for high-frequency and harsh-environment applications. Although silicon is the most studied semiconductor for field emitters, III-Nitrides are also very promising thanks to their tunable electron affinities. Two main challenges exist for low turn-on-voltage III-Nitrides field emitters: lack of a self-aligned gate and tip-sharpening technologies. In this work, we demonstrate self-aligned-gated GaN field emitter arrays whose tips are sharpened by a wet-based digital etching technology. This technology allows to reduce the tip size from 40 nm down to 20 nm. Gated GaN field emitters with a turn-on voltage ($V_{GE,ON}$) of 20 V and current density of 150 mA/cm^2 at V_{GE} = 50 V have been demonstrated.**

***Index Terms*— digital etching, field emitter arrays, GaN**

I. Introduction

FIELD emitters (FE), a vacuum transistor based on field emission phenomena, are excellent candidates for harsh-environment and high-frequency electronics thanks to their radiation hardness and scattering-free electron transport [1]. Among different materials used as FEs, silicon is one of the most well-developed [2]–[5]. To reduce operation voltage in FEs, sharp tips and reduced gate-emitter distance are needed. Si FEs with a sub-10 nm tip radius and self-aligned gate have demonstrated sub-20 V turn-on operation [3]. To further improve FEs, III-Nitrides are promising thanks to their tunable electron affinities [6], [7]. A low electron affinity helps to enhance the electron tunneling from the semiconductor to vacuum. Electron affinities of III-Nitrides such as AlGaN can be reduced by increasing the Al ratio [6] or by changing the surface polarity from metal-polar to N-polar [7].

Despite their potential, most GaN field emission devices reported in literature so far have a turn-on voltage larger than 100 V due to the limitation of two-terminal geometries and relatively wide tips [8]–[21]. A planar-type GaN field emitter with a 20-nm tip radius and a 30-nm collector-emitter gap was recently reported with a turn-on voltage of 1.8 V [22]; however, its two terminal structure lacks gain and limits its functionality to a diode-like behavior. In our prior work, GaN vertical nanowire (NW) field emitter arrays (FEA) with a self-aligned gate were demonstrated with a reduced turn-on voltage of 27 V and maximum current density of 14 mA/cm^2 [23]. In this work, GaN FEAs with enhanced performance are reported thanks to the use of a new digital etching (DE) technology and an improved epitaxial structure. By sharpening tips down to 20 nm, the turn-on voltage can be reduced to 20 V. Moreover, the current density is enhanced to 150 mA/cm^2 by reducing the resistance in the epitaxial structure.

This work was supported by the AFOSR/MURI, grant no. FA9550-18-1-0436. Fabrication was performed in MTL and NSL in MIT.(Corresponding authors: Pao-Chuan Shih; Tomás Palacios.)

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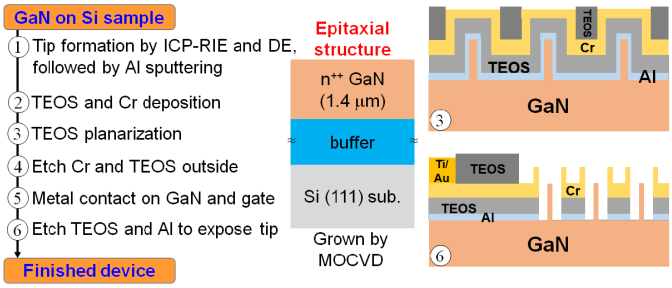

Fig. 1. Process flow, epitaxial structure, and the device geometry after the 3rd and final steps.

II. Device Fabrication

GaN FEs are fabricated on a GaN-on-Si wafer grown by Enkris Semiconductor, Inc. using metal organic chemical vapor deposition (MOCVD). The structure consists of a 1.4 μm n^{++}-GaN (Si: 1 $\times$ 10^{19} cm^{-3}) layer on a 1.4 μm buffer layer grown on the Si substrate. The process flow for the self-aligned-gated GaN FEA is summarized in Fig. 1.

The fabrication starts with (1) tip formation. Emitters are defined by electron-beam lithography with Ni lift-off and following Cl_2/BCl_3-based Inductively Coupled Plasma-Reactive Ion Etching (ICP-RIE). After this etching process, GaN nanopyramids with tip size of about 40 nm and height of 300 nm are formed. After the Ni mask is removed, the GaN nanopyramids are sharpened by a wet-based digital etching (DE). Conventional oxygen-plasma-based DEs are anisotropic and they do not sharpen vertical tips [24], [25]. Furthermore, the use of a biased plasma could potentially damage tips. Therefore, we developed a new wet-chemical-only DE. The sample is firstly oxidized by a mixture of H_2SO_4 and 30% H_2O_2 with a ratio of 1:1 for 4 mins and is then rinsed with

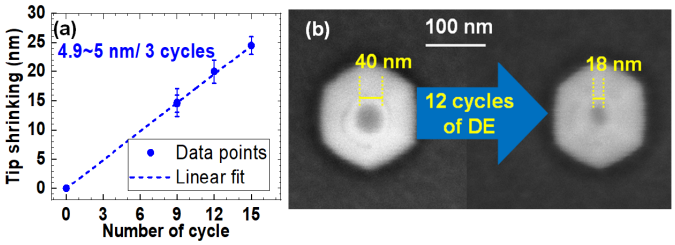

Fig. 2. (a) Tip sharpening vs. cycles of DE and (b) SEM images of a tip before and after DE. Each data point in (a) has 8 tips' results.

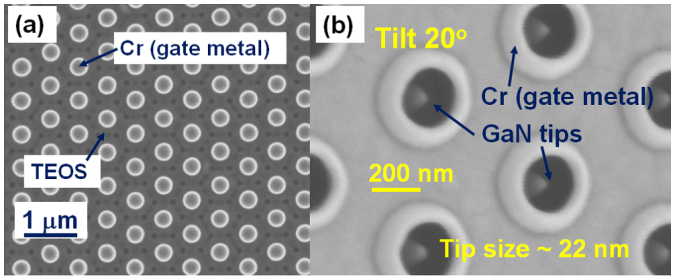

Fig. 3. Top-view SEM images of (a) device after planarization and (b) finished device.

DI water. After that, the oxidized layer is removed by dilute HCl (HCl : H_2O = 1 : 3) for 2 mins followed by a DI water rinse. This cycle is repeated as many times as needed. Every 3 cycles of DE, the mixture of H_2SO_4 and H_2O_2 is renewed. The results and scanning electron microscope (SEM) images of the resulting tips are shown in Fig. 2. The tip is shrunk by about 5 nm after 3 cycles of DE, and sub-20 nm tips have been achieved by this new DE technology.

After DE, a thin layer of Al is sputtered to protect GaN tips. (2) The gate stack is then formed by plasma enhanced chemical vapor deposition (PECVD) of 200 nm Tetraethyl orthosilicate (TEOS) and sputtering 80 nm Cr as gate metal. Once the gate stack is deposited, (3) the device is planarized by thick TEOS deposition followed by a timed CF_4-based RIE to expose the top surface of the gate metal. (Fig. 3 (a)).

After planarization, (4) the gate metal is selectively etched by Cl_2-based ICP-RIE with TEOS as a hard mask. The gate is self-aligned to the emitter tips without the need of lithographical alignment. The TEOS layer on the contact region is removed by buffered oxide etchant (BOE) to allow for direct contact on GaN in the following step. Then (5) the metal (Ti/Au) is deposited on the Cr layer as gate pad metal, and on the n^{++}-GaN layer as source contact, (6) the tips are finally exposed by etching the TEOS with RIE and BOE and by removing Al with CD-26 developer. An SEM image of a finished GaN FEA is shown in Fig. 3 (b). It is noted that the tip width is a bit larger than the size right after DE. This issue needs further investigation in the future.

III. Results and Discussion

The fabricated GaN vertical FEA is measured in an ultrahigh-vacuum chamber with base pressure around 3×10^{-9} Torr. The measurement setup is illustrated in Fig. 4(a). The anode electrode is a suspended tungsten ball with 0.5-mm

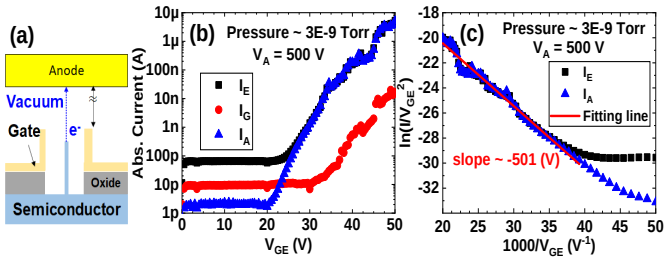

Fig. 4. (a) Measurement setup, (b) transfer characteristics, and (c) F-N plot of gated GaN vertical FEA.

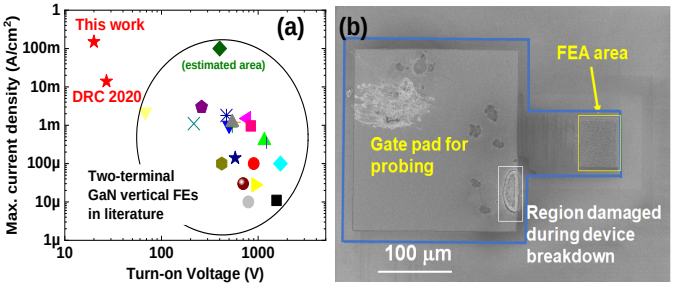

Fig. 5. (a) Benchmark of GaN vertical FEs [8]–[21] and (b) SEM image of the device after measurement. The blue lines in (b) indicate the whole GaN FEA device.

diameter and can be positioned on top of the measured GaN FEA. The gap between the anode and FEA is approximately 1 mm. When the emitters turn on, electrons will tunnel from the GaN tips into vacuum because of the strong electrostatic field induced by gate-emitter voltage (V_{GE}) and are then accelerated towards the anode if the electric field from the anode is strong enough.

After conditioning the self-aligned-gated GaN vertical nanopyramid FEA by sweeping V_{GE} several times, the transfer characteristics of this FEA are measured (Fig. 4(b)). This array consists of 100×100 GaN nanopyramids with a tip size of about 20-25 nm. In this work, the array is arranged in an hexagonal pattern and the distance between two nearby pyramids is about 600 nm. Based on SEM inspection, the gated emitter area is about $63\ \mu m \times 53.5\ \mu m$. The anode voltage ($V_A$) is fixed at 500 V during measurement. This FEA turns on at $V_{GE} = 20\ V$ when the anode current (I_A) starts increasing from the noise level. At $V_{GE} = 50\ V$, the maximum anode current is about $5\ \mu A$, which equals to a current density of 150 mA/cm^2. Moreover, the gate current (I_G) is only about 0.5% of the anode current at $V_{GE} = 50\ V$.

The Fowler-Nordheim (F-N) plot of this device is shown in Fig. 4(c). A negative-slope straight line indicates field emission is the dominant mechanism in the current conduction of this device. Based on the slope (b_{FN}) of 501 V, the gate-emitter field factor (β_{GE}) is $9.6 \times 10^5\ cm^{-1}$, obtained from the equation: $\beta_{GE} \approx \frac{0.95\times6.83\times10^7\times\phi^{1.5}}{b_{FN}}$, assuming the work function (ϕ) of n^{++}-GaN is 3.8 eV [7]. This equation is based on the Murphy-Good field emission equation [26] with an approximation proposed by Spindt *et al.* [27]. This field factor indicates how strongly the gate-emitter voltage controls the field emission; hence, high β_{GE} is preferred.

TABLE I
COMPARISON BETWEEN DIFFERENT SELF-ALIGNED-GATED FEAS [2]–[4], [23], [28]–[30].

Materials	Number of tips	$V_{GE,ON}$ (V) (@ I_A)	J_{max} (A/cm^2) (@ $V_{GE} - V_{GE,ON}$)	Slope b_{FN} (V)	Field factor β_{GE} (cm^{-1})	Reference
Si	50×50	22 V (@ 100 pA)	104 (43 V)	468	1.137×10^6	[2]
Si	1000×1000	19 V (@ 100 pA)	1.37 (31 V)	521	1.02×10^6	[3]
Si	7	25 V (@ 10 pA)	1.92 (35 V)	–	–	[4]
Mo	1.65×10^5	38 V (@ 10 nA)	0.085 (26 V)	917	7.35×10^5	[28]
Ti	32	55 V (@ 10 pA)	5×10^{-5} (55 V)	–	–	[29]
CNT	1280	44 V (@ 1 nA)	0.0019 (26 V)	–	–	[30]
GaN	50×50	27 V (@ 10 pA)	0.014 (33 V)	578	8.32×10^5	[23]
GaN	$\mathbf{100 \times 100}$	**20 V (@ 1 pA)**	**0.15 (30 V)**	**501**	$\mathbf{9.60 \times 10^5}$	**This work**

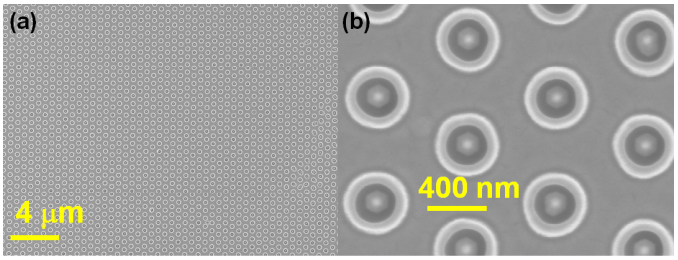

Fig. 6. (a) An overall SEM image and (b) a zoomed-in SEM image of the GaN FEA area after measurement.

The performance of this GaN FEA is compared with other GaN vertical FEs in literature (Fig. 5(a)) [8]–[21]. To the best of our knowledge, this presented device has the lowest turn-on voltage and the highest current density among GaN vertical FEs. Since the gate current is still 2 orders of magnitude lower than the anode current (Fig. 4(a)), it is expected that this device could provide more anode current if V_{GE} increases further. Unfortunately, the gate stack broke in subsequent measurements, causing the gate terminal to short with the n^{++}-GaN. The destroyed device was then investigated again by SEM (Fig. 5(b) and Fig. 6). There is no observable damage in the FEA area (Fig. 6), while there is a clear degradation of the gate stack near the large gate pad area. By increasing the oxide quality or its thickness under the gate pad region, the stability of this device is expected to be improved in the future. Furthermore, given that there is no observable damage in the FEA area under SEM inspection, this GaN FEA should be able to provide even higher anode current as V_{GE} is increased once that the early pad breakdown is resolved (Fig. 5(b)).

Our self-aligned-gated GaN vertical FEA is also compared with different non-GaN self-aligned-gated FEAs reported in literature (Table I) [2]–[4], [23], [28]–[30]. To make a fair comparison, we only list devices whose log-scale transfer characteristics are available for accurate turn-on voltage comparison. In literature, turn-on voltages are generally extracted as the voltage when the anode current starts increasing, and this value might be affected by noise floors in different measurement setups/systems. In spite of this uncertainty, it should be noted that the turn-on voltage ($V_{GE,ON}$) of our device is already comparable with state-of-the-art Si FEAs, though the tip width of our GaN FEA is still about 3× larger than Si FEAs [3]. By extracting out b_{FN}, the field factor (β_{GE}) can be estimated via the equation used above if we know material's work function. This field factor is mostly geometrically determined and can be used as an indicator for benchmarking different materials' FEAs. In FEAs, a higher β_{GE} indicates the device geometry is better for field emission applications since a reduced V_{GE} is needed to induce strong enough electric field at tips' surface. The field factor of our device is already comparable to the ones reported in other material systems because of the sharpened GaN tips achieved by this new digital etching technology. By using this new technology, GaN tips can be potentially sharpened even further to make them as sharp as Si tips. Thanks to their lower electron affinity, GaN FEAs can possibly provide better performance than Si FEAs. However, the maximum anode current density (J_{max}) of our device is still at least an order of magnitude lower than ones in the best Si FEAs.

In summary, self-aligned-gated GaN vertical FEA demonstrates competitive performance, and higher current density is expected if the low breakdown voltage of the gate-stack is solved. Further performance improvements are expected when applying the developed tip-sharpening technology to N-polar III-Nitrides and AlGaN-alloys. At the same time, field emitters with integrated anode are also currently investigated by different groups [29], [31]. To make circuits based on field emission devices, both low-turn-on-voltage device with low-electron-affinity materials and integrated anode are necessary.

IV. CONCLUSION

A self-aligned-gated GaN vertical FEA sharpened by a new wet-based digital etching process is presented. GaN tips are shrunk from 40 nm to sub-20 nm. Devices based on these tips have turn-on voltage of 20 V and current density of 150 mA/cm^2, which are the best among GaN vertical FEs and are competitive with state-of-the-art silicon self-aligned-gated FEAs. This performance demonstrates the great potential for further improvement in III-Nitride field emission devices.

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