A Basic Isolated Half-Bridge Silicon Carbide Gate Driver for Electric and Hybrid Electric Vehicles

by

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Submitted to the Department of Electrical Engineering and Computer Science
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Abstract

A Basic, Isolated, Half-Bridge Silicon Carbide Gate Driver was designed and validated using Cadence and SPICE. The architectures of similar gate drivers were studied and simplified to reduce the total area of the gate driver. The fabrication process was also carefully selected to minimize the total area. The gate driver architecture consisted of various analog and mixed signal subcircuits including floating voltage rail generators, inverter chains, and an on-off key receiver among others. Extensive simulations were performed in SPICE and Cadence to analyze the gate driver behavior for various temperature conditions, operating voltages, load conditions, and process corners. The final product was able to drive 6 amps of peak output current, with 10 nanoseconds of propagation delay, and with a 2 milliamp quiescent current.

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I would also like to thank my family and friends for all of their support, especially Gloria, Joshua, and Viktor. Your love and faith in me brought me to this point. Thank you. I love you guys.

And of course, all the glory to God.

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Chapter 1

Introduction

With the popularization and proliferation of electric and hybrid electric vehicles comes the need for robust, small power electronics that can operate in extreme operating conditions. Because electric and hybrid-electric vehicles operate at high voltages and high temperature, materials that can better handle these conditions have become an interesting area of investigation.

Wide-bandgap materials are a promising avenue for this application space. These wide-bandgap materials are so named because their bandgap is larger than that of silicon. As a result, wide-bandgap materials like gallium nitride and silicon carbide can operate at higher operating frequencies, at higher temperatures, and at higher voltages [8] . They also have lower on-resistances which can help save on area as well as result in reduced loss and improved efficiency. For electric and hybrid electric vehicles, this makes power electronics made with wide-bandgap materials not only more performant, but also safer for commercial use.

Of course, these materials are not without drawbacks. Because the processing technology is relatively new, wide-bandgap materials do not have the same reliability data nor the same supply security as traditional silicon [7]. Therefore, fabrication processes that use wide-bandgap materials are also generally more expensive that those that use traditional silicon.

Between silicon carbide and gallium nitride, silicon carbide can work at even higher voltages (900-1200 versus 650 V) [8]. This makes SiC the wide bandgap material of choice for the electric vehicle market.

Nonetheless, with adoption from Tesla and other manufacturers [7], wide-bandgap materials and silicon carbide in particular are an exciting opportunity for the development of new power electronics for electric and hybrid electric vehicles.

Of the power electronics utilized in electric and hybrid electric vehicles, gate drivers form a small but critical part of the control circuitry. The gate drivers control the switching transistors of the power converters and inverters throughout the vehicles. Gate drivers need to be powerful enough to provide sufficient driving current to control the transistors. This output peak current varies for the intended application or specific vehicle but will fall somewhere within the four-amp to thirty-amp range [8].

For these applications with extreme operating voltages, one necessary feature is galvanic isolation. With the use of a transformer, signals can be kept intact while providing the isolation necessary for safety and for the protection of devices.

Additionally, the gate driver must be carefully timed. The gate driver should minimize the total propagation delay and the rise and fall times. The rise and fall times should be as symmetrical as possible. They should also be designed to ensure that there is no shoot-through current at the output.

Finally, the power consumption and total area should be minimized to ensure maximum efficiency and minimum fabrication cost.

The goal of this project was to design and validate a simple, performant gate driver

using a silicon carbide process technology. The gate driver needed to have around 6 amps of peak output current, less than 20 nanoseconds of propagation delay, and must minimize the total die area to minimize the fabrication cost. To accomplish this, various cost reduction strategies were used including the simplification of the gate driver architecture, careful process selection, and conceding to a higher power consumption.

Chapter 2

Previous Work

Various other gate drivers were studied to determine the architecture for this gate driver.

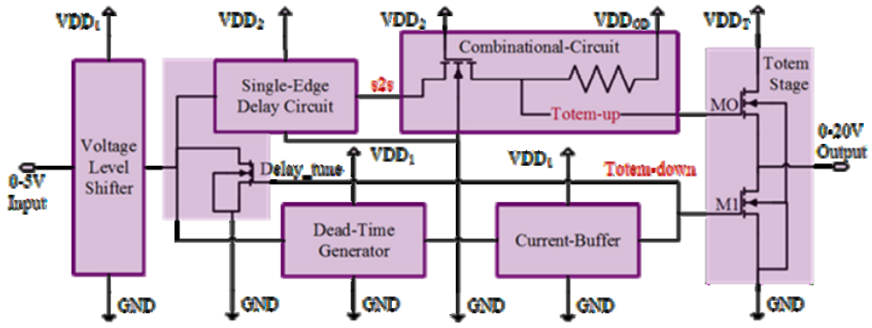
Other gate drivers often included several peripheral features that were omitted to reduce the total die area. Common additional features include protection features such as soft-start circuitry, Miller clamps, and fault protections [8]. Other common peripheral features include programmable features that enable temperature monitoring, specific voltage offsets, and additional timing control [1].

One gate driver that excluded these peripheral features was developed at Intel [5]. This gate driver operated at similar switching frequencies of 500kHz to 1 MHz. The propagation delay and fall/rise times were significantly higher at 150 ns and 50ns respectively. It was able to achieve this for similar operating voltages, ranging from 0-30 V and a much higher temperature range than what is necessary for this project, up to 420 degrees Celsius. The peak output current was about 3 amps. This driver outperformed silicon technologies that used silicon-on-insulator fabrication methods to improve the performance. It was also able to have a much smaller area.

This driver omitted peripheral subcircuits and adhered to a simple architecture to reduce the area and therefore the cost. The block diagram of this circuit is depicted

below:

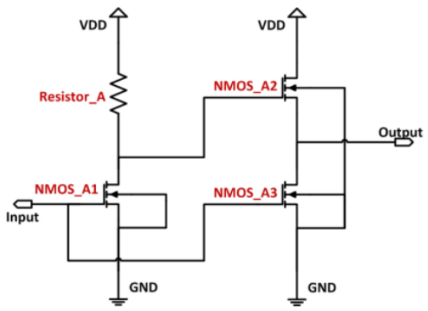
Figure 2-1: A block diagram of the SiC gate driver [5]



Here, the level shifter changes the voltage level of the control signal. The single-edge delay circuit and dead-time generator ensure that there is no shoot-through current by ensuring that the two output MOSFETs are never on at the same time. The combinational-circuit ensures that the output MOSFET MO can be turned on properly, and the current-buffer is needed to properly drive the pull-down device M1 at the output.

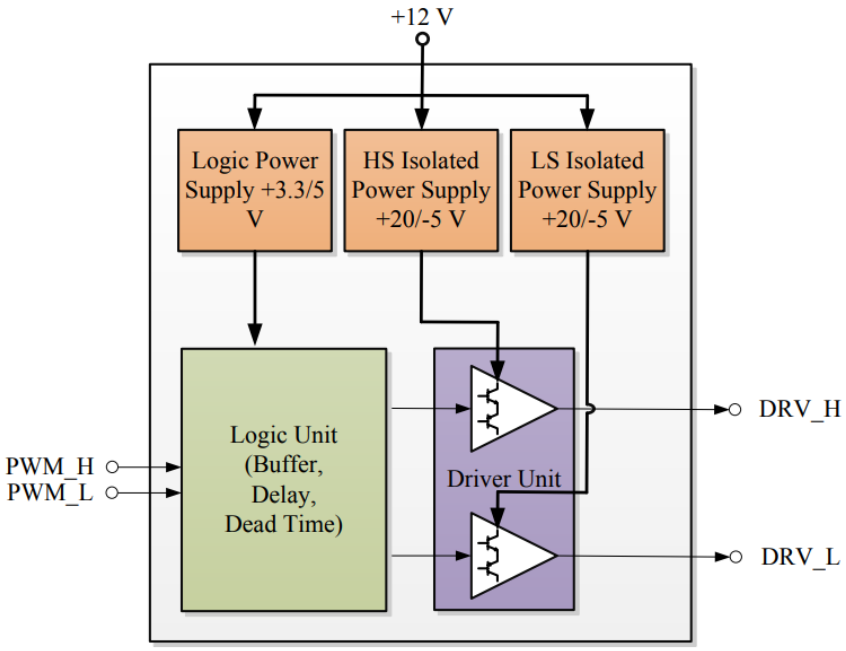
This gate driver outperformed those made with an SOI process, with an area one tenth of the silicon counterpart and an output power 5 times bigger. However, this gate driver was constrained by the technology available. The SiC process that was used had no PMOS transistors. This affected several aspects of the design, including the inverter design. A source-follower inverter was used, depicted below.

Figure 2-2: The source-follower inverter used throughout this gate drive [5]



Another SiC gate driver also used a dead-time control logic unit to avoid shoot-through current [3]. This one additionally used isolated rails to provide the appropriate rails to control the various MOSFETs as well as to power the logic in the dead-time control block. A block diagram of this gate driver is included below:

Figure 2-3: A block diagram of another SiC gate driver [3]



The logic unit consists of a level shifter, delay circuits that are used for filtering, and a dead time control circuit. This project was primarily focused on ensuring proper timing control for high frequency, high voltage, and high current voltages.

Other gate drivers made by Analog Devices were also studied to determine a simplified architecture. These predecessors gave critical insights into the design process.

Chapter 3

Process and Part Selection

Before tackling the design, the fabrication process had to be selected. The process selected influences the breakdown voltage, the on-resistance of the MOSFETs per unit area, and the maximum current density. Each process will also have different fabrication costs for the same design.

Higher current densities are desirable, as they enable higher driving capability respectively. To contrast, a low Rdson is preferred to reduce the output impedance of the gate driver. For the gate driver of this project, the supply voltage will vary from 0 to 30 volts, which would suggest a breakdown voltage around 40 volts. The breakdown voltage and on-resistances were studied to narrow down what process to use. Then saturation current was compared to select the best process.

These data suggested that a 130 nanometer process was the best process for this gate driver with a suitable breakdown voltage of about 45 volts, a low Rdson, and the highest Idsat of the three processes studied more thoroughly.

Of the parts available with this process, four active devices were utilized throughout the design: a high voltage LDPMOSFET, a high-voltage LDNMOSFET, a 5 volt NMOS and a 5 volt PMOS device.

The high-voltage LDMOSFETs were used because they could withstand the higher voltages seen throughout the circuit, up to about 30 volts across the drain-source terminals. These devices were designed for high switching frequency applications, and came with thin oxides to enable switching frequencies up to 10MHz. Because of this thin oxide, the gate-source connection could not withstand more than 5.5 volts. The faster switching allows for a higher efficiency, but the 5.5 maximum gate voltage influenced the design. The laterally-diffused MOSFETs require fewer fabrication steps. This makes them cheaper to fabricate than traditional vertically-diffused processes.

The 5 volt MOSFETs were used when lower voltages were present. These devices were much quicker than the high voltage devices. They are also smaller since a drift region is not necessary to tolerate the higher voltages.

Chapter 4

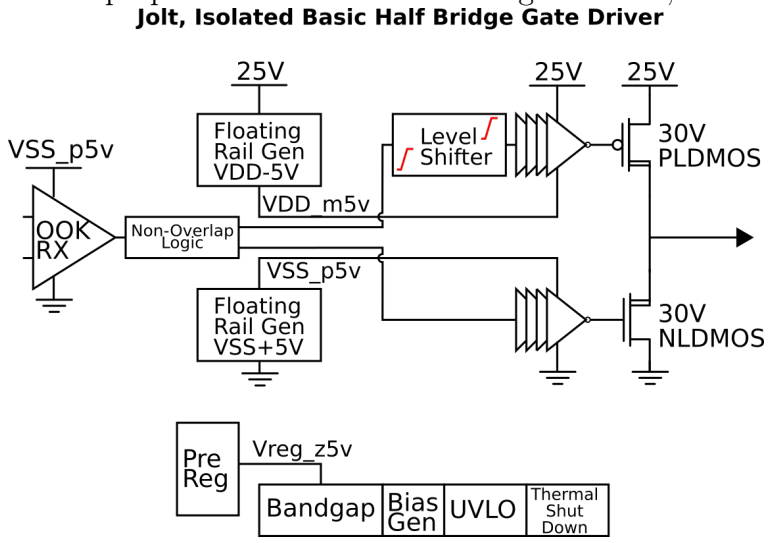
Design and Evaluation

The next section describes the design efforts made for this project. The subcircuits are presented in the order they come in in the signal chain, not in the chronological order they were developed in.

4.1 Gate Driver Architecture

After studying the architecture of various similar gate drivers that Analog Devices had, a preliminary architecture was designed, depicted below:

Figure 4-1: The proposed architecture for this gate driver, code name Jolt



The signal chain starts with the on-off key receiver. This subcircuit takes control

signals from the transformer on another die and demodulates it. The signal is then sent to the non-overlapping logic circuit. This block takes the control signal from the receiver and generates two control signals for the output NMOS and PMOS transistors. This block does so while ensuring that the two output transistors are never simultaneously on.

From the non-overlapping logic unit, the signal that controls the output PMOS is then sent to the level shifter, which changes the control signal from a signal that switches from 0 to 5 volts into a signal that switches from VDDHI-5 to VDDHI, where VDDHI is the high rail used to power the gate driver. So, for example, if the high rail is 25V like in the figure above, the level shifter turns the 0 to 5 volt switching signal to a 20 to 25 volt switching waveform. The level shifter ensures that the PMOS can be properly controlled, while not damaging it.

The gate oxides of the output transistors cannot experience a voltage difference greater than about 5.5 volts since they are thin. While the thin oxide allows for higher switching frequencies, it also makes them susceptible to breaking down when the voltage across it is too large. The PMOS cannot be controlled with a 5 volt signal, it must be powered with a voltage high enough to properly turn it on and off. To have a voltage that is high enough to turn off the PMOS while not swinging low enough to damage the oxide, the level shifter is used.

The two floating voltage rail generators are used to provide reference voltages that are used throughout the gate driver. The low-side rail provides a voltage reference 5 volts above the low supply rail VSS. Meanwhile the high-side floating rail provides a voltage 5 volts under the supply voltage VDDHI. These voltages are used throughout the gate driver: in the level shifter, to supply the inverter chains, and to power the logic gates in the non-overlapping logic unit and in the inverter chains.

From the level shifter the signal that controls the output PMOS enters the inverter

chain. The inverter chain reduces the load capacitance on the level shifter for this path of the signal chain. The output buffer has a relatively large load capacitance of about 2 nanofarads. If the level shifter was to drive the output buffer by itself, it would drastically increase the driving current required to drive it. This would then drastically increase the size of the devices in the level shifter. The additional area of the inverter chains does not compare with the area increase that their omission would necessitate. So by adding it, we reduce the total area of the gate driver.

The control path for the NMOS is similar, but different in some key ways. It starts in the non-overlapping logic unit, then is sent directly to the inverter chain. Since the NMOS is connected to VSS, the 0 to 5 volt control signal can adequately control the NMOS without causing any damage to its thin oxide. The inverter chain here similarly reduces the load capacitance on the non-overlapping logic unit.

Finally, the output buffer is what sources/sinks the output current. For this application, there are three load conditions of interest: a sourcing condition, a sinking condition, and a purely capacitive one. In the sourcing condition, an output resistor in connected in series with the output capacitor that is connected to the low supply rail (VSS). In the sink condition, there is a pull-up resistor connected at the output and the output capacitor is tied to the low supply rail. In the purely capacitive load condition, the load consists solely of a load capacitor tied to VSS.

The diagram also includes various housekeeping blocks that were intended to be completed for this project. The pre-regulator was meant to create a reference voltage, as would the bandgap reference. The bias generator creates a biasing current of 10 microamps used throughout the gate driver. The under-voltage lockout circuit and thermal shutdown circuits prevent operation in conditions that would result in component damage or strange/incorrect outputs.

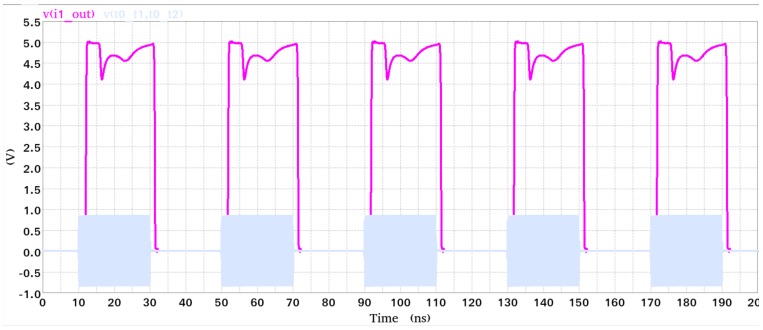
4.2 On-off key receiver

The on-off key receiver is responsible for demodulating the control signal for the gate driver. The gate driver designed here would come in a package that has three die: two of the gate drivers and one control die. The control die consists of a on-off key transmitter and a transformer that galvanically isolates the control signal for safety reasons. The transmitter sends the signal through the transformer, then to the other die, the focus of this project.

The receiver amplifies the signal, then uses current mirrors to extract the envelope of the modulated signal. Finally, the signal is sent through a buffer made up of two inverters to clean up the signal.

A simplified transmitter block was created in Cadence to simulate the real transmitter. This transmitter created the on-off key modulation. This modulation scheme uses the absence/presence of a sinusoid to represent digital information. The receiver then turns this modulated signal into a digital signal varying from zero to five volts. An example of the output of the transmitter and the output of the receiver is depicted in the figure below:

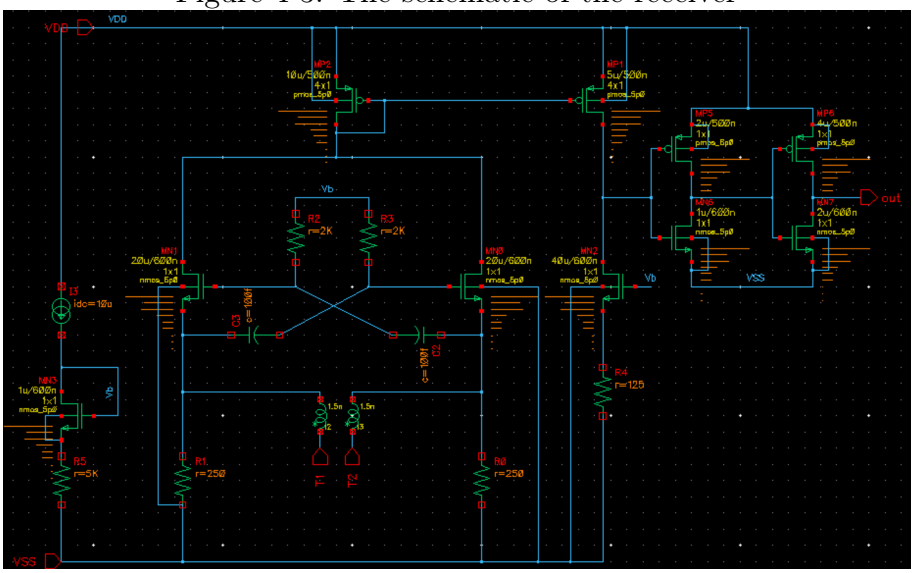
Figure 4-2: Waveforms of the modulated input to the receiver in periwinkle and the output of the receiver in fuschia



The receiver works as follows: the differential pair sends the current to a current mirror. Then the current mirror sends an output voltage to a buffer comprised of two inverters. On that same branch, a current mirror matches the current from a current

reference. The schematic is included in the picture below:

Figure 4-3: The schematic of the receiver



4.3 Non-overlapping logic

After the control signal is demodulated from the transmitter on the other die, the signal is then sent to the non-overlapping logic unit to ensure proper timing to avoid any shoot-through current. For the rising edge, the NMOS must turn on after the PMOS turns off. For the falling edge, the PMOS must turn on after the NMOS turns off.

To accomplish this, some combinatorial logic is used in feedback to create the two signals controlling the NMOS and PMOS. This logic was made without the use of a library to allow for customization of each of the logic gates. For this block, NAND, NOR, and NOT gates were designed. The schematics for each are depicted in the figures below:

Figure 4-4: A schematic of the inverter design [6]

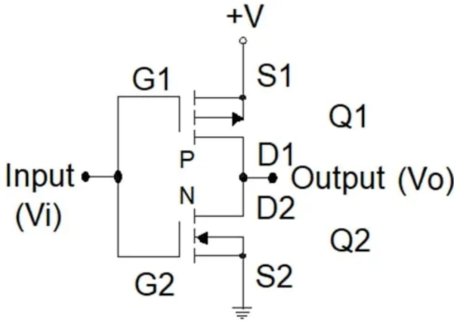


Figure 4-5: A schematic of the NOR logic gate design [6]

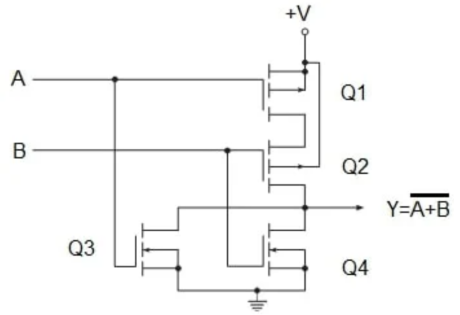
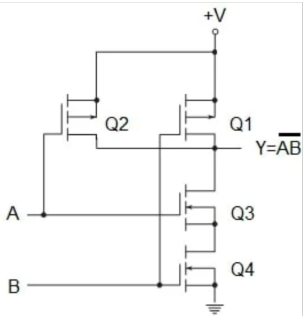


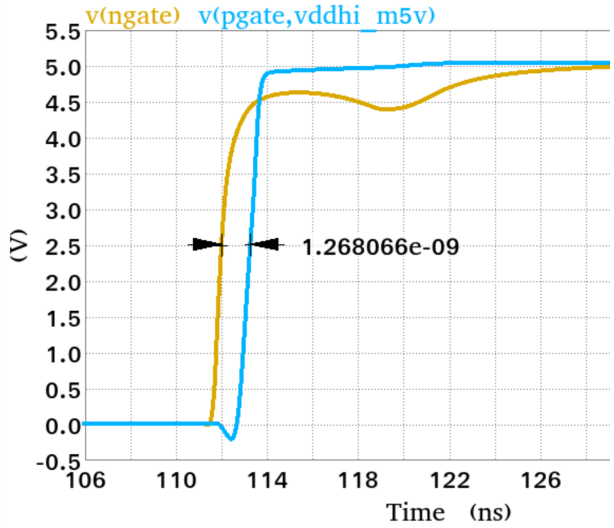
Figure 4-6: A schematic of the NAND logic gate design [6]



At first, the design seemed to work fine. However, when it was integrated with the other blocks several timing issues arose. The output PMOS was not turning off before the NMOS turned on. For the rising transitions there was a commutation

interval where both the PMOS and the NMOS were turned on, which resulted in shoot-through current. A picture of this issue is included below:

Figure 4-7: A waveform depicting the timing issue that the non-overlapping logic had



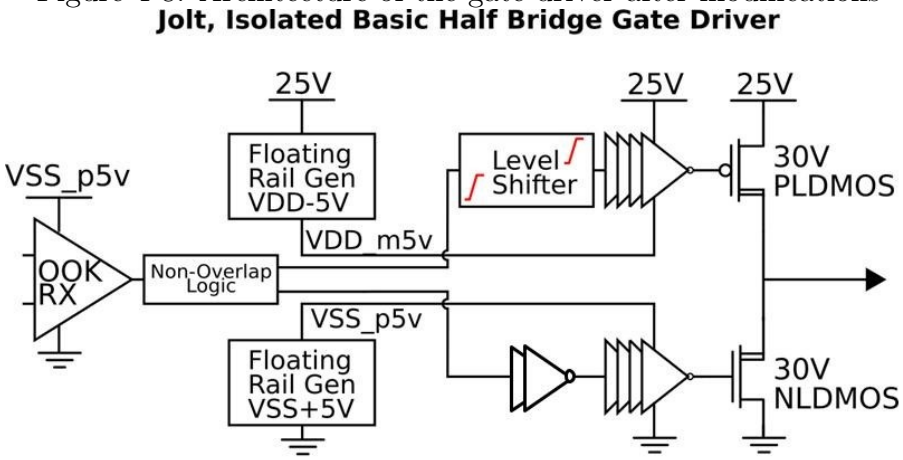
To fix this, a number of strategies were attempted. First, one of the output inverters in the non-overlapping logic was made significantly larger. In theory, this would spend up the PMOS, making it turn off faster and eliminating the overlap time. Unfortunately, this strategy was not successful.

The next attempt involved a slight modification of the combinatorial logic. This also didn't solve the problem. The third modification was a change in the architecture of the level shifter, again to turn off the PMOS faster. This was also unsuccessful.

Finally, an additional two-stage inverter chain was added to the low-side signal chain, after the non-overlapping logic but before the low-side inverter chain. Instead of speeding up the PMOS switching transition, this modification slowed down the NMOS transition, ensuring that the two output transistors are never simultaneously on. The addition of the mini-inverter chain is shown in the architecture in the figure below:

To increase the delay on the low-side signal chain, the width of the transistors was minimized. The reduction of the width meant that the current flow was constricted,

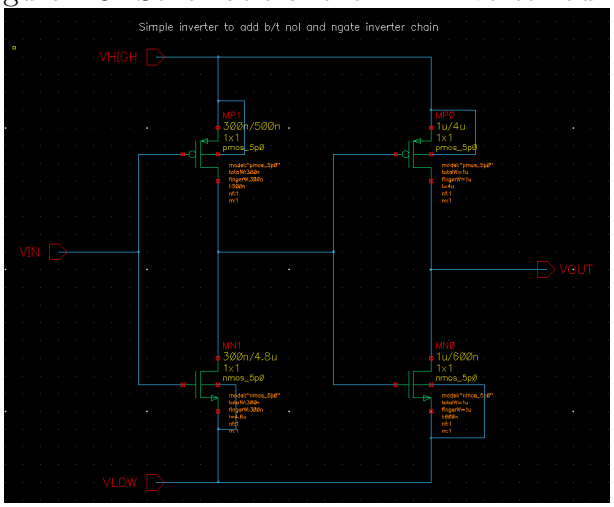
Figure 4-8: Architecture of the gate driver after modifications



resulting in a slower transition. The same effect could be achieved by increasing the lengths of the devices.

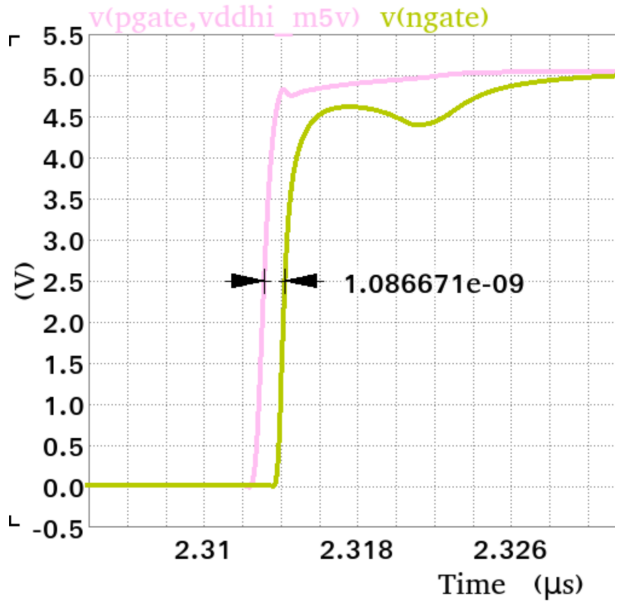
However, to target the rising edge of the waveform, these changes were exaggerated in the transistors responsible for these transitions: the NMOS in the first inverter and the PMOS in the second. During the rising transition, the input to the mini inverter chain is rising, turning on the NMOS in the first inverter. Once the NMOS is turned on, the output of the first inverter is pulled low, which then turns on the PMOS in the second inverter. When the PMOS turns on, the output of the mini-inverter chain is pulled high. The schematic is depicted below.

Figure 4-9: Schematic of the mini inverter buffer



After some tweaking, these modifications resulted in a properly functioning rising transition: the signal controlling the output PMOS turned off before the NMOS was turned on, depicted below:

Figure 4-10: A waveform depicting the proper operation of the non-overlapping logic after adding the secondary inverter chain.

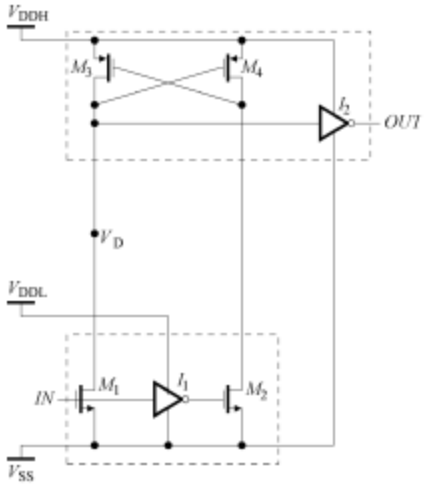


While this solution did solve the problem, the dimensions of these transistors is larger than is ideal, with lengths around 3-5 microns. Furthermore, there was only an approximately 1 nanosecond delay between waveforms in both the rising and falling transitions, which is enough for this initial design effort, but leaves room for improvement. Methods of performing these improvements are described in a later section.

4.4 Level shifter

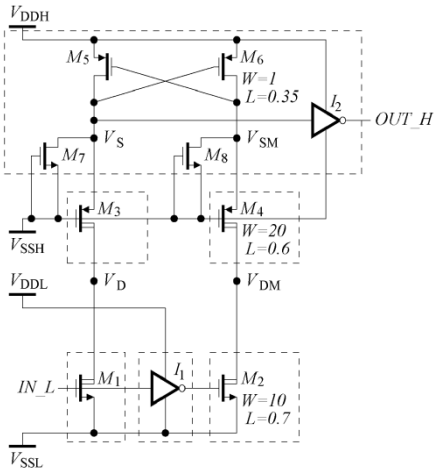
The level shifter used in this project was based on a simple level shifter that was modified to minimize the leakage current [4]. The level shifter changes the voltage of a signal while maintaining its integrity. The basic schematic is depicted below:

Figure 4-11: A schematic of a simple level shifter [4]



In the modified version, a cascode is added in series with each of the PMOS transistors to reduce the power consumption.

Figure 4-12: A schematic of a modified level shifter [4]



When the input goes high, M1 conducts and M2 does not. This pulls VD low and M4 conducts. This pulls VB high which turns M3 off. If VD is low, then the output is high. When the input goes low, M1 turns off and M2 turns on. VB is pulled low, which turns on M3. VD is high which turns off M4. If VD is high, then the output is low. Here, the voltage at the output would switch from VSS to Vddh, which in our case would be the output from the high side voltage rail generator, or VDD-5V and VDDH = VDD. VDDL comes from the output of the low side voltage rail generator,

or VSS+5V.

While the overall operation worked with a variety of dimensions, proper sizing can ensure that the propagation delay that the level shifter adds to the signal chain is minimized. By increasing the widths of the transistors, the transistors will transition more quickly, reducing the propagation delay. The sizing of the transistors within the inverters is also to be considered. After some tweaking, the transistors were sized properly for this application.

However, after creating the non-overlapping logic block and integrating it, the level shifter was too slow. So, to modify this the architecture was changed slightly. An inverter was added to the input and the output connection was modified so that the output was not inverted.

4.5 Floating voltage rail generator: high side

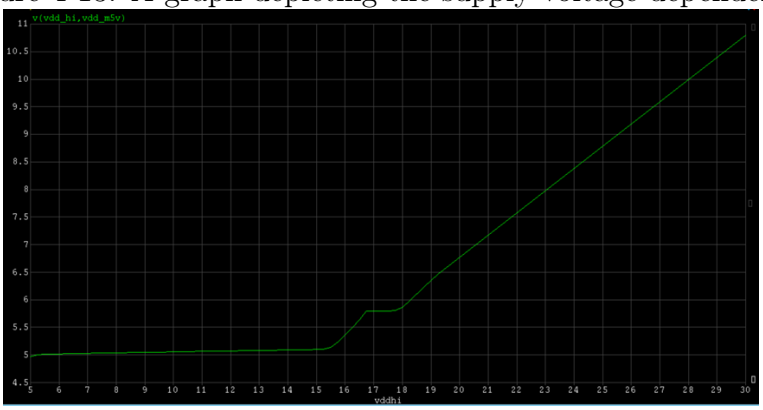
The voltage rail generators provide rail voltages for proper operation of other sub-circuits throughout the gate driver. For this gate driver, there are two voltage rail generators: one providing a voltage 5V under the high rail, VDDHI, and one providing a voltage 5V above the low rail, VSS. The high-side floating rail provides this voltage for the inverter chain that drives the PMOS in the output buffer and the level shifter. The floating rail generator works by creating a reference voltage with a biasing current, which is then sent through a source follower that has a biasing network.

The reference voltage is created by sending the 10 microamp current through a 500 kiloohm to get the desired voltage drop of 5 volts under the rail. The proper biasing resistor value was found through simulation.

After testing the initial proper operation, additional evaluative simulations were

done. The voltage rail generators must work for a variety of rail voltages (VDDHI). Ideally, the difference between the high rail (VDDHI) and the output of the voltage rail generator would be constant at 5 volts for all values of VDDHI. However, at first go there was a linear dependency on VDDHI, depicted below:

Figure 4-13: A graph depicting the supply voltage dependency

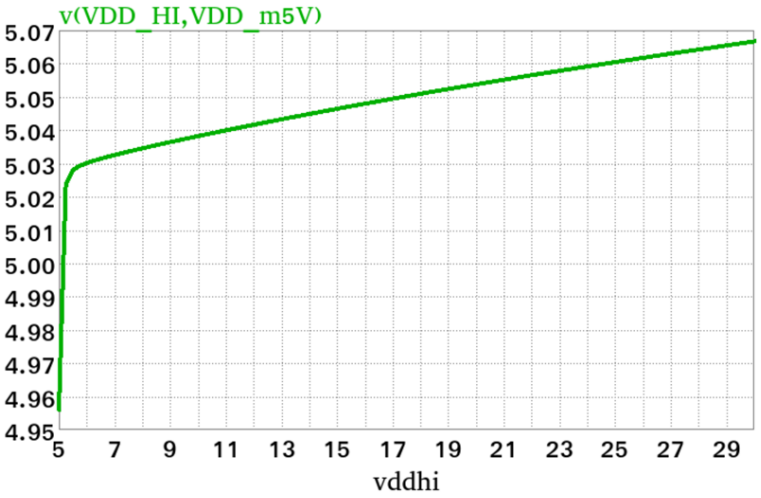


This dependency was due to the body effect. The body connections of the voltage rail generator were not properly biased, meaning that the threshold voltage of the transistors was now related to the voltage across the body-source terminals. This body-source voltage was related to the rail voltage (VDDHI) which led to this relationship.

To fix this, the cross section of these devices was studied to note where the p-n junctions were formed, and how leakage current would likely flow if certain connections were not tied to ground/the supply correctly. From this, the new connections were determined.

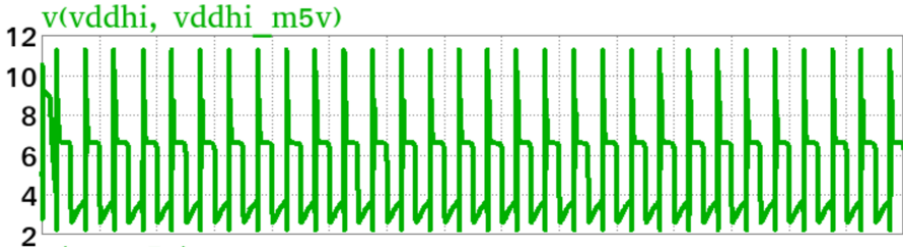
These new connections prevented the effects of a non-zero body-source potential and of leakage currents through p-n junctions, resulting in an output voltage that is consistently VDDHI-5 for all possible VDDHI for this application, depicted below.

Figure 4-14: A graph of the output voltage of the high-side floating voltage rail generator



Once the floating voltage rail generators were working, they were integrated with the other blocks that had been designed up until that point, the inverter chains and the output buffer. As this was done, a problem was noticed: at the transitions, there were significant current draws on the voltage rail generators, leading to big fluctuations in the output voltages that both were outputting. A waveform of the high-side rail depicting the egregious overshoot and undershoot are shown below. The undershoot went up to 100 percent of the stable value. Note that the graph depicts the difference between the high supply rail (VDDHI) and the output of the floating rail.

Figure 4-15: A waveform of the output voltage of the high-side floating rail

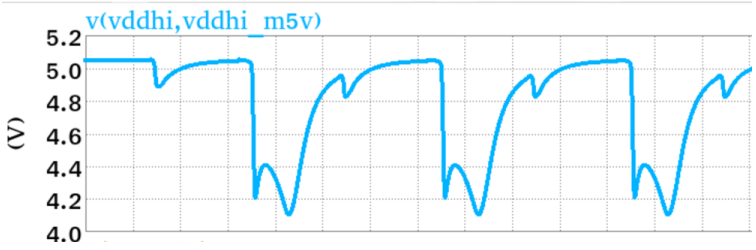


To solve this, bypass capacitors were added to stabilize the reference voltage, bias point, and the output voltage. Here, the design tradeoff was the mitigation of the overshoot/undershoot of the output voltages versus the increase in total area (and therefore, gate driver cost) due to the addition of these bypass capacitors.

To balance the two concerns, some concessions were made. The output voltage bypass capacitors of the two floating voltage rail generators were made a bit larger than the others. Another adjustment made was changing the way that the reference voltage was stabilized with the capacitor. Instead of connecting it to the reference voltage, it was connected to the gate of the transistor in that branch. This led to a marked improvement in the undershoot/overshoot.

After much simulation, the undershoot and overshoot managed to stay under the 20 percent margin of error, depicted below.

Figure 4-16: A waveform depicting the lower overshoot/undershoot



While a ten percent margin would have been better, this was acceptable for this project. Further improvements are mentioned in the discussion section.

4.6 Floating voltage rail generator: low-side

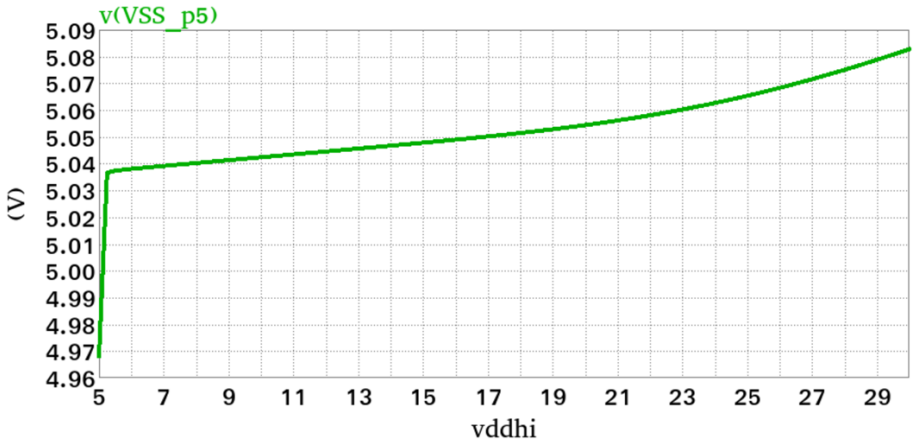
The low-side floating voltage rail generator operates largely like the high-side version, with some topology reflections. A reference voltage is created using a current source and a resistor, a source follower then gives the output with the help of a biasing network. The design process largely followed that of the high side: the biasing resistor was determine through simulation and the supply voltage dependency was also noticed.

The devices used for the low-side floating rail generator are both the 5 volt devices and the 30 volt devices. The 5 volt devices were used where the voltages were lower

and the 30 volt devices were used to protect the 5 volt devices from higher voltages. This meant that the proper biasing for the devices was slightly different than that for the devise in the high-side floating rail generator.

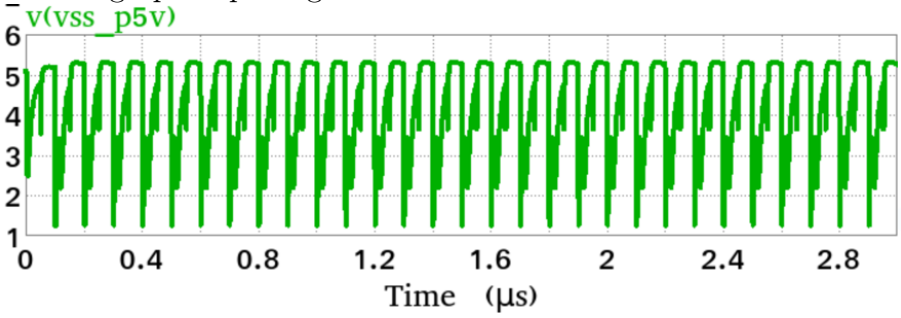
After properly biasing the devices, the supply rail dependency was eliminated, depicted below:

Figure 4-17: A graph of the output of the low-side voltage generator for various supply voltages



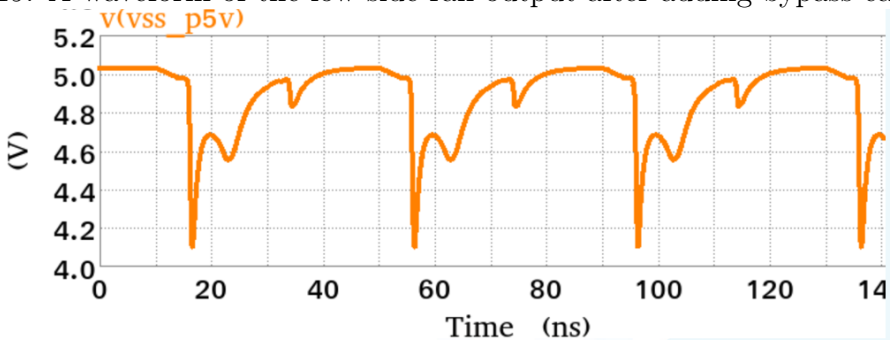
After integrating the low-side, a similar problem arose with the overshoot of the output voltage. The addition of bypass capacitors solved this problem after some testing. The before and after waveforms are depicted below:

Figure 4-18: A graph depicting the undershoot and overshoot of the low-side rail



Further improvements are described in the discussion section.

Figure 4-19: A waveform of the low-side rail output after adding bypass capacitors



4.7 Inverter Chain

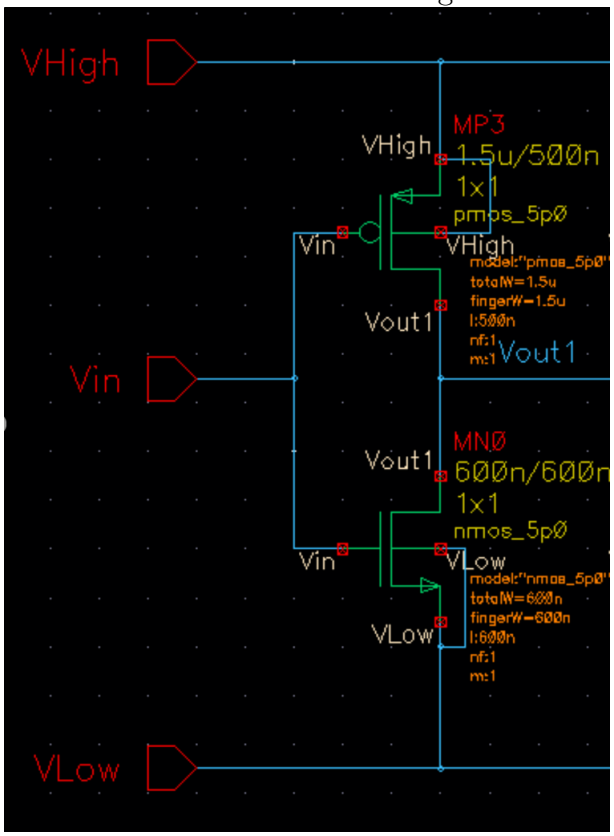
The inverter chain minimizes the load capacitance on the level shifter and non-overlapping logic blocks to minimize the load capacitance on the level shifter and on the non-overlapping logic blocks. This way, the dimensions of the devices in the other driving blocks can be minimized. Without the inverter chain, the load capacitance of the driving blocks is based on the output capacitance and the gate capacitance of the output buffer MOSFETS as well as other intrinsic capacitances, which totals to about 3 nanofarads. With the inclusion of the inverter chain, the capacitance seen by these driving blocks is on the order of a couple of femtofarads.

The goal is to create an inverter chain that reduces the capacitance that the upstream blocks must drive while minimizing any additional propagation delay. To do this, the fanout, number of stages, and the dimensions of the initial stage, must be optimized [2].

For the initial stage there are a couple of factors that determine the dimensions. Firstly, the dimensions of the two transistors in the first stage should be two to three times the minimum width to ensure that it has enough driving strength to drive the next stage. Furthermore, we want the PMOS and NMOS to have symmetrical delay. To do this, in each inverter the PMOS should be two to three times bigger than its NMOS counterpart. This accounts for the disparity in the mobility of the charge carriers for PMOS and NMOS transistors. Finally, the number of fingers in each

NMOS and its corresponding PMOS must be the same. This simplifies the layout, so that the two can connect more easily. With all of these constraints, the dimensions of the first stage of the inverter chain can be determined, depicted below:

Figure 4-20: The schematic of the first stage of the inverter chain



Next, the number of stages and fanout should be determined. Initially, the number of stages for this gate driver was based off of the inverter chain of a previous gate driver. Lastly, the fanout of the inverter chain can be calculated using the following equation:

$$F = C_L/C_g$$

Or the factor by which the dimensions width changes between each stage can also be determined with the following equation:

$$f = \sqrt[N]{C_L/C_g}$$

Where C_L is the load capacitance that the inverter chain will drive, C_g1 is the gate capacitance of the first stage, and N is the number of stages. For $Cg = 1.5E-14$, $C_L = 2E - 11$, and $N = 4$ this results:

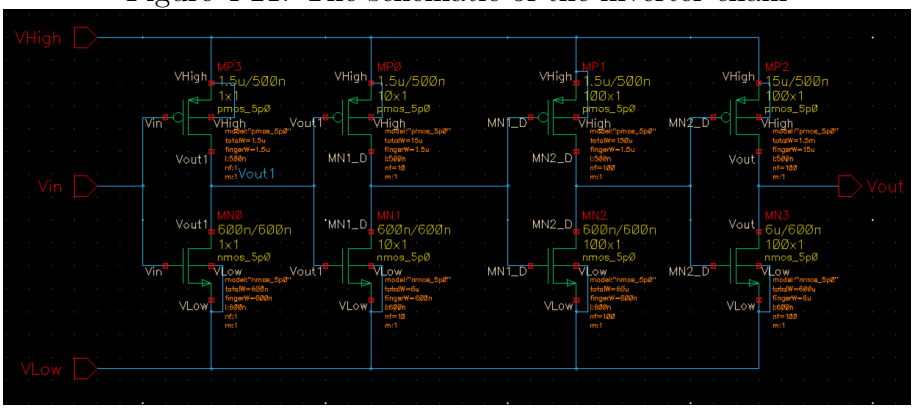
$$f = \sqrt[4]{1333.33}$$

$$f = 6.042$$

Ratios of 5, 7, and 10 were tried. The ratio of 10 worked best. When this was implemented, the delay was 1.49 ns for typical operating conditions. This is in the range of what would be expected.

At first, identical inverter chains were used to drive both the NMOS and the PMOS, depicted below. The only difference being the rail voltages of each of ensure that the high enough voltages were used to drive the PMOS compared to those driving the NMOS . However, when integrating the block this likely caused the mismatch in the rising/fall times of the different output conditions, especially the sinking condition. This also might have led to problems with the non-overlapping logic unit. One solution would be to resize the inverter chain that would drive the PMOS of the output buffer.

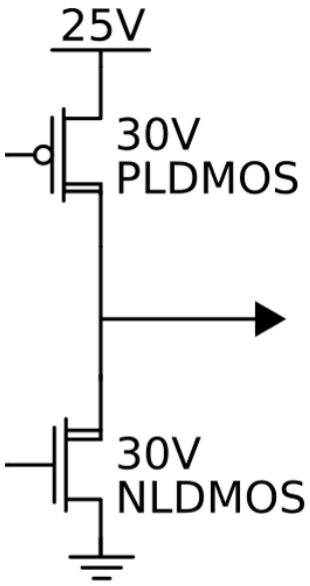
Figure 4-21: The schematic of the inverter chain



4.8 Output Buffer

The output buffer sources and sinks the output current. For this application, the gate driver must be able to source/sink 6 amps of current. To do this, a PMOS and NMOS are connected in series. In order to be able to source/sink that current, the output transistors must be properly sized. When driving a large capacitive load, the largest factor for the driving current for devices made with this process is the on-resistance. The on-resistance is largely determined by the dimensions of the device.

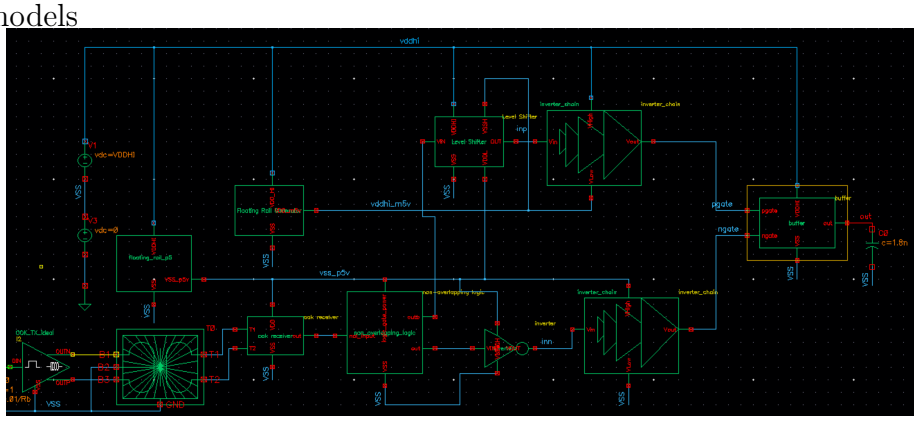
Figure 4-22: A schematic of the output buffer



4.9 Integration and Validation

Once all of the subcircuit blocks were working and seemed to work in conjunction, more extensive validation was done using SPICE. The integrated gate driver is shown below.

Figure 4-23: A schematic of the complete gate driver with the transmitter and transformer models



Load Condition	Temperature	Process Corner	Operating Voltage
Sourcing	-40, 0, 25,75, 125	Slow	Vary from 0 to 30V
Sinking	-	Nominal	-
Purely Capacitive	-	Fast	-

Table 4.1: A table of the various testing conditions

There were several metrics that had to be measured for various operating conditions, including the peak output current, the propagation delay, the rise and fall times, and the quiescent current. Furthermore, correct general operation of the gate driver also had to be tested for each of the operation conditions (that varied temperature, operating voltages, process corners, and different load conditions). Each variation is listed in the table above.

4.9.1 Sourcing Output Condition

The sourcing condition had the output was tied to a 1.8 nanofarad capacitor in series with a 1 ohm resistor that was tied to ground. In this condition, the output buffer sources the output current; the current flows out from the buffer through the load to

ground. The PMOS turns on and current flows from the voltage rail to the output. Then when the NMOS turns on, the output capacitor discharges and current flows from the output of the output buffer through the NMOS and to the low rail (VSS).

In this output condition, the output voltage swings from zero to VDDHI since when the NMOS is turned on, the output voltage is pulled down to VSS. Then when the NMOS is off and the PMOS is turned on the capacitor charges up to VDDHI.

4.9.2 Sinking Output Condition

The sinking condition consisted of the output of the gate driver was connected to a 1 ohm pull-up resistor that was tied to the high rail (VDDHI). A 1.8 nanofarad capacitor was connected in series to ground.

In this output condition, the output swings from some non-zero voltage to VDDHI. When the NMOS turns on, instead of the capacitor discharging fully, the pull-up resistor and the on-resistance of the NMOS act like a voltage divider.

4.9.3 Purely Capacitive Output Condition

In this load condition the output is tied to a capacitor that is then tied to VSS. In this load condition, like in the sourcing condition, the output voltage swings from 0 to VDDHI.

4.9.4 Measurement Note

The propagation delay was measured from the rising edge of the signal going into the receiver and the start of the transition at the output node. The transmitter only adds about 1-2 nanoseconds of delay.

4.9.5 Results Summary

Only some graphs of the results of the validation are included below for brevity. These show the temperature and voltage dependencies for the peak output current. It is important to note that the while the gate driver would operate for supply voltages varying from 0 to 30 volts, the undervoltage-lockout circuit would prevent any operation for supply voltages under 8 volts. In other words, for supply voltages lower than 8 volts, the gate driver would have zero output current.

Figure 4-24: A graph of the peak output current for different temperatures

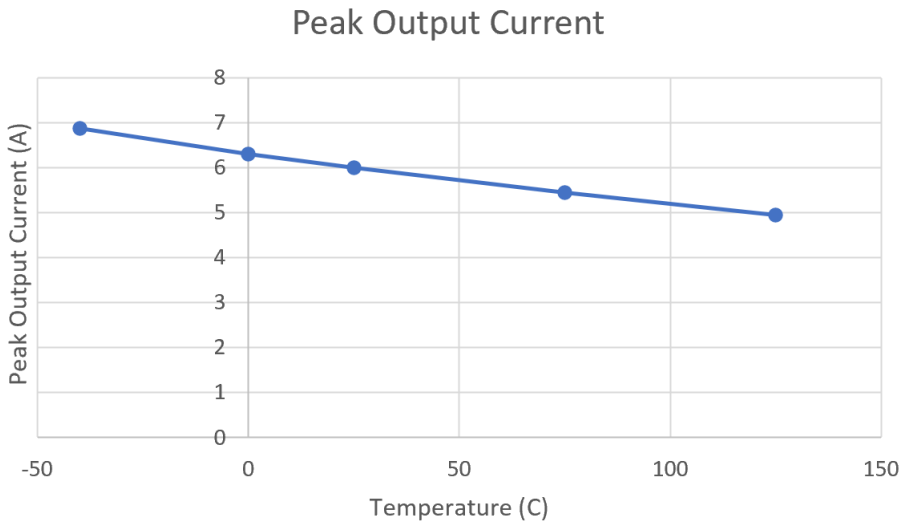
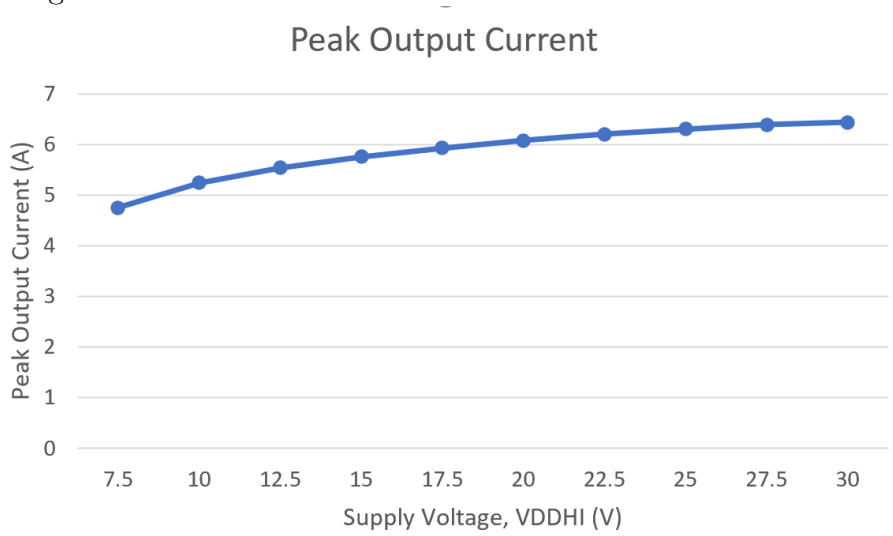


Figure 4-25: A graph of the peak output current for different supply voltages. Measured at 0 degrees C



Besides the temperature and voltage variations, there was one other observation made in simulation. The rise/fall times were not symmetrical. Furthermore, this asymmetry was exacerbated when comparing the different load conditions. While the sourcing and purely capacitive conditions had fairly similar rise/fall times the sinking condition was significantly (and consistently) faster. There are some ways this variation could be minimized, discussed in the next section.

Chapter 5

Discussion

5.1 Comparison to predecessors and counterparts

Compared to its contemporary counterparts, this gate driver performed just as well if not better for similar typical conditions. For a supply rail (VDDHI) of 25 volts, this gate driver has a higher peal output current of about 6 amps. It also had a lower output resistance and a lower propagation delay for the same temperature range. A summary of the metrics is listed in the table below:

However, it was not as performant for some of the lower temperatures and lower end of the supply voltage range. This should improve with the addition of the housekeepings blocks, although more design efforts may be necessary. It also had a fairly high quiescent current of about 2 milliamps, which enabled it to be so fast.

Features	Jolt	ADuM4223	TI UCC21530	Silicon Labs	Silicon Labs
Supply Voltage (V)	25	18	25	30	30
Peak Iout (A)	6	4	4/6	1.8/4	2/4
Output Res (ohms)	0.4/0.6	0.6/1.1	0.55/1.14	1.0/2.7	1.0/2.7
Temp Range (Celsius)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Prop Delay (ns)	10	43	19	30	24

Table 5.1: A table summarizing the performance of this and other gate drivers

5.2 Next Steps

There are some improvements that could be made as well as some things that were not accomplished during the internship.

First, the overshoot and undershoot of the voltage rail generators could be decreased by adding a source follower to the topology. Another improvement that could be made for this block is to modify the architecture such that the resistors in the design are replaced with transistors. This would require a complete redesign of the two blocks but would save cost because with this process it is cheaper to fabricate transistors than integrated resistors (need to double check, might be reduced cost due to reduced area).

Another area for improvement would be to optimize the inverter chain for the PMOS signal chain. As was mentioned, this design used the same inverter chains for both the NMOS and the PMOS. However, the PMOS inverter chain could be sized differently to account for the difference in carrier mobility. This modification might make the additional inverter chain on the NMOS chain obsolete.

Finally, another potential improvement could be achieved with a different fabrication process. As the silicon carbide fabrication processes continue to develop, better processes may soon become available.

Of course, there are a few things that were not accomplished in this project. Throughout the design several biasing currents and reference voltages were used that were not designed. The design of these elements is left for future development. Additionally, there are a couple of tests that were outside of the scope of this project including ESD simulation and common-mode rejection ratio simulations. These would be useful simulations but were not a priority for this project.

Chapter 6

Conclusion

The design and simulation of a basic, half bridge, isolated silicon carbide gate driver. The gate driver was able to output 6 amps of peak output current, with less than 10 nanoseconds of propagation delay. It was had fall times and rise times under 20 nanoseconds, with some asymmetry. Finally, it had a low output resistance. It worked for a wide range of temperatures. It did have a fairly high quiescent current of about 2 milliamps, which is fine for this application.

Appendix A

Tables

Load Condition	Temperature	Process Corner	Operating Voltage
Sourcing	-40, 0, 25,75, 125	Slow	Vary from 0 to 30V
Sinking	-	Nominal	-
Purely Capacitive	-	Fast	-

Table A.1: A table of the various testing conditions

Features	Jolt	ADuM4223	TI UCC21530	Silicon Labs	Silicon Labs
Supply Voltage (V)	25	18	25	30	30
Peak Iout (A)	6	4	4/6	1.8/4	2/4
Output Res (ohms)	0.4/0.6	0.6/1.1	0.55/1.14	1.0/2.7	1.0/2.7
Temp Range (Celsius)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Prop Delay (ns)	10	43	19	30	24

Table A.2: A table summarizing the performance of this and other gate drivers

Appendix B

Circuit Schematics

Figure B-1: The proposed architecture for this gate driver, code name Jolt

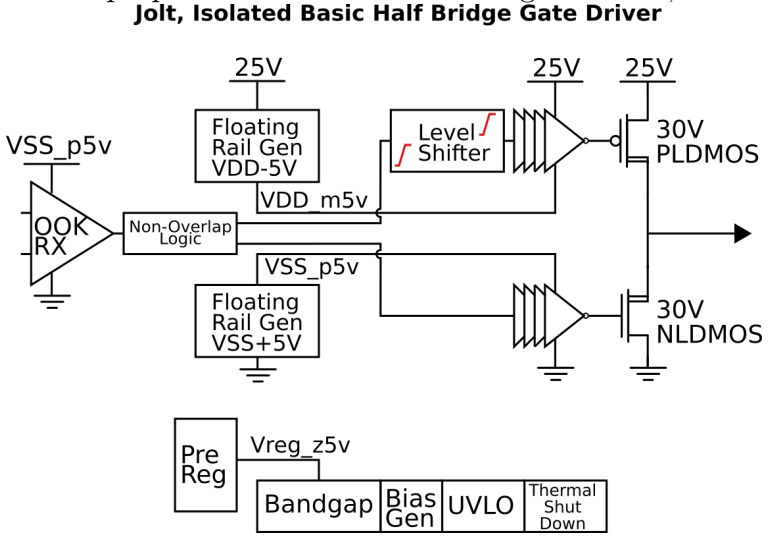


Figure B-2: The schematic of the receiver

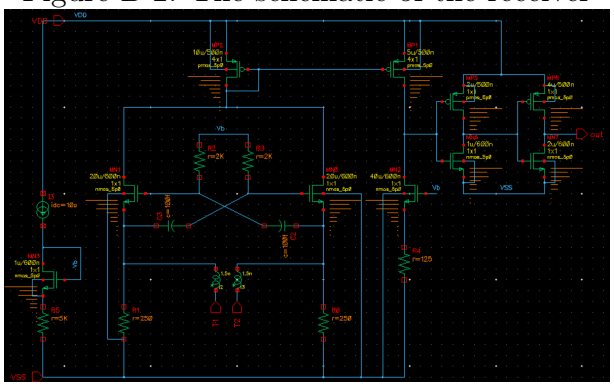


Figure B-3: A schematic of the inverter design [6]

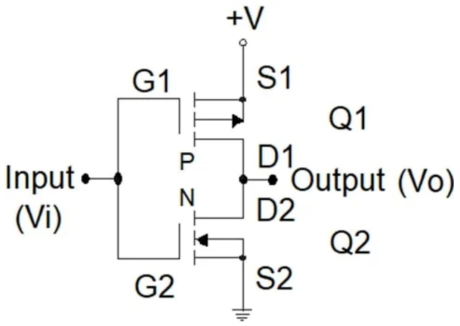


Figure B-4: A schematic of the NOR logic gate design [6]

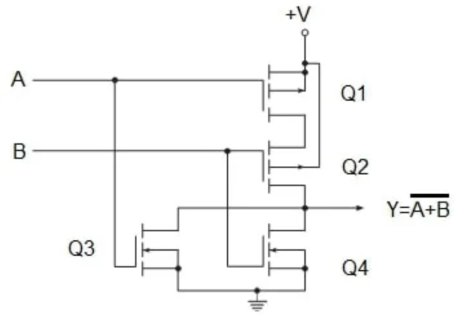


Figure B-5: A schematic of the NAND logic gate design [6]

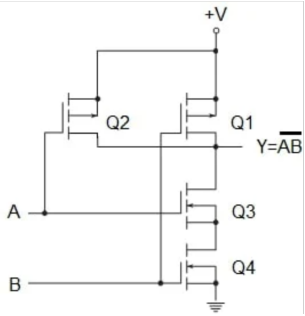


Figure B-6: Architecture of the gate driver after modifications

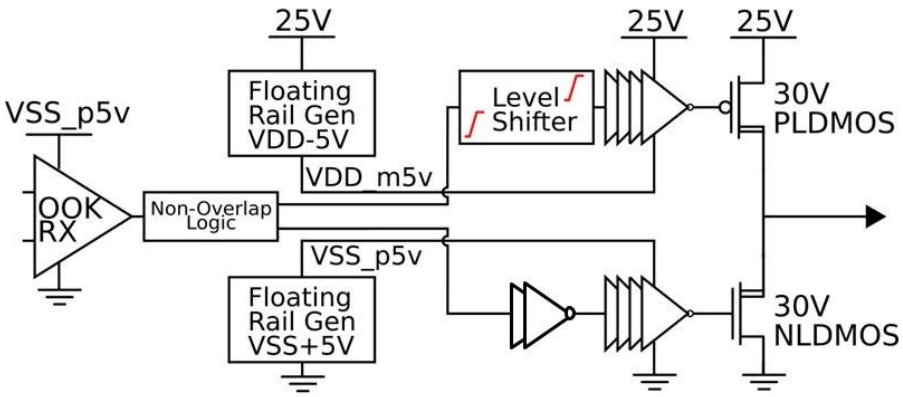


Figure B-7: Schematic of the mini inverter buffer

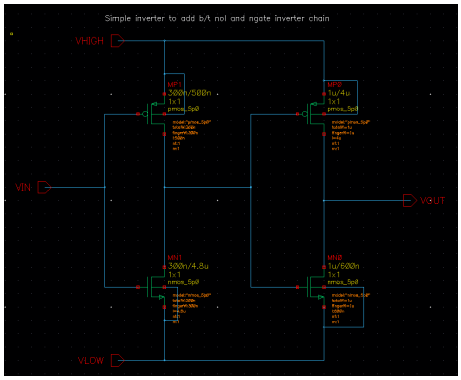


Figure B-8: A schematic of a simple level shifter [4]

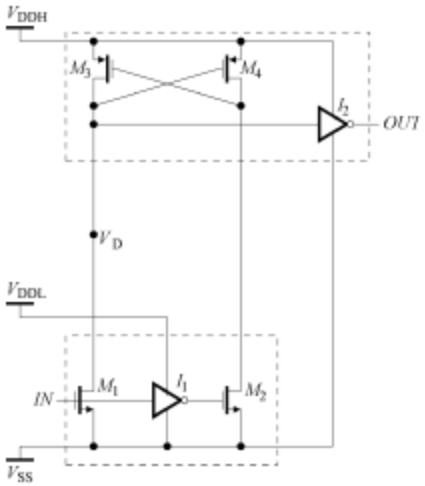


Figure B-9: A schematic of a modified level shifter [4]

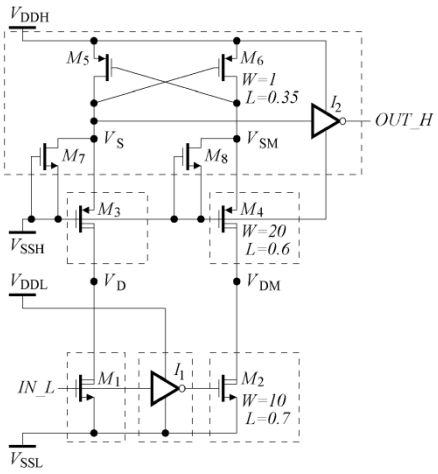


Figure B-10: The schematic of the inverter chain

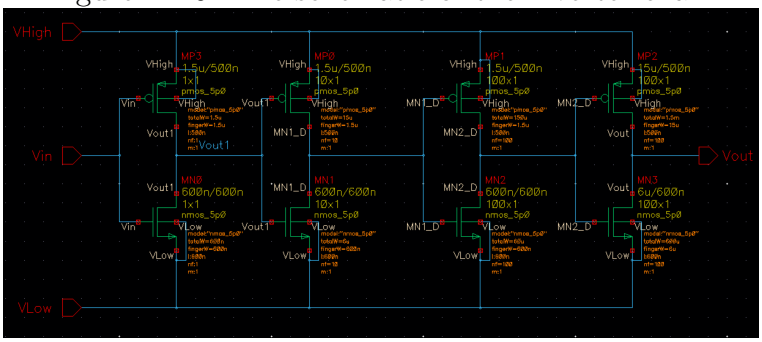


Figure B-11: A schematic of the output buffer

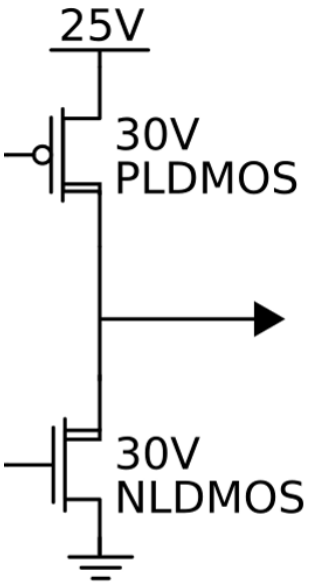
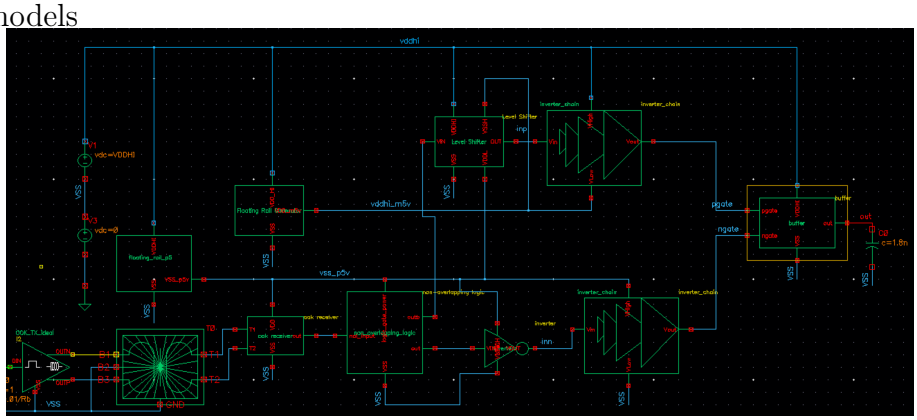


Figure B-12: A schematic of the complete gate driver with the transmitter and transformer models



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