Design of a Precision, Very Low 1/f Noise, Low Power, Rail-Rail I/O, Integrated Bi-CMOS Operational Amplifier

by

Rhian Austin Chavez

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Author .....
Department of Electrical Engineering and Computer Science
January 14, 2022

Certified by .....
Lance Bourque
IC Design Engineer, Analog Devices, Inc.
Thesis Supervisor

Certified by .....
Ruonan Han
Associate Professor, Electrical Engineering and Computer Science
Thesis Supervisor

Accepted by .....
Katrina LaCurts
Chair, Master of Engineering Thesis Committee

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Abstract

The detailed design of a precision, very low $1/f$ noise, 100μA, 30V, rail to rail input and output, integrated Bi-CMOS operational amplifier is presented. Necessity for such an amplifier in the current technological space is examined. Specific attention is given to the novel design of a stable current source requiring no more than approximately 50mV of overhead, for use with a very low noise native NMOS differential input pair. An improved technique for analyzing MOSFET $1/f$ noise in modern simulation environments is explored. Special consideration is given to the usage of native NMOS devices as the primary input pair, which are required in order to meet the low noise and zero input bias current requirements simultaneously. Detailed descriptions of key amplifier stages are given; rail to rail input, folded cascode, Monticelli rail to rail output, and Miller compensation. Finally, amplifier transient, spectral, and noise results are presented and discussed.

Thesis Supervisor: Lance Bourque
Title: IC Design Engineer, Analog Devices, Inc.

Thesis Supervisor: Ruonan Han
Title: Associate Professor, Electrical Engineering and Computer Science

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To my parents who raised me and gave me the opportunity to commit time to intellectual passions, I am deeply grateful.

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Chapter 1

Motivation

Operational amplifiers are ubiquitous in analog electronics, and as modern technology progresses towards faster, smaller, and lower power devices, the need for innovation in operational amplifier design is no exception. Decreased power consumption without sacrificing performance is always beneficial in any electronic system, particularly modern consumer devices where every minute of battery life is critical. Very low noise amplification and signal conditioning is also critical to maintain signal integrity in every analog application. These key performance characteristics, paired with versatile rail-to-rail input and output voltage, small 5V version in SOT23 integrated package, and precision, result in a capable operational amplifier available for use in a wide array of high performance applications. Currently, Analog Devices does not offer an operational amplifier that meets the specifications achieved by this thesis project.

One natural application of the technology is a highly sensitive trans-impedance amplifier used to create a voltage proportional to photo-diode current as shown in figure 1-1.

Such a system can potentially be employed as part of a modern satellite, used for receiving information in the form of light from another satellite nearby. It is likely the the signal to noise ratio seen by the photo-diode is relatively low, and any substantial additional noise contributed by the operational amplifier would unacceptably reduce the system's ability to discern received signals from background noise. Clearly, the lowest power device which meets the noise and precision requirements demanded by

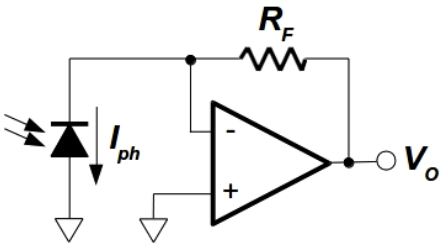

Figure 1-1: Trans-impedance Amplifier Example

such an exotic environment is the best choice. There are countless other applications for such a precise, low noise device. For example, precision low frequency analog front end circuits.

There are many technological and physical barriers to the design of such a low noise CMOS input operational amplifier. $1/f$ noise is present in all electronic devices, and one of the most straightforward means of reduction for a given device is increasing area. Unfortunately, to the first order, an increase in device area corresponds linearly with an increase in capacitance. The increased capacitance, if at the input of an operational amplifier, leads to reduced stability, reduced gain-bandwidth-product, and other issues. The unique strategy employed to address this substantial challenge is discussed extensively in the coming chapters. Also discussed are the employed more conventional means of designing a two stage, rail to rail input and output operational amplifier.

Chapter 2

Design Specifications & Associated Challenges

Specification	Value	Unit
Supply Voltage	30	V
Supply Current	100	μA
Technology	BiCMOS	
$1/f$ Noise 0-10 Hz	$<$500	nV_{PP}
GBW	600	kHz
C_{in}	$<$40	pF
Input Bias Current	≈ 0	nA
Rail-Rail I/O	Yes	
5V Package	SOT23	
Temperature Range	[-40,125]	°C

Table 2.1: Design Specifications

The many specifications required by this operational amplifier and the circuitry required to achieve them warrant detailed discussion, of which the remainder of this thesis is comprised. Although, a brief introduction to each significant requirement is detailed in this chapter.

2.1 Input Bias Current

A near zero input bias current requires the use of either CMOS or JFET input devices, as BJTs require a non-zero base current. Rail to rail JFET devices would require the use of an auxiliary charge pump circuit, while CMOS input does not. Therefore, CMOS input devices were chosen.

2.2 Noise

The most novel specification of this operational amplifier is the 500 nV_{PP} $1/f$ noise performance given the CMOS input devices. CMOS input devices, which typically have higher $1/f$ noise than JFET devices are used in this amplifier.

It is notable that the primary means of decreasing $1/f$ noise for a given device is by increasing size in the CMOS gate plane, so input capacitance needs to be balanced with noise in this design.

2.3 Input Capacitance

As mentioned in the previous section, decreasing $1/f$ noise necessarily increases input capacitance. An operational amplifier with too much input capacitance is likely to be unstable in feedback either due to the increased capacitive load on the output stage, or to a pole formed with the feedback resistance and the input capacitance, and would be an undesirable option in electronic systems.

Various techniques were employed while attempting to reduce the input capacitance while maintaining the $1/f$ noise performance. Luckily, the sub-threshold op-

eration of the MOS devices resulted in an advantageous inversion state, yielding low gate capacitance given the large device sizes.

2.4 Rail to Rail Input & Output

Rail to rail input and output terminals are a very convenient parameter for operational amplifiers to have in many applications. When the range of input and output voltages spans the entire supply, there is no need for stringent DC bias conditioning before applying a signal, or limiting amplitude restrictions (besides the supply voltage).

Input rail to rail is typically achieved by using both NMOS and PMOS input devices, as some NMOS devices can be used with $V_i = V_{DD}$ and some PMOS devices can be used with $V_i = V_{SS}$, given an appropriate devices geometry such that $|V_{DS}| > |V_{GS} - V_T|$; the device is operating in saturation. In this amplifier, native NMOS devices are used instead of PMOS to reach the low rail, which requires a novel low-overhead current source to supply the bias tail current. The novel methods of current sourcing, steering, and input device selection are described in this thesis.

Output rail-rail is achieved with a Monticelli output stage, and is described in depth as well.

2.5 Die Size

The required integrated package size is SOT23, therefore there is a physical size limit on the sum of all active and passive sections of the operational amplifier. This is particularly tricky because low power consumption leads to larger resistors for the same voltage. Also, low $1/f$ noise requires large devices, so a delicate balance of these properties is necessary for this design.

2.6 Power

The current consumption is limited to 100 μA from a 30V rail. Such low power forces almost all devices to operate in the sub-threshold region. As mentioned before, sufficient resistors are forced to be quite large to achieve substantial voltage drops with such low current.

Very low current consumption leads to relatively small values of trans-conductance g_m and large values of output impedance r_o. Amplifier bandwidth is limited primarily by the achievable g_m and capacitance. DC Gain is on the order of $g_m r_o$ and is potentially quite large due to the low power consumption since g_m increases linearly with drain current while in sub-threshold, as opposed to square root in saturation.

2.7 Gain & Bandwidth

High open loop gain reduces the closed loop offset voltage, so the open loop gain of the amplifier determines the closed loop offset voltage, and must be sufficiently high to achieve precise operation. The amplifier also employs digital trim for matching, though the details and design are beyond the scope of this thesis.

The bandwidth is determined by the open loop gain, first and second stage capacitance, and compensation network. The details of compensation are described in depth in the respective chapter.

2.8 Stability

Amplifier stability is intrinsically related to bandwidth through the compensation network design, as the main purpose of compensation is to ensure stability. Primarily, Miller compensation is used to stabilize the amplifier.

The low-overhead current source also requires a stabilization network, which is described in the respective chapter.

Chapter 3

High Level Architecture & Signal Path

The required specifications necessitate many building blocks of the overall system signal path. A high level diagram of the amplifier system is shown in figure 3-1. Justification for each element shown, and a brief explanation of its function is presented in this section. Thorough descriptions of each stage are detailed in the remaining sections.

3.1 Native NMOS Input

The input stage is comprised primarily of a differential pair of very large native NMOS devices. These devices are necessarily large to achieve minimal $1/f$ noise performance. Also, since the devices are native NMOS, the threshold voltage V_T is less than zero, allowing for operation of the devices near $V_{IN} = V_{SS}$. Since the amplifier must be able to accommodate rail-rail input voltage swing, the NMOS differential input pair must be provided tail current by a current source with near infinite output impedance while only seeing $|V_{GS}|$ of the NMOS input across it. Note that an input voltage of V_{SS} could more simply be handled by using PMOS input devices, though it was found that in this process, native NMOS devices provide superior $1/f$ performance.

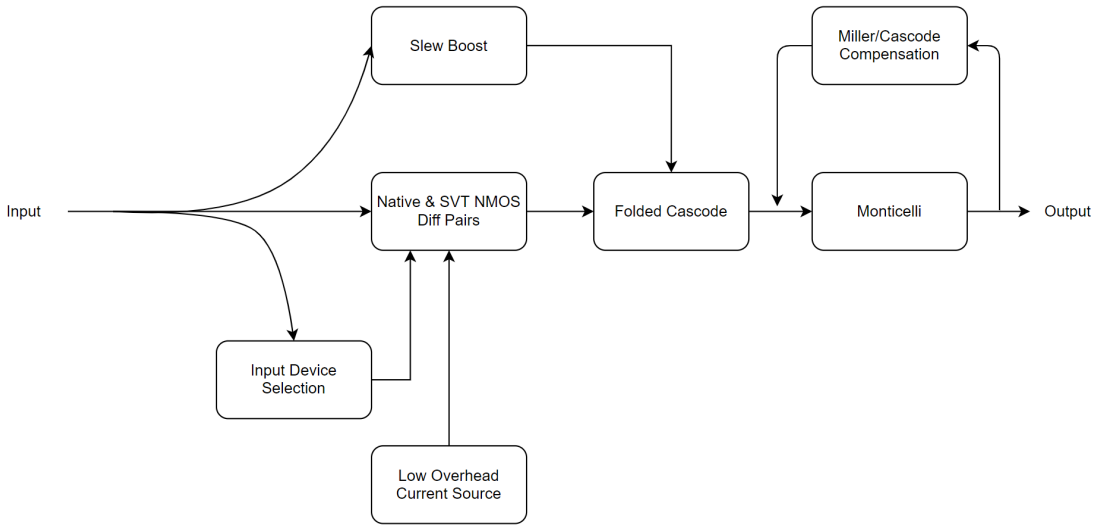

Figure 3-1: Full Circuit Block Diagram

3.2 Low Overhead Current Source

The current source which feeds the input differential pair needs to be able to operate with very little voltage across it. The inclusion of such a mechanism is required by $1/f$ noise minimization in this amplifier. The working principle of this current source is described in much detail in later sections, but a brief description is that output current is sensed and compared to the required output current, and the error is corrected using a high gain feedback loop, such that the gate voltage on the NMOS providing the output current is modulated in response to a changing drain voltage.

3.3 Standard NMOS Input

The input voltage also needs to be able to swing all the way to V_{DD}, which would not be sustainable with a negative V_T native NMOS device because the source voltage would need to be greater than V_{DD}. Therefore, also connected in parallel are a pair of usually inactive standard NMOS devices. The transition between these two input pairs needs to be as smooth as possible, and result in the same transconductance

g_m into the next amplifier stage. A robust input device selection mechanism was developed to accomplish this task.

3.4 Input Device Selection

Switching between input devices near $V_{in} = V_{DD}$ is accomplished by sensing the common mode input voltage and turning off transistor switches in series with the main input pair, as well as directing the bias current to the alternate input devices. Although, since this amplifier needs to accommodate 30V swing, the voltage driving the gate of the switch transistors also needs follow the common mode input voltage during nominal operation so that the maximum V_{gs} of the switching devices (5V) is not exceeded by a switching mechanism sitting near V_{DD}.

3.5 Folded Cascode

The current transduced from the input devices is "folded" over into a high gain and wide-input-swing-accommodating high impedance stage. The folded cascode allows for input voltages near V_{DD} and very high impedance yielding high first stage gain. Many devices in this stage also need to optimized for low $1/f$ noise performance due to their proximity to the input of the signal path.

3.6 Monticelli Output Stage

The output voltage also needs to be rail-rail, necessitating the use of a common source output stage, which is achieved with a Monticelli output[8] configuration. The high gain and high DC output impedance of the Monticelli stage make this amplifier into more of a transconductance amplifier. Details of the design and operating principles are covered in the associated section.

3.7 Slew Boost

When a large differential voltage is applied to the input in the form of a large step, the input differential pair can maximally provide the total tail current to one side, yielding non-linear response of the entire amplifier for large differential input voltages. This limitation is reconciled by the use of a parallel, nominally inactive, slew boost circuit that is also comprised of a heavily degenerated differential pair transconductance feeding directly into the folded cascode.

3.8 Compensation

Given the high DC gain and capacitive dynamics of the entire two stage amplifier, instability is all but guaranteed when the device is connected in negative feedback due to the two dominant poles existing significantly before the unity gain cutoff frequency. Miller compensation and intentional right half plane zero removal are employed to ensure feedback stability for reasonably sized load capacitance.

Chapter 4

Flicker Noise & Native NMOS Input

Given the stringent input referred flicker noise requirement for the operational amplifier, much consideration was given to the noise performance of the first devices in the signal chain since they have the most substantial impact on total noise performance. This section will describe the unique characteristics of flicker noise, decision to use native NMOS input devices, and the associated design challenges.

4.1 Flicker Noise

The standard MOSFET simulation model BSIM4 [11] empirically models drain current flicker noise as:

$$S_{id}(f) = \frac{K_F I_{DS}^{AF}}{C_{ox\_eff} L_{eff}^2} \frac{1}{f^{\epsilon}} \tag{4.1}$$

This model is generally considered to be oversimplified, although it used throughout this thesis due to the ease by which it is related to the gate voltage noise spectrum $S_{vg}(f)$ through g_m.

There are a couple different theories based on first principles which attempt to describe the fundamental mechanisms that directly cause noise with a spectral power density that follows a $1/f$ characteristic [5].

4.1.1 The McWhorter Model (Number Fluctuations)

The McWhorter model states that flicker noise is generated by fluctuations in the number of carriers due to charge trapping in surface states, such as SiO_2-Si interface under the gate of a MOSFET. The necessary $1/f$ spectrum is obtained by assuming the time constant τ of the surface states varies with a $1/\tau$ distribution.

4.1.2 The Hooge Model (Mobility Fluctuations)

The Hooge model states that flicker noise is generated by fluctuations in the resistance that follow a $1/f$ spectral density.

Both models have received some experimental and theoretical support, but still carry some empirical parameters in the final spectral density expressions.

4.1.3 Simplified Empirical Model

A much simplified empirical model for the input referred voltage flicker noise power spectral density, which with reasonable accuracy captures the noise spectrum with the correct parameters is as follows:

$$S_{vg}(f) = \frac{K_V}{L_{eff}W}\frac{1}{f^{\epsilon}} \tag{4.2}$$

Where K_V and ϵ are curve fitting parameters, and ϵ is assumed to equal 1. Note that according to equation 4.2, $S_{vg}(f)$ depends only on device gate area and not on the bias condition. While searching for the lowest $1/f$ noise device to use as the input to this operational amplifier, direct comparison of K_V was used to reflect performance.

4.1.4 Device Options

In a typical operational amplifier design, substantial attention is given to the noise sourced from the input differential pair. Typically when minimizing flicker noise, one would attempt to use non MOS input devices such as bipolar junction transistors (BJT) or junction field effect transistors (JFET). Each of these options has a sub-

stantial physical or practical disadvantage in this amplifier, necessitating the use of MOSFET input devices.

BJTs require substantial input current to operate, which would violate the need for near zero input bias current to this amplifier, therefore they are disqualified from consideration at the input of this amplifier. Although, the low flicker noise properties of BJTs are taken advantage of within the folded cascode section, which is detailed in the appropriate section.

JFETs do not require substantial input bias current, although typically still more current than MOSFET devices due to their gate junction leakage. The principal challenge associated with using JFET input devices is the need to develop a charge pump circuit to keep the devices biased properly (out of the triode regime) throughout the entire rail to rail operation. Although the use of JFET devices would likely have reduced flicker noise power substantially, it was determined that the design of a robust charge pump circuit was out of the scope of this thesis.

4.2 Device Advantage

After deducing that the only reasonably zero input bias current devices are MOSFET, the question of which MOSFET devices to use was answered by comparing the flicker noise performance of each device based on measured data shown in figure 4-1. The details of each axis are redacted to maintain the security of internal Analog Devices intellectual property, but the green markers correspond to the native NMOS devices. The markers which have lower S_{vg} than the native NMOS are substantially larger, meaning the K_V is not actually greater than the native NMOS devices. Therefore, native NMOS were chosen as the appropriate input devices after normalization over device area.

After deducing that the native NMOS devices would provide the lowest flicker noise contribution, attention was turned to the feasibility of using such devices, as they are typically deemed too unreliable for critical use.

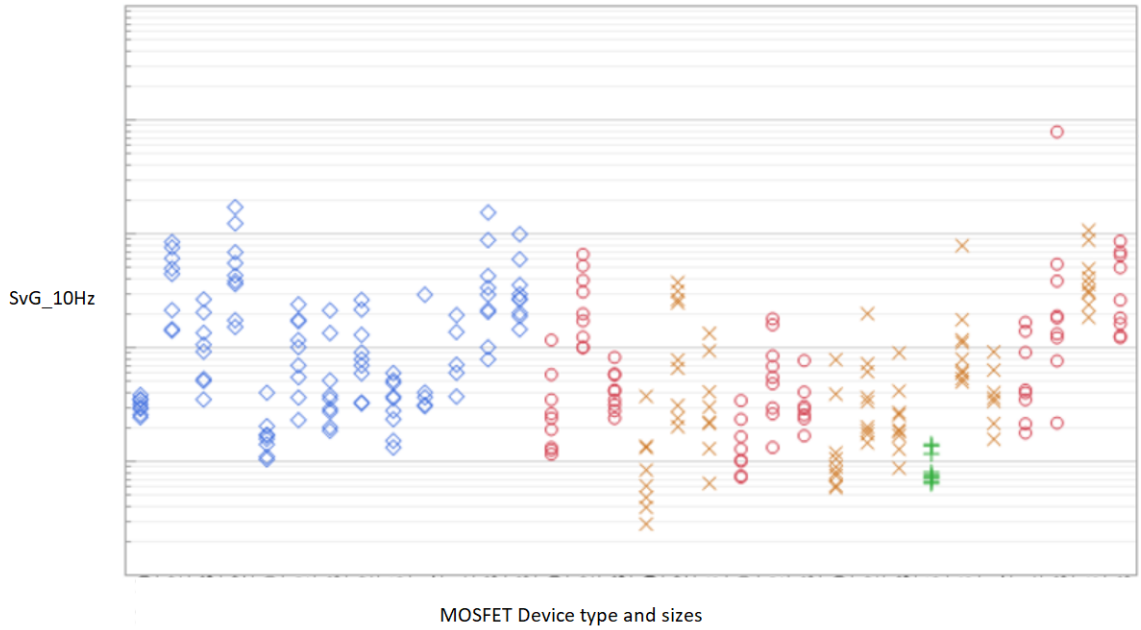

Figure 4-1: MOSFET 1/f Noise Measurements

4.3 Native NMOS

Native NMOS [2] devices are MOSFETs that don't have a channel implant and typically have a threshold voltage around 0V. The low threshold voltage is achieved by a lack of channel doping, yielding a MOSFET placed in a native Si tub.

Depicted in figure 4-2, the typically p type body would have few dopants, lowering the threshold voltage from the typically heavily p doped implant in standard V_T NMOS. Therefore, the channel would be conductive unless a sufficient negative V_{gs} is applied to bring the channel into a p type regime, by reducing the concentration of electrons and increasing the concentration of holes.

4.4 Challenges & Solutions

4.4.1 Reliability

The primary concerns with using native NMOS devices as the input differential pair to this operational amplifier are the reliability of the simulation model, and sensitivity of key parameters to variation in channel length and minor process shifts. If the simula-

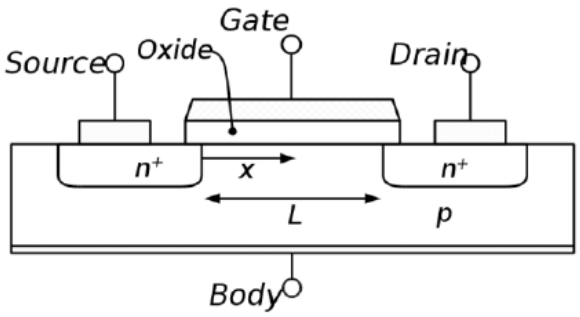

Figure 4-2: NMOS Cross-Section [6]

O : Available for Vgs<0V

5V NAT device		Length			
		1.6	2	4	10
Width	1.2	O	O	O	O
	3	X	X	O	O
	5	X	X	O	O
	10	X	X	O	O

Figure 4-3: Native NMOS Size Limitations

tion models are inaccurate, the devices obviously can not be used to support a reliable amplifier, and standard PMOS input devices must suffice. If certain parameters such as g_m and V_{gs} are too sensitive to length and process variation, small inconsistencies have the potential to substantially impact precision amplifier performance.

Figure 4-3 roughly conveys which dimensions of native NMOS devices can be reliably simulated in this TSMC process. Clearly, devices wider than approximately 3um are not reliably modeled for lengths less than approximately 2um. For devices shorter than this length, TSMC does not suggest using them at all in designs, as drain-source punch-through may render the transducer effect useless.

To ensure the low variability of critical device parameters such as g_m and V_{gs}, these parameters were simulated at the approximate input device width required to achieve sufficiently low flicker noise performance, shown in figures 4-4 and 4-5. Finalized device length was set to 14um, well beyond the regime of punch-through, and sufficiently greater than the $<3\mu$m length regime that yields high key parameter

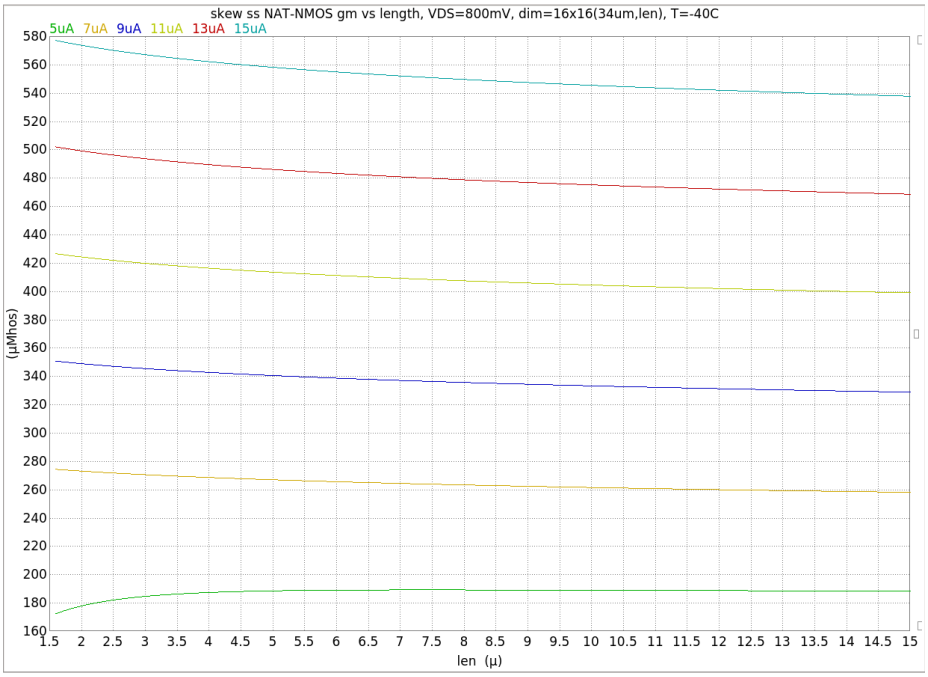

Figure 4-4: Native NMOS g_m vs. Length and I_d

variability.

4.4.2 Noise Model

A key drawback of using the native NMOS devices in the amplifier, was the unavailability of a flicker noise model that was accurate in the deep sub-threshold region of operation of the input native NMOS device. Without an accurate representation of the flicker noise at the input of the amplifier, there is no hope of reliably characterizing the total input referred noise of the entire amplifier.

Luckily, measured flicker noise data was available for some bias conditions for the native NMOS in this process. Given the simplicity of equation 4.2, the parameter K_V can be easily extrapolated from the measurement data if measured device dimensions and frequency are also provided.

Given that the parameters in the flicker noise model in BSIM4, given by equation 4.1, can be modified at simulator run time, just before running noise simulations, the native NMOS flicker noise can be accurately simulated based on the extrapolated flicker noise coefficient K_V from the measured data. All that is required is the

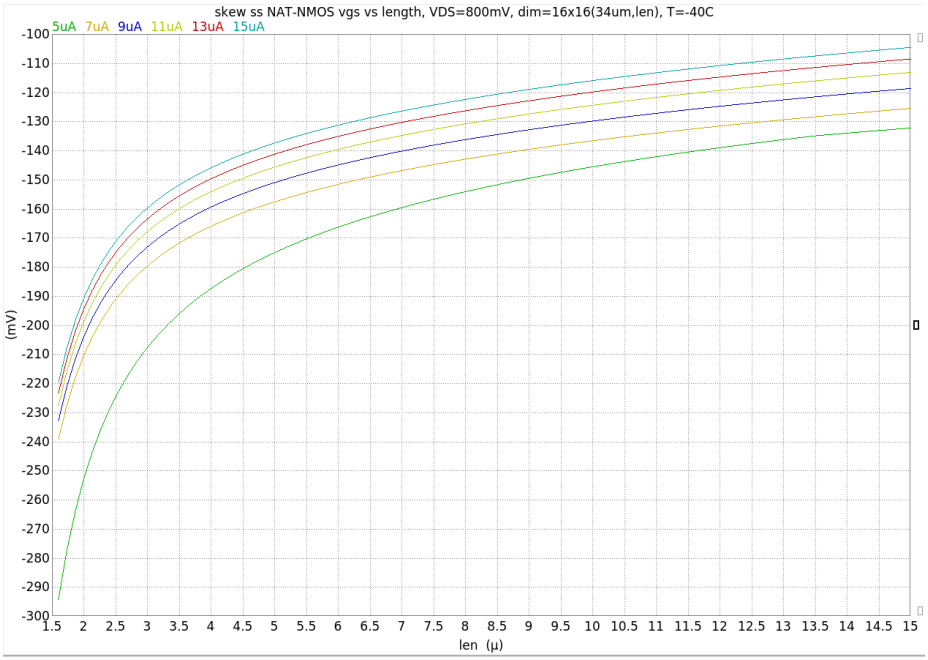

Figure 4-5: Native NMOS V_{gs} vs. Length and I_{ds}

transconductance g_m and drain bias current I_D from the operating point of interest, since the power spectral density (PSD) of the gate voltage and drain current flicker noise are readily proportional by g_m.

$$S_{id} = g_m^2 S_{vg} \tag{4.3}$$

Using equations 4.1, 4.2, and 4.3, an accurate and bias dependent expression for K_F can be written as:

$$K_F = \frac{K_V g_m^2 C_{ox\_eff} L_{eff}}{I_D W} \tag{4.4}$$

This expression is clearly dependent upon fundamental characteristics of the device extrapolated from measured data, K_V, and the bias point, g_m and I_D. Simply setting the BSIM4 flicker noise parameter K_F equal to this value allows reliable simulation of drain current flicker noise at any reasonable bias point, given the assumption of equation 4.2 holds, which it usually does for reasonable device sizes.

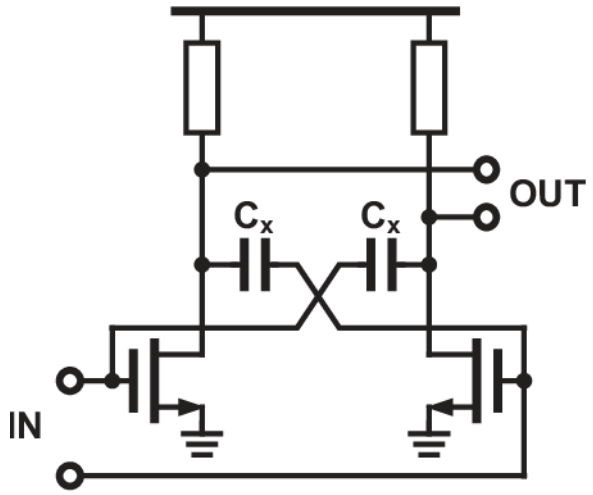

Figure 4-6: Cross Coupled Capacitance Neutralization Example Circuit

4.4.3 Gate Capacitance

Initially, it was reasonably assumed that very large input devices, which are required for very low flicker noise, would necessitate very large uncompensated input capacitance. Very large input capacitance would be detrimental to the overall performance of the amplifier for many reasons. Mainly, the closed loop stability and bandwidth would be reduced. Also, the whatever circuit is driving the input to the closed loop operational amplifier would be forced to drive a substantial capacitive load, further reducing the bandwidth.

One technique to deal with this problem is known as cross-coupled-capactive-neutralization, and was explored extensively. The key issue with this technique for this particular circuit was the voltage gain required to feed-back current through a neutralization capacitor was reduced once a low frequency pole was reached in frequency, which then caused the capacitance to increase from the typical non-compensated value. Also, differential capacitive neutralization relies upon a gate to drain voltage gain substantially greater than unity to achieve a reasonable match of C_{gd} and the cross coupled neutralization capacitors. Figure 4-6 demonstrates this technique.

Luckily, cross coupled neutralization was not necessary to achieve relatively low input capacitance considering the very large size of the input devices. Optimizations were made to to the length of the input devices to reduce the input capacitance as

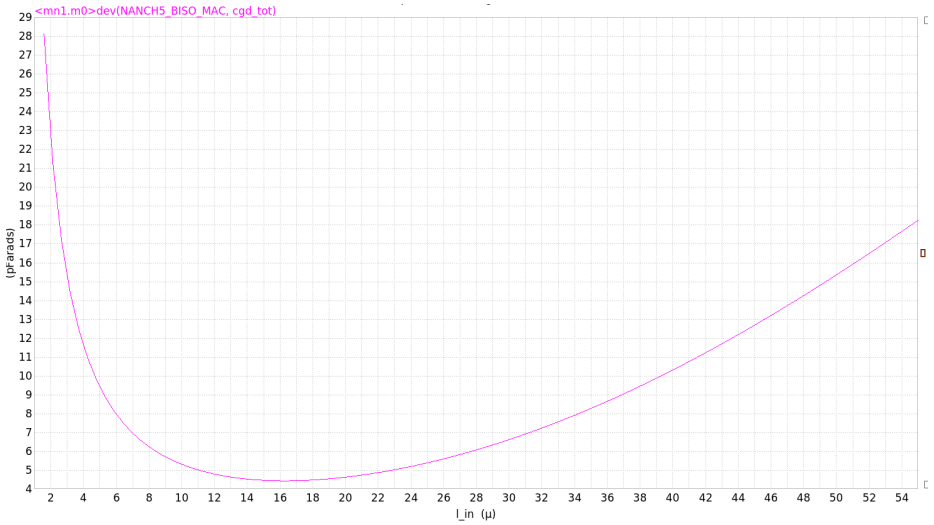

Figure 4-7: Native NMOS Gate Capacitance vs. Length

shown in figure 4-7.

Also, due to the very low current being used throughout this entire amplifier, less than 100μA, and the very large input devices, they are operating in sub-threshold, and therefore the MOS capacitor of each device is operating in the depletion regime. In the depletion regime, an inversion layer has not formed in the channel, and the effective thickness of the MOS capacitor dielectric is substantially greater, therefore reducing the capacitance. This effect is illustrated in figure 4-8.

Selecting the device length that minimized input capacitance while maintaining sufficient g_m, yielded common mode and differential input capacitance as a function of frequency shown in figures 4-9 and 4-10.

The dynamics of the high frequency capacitive distortion are not analyzed in depth in this thesis, although the very low frequency, around 1 Hz, substantial decrease in common mode input capacitance is likely a computational error.

4.4.4 Small Negative V_{gs}

The native NMOS devices, at the size necessary to achieve sufficiently low flicker noise, and biased with approximately 9μA of total drain current, have a V_{gs} of about -120mV. The magnitude of this negative V_{gs} is substantially less than the typical PMOS $|V_{gs}|$ that would be used to operate the input stage at a common mode input

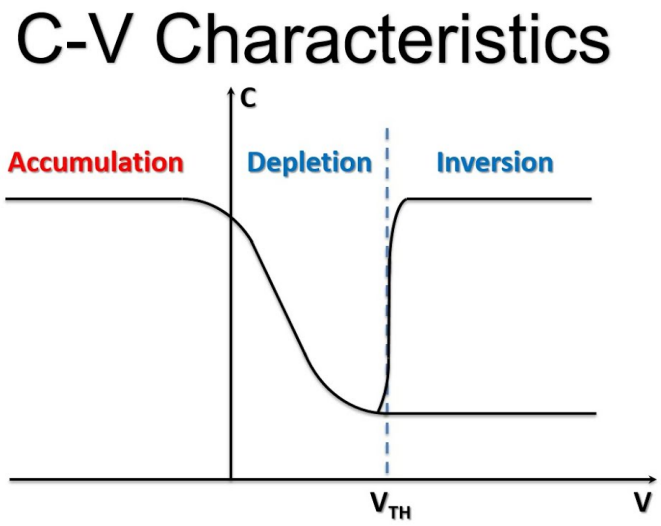

Figure 4-8: Generic MOS Capacitor vs. Gate Voltage

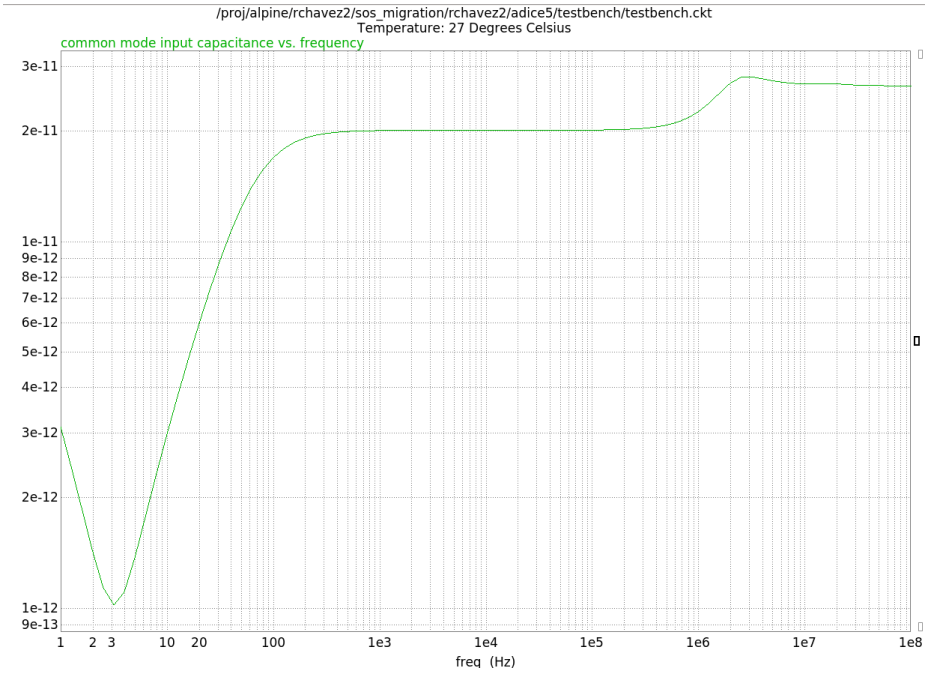

Figure 4-9: Native NMOS Common Mode Input Capacitance vs. Frequency

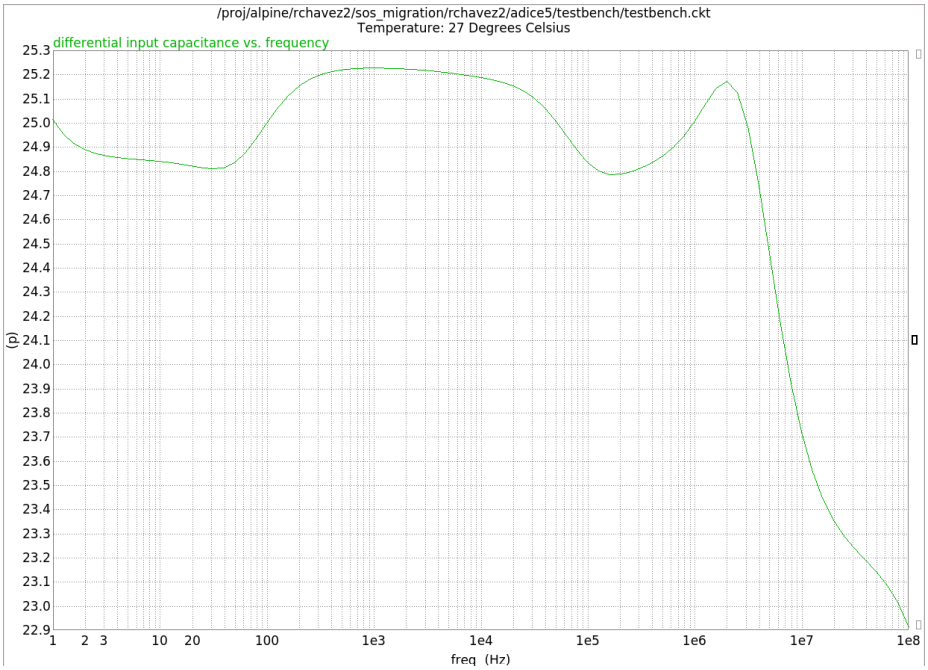

Figure 4-10: Native NMOS Differential Mode Input Capacitance vs. Frequency

voltage of V_{SS}. Also, the PMOS devices operating near $V_{cm} = V_{SS}$ is limited primarily by the minimum V_{ds} that would leave the device in saturation and preserve consistent input stage g_m.

While using native NMOS devices with $V_{cm} = V_{SS}$, the minimum V_{cm} is limited primarily by the magnitude $|V_{gs}|$ and the minimum V_{ds} that the tail current source can sustain with constant output current. Also, even if current is maintained near the quiescent level, the output impedance must remain very high to maintain sufficient common mode rejection.

For these reasons, a *low-overhead current source* was developed to allow the use of low flicker noise native NMOS devices operating near and at $V_{cm} = V_{SS}$. The design and results of this novel current source are discussed in detail in chapter 6.

4.4.5 Cascode Pole - Body Terminal g_m Boost

The input differential pair needs to be cascoded for two primary reasons. First, the native NMOS input devices have a maximum V_{dg} of 5V before permanent damage occurs due to high oxide field effects. Since this amplifier needs to operate with a

maximum 30V supply, most devices either need to cascoded with high V_{dg} tolerant DMOS devices, or replaced with them. Second, the input stage feeds directly into the folded cascode, and the high output impedance provided by the cascode devices translates directly into a more ideal transconductance stage.

The cascode devices also introduce another pole into the transconductive dynamics of the input stage, shorting out some of the output current into the shunt capacitance seen at the intermediate node. This pole frequency is determined primarily by the g_m of the cascode devices, C_{gs} of the cascode devices, and C_{gd} of the native NMOS input devices. A balance between the between the g_m and C_{gs} of the cascode devices was required to push the pole as far out in frequency as possible, while maintaining sufficient total output current.

The pole at the intermediate node between the native input devices and the cascode devices is nominally at about the angular frequency g_m/C. Therefore, any increase in g_m will increase the pole frequency. One method of increasing the effective g_m is by tying the body of each cascode device to the source of the other cascode device. This works because the voltage swing at intermediate node is non-zero due to the impedance seen at that node, and the body of each MOS device negatively modulates its threshold voltage. A decrease in threshold voltage increases the drain current in the same way as the gate voltage g_m, and is described by the back gate transconductance g_{mb}. Therefore, since the intermediate nodes have opposite polarity, the effective transconductance g_{m_eff} is greater than without the cross-coupled body terminals. The increased g_{m_eff} directly translates into an increased cascode pole frequency, further idealizing the dynamics of the input stage across the necessary frequency range.

4.5 Final Primary Input Stage

The finalized simplified schematic of the native NMOS input stage is shown in figure 4-11. **U1** and **U2** are the native NMOS devices, while **U3** and **U4** are the 30V tolerant DMOS cascode devices. The cross-coupled body ties are readily apparent.

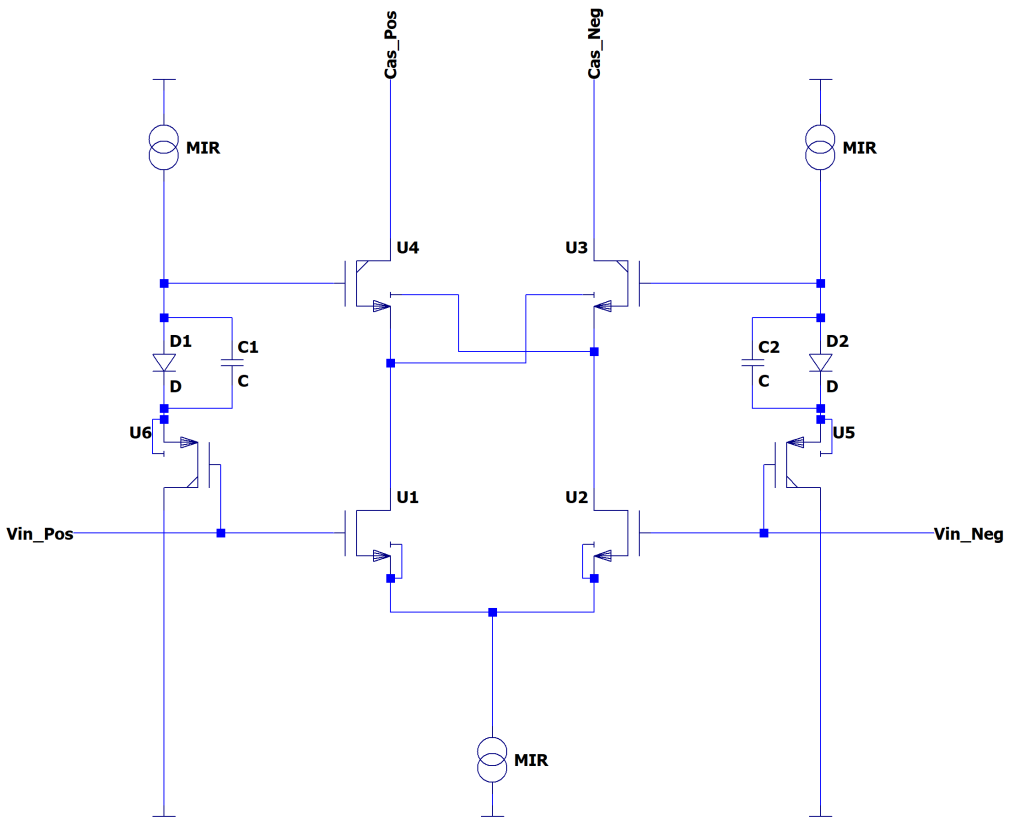

Figure 4-11: Simplified Native NMOS Input Schematic

Biasing of the cascode device gates is also shown to be differential, and driven by high voltage PMOS (to account for 30V common mode range) and a diode to allow for suitable headroom across the native NMOS devices. Capacitors **C1** and **C2** are used to push out the pole associated with these bias networks.

Chapter 5

Rail-Rail Input Device Switch

5.1 Mechanism Justification

To allow for the input to consistently transduce current when the common mode input voltage is near V_{SS} or V_{DD}, two types of devices need to comprise two complementary differential input pairs that route current to the folded cascode.

Typically, an NMOS differential pair is placed in parallel with a PMOS differential pair, as shown in figure 5-1. This method requires two tail current sources, each driving a differential pair. Also, both differential pairs can either be on constantly or switched on and off relative to the common mode input voltage.

This amplifier design uses native NMOS input devices for the majority of the common mode input range, and switches to a pair of standard threshold NMOS devices near $V_{cm} = V_{DD}$. At the higher end of V_{cm}, the native NMOS input devices can no longer sustain the required negative V_{gs} to conduct the tail current, they also triode. Resolution of this issue requires placing standard NMOS devices with a positive threshold voltage in parallel, and routing the current to them instead. Standard NMOS devices can have a gate voltage at V_{DD} and drain voltage less than V_{DD}, as long as the drain voltage is not more than a threshold voltage beneath V_{DD}, which can be enforced with proper folded cascode design.

There are many challenges with designing such a switched input mechanism, particularly because of the required 30V common mode input voltage range. Also, the

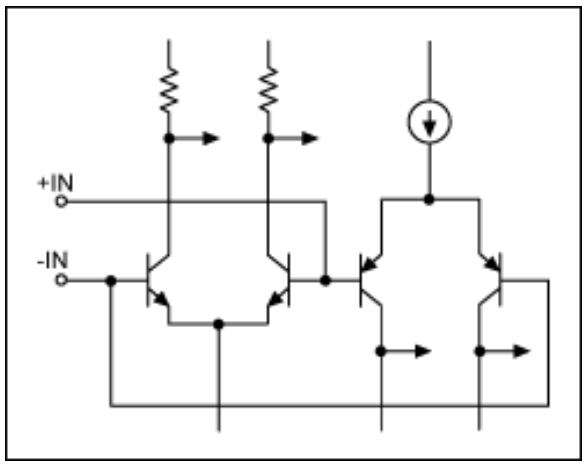

Figure 5-1: Standard P-type & N-type Rail-Rail Input Stage [9]

very large native NMOS input devices yielding non-negligible input capacitance pose a problem when connecting the alternative differential pair. These issues and associated solutions are described in this chapter, as well as the circuits that make input selection relative to V_{cm} possible.

5.2 V_{cm} Tracker

The mechanism to switch between input differential pairs could be quite simple, if it weren't for the fact that this is a 30V operational amplifier. More than half of the transistors in the entire amplifier are rated for less than 5V gate to drain/source voltage, before permanent damage occurs to the devices. For this reason, the mechanism that is sensing the common mode input voltage and switching between devices can not be comparing the common mode input voltage to a constant *switching threshold*. If a constant switching threshold were used, there would be instances where the difference between that threshold threshold and the common mode input voltage are greater than 5V, damaging the transistors comprising the switching circuit.

The most straightforward means of resolving the 5V breakdown voltage issue is to create a switching threshold voltage which tracks the input common mode voltage, but is offset by a sufficient amount such that the proper input differential pair is selected for use. A simplified version of the circuit that achieves this requirement is

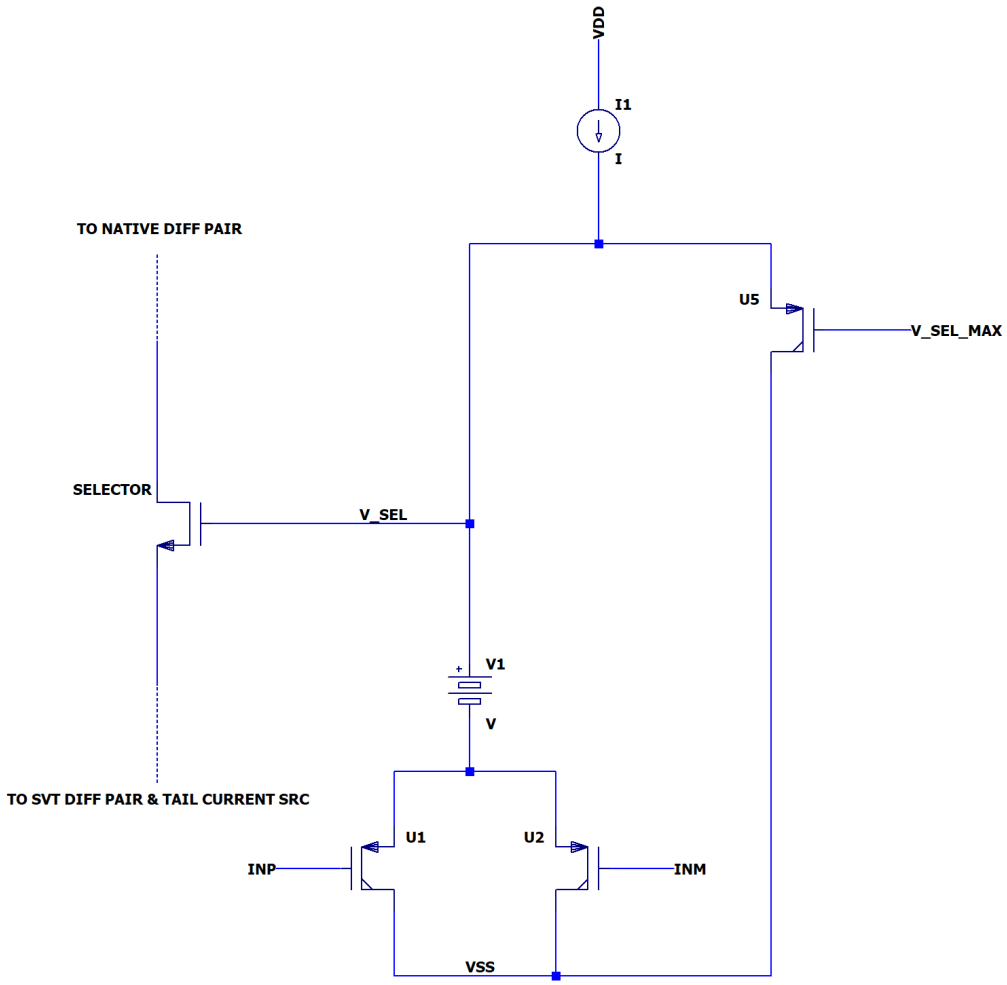

Figure 5-2: Simplified Common Mode Input Voltage Tracker Circuit

shown in fig 5-2.

A differential pair comprised of two high voltage PMOS devices, **U1** and **U2**, is driven by the differential input to the operational amplifier. An offset common mode input voltage is generated at the common source node, and is further offset by an effective "battery" to generate the switching threshold voltage labeled V_{SEL}. Over the lower part of the common mode input voltage, V_{SEL} is about 3V greater than the common mode input voltage, and drives the input device selection circuits when compared with the common mode input voltage. Although, this voltage must not always be greater than V_{cm}, otherwise the native NMOS input devices would

always be selected for use. Device **U5** in figure 5-2 sets the maximum V_{SEL} voltage that can be achieved with this common mode tracker, because once V_{SEL} is equal to V_{SEL_MAX} plus U5's V_{gs} when conducting tail current, V_{SEL} will not increase further due to the **U5**'s conducting all of the bias current.

This input common mode voltage tracking mechanism allows for the switching devices, such as **SELECTOR**, to operate properly without being destroyed by greater than 5V gate to source/drain voltages. The means by which these switching devices turn on and off the alternative differential input pairs are described in the following sections.

The resulting behavior of the common mode input tracking circuit is shown in figure 5-3. It is clear that for V_{cm} less than about 28.4V relative to VSS, V_{SEL} is sufficiently greater than V_{cm}, but beyond this threshold value, V_{cm} is greater than V_{SEL}, yielding voltages that can be compared to switch between input differential pairs without breaking the 5V devices.

There are a few issues with using the difference between V_{SEL} and V_{cm} directly to control the switching devices, particularly the gate connections. Namely, the two voltages converge and diverge rather *slowly*, meaning the MOSFETs that are sensing the difference will turn on and off rather *slowly*, which may not yield desired behavior.

5.3 Current Routing

A simplified schematic of the current routing circuit and gate switching mechanism is shown in figure 5-4. It is clear that the native NMOS differential pair and standard NMOS differential pair are in parallel, besides the additional **SELECTOR** device in series with the native NMOS pair. The gate of the **SELECTOR** device is driven by the V_{SEL} voltage generated by the common mode input tracker. When the native NMOS input devices should be conducting, the V_{SEL} voltage is about 3V greater than V_{cm} so **SELECTOR** is heavily trioded, and needs very little V_{ds} to conduct the full tail current through the native NMOS differential pair. It is also clear that the common source node that the native NMOS and standard NMOS differential pairs

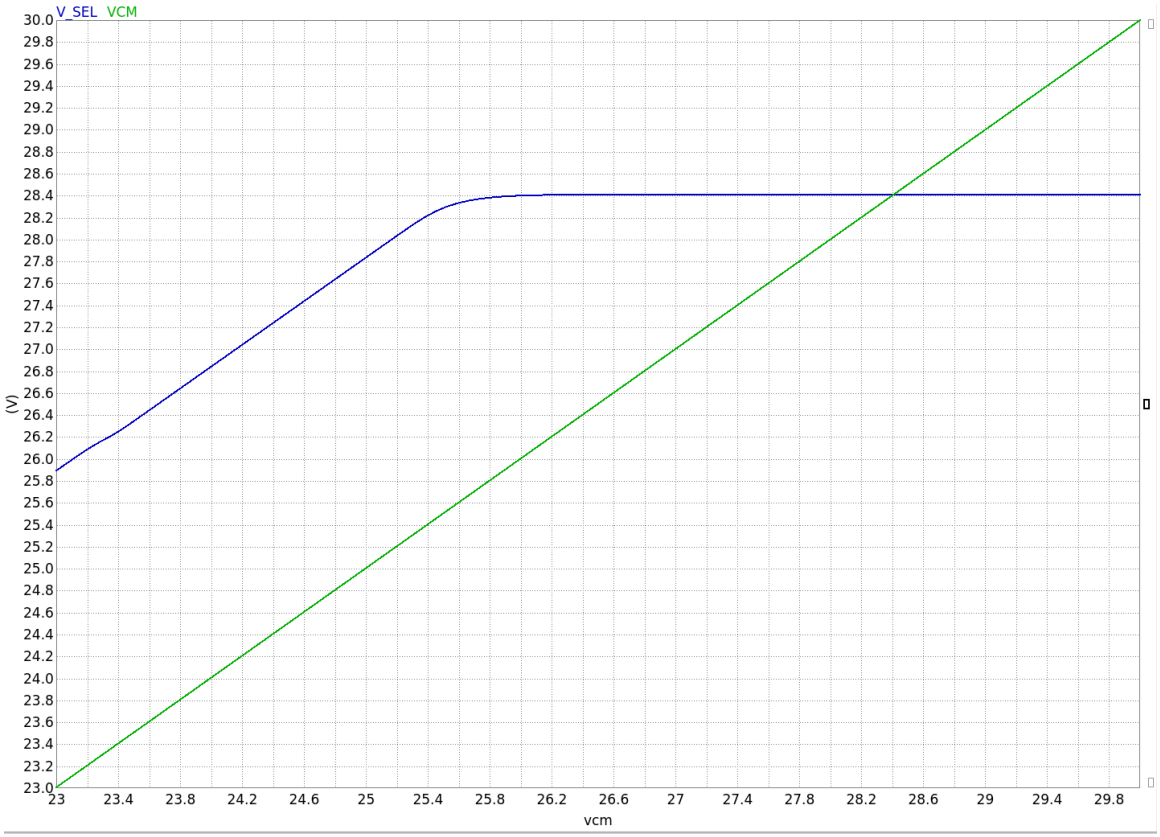

Figure 5-3: Common Mode Input Voltage Tracker Output

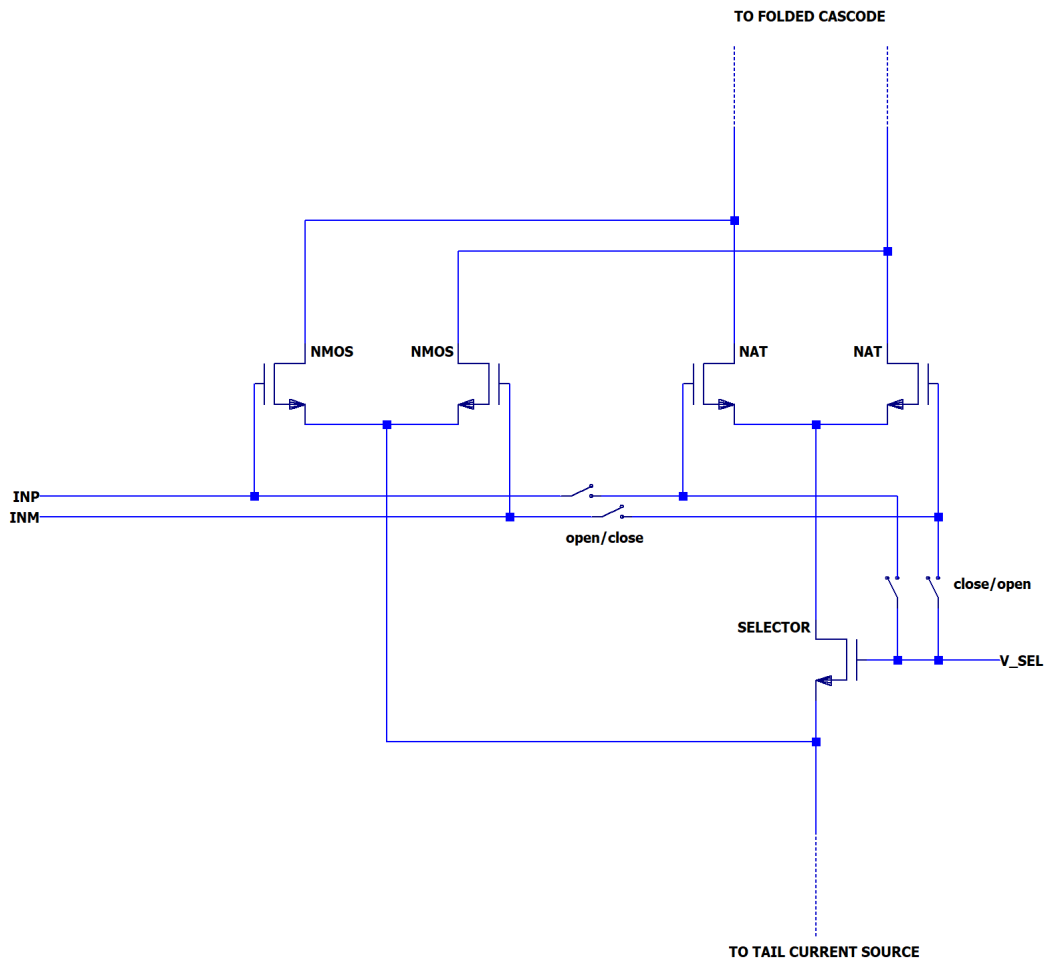

Figure 5-4: Input Differential Pair Switching Mechanisms

effectively share is driven by the negative V_{gs} of the native NMOS devices. If the shared source node were driven by the standard NMOS devices, the native devices would be greatly over-driven and should be conducting all the current, but it was already assumed that the standard NMOS were conducting and driving the source node, yielding an inconsistency. Therefore, when **SELECTOR** is on, the native NMOS devices are conducting and the standard NMOS devices are not. A simpler way to think about this switching mechanism is that the standard NMOS devices are half of a differential pair with the NMOS **SELECTOR** device.

While V_{SEL} is greater than V_{cm}, the native NMOS devices conduct the tail current, and while V_{SEL} is less than V_{cm}, the standard NMOS devices conduct the tail current.

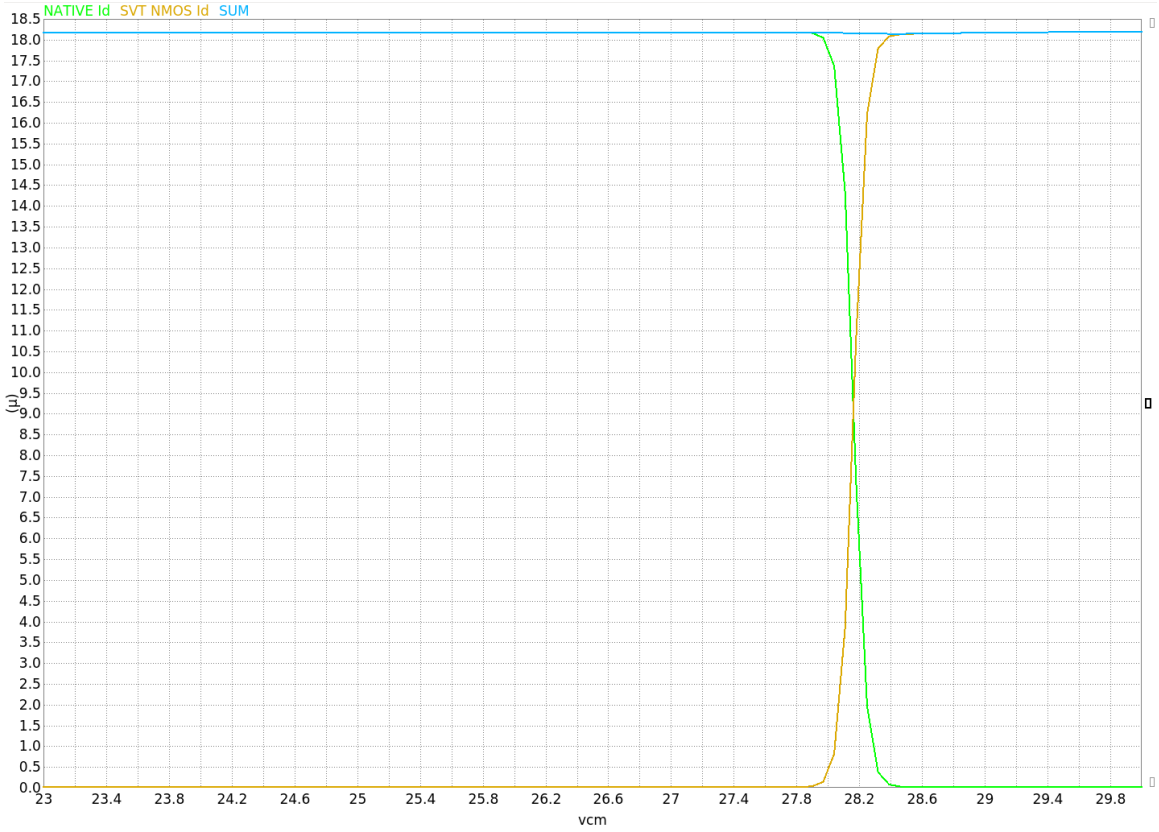

Figure 5-5: Input Differential Pair Current Routing Results

The results of this switching mechanism are shown in figure 5-5. The resulting behavior very closely resembles that of a differential pair that is heavily one-sided for the majority of full amplifier common mode input voltages. Note, the sum of the currents through the native NMOS and standard NMOS devices is constant throughout the entire common mode input range.

Although the full tail current fed into the folded cascode is constant, the parameter of interest is actually the total g_m from the input stage to the folded cascode. Attempts were made to make the standard NMOS g_m as close to the native NMOS g_m by varying device sizes. With more time for this thesis, a delta in the tail current occurring at the switching boundary could more appropriately maintain a constant g_m when V_{cm} is near VDD.

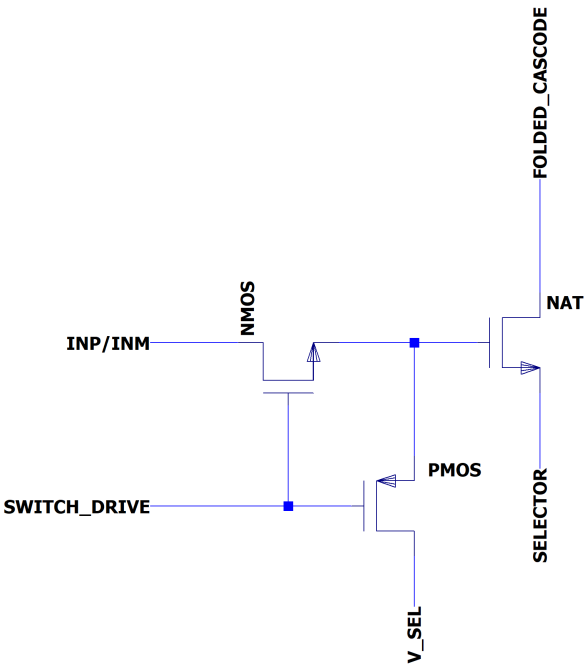

Figure 5-6: Native NMOS Gate Switches

5.4 Gate Switch

The native NMOS input devices are extremely large, and as described in chapter 4, have common mode and differential mode input capacitance of approximately 20pF while conducting 18μA of current total. This relatively low input capacitance is only achieved due to the bias point of the MOSFET gate capacitor when 18μA of current is being conducted. When the devices are no longer conducting, and the standard NMOS devices are conducting instead, the input capacitance increases dramatically, likely due to the native NMOS devices entering accumulation mode, and the effective capacitor thickness being reduced to basically t_{ox_eff}.

The dramatically increased native NMOS gate capacitance when V_{cm} is near VDD is unacceptable for the performance and stability of the operational amplifier. Therefore, the gate connection to the native NMOS devices must be opened and closed upon device switching in addition to current routing.

Figure 5-4 shows how the native NMOS gate connection circuit fits into the entire input stage, and figure 5-6 shows a detailed view of the complementary NMOS and

PMOS switching devices for one side. Ideally, the gate connection should be instantly switched off when the native NMOS device capacitance begins to increase and the tail current begins to decrease, but the total g_m needs to have a smooth transition to the standard NMOS g_m. The need for a *quick* gate switching action is difficult to achieve with series and shunt NMOS and PMOS devices respectively if the V_{SEL} voltage is directly used as the gate drive for the switches. Both the NMOS and PMOS devices need at least a V_{th} to open and close, so the transition would occur slowly and likely not at the desired V_{cm} voltage.

This issue is reconciled by using a gate switch drive circuit detailed in figure 5-7. The circuit operates on the principle of a differential pair comparing the common mode input voltage to the common mode tracking V_{SEL} voltage. Devices **U1** and **U2** sense the common mode input voltage, and are in parallel with U3 which is driven by V_{SEL}, the current is routed to either side depending on the relative values of these voltages. When **U1** and **U2** are conducting, the current **I1** is mirrored to the **SWITCH_DRIVE** node and pulls **SWITCH_DRIVE** down through **U4**, leaving the voltage a V_{gs} beneath V_{SEL}; note that since **U3** is not conducting, the mirror **U3** feeds into is not conducting either. Alternatively, when **U3** is conducting and **U1** and **U2** are not, the **SWITCH_DRIVE** voltage is pulled up to a diode voltage and threshold voltage above V_{SEL} through **U5** and D1; note that the mirrors that **U1** and **U2** feed into are not conducting since U1 and U2 are not conducting.

This new **SWITCH_DRIVE** voltage still tracks the common mode input and V_{SEL}, but can sufficiently overdrive the gate connection NMOS and PMOS devices around the transition point. This circuit also avoids damage to the switching devices by driving the gates by a voltage that is never greater than 5V away from V_{cm}. Also, the PMOS devices *hold* the gate voltage of the native NMOS devices at V_{SEL}, the voltage that the V_{cm} reaches upon transition to the standard NMOS input devices. Without the *holding* of the large gate capacitors at this value, substantial distortion would result from the charging and discharging of the native NMOS input devices upon transition between the two input pairs.

The resulting SWITCH_DRIVE voltage and native NMOS common mode gate

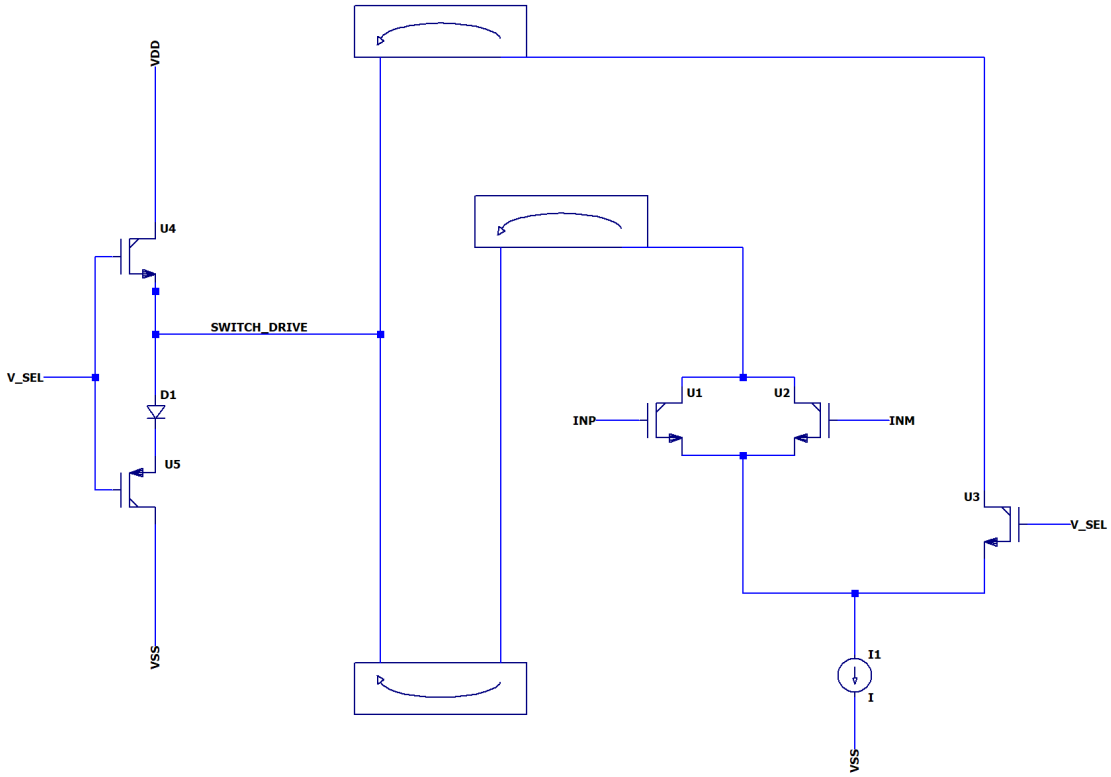

Figure 5-7: Native NMOS Gate Switch Drive Circuit

Figure 5-8: Native NMOS Gate Switch Results

voltage are compared to the common mode input voltage V_{cm} in figure 5-8.

It is clear that a small amount of distortion can occur upon this transition, as apparent in the black trace of figure 5-8. The key results of this switching circuitry is shown in figure 5-9. Around the transition between a native NMOS differential input pair to a standard NMOS differential input pair, the total g_m coming out of the input stage has a smooth and relatively small transition, yielding a small disturbance to the total amplifier behavior. The reduced g_m at $V_{cm} > 29.6$V is due to the failure of the low-overhead current source, which will be described in chapter 6. With more time for work on this thesis, an additional switching mechanism would have been added to the current source to avoid this. Although, 400mV away from V_{DD} is very nearly common mode input at high-side rail operation.

Figure 5-9: Input Stage g_m Near Input Device Switching Voltage

Chapter 6

Low Overhead Current Source

The NMOS input differential pairs require an NMOS current source to provide the necessary bias current. Throughout the majority of the input common mode voltage levels, a standard constant gate voltage current source would provide a fairly constant output current. Although, the native NMOS input devices need to be able to operate at $V_{cm} = V_{SS}$, and since the gate to source voltage V_{gs} of the native NMOS devices is approximately -200 mV, this would require an NMOS current source that can provide a sufficient output current with only 200 mV of drain to source voltage. 200 mV proved to be too small a voltage for a standard current source, and would reduce the output current to nearly zero.

The requirement for amplifier operation when $V_{cm} = V_{SS}$ and using native NMOS input devices therefore necessitates the design of a new type of current source that can operate with very low drain to source voltage. Given the many potential methods of achieving this goal, much of the time spent on this thesis work was exploring and designing potential circuits to meet this requirement.

6.1 Initial Considerations

Inspiration for the design of the low overhead current source was initially taken from the circuit shown in figure 6-1, taken from an academic paper by Kush Gulati and Hae-Seung Lee in 1998 [4].

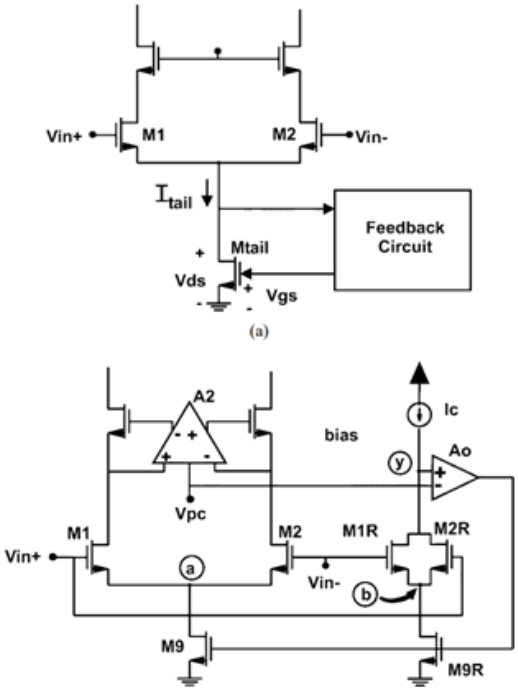

Figure 6-1: Initial Low Overhead Current Source Inspiration

The concept of a low overhead current source is implemented by sensing the output current and using that signal in a feedback network that drives the gate voltage of the current source. In this way, reduction in output current when the drain voltage of the current source is reduced such that the MOS device enters the triode region can be compensated by an increased gate voltage, yielding a fairly constant output current after error correction.

The Gulati/Lee paper's implementation of this current sensing feedback concept is shown in the lower portion of figure 6-1. The feedback circuit consists of a scaled down replica of the input stage consisting of **M1R**, **M2R**, and **M9R**. The amplifier **A0** acts to keep the drain voltage on the replica and main input pair equal, therefore enforcing the bias state of the replica to be identical to that of the main input pair.

The key to maintaining a constant current output from **M9** in this circuit is the constant bias current **Ic** into the replica input stage. Since the feedback network enforces the bias state of the main input stage to be equal to that of the replica, the output current of the main input stage must also be a scaled up **Ic**, and the gate voltage of M9 and M9R is modulated inversely with the drain voltage to maintain

this constant output current.

Initial attempts at implementing a low overhead current source started with this replica input stage concept, and are described in the following section. Although, there are many issues with this circuit when implemented with a very large input pair that has substantial capacitance, and a very low power circuit that has very high output impedance at the drain of most MOS devices, yielding many low frequency poles and zeros in the open loop frequency response of this feedback network.

6.2 Design Exploration

The work derived from the circuit in figure 6-1 is almost identically implemented in the simplified schematic shown in figure 6-2. **M_rep1** and **M_rep2** are scaled down replicas of the native NMOS input pair. The common mode drain voltage of the main input pair is compared to that of the replica devices with the desired current forced through them by **I_ref**.

The frequency response of this feedback circuit near and at DC is actually very good, and it is capable of providing a constant DC output current with sufficiently low drain voltage on the current source. The issue with this implementation comes from the fact that the **POS** node at the drain of the replica input pairs has very high output resistance and reasonably high capacitance due to the substantial size of the replica input pairs and the very low current **I_ref**. The **POS** node in this circuit is a critical portion of the feedback network controlling the output current, and the very high output resistance and reasonably high capacitance yield very difficult to control dynamics in the open loop frequency response of the feedback network.

The very slow response of the **POS** node results in unacceptably distorted step response and frequency response of this low overhead current source. Many variations on this design were implemented and tested, but the low current and large capacitance nature of a native NMOS input pair replica proved unmanageable for this low overhead current source.

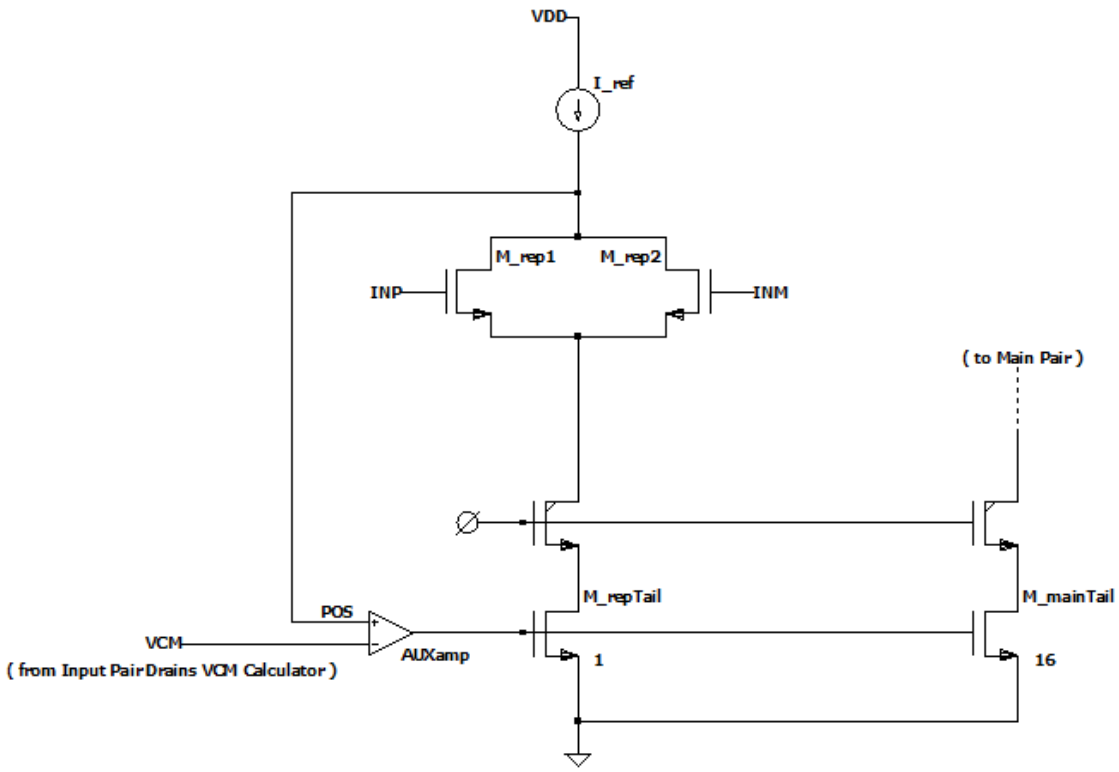

Figure 6-2: Low Overhead Current Source Design Consideration

6.3 Final Design

Avoiding the slow dynamics of the previous iterations of the low overhead current source that employed a replica native NMOS differential pair required re-imagination of how the current source should sense the output current and create an error signal that when amplified drives the gate of the main current source. Rather than sensing the output current indirectly at the drain of the replica input devices, the common source voltage of the main input pair is sensed and forced upon the drain voltage of a replica current source **M_tailReplica** as shown in figure 6-3. The replica current source device therefore creates an output current that is an exact scaled down replica of the main current mirror device **M_tail** since the bias voltages are all identical. This scaled down replica current is compared with a desired output current after both currents are converted to voltages by resistors **R**. The error signal is a voltage applied to the gate of both the main and replica current sources.

This feedback accomplishes the same goal as previous iterations without the need

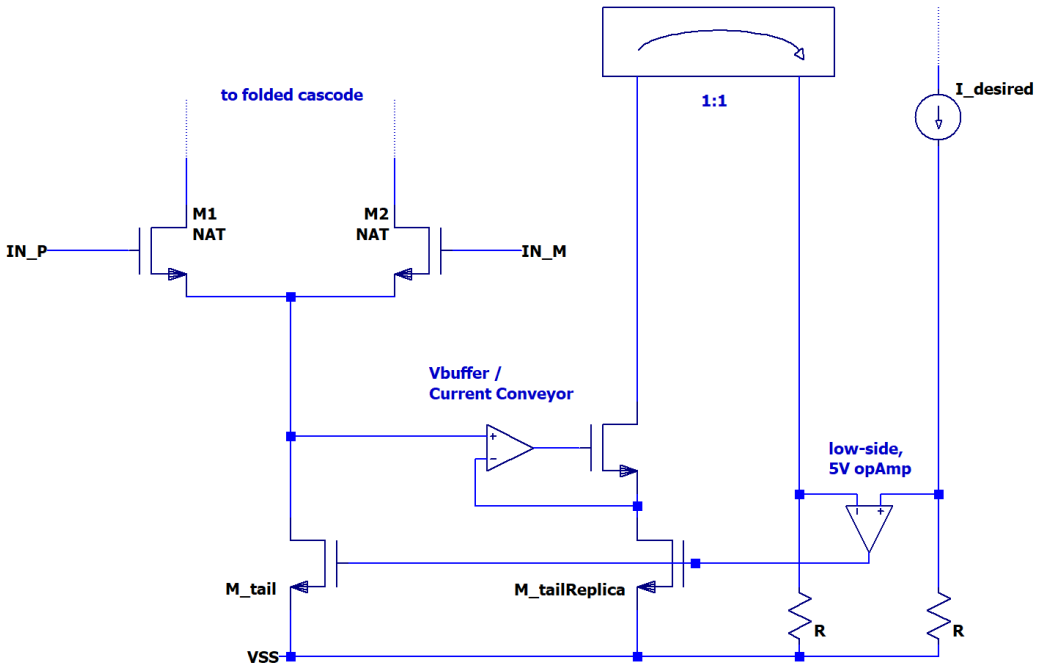

Figure 6-3: Final Low Overhead Current Source Design

for a very slow node accompanying a replica of the main input differential pair. The slowest portion of this system is actually the nodes associated with the main native NMOS differential pair, but these nodes are out the feedback loop that is forcing output current and drain voltages of the current sources to be equal.

6.3.1 Voltage Buffer

The **Vbuffer/Current Conveyer** circuit is a critical portion of this system, forcing the bias states of **M_tail** and **M_tailReplica** to be exactly equal. This mechanism is shown in figure 6-4. The current going through **U1** and **U3** is set by the ideally equal current mirrors, and is scaled to match **Iout_Replica**. The voltage at the source of **U1** and therefore the source of **U2** is equal to the voltage at the common source node of the main native NMOS input devices. The current through **U2** is equal to the current through **U1**, so this system yields a fairly accurate voltage buffer at the cost of very little current and only four extra devices. The N-type DMOS devices

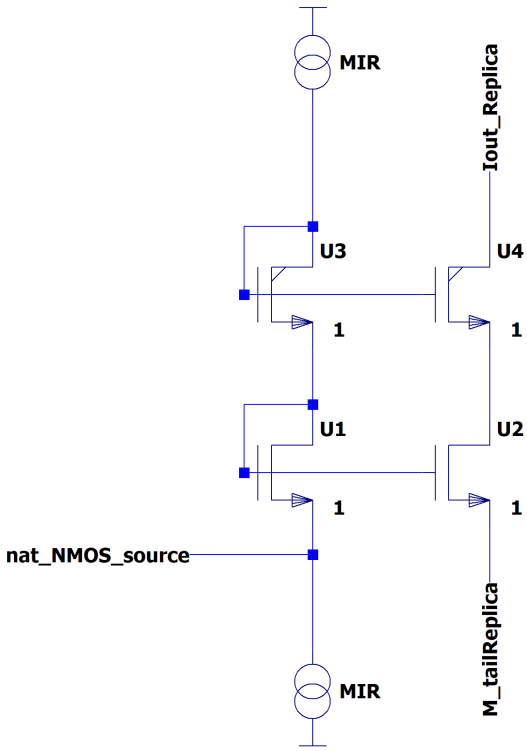

Figure 6-4: Low Overhead Current Source Voltage Buffer

U3 and **U4** have the dual functionality of protecting the gate to drain terminals of **U1** and **U2** from breakdown, and also maintaining nominally the same voltage at the drain of **U1** and **U2**, yielding more accurate voltage replication.

6.3.2 Mini Operational Amplifier

The **low-side 5V opAmp** shown in figure 6-3 is critical to the performance of the low overhead current source. The comparison of the output current to a reference output current **I_desired** is done here. There are a few key design decisions for this voltage amplification mentioned here.

The output voltage of this amplifier must be capable of driving the gates of **M_tail** and **M_tailReplica** across the full required range; normally near V_{SS} up to approximately V_{SS}+5V. This consideration requires that the device be biased near V_{SS} and have a common source output stage.

The **low-side 5V opAmp** can also be made entirely with 5V MOSFETs since

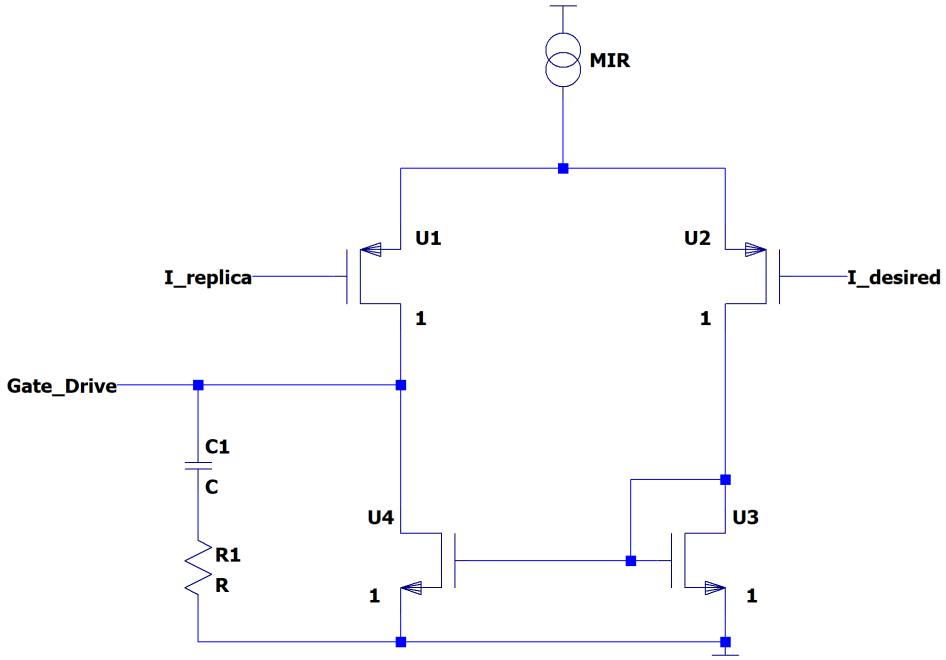

Figure 6-5: Low Overhead Current Source 5V Op-Amp

the input and output of this amplifier will always be within 5V of V_{SS}. Finally, the device must have sufficient gain and bandwidth to drive the error suitably near zero across all necessary frequencies; approximately 1 Mhz.

These design considerations result in the single stage operational amplifier shown in figure 6-5.

6.3.3 Compensation & Stability

The feedback network comprising the low overhead current source is actually a two stage amplifier in feedback. As such, this network has the potential to be unstable without proper compensation, and in fact is. The issue of closed loop instability was potentially resolved with either Miller compensation or dominant pole compensation, both with modified zero placement. The details of Miller compensation are described in Chapter 8.

Miller compensation was found to require substantially larger resistance to move the associated zero out of the right half plane, and therefore dominant pole com-

pensation was chosen. The dominant pole compensation was achieved by adding a relatively large capacitor in parallel with the shared gate-source connection of the main and replica current source devices; simply lowering the frequency of the associated pole at that node. The reduction of the pole frequency results in the reduction of the open loop crossover frequency to a sufficiently low value such that at least 60 degrees of phase margin is achieved. The addition of **R1** corresponds to the addition of a left half plane zero to the open loop frequency response, which can be strategically placed to improve the stability of the network.

6.4 Results

The key results of the low overhead current source design are summarized in this section. Notably, as shown in figure 6-6, the DC output current is constant for an input common mode voltage of -200mV, well beyond the desired 0V specification.

Also, the step response shown in figure 6-7 shows an acceptably small amount of distortion. The plot shows the output current of the low overhead current source while the common mode input voltage steps down 1V to V_{SS} at a rate of 1V/1us. It is clear that about 1.6% variation in output current results from such a step in common mode input voltage during the slew period and recovers quickly.

The novel design of this low overhead current source allows for this operational amplifier to operate effectively at a common mode input voltage at and even beneath V_{SS}. This design proves effective and has the potential to be used in other circuits requiring low overhead current sources.

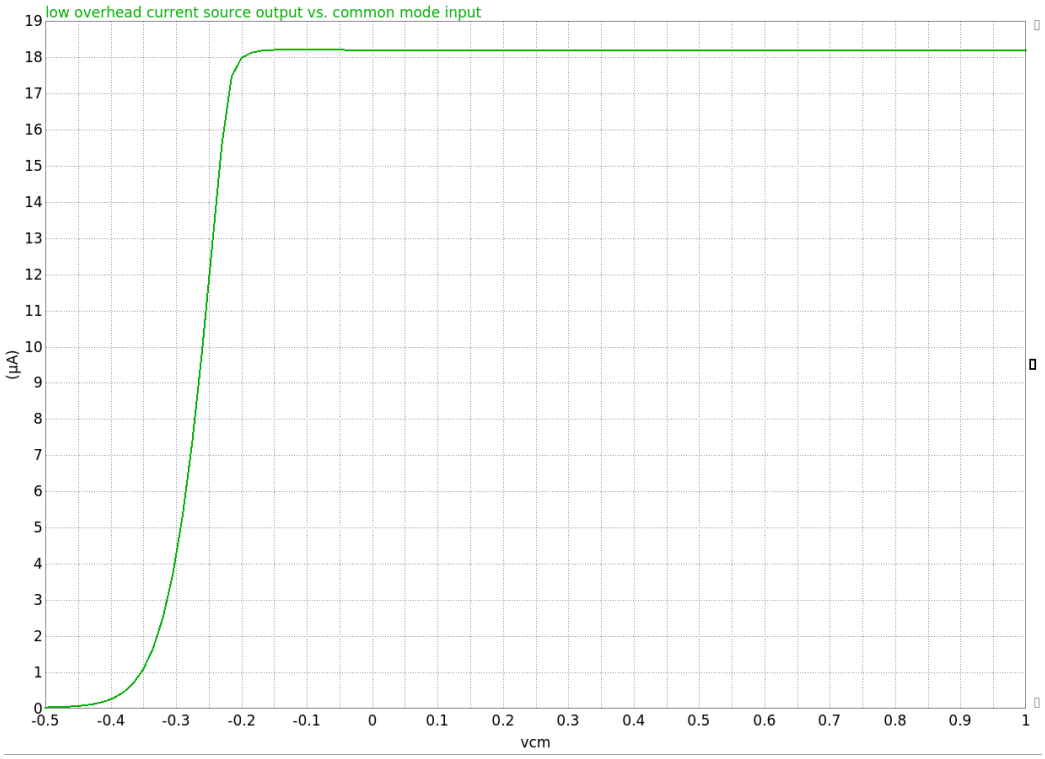

Figure 6-6: Low Overhead Current Source Output Current vs. V_{incm}

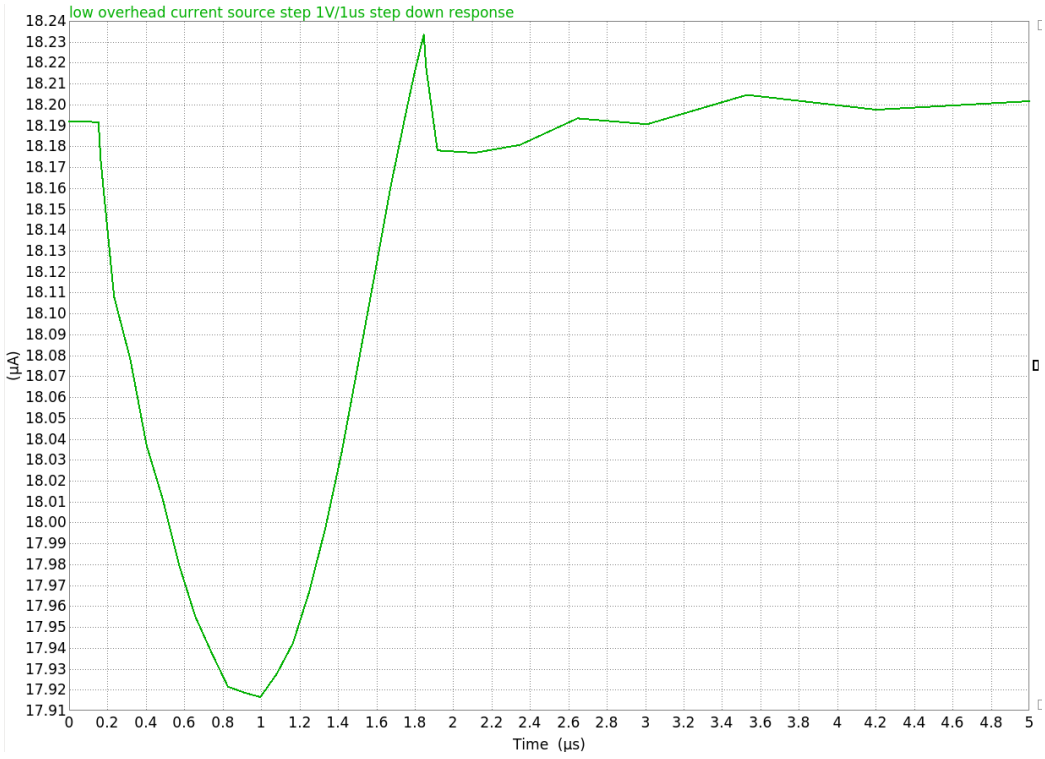

Figure 6-7: Low Overhead Current Source Step Down Response

Chapter 7

Folded Cascode & Monticelli Output Stage

7.1 Design Motivation

A folded cascode is an input stage topology that allows for greater output impedance, and ease of use with a Monticelli output stage. The advantages of the folded cascode come at the cost of increased power and complexity.

The Monticelli output stage [8] allows for rail to rail output swing by driving the output node with NMOS and PMOS common source devices simultaneously, and also provides second stage amplification with high impedance output and high g_m.

The basic operational theory of each of these architectures is detailed in this chapter, along with the connection to each other and the input stage.

7.2 Schematic & Operational Basics

7.2.1 Folded Cascode

A simplified schematic of the folded cascode is shown in figure 7-1. Devices **U6** and **U5** act as constant bias current sources that feed into the input differential pair comprised of **U1** and **U2**, the low-side mirror comprised of **Q1**, **Q2** and **U11**, and the

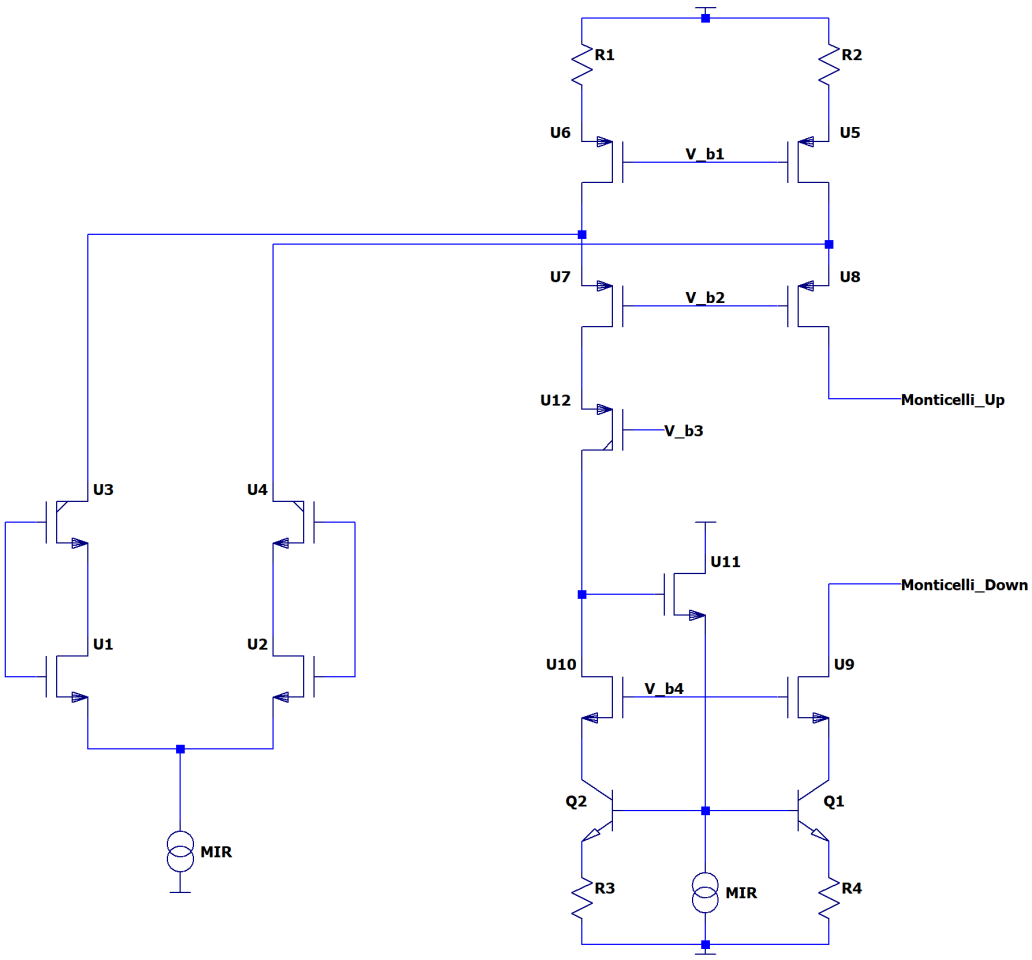

Figure 7-1: Simplified Folded Cascode Schematic

Monticelli biasing network (not shown). The bias generation for the key devices is not shown, but is designated by voltages **V_b1**, **V_b2**, **V_b3** and **V_b4**. It is clear that in order to maintain an equal amount of current through **Q1** and **Q2**, **U11** is used to provide the base bias current to both **Q1** and **Q2**. This also holds the voltage at the drain of **U10** at **U11**'s V_{gs}, plus a base-emitter voltage, plus a resistive offset above V_{SS}, necessitating only a high voltage P-type DMOS device **U12** to protect the drain of **U7**.

7.2.2 Monticelli Output Stage

A simplified schematic of the Monticelli output stage is shown in figure 7-2. This circuit allows for a common source output stage to be driven by a differential input current from the folded cascode. The common source configuration of the output transistors is necessary to achieve rail to rail output voltage, since a source follower output stage would be limited by the output transistor's V_{gs}. The topology also allows for ease of use with a variable up to 30V power supply voltage, since the biasing is all relative to V_{DD} and V_{SS}.

Differential input current is provided by the folded cascode into nodes **Folded_Cascode_Up** and **Folded_Cascode_Down**. When **Folded_Cascode_Up** provides more current than **Folded_Cascode_Down**, the increased voltage at the aforementioned nodes is cascaded down to the gates of devices **U5** and **U1**, resulting in increased output sinking current. The opposite effect, increased output sourcing current, takes place when **Folded_Cascode_Down** provides more current than **Folded_Cascode_Up**.

The quiescent current through all nodes is based on the quadratic translinear principle [3]: resulting current through all common source devices is proportional to the diode ladder bias current as a function of the relative device geometries.

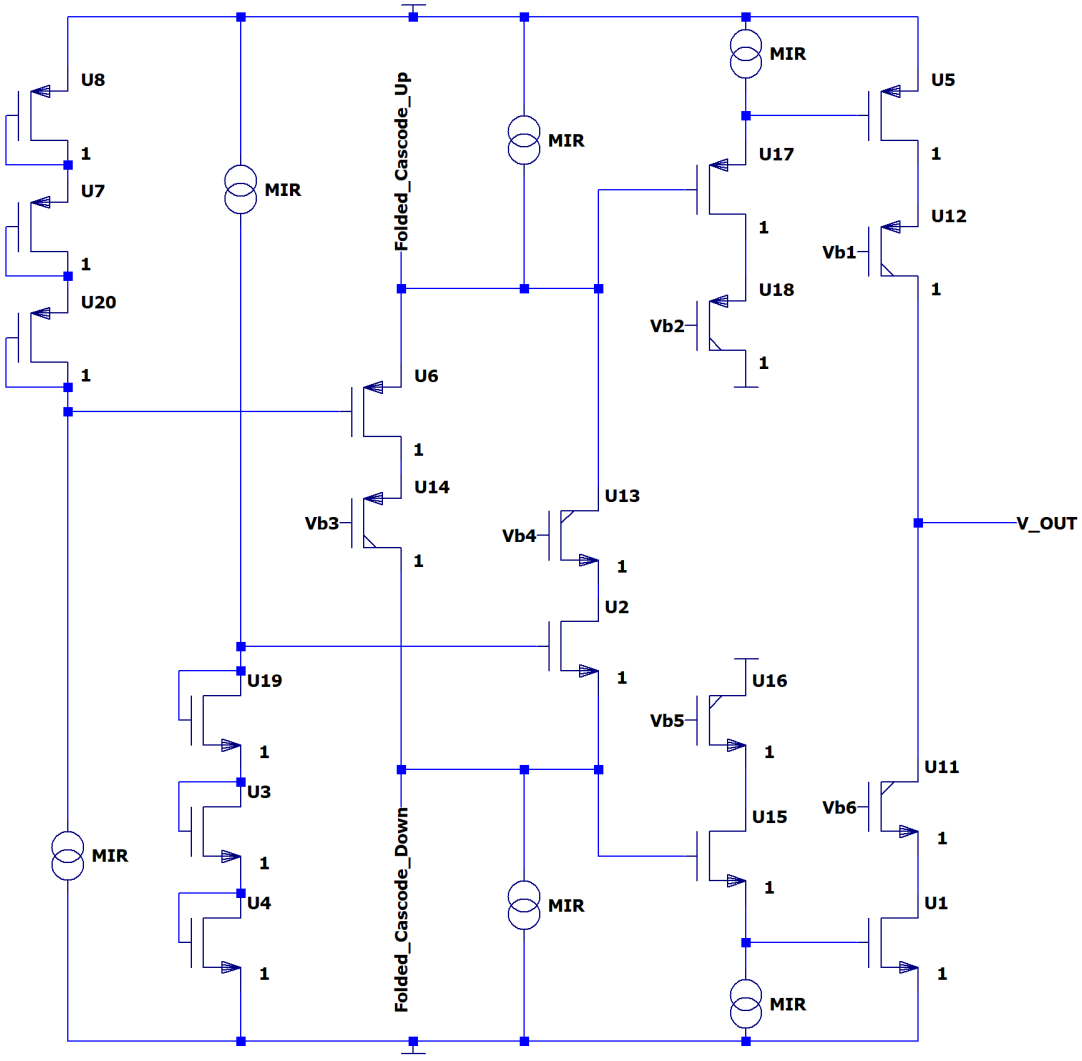

Figure 7-2: Simplified Monticelli Output Stage Schematic

7.3 Noise Considerations

Noise is of critical importance in the folded cascode due to its proximity in the signal chain to the main differential input pair, resulting in key devices having a large impact on total input referred flicker noise.

7.3.1 NPN Mirror

Devices **U5**, **U6**, **Q1**, and **Q2** of figure 7-1 all have a substantial contribution to the total input referred flicker noise of the operational amplifier. Therefore, any means of reducing the flicker noise in these devices results in substantially less total flicker noise.

It is clear that devices **Q1** and **Q2** are NPN BJTs, rather than NMOS. The decision to use NPN transistors here is directly a consequence of the substantially reduced flicker noise in BJTs relative to MOS devices. The only reason why devices **U5** and **U6** are not PNP BJTs is because these devices were not available in the TSMC process used by this thesis.

The base bias current of **Q1** and **Q2** is provided by the common source NMOS **U11**. Also, additional current through **U11** that is not provided to the bases **Q1** and **Q2** was found to avoid an alternative operating point where the folded cascode is not operational.

Q1 needs to behave as a current mirror of **Q2**, and since the gate of **U11** does not require current to operate but still drives the bases of **Q2** and **Q1**, current mirroring still takes place without the left leg of the folded cascode providing the base current to each BJT, which would unbalance the current mirror by a factor of $1 - 2/\beta$.

7.3.2 Resistive Degeneration

In figure 7-1 it is clear that devices **Q1**, **Q2**, **U5**, and **U6** are resistively degenerated. The resistive degeneration has the effect of reducing the drain-source and collector-emitter current white and flicker noise by negative feedback. The total noise current out of the drains/collectors is reduced as the resistance increases, and the upper limit

of the resistance is set by the available voltage headroom. Also, the resistors used do not contribute substantial noise because they are made from very low noise material.

7.3.3 Key Device Sizing

For the MOS devices which contribute a substantial amount to the total input referred flicker noise of the operational amplifier, their individual flicker noise can be reduced by increasing their width and length as described in Chapter 3.

Chapter 8

Compensation & Stability

Operational amplifiers are typically multi-stage amplifiers with complex dynamics, especially as the frequency increases. The dynamics of the system are described using the frequency domain transfer function comprised of many poles and zeros. The stability of the system is governed by the location of the poles in the complex plane.

The stability of operational amplifiers must be analyzed in the context of a closed loop feedback system, since the typical use case, including external feedback, changes the overall transfer function based on Black's formula [7]. A block diagram useful for describing the dynamics of feedback systems is shown in figure 8-1.

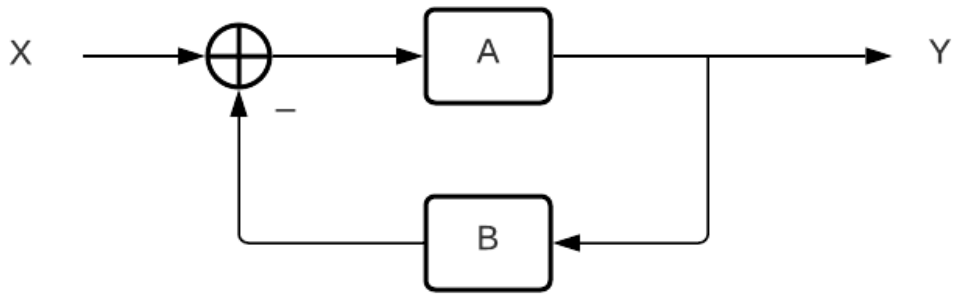

Figure 8-1: Feedback Block Diagram

The overall closed loop transfer function of this feedback system is given by:

$$\frac{Y}{X} = \frac{A}{1 + AB} \tag{8.1}$$

It is clear that this closed loop transfer function has an asymptote when **AB** is equal to -1, yielding an infinite value for the output of this system. In fact, the stability of the closed loop system can be analysed by only looking at the term **AB** in the denominator of the closed loop transfer function, denoted the *loop gain*.

It can be shown that the system is stable, for systems where the gain crosses 0dB once, when the loop gain magnitude reaches unity before the phase reaches negative 180°, a condition also referred to as having a *phase margin* greater than 0. Ideally, the phase margin should be at least 60°to ensure transient response with very little ringing.

8.1 Miller Compensation Basics

Miller compensation is a widely used means of stabilizing unstable multiple stage high gain systems. The main idea is to add a capacitor in parallel with the inverting second gain stage which has the effect of splitting the two dominant poles in the frequency domain; making one much lower frequency while making the other higher frequency. This pole splitting action allows for improved phase margin by making the system look more similar to a single-pole system at the unity gain crossover frequency. A block diagram showing the miller capacitor $\mathbf{C_m}$ in parallel with the second gain stage of a two stage amplifier is shown in figure 8-2.

The inclusion of a resistor $\mathbf{R_m}$ in series with $\mathbf{C_m}$ is due to the creation of a right half plane zero that accompanies miller compensation [10]. The angular frequency of the zero is approximately given by the following equation.

$$z \approx \frac{1}{(1/g_{m2} - R_m)C_m} \tag{8.2}$$

It is clear that careful selection of the value of $\mathbf{R_m}$ can force the frequency of

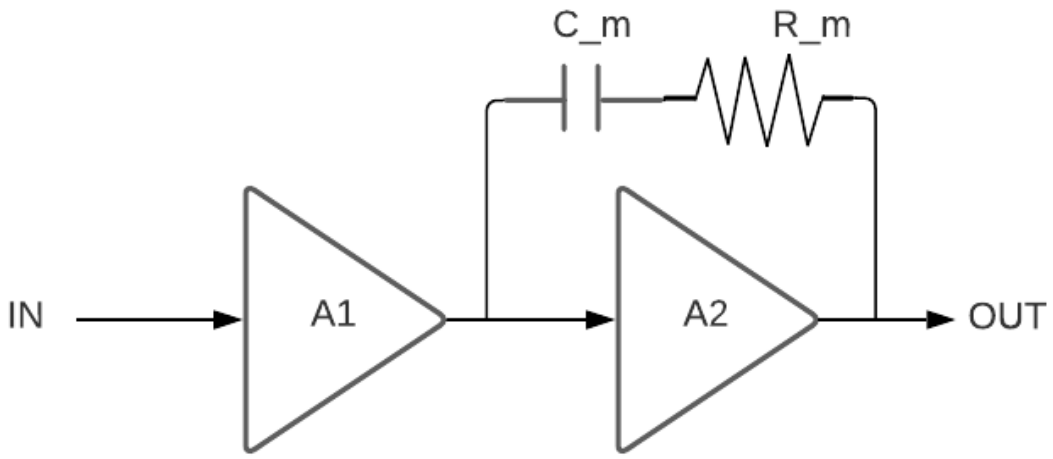

Figure 8-2: Miller Compensation Block Diagram

this zero to infinity, or at least to the left half plane so that it is not particularly detrimental to closed loop amplifier stability.

8.2 Application & Stability Results

It is clear that the second high gain stage in this amplifier design is the Monticelli output stage, and that the miller capacitor $\mathbf{C_m}$ and resistor $\mathbf{R_m}$ should be tied from the output to the input of this gain stage. These positions are clear from the preceding discussion in chapter 7.

Careful tuning of the values of these components, and simultaneously monitoring of loop gain as a function of frequency yielded the satisfactory gain and phase margins shown in figure 8-3 and therefore closed loop amplifier stability.

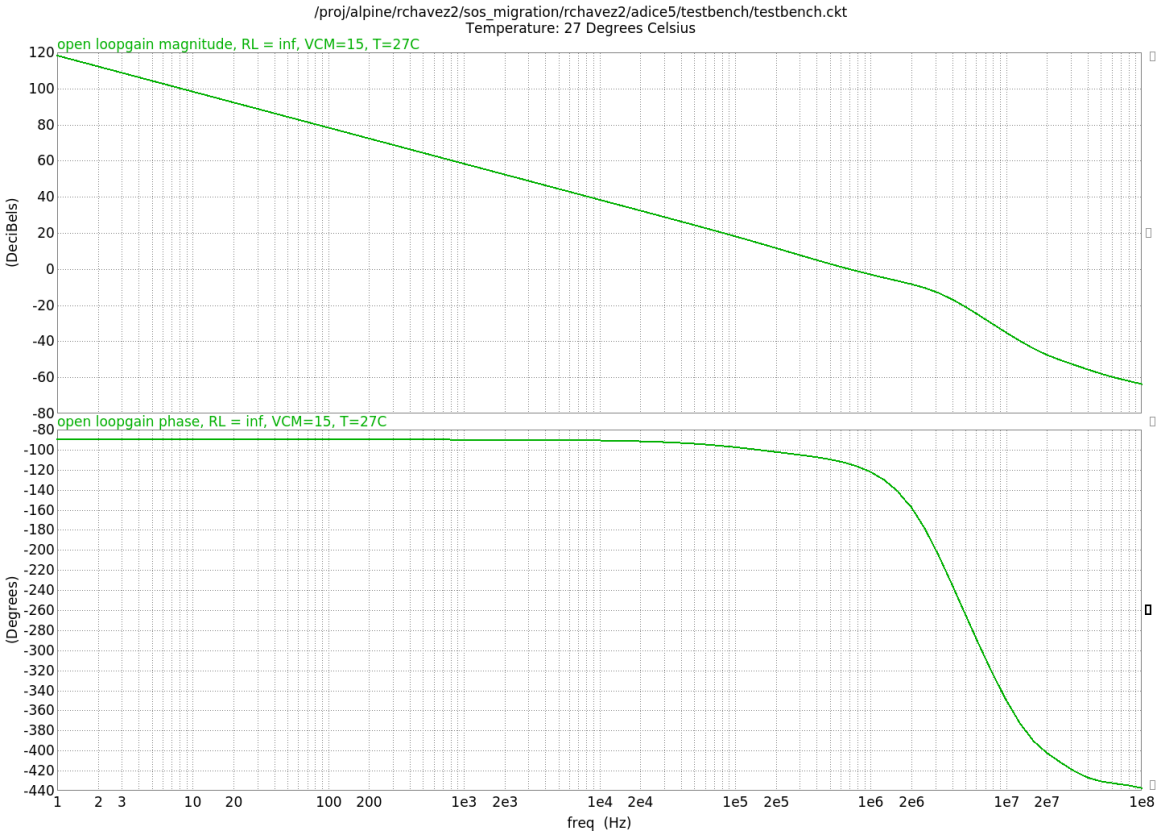

Figure 8-3: Final Loop Gain/Phase

Chapter 9

Results

9.1 Final Specifications

Specification	Value	Unit
Supply Voltage	30	V
Supply Current	110	μA
Technology	BiCMOS	
$1/f$ Noise 0-10 Hz	564	nV_{PP}
GBW	1	MHz
C_{in}	20	pF
Input Bias Current	0	nA
Rail-Rail Input	Low-Side	
Rail-Rail Output	Yes	
5V Package	SOT23	
Temperature Range	[-40,125]	°C

Table 9.1: Final Amplifier Specifications

The key results of this thesis project that pertain to the entire operational amplifier are presented in this chapter. Many auxiliary circuits, such as the slew boost, band-

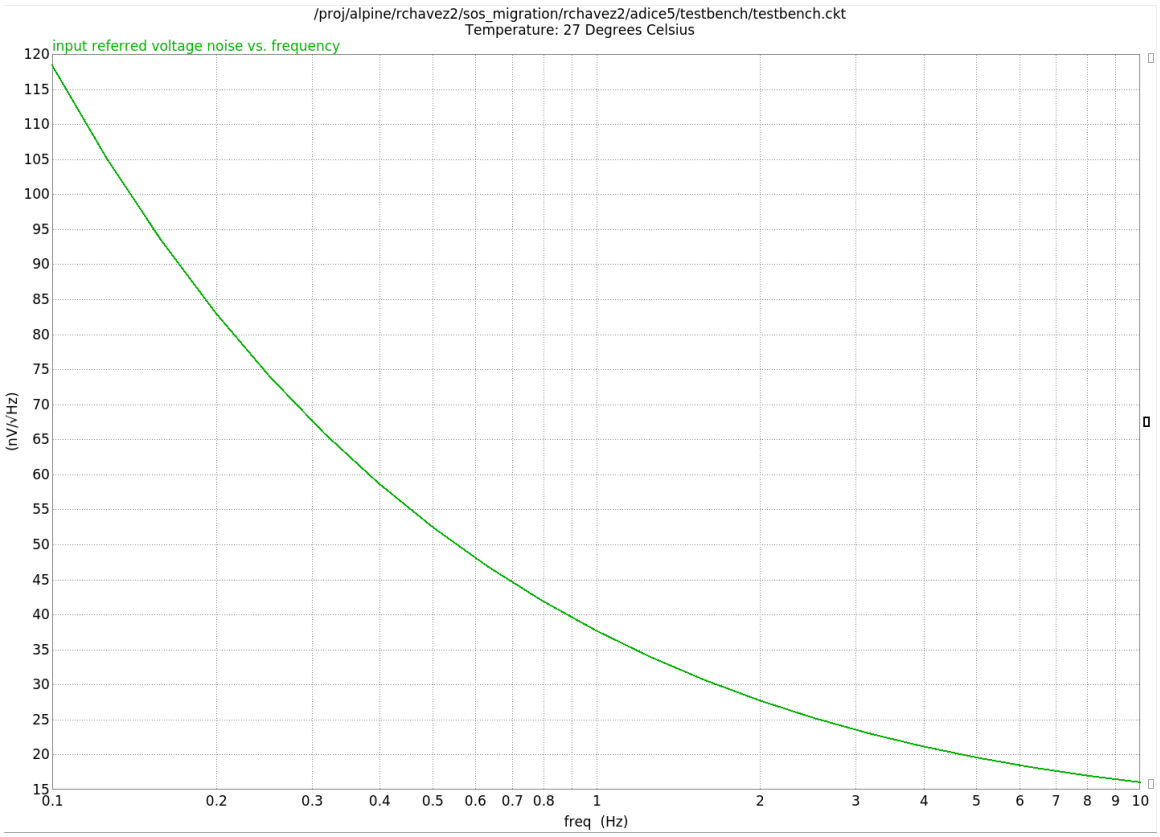

Figure 9-1: Final Input Referred Flicker Noise Voltage

gap references, and over-voltage protection mechanisms are not detailed in this thesis.

Variation of amplifier performance across temperature and process variations was analyzed to ensure stability and sufficient behavior, although these conclusions were used to verify behavior of key sub-circuits, this verification is not presented in this thesis.

9.2 Flicker Noise

The key result of this thesis project is the very low input referred flicker noise voltage using native NMOS input devices. The plot shown in figure 9-1 shows the power spectral density of the input referred voltage noise as a function of frequency. The spot noise at 1 Hz is approximately 37.6 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, and the integrated flicker noise from 0.1 to 10 Hz is approximately 564 $\mathrm{nV_{PP}}$ [1].

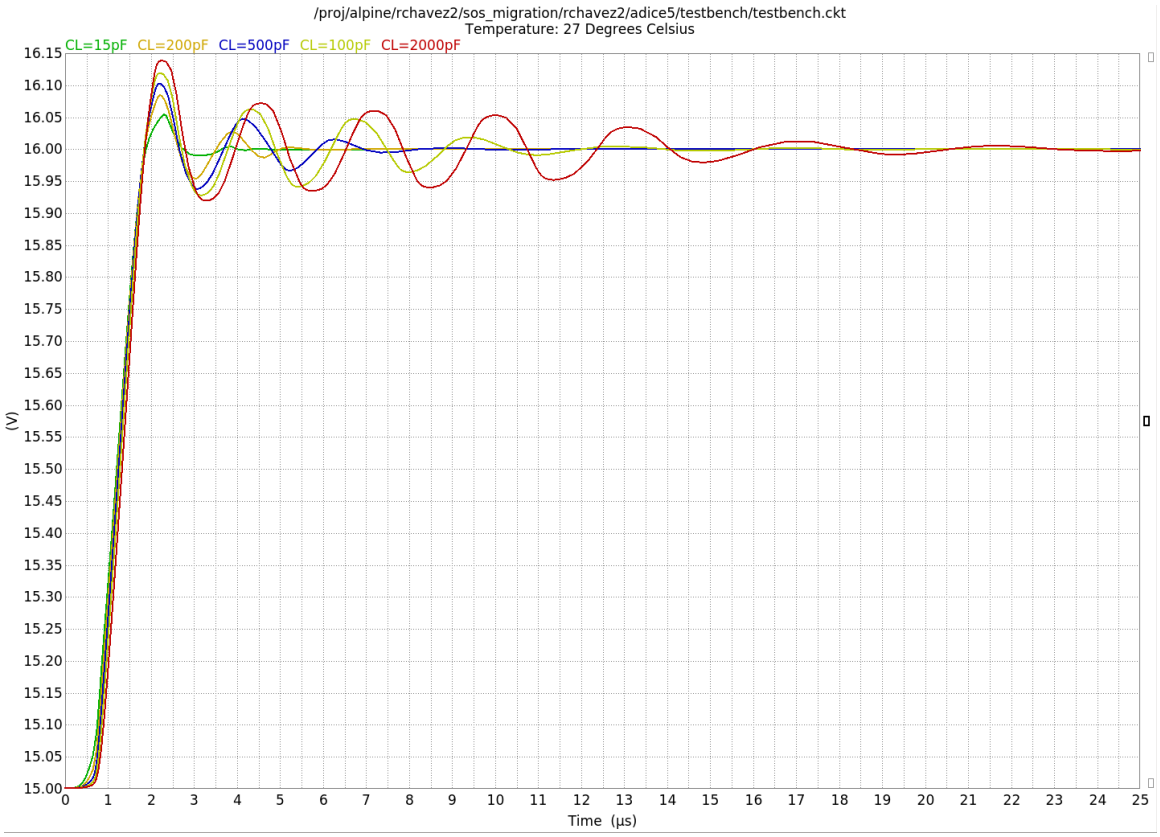

Figure 9-2: Final Step Response Vs. Load Capacitance

9.3 Dynamics

The closed loop amplifier performance is characterized by the unity gain closed loop step response. The output is loaded with a 150kΩ resistor and various capacitor sizes listed within figure 9-2. The large resistance is necessary so that the limited output current capability of the low power Monticelli output stage is not saturated. The amplifier is clearly stable, although more attention could be given to the ringing at large load capacitance, and modifications to the compensation network would likely improve performance. The applied step is a 1V/1us step in voltage on the non-inverting input of the amplifier while in unity gain feedback configuration.

Chapter 10

Conclusion & Further Work

The many aspects of the design of this operational amplifier were explored in detail. Such a low noise, low power operational amplifier is shown to be useful in various precision applications such as sensors and various low frequency electronic systems.

Given the complexity of the entire amplifier, only the key design challenges and solutions are examined in this thesis. In particular, the low-overhead current source and native NMOS input devices.

Throughout work on this thesis, the author gained crucial experience and knowledge about industry standard analog integrated circuit design. Particularly how to design with noise in mind, and creatively iterate on novel circuit architectures to solve unusual problems.

With more time to work on this design, the layout of the circuit could be completed, and eventual tape-out and post tape-out verification. More time can and should be given to the high-side input failure of the low-overhead current source, as a simple switching mechanism as detailed in chapter 5 should suffice to solve the problem.

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