High Angular Resolution Beam Steering Terahertz Antenna Arrays for Imaging Applications

by

Nathan M. Monroe

S.B., Massachusetts Institute of Technology (2013)

M. Eng., Massachusetts Institute of Technology (2017)

Submitted to the Department of Electrical Engineering and Computer Science

in partial fulfillment of the requirements for the degree of

Doctor of Philosophy in Electrical Engineering and Computer Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

February 2022

Author...

Department of Electrical Engineering and Computer Science

January 26, 2022

Certified by..

Ruonan Han

Associate Professor of Electrical Engineering and Computer Science

Thesis Supervisor

Accepted By...

Leslie A. Kolodziejski

Professor of Electrical Engineering and Computer Science

Chair, Department Committee on Graduate Students

High Angular Resolution Beam Steering Terahertz Antenna Arrays for Imaging Applications

by

Nathan M. Monroe

Submitted to the Department of Electrical Engineering and Computer Science on February 1, 2022, in partial fulfillment of the requirements for the degree of

Doctor of Philosophy in Electrical Engineering and Computer Science

Abstract

Terahertz antenna arrays can produce Terahertz electromagnetic waves that can be steered by electronic control. They are a promising technology for many applications, including imaging, radar, communications and other sensing applications due to bandwidth availability, penetration of dielectric materials, and short wavelength, enabling smaller structures. There is particular application in automotive radar imaging, where a narrow FMCW radar beam is swept across a scene to produce a depth image which, unlike LIDAR, is tolerant to environmental conditions such as rain and snow. However, challenges exist in the design of large dense THz arrays, limiting demonstrations to hundreds of antennas, a fraction of the size required for high-resolution imaging. This is explained by challenges including THz phase shifters which are high-loss and too large for dense integration, consume large DC power, and introduce amplitude and phase errors. In addition, challenges exist with high-loss on-chip RF power distribution, array scalability and phase control.

The approaches taken in this work address these issues, enabling a 98x98 antenna array at 265GHz which employs passive one bit phase shifters based on two MOSFET switches. These phase shifters are low-loss, low-area and consume no DC power. A reflector array (reflectarray) architecture and in-unit memory address RF distribution and digital control challenges, and a scalable design allows for arbitrary array sizes. In-unit memory additionally enables performance-enhancing algorithms to mitigate beam squint and radiation sidelobes which improve effective resolution of a wideband FMCW radar image and enable radiation performance approaching that of ideal phase shifters. The concepts are demonstrated on-chip in a 22nm FinFET CMOS process, with a 4x4mm^2 chip containing a dense 7x7 antenna array.

An on-PCB tiling of 14x14 chips produces a 98x98 antenna array, which demonstrates electronic steering over a 120 degree window of a 1x1 degree THz beam with 42dBi of directivity, and is further enhanced by algorithmic approaches. The antenna array is employed in a radar imaging application where the high-directivity beam is used to produce 90x90 pixel radar images. This represents the largest beam-steering THz antenna array demonstrated to date, and a step towards practical solid-state THz imaging.

Thesis Supervisor: Ruonan Han

Title: Associate Professor of Electrical Engineering and Computer Science

Acknowledgements

I would like to thank my family for their perpetual support in every sense of the word. My parents Mark Monroe and Julie McKay as my cheerleaders and mentors, with the constant encouragement and advice and providing the solid foundation for me as a researcher and person. My brother and sister Ryan and Morgan Monroe for the comedic relief and helpful insights. My partner Muching Zhang for helping me stay focused on what's important, being there through difficult and stressful deadlines and always having my back. Words can't express the gratitude for all of you. This thesis is dedicated to you.

Thanks to Professor Ruonan Han, my Ph.D. advisor who welcomed me in as a floundering and uncertain student, and through patient mentorship and bold perspective helped guide me through my Ph.D. studies. Professor Han's methodical approach to creative problem-solving and ability to bridge concepts between disparate fields should be an inspiration to all. Thanks to Professor Jeffrey Lang who served as my advisor for the initial portion of my graduate studies and carefully guided and mentored me through my growth as a researcher and engineer. Thanks to professor Gregory Wornell who also served on the thesis committee and provided invaluable insights on array intuition and signal processing analogies.

Furthermore, I'd like to thank my colleagues in the Han group, including Dr. Cheng Wang, Dr. Zhi Hu, Dr. Xiang Yi, Dr. Jack Halloway, Dr. Mohamed Ibrahim, Muhammad Ibrahim Khan, Mina Kim, Jinchen Wang, Mohamed Elsheikh, Alec Yen, Xibi Chen, Eunseok Lee, Xingyu Zou, Yukimi Morimoto, and Jimmy Mawdsley for helpful technical discussions, and support (emotional and otherwise) during busy tapeout and testing sessions.

Contents

8

List of Figures

12

List of Tables

Chapter 1

Introduction

1.1 Thesis Objective and Contributions

Antenna arrays in the THz frequency range are of great research interest, primarily due to their small physical size for a large electrical size. However, large dense THz antenna arrays have been a great challenge to the research community. This Thesis aims to address many of the related challenges. The target performance of a 1x1$^{\text{o}}$ beam of radiated energy is intended for imaging radar applications, where a radiated beam is swept across a scene to generate a two dimensional image of approximately 100x100 pixels. This performance target is achieved by the implementation of a 98x98 dense antenna array operating at 265GHz, where each antenna's radiated phase is controllable electronically, allowing for rapid and precise beam steering. A number of challenges exist in the implementation of such a large array, which were identified and addressed. The losses of on-chip THz power distribution were addressed by adopting a reflectarray architecture, where THz energy is distributed spatially to each antenna element by a feed antenna. Challenges in implementing small-scale, low power and low loss switches were addressed by the development of a one-bit passive phase shifter approach, based on two MOSFET switches and symmetrical antenna feed. Scalability issues in the fabrication and assembly of such a large array were addressed on the chip design level, with a chip architecture that allows for tiling copies of a chip to create a large array, and an architecture that is robust to defects in array fabrication and assembly. Challenges in digital control and bandwidth limitations were addressed by incorporating local memory within each antenna, allowing a library of pre-computed phase states to be loaded onto the array

at system startup. The incorporation of on-chip memory allows for demonstration of performance-enhancing algorithms, including those for mitigating sidelobes and beam squint. The approaches introduced here were also demonstrated in an imaging radar application with resulting 90x90 pixel 3D radar images. This is the first solid state THz radar imager demonstrated to date having significant angular resolution in both dimensions.

The publications related to these works are:

1. Nathan M Monroe, Georgios C Dogiamis, Robert Stingel, Preston Myers, Xibi Chen, Ruonan Han, "Electronic THz Pencil Beam Forming and 2D Steering for High Angular-Resolution Operation: A 98×98 Unit, 265GHz CMOS Reflectarray with In-Unit Digital Beam Shaping and Squint Correction" *2022 IEEE International Solid- State Circuits Conference (ISSCC)*, 2022 (accepted)

2. Qiang Yu, Said Rami, James Waldemer, Yunzhe Ma, Vijaya Neeli, Jeffrey Garrett, Guannan Liu, Jabeom Koo, Mauricio Marulanda, Saurabh Morarka, Surej Ravikumar, Yi-Shin Yeh, Jessica Chou, Thomas Brown, Triveni Rane, Carlos Nieva, Dyan Ali, Sameer Joglekar, Mark Armstrong, Jeremy Wahl, Leif Paulson, Georgios Dogiamis, Nathan Monroe, Ruonan Han, Hyung-Jin Lee, Hui Fu, Bernhard Sell, Eric Karl, Ying Zhang, "mmWave and sub-THz Technology Development in Intel 22nm FinFET (22FFL) Process," *2020 IEEE International Electron Devices Meeting (IEDM)*, 2020, pp. 17.4.1-17.4.4, doi: 10.1109/IEDM13553.2020.9372105.

1.2 Thesis Organization

This chapter provides a context for the research, a motivation, and the research contributions made by this work. Chapter 2 describes in broader detail prerequisite background knowledge, including Terahertz (THz) electromagnetic waves, the THz gap, antenna arrays and their considerations, and imaging applications. Chapter 3 describes the design of the THz antenna array from bottom-up, with design of the

antenna element, chip-level digital architecture and I/O architecture, and system-level architecture including assembly and feed design. It also describes the testbench used for array characterization, calibration methods, plus the measurement results themselves. Chapter 4 details the design of the THz one-bit phased array, incorporating many of the principles described in Chapter 3. It includes design of the antenna element, THz mixer, baseband receiver path, THz source design, chip-level array architecture and system-level array architecture. Chapter 5 contains a description of the algorithms used for performance enhancement, building on the reflectarray architecture described in Chapter 3. This includes algorithms for the reduction of sidelobes and mitigation of beam squint in wideband FMCW radar applications and includes measurement results. In Chapter 6, the previously described THz reflectarray is demonstrated in an imaging radar application, with a description of associated hardware and software and imaging results. Chapter 7 provides a summary of results, lessons learned, concluding remarks and suggestions for future work.

Chapter 2

Background and Motivation

Terahertz radar imaging is a long sought after technology with broad application across automotive, aerospace, robotics and other applications [1][2]. This dissertation's goals of high resolution THz radar imaging are met through a variety of approaches across circuit and electronics design, electromagnetics, signal processing, statistical modeling, manufacturing, mechanical design and others. This chapter opens with an overview of prerequisite background information and motivation for the work. Section 2.1 introduces Terahertz electromagnetic waves and their broad applications, including imaging radar. Section 2.2 reviews Terahertz antenna arrays and phased array techniques in general, including closely-related reflectarray and transmitarray techniques. It also discusses some of the challenges particular to Terahertz implementations of these arrays, namely phase shifters and quantization, power distribution, scalability, control, and beam squint considerations.

2.1. THz Electromagnetic Waves and Their Applications

The Terahertz spectrum of electromagnetic waves, ranging in frequency from approximately 0.1 THz to 10 THz, has been gaining increasing attention in the scientific and engineering research communities for a number of reasons, including bandwidth availability, relatively short wavelength, and interesting wave-matter

interaction properties, amongst others [2], [3]. The efficient generation and sensing of Terahertz waves has proven to be an elusive achievement, as explained by the "THz gap" between classical low-frequency semiconductor device-based approaches and optical techniques [4], as seen in Figure 2-1. At the same time, THz systems have the potential to enable a broad range of applications such as communications [5], [6], pathogen sanitation [7], space-based applications [8]–[11], in addition to numerous imaging applications discussed below.

Terahertz imaging is an emerging technology with expanded research interest over the past decade. Terahertz imaging systems have been demonstrated with applications in security [12], military [13], [14], spectroscopy [3], nondestructive testing [2], medical imaging [2], and others. In such systems, THz waves are directed at sample targets with received signal taken either by reflection or transmission through a target to create an array of pixels. Most common approaches create a matrix of such pixels to generate an image. These systems rely nearly exclusively on
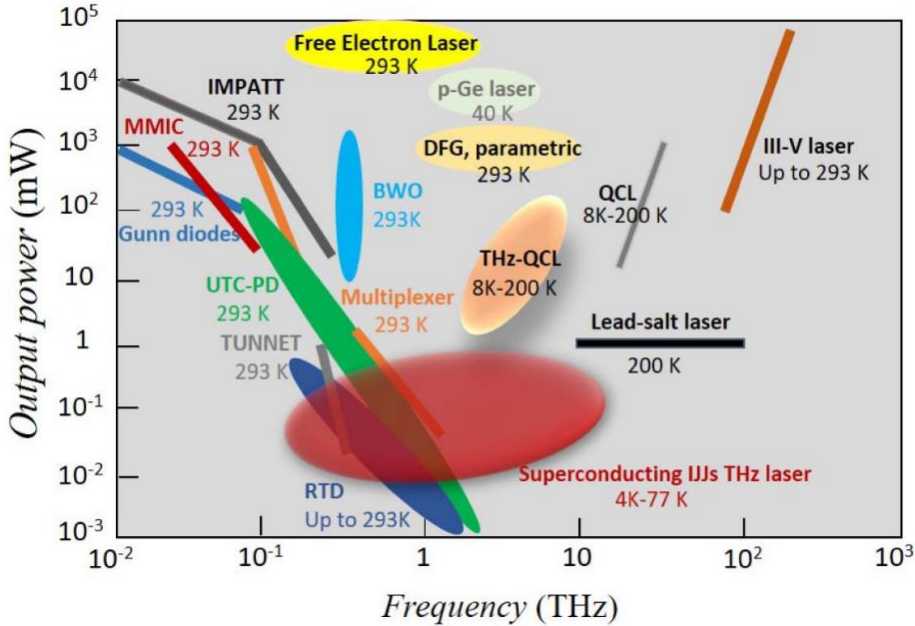
Figure 2-1. The Terahertz Gap [4], the frequency range between approximately 0.1-10THz where efficient generation, manipulation, and detection of electromagnetic waves is difficult.

motorized beam steering, with approaches such as motorized reflector mirrors [15]–[17], gimbaled sample stage [18], or actuated lenses [19] to steer a radiated beam. These approaches, while effective, are in general large, heavy and expensive, with large power consumption and slow image acquisition, and reliability issues associated with physical movement.

2.1.1. Imaging Radar

Imaging radar is a special case of imaging, where radiofrequency energy is used to create a three-dimensional radar image; each pixel contains depth information. While this approach is theoretically possible at any frequency, it is particularly attractive at THz frequencies for reasons that will be explained later but can be summarized as practicality issues related to size and weight. Terahertz imaging radar is of great interest for automotive applications [20]. In this application, THz radiation in an FMCW configuration is utilized to produce a three dimensional depth image, to be used by an autonomous vehicle for object detection and recognition. This stands as an alternative to LIDAR, the current widely-used approach, which is significantly more sensitive to environmental factors such as rain, fog and snow [21]. THz imaging radar for automotive applications is a path little explored, as the existing mechanical beam scanning systems make it impractical in these applications. At the same time, a number of other potential applications would benefit from reduced size and weight arising from a Terahertz implementation of imaging radar, including aerospace, consumer and defense applications. The ability of Terahertz waves to penetrate certain dielectric materials such as clothing, walls and packages and envelopes have the potential to enable applications that weren't previously possible [17].

An existing method for imaging radar is based on Multiple-Input-Multiple-Output (MIMO) techniques [22], [23]. In MIMO approaches, a number of independent transmit and receive antennas, each with independent RF transceivers, are combined via signal processing to produce large virtual arrays enabling enhanced imaging resolution performance exceeding what is possible with classical techniques using an

equal number of antenna elements. While promising for certain low-cost radar applications, MIMO techniques represent a number of challenges. The large number of transceivers present a complex layout and distribution problem for the RF and baseband signals as well as increased power consumption. These issues are exacerbated in the context of 2-dimensional dense antenna arrays which are required for 3-dimensional imaging. To date, no MIMO array has been demonstrated with significant imaging capabilities in two dimensions.

Regardless of the approach taken for radar imaging, typical approaches rely on the generation of a narrow beam of radiated (or received) energy. In a typical radar imaging application, a pixel is generated by steering a narrow beam in a direction and taking a sample of radar distance. By sweeping the beam around a scene in a rasterized fashion, a 3-dimensional radar image is created. The beam is swept in increments equal to the beamwidth to maximize imaging speed while mitigating redundant information in the resulting image. Therefore, the maximum achievable effective image resolution is determined by the width of the beam. In this work, a goal of a 100x100 pixel 3-dimensional radar image has been set based on autonomous vehicular vision applications. Assuming a viewing window of [-50 +50] degrees in both dimensions, this translates to a requirement for a beam width of approximately one degree in both dimensions. As in all aperture antennas, beam steering angles far away from boresight cause a widening of the mainlobe due to a decrease in effective aperture size. Therefore, in this technique there is a graceful degradation in performance at wide angles due to the wider beam.

2.2. THz Antenna Arrays

A long-time alternative to mechanical actuation in beam steered systems at any frequency is phased array beam steering techniques [24]–[26]. In this well-known approach, two or more antennas are placed in a one or higher dimensional array. The antennas are fed at the same frequency but varying amplitude and/or phase.

This configuration synthesizes a larger effective antenna aperture whose radiation characteristics are controlled electronically by selection of its constituent antennas' amplitude and/or phase. This can be used to, for example, focus the antenna's radiated energy into a narrow, collimated beam, while the electronic control often has superior performance to its mechanically-steered counterpart. Phased array antennas' ability to control their radiation pattern electronically allow for rapidly configurable beam steering in a package that is often smaller, lighter in weight, more reliable, and lower power than mechanically steered approaches while having the ability to steer radiated energy to new directions much more rapidly.

Terahertz phased arrays are an interesting application of phased array technology, with broad applications in imaging, radar, communications, or any application that benefits from a configurable radiation pattern [27]–[39]. Terahertz frequencies are particularly attractive for phased array techniques due to the reduced wavelength, and therefore reduced physical size for a given electrical size, as determined by a fundamental relationship between the two:

$$D = \frac{4\pi A f^2}{c^2} \qquad (2.1)$$
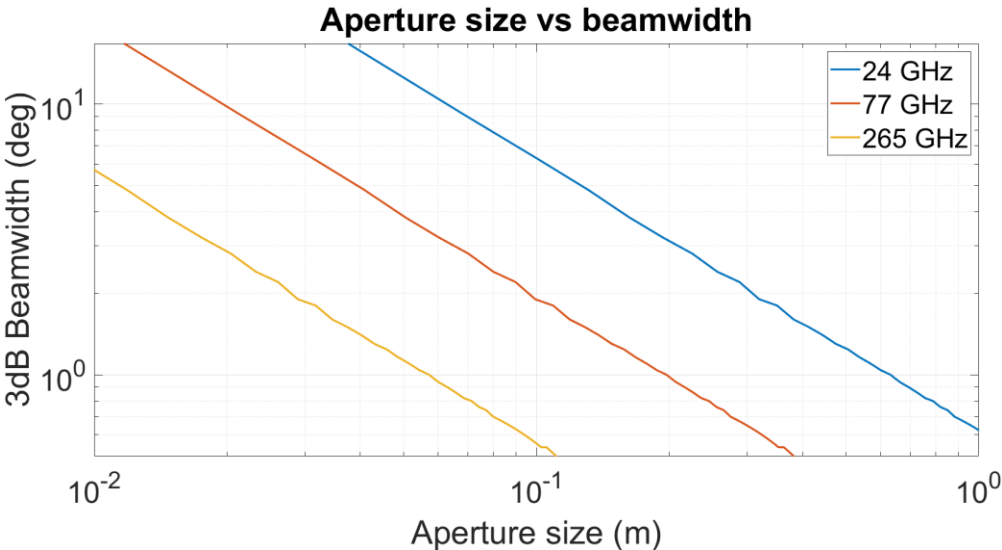
Figure 2-2. Aperture size of a radiofrequency radiator versus the 3dB width of the resulting beam.

27

where D is beam directivity, A is aperture area in square meters, f is frequency in Hertz, and c is the speed of light in meters per second. This relationship can be seen in Figure 2-2, which depicts a fundamental tradeoff in required size for a given beamwidth at a number of frequencies. As frequency increases, physical size decreases for a given beamwidth; the reduced physical size enabled by Terahertz technology opens the door for new applications that were previously limited in practicality due to their physical size.

Despite their promise, THz phased arrays have seen slow progress due to a number of challenges. The high frequency generally precludes more conventional discrete circuit board based approaches; nearly all implementations rely on semiconductor integration due to the precise manufacturing, low parasitics and modeling abilities.

While the relatively high frequency of THz waves allows for relatively smaller phased array sizes, the semiconductor die size required for high gain and narrow beam phased arrays is prohibitive in both cost and fabrication yield. In addition, the on-chip losses in RF signal distribution and radiation often outweigh the advantages of the increased frequency and proportionally smaller wavelength. The routing density
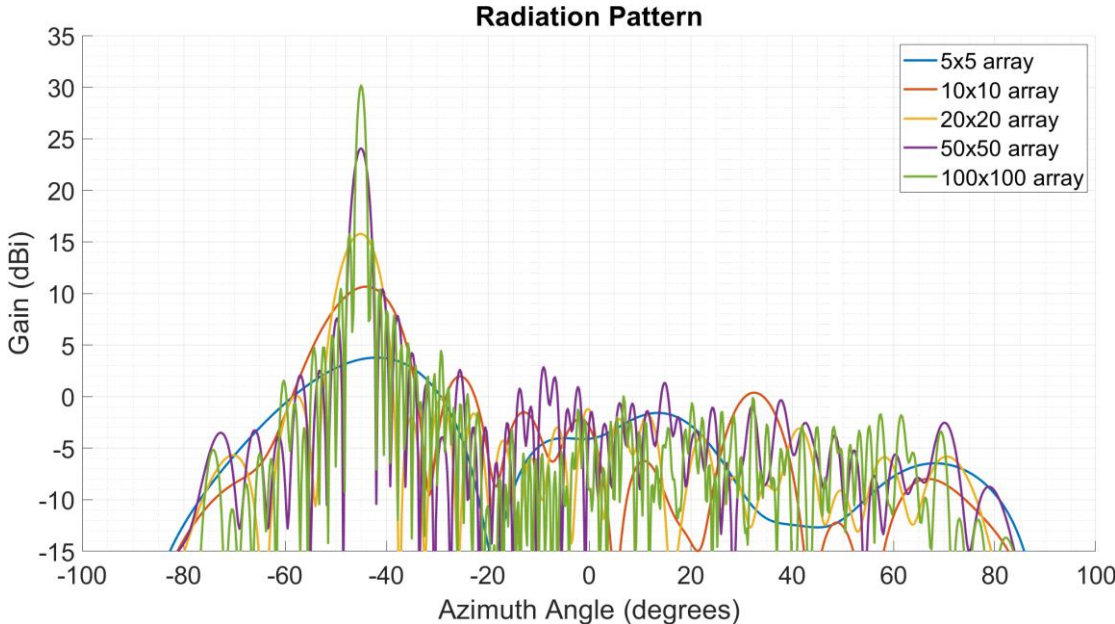
Figure 2-3. Simulated radiation pattern of antenna arrays with varying numbers of antennas and conditions similar to those described in Chapter 3.

and congestion issues have precluded large dense arrays. These factors have contributed to the lack of successful demonstration of the large-scale Terahertz antenna arrays that are necessary for high angular resolution imaging, with leading implementations consisting of tens or hundreds of antenna elements [40], [41].

In a typical dense phased antenna array, the ideal inter-element spacing is often most optimally one half of the operating wavelength, driven by grating lobe performance and other performance considerations [26]. Therefore, in this work, driven by the design goal of one degree beamwidth and the design operating frequency of 265GHz, the relationship seen in Figure 2-2 results in an aperture size of 5.7cm, leading to an array size design goal of 100x100 antennas, assuming dense antenna placement. Alternatively, this relationship can be viewed by assuming dense antenna placement and considering the relationship between number of antennas and mainlobe beamwidth, where more antennas increases effective aperture size and therefore decreases mainlobe beamwidth. A simulation of this relationship can be seen in Figure 2-3, which depicts simulated radiation patterns for 1-bit reflectarrays
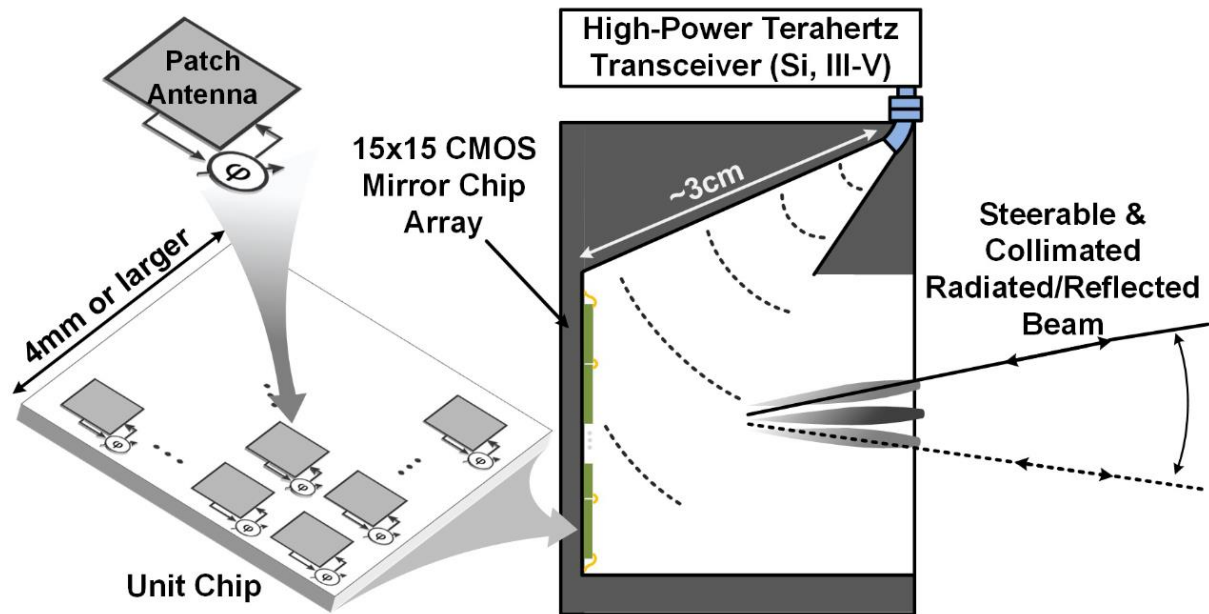
Figure 2-4. Conceptual diagram of reflectarray antenna.

with varying numbers of antennas and a spatial feed distance equal to the aperture size, the consequences of which are discussed in future sections.

2.2.1. Reflectarray and Transmitarray Antennas

Reflectarrays and Transmitarrays are close relatives of phased arrays, with a few key differences [42], [43]. A reflectarray is an array of reflective antennas, each with phase and/or amplitude control. The RF energy is distributed spatially through a feed antenna, which radiates energy onto the array, as seen in Figure 2-4. Each element in the reflectarray receives, applies a phase/amplitude weight, and reradiates in a fashion similar to a reflector antenna. For this reason, they are often thought of as controllable mirrors. Transmitarrays are closely related with the difference being that in a transmitarray the energy flows through the antenna array and is radiated out the opposite side in a manner that is more analogous to a lens [44]–[46]. Reflectarrays and transmitarrays were originally developed to mitigate the losses associated with RF signal distribution in classic phased arrays, however they also address phase synchronization issues in phased arrays, and mitigate routing congestion and density challenges in large two-dimensional arrays. There are additional losses incurred in the spatial feed configuration, generally known as aperture efficiency losses. Aperture efficiency losses are described by two main terms:

$$\eta_{ap} = \eta_{ill}\eta_{sp} \qquad (2.2)$$

where η_{ap} is aperture efficiency, η_{ill} is illumination efficiency, and η_{sp} is spillover efficiency. Illumination efficiency represents losses related to energy from the feed antenna which "spill over" the edge of the reflectarray or transmitarray and are not captured or beamformed. Spillover efficiency captures losses in directivity related to nonuniform distribution of illumination power over the reflectarray or transmitarray aperture, leading to a reduction in effective aperture size and associated directivity. Optimization of these terms requires careful codesign of the antenna array and its feed, in addition to sidelobe suppression considerations as discussed in future

30

sections. Typical aperture efficiencies are approximately 50-70% for optimized systems.

 In addition, in integrated systems with patch antennas having low radiation efficiency, there is an additional loss term due to the double penalty in radiation efficiency, as the RF energy is received and re-radiated. In monostatic radar applications where energy flows through the antenna array twice in a round-trip fashion, these losses are magnified with radiation efficiency losses being experienced four times. Reflectarrays and transmitarrays share many of the same applications as classical phased arrays, however they have particular motivations in the generation of Orthogonal Angular Momentum (OAM) waves [47]–[53], and any application where size and weight is a premium, especially airborne and space applications [8]–[11], [54]. Similar to phased arrays, reflectarrays and transmitarrays come in both fixed [55]–[59] and reconfigurable [55], [60]–[63] varieties. The reflectarray and transmitarray architectures are particularly desirable for integrated THz antenna arrays, where RF distribution losses are especially high. This work adopts the reflectarray architecture to allow for large arrays with relatively low distribution
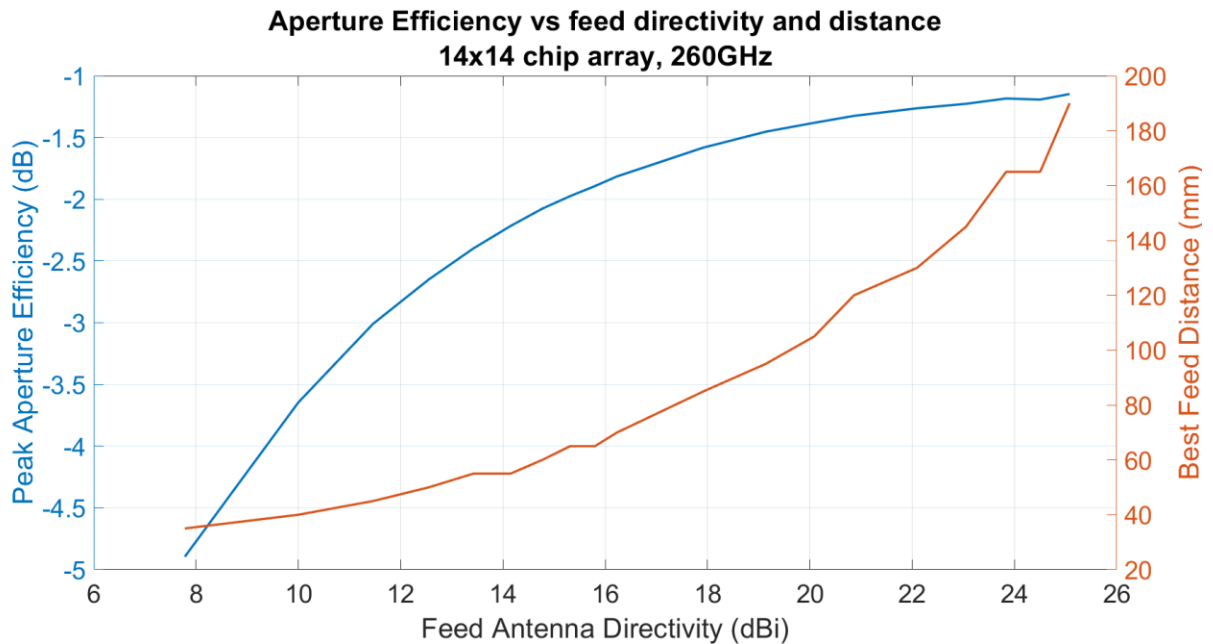
Figure 2-5. Relationship between feed distance, antenna directivity and aperture efficiency.

31

loss, and to avoid the signal routing challenges that come with traditional phased array architectures.

Despite improving upon the losses typical in THz phased arrays and their associated signal distribution losses, loss terms still exist in both transmitarrays and reflectarrays. Such losses are well documented [43] and generally are primarily described by spillover efficiency and illumination efficiency, which capture the effect of feed energy being both nonuniform over the antenna array aperture, and only a portion of the feed energy being incident on the antenna array. Typical optimized aperture efficiencies incur losses in the -2 to -3dB range and require a tradeoff between design parameters in array and feed geometry and appropriate design of the feed antenna's radiation pattern, with higher efficiencies resulting from feed antennas which are higher gain and placed further away. This relationship can be seen in Figure 2-5, simulated aperture efficiency for various combinations of feed distance and antenna directivity. Therefore, there is a tradeoff between aperture efficiency and total system volume.

As described previously, a reflectarray or transmitarray antenna depends heavily on the location of the feed source or receiver for the geometrical feed phase shift needed for calculation of phases required for beam forming in a specific direction. Any displacement between assumed feed location and actual feed location manifests as a tilting in mainlobe direction, as seen in Figure 2-6, which depicts the effect of mainlobe direction as a function of d_x, the error in x between assumed feed location and actual feed location, with a beam steered to -45 degrees. As will be discussed in future sections, a reflectarray or transmitarray with bidirectional phase shifters can enhance the performance of radar imagers by exploiting reciprocity and enabling collocation of Transmit and Receive radiation patterns and an effective stacking of the patterns, improving directivity and reducing clutter. However, with the narrow beams required for high resolution imaging, Figure 2-6 shows that minute levels of displacement between transmitter and receiver tilts their effective radiation patterns such that they are no longer coincident, severely degrading performance.
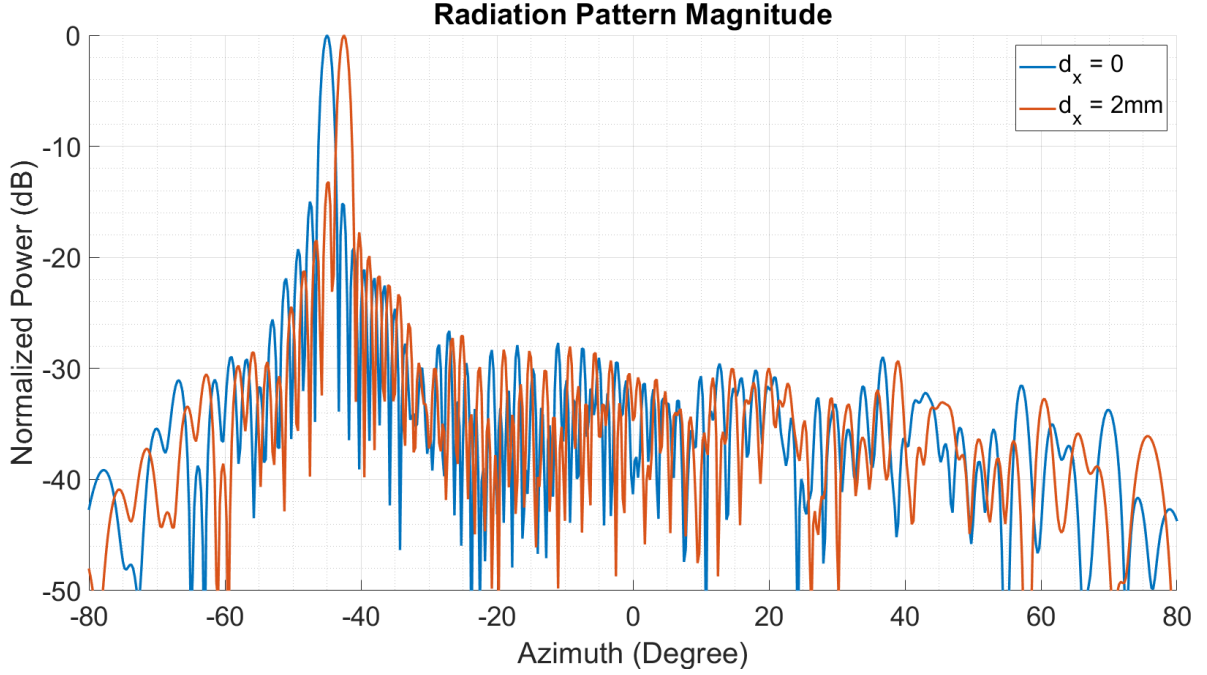
Figure 2-6. Feed location error d_x between assumed feed location in x and actual feed location in x, and its effect on radiation pattern.

Similar to phased arrays, the radiation pattern of a reflectarray is directly related to the fourier transform of fields across it's aperture, in a well-known relation between the two [26]. This relation is seen by matching terms between the two expressions. In an antenna array with N antennas each having a complex weight I_m, the array factor AF is given as

$$AF = \sum_{m=0}^{N-1} I_m e^{jm\psi} \qquad (2.3)$$

where the spatial term ψ is equal to

$$\psi = kd\cos(\theta) \qquad (2.4)$$

with k as wavenumber, d as the spacing between antennas, and theta as the desired direction with which to compute the array factor. By analogy, a discrete Fourier Transform is given as

$$X_{2\pi}(\omega) = \sum_{n=-\infty}^{\infty} x[n]e^{-j\omega n} \qquad (2.5)$$

where X is the frequency domain weights, x is the time-domain samples, and ω is frequency. In this analogy, an antenna array can be thought of as a spatial sampler, where each antenna is sampling a desired electromagnetic wavefront. Per this analogy, any periodicity in amplitude or phase across an aperture manifests as coherent tones in the Fourier transform, resulting in coherent sidelobes in the radiation pattern. As will be discussed in future sections, the near-field feed in reflectarrays mitigates the effect of this in phase quantized systems. However, additional periodicities can exist from (for example) regular perturbations in antenna placement. An example of this can be seen in Figure 2-7, which depicts simulated radiation pattern for a 98x98 reflectarray antenna with equal antenna spacing, and with a +300μm perturbation in antenna spacing every seventh antenna. The periodicity in phase and amplitude, arising from nonuniform antenna placement, is inherent to the array regardless of phase quantization and cannot be mitigated by
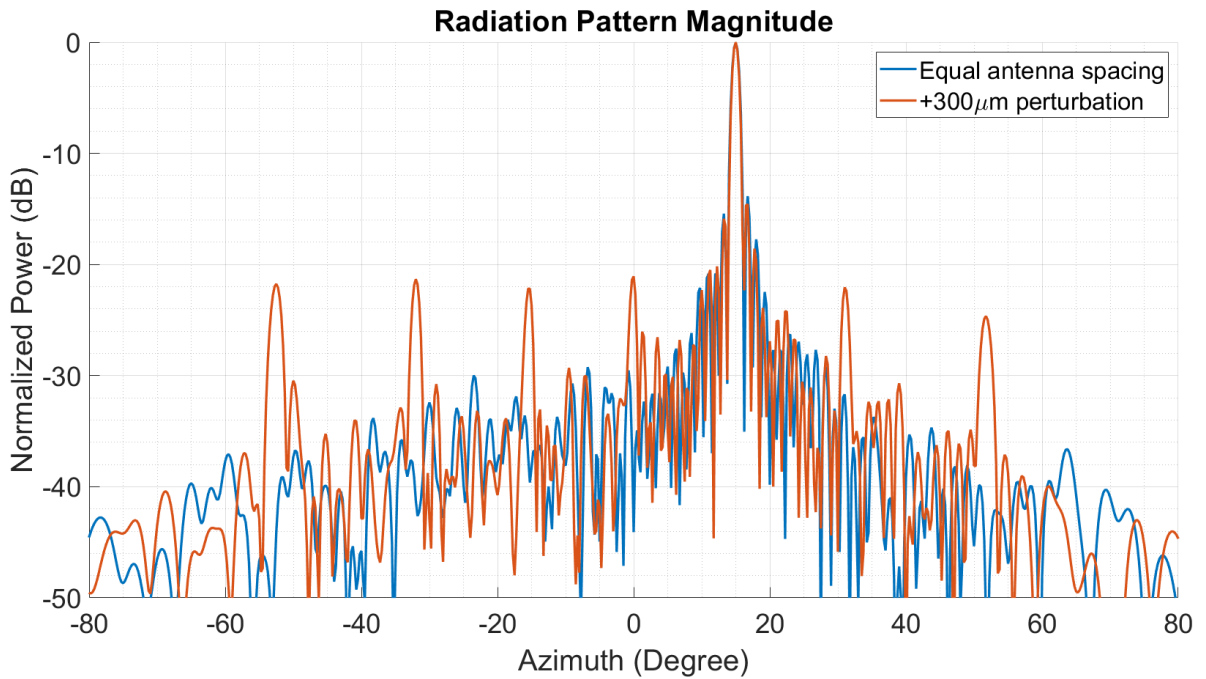
Figure 2-7. Simulated radiation pattern for 98x98 reflectarray with equal antenna spacing, and with an added +300μm perturbation in antenna spacing every seventh antenna.
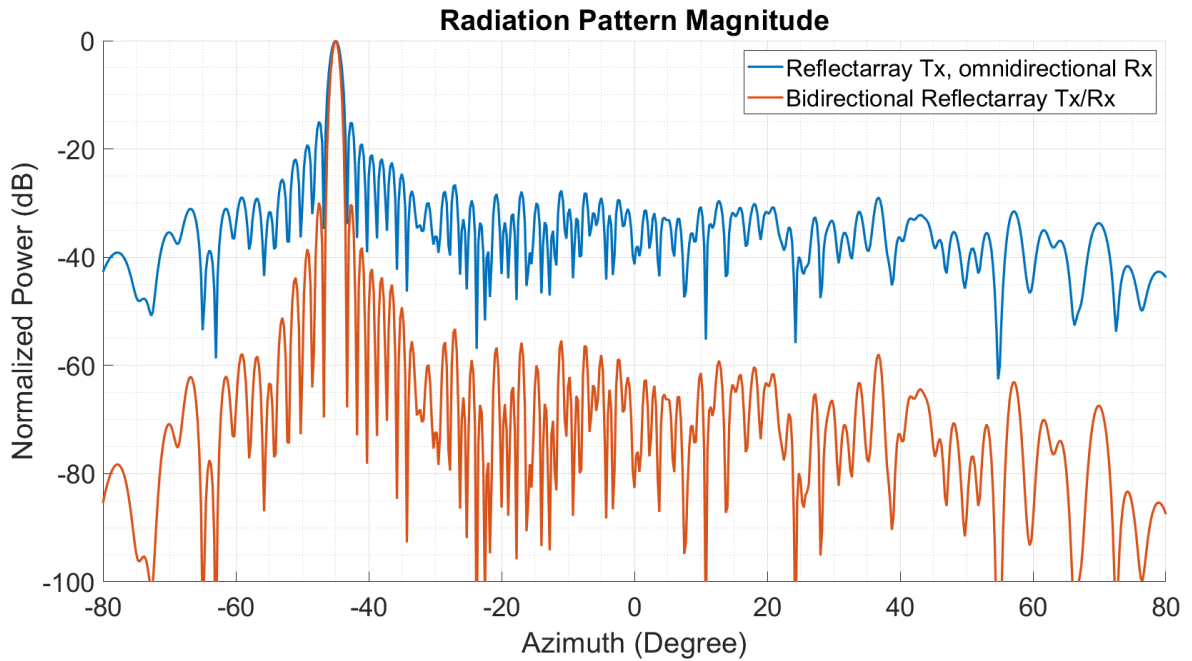
Figure 2-8. Simulated effective radiation pattern for a one-way reflectarray with omnidirectional receive antenna, and bidirectional reflectarray with collocated transmitter and receiver at the feed point.

measures such as sidelobe mitigation algorithms or feed placement, which are discussed in future sections. Therefore, to minimize sidelobes in an antenna array system it is crucial to minimize such periodicities. This becomes a relevant challenge in the assembly of the reflectarray described in Chapter 3, where tiles of 7x7 antennas are assembled together to produce a large array, leading to potential assembly and fabrication tolerances and errors which could result in such periodicities.

2.2.2. Phase Shifters

One of the more significant challenges associated with building THz phased arrays or reflectarrays is in the design of the phase shifter. A number of on-chip THz phase shifting approaches have been described, such as vector modulation [28], [29], [36], Y-vector networks [64], and variable capacitance [33], [35]. These approaches suffer a number of drawbacks which preclude their integration into large-scale THz dense antenna arrays, with the high gain and narrow beam required for THz imaging

applications. These approaches often suffer from high insertion loss often exceeding 10dB, further weakening the already-low THz signal and negatively impacting signal to noise ratio. In addition, these approaches tend to be large in size, with a required chip area that not only reduces available area for other circuits, but often exceeds the $\lambda/2$ x $\lambda/2$ footprint required for integration of dense phased arrays [29], [38], [39]. Finally, a number of these phase shifting approaches consume large amounts of DC power, frequently in excess of 10mW. This problem is magnified in large phased arrays which require many phase shifters. The large total DC power is not only undesirable for many applications, but in some cases untenable due to thermal constraints in integrated circuits. Certain demonstrated works perform phase shifting at lower frequencies before frequency multiplication which mitigates some of these issues, however this approach exacerbates issues such as DC power and chip area. Finally, the existing phase shifter implementations are directional, necessitating the use of bistatic radar architectures.

In addition to the above limitations, typical phase shifter approaches are unidirectional. Bidirectional phase shifters have the great advantage in monostatic reflectarray imagers of antenna reciprocity. Due to reciprocity, a reflectarray's radiation pattern such as one seen in Figure 2-3 to apply in both directions: from the feed antenna to a far-field target and vice-versa. Therefore, given a monostatic transceiver at the feed location and a reflectarray with bidirectional phase shifters, the effective radiation patterns are collocated, allowing for their stacking in the effective system-level radiation pattern, enhancing the directivity significantly. This can be seen in Figure 2-8, simulated radiation patterns for one-way operation and bidirectional operation for a 98 x 98 antenna reflectarray, where the one-way operation assumes a bistatic radar with omnidirectional receive antenna, and the bidirectional operation assumes collocation of transmitter and receiver.

As will be discussed in future sections, this work addresses these issues by the use of a passive one-bit phase shifter topology.

2.2.3. Phase Quantization

Radiation Pattern Magnitude
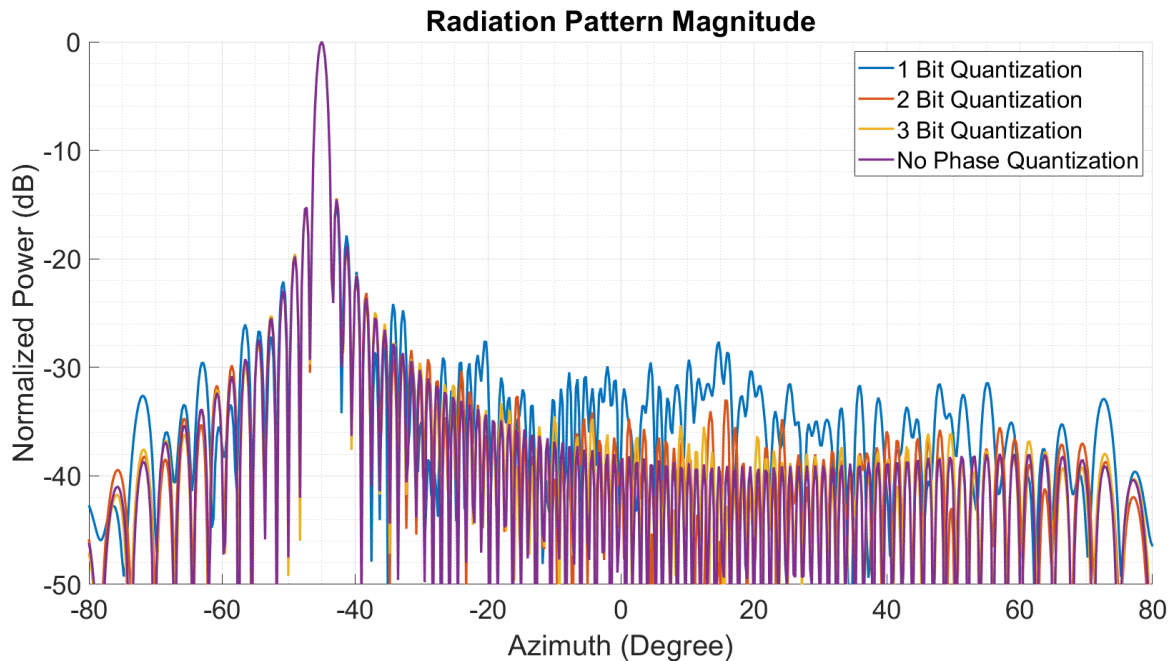
Figure 2-9. Effect of phase quantization on radiation pattern response in a dense 98x98 one bit reflectarray at 265GHz.

Reflectarrays and transmitarrays at RF [65]–[69] and mm-wave [70], [71] frequencies have been widely demonstrated and are generally well understood. Common implementations include phase shifters which rely on pin diode switches [72]–[75], varactors [66], [76]–[79], or RF MEMS switches [62], [63], [67], [80]–[82]. A number of emerging approaches incorporate liquid crystal materials [83]–[88], ferroelectric materials such as perovskites [11], [89], or functional materials such as graphene [47], [90]–[93]. Regardless of the approach taken for phase shifting, a commonality between all phased arrays, reflectarrays and transmitarrays is the crucial design decision of phase quantization. Practical arrays have phase shifters with finite resolution and a nonzero step size in phase, with discretized value of allowable phase shift. Consequently, a step in the process of calculating phases for a desired radiation pattern involves quantization from the ideal phase to the allowable discretized phases. The phase error term arising from this quantization noise leads to sidelobes in the radiation pattern, known as quantization lobes [94]–[104]. The relationship between phase resolution and average quantization lobe level is well understood and can be derived in a manner similar to quantization noise for Analog to Digital

37
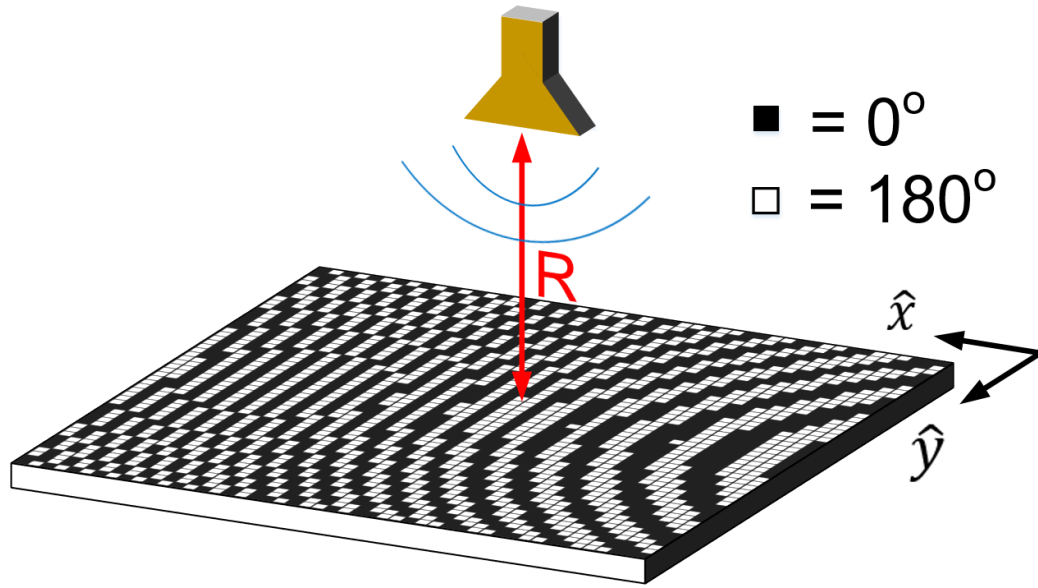
Figure 2-10. Array geometry with near-field feed leading to spherical phase term and decorrelation of quantization noise.

Converters [97], [105], [106]. An example of this relationship can be seen in Figure 2-9, which shows simulated radiation patterns for a 98x98 dense reflectarray at 265GHz with various levels of phase quantization.

In a typical uniformly spaced dense phased array with a beam steered off boresight, the ideal phase for successive elements follows a linear progression. The quantized version of this follows a "stairstep" pattern, leading to a phase error term which is the difference of these two and resembles a sawtooth function [107]. Due to the Fourier transform analogy between phased array complex weights and the radiation pattern's array factor, it can be said that the phase error's "sawtooth function" has well-defined frequency content which manifests as strong sidelobes in the radiation pattern. Equivalently, the correlation between phase error for adjacent antennas in the array results in coherent quantization lobes, where most of the quantization noise energy is focused in certain directions. A number of approaches have been proposed to mitigate this [94], [95], [101], [104], [108]–[112]. One particularly compelling one arises from the system-level design of transmitarrays and reflectarrays. In these systems, the placement of the feed antenna can be chosen such that the field which impinges on the antenna array is not planar but rather spherical, as seen in Figure

2-10. This arises from a difference in path length D_{ant} between the feed antenna and various elements in the antenna array, as given by

$$D_{ant} = \sqrt{R^2 + x^2 + y^2} \qquad (2.6)$$

where R is the distance from the feed antenna to the array in meters, and x and y are the distance from a given antenna to the center of the array, in meters. Equation 2.6 assumes the feed antenna is placed at the boresight of the antenna array, and that the feed antenna is accurately modeled as a point source.

In a typical antenna array with no spatial feed effect and no phase quantization, the phase calculation to steer a beam in a two-dimensional direction (φ_s, ϑ_s) is equal to

$$\phi_b = k(x * \sin(\phi_s)\cos(\theta_s) + y * \cos(\phi_s)\sin(\theta_s)) \qquad (2.7)$$

The additional spherical phase term is included in the calculation for quantized phase φ_q which is given by

$$\Phi_q = round(\phi_b - kD_{ant}) \qquad (2.8)$$

where the *round* operator serves to round the phase to the nearest valid value. As in all quantized systems, the phase quantization process introduces a phase quantization error term φ_e which is equal to

$$\phi_q = \phi_e - (\phi_b - kD_{ant}) \qquad (2.9)$$

or the difference between the ideal phase and its quantized state.

The inclusion of this spherical phase term serves to "whiten" the quantization error term, spreading the radiated quantization lobes to all directions [43]. This effect is a strong function of feed antenna placement and represents a crucial tradeoff between peak sidelobe level and aperture efficiency losses. An example of this can be seen in simulated data in Figure 2-11, which shows radiation pattern for various feed distances for a dense 98x98 one bit reflectarray at 265GHz. This approach and related approaches mitigate the peak quantization lobe level and have no effect on average quantization lobe level. Regardless they have been used extensively and have enabled the relaxation of phase resolution requirements even to the most extreme
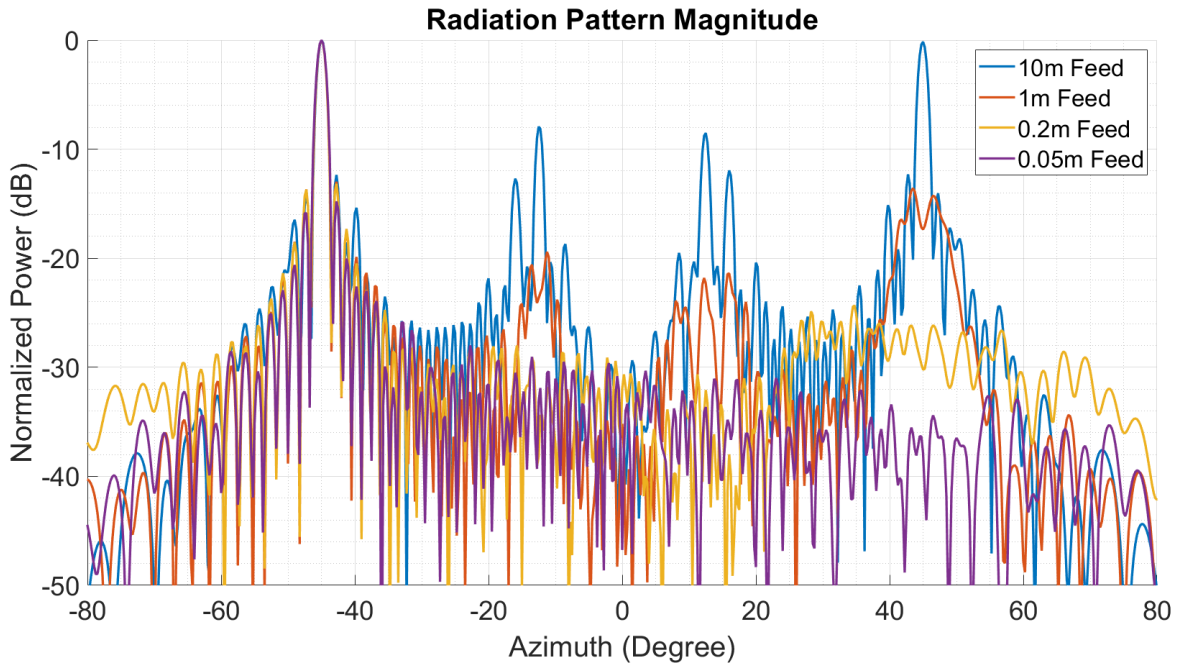
Figure 2-11. Effect of feed antenna distance on peak sidelobe level in a dense 98x98 one bit reflectarray at 265GHz.

case of 1-bit phase resolution, with a step size of 180 degrees. While this has enabled discrete designs to employ on-off based phase shifters using pin diodes or RF MEMS switches, those approaches still suffer from high power consumption and integration challenges with some solutions consuming 100 Amperes of current and requiring a dozen or more printed circuit boards [113]–[115].

While the above approaches serve to mitigate peak sidelobe level due to quantization noise, they do nothing for the average quantization sidelobe noise level, a reduction of which many applications would benefit from. There has been some work to improve upon this, with approaches typically relying on dithering in time and/or space to either move the quantization noise to more palatable directions and/or frequencies, or reduce it via integration [103], [104], [110], [112], [116]–[121]. While these approaches have shown some promise, practical implementation in discrete systems remains a challenge due to the rapid state change required of many antenna elements, exacerbating the digital bandwidth challenges discussed in future sections. In addition, while the near field feed approach is necessary for the breaking of phase error in quantized systems, it is at odds with the design considerations for maximum

aperture efficiency described in previous sections. Therefore, there is a tradeoff between peak sidelobe level and aperture efficiency. Optimal values of these requires a careful codesign of the array and feed.

2.2.4. Digital Bandwidth Requirements

The local memory for storage of beam states is an essential element of the design for real-time imaging as it relieves bandwidth burdens during rapid beam steering applications, and also enables performance enhancing algorithms, as discussed in future sections. The digital bandwidth B, in bits per second, required for the computation and communication of phase states in an imaging application, is equal to

$$B = \frac{N_{ant}N_{px}F_sN_b}{\tau} \qquad (2.10)$$

where N_{ant} is the number of antennas, N_{px} is the number of pixels in the resulting image, F_s is the frame rate of the imager in frames per second, N_b is the number of bits per beam state, and τ is the fraction of integration time allowed for updating of phase states. As an example, consider an application where a 100x100 antenna array is applied to a 10 frame per second, 100x100 pixel radar imager. Such an imager would require a beam steering update rate of 100k beam states per second, each requiring 10k phase shift values. Many applications require multiple sets of phases per beam direction for algorithms such as beam squint mitigation or sidelobe mitigation (discussed in future sections), requiring for example 8 phases per beam state, resulting in an effective phase update rate of 800k phase states per second. Assuming each antenna employs a one-bit phase shifter, each phase state consists of 10k bits, for an equal number of antennas. Based on these assumptions, the resulting data rate is 8G bits per second. If it is assumed that the array update time only consumes 10% of the total integration period per beam state, the short-term data rate is nearly 80G bits per second, an unattainable bitrate even in the context of parallelization. It also requires the constant computation of an equal number of bits, and the associated complexity and power consumption. Such a design is also

unnecessarily wasteful; redundant information is communicated as the array repeats it's beam steering sequence. In contrast, in the local memory approach taken in this work and introduced in future sections, the array's 778M bits of phase states are precomputed and loaded onto the array once at startup. In the above example, a low frequency 800KHz master clock cycles the array's antennas to their beam states with equivalent performance.

2.2.5. Beam Squint Considerations

Beam squint is a performance-degrading effect in wideband FMCW phased array radars [122]. This effect arises from the fact that in a phased array antenna, the phases for beamforming are set based on an operation frequency, often the center frequency of the FMCW radar. During the radar's operation, the phased array will experience varying instantaneous frequencies during the FMCW chirp. The difference between the instantaneous frequency and the frequency assumed during beamforming phase calculation leads to an error which manifests as beam squint. As a result, the mainlobe's direction is perturbed from the one intended during the beamforming operation. This effect can be seen in measured results in Figure 2-12,
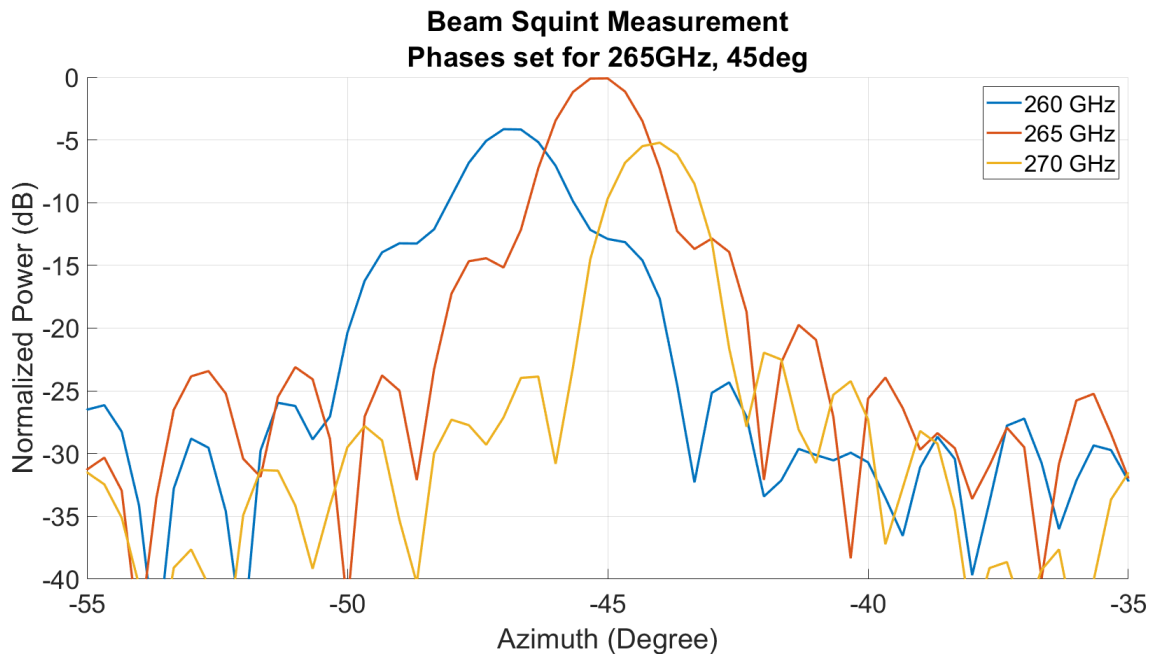
Figure 2-12. Beam squint demonstration.

where phases are set for 265GHz and radiation pattern measurements are taken at 260, 265 and 270GHz, where the beam's mainlobe is perturbed by more than three degrees. In these measurements, reduced amplitude at 260GHz and 270GHz arise from the on chip antenna's limited bandwidth. In this case where the perturbation in mainlobe direction significantly exceeds the mainlobe's beamwidth, the effective image resolution of the radar is degraded. This effect is particularly pronounced at large angles off boresight and for wideband systems. As will be discussed in future sections, this work addresses this issue through the use of in-unit memory and squint suppression algorithms.

Chapter 3

Design and Measurement of THz Reflectarray

This work aims to develop and demonstrate a high angular resolution THz reflectarray antenna, suitable for THz imaging and radar applications. A scalable design on-chip in 22nm FinFET technology allows for multiple chips to be tiled in a dense array, with the goal of 100x100 antennas for a 1x1 degree beam. The choice of THz frequencies allows for a large electrical size in a practical physical size. The reflectarray architecture choice enables low-resolution phase shifters based on CMOS switches, which combined with CMOS integration allow for superior performance in terms of DC power, RF loss, integration complexity and design simplicity. The CMOS integration, architecture and minimally-sized phase shifter topology allow for each antenna to have local memory, which enables both beam steering at practical speeds and also the development of algorithms to improve upon radiation performance and sidelobe level. This chapter details the features of the THz reflectarray system and its measurement.

3.1. Overview

The array is implemented as a reflectarray architecture operating at a center frequency of 265GHz. In a reflectarray architecture, a 2D array of antennas are fed RF energy spatially from a feed horn antenna [123]. Each antenna in the reflectarray receives, phase shifts, and reradiates the RF energy to steer a radiated beam. The spatial feed architecture is chosen to mitigate losses associated with distribution of

THz energy on-chip, to avoid signal routing challenges on-chip, and to shape the sidelobes associated with phase quantization. The feed horn antenna's radiation pattern and placement is co-designed with the antenna array itself to balance its role in system losses and sidelobe performance.

The antenna array is implemented on-chip, using Intel 22FFL 22nm FinFET process. Each chip measures 4 x 4 mm^2 and contains a dense array of 7 x 7 antennas, spaced at $\lambda/2$ at the operating frequency of 265GHz. The chip is designed such that it can be connected via wire bonds to either a carrier circuit board, or to adjacent chips. This allows for the chip to be tiled in the creation of a large dense array of antennas which is scalable in size to meet a desired application's performance requirements. This work's target of a 1 x 1 degree radiated beam is achieved by a 98 x 98 array of antennas, implemented as a 14 x 14 tiled array of chips.

Each of the chip's 7x7 antennas is identical, and consists of a dual-polarity patch antenna which receives the linearly polarized feed signal, phase shifts and re-radiates in the orthogonal linear polarity. The choice of dual polarity mitigates performance degradation due to undesired reflections of RF power in the structures surrounding the antennas, which are in the opposite polarity from the desired beam steered signal. The phase shifter is implemented as a one-bit phase shifter with a step size of 180 degrees. This is achieved through the use of two MOSFET switches which control the feed point of the antenna to be opposite sides of the symmetric patch antenna. Incident RF energy received from the vertical polarity is fed to either the left or right edge of the patch antenna, resulting in a radiated signal with a horizontal polarity and a relative phase shift of 0 or 180 degrees. The antenna is implemented in the ultra-thick C4 layer of the 22FFL process, a layer that is intended for IO pads.

Each of the 7x7 antennas per chip incorporates local memory for storage of phase states [123]. This allows for a sequence of beam steering patterns to be pre-calculated and loaded onto the antenna array *a-priori*. The patch antenna and ground consume area only in the top metal layers, leaving the entire lower metal layers and base layers (excepting two FETs as phase shifters) free for this purpose. Each antenna
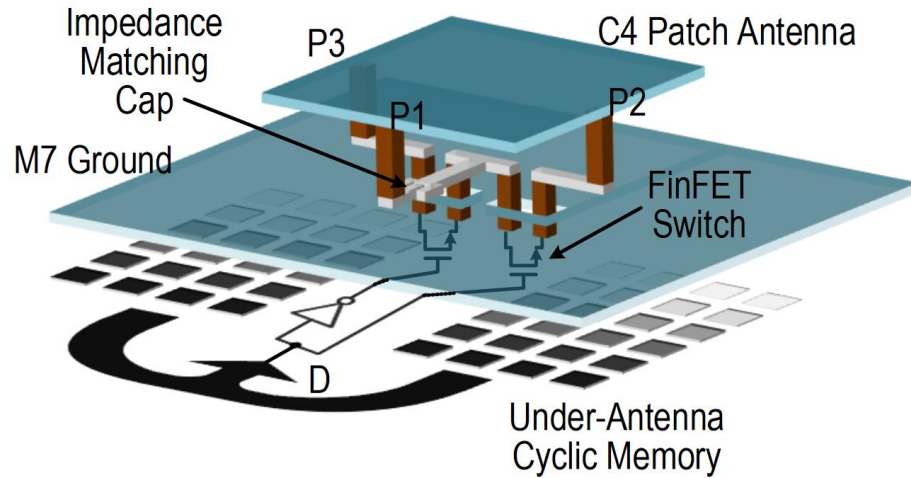
Figure 3-1. Dual-polarity patch antenna design with integrated one-bit phase shifter and in-unit memory.

contains about 81 Kbits of memory implemented as shift register ring buffers, yielding an equal number of beam steering states. During antenna operation, a master clock advances each antenna's shift registers in tandem, steering the beam to its next state.

3.2. Design of Antenna Element

The reflectarray is comprised of an array of identical antenna elements. In order to perform reconfigurable beam steering, each antenna element incorporates phase shifting capability. The antenna element is carefully designed for efficiency, bandwidth, and manufacturability.

A schematic of the antenna element can be seen in Figure 3-1. The antenna is designed as a dual-polarity patch antenna, receiving the feed signal TM_{010}, phase shifting, and re-radiating on the TM_{100} mode. The dual polarity design mitigates performance degradations associated with reflections in structures surrounding the reflectarray, which in a single-polarity design would interfere with the beam-formed wavefront to degrade its performance [43]. In the dual polarity design, such reflections are in the opposite polarity and are therefore attenuated by the cross-

46
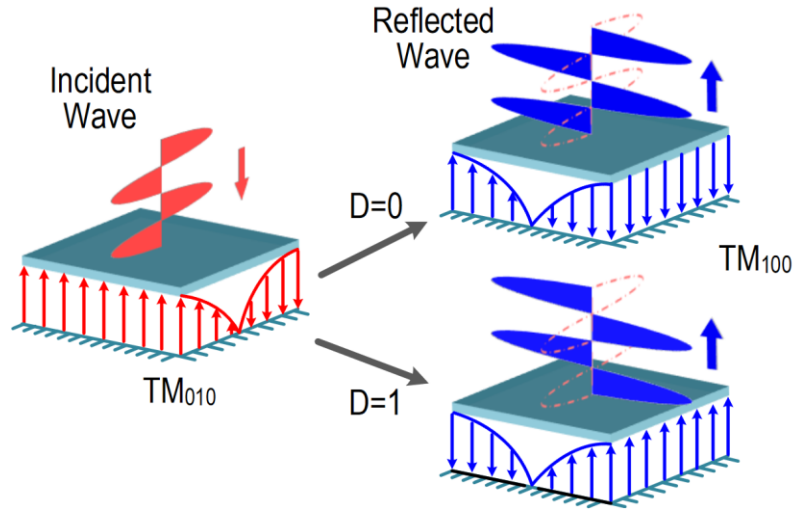
Figure 3-2. Dual-polarity patch antenna design demonstrating field distribution in phase state cases.

polarization response of the receiving antenna in a unidirectional reflectarray configuration.

The antenna incorporates a one-bit phase shifter, implemented as two MOSFET switches as seen in Figure 3-1. One of the two switches is on at a time, routing the received signal in the TM_{010} mode from the antenna's edge at point P1 to re-radiate it in the TM_{100} mode by feeding the antenna on the edges at points P2 and P3. As seen in Figure 3-2, by exciting the TM_{100} mode at either point P2 or P3, the resulting radiated energy has a relative phase of 0 or 180 degrees, thus implementing a phase shifter [123]. The MOSFET switches are controlled by digital logic, discussed in future sections. A capacitor, seen in Figure 3-1, implements impedance matching to account for impedances associated with antenna feed inductance. A circularly polarized incident wave will experience a flip in handedness of the reflected wave, similar to that discussed in [124].

The choice of phase shifter and the particular design described here confer a number of advantages over typical phase shifter designs in typical reconfigurable reflectarrays and phased arrays at THz frequencies. Aside from gate leakage, the two-MOSFET phase shifter design presented here consumes no DC power when the beam is in a static state, an essential property for arrays with the large number of antenna elements required for high angular resolution beam steering. In addition, the low
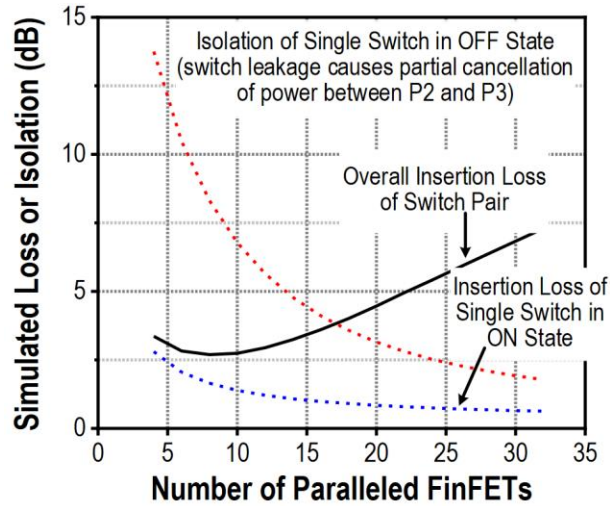
Figure 3-3. Dual-polarity patch antenna design demonstrating field distribution in phase state cases.

insertion loss, modeled to be 2.7dB in this design, allows for enhanced SNR in imaging and communication applications as compared to existing phase shifter designs discussed in previous sections. Furthermore, the extremely small chip area consumed by the two-MOSFET phase shifter allow not only dense integration of antenna elements in an array, but also leave the vast majority of chip area unused, allowing it to be used for other purposes such as computation structures or memory. This stands in contrast to typical on-chip phase shiter designs described in previous sections. An additional benefit of the two-MOSFET phase shifter is that it is by-design amplitude matched for the two phase configurations, and guaranteed by design to have a broadband, perfect 180 degree phase shift without phase errors, due to symmetry. Being free of resonant structures or frequency-dependent components such as varactors, the bandwidth of the system is only limited by the bandwidth of the antennas themselves, not the phase shifter. The phase shifter's bidirectionality allows the reflectarray to be incorporated into a monostatic radar configuration, reducing system complexity and ensuring the Tx and Rx beams are collocated, leading to a significant increase in effective directivity. Finally, the simplicity of the described phase shifter allows it to be easily and rapidly implemented in highly integrated systems.

During the design of the antenna and phase shifter, a design tradeoff exists in the sizing of the phase shifter's MOSFET switches, as seen in Figure 3-3. The two MOSFET switches are set to be equal in size for symmetry reasons. Increasing the size of the switches determines both insertion loss of the switch which is on, and the isolation of the switch which is off. The finite isolation of the "off" switch results in a portion of the feed signal from P1 leaking through to the unintended side of the TM_{100} polarity, creating a common-mode component in the TM_{100} mode and reducing the effective amplitude of the differential mode, and therefore reducing radiated power. The ideal point is dependent on system impedances and in this implementation has a total loss of 3dB.

The design decision to implement one bit phase shifters, while enabling a number of advantages described above, comes at a performance expense. As well-documented result of quantization in phase shifters is a performance degradation resulting from errors in the quantization of phase [43], [107], [125]. These errors result in sidelobes in the radiation pattern, known as quantization lobes. Quantization lobes are discussed in previous sections and the efforts taken here to mitigate them are discussed in future sections. One bit phase quantized reflectarrays are a well-known technique in discrete designs at lower frequencies [69],[126], [127] where control is complex and phase shifters often implemented as lossy and power-hungry varactors or pin diodes.

The antenna is implemented as a microstrip patch antenna, common to THz antennas in integrated processes [27][128]. Ansys HFSS full-wave electromagnetic simulation tools were used to assist the design process. The antenna's ground plane is implemented in a thick upper metal layer, with the radiator implemented as a square patch in the C4 layer. This layer is typically intended for input/output pads; a number of fabrication process changes were required to enable this [129]. Coupling between antennas is a well-known phenomenon in dense antenna arrays, known to cause detuning and radiation performance degradation due to near-field coupling of adjacent antennas [130]. This was mitigated in a number of ways. A ground ring surrounding each antenna assists in confining fields away from adjacent antennas.

Reflectarray unit antenna two-way frequency response (measured)
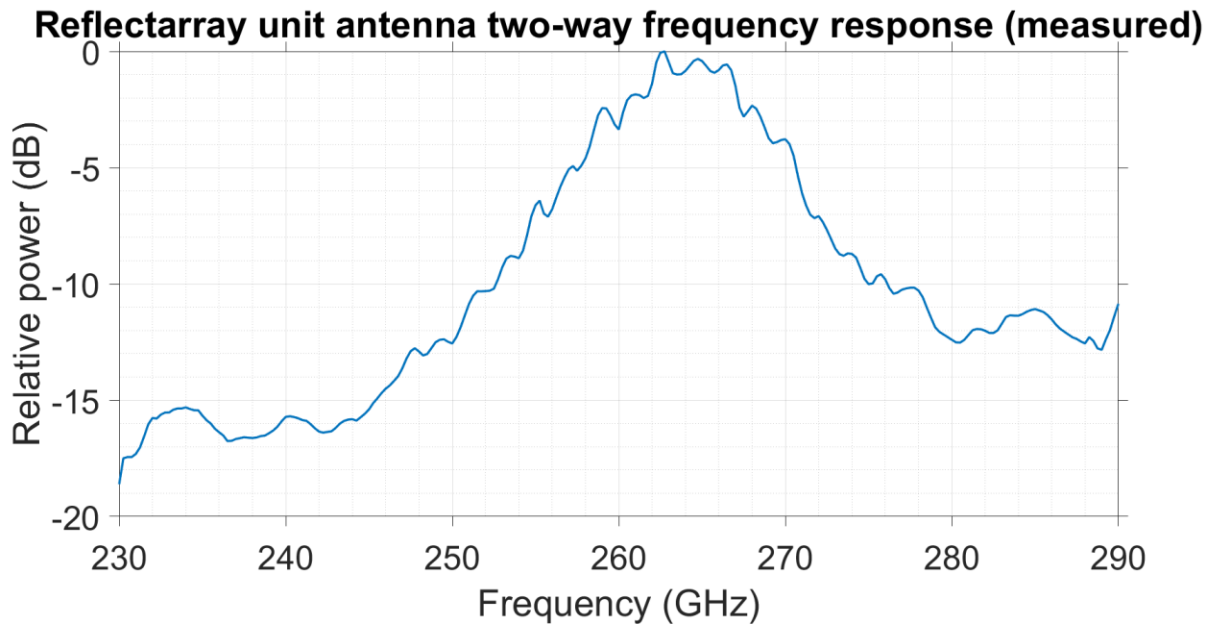
Figure 3-4. Measured round trip antenna bandwidth.

In addition, periodic boundary conditions and floquet modes were used during design simulation to incorporate the effect of adjacent antennas on detuning and radiation performance, with simulations suggesting antenna mutual coupling to be negligible.

The antenna is modeled to have a radiation efficiency of 9% and 10% in the TM_{010} and TM_{100} modes, respectively. Centered at 265GHz, the antenna is modeled to have an end-to-end 3dB bandwidth (incorporating both transmit and receive of the antenna) of 10 GHz. Measured antenna bandwidth, collected using techniques described in future sections, can be seen in Figure 3-4. The antenna is simulated to have a directivity of 7dB and 7dB in the TM_{010} and TM_{100} modes, respectively.

The antenna design, intended for dual-polarity operation at 265GHz, allows for scalable integration of dense antenna arrays, with the phase shifter occupying approximately 10 x 10 μm^2. The patch antenna's use of the thick C4 layer allows for high efficiency. The one-bit phase shifting technique enables low-power, low-loss and highly integrated dense antenna arrays.

50
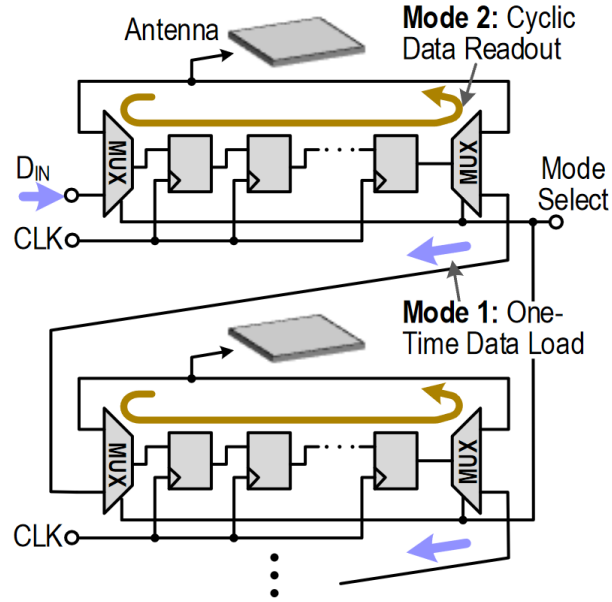
Figure 3-5. In-unit memory architecture.

3.3. Digital Architecture

This section describes the digital architecture of the 1-bit reflectarray chip. The chip's digital architecture enables integration of dense arrays, while incorporating a number of features to enhance performance.

When integrating multiple antenna elements into an array, the allowable area occupied by an antenna and it's supporting circuitry is constrained to a footprint with an area determined by the distance between adjacent antenna elements. Therefore, all circuits and structures associated with a single antenna much fit within such a footprint. The antenna's radiating element and phase shifting elements, previously discussed, only consume the top metal layers of the silicon process, with the exception of a small amount of active area and lower interconnect layers used for the phase shifter's two transistors. Therefore, nearly the entirety of the antenna footprint's active area and lower metal layer area is free for use by other circuits such as local memory or local computation circuits.

The one bit reflectarray chip applies this free area towards local memory. Within a chip, each antenna contains approximately 81k bits of local storage, for storing phase states for that antenna's phase shifter. As the phase shifter is one bit in nature, 81k bits of storage allows for the storage of an equal number of phase states.

The digital architecture for each antenna can be seen in Figure 3-5. Phase states for a sequence of beam steering patterns are pre-computed, and loaded onto the chip array during startup. The 81k bit local memory per antenna is implemented as a shift register. During program time (Mode 1), all shift registers for all antennas within a chip are placed in series, allowing precomputed phase states to be loaded onto the chip's memory using a SPI-like interface. Subsequently, the chip is placed in run mode (Mode 2), where the shift registers for each antenna are placed in a ring buffer configuration. A single master clock is distributed to each antenna, advancing the ring buffer to the next programmed phase state, steering the beam to its next direction.

In this implementation, shift registers were used as memory elements for storage of phase states. In more practical implementations, static RAM (SRAM) is used in lieu of shift registers. SRAM-based memory implementations come with many orders of magnitude improvement in memory capacity and power consumption. In addition, an SRAM based approach has robustness advantages, where a fabrication defect only affects a single phase state of a single antenna. In contrast, a fabrication defect in a single shift register prevents successful programming of all antennas downstream of the failure, resulting in a design which is much less tolerant to fabrication defects. Nevertheless, the concept of local memory as an enabler for rapid imaging in large arrays is successfully demonstrated.

The use of shift registers in this implementation represents a worst-case scenario for power integrity. This is due to the near-simultaneous switching of >4 million shift registers within one chip, and the associated impulse-like spike of current. If left unmitigated, this spike of current is approximately 2.3 Amperes in height, over a duration of 7 ns, for a total charge of approximately 16.1n Coulombs. Given finite

resistances and inductances in the power distribution network, the corresponding voltage droop could corrupt memory states. This is particularly noticeable in the chips in the center of the array which have their power supply fed through as many as seven chips' worth of bondwires and on-chip power routing. A number of measures were taken to mitigate this risk. First, on-chip power routing and wirebond profiles were designed to minimize impedances to the extent possible, using wide and thick power distribution and low-profile bondwires. Secondly, within the memory for one antenna, the shift register block is implemented as two blocks: a block of 40690 shift registers which latch on the rising clock edge, followed by an equal number which latch on the falling edge. Therefore, assuming the clock edge rate is slow enough for transients to settle, the pulse of current at worst-case is half its original height. This comes at the expense of reduced timing margin and the reduction in effective memory capacity by one bit. Thirdly, clock delay buffers between each antenna were incorporated within a chip, delaying the clock feed to each antenna by approximately 100ps, spreading out the current pulse. This limits the maximum switching speed of the array to approximately 200MHz which has no practical impact as the array's switching speed is limited by other factors. Fourth, the processes' MIMCAP layers were used, along with MOMCAPs in available base-layer area to implement on-chip decoupling capacitance to the maximum extent possible. The modeled decoupling capacitance per chip is approximately 92 nF, limiting voltage droop per switching event to approximately 175 mV, shown via simulation to have appropriate levels of margin for data corruption.

The use of shift registers versus SRAM-based approaches also leads to an increased VDD current and power consumption, primarily due to switching currents during shift register operation. This ultimately constrains the maximum theoretical switching speed of the array due to constraints on bond wire fusing current, which limit bondwire current to approximately 0.9 A. In this implementation, the worst-case current occurs for bondwires on the edge of the array which convey current from PCB to all chips in the center of the array. The constraint of 0.9 A of DC bondwire fusing current constrains the chip array clock to a maximum rate of 3 MHz

(in operation mode with all chips switching simultaneously), per circuit models, with appropriate margin applied. Future implementations employing SRAM based memory would not only increase the memory density by an order of magnitude and provide the other benefits listed previously, it would significantly relax the constraints on switching speed and power.

3.4. Chip Level Array Architecture

This section details the chip-level architecture of the reflectarray chip, and the associated considerations. A number of challenges exist on the chip-level, particularly when allowing for the need to tile the chip into a large array, and complex assembly with many chips and interconnections; the chip must be robust to failures in fabrication and assembly.
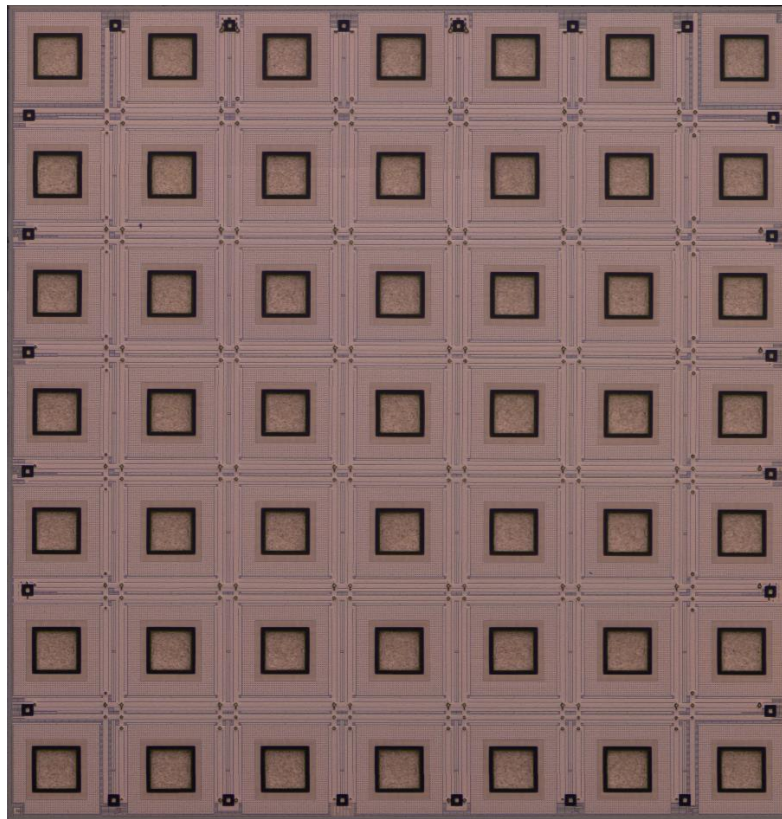
Figure 3-6. Reflectarray die photo.
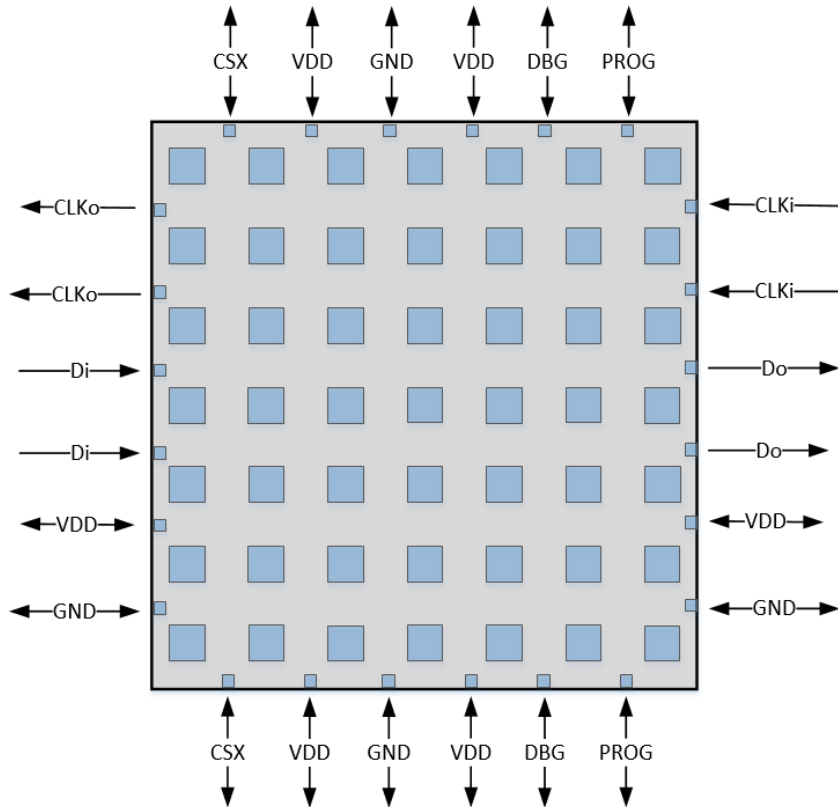
Figure 3-7. Reflectarray chip I/O architecture.

A die photo can be seen in Figure 3-6. The chip, measuring approximately 4x4 mm^2, was implemented in the Intel 22FFL 22nm FinFET process. The chip consists of a 7x7 antenna array, with the aforementioned 265GHz antennas integrated with the aforementioned digital subsystem with 81k bits of local storage per antenna. The resulting available memory per chip is approximately 3.97M bits. Each antenna is spaced at a distance of 0.50λ x 0.53λ in X and Y dimensions, respectively. The on-chip antenna spacing is such that antenna-antenna distance is preserved in adjacent antennas both within a given chip, and adjacent antennas on two adjacent chips.

As is described in future sections, the final assembly includes 196 individual dies in a tiled array, connected by more than 2500 bondwires. Given the scale and complexity of such an assembly, the risk of failures in chip fabrication or assembly is high. Accordingly, the chip-level architecture is designed to be robust; the most likely failure modes such as isolated wirebond open circuits have no impact on array
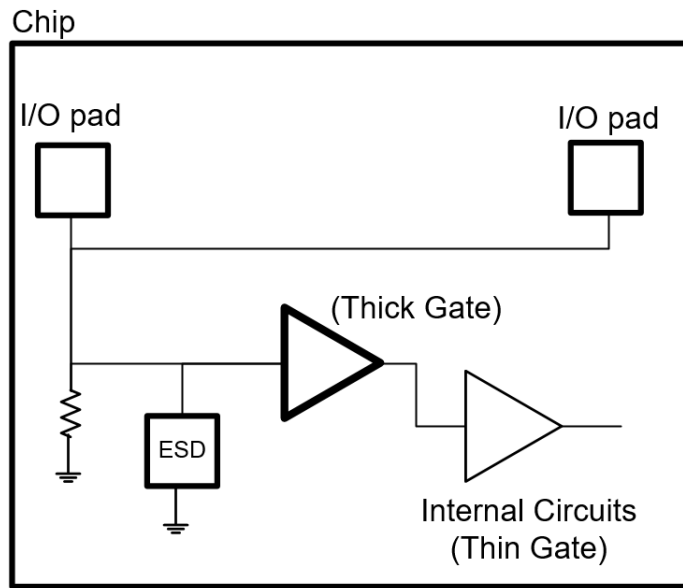
Figure 3-8. Reflectarray chip I/O internal architecture.

operation. Less likely failure modes such as chip fabrication defects, bondwire short circuits, or multiple correlated bondwire open circuits cause a graceful degradation of array performance with a small number of failed antennas.

The array's I/O architecture can be seen in Figure 3-7. Clock and Data signals for programming of phase states and cycling of phase states are fed between adjacent chips within a row. Horizontally-aligned clock and data signals, being of high speed, are redriven by each chip for speed and signal integrity reasons, at the cost of these signals being unidirectional. Therefore, the risk of assembly failures is mitigated by budgeting two wirebond pads per each of these signals. The DBG, CS and PROG signals are slow digital signals used to control the state of the array, and are fed between adjacent chips within a column. Being "slow" signals, these do not require on-chip redriving and are therefore bidirectional.

The internal architecture of these "slow" I/O pads can be seen in Figure 3-8. An ohmic connection exists between the two I/O pads on opposite edges for a given signal. This approach allows the signal to be fed from either or both of the two I/O pads. For each of these signals, each column of chips in the array is fed from the
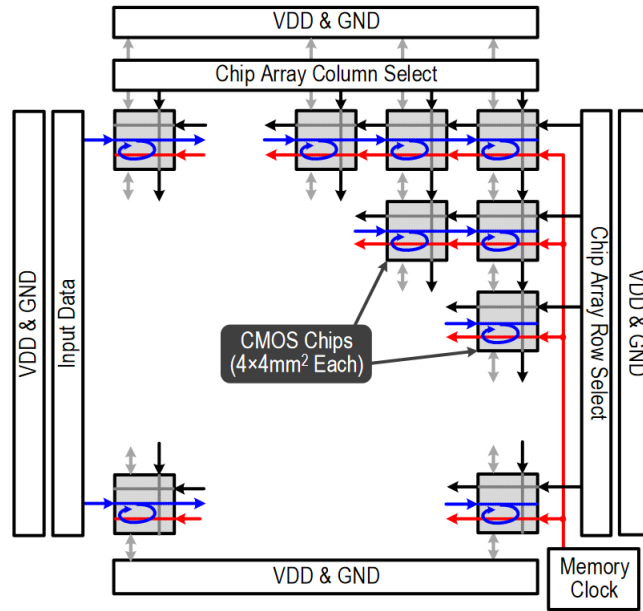
Figure 3-9. Reflectarray system level digital architecture.

PCB from both the top and bottom edges of the chip array, allowing the signal to be successfully conveyed in the case of a single open-circuit within a given signal within a given column. In the case of multiple open circuits within a given signal within a given column, the chips between the two failures revert to the most conservative default state as determined by pullup/down resistors within each chip.

Each chip contains a chip select signal, as seen in Figure 3-9. When asserted, incoming clock and data signals are fed to shift registers within the chip. When not asserted, these signals are fed directly from input pad to output pad, bypassing the chip's internal circuits entirely. This approach for selecting columns of chips, combined with PCB-level muxing of clock and data signals for selecting rows of chips, allows each chip to be addressed individually. Therefore, chips with fabrication defects in their shift registers can be bypassed, allowing the rest of the array to function with only a minor degradation in performance.

The PROG signal is used to set the array to be in programming mode (Mode 1) or operation mode (mode 2). The DBG signal is used for debugging and bringup purposes.

57

3.5. System Level Architecture

The design of a reflectarray system represents complex tradeoffs between performance metrics such as gain, sidelobe level, volume, and cost. This section contains the design decisions and considerations in the reflectarray system and it's two primary components, the feed structure and the array itself. A high level depiction of the reflectarray system can be seen in Figure 3-10. A THz FMCW transceiver produces THz energy which is fed through a feed antenna, which radiates onto the reflectarray. Each element within the reflectarray receives, phase shifts, and re-radiates to steer the beam in a desired direction. Echoes from a radar target are incident on the reflectarray, which steers the incident energy back towards the transceiver. A primary advantage of the one-bit phase shifters described here is their inherent bidirectionality. This allows for exploitation of reciprocity in the antenna array's radiation pattern, resulting in Tx and Rx radiation patterns which are coincident by design. As a result, the Tx and Rx subsystems of the transceiver can be collocated and the effective directionality of the reflectarray is squared. The decrease in effective sidelobe energy results in reduced clutter in the radar image and
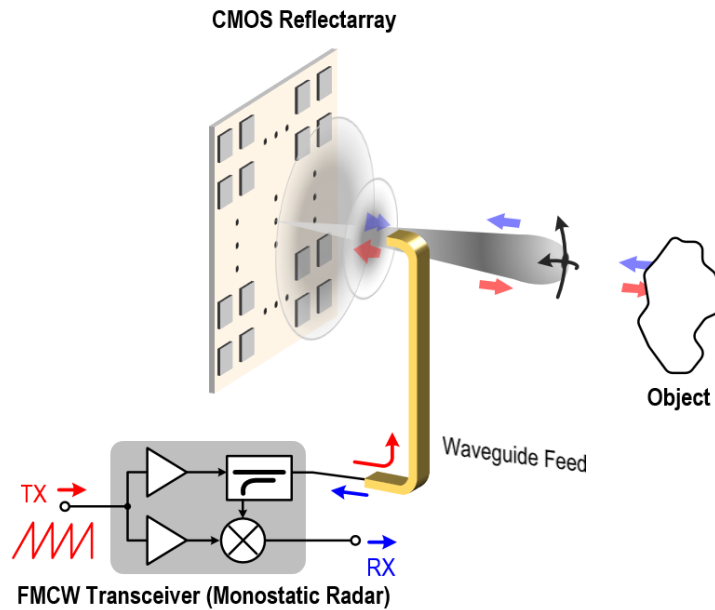
Figure 3-10. Reflectarray imaging radar architecture.

therefore a higher image quality. A simplified model, predicting radiation pattern magnitude and phase for the given reflectarray system parameters, can be found at https://github.com/nathan554/THz_Reflectarray.

3.5.1. Reflectarray Assembly

A schematic depiction of the reflectarray assembly can be seen in Figure 3-11. The reflectarray is implemented as a 14x14 tiled array of the previously described chip, resulting in a 98x98 antenna array. The square aperture, measuring approximately 5.6 x 5.6 cm^2, is chosen to meet the beamwidth goal of 1° as described previously with the goal of yielding a 100x100 pixel radar image.

The implementation of the reflectarray can be seen in Figure 3-12. The array contains 2520 wirebonds between chips and from array edge to PCB, for conveyance of power and signals for array programming and control. Automated die attach and wirebonding was performed by Intel Corporation in Chandler, AZ and employs die attach film for flatness in the chip array. A die-die spacing of 50μm ensures a
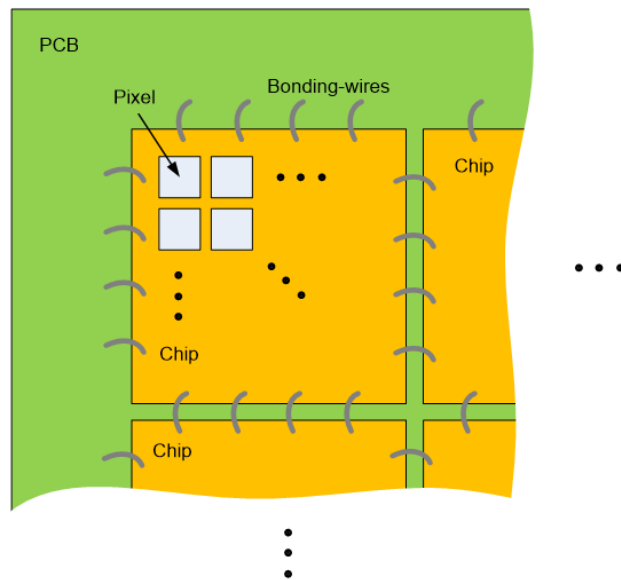
Figure 3-11. Schematic depiction of reflectarray created as tiling of identical CMOS chips, stitched together by bond wires.
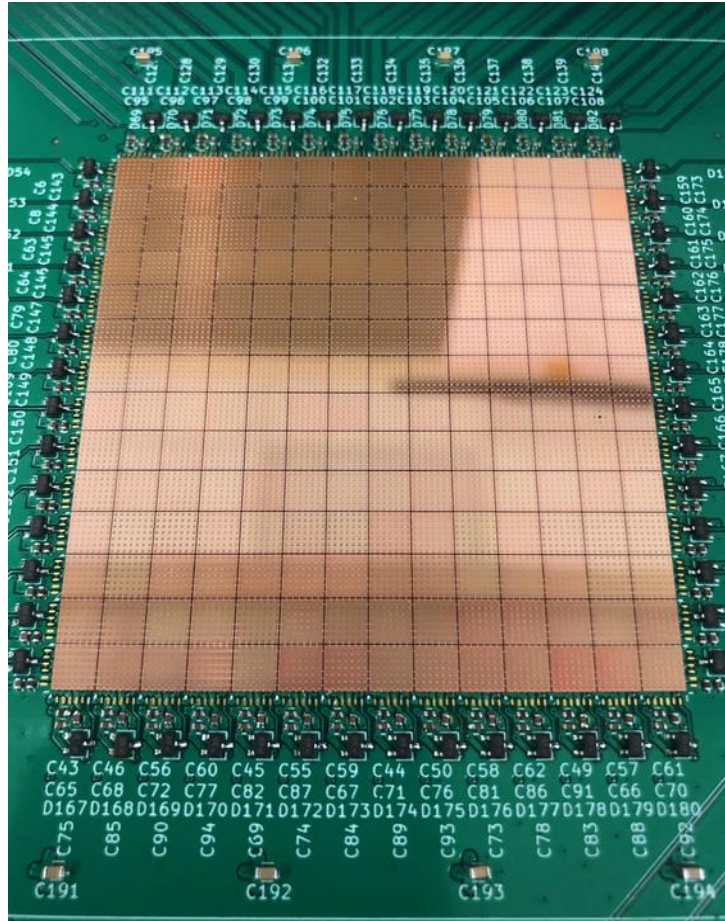
Figure 3-12. Realized implementation of reflectarray created as tiling of identical CMOS chips, stitched together by bond wires.

constant antenna-antenna spacing, consistent with the chip design. Efforts were made to minimize the vertical profile of the wirebonds to minimize interference with the radiation pattern of nearby antennas; simulations suggest the effect of bondwires on antenna radiation patterns was minimal.

The reflectarray PCB contains a number of supporting circuits for power integrity, ESD protection, test and bringup, and connection to control and measurement circuits. A 3D printed enclosure protects the chip array while minimizing blockage during operation.

3.5.2. Feed design

The antenna array combines with a feed structure to comprise the reflectarray system. As previously discussed, the feed antenna design and geometry plays a critical role in reflectarray performance metrics such as peak sidelobe level and aperture efficiency, as discussed in Chapter 2. Therefore, a codesign of antenna array and feed structure is critical.
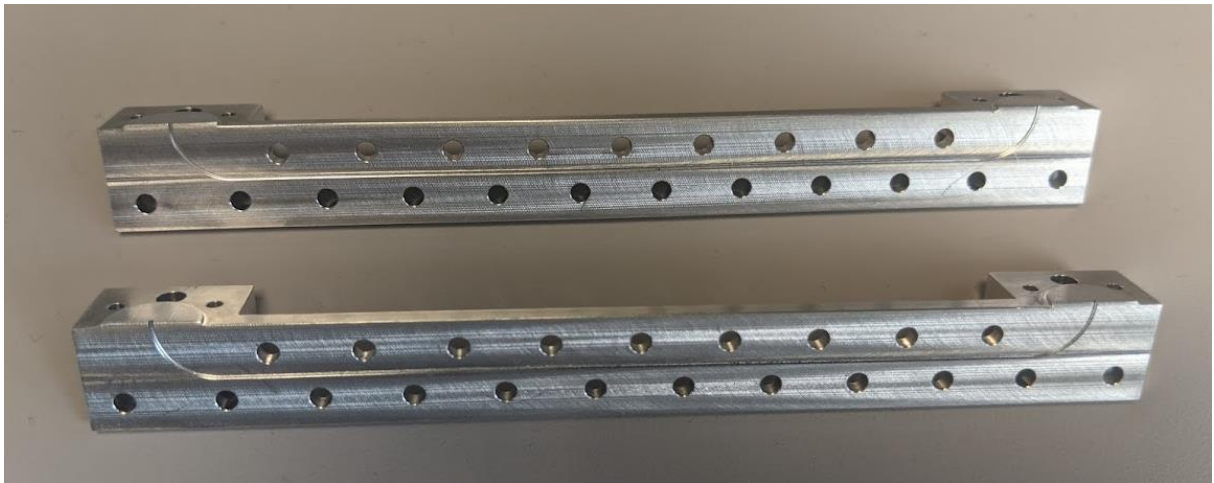
Figure 3-13. Custom machined waveguide piece serving as feed for reflectarray. Waveguide flanges, used for insertion loss measurements, were removed subsequent to this photo.
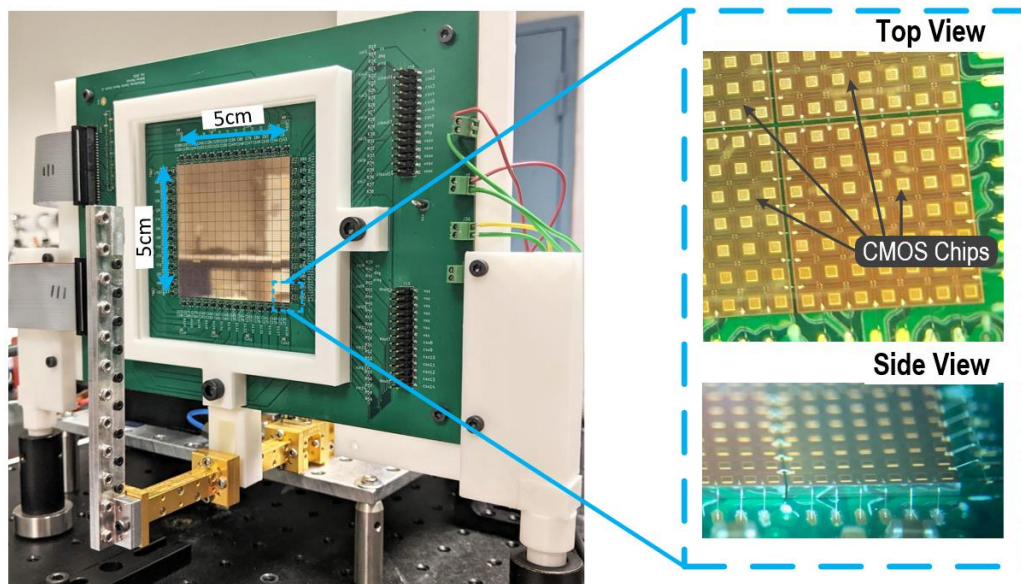
Figure 3-14. Completed reflectarray prototype depicting stitched CMOS chips, waveguide feed, and 3D printed fixtures.
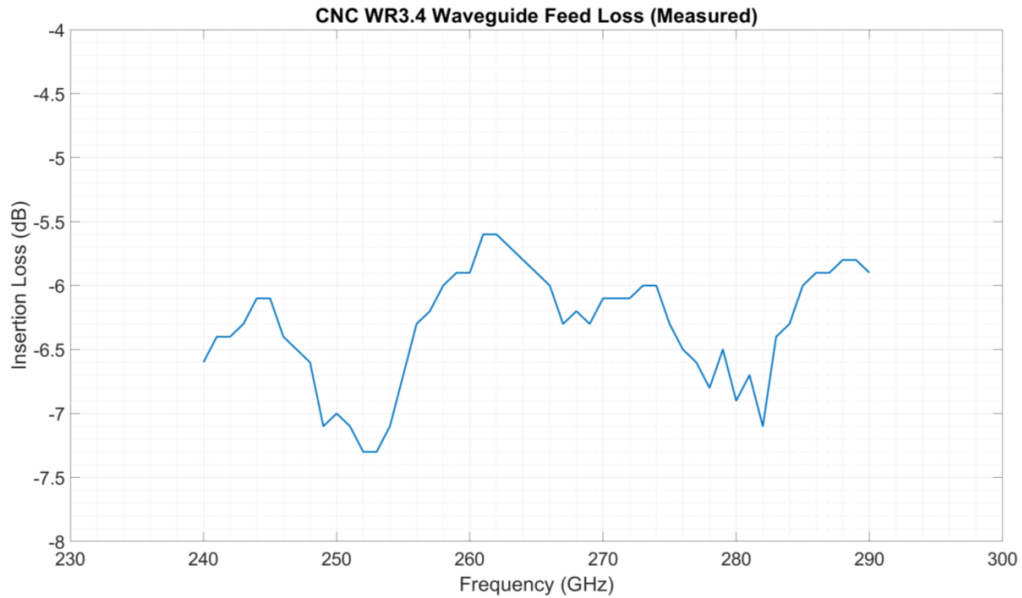
Figure 3-15. Reflectarray feed waveguide measured insertion loss.

A schematic depiction of the feed waveguide and antenna structure can be seen in Figure 3-10, and photos showing the feed structure and complete realized system can be seen in Figure 3-14. The geometry depicted carries a number of advantages. By minimizing the volume of structure in the viewing area of the reflectarray, standing waves are minimized between the feed structure and the reflectarray. In addition, it mitigates blockage of the reflectarray's viewing area, with reflections and diffractions of the reflected energy and the associated performance degradation.

The feed structure is CNC machined (Protolabs Inc, Maple Plain, MN) from 2021 grade Aluminum. As seen in Figure 3-13, it consists of two identical halves in a split-block structure, representing a WR-3.4 waveguide approximately 11cm in length, with WR-3.4 flanges on both ends. The two halves are held together with low profile M3 screws and nuts.
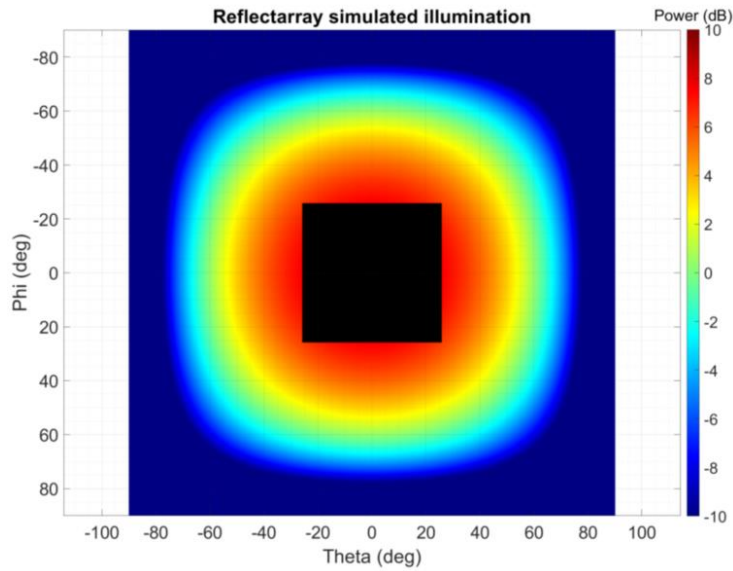
Figure 3-16. Simulated illumination power distribution across reflectarray. The black square represents the portion of illumination power captured by the reflectarray.

Source	Loss
Feed waveguide loss	-6dB
Aperture efficiency	-6dB
Rx patch antenna efficiency	-9dB
Phase shifter	-3dB
1 bit phase quantization loss	-4dB
Tx patch antenna efficiency	-10dB
Total loss	**-38dB**

Directivity	**42dBi**
Total gain	**4dBi**

Table 3-1. Estimated losses in THz reflectarray system.

The insertion loss of the waveguide and feed structure are critical, as this loss is doubled in an imaging radar application where the energy passes through the structure twice. The loss of the structure is measuring using VDI WR-3.4 Frequency Extenders (Virginia Diodes, Charlottesville VA). The measured one-way loss of the

63

feed structure can be seen in Figure 3-15. At the operating frequency of 265GHz, the one-way loss is approximately 6dB, or 0.55db/cm.

Following loss measurements, the waveguide flange was removed on the reflectarray feed side to further minimize feed blockage. The feed antenna is therefore a simple waveguide opening. The feed antenna's simulated directivity is 9dBi. The feed structure is placed with the phase center at a distance of 5.8cm from the reflectarray, a balance of aperture efficiency and sidelobe suppression as discussed in previous sections. Figure 3-16 shows a simulation of the energy from the feed structure captured by the reflectarray, where the black square represents the portion of illumination power captured by the reflectarray. The resulting effective edge taper is 1.3 dB, with a simulated aperture efficiency of -5.4 dB.

Table 3-1 shows an accounting of all losses incurred in the reflectarray implementation. There exist opportunities to improve system losses above those listed here. For example, an integrated solid-state THz transceiver placed at the feed point would eliminate feed waveguide loss, and improved feed design would improve aperture efficiency to an optimal point of approximately -2dB, for a gain of ~4dB.
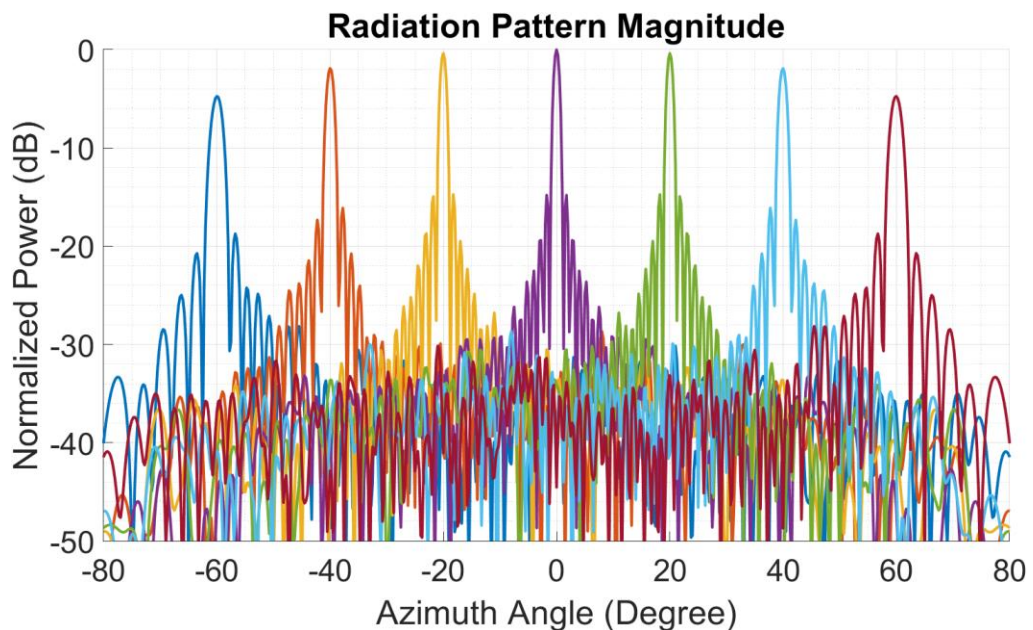
Figure 3-17. Simulated one-way radiation patterns of one bit reflectarray.
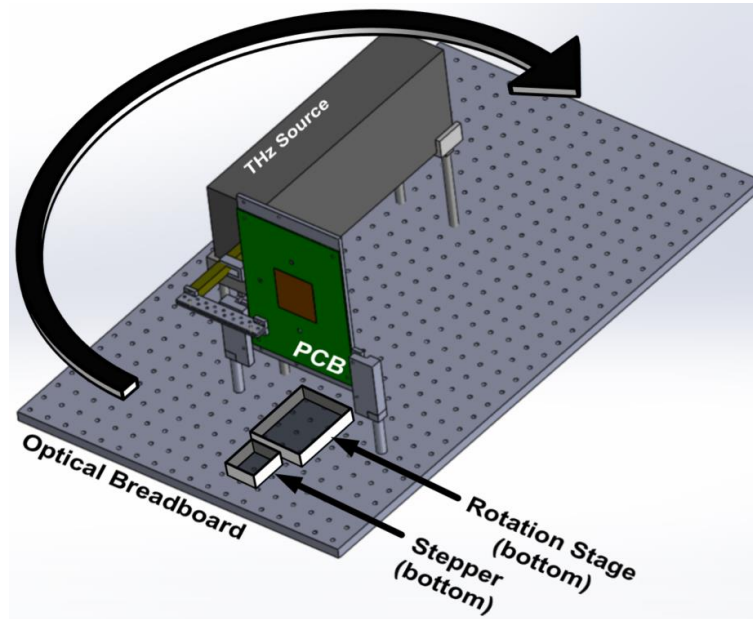
Figure 3-18. Top view depiction of reflectarray radiation pattern measurement mechanical setup, with H-plane test fixturing.

Finally, on-chip patch antenna design could be improved to increase radiation efficiency to a more typical maximum radiation efficiency of -6dB, an improvement of 7dB when including transmit and receive. Figure 3-17 shows a series of simulated one-way radiation patterns with the given reflectarray parameters and beam steered in different directions.

3.6. Testbench and Measurement Setup

The measurement of a high angular resolution reflectarray represents a number of challenges in practical implementation. Equipment cost and availability constraints dictate that a single THz source and receiver be used to measure radiation patterns. At the same time, the geometry between the feed structure and reflectarray must remain fixed, as this geometry is critical to calculation of phases for beam steering. These structures' geometry must remain fixed within a small fraction of a wavelength to preserve the phase relationship. Therefore, while measuring azimuth and elevation
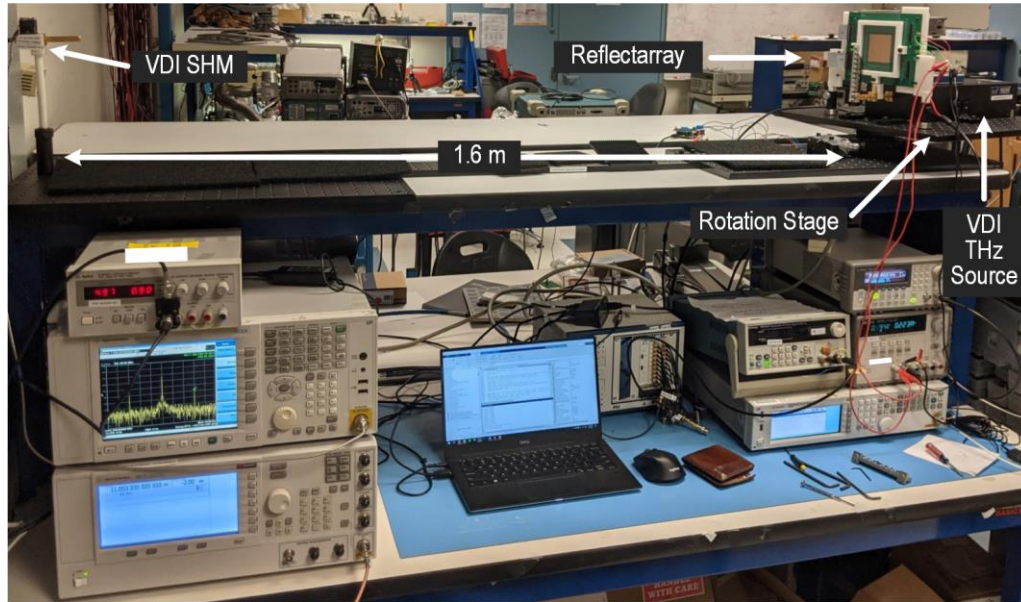
Figure 3-19. Photo of realized reflectarray radiation pattern measurement setup.

cuts of the radiation pattern, it is necessary to either fix the geometry of a stationary reflectarray and feed while rotating a receiver, or fix a stationary receiver while rotating the reflectarray and feed structure. The latter scheme was chosen in this test setup.

At the same time, the expected beamwidth of one degree places severe constraints on the resolution and precision of a rotating table; the table must be able to rotate with resolution much smaller than a fraction of a degree to adequately measure angular samples of a sharp beam. These requirements make manual rotation impractical. Instead an automated setup was developed, with reflectarray, feed structure and THz source mounted to an optical breadboard which is in turn mounted to a rotation stage (Edmund Scientific EDM-38195-A). The rotation stage is driven by a stepper motor (Stepperonline PG-5) with a planetary gear ratio of 5, allowing for an angular resolution of 0.0029 degrees when rotating the reflectarray. The stepper motor is driven by a motor driver which is controlled by a PC, allowing for automated measurement. A top-view schematic diagram of the mechanical test setup can be seen in Figure 3-18, while the realized test bench can be seen in Figure 3-19. THz absorbing material surrounding the test fixtures mitigates reflections of

THz energy from nearby structures, preventing them from contaminating the radiation pattern measurement.

The reflectarray is supported by a rigid 3D printed structure, as seen in Figure 3-14. The structure fixes the reflectarray and ensures it is rigidly centered over the center of rotation of the rotation stage. It also has features to ensure the desired (fixed)
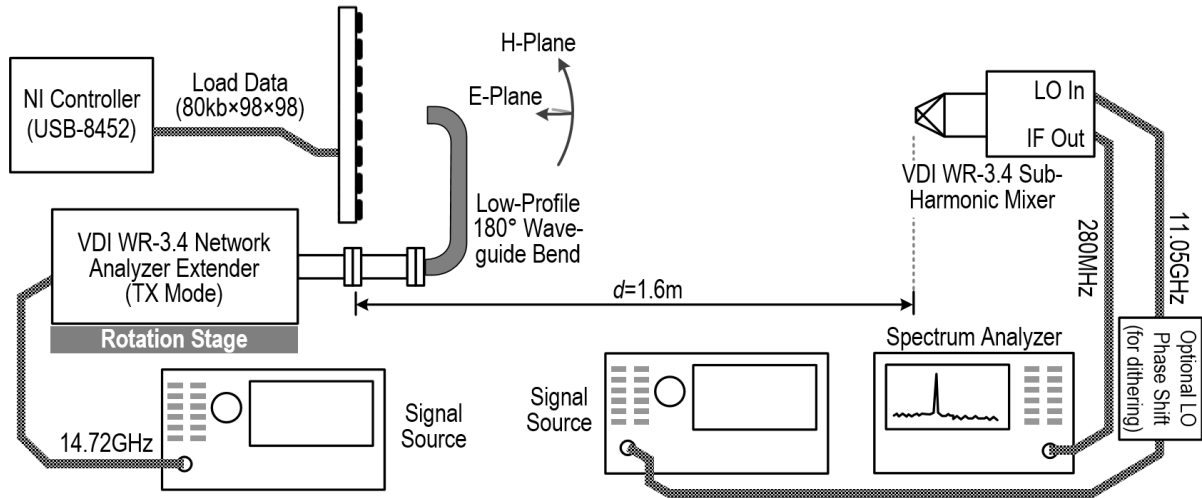
Figure 3-20. Block diagram of RF components in radiation pattern measurement test setup.
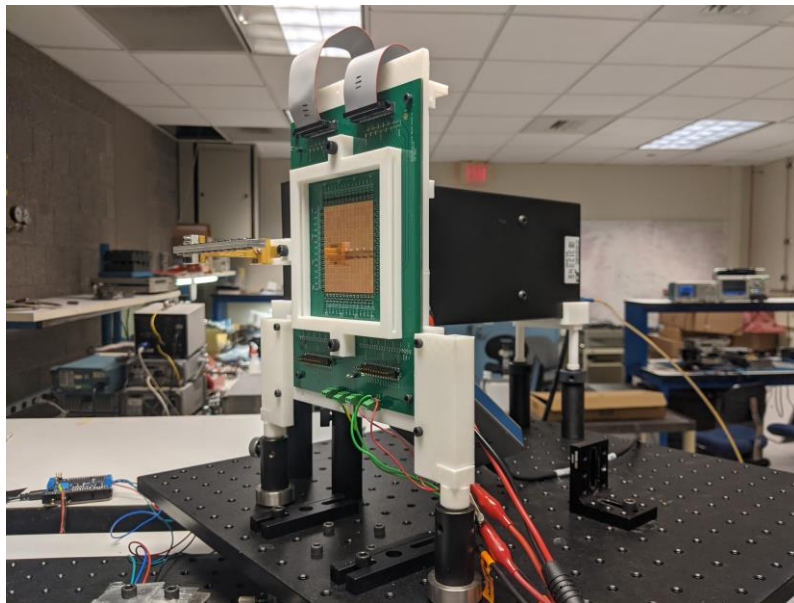
Figure 3-21. Photo of fixture for reflectarray H-plane radiation pattern measurement.
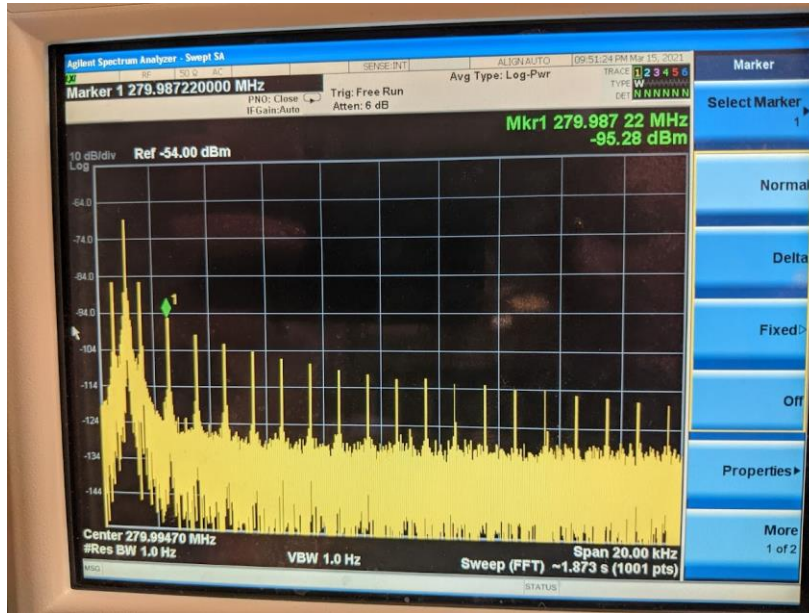
Figure 3-22. Representative output spectrum of reflectarray radiation pattern with 3KHz BPSK modulation.

geometry with the THz source and feed structure. As seen in Figure 3-21, a separate 3D printed test fixture allows the entire array, THz source and feed structure to be rotated by 90 degrees to allow for measurement of both E-plane and H-plane cuts of the radiation pattern.

A block diagram of the RF portion of the measurement setup can be seen in Figure 3-20. A VDI VNAX-729 WR-3.4 Frequency Extender is fed by an external RF source, as controlled by a host PC over GPIB. The frequency extender applies a frequency multiplication ratio of 18x, resulting in a 265GHz output at -5dBm, fed through the previously described waveguide onto the reflectarray. Reflected energy is received by a VDI WR3.4 sub-harmonic mixer via a 25dBi horn antenna. The receive antenna is placed in the opposite polarity of the feed antenna, consistent with the reflectarray's polarization flip. The mixer's local oscillator is fed by an external RF source through a frequency multiplier ratio of 24x. The receiver's low-frequency output is fed to a spectrum analyzer, with control signals and results communicated to/from a host PC over GPIB. The frequencies of the Tx and Rx portions are offset to result in an IF frequency of 280MHz, the frequency in which the receiver has the

68
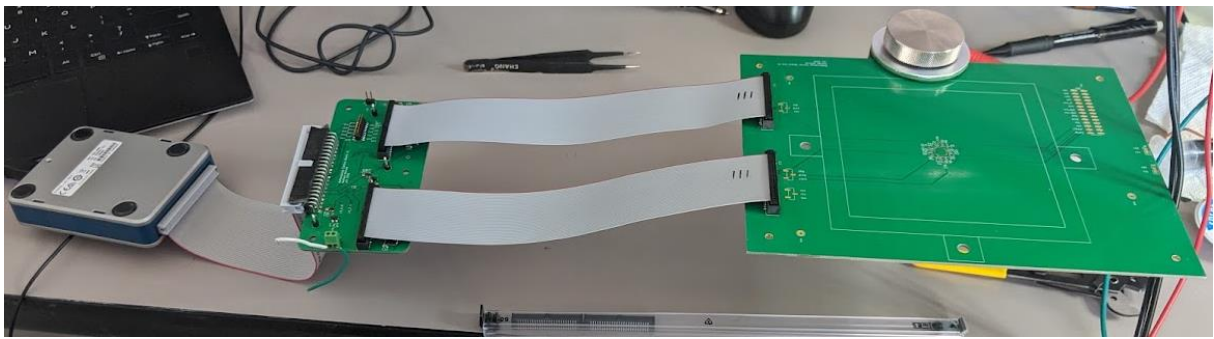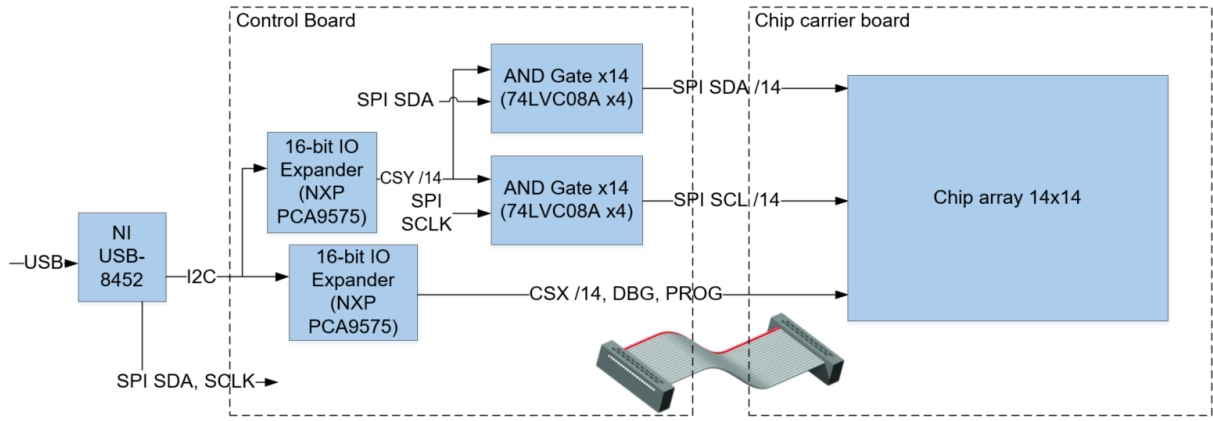
Figure 3-23. (Top) Block diagram of reflectarray signaling and control hardware (Bottom) Realized implementation.

best noise figure and therefore the measurement setup has the highest dynamic range.

Consistent with typical reflectarray designs, the reflectarray has a less-than-unity aperture efficiency and therefore there is nonzero energy radiated from the feed antenna which reflects off passive structures surrounding the reflectarray itself. While these reflections are of the orthogonal linear polarity of the receive antenna, due to the receive antenna's finite cross-polarization response this unwanted energy appears in the receive signal, contaminating results and reducing dynamic range. This is exacerbated in the presently described reflectarray due to the losses in the beamformed path, as described previously. Therefore, to overcome this, the radiation pattern of the reflectarray is modulated, separating in frequency the response of the reflectarray from that of the undesired (and unmodulated) reflections from the surrounding structures. During testing, for a given beam direction, the quantized

phases are calculated and the programmed phases are alternated between their original state and the inverse of this state, where 0 degree antennas become 180 degree antennas and vice versa. This BPSK-like modulation preserves the magnitude of the radiation pattern in all directions while applying a square-wave phase modulation in all directions. The resulting spectrum analyzer response resembles the center IF frequency, caused by undesired reflections, plus modulation peaks at odd harmonics of the reflectarray modulation frequency, consistent with square wave modulation. A representative result of this can be seen in Figure 3-22, as seen at the spectrum analyzer output.

A block diagram depicting the reflectarray control and signaling scheme can be seen in Figure 3-23, along with realized hardware implementation. A USB interface (USB-8452, National Instruments, Austin TX) interprets commands from a host PC over USB and generates signals which feed into a custom printed circuit board with circuits to translate the signals into the [CSx, PROG, DBG, CLKx, DATx] signals required to control the chip array. IDC cables connect the control board with the printed circuit board containing the reflectarray itself. A custom-built MATLAB API automates the generation of quantized phases from a behavioral model and the loading of these phases onto the reflectarray's local memory. During radiation pattern measurement, the control circuit board is mounted to a 3D printed fixture on the back side of the reflectarray.

3.7. Array Calibration

For reasons that are yet to be determined, initial radiation pattern measurements of the reflectarray revealed a mainlobe gain reduction of approximately 15dB compared to what was predicted by analytical and numerical models, while maintaining the mainlobe beamwidth and direction that was expected. Figure 3-24 shows a representative measurement of initial radiation pattern prior to any calibration efforts, where quantized phases were calculated based on traditional reflectarray techniques, using feed geometry and array geometry. Normalization in this Figure causes the sidelobes to appear as being higher than expected when in reality it is the

E-plane radiation pattern
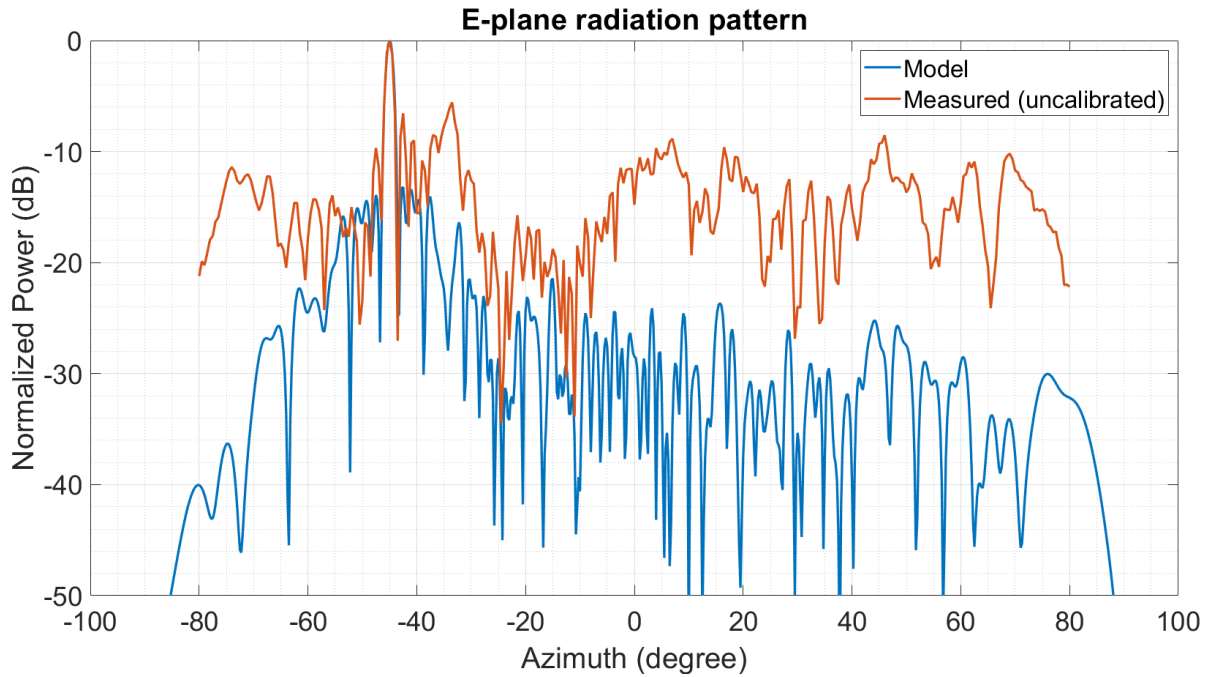
Figure 3-24. Measured radiation pattern depicting suboptimal sidelobes, prior to array calibration. Note: the above data is depicted on an early array prototype with missing data for rows 6, 11, and 14, resulting in increased close-in sidelobes in modeled results, which do not exist in final measurement data in future sections.

mainlobe which is experiencing reduced gain. Empirical evidence presented later in this section revealed that the source of this discrepancy was not a random term arising from array fabrication, but a systematic discrepancy in phases between the reflectarray's phase model and the physical hardware. Therefore, while the procedure to correct this is termed a calibration, it is more accurately described as a method to optimize mainlobe gain and in the process reveal missing phase terms to be used when calculating quantized phases. The calibration procedure is performed once. This section describes the calibration procedure.

To determine the source of the gain discrepancy, the array phases were set and testbench rotated such that the mainlobe points directly toward the receiver. The array's chips were enabled one at a time, while measuring received THz power, to generate a "heat map" describing each chip's contribution to mainlobe power. A representative such heat map can be seen in Figure 3-25. While a few decibels of reduced power is expected at the edges of the array due to feed amplitude taper, to

71
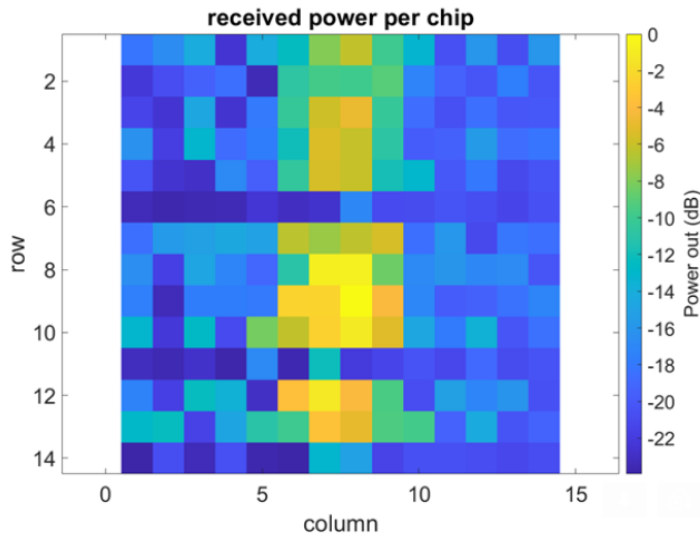
Figure 3-25. Measured heat map depicting each chip's contribution to mainlobe power for uncalibrated array. Note: the above data is depicted on an early array prototype with missing data for rows 6, 11, and 14.

first order approximation the heatmap should be fairly constant across the aperture. The results of this measurement are revealing about the nature of the missing phase term. The shape describes an effective aperture as a vertical column approximately four chips wide, where the long dimension aligns with the axis of cut. The aperture's effective length in this axis is as expected, explaining the 1 degree beamwidth agreeing with models. The reduced aperture width in the opposite axis of approximately four chips (28 antennas), causes a mainlobe gain reduction of $(4/14)^2$, equal to 11dB, consistent with measured results. Furthermore, the column-like shape apparent in Figure 3-25, where the column is aligned with the center of the array and tapers off towards the edges, provides evidence that a missing phase term exists which is aligned with the horizontal axis of chips, and assumes an even function shape which is smooth; it varies slowly over the scale of one chip (seven antennas) and likely has no discontinuities.

Based on the above evidence, a procedure was developed to determine experimentally the shape and value of the missing phase term. The procedure is similar to and was inspired by Finite Element Analysis, where complex shapes are discretized into linear elements in a process termed meshing. A similar procedure is adopted here to

72
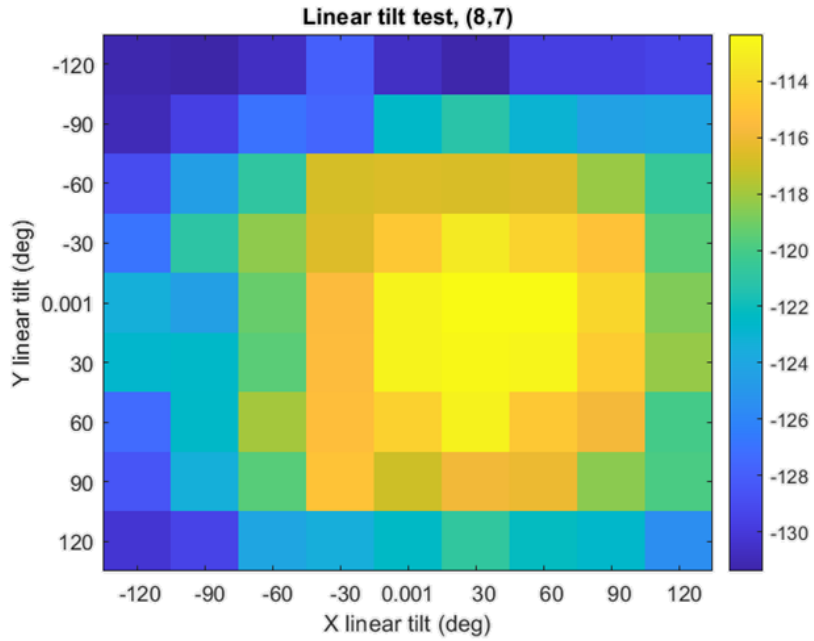
Figure 3-26. Representative measured chip power output as a function of linear tilt terms C_x and C_y during the calibration procedure for the (8,7) chip.

determine the shape and value of the missing phase term in the array's phase calculation. This procedure is applied one chip at a time. In this procedure, the phases for the chip's 49 antennas are calculated to point it's reflected beam at the receiver, and that chip's contribution to mainlobe power is measured. Subsequently, the chip's phases are recalculated, while adding an additional phase matrix C to the phases before quantizing. The matrix C applies an additional phase term which has linear components in X and Y over the scale of that chip's antennas, the slopes of which are termed C_x and C_y. Therefore, the calibration matrix C for each chip's antennas, is equal to

$$C = C_x * \begin{bmatrix} 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \end{bmatrix} [-3 -2 -1\ 0\ 1\ 2\ 3] + C_y * \begin{bmatrix} -3 \\ -2 \\ -1 \\ 0 \\ 1 \\ 2 \\ 3 \end{bmatrix} [1\ 1\ 1\ 1\ 1\ 1\ 1] \qquad (3.1)$$

73
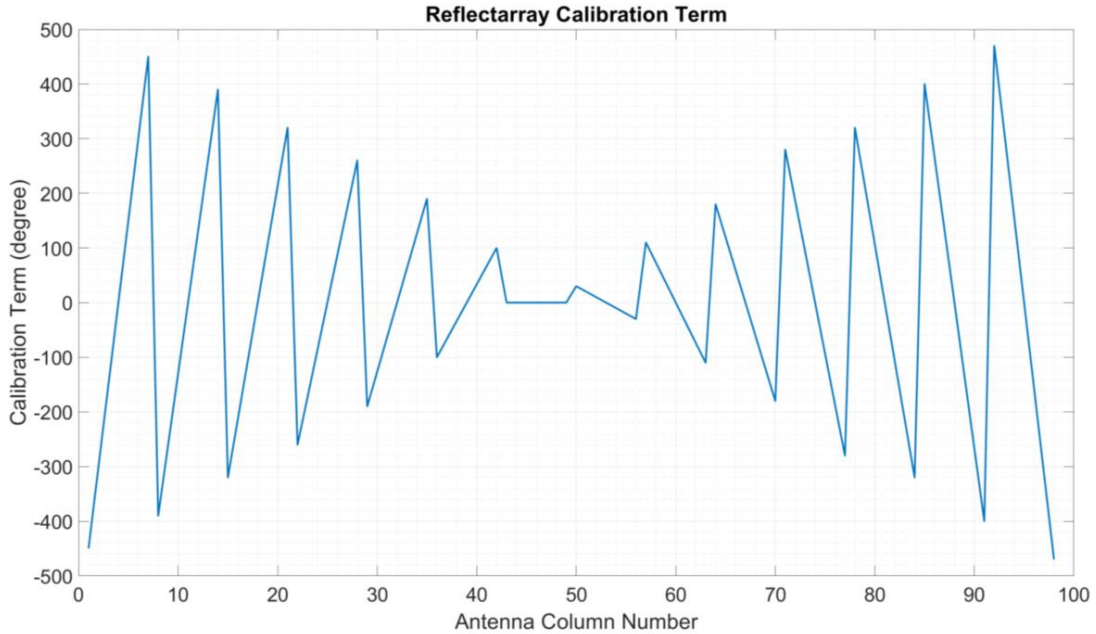
Figure 3-27. Variation of phase calibration term C as a function of antenna column in the array, arising from chip-level linear terms C_x.

The procedure operates iteratively, where the antenna's phases are requantized with the inclusion of the phase matrix C and varying values of C_x and C_y, while measuring received power, until the optimal point is found. Therefore, the procedure is an optimizer which applies a linear tilt in X and Y to each chip's mainlobe to point them at the receiver. An example of the resulting data for a given chip can be seen in Figure 3-26, which shows received power for a given chip as a function of the linear tilt terms C_x and C_y.

By repeating this procedure for all chips and storing the Cx and Cy variables, the matrix C for the entire 98x98 antenna array (of 14x14 chips) can be obtained. Empirical evidence revealed that previous assertions about the shape of the missing phase term were correct: the term only varied by horizontal location (C_y always equals zero), C_x is constant for chips within a given column and is symmetric about the center column of the array. Therefore, it was only necessary to perform the above procedure on seven chips, with the above simplifications allowing the values to be calculated for the rest of the array. Figure 3-27 depicts the phase term's variation over columns of the array, based on values of C_x for each of the 14 chip columns. A

74
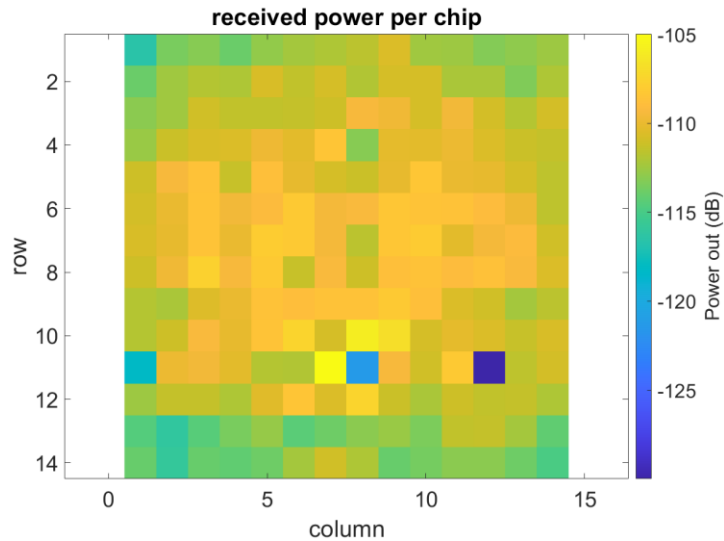
Figure 3-28. Measured heat map depicting each chip's contribution to mainlobe power after applying array calibration term C.

heatmap of the contributions of each chip to mainlobe power after inclusion of the correction term C can be seen in Figure 3-28.

The procedure outlined above optimizes the unknown phase term C on a chip-level linear interpolation to maximize each chip's contribution to mainlobe power, however it does not guarantee that the antennas between chips are in phase with each other. A summation of the power levels measured and shown in Figure 3-28 results in a received power consistent with the gain levels predicted by the original numerical models, however to achieve this in the experimental array a second calibration step was needed. It was determined experimentally that subsequent to the above procedure, all 14 chips in a given column were indeed mutually in phase; a total column's power contribution to the mainlobe was equal to the sum of each chip's contribution, however this was found empirically to not be the case between columns. The secondary calibration procedure chooses a column as the reference column and is applied pairwise with each of the remaining chip columns. It applies a "DC" phase term D to a column of chips such that it's antennas operate in phase with those of the reference column. This is achieved when the power received from both columns together equals the power from each column individually. Therefore,

75
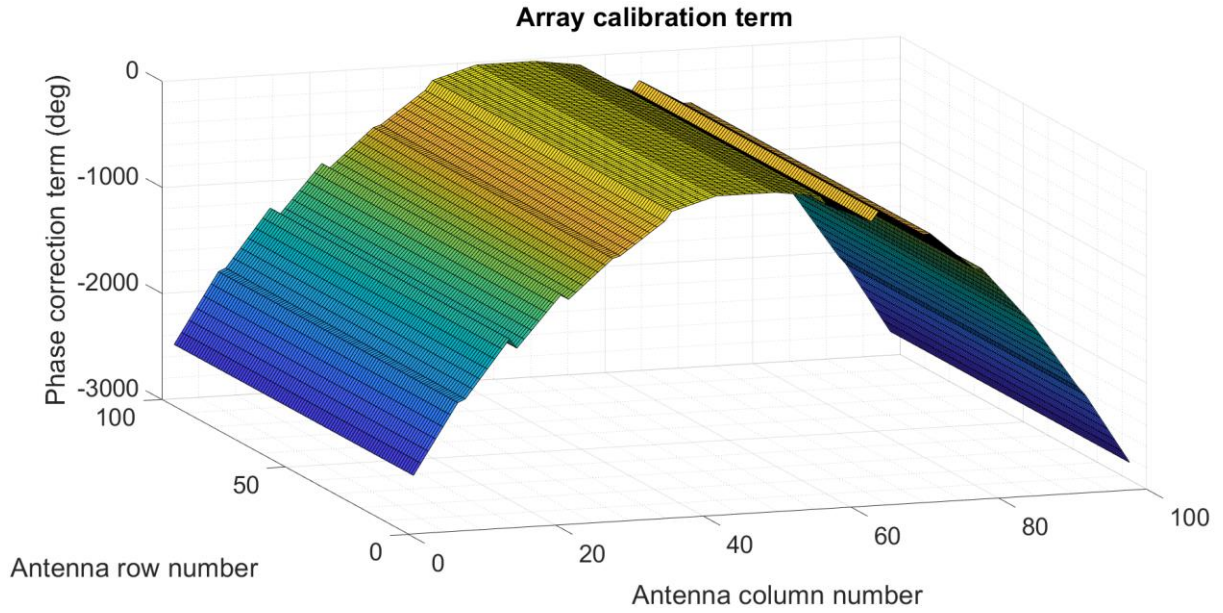
Figure 3-29. Final phase calibration term arising from phase calibration matrices C + D.

this secondary calibration step is also an optimizer which optimizes for maximum mainlobe gain. The resulting final phase calibration term E is equal to

$$E = C + D \qquad (3.2)$$

The values of this matrix E can be seen in Figure 3-29.

The above procedure was used to calibrate phases and was used to produce radiation pattern measurements presented in Section 3.8. It was found experimentally that a single set of phase calibration values applies to all radiation pattern measurements in the E-plane, regardless of beam steering angle. However, it was found experimentally that the calibration value changes based on intended beam steering angle in the H-plane. In addition, despite calibration H-plane measurements exhibited periodic coherent sidelobes, shown in Section 3.8. These sidelobes are consistent with a periodic phase error on the scale of one chip, which is likely due to the linear approximation of what is likely a smooth phase function, and the resulting periodicity in phase error. This also manifests as vertically-aligned points in imager Point Spread Function measurements shown in Chapter 6. Regardless, the

calibration scheme is effective at achieving mainlobe performance as predicted by array numerical models and analytical models.

While the term "calibration" is used in these descriptions, the above procedure more accurately derives a missing phase term in the array model by optimizing for mainlobe gain. The calibration term is time-invariant and only needs to be performed once for a given array configuration. In future iterations of this work, when the source of the missing term is identified, it can be included in phase calculations such that this calibration step is no longer necessary.

While the physical reason for the missing phase term is not known, there exists evidence as to it's cause. The fact that the procedure varies with feed geometry and with H-plane mainlobe location suggests that the missing term is related to array geometry. In addition, the magnitude of the term is extremely similar to twice the X-varying component of the phase term arising from the feed antenna geometry. In addition, perturbations from bondwires, surface wave scattering in feed aperture, placement errors in chip X location, PCB thermal expansion, patch antenna near-field coupling, phase response in feed antenna and/or on-chip patch antennas, and array non-flatness in Z were considered as potential explanations. Regardless of the
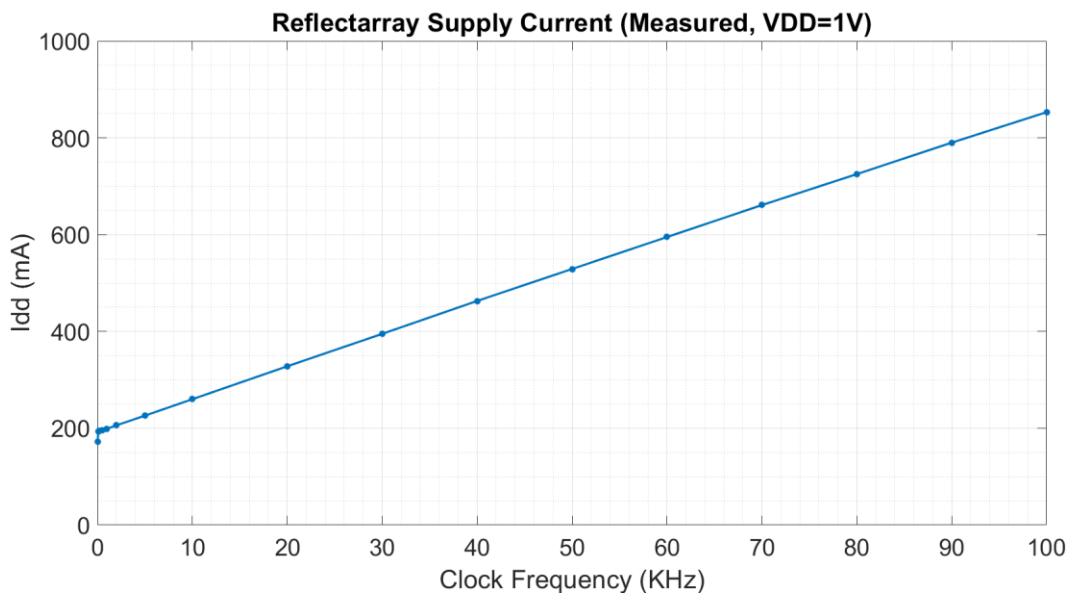
Figure 3-30. Reflectarray measured VDD current (VDD=1V) versus shift register clock frequency.

cause, this procedure proves that the phase term can be compensated for in a one-time optimzation with negligible loss of performance.

3.8. Measurement Results

This section presents measurement results of reflectarray performance, and their comparison to behavioral models.

The array was measured to have a static DC power consumption of 140 mA at VDD=1V, resulting from leakage in the shift register array. This results in an average leakage current of 0.7mA in each of the 196 chips, consistent with simulations. During reflectarray operation, the beam is switched to a new state with a master clock which cycles each antenna's ring buffer, with all acting in parallel. The average power consumed during such an operation is 6.6 mA/KHz. The measured VDD current consumption as a function of clock frequency can be seen in Figure 3-30. The VDD current arises nearly exclusively from leakage and switching current of the shift registers used in memory storage. As discussed previously, the one-bit phase shifters consume no DC current. Future implementations employing
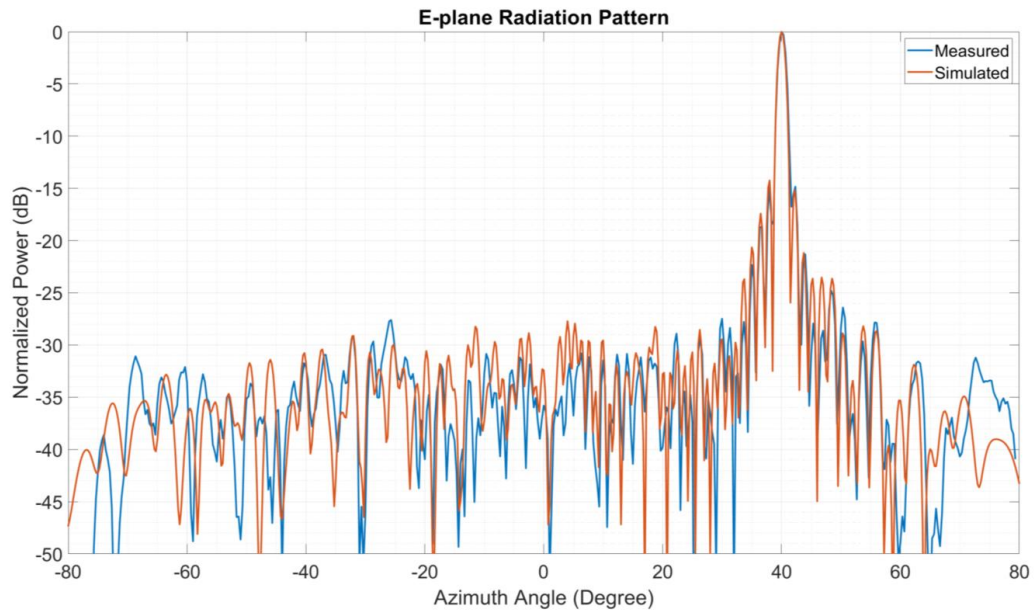
Figure 3-31. Measured and modeled E-plane cuts of reflectarray radiation pattern at 265GHz.

78

static RAM in place of shift register memory could be expected to exhibit orders of magnitude less leakage and dynamic current, while also improving memory density. Maximum clock frequency was not measured experimentally due to limited number of prototypes and risk of damage; it is expected to be limited in this implementation by bond wire current handling capacity.
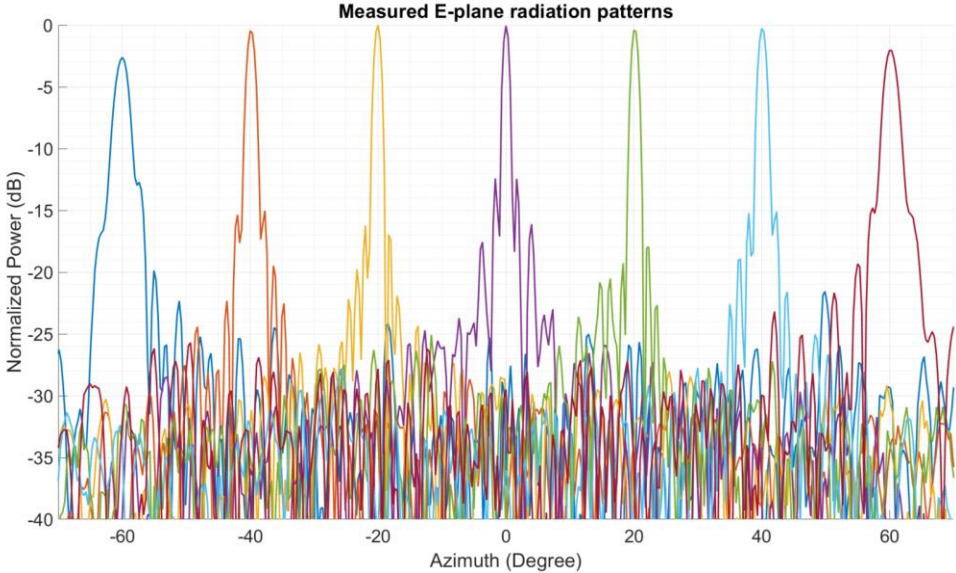
Figure 3-32. Measured E-plane cuts of reflectarray radiation pattern at 265GHz over a range of [-60 60] degrees.
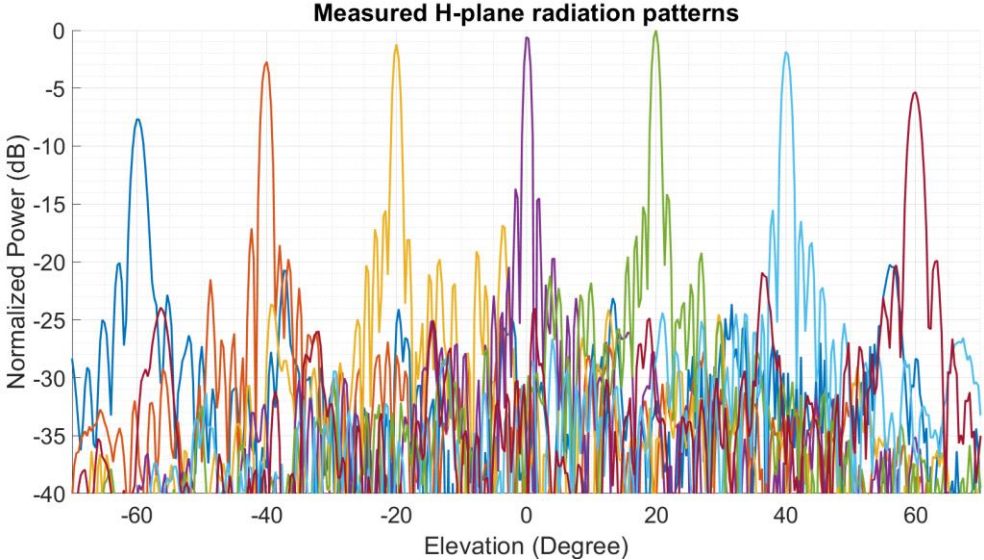
Figure 3-33. Measured H-plane cuts of reflectarray radiation pattern at 265GHz over a range of [-60 60] degrees.
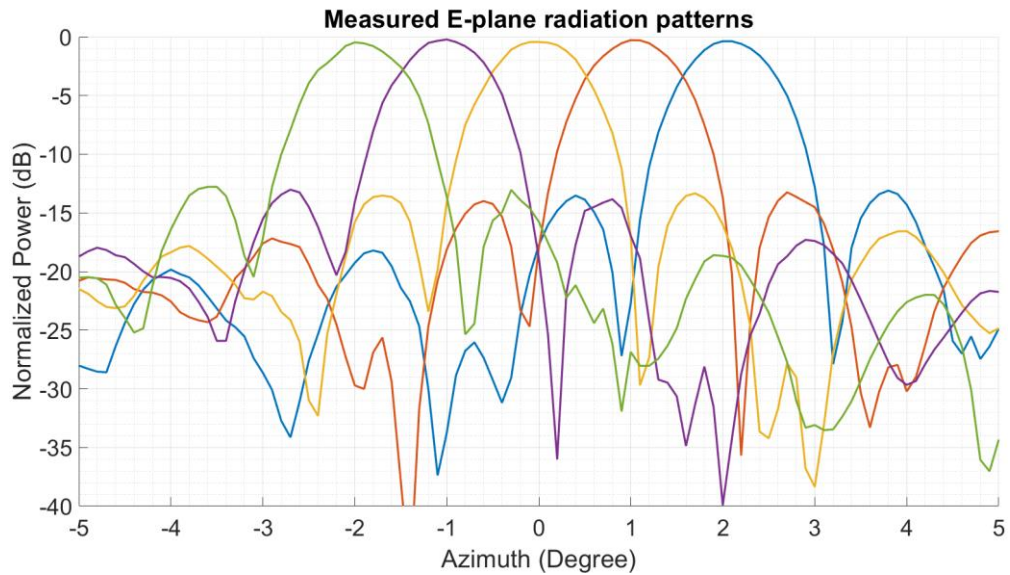
Figure 3-34. Measured E-plane cuts of reflectarray radiation pattern at 265GHz over a range of [-2 -1 0 1 2] degrees.

A measured representative E-plane radiation pattern at 265GHz is shown in Figure 3-31, with comparison to analytical model predictions. The radiation pattern exhibits a quantization noise floor of approximately 32dB below the mainlobe in this case. Discrepancies between the model and measured patterns are explained by miniscule alignment errors in test setup, imperfect modeling of amplitude taper arising from feedhorn radiation pattern and alignment, imperfect calibration and the omission of feedhorn blockage in the analytical model. In this measurement and all measured results, the shape of the close-in sidelobes and width of the mainlobe are determined by the amount of amplitude taper in the array's aperture, resulting from the feed. The relatively low taper in this implementation, as described in previous sections, leads to narrow mainlobe and higher close-in sidelobes than more typical edge amplitude tapers of 10dB. This is easily improved in future iterations, while also improving aperture efficiency.

Figures 3-32 and 3-33, respectively, depict radiation pattern measurements in E-plane and H-plane cuts over a range of [-60 60] degrees. The measured radiation pattern is consistent with model predictions and demonstrates a peak directivity of 42dBi and 3dB beamwidth of 1 degree at boresight. Beamwidth and directivity

80

	Freq. (GHz)	Beam Forming Approach	Array Size	3dB Beam-width	Steering Range	Automatic Beam Profile Correction?	Technology	Area	Power Consumption	3D Sensing Demo?
ISSCC 2021[132]	380	Active-Driven Beam Squint Antenna	2x1	~15° [1]	±40°	No	65nm CMOS	3mm²	0.14W (TX) 0.16 (RX)	NA
ISSCC 2021[131]	450	Active Reconfigurable Array+Si Lens	3x7	~7° [2]	±28° & ±8°	No	65nm CMOS	4mm²	0.051~0.095W	
SPIE 2019 [41]	235	Reflect Array (Tiled GaN Chips)	32x32 [3]	~3°	> ±40°	No	GaN + Silicon Micromachining	31mm² (Chip) 500mm² (Array)	NA	
Nat. E. 2020 [40]	300	Transmit Array (Tiled CMOS Chips)	24x24	~10° [4]	±30°	No	65nm CMOS	4mm² (Chip) 16mm² (Array)	0.025W [5] (f_{clk}=5GHz)	
This Work [123]	260	Reflect Array [6] (Tiled CMOS Chips)	98x98	1°	> ±60°	Yes	22nm CMOS	16mm² (Chip) 3100mm² (Array)	0.85W [7] (f_{clk}=100kHz)	Yes

(1) Achieved only in one dimension.   (2) Achieved through a Si lens (R=5mm).   (3) ~50% of array units not functioning
(4) Estimated from the simulated value   (5) Dynamic power driving phase shifter switches.   (6) The only all-inclusive solution requiring no external data
      control during beam scanning   (7) Dynamic power driving 98x98x2 phase shifter switches and 780Mb built-in cyclic memory

Table 3-2. Performance comparison of THz antenna arrays.

degrade at higher angles, consistent with typical antenna arrays. If used in a monostatic FMCW radar application, the reciprocity of the phase shifters and reflectarray can be used to produce an imaging radar with Tx and Rx patterns which are collocated by design. This would result in an effective directivity which is double the value measured in this one-way radiation pattern measurement.

In an imaging radar application, the antenna array is used to steer a narrow beam and take a distance sample over the size of that beam, and subsequently sweep the beam across a scene in a rasterized manner to create an image. In such a scheme, the effective resolution of the image is limited by the beamwidth. It also requires the capability of stepping the beam across the scene in increments equal to the beamwidth, or 1 degree in this case. Figure 3-34 depicts this capability, with measured results of E-plane radiation pattern at 265GHz demonstrating mainlobe steering at [-2 -1 0 1 2] degrees. Analytical models predict the ability to steer the beam with a much finer precision than 1 degree, however in an imaging radar application with a 1 degree wide beam this would produce redundant information.

Table 3-2 shows a comparison of this work's reflectarray with other works from academic literature [40], [41], [123], [131], [132].

Chapter 4

Design of THz Phased Array Radar

This section describes the one bit THz phased array radar. The radar applies the concepts from the previously described THz reflectarray with enhancements to yield a system with the benefits of the reflectarray's sidelobe suppression without the reflectarray's complexities and system volume. In addition, an integrated THz transceiver allows for a compact and highly integrated system.

4.1. Overview

The phased array radar is designed as a tiling of CMOS chips, each containing a 6x2 element phased array operating at a center frequency of 265GHz. Similar to the previously described reflectarray, the phased array radar employs one-bit phase shifters implemented as two MOSFET switches, directing the RF feed to opposing sides of a patch antenna. Peak sidelobe suppression, achieved in the reflectarray structure by spherical wavefront feed and resulting breaking of periodicity in phase quantization error, is instead achieved in this case by random, fixed phase offsets applied to each antenna. This is implemented as transmission lines of random length inserted in the feed of each of the 12 antennas. These transmission lines of random length are hard-coded at design time and offer the same benefit as the reflectarray's spherical wavefront, without the geometric requirement and losses associated with the spatial feed. The phased array generates 265GHz RF energy via frequency multipliers from an off-chip feed of 28GHz. Each antenna incorporates a single transistor mixer, which mixes the outgoing FMCW signal (doubling as the LO) with

a delayed echo signal to produce an IF signal. An analog path consisting of low-frequency Low Noise Amplifiers, baseband one-bit baseband phase shifters and power combiners allow the Rx beam to be steered independently of the Tx beam. Shift registers provide local memory for each antenna for storage of a single beam state, with one bit each for Tx phase shifter, Rx phase shifter, plus one "off bit", providing the functionality to turn an antenna off for calibration purposes. The chip is designed to be tiled to create a large array so the array can be scaled in size to meet variable performance requirements. Additional phase randomization is provided on the PCB level. The chip is implemented in Intel 22FFL 22nm FinFET technology, occupying an area of 2 x 4 mm^2. To the authors knowledge, this chip represents the first THz band Amplifier Multiplier Chain and first THz band transceiver to date in the 22FFL process.

4.2 Design of THz Generation Path

The THz generation path is designed to take as input a low-frequency 28GHz signal from external off chip sources and produce 265GHz output for use by the radar. This
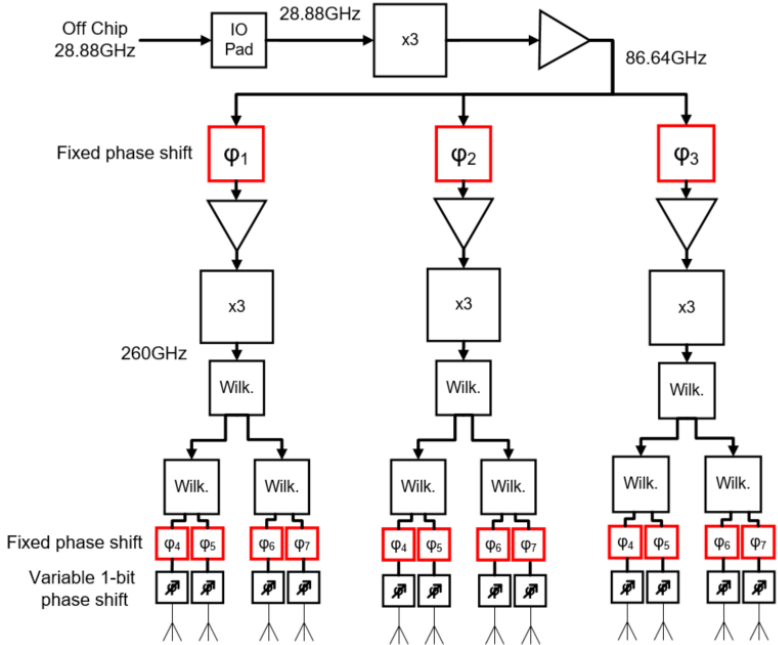
Figure 4-1. One-bit phased array THz generation path.
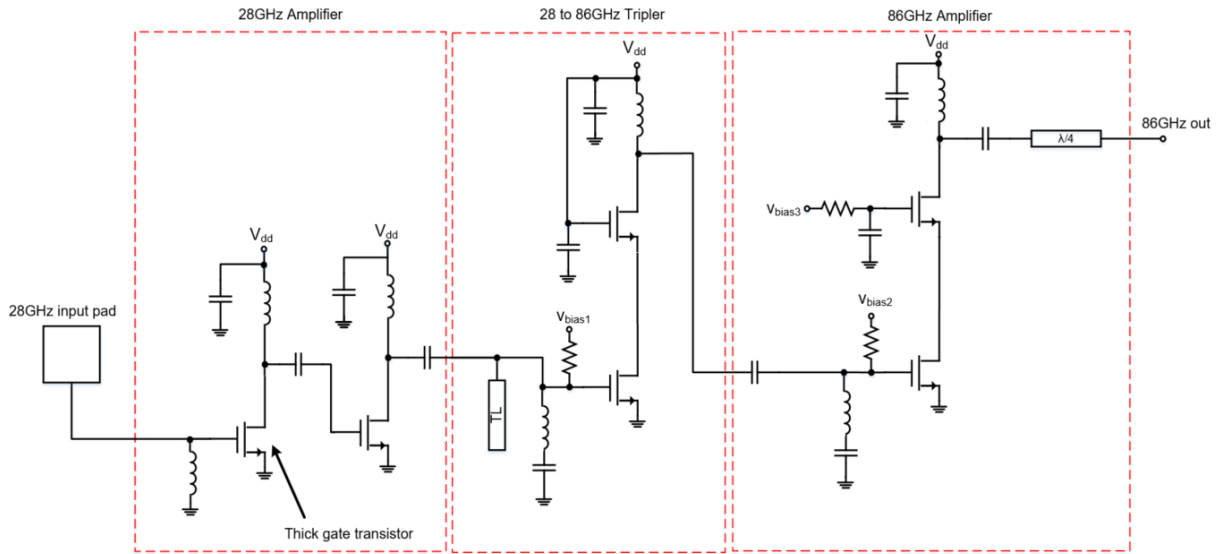
Figure 4-2. Circuit schematic of THz generation path's input stage and 86GHz tripler and amplifier.

is achieved through an Amplifier-Multiplier Chain (AMC), as seen in Figure 4-1, a block diagram of the THz generation path.

The Amplifier-Multiplier Chain is a conventional design consisting of Common Source amplifiers and frequency multipliers for each stage, some with Cascode configuration. A schematic of the 28GHz input stage, 28GHz to 86GHz frequency tripler, and 86GHz amplifier can be seen in Figure 4-2. The 28GHz input stage consists of a thick gate Common Source amplifier for ESD robustness, followed by thin-gate Common Source amplifier for gain, and is modeled to output -1.4 dBm of power at -5 dBm of input power. The 28 to 86GHz tripler is a Cascode configuration, with a harmonic reflector at the input. It is modeled to output -13.6 dBm of 86GHz for a given -1.4 dBm of 28GHz input power. The 86GHz amplifier is a Cascode configuration, producing -3.5 dBm of output power for -13.6 dBm of input power. The output of the 86GHz amplifier is split to three using a T-junction splitter, followed by transmission lines to each of the three groups of four antennas. These transmission lines are set to be of random length, as determined by numerical simulation to maximize disruption of periodicity in phase error and therefore
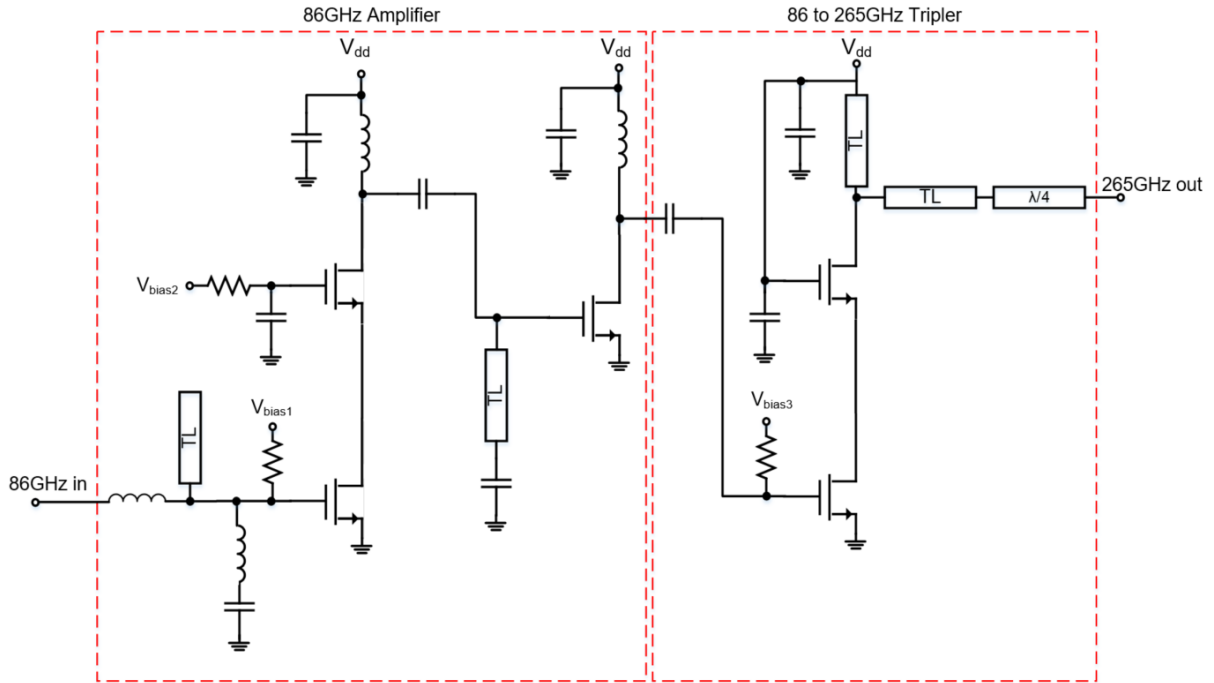
Figure 4-3. Circuit schematic of THz generation path's second half, consisting of 86GHz amplifier and 265GHz tripler.

minimize sidelobes. The lengths of the three transmission lines are matched to within 180 degrees to minimize unequal losses and therefore periodicity in amplitude in a tiled array of chips, which would degrade radiation patterns.

There exists significant signal loss in the 1 to 3 T-junction splitter plus ~1.5mm of transmission line to distribute the 86GHz signal to each group of four antennas. Therefore, a second 86GHz amplifier, identical to the first, precedes the final 86-265GHz frequency tripler. Each of the three groups of four antennas contains identical circuitry consisting of this second 86GHz amplifier followed by the 86-265GHz frequency tripler. A schematic of the final portion of the THz generation path containing these two blocks can be seen in Figure 4-3. The output power of each of the three secondary 86GHz amplifiers is -2.5 dBm. A common source 86GHz power amplifier is used to increase voltage swing on the gate of the final stage, an 86-265GHz frequency tripler. Using a Cascode configuration, each of the 265GHz
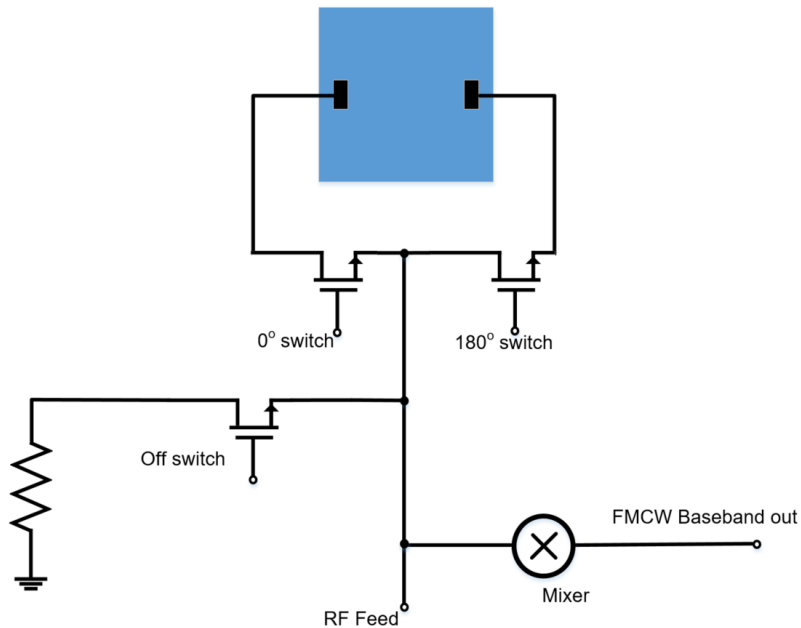
Figure 4-4. Schematic depiction of antenna element, including one-bit phase shifter, off switch and mixer.

frequency triplers outputs -12.6 dBm of 265GHz power. The three 86-265GHz triplers on the chip outputs a combined modeled power of -7.8 dBm at 265GHz.

A significant challenge exists in the design of high power THz sources, as described by the THz gap discussed previously. At more advanced process nodes such as the 22nm FinFET process used here, the F_t and F_{max} of transistors improves, decreasing losses of frequency multipliers and allowing for positive gain at higher frequencies. However, challenges increase in mitigating increased interconnect losses at more advanced nodes. In addition, reduction in supply voltages (VDD=1V in this process) reduce headroom and allowable voltage swing. Given the relative lack of experience in this process, a conservative design decision was made to constrain circuit design to never exceed DC+RF voltage of 1.2V due to uncertainties in breakdown voltages and device reliability. As a result, suboptimal amplifier performance is attained and gate voltage swings are limited in frequency multiplier stages, reducing nonlinear operation and increasing frequency multiplier conversion loss. It is quite likely that

86
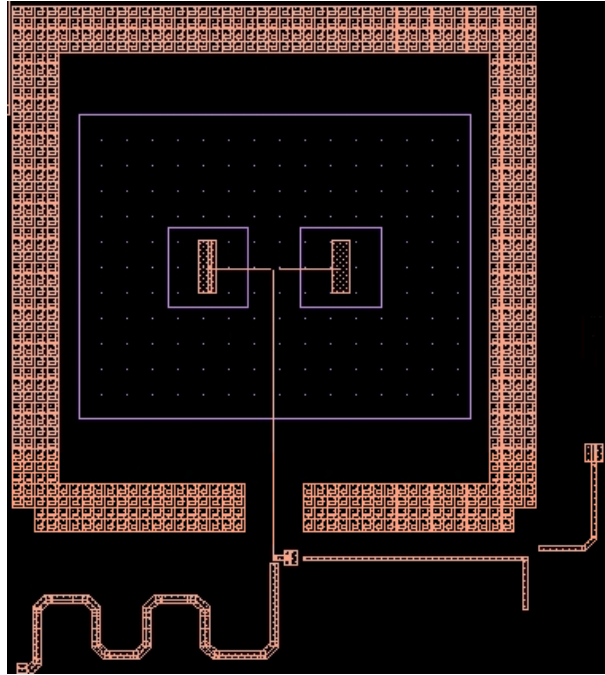
Figure 4-5. Actual realized implementation of antenna element.

with more silicon learnings and more aggressive designs, higher THz power levels can be achieved over this design.

Following a quarter wave transformer, the output of the 265GHz tripler is divided into four outputs by a series of Wilkinson dividers, followed by transmission line feed to each of the 12 antennas, with lengths randomized by numerical optimization for minimum sidelobe level.

4.3. Design of Antenna Element

The antenna element is similar to that described in the reflectarray. A schematic depiction of the antenna element can be seen in Figure 4-4, with actual realized implementation in Figure 4-5. Based on a similar one-bit phase shifter architecture, the antenna element uses two MOSFET switches to route THz energy to either side of a patch antenna implemented in the C4 layer. A single bit shift register stores phase setting as commanded by the SPI interface.

Due to the geometries and material properties involved, there is significant coupling from the antenna's feed line and the C4 patch antenna, producing significant radiation in the opposite polarity from that intended. This effect was anticipated and attempted to be mitigated by reduction of the patch antenna's dimension in the off-polarity to shift its resonance significantly out of the frequency range used in this system.

Unlike the case of the one bit reflectarray described in Chapter 3, the antenna element incorporates an additional third switch, implementing the ability to "turn off" an antenna, as commanded by a second bit in the antenna's shift register storage. When asserted, digital logic results in the two phase shifter transistors being turned off, and the "off switch" to be turned on, dissipating incident energy through the switch such that no energy is radiated by the antenna. The switch is sized to provide
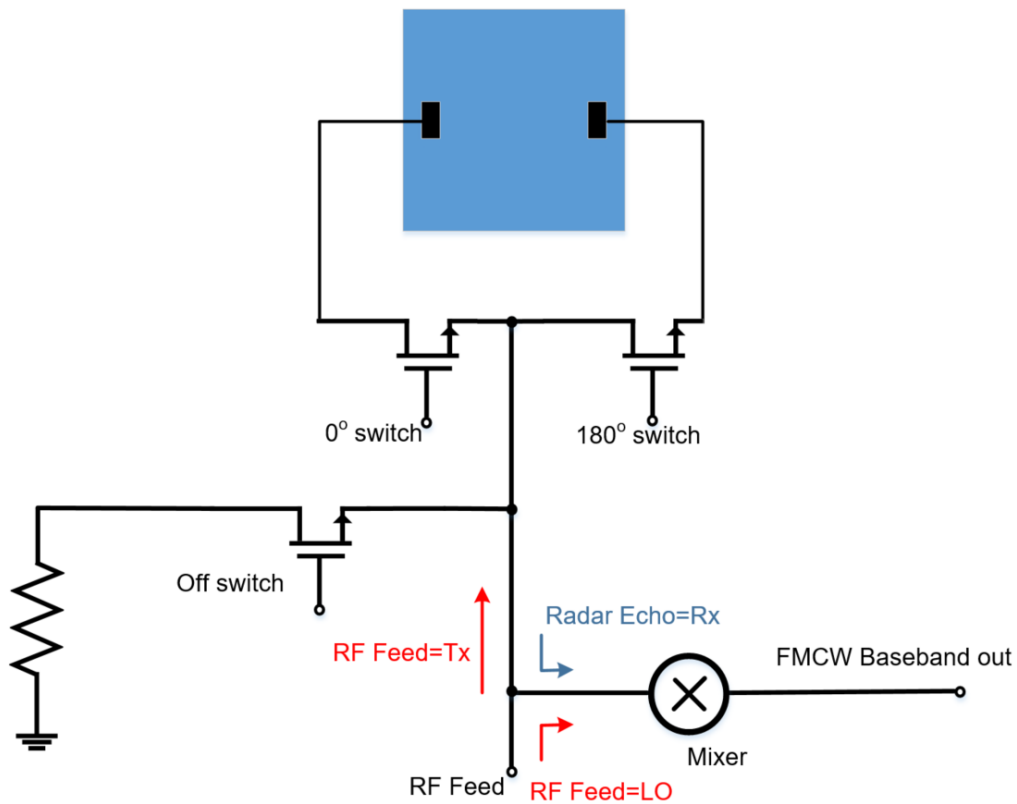
Figure 4-6. Equal splitting of RF feed signal to serve as mixer LO and radiated power source. A portion of the echo signals from the antenna is received by the mixer to produce a low-frequency radar output signal.

a matched load. This feature allows individual antennas to be turned on for calibration of antenna magnitude and phase. Including the 1bit phase shifter's 3dB of insertion loss, the antenna is modeled to have an overall gain of -2dB.

As will be discussed in future sections, the antenna additionally serves as a receiving antenna, receiving radar echo signals to be fed to the receiving mixer. Such received signals experience the same phase shift as the transmitted signals due to the reciprocal nature of the phase shifter. However, based on the assumption that the received radar echo is a plane wave signal, the effective receiver radiation pattern does not necessarily point in the same direction as the transmitter's radiation pattern. This is further complicated by the fixed transmission line phase shifters to each antenna, which phase shifts not only the transmitted energy to each antenna but also the LO to each antenna's receiver. Therefore, an additional degree of freedom in phase is needed to ensure the receiver's response pattern is pointed in the same direction as the transmitter's. This is achieved by a baseband phase shifter, as discussed in future sections.
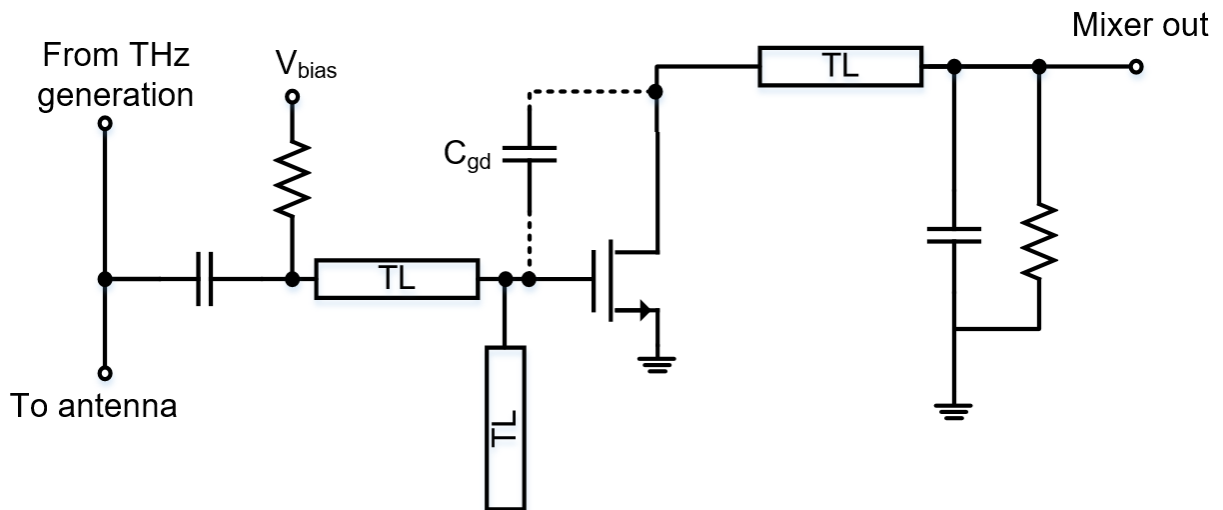
Figure 4-7. Circuit-level schematic depicting design of the radar transceiver's mixer.

4.4. Design of THz Mixer

The Terahertz Mixer serves as the receiver for the Terahertz one-bit phased array radar. Placed in a T-junction power divider configuration with the antenna, incident power from the THz generation path is split equally between the antenna and the THz mixer, as seen in Figure 4-6. The portion leading to the antenna serves as the transmit power for the radar, while the portion leading to the THz mixer serves as the LO for the mixer. At the same time, radar echo returns are received by the same antenna, with a portion of the signal feeding to the mixer, as seen in Figure 4-6. A schematic representing the design of the mixer can be seen in Figure 4-7. The mixer is designed as a square law detector, similar to [133]. By using the transistor's inherent nonlinearity, the FMCW LO is mixed with the echo signal to produce a number of frequency components which includes low-frequency IF signal, with a frequency content which represents the range of radar targets. The mixer's principle of operation relies on the capacitance C_{gd}, a parasitic capacitance inherent to the transistor, acting as a coupling between the transistor's gate and drain to produce second order currents, as described in [133]. The FMCW chirp rate is chosen such that IF radar signals are above the frequency range of interest. Therefore, the mixer's
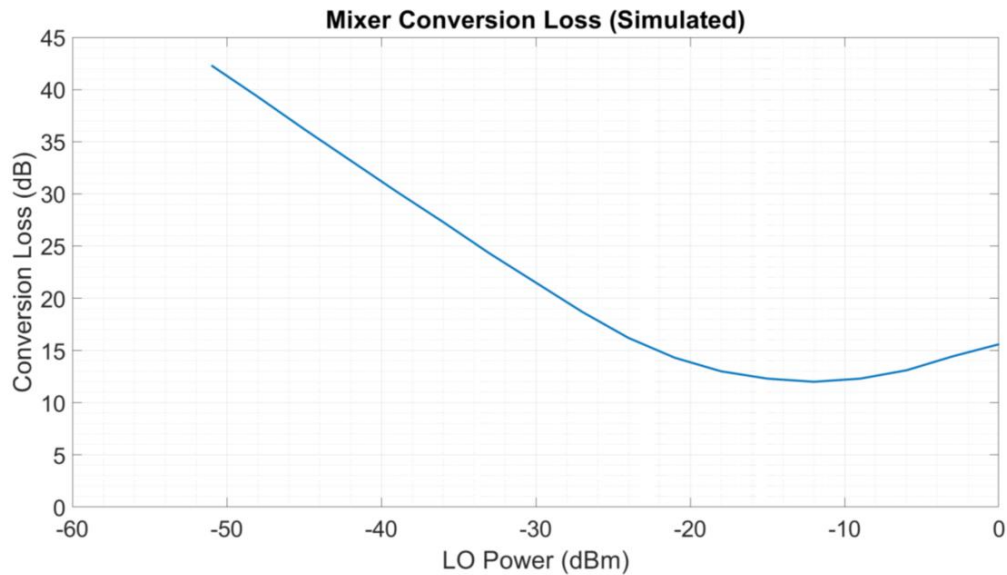
Figure 4-8. Simulated conversion loss vs LO power for the single transistor mixer.

90
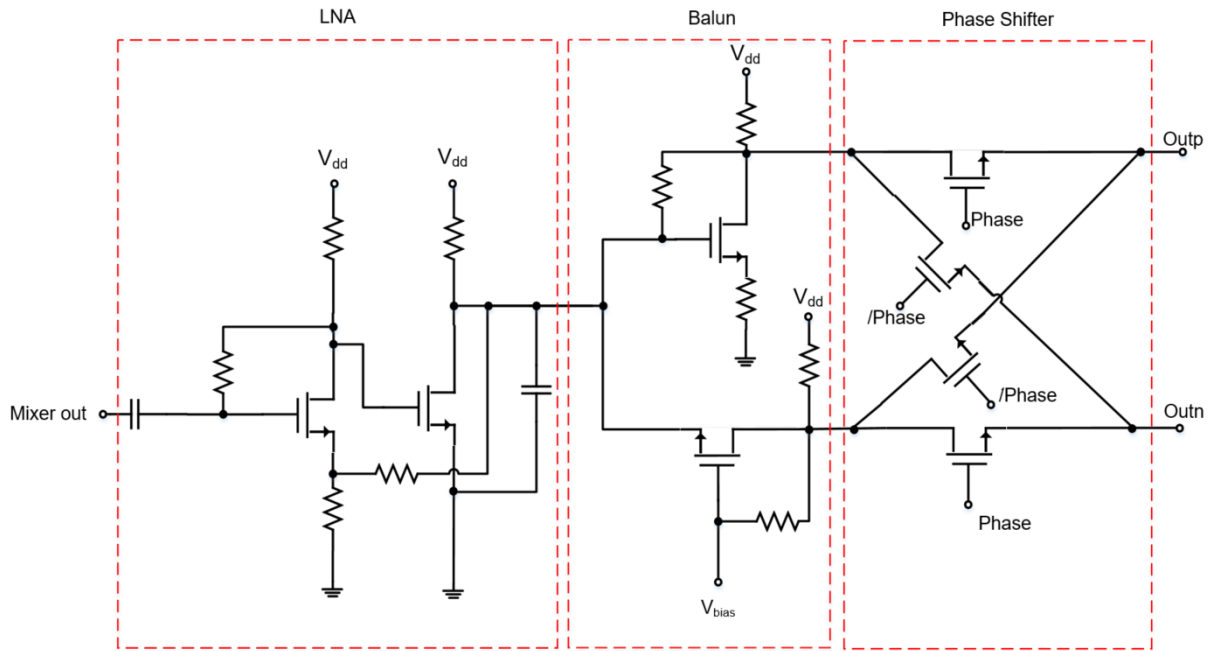
Figure 4-9. Circuit-level schematic depicting design of the radar transceiver's baseband circuits, consisting of High-pass filter, LNA, Low-pass filter, balun, and one-bit phase shifter.

noise figure is equal to its conversion loss, which is modeled to be 20dB. A capacitor on the output of the mixer serves as an RF short, allowing decoupling from subsequent baseband stages.

As is typical of mixing receivers, the mixer's conversion loss is a strong function of LO power. Stronger LO overdrive enhances the second order nonlinear characteristics of the mixer, improving conversion loss. This can be seen in Figure 4-8, a simulation of the relationship between these two values. In this system, the RF feed to each of the 12 antenna + mixer units is simulated to be -27dBm, after power splitting and losses in distribution. In this design, there is an equal splitting of power between the LO and antenna, leaving approximately -30dBm for each. The division of power between these two (and therefore design of according impedances) represents a complex system-level tradeoff between radiated power, mixer conversion loss and the portion of echo power that is coupled into the mixer. As seen in Figure 4-8, in this regime of mixer operation there is a linear relationship between LO power and conversion loss. Therefore, at a system level there is extreme sensitivity in

performance to the total RF power output by the THz generation stage; any reduction in THz power reduces both radiated power and mixer conversion loss, creating a disproportionate effect on IF power and therefore SNR in the final radar solution.

4.5 Design of Baseband Receiver Path

An annotated circuit schematic of the baseband receiver path can be seen in Figure 4-9. The path includes a high-pass filter to eliminate low frequency components arising from flicker noise and additionally eliminate low frequency IF signals arising from the LO mixing with reflections at the phase shifter, antenna or bondwires. Such reflections are of short time delay and therefore produce low frequency components which are potentially of high enough amplitude to saturate subsequent stages.

Following high-pass filtering, a Low Noise Amplifier (LNA) stage provides low-noise gain to the IF signal. As seen in Figure 4-9, the LNA consists of a two-stage common
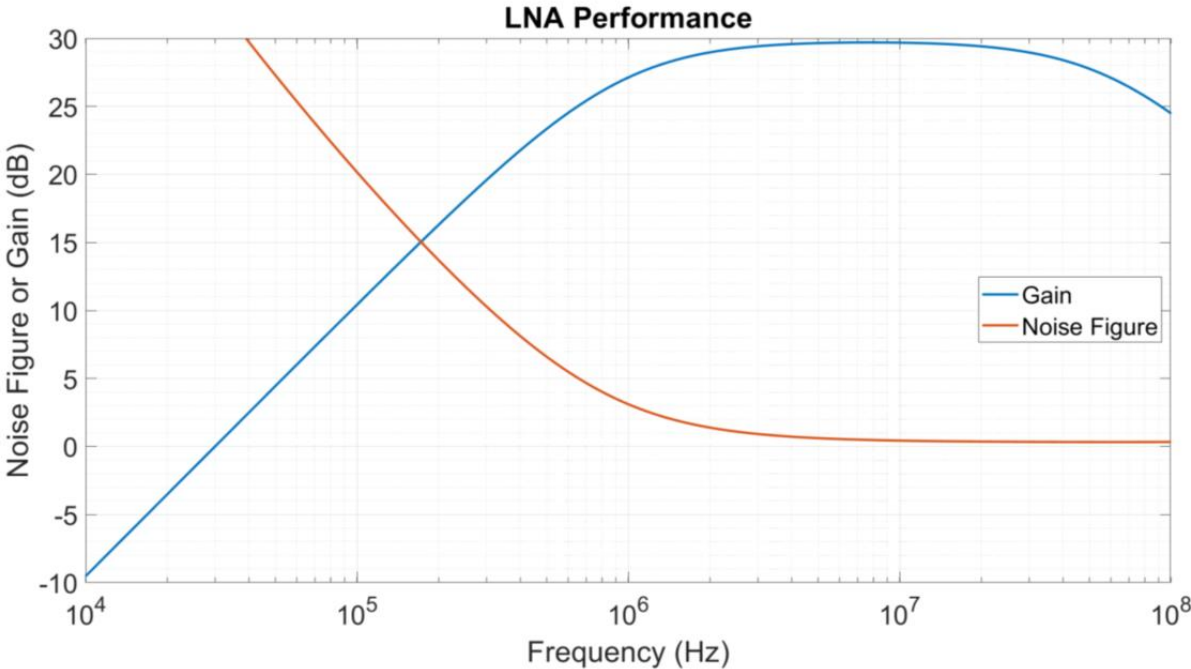
Figure 4-10. LNA simulated gain and noise figure.
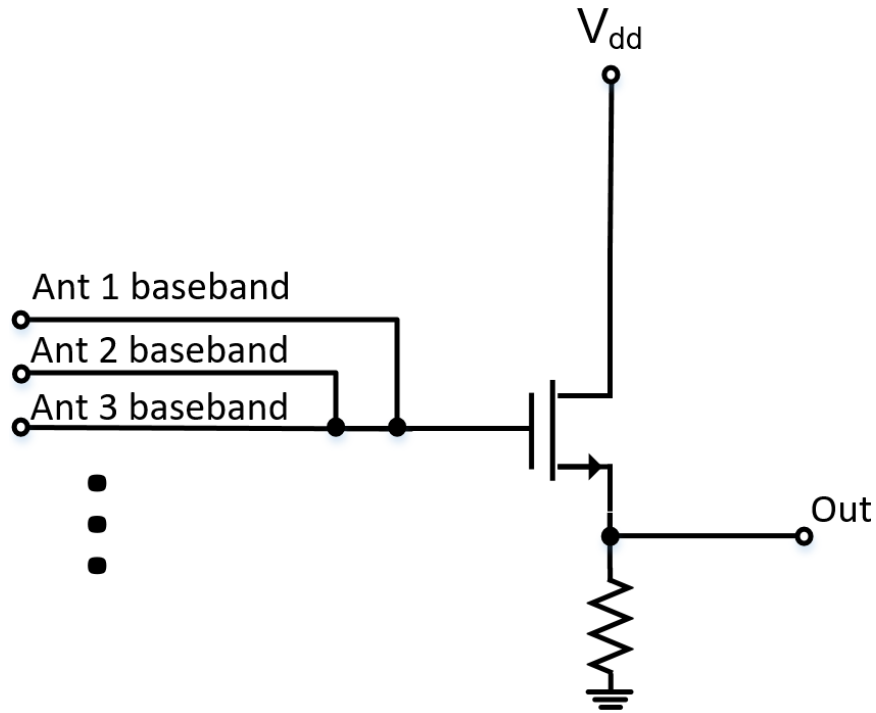
Figure 4-11. Summation of 12 antennas' baseband output via current-mode summation, followed by common drain buffering. This is repeated for each polarity in the differential output signal.

source (CS) amplifier, with additional circuitry for biasing, stability and low-pass output. The amplifier is modeled to consume 1.1mA of DC current, and have 29dB of passband gain. Figure 4-10 depicts simulated gain and noise figure of the LNA. The LNA was designed with low noise voltage such that the noise of the system is dominated by the mixer's noise.

Following the LNA is an analog balun, converting the single-ended output to a differential one to facilitate one-bit phase shifting in subsequent stages. As seen in Figure 4-9, the balun consists of a common base amplifier, serving as a noninverting amplifier, in parallel with a common source amplifier, serving as an inverting amplifier. The two amplifiers are designed to be matched in common-mode voltages and equal in gain to minimize the common mode component of the resulting signal. The balun is modeled to have a gain of 13dB and a current consumption of 0.3mA.

The subsequent stage is an analog baseband one-bit phase shifter, as seen in Figure 4-9. The balun's differential output is either inverted (/Phase) or not inverted

(Phase), as set by a bit in the antenna logic's shift register. This provides a lossless, broadband phase shift of exactly 180 degrees in the passband.

In aggregate, the baseband receiver path for each antenna consists of circuitry to amplify and phase shift baseband radar signals in a low-loss and low-noise way, for processing at the chip level.

4.6. Chip Level Array Architecture

On the chip level, the THz generation path takes an input 28GHz FMCW signal and generates a 265GHz FMCW signal, which is fed to each of the twelve antennas, which are spaced at approximately half wavelength spacing in a 2 x 6 configuration. Each antenna additionally contains a power splitter, allowing a portion of the THz energy to be fed to a mixer to serve as a Local Oscillator and mix with radar echo signals.

A SPI-like interface is used to control the settings for the antennas, each of which includes a 3-bit shift register with one bit each for the THz Tx phase shifter, baseband Rx phase shifter, and off switch. All shift registers for each of the 12
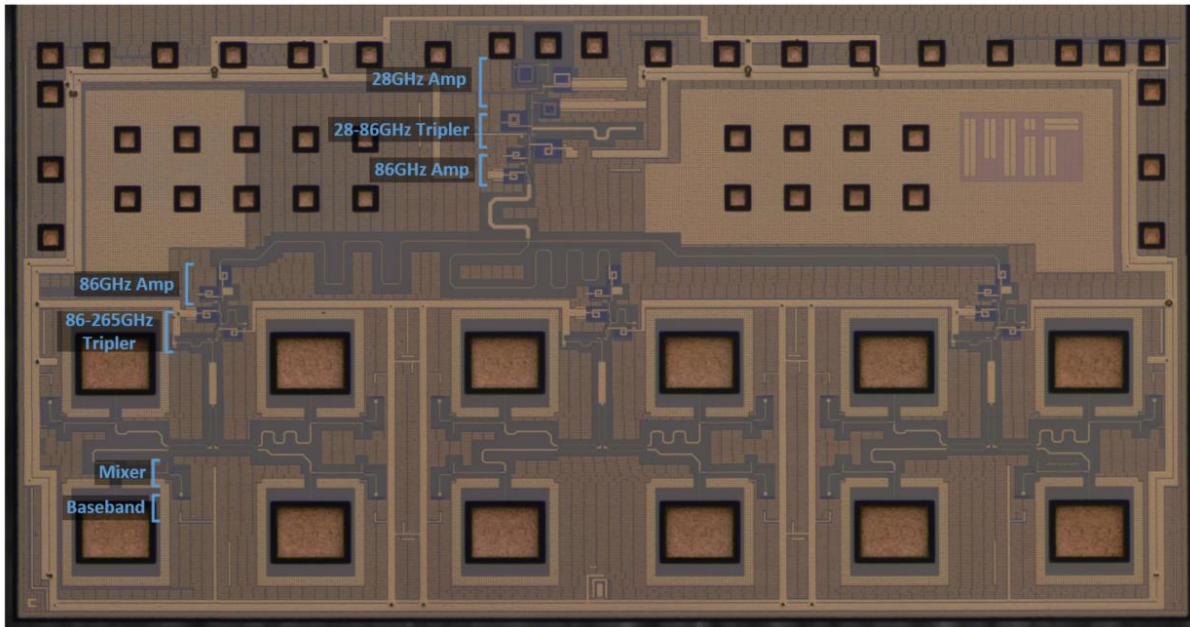
Figure 4-12. Die Photo of one-bit phased array chip, with annotations.
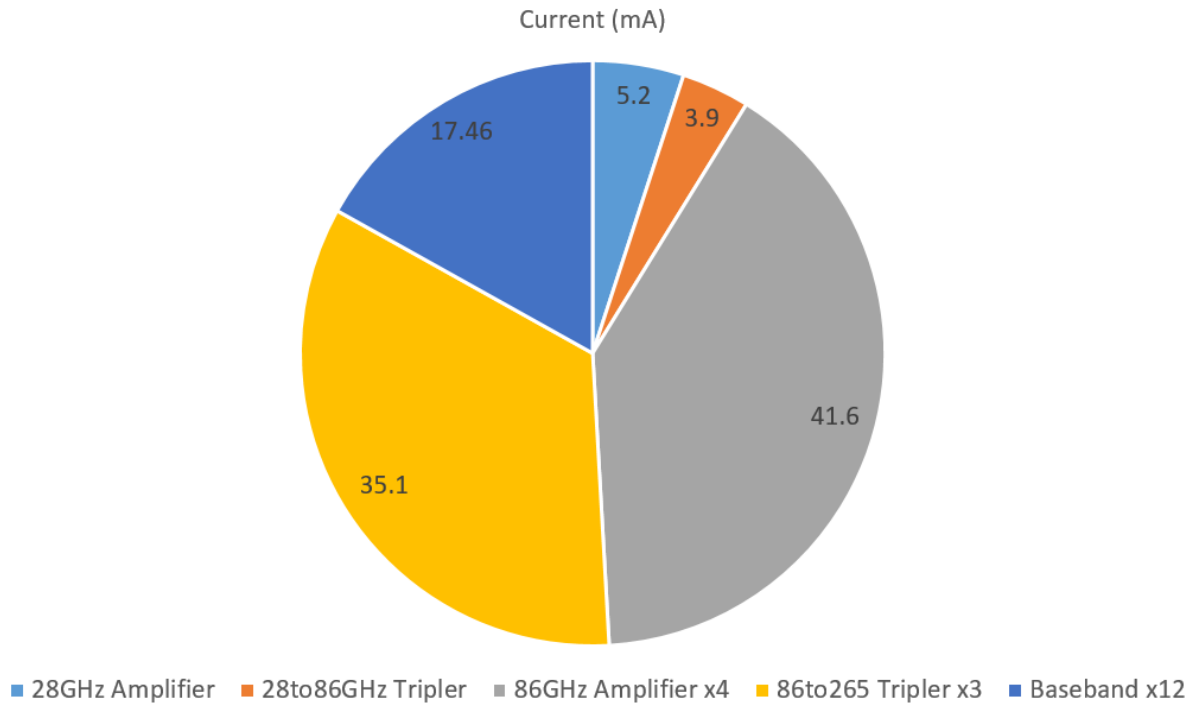
Figure 4-13. Component breakdown of power consumption of one-bit phased array chip.

antennas are placed in a serial configuration, with input and output data and clock signals on opposing sides of the chip for tiling with adjacent chips.

Each antenna's low-frequency differential output within a chip is combined by current-mode summing via direct connection of their output stages, as seen in Figure 4-11. An additional common-drain amplifier on each polarity of the differential radar output signal buffers the signal for off-chip use.

A die photo of the chip can be seen in Figure 4-12. The chip is implemented in Intel 22nm FinFET technology and measures 2 x 4 mm^2. The total power consumption of the chip is modeled to be 103 mA. A chip-level breakdown of modeled power consumption by component can be seen in Figure 4-13.

4.7. System Level Architecture

On a system level, similar to the previously described reflectarray, multiple chips are tiled to create a large antenna array. In particular, 16 chips are tiled onto a PCB,
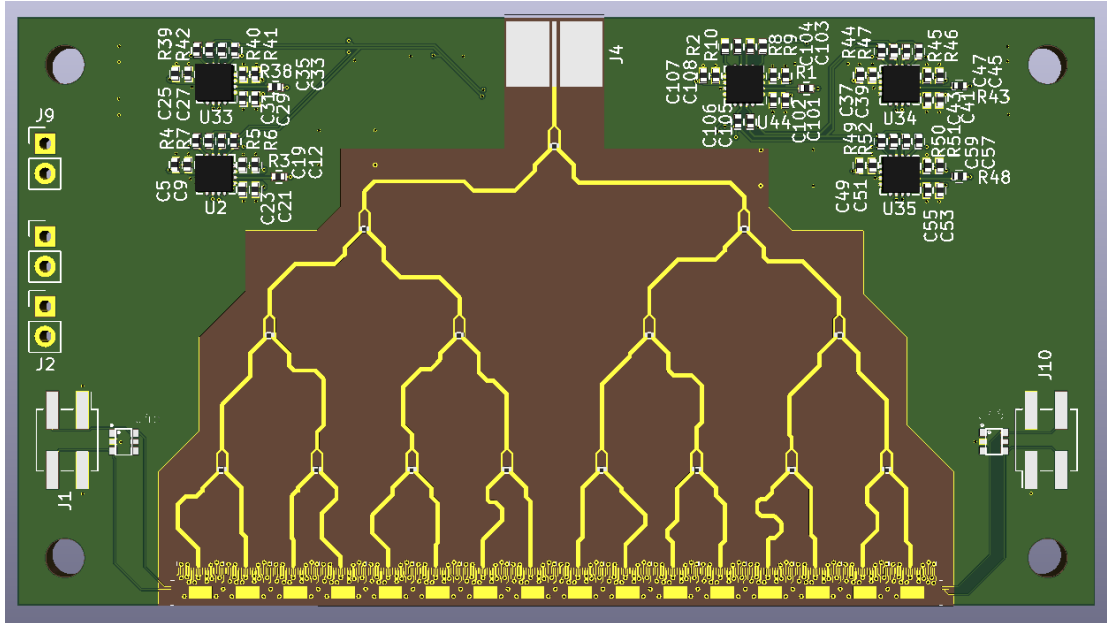
Figure 4-14. CAD drawing of 16-chip phased array PCB.

with two PCBs placed back to back to create in total a 96 x 4 antenna array. Chips are stitched together for daisy chain-style communication of clock and data for control, while power, RF and bias signals are conveyed directly from PCB. A block diagram of the RF portion of the system level design can be seen in Figure 4-15.

As previously discussed, the purpose of the on-chip fixed transmission line phase shifters is to break periodicity in phase error arising from one-bit phase quantization in a manner analogous to the spatial feed in the reflectarray case. This serves to break periodicity of phase errors within chip and reduce peak sidelobe levels within a chip, however a large array is produced from a tiling of identical chips. The periodicity in these phase errors exists on the chip level, every six antennas. Due to the Fourier transform analogy between aperture wavefront and radiation pattern, this low spatial frequency term in the phase error translates to periodic and coherent sidelobes in the radiation pattern. This is resolved by a further randomization of phase on the PCB level, through the length of low-frequency 28GHz transmission lines fed to each of the 16 chips. This can be seen in Figure 4-14, a computer generated layout of the chip carrier PCB. Implemented in Rogers 4002 material, it conveys a single 28GHz FMCW input through Wilkinson dividers and transmission
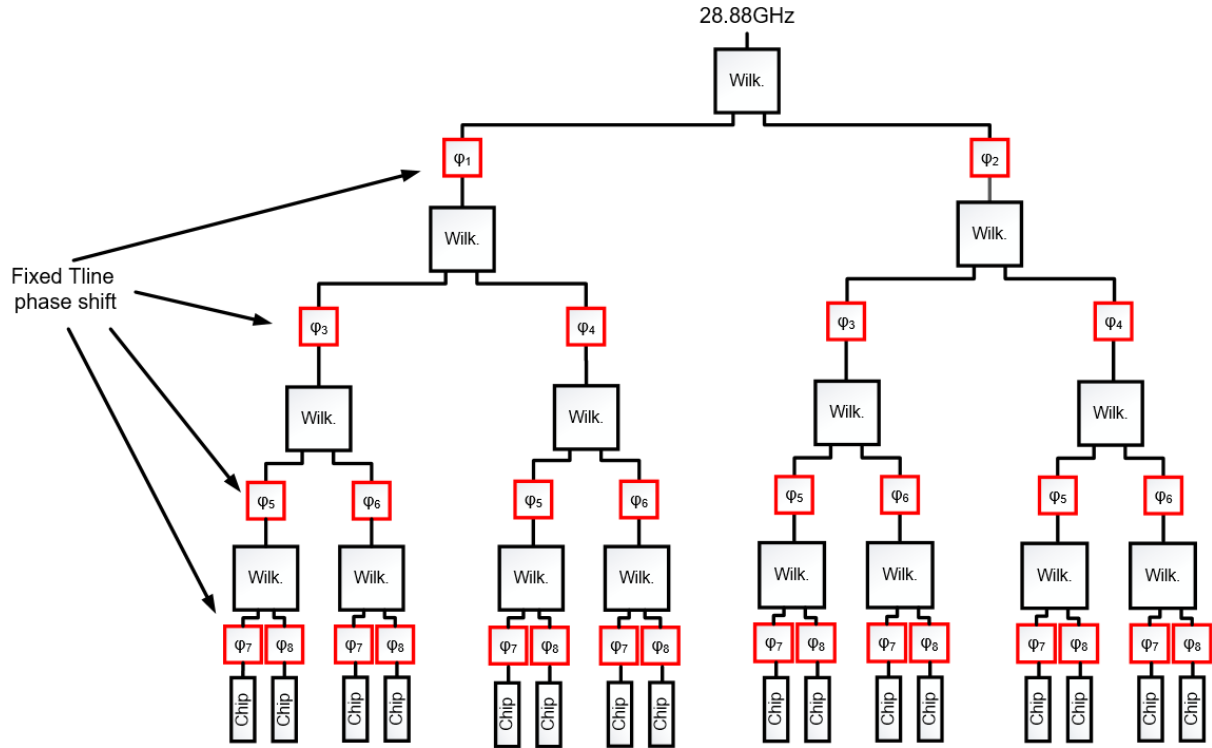
Figure 4-15. System-level RF block diagram of one bit THz phased array.

line phase shifters to each of the 16 chips per PCB. The random phase shift values were chosen via numerical simulation to minimize peak sidelobe level.

Similar to on-chip power combining for IF radar output signals, multiple chips' differential IF outputs are combined, as seen in the system-level IF block diagram in Figure 4-16. Groups of four chips are combined in current-mode summing, and fed into differential amplifiers (LT-6402, Analog Devices, Wilmington, MA). The output of each of these "group of four" differential amplifiers is fed together using current-mode summation, and the final output signal of the combined 16 chips is buffered via another differential amplifier before output to spectrum analyzer or ADC.

A simulated radiation pattern arising from the 98 x 4 one-bit phased antenna array in the above configuration can be seen in Figure 4-17.
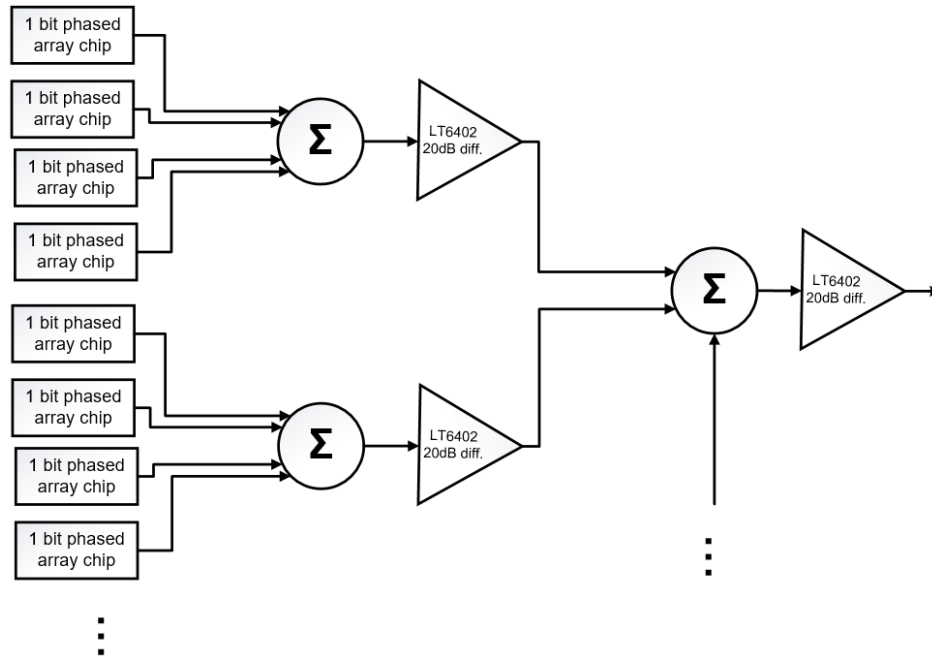
Figure 4-16. System-level block diagram of IF signal flow for THz one-bit phased array radar.

The architecture described here conveys the ability to independently steer the Tx and Rx radiation patterns through the antenna one-bit phase shifter and IF one bit phase shifters, respectively. While many applications would derive maximum performance from the spatial alignment of transmit and receive radiation patterns, it is possible that additional benefits and applications arise from this additional degree of freedom. In addition, other benefits are possible such as the reduction in sidelobes by mitigation techniques such as those described in future chapters of this thesis. Additional performance enhancements may be possible by the dithering of both transmit and receive patterns. This presents an opportunity for future research. Regardless, the one-bit phased array radar technique described here builds on the techniques described in the reflectarray in previous chapters by trading the spatial feed for randomized feed phases, trading the spatial feed complexity and hardware for additional losses in the feed for the one-bit phased array case. Additionally, this work presents a fully integrated THz radar transceiver with the ability to independently steer the receive radiation pattern from the transmit one, by
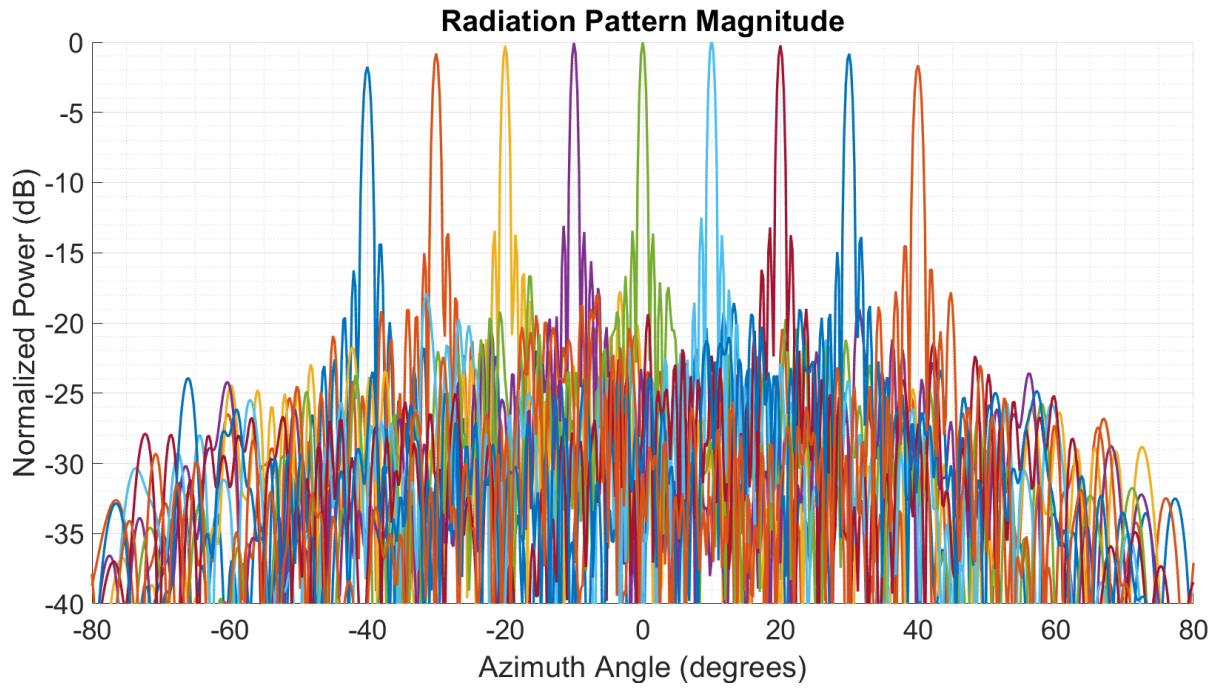
Figure 4-17. Simulated radiation pattern of 16x2 chip one bit THz phased array radar.

employing one-bit phase shifters in the receiver path. This allows for a simplified
THz system employing only a single baseband sampler and processing path.

Chapter 5

Array Performance Enhancement Algorithms

In this section, techniques are introduced for the enhancement of antenna array performance in radar imaging applications. In particular, a method for correction for beam squint in wideband FMCW radar applications is introduced, along with application of a sidelobe mitigation in radar imaging applications. Both requiring rapid updates in programmed phase states, both techniques for performance enhancement rely on and are enabled by each antenna's built in memory.

5.1. Beam Squint Correction

Beam squint is a performance-degrading issue in wideband FMCW radars, as described in previous sections. While wide available bandwidths are a common argument for the utility of THz systems, the same wide bandwidth leads to this performance reduction, dampening the argument for the use of THz for FMCW radars. As described in previous sections, a 10GHz bandwidth in a classical phased array system with a single set of phases can result in a beam squint exceeding three degrees in typical applications. This increases the effective beamwidth seen during one chirp of radar operation, reducing the effective resolution of the resulting radar image, particularly at wide angles from boresight.

A scheme to mitigate this beam squint effect is straightforward. It relies on updating the programmed array's phases based on the appropriate frequency at different points in the frequency chirp, such that the difference between the assumed frequency during phase calculation and instantaneous frequency is minimized, thereby minimizing beam squint. Such a technique was previously impractical due

to the rapid updating of phases it entails and the associated digital bandwidth. However, in this hardware implementation where phases are pre-calculated, loaded onto the array at startup, and cycled during array operation, it is attainable.

5.1.1. Measurement results

In this scheme, phase shifter settings are updated mid-chirp to account for varying instantaneous frequencies. This stands in contrast to results presented in Chapter 2, where a single set of phases is assumed while measuring radiation performance at different frequencies. A replication of the measured radiation pattern results presented in Chapter 2 can be seen in Figure 5-1, along with measured radiation results incorporating the beam squint mitigation scheme, where different sets of phases are assumed at each of 260, 265 and 270GHz. In both cases of measurement results, the same testbench and methodology was used as described in Chapter 3. As can be seen from the measured results, prior to the incorporation of beam squint mitigation the beam's direction moves by more than 3 degrees over a 10GHz bandwidth. After implementation of the beam squint mitigation, the mainlobe direction's movement has been reduced to below measurable levels. During FMCW radar operation any number of frequencies could be chosen for phase states based on
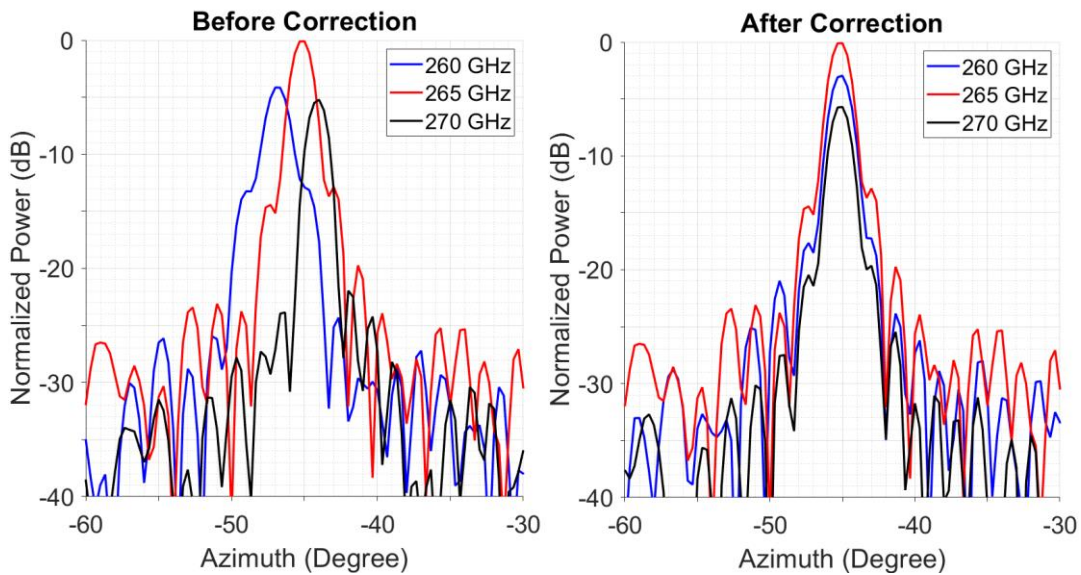
Figure 5-1. Beam Squint mitigation scheme.

acceptable level of beam squint; a tradeoff exists with memory and power consumption. Such a technique is enabled by the incorporation of on-chip memory. The technique requires synchronization between the low-frequency FMCW ramp signal and the reflectarray's clock to coordinate programmed phase states during a chirp sequence. The extreme limit of this technique is set by the update rate of the phase shifters in the array, however more practical limits exist in memory and power consumption.

5.2. Sidelobe Reduction

Sidelobes are a consideration in any RF wireless system, including radars and particularly imaging radars. The IF signal's frequency content represents distance to
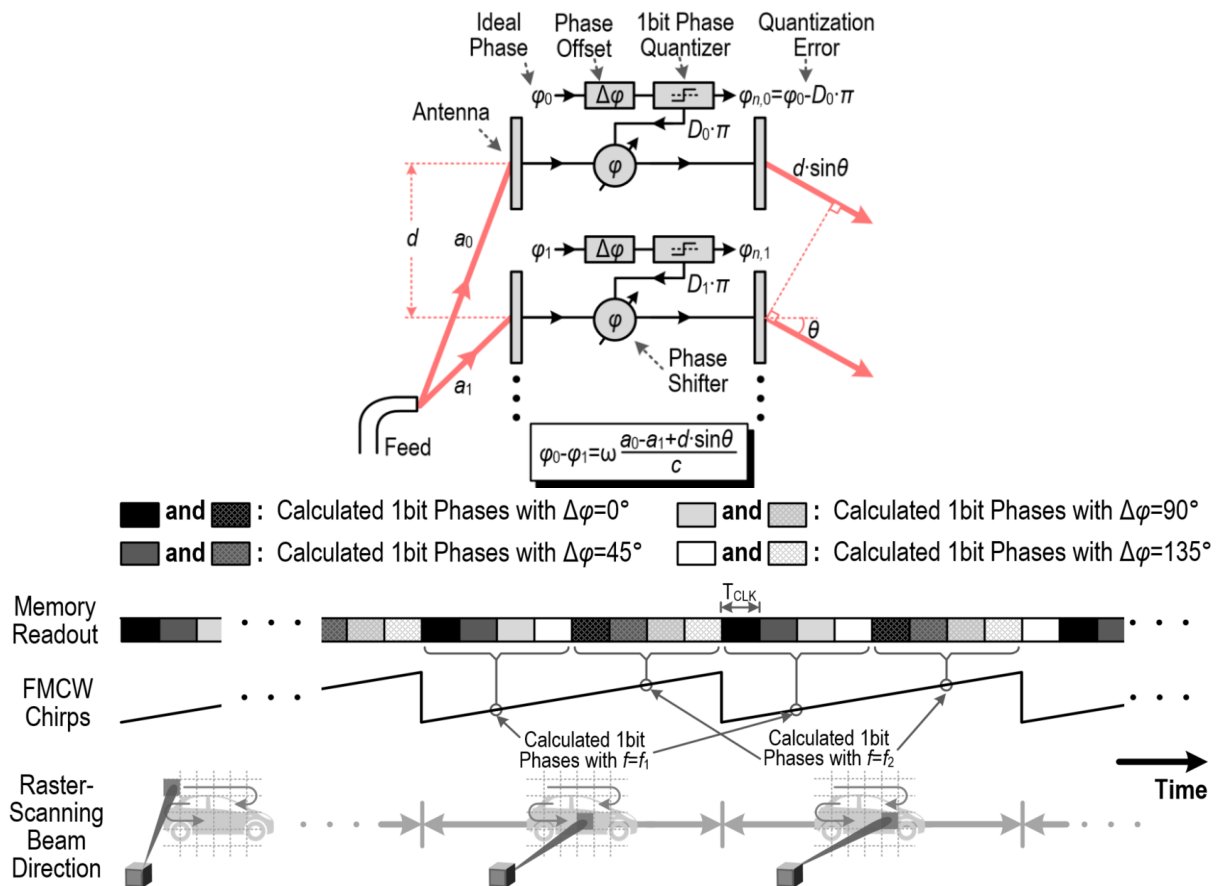
Figure 5-2. Sidelobe reduction scheme.

102

$\phi_f = 0^o$ $\phi_f = 45^o$ $\phi_f = 90^o$ $\phi_f = 135^o$
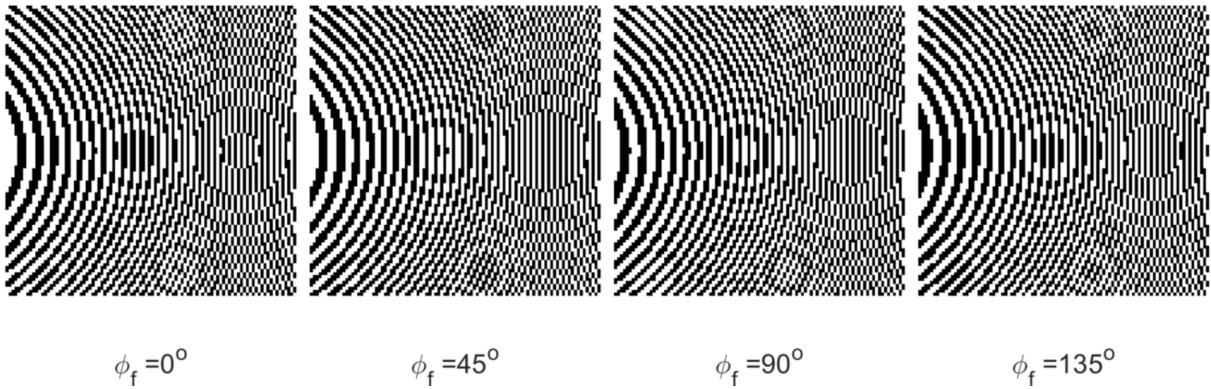
Figure 5-3. Quantized phases for four equally distributed values of φ_f, as used in sidelobe mitigation scheme.

radar targets, and is a linear combination of different directions' reflectivities and distances, weighted by the antenna's radiation pattern. In imaging radar systems with rasterized high-gain beams, finite sidelobes in radiation pattern when combined with non-sparse environments can result in false returns which are indistinguishable from the returns in the desired direction, presenting as clutter in the resulting radar image. While this undesirable effect is mitigated by having high directivity mainlobe beams such as in the presented reflectarray, it is degraded by the use of one bit
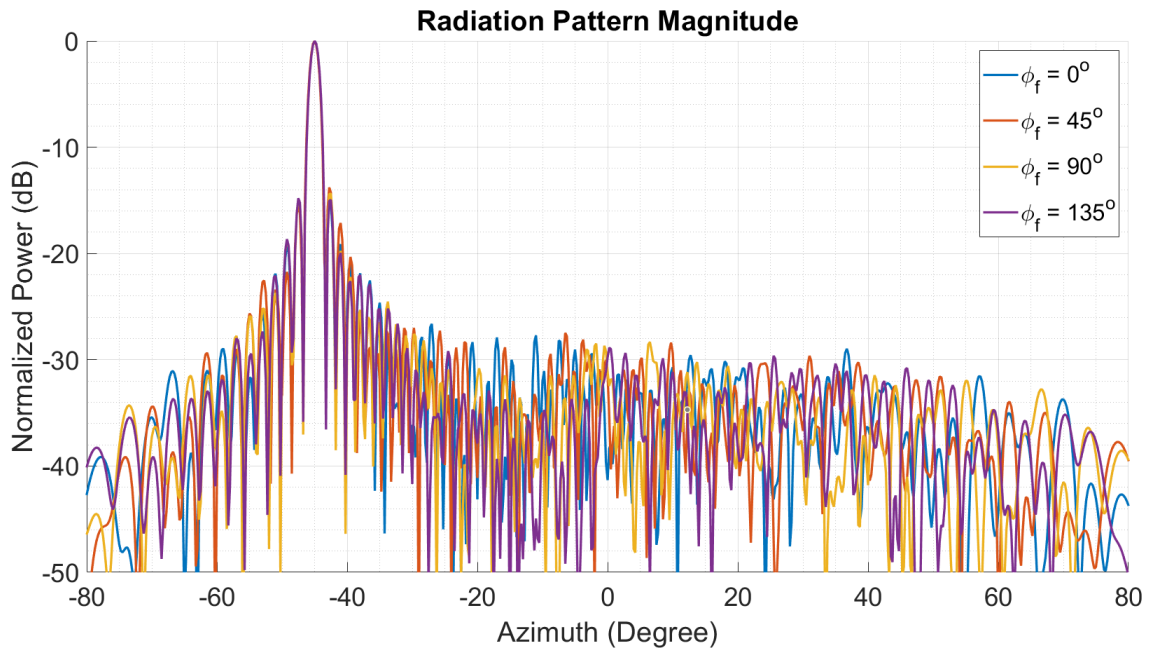
Figure 5-4. Radiation pattern magnitude for four equally distributed values of φ_f, as used in sidelobe mitigation scheme.

103

phase shifters and their associated increase in quantization sidelobes, as discussed in Chapter 2. A number of methods exist to shape the quantization noise and reduce peak sidelobe levels to an average level, however these methods either preserve or increase average sidelobe level [107], [120], [134].

There exists one known technique to reduce the average quantization sidelobe level in a phased array based radar imager, which has been discussed both theoretically [107] and experimentally [120]. In this dithering-like approach, a phase term φ_f is added to all antennas phases before quantization. This term is constant across the entire array, but varies with time during multiple integrations of the radar imager, as seen in Figure 5-2. The inclusion of this term φ_f will alter the quantized states of each antenna, flipping some from 0 to 180 degrees or vice-versa, as can be seen in
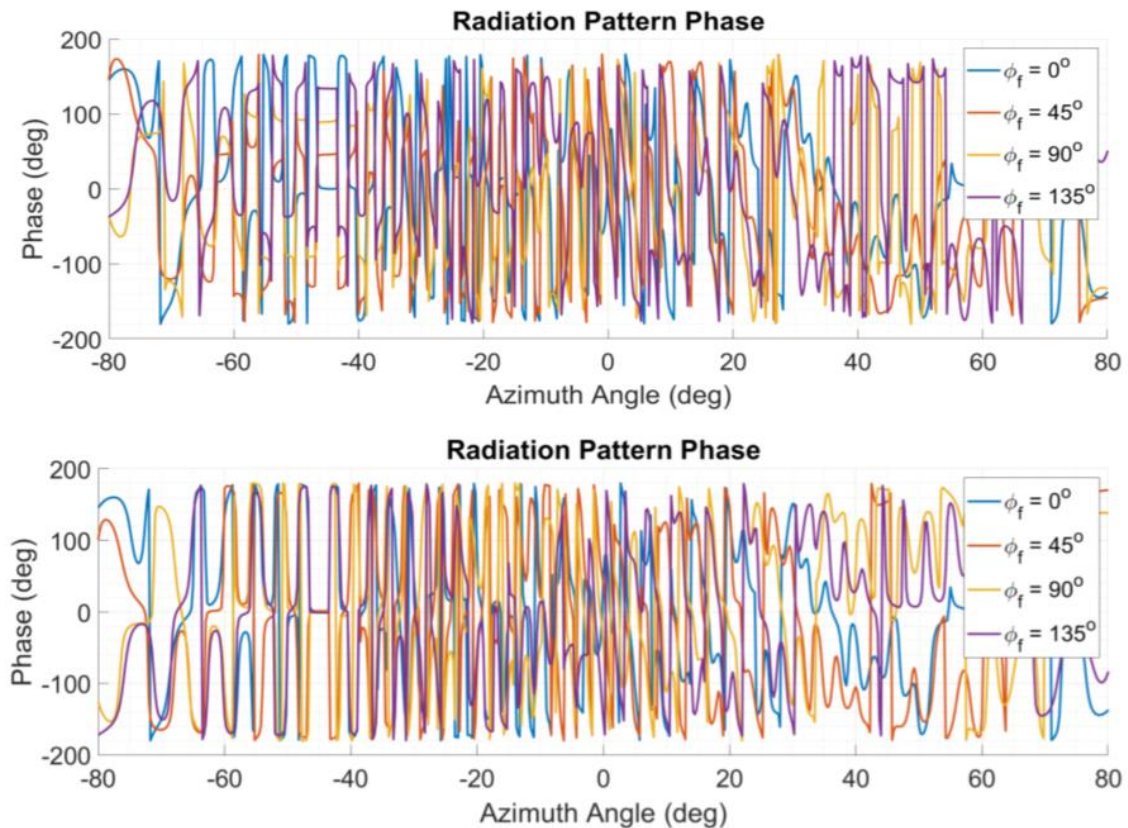
Figure 5-5. Radiation pattern phase for four equally distributed values of φ_f, as used in sidelobe mitigation scheme, both before correction (top) and after correction (bottom) for a mainlobe steered to -45 degrees.
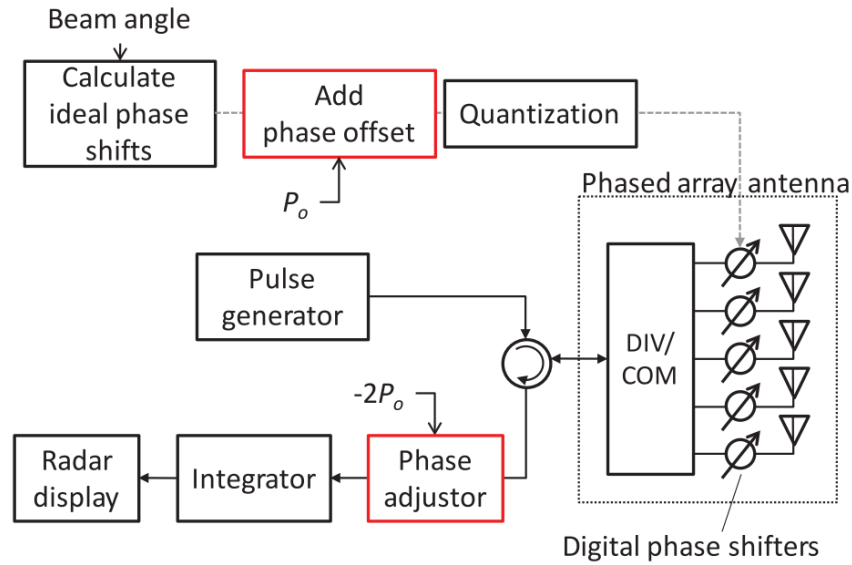
Figure 5-6. Original sidelobe mitigation scheme hardware block diagram, reproduced from Kamoda et al.

Figure 5-3. As seen in Figures 5-4 and 5-5, the effect on the radiation pattern's mainlobe and sidelobes are different. The radiation pattern's mainlobe's direction is preserved, while it's phase is shifted by the same amount φ_f. In contrast, the sidelobes arising from quantization are randomized in both magnitude and phase. The mainlobe phase shift is undone by the inclusion of a baseband phase shifter, the only extra piece of hardware needed for this technique. In multiple integrations the phases are updated according to varying values of φ_f while the baseband phase shifter shifts accordingly, such that the mainlobe adds coherently and the sidelobes add incoherently. A block diagram of this approach, reproduced from [107], can be seen in Figure 5-6, where φ_f is equal to P_o, and the baseband phase shifter's value is either P_o or $2P_o$ based on the use of a monostatic or bistatic radar. The resulting radar has an effective radiation pattern with lower sidelobes, approaching a radiation pattern arising from perfect phase shifters with infinite numbers of integrations, as seen in simulated data in Figure 5-7, with simulated reflectarray parameters equal to the experimental hardware presented in Chapter 3. This two-dimensional radiation pattern is equivalent to a point-spread-function (PSF) in an imager. In this approach, the optimal values of φ_f are equally distributed over [0 LSB], where LSB is the minimum step size of the quantized phase. For example, with a one-bit phase

shifter and four integrations, the optimal values of φ_f are [0 45 90 135] degrees, maximizing the randomness applied to the quantization sidelobes.

While this approach is extremely powerful in its ability to reduce sidelobes and mitigate the detrimental effects of phase quantization, it is limited in its practicality in real-world real-time imaging applications for two reasons. Firstly, the approach as presented calls upon a baseband phase shifter to maintain mainlobe coherence.
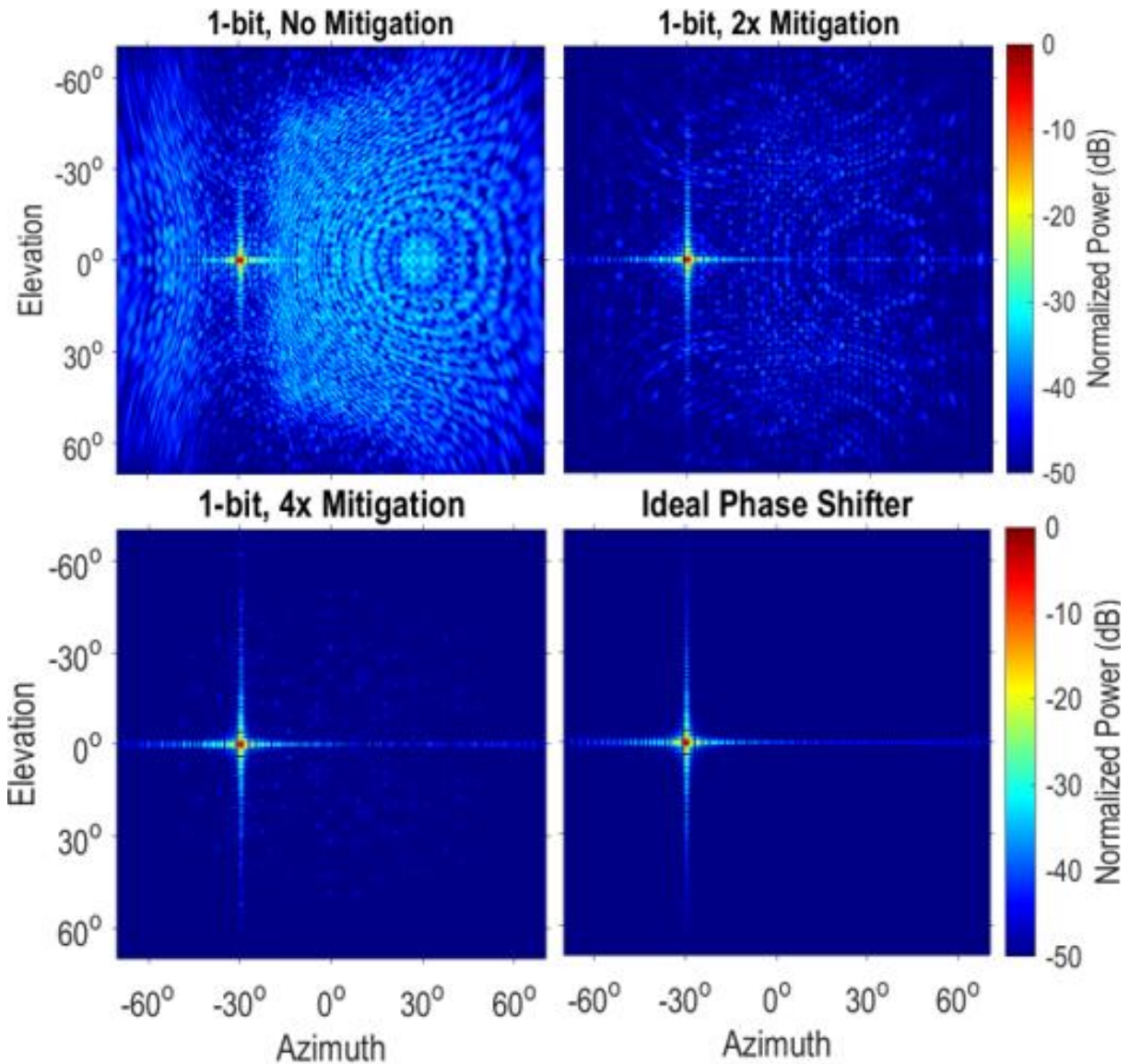
Figure 5-7. Two dimensional radiation pattern simulated magnitude for a one-bit phase shifter with no sidelobe mitigation, two and four integrations, and with ideal phase shifters.
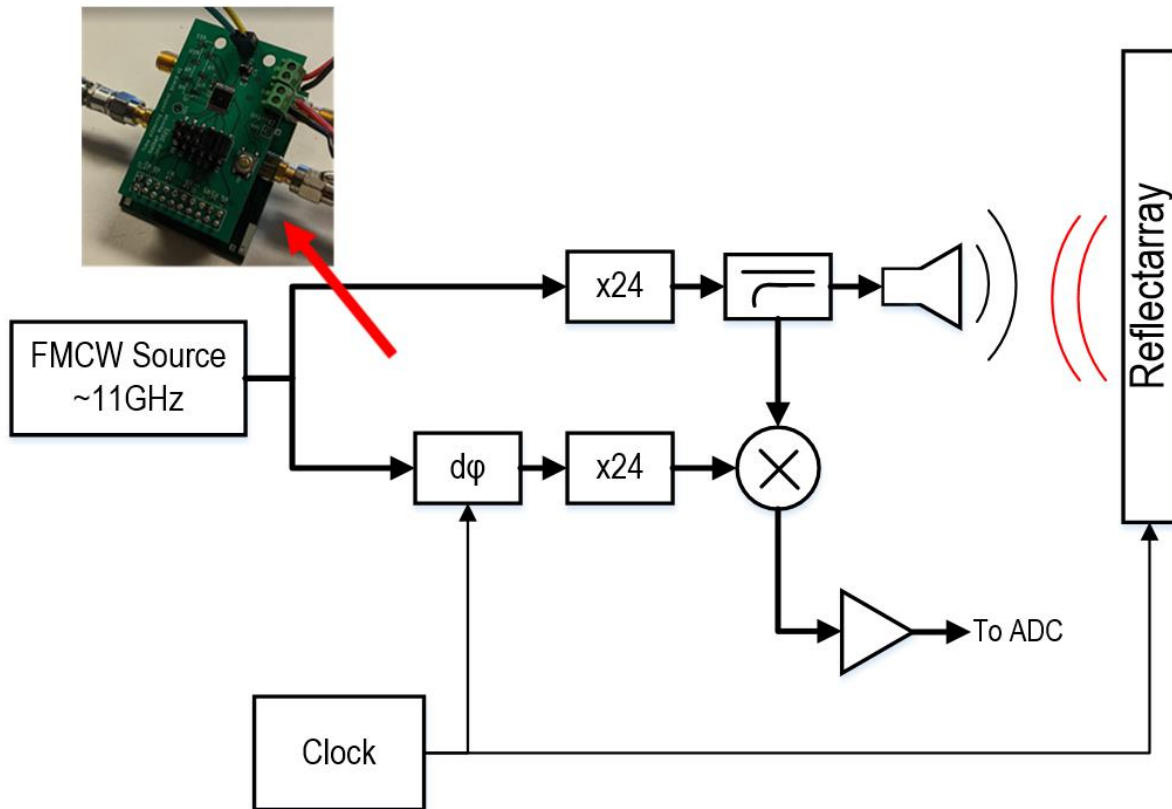
Figure 5-8. Improved hardware block diagram for sidelobe mitigation with low-frequency phase shifter integrated into LO path. (inset) realized hardware implementation.

Accurate broadband phase shifters at baseband are difficult to achieve with analog circuits. Alternatively, DSP-based approaches come with a heavy computational burden given the number of samples, integrations and pixels a relatively short times necessary for high framerate imaging. Therefore, in this work, a simple modification is made to move the phase shifter into the Local Oscillator path, as seen in Figure 5-8. By phase shifting the LO relative to the transmitted signal, the mixer's output IF signal is phase shifted by an equivalent amount, allowing it to be equivalently tuned to maintain mainlobe coherence. By incorporating the phase shifter into the low frequency LO path before frequency multipliers, simple off-the-shelf parts can be used which meet relatively narrowband requirements.

In the implemented system, a digital phase shifter is used (MAPS-010166, MACOM, Lowell, MA), with additional counter and control circuits as seen in Figure 5-8. This

allows the LO phase shifter to be driven by the same clock as the reflectarray, as seen in Figure 5-8, such that the two increment to successive φ_f values in tandem. This self-synchronized design requires no additional hardware, and is transparent to the radar transceiver.

The second element of impracticality in the existing sidelobe mitigation approach is in its exacerbation of the digital bandwith issues discussed in Chapter 2, where each antenna requires multiple bits for each pixel and a corresponding increase in digital bandwidth needs. This is effectively mitigated in this work's reflectarray described in Chapter 3, where each antenna incorporates local memory to store precomputed phase states. Therefore, the sequence of beam states required for imaging, with sidelobe mitigation and beam squint mitigation and pre-computed and loaded onto the array at startup, effectively eliminating the digital bandwidth issues and allowing for practical implementation of these algorithms. The resulting reflectarray-based THz imaging system has sidelobe performance approaching that of one with ideal phase shifters, while maintaining all the benefits of one bit phased shifters as described in Chapter 3.

5.2.1 Far Field sidelobe reduction

As discussed in Chapter 2, antenna arrays with one bit of phase quantization are a special case due to the ambiguity and redundancy between 0 and 180 degrees, resulting in symmetry in radiation patterns. This is mitigated in the case of reflectarrays with near field feed, where the spherical phase term breaks the phase symmetry, causing the sidelobes to "whiten" and reduce to approximately their average level while reducing the peak sidelobe level significantly. This approach allows for the use of one-bit phase shifters while eliminating the symmetrical sidelobes. Such an approach, while effective, places additional constraints on feed geometry, as discussed in Chapter 2, and also introduces a tradeoff between aperture efficiency and sidelobe mitigation.

The sidelobe mitigation approach described previously and adapted in this work serves to mitigate all quantization sidelobes, including the symmetric sidelobes arising from a one bit quantized reflectarray with a far field feed. This can be seen in simulation data in Figure 5-9, which includes simulation data for a reflectarray configuration presented in Chapter 3 with an incident plane wave, emulating a radiation source which is far away. Intended mainlobe direction is at -45 degrees, and increasing integrations with the sidelobe mitigation eliminates symmetric sidelobes at +45 degrees and others. This effect, previously unreported in literature, allows for the breaking of tradeoffs in feed design between sidelobe mitigation, system volume and aperture efficiency. In addition, with simple adaptation to communication protocols, could allow for the adoption of smart THz one bit reflective surfaces in future generations of communication systems as have been proposed in [70], [135]–[137]. Such surfaces' applicability is enhanced using the features described in this work's reflectarray, with local computation or memory enhancing smart reflectors' performance and low power operation allowing such
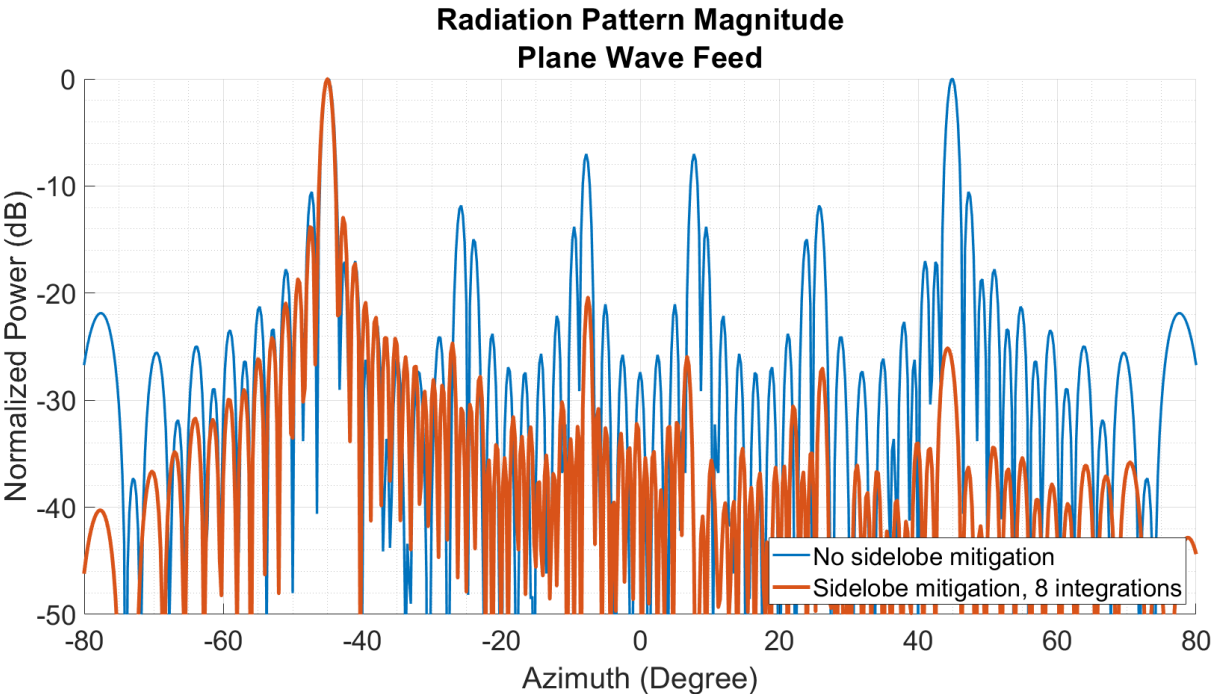
Figure 5-9. Simulated radiation pattern of one bit reflectarray with far-field feed, resulting in an incident plane wave, with no sidelobe mitigation and with 8 integrations of sidelobe mitigation.

surfaces to be powered by far-field THz power transfer, energy harvesting or other approaches.

5.2.2. Measurement results

The sidelobe reduction approach described in this Chapter was implemented with the reflectarray and testbench described in Chapter 3. Measurements were taken of E-plane cuts of radiation pattern with no sidelobe mitigation, 2 integrations and 4 integrations. Measured results can be seen in Figure 5-10. Radiation pattern measurements indicate a reduction in average sidelobe level of 4.6 dB for 4 integrations when considering only E-plane cuts of radiation pattern. However, measured results are consistent with 2-dimensional simulated radiation pattern measurements seen in Figure 5-7, approaching the case with ideal phase shifters with diminishing returns. As the principal E-plane and H-plane cuts have significant sidelobe contribution from amplitude taper over the aperture which is not mitigated

Measured E-plane radiation patterns with sidelobe mitigation
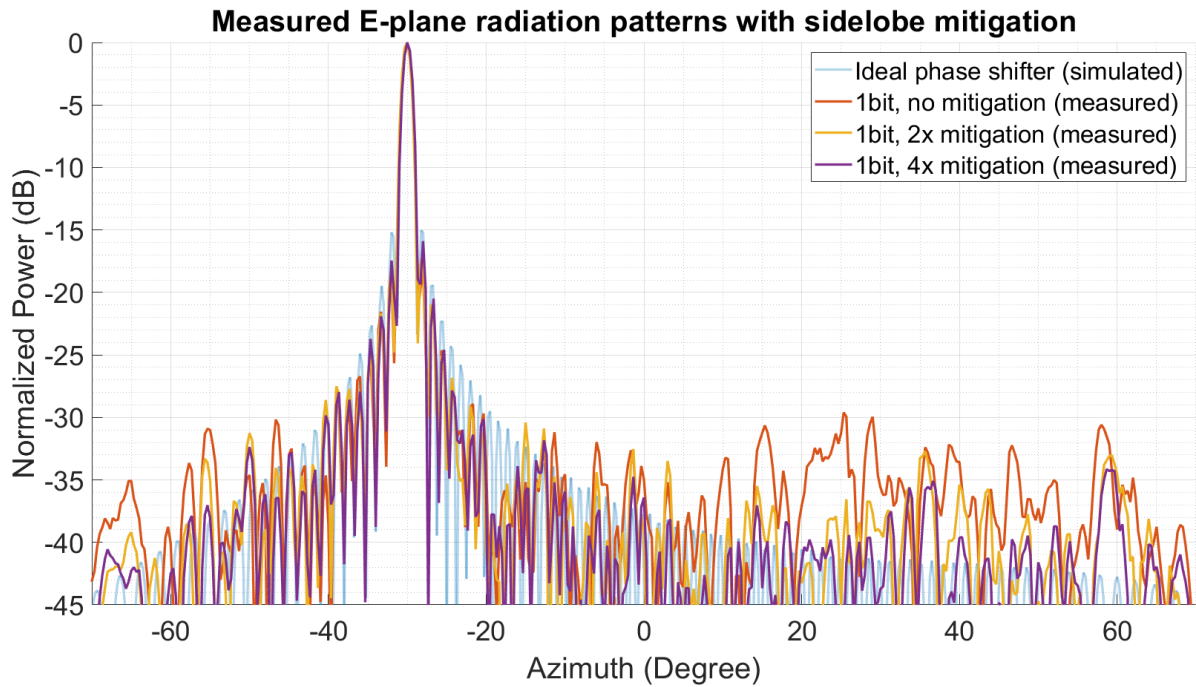
Figure 5-10. Measured radiation pattern of one bit reflectarray with no sidelobe mitigation and sidelobe mitigation with 2 and 4 integrations, plus simulated radiation pattern of reflectarray with ideal phase shifters.

by this approach, most of the sidelobe reduction benefit comes in off-axis directions which cannot be measured with this work's testbench.

There exist in the measured radiation pattern results peaks in sidelobes which are not reduced by the sidelobe reduction approach. For example, +36 and +59 degrees in Figure 5-10. These sidelobes are consistent with and likely explained by periodic perturbations in phase error due to possible effects such as bondwire interference or minute errors in die placement. These become more difficult to eliminate as array sizes increase and sidelobe levels are reduced.

The sidelobe mitigation scheme discussed here adapts and improves upon the method presented in [107], while making it practical for high frame rate and high resolution imaging radars. The inclusion of LO phase shifters increases practicality for THz imaging radars with incorporated frequency multipliers, while the incorporation of in-unit memory allows for practical implementation of the method by eliminating digital bandwidth challenges. The resulting radar imager is approaching in performance one with ideal phase shifters, while maintaining the benefits of one bit phase shifters.

Chapter 6

THz Radar Imaging Demonstration

In this chapter, the previously-described reflectarray is applied in the demonstration of a solid-state THz imaging radar application. The hardware and software systems necessary for such a demonstration are detailed. Finally, imaging results are presented in various scenarios with the reflectarray radar imager operating in various modes to demonstrate the applicability and utility of the technological approaches taken in this work.

6.1. Radar Imager Hardware Description

The radar imager described in this section consists of three primary hardware elements: a THz transmitter, THz receiver, plus the THz reflectarray which was previously described in Chapter 3. The THz transmitter contains circuits to generate an FMCW signal at THz frequencies. This THz FMCW energy is incident onto the previously described reflectarray. The reflectarray reflects the THz FMCW energy into a specified direction with its programmable narrow beam. The energy reflects off of a radar target and echo signals are incident on the THz receiver, where the echo signals are mixed with the FMCW Local Oscillator to produce a beat frequency signal, where the beat frequency encodes distance to the radar target. Therefore, this implementation is a bistatic radar configuration. This distance sample represents distance in a particular direction, representing one pixel in the radar image. The reflectarray's beam is successively swept across a scene with distance measurements taken in each direction to produce a depth image.

6.1.1. THz FMCW radar

A block diagram of the THz FMCW radar can be seen in Figure 6-1. An RF source (Keysight N5173b) is configured to produce an FMCW signal over 10.95GHz~11.04GHz. This signal is fed to a discrete Wilkinson divider (Minicircuits ZX10-2-126-S+), which feeds the FMCW signal to both a high power WR3.4 THz source (VDI AMC-681) and a THz WR3.4 harmonic mixer (VDI WR3.4MixAMC-I) which serves as the receiver. Both transmitter and receiver have an internal frequency multiplier of 24x, resulting in a final frequency range of 262-264GHz, corresponding to a bandwidth of 1.92GHz and a range resolution of approximately 7 centimeters, both limited by bandwidth limitations in both THz source and RF source. The THz source is fed to the reflectarray through a custom waveguide feed described in Chapter 3. The reflectarray is configured to steer a narrow Tx beam of THz energy on a small portion of the target scene, and reflected echo signals are
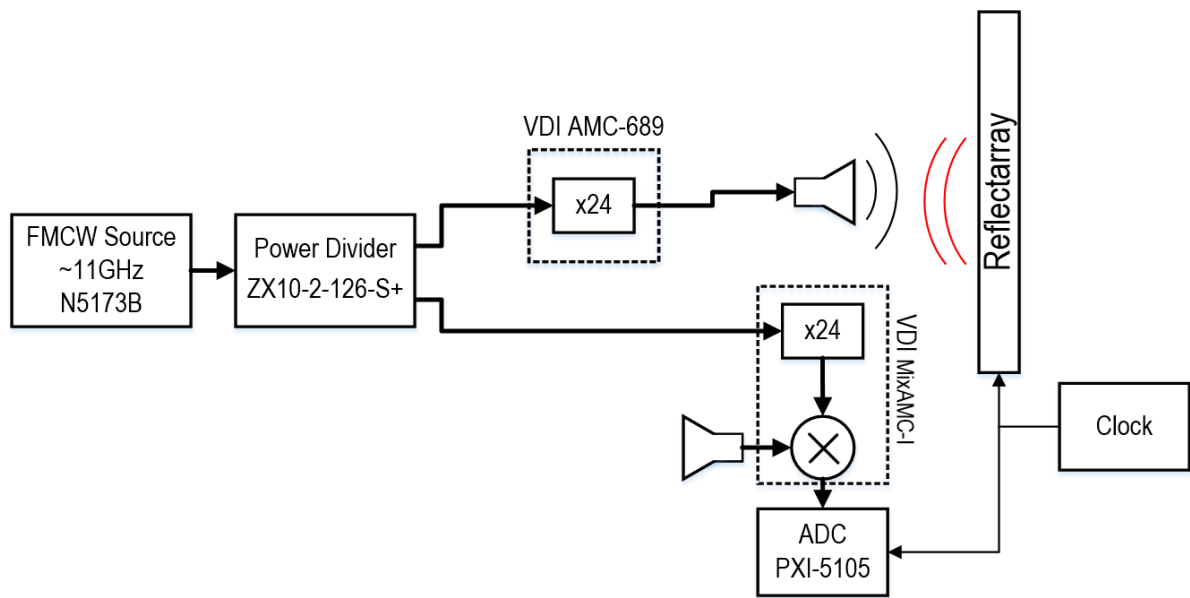
Figure 6-1. Block diagram of THz FMCW radar imager.
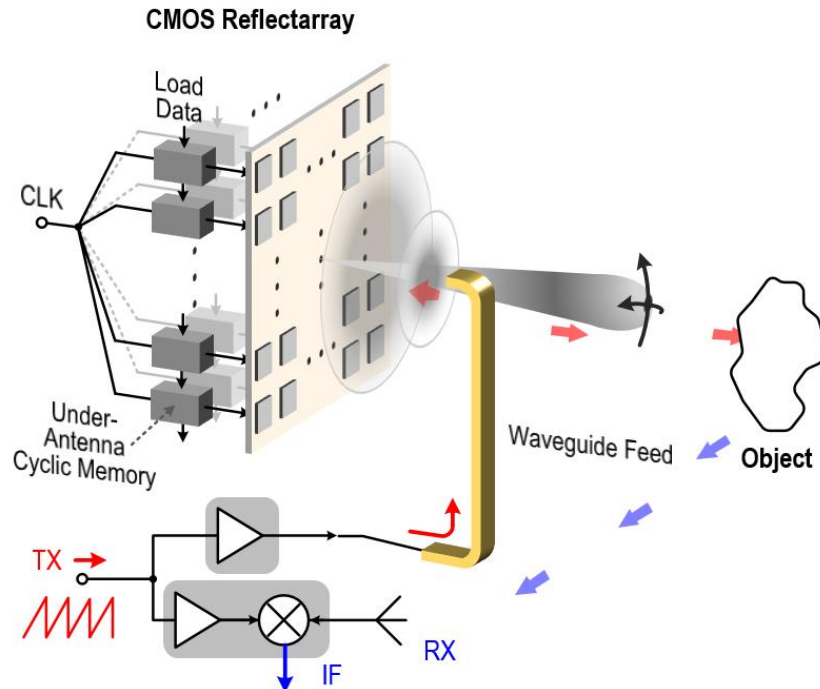
Figure 6-2. Schematic depicting physical representation of THz imaging radar.

received by the receiver which is placed nearly coincident with the transmitter, as seen in Figure 6-2. The receiver aperture is an open-ended WR3.4 waveguide with low ~10dBi of gain, allowing for adequate reception of radar signals over the desired viewing window of [-45 +45] degrees. While a monostatic radar configuration could theoretically produce a radar imager with an effective 84dBi of directivity due to the coincident nature of the Tx and Rx beam patterns, reciprocity in the reflectarray's radiation pattern and collocation of THz transmitter and receiver, equipment limitations and the requirement of a directional coupler mandated the adoption of a bistatic radar architecture in this proof of concept, limiting directivity to approximately 42dBi with a high directivity Tx beam and nearly omnidirectional Rx pattern. A photo of the THz portion of the reflectarray imager can be seen in Figure 6-3.

The reflectarray operation is configured to produce high directivity, 1 degree wide beams in successive steps of 1 degree over a viewing range of [-45 +45] degrees in

114
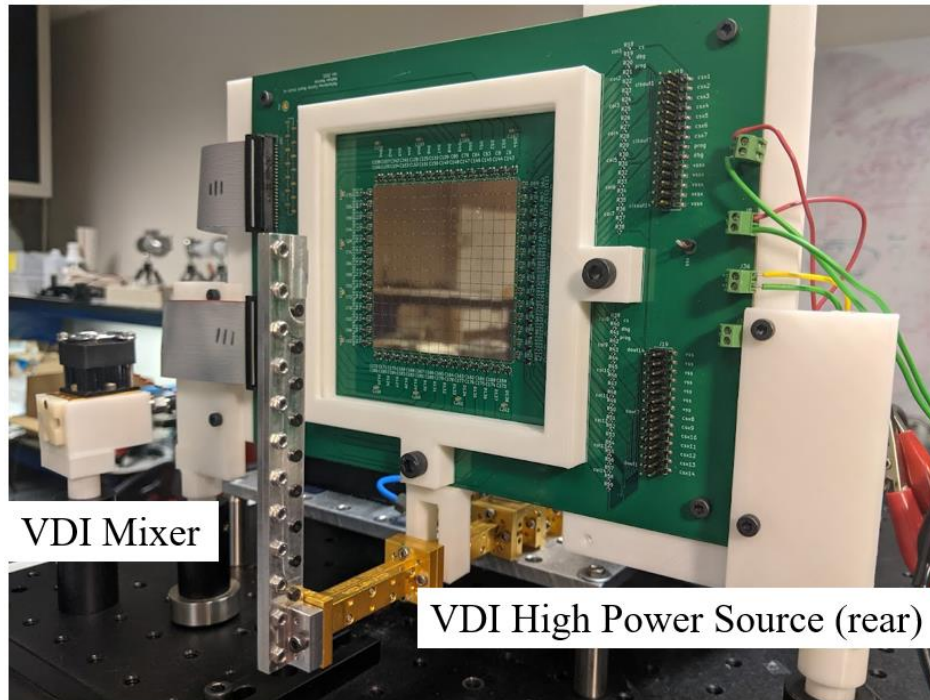
Figure 6-3. Terahertz portion of FMCW imaging radar.

both axes to produce a resulting 90x90 pixel image. Beam states are precalculated using MATLAB models and loaded onto the array at system startup.

The FMCW parameters are seen in Table 6-1. The RF generator's FMCW chirp is generated by analog modulation input, fed by a function generator (Tektronix AFG3102) which generates phase-aligned ramp chirp signals and clock signals for the reflectarray's beam states. The integration time of 15ms per pixel yields a total frame integration time of 121.5 seconds for a 90 x 90 pixel imager, when ignoring computational constraints and time cost during signal processing.

The IF signal output from the THz receiver is fed directly into a Pxi sampling system (National Instruments, Austin, TX) consisting of a PXI-5105 12-Bit, 8 channel 60MS/s digitizer and a PXIe-8301 interface, allowing the digitizer to be controlled by a PC via MATLAB. Operating at a sampling rate of 10MS/s, the digitizer synchronously samples the IF signal. All equipment, including the digitizer's sampling clock, are synchronized by 10MHz reference signal. A picture of the complete realized test setup can be seen in Figure 6-4.
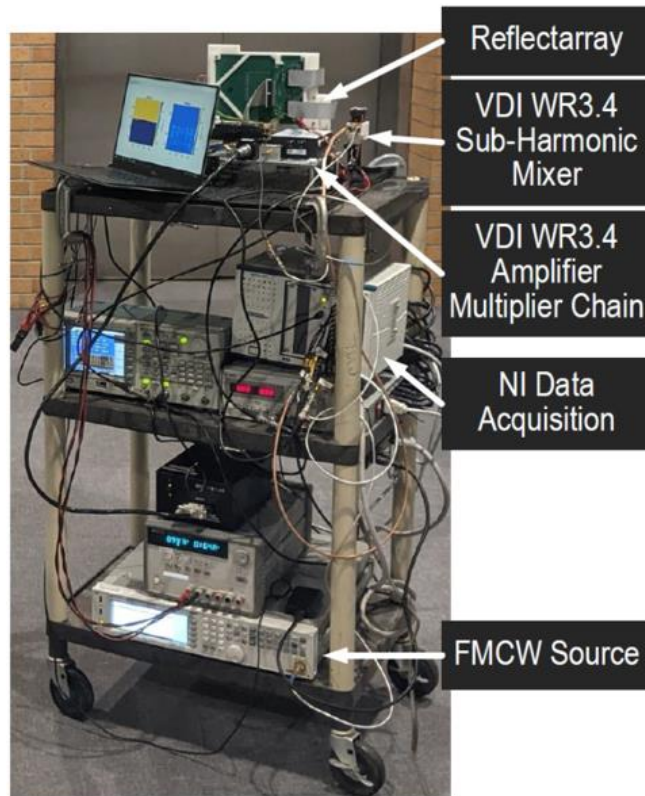
Figure 6-4. Complete realization of THz imaging radar system.

6.2. Radar Imager Software Description

Synchronization of FMCW function generators, clock generators and associated lab equipment are performed from a host PC by MATLAB over GPIB. Synchronization, control and data collection with the NI digitizer is performed from a host PC by MATLAB using low level drivers and a Thunderbolt interface. The reflectarray is programmed and controlled using the interface described in previous sections via a host PC by MATLAB. Signal processing is performed on host PC by MATLAB.

The imaging radar follows conventional FMCW radar signal processing techniques. IF waveforms are sampled, aligned to the falling edge of the reflectarray's clock, which aligns with change in reflectarray beam state. IF waveforms from multiple chirp integrations are averaged to improve signal to noise ratio. The first and last 5% of the averaged IF waveform is removed to mitigate transient noise due to sharp

Parameter	Value
Chirp rate (MHz/μs)	62.5
Transmit Power (dBm)	20
Transmit Bandwidth (GHz)	1.92
Frequency (GHz)	263~265
Resolution (cm)	7.8
Pixel Integration Time (ms)	15

Table 6-1. Terahertz reflectarray radar imager system parameters.

changes in RF generator frequency. A hamming window is applied to the resulting waveform, followed by a Fast Fourier Transform. Low frequencies associated with RF-LO leakage discussed in previous sections are blanked out, followed by a mapping of frequency to range using classic FMCW radar analysis and the FMCW radar parameters seen in Table 6-1. Finally, the radar range associated with the strongest return signal is recorded as a pixel in a two-dimensional image, where the pixel's location maps to the beam pointing direction of the reflectarray. This process is repeated in all directions to produce a two-dimensional image, and further repeated to create multiple images in a stream. While in this demonstration the amplitude thresholding for positive determination of radar targets is hard coded, in more practical applications it could be determined adaptively. Thresholding of return amplitude to determine the presence of a radar target is a classic detection problem, with a tradeoff between likelihood of false positive and false negative. In addition to amplitude thresholding, the imaging radar has range gating applied to filter out targets closer than a minimum range or further than a maximum range. The low range gating serves to filter out false targets arising from phase noise, amplitude noise, Tx-Rx leakage and other low frequency components which could produce false returns. The high range gating serves to eliminate false returns from multipath effects in the cluttered test environment. In addition, more advanced image

processing algorithms such as clustering and Constant False Alarm Rate (CFAR) could be applied. In this imaging demonstration, the performance-enhancing algorithms for squint mitigation and sidelobe reduction described in Chapter 5 are not applied.

The software pipeline is vectorized and optimized for speed. While signals from the current row of pixels is being processed, signal acquisition and integration is happening in parallel for the subsequent row of pixels. A 2017 Dell XPS 13 laptop is used for signal processing, with a dual-core Intel Core i7-7560 CPU. The per-row RF integration time is 1350 ms (15 ms per pixel). The time to transmit IF signal from digitizer to PC is limited by PC memory bandwidth constraints to ˜2000 ms per row, limiting the framerate in this implementation to ˜300 seconds per frame for a 90x90 px image. However, with more modern hardware or on-chip integrated signal processing, the framerate of 121.5 seconds per frame is possible with the given THz hardware. Higher power THz sources, reduction in reflectarray losses or a more sensitive receiver could further improve this limitation. There exist multiple opportunities to achieve multiple orders of magnitude increase in reflectarray losses and therefore frame rate. Performance tradeoffs, such as reducing the maximum range of the radar scene or image resolution could further increase frame rate. The code to implement the above imaging can be found at https://github.com/nathan554/THz_Reflectarray.

6.3. Radar Modulation Techniques

As described in Chapter 3, there is a significant performance degradation in the reflectarray's radiation pattern due to undesired reflections of THz waves from passive structures surrounding the reflectarray. This is exacerbated by the low aperture efficiency and the high signal losses in the reflectarray itself which significantly attenuate the beamformed signal, despite the polarity-flipping nature of the reflectarray. As described in Chapter 3, a BPSK-like modulation technique was introduced to separate in frequency the desired beamformed signal from the

118
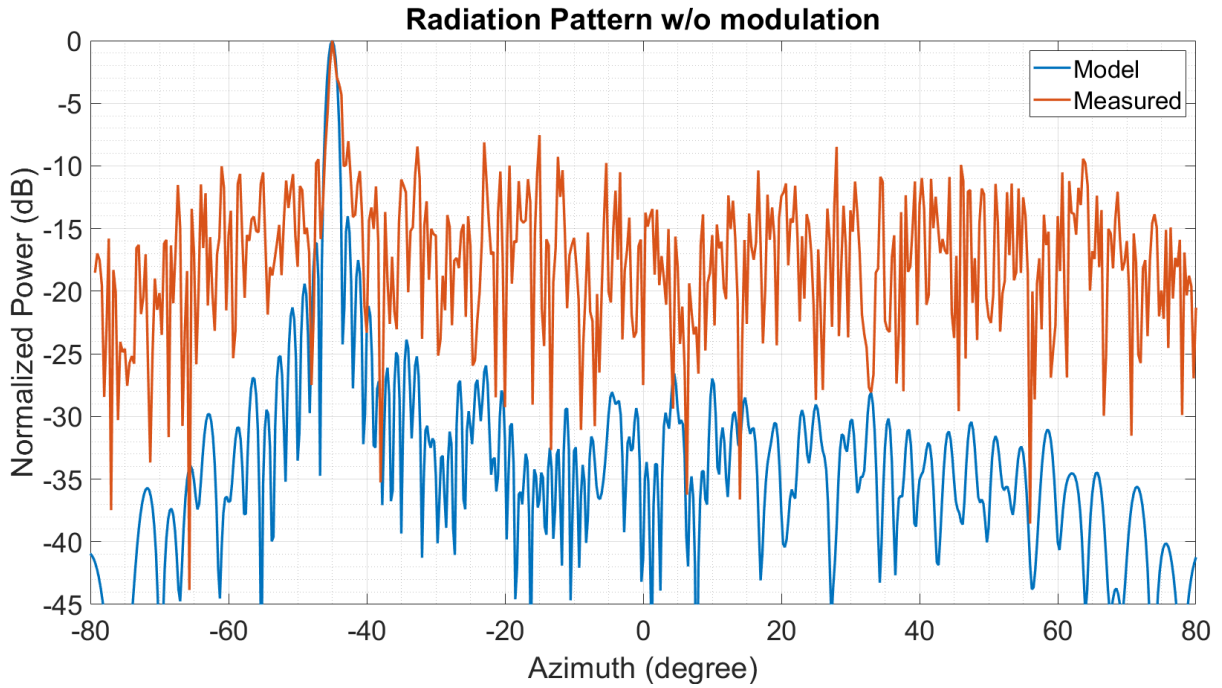
Figure 6-5. Radiation pattern showing degradation of performance in the absence of modulation.

reflectarray from the undesired reflections from passive structures, which underwent no modulation. To illustrate the necessity of this BPSK-like modulation scheme, Figure 6-5 depicts a measured radiation pattern of the reflectarray without the BPSK modulation. This pattern was measured using the testbench described in Chapter 3, except with no modulation during measurement. A comparison to modeled reflectarray radiation pattern is also depicted. As can be seen, the apparent noise floor of the radiation pattern is much higher than expected, due to the inability to distinguish the desired reflections from the undesired ones. In essence, the received power is a superposition of the desired beamformed THz power and the undesired passive reflected power, resulting in an effective noise floor which is approximately 18dB higher, a corresponding reduction in directivity, and a corresponding increase in clutter in the resulting radar image. Therefore, there exists the need to eliminate the effect of these undesired reflections in the radar imaging application.

In order to address the above issues, a BPSK-like modulation scheme similar to the one described in Chapter 3 is introduced and applied here, in the context of radar

119
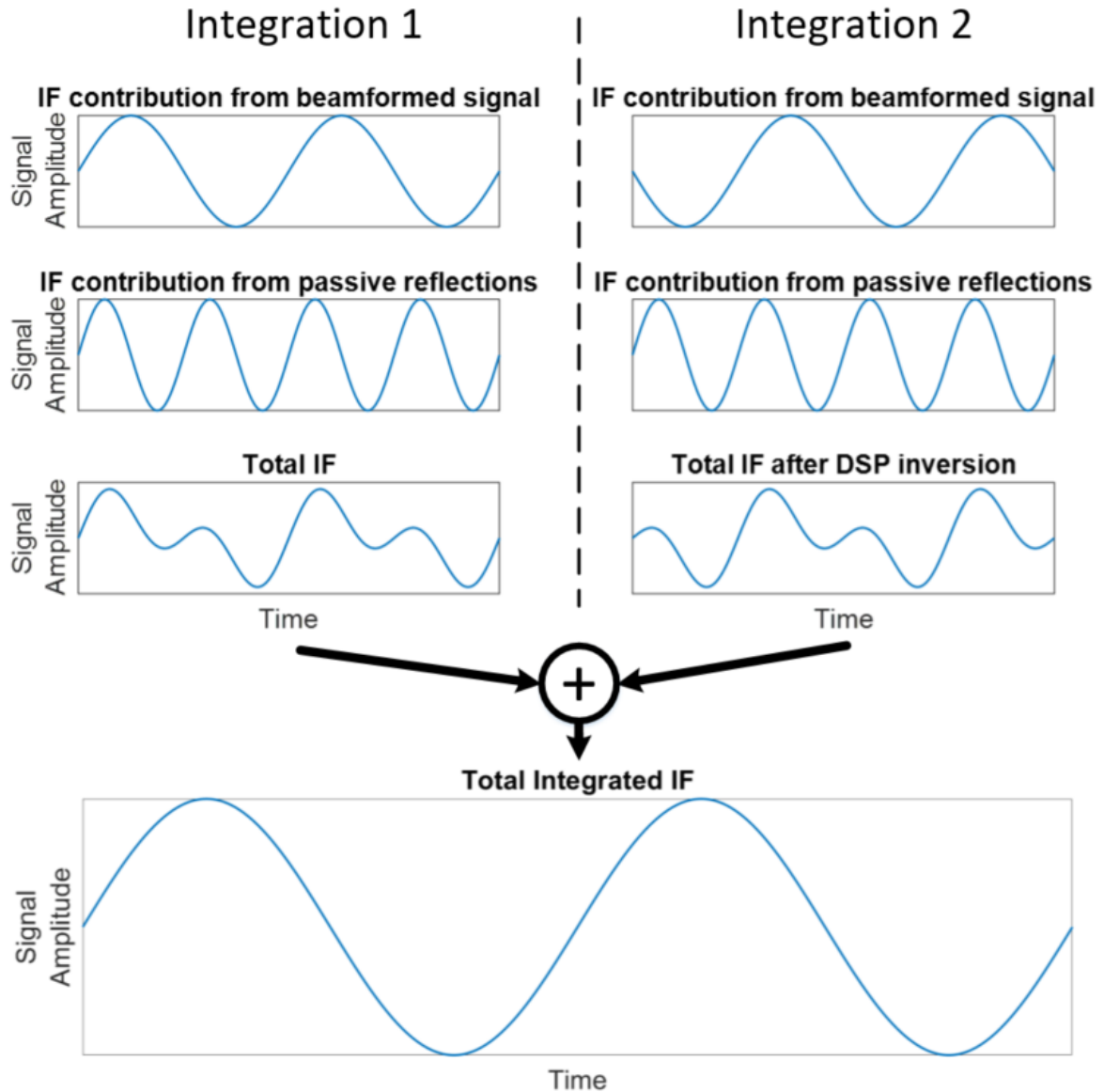
Figure 6-6. Conceptual depiction of BPSK-like modulation scheme.

imaging. A conceptual depiction of the scheme can be seen in Figure 6-6, which depicts the scheme for only two integrations of a pixel in the radar imager. However, it can be generalized to any non-zero even number of integrations. In this modulation scheme, one sample of IF signal is taken for a single integration (labeled integration 1) with the beam pointed in a certain direction. In the subsequent integration (labeled integration 2), the reflectarray is inverted in its programmed phases, such that all phase shifters set to "0 degrees" are flipped to "180 degrees" and vice-versa.

This has the effect of maintaining the radiation pattern's magnitude, while flipping its phase by 180 degrees. Ignoring system nonlinearities, the received IF signal is a linear combination of the reflectarray's response at varying angles, weighted by time-varying radiation pattern, and the undesired reflection's response at varying angles, weighted by it's (unknown but fixed) radiation pattern. Therefore, the effect of inverting the reflectarray's phases in the second integration is that the contribution to the IF signal arising from the reflectarray's beamformed signal is inverted, while the undesired contribution to the IF signal arising from the undesired reflections from passive structures is identical to that in the first integration. In DSP post-processing, the IF signal from the second integration is inverted and summed with the first integration. By applying a double inversion to the desired signal (once through the reflectarray and once through DSP post processing) and a single inversion to the undesired signal (once through post processing), the contribution to radar response from the undesired passive reflections is eliminated.

While not fundamentally necessary for the successful application of the approaches introduced in this Thesis, given the specifics of the system implemented here, the modulation scheme described above is a necessary component of the imaging radar demonstration. However, also due to the specifics in the described implementation, it introduces a number of issues and challenges. The design decision of shift register-based memory in lieu of SRAM-based memory was due to tool limitations, however it limits the amount of available memory, constrains beam states to cyclical patterns (rather than random accesses in the case of SRAM), and limits the speed at which the array can be programmed. The array's programming takes approximately ten minutes due to testbench limitations which further limit programming speed. As a result, it is impractical to allow for the array to be reprogrammed with phase states in an imaging radar application due to its severe time cost. As a result, all phase states for a desired imaging application must fit within the ~81k bits available per antenna. Assuming a 90 x 90 pixel image, 81k available bits of memory allows for ten bits of phase state storage per pixel in the resulting image. Prior to the introduction of the BPSK modulation scheme described above, a single pixel in the

radar imager only consumes a single bit of phase state storage, regardless of the number of integrations per pixel.

With the introduction of the BPSK-like modulation described here, each pixel in the radar image requires a minimum of two bits: one bit for the desired phase plus a second bit for that bit's inverted value. In such a scheme, N total integrations would be achieved by collecting N/2 integrations with the reflectarray set to the first bit, then N integrations collected with the reflectarray set to the second bit, then summing the integrations and performing required calculations to process the resulting IF signal. However, it was found empirically that this scheme has poor performance, due to drift over time in either the THz source or receiver's performance characteristics, when the modulation scheme is implemented in the way described above the two components of the modulation are sufficiently different that cancellation of the undesired IF components are not achieved. This drift is likely due to noise in bias circuitry or thermal effects, and empirically appears to occur on a time scale of approximately 10ms.

An alternative to the THz drift issue described above is to alternate reflectarray phase and IF inversion in every integration. However, with the hundreds of integrations required for adequate SNR, given the implementation details and memory limitations of the system described in this Thesis, such a scheme is not possible due to the number of bits required. Therefore, an intermediate approach is taken to mitigate the THz drift issue while fitting within allowable memory budget. In the approach taken here, the bit flipping for the modulation occurs every 100 integrations. As a result, for 1000 total integrations only ten bits are needed, fitting within the memory budget for a 90 x 90 pixel imager. It was found empirically that in the ~1ms time scale between steps in the modulation sequence, drift in the THz system was low enough that successful cancellation of the undesired signal was achieved. Therefore, this approach allows the BPSK-like modulation to be used effectively while still achieving system level parameters of image resolution and SNR. As a final note, improvements on the system described here would use SRAM-based memory for a ~10x increase in available memory, reducing the memory constraints.

In addition, it could include either random access or simple logic for a built-in way to apply BPSK modulation without consuming additional memory bits. Finally, improved RF losses would reduce the reflectarray's losses, reducing the effect of the undesired reflections and therefore the need for this modulation scheme. Regardless, in the implementation described here the BPSK-like methods are effective at achieving adequate imaging performance from the reflectarray system.

6.4 Imaging Radar Performance

The imaging radar's performance is described by a tradeoff of SNR and integration time, as is typical of radars, where integration time determines maximum possible frame rate. In the system parameters chosen above, the radar has a maximum range of 7 meters, as limited by Nyquist criteria on the digital sampler. Due to limitations in the digital bandwidth of the sampler, chirp rate and IF frequency range reduced as much as possible to reduce sample rate. However, the radar has been demonstrated to a maximum range of 18 meters, as limited by availability of a suitable test range. The radar was characterized by employing the use of copper
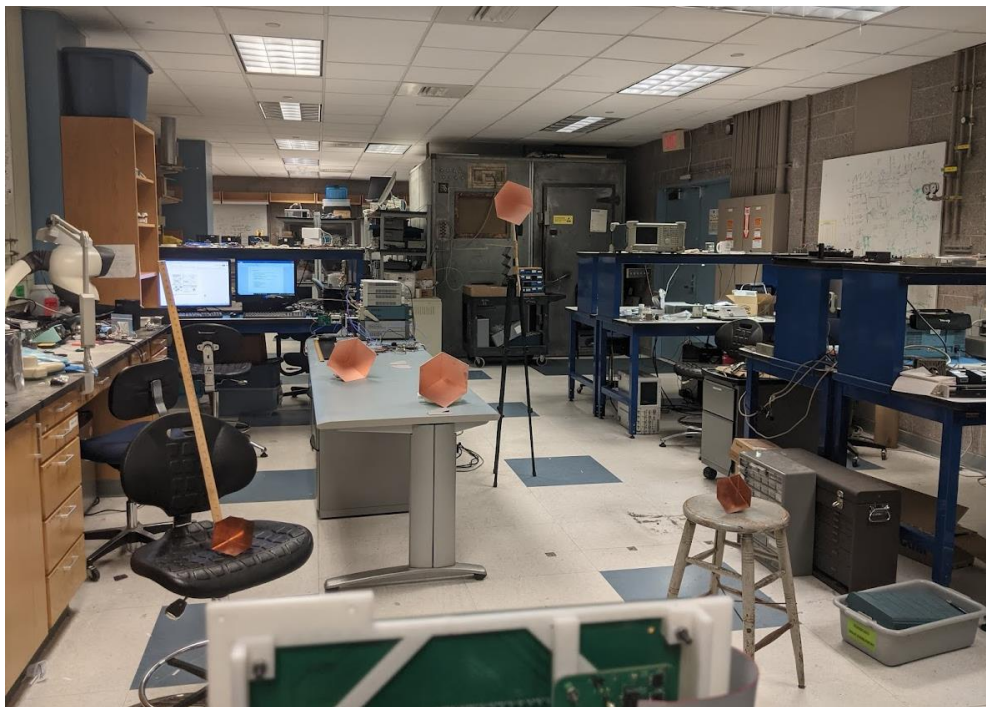
Figure 6-7. Example radar scene with copper corner reflectors as radar targets.
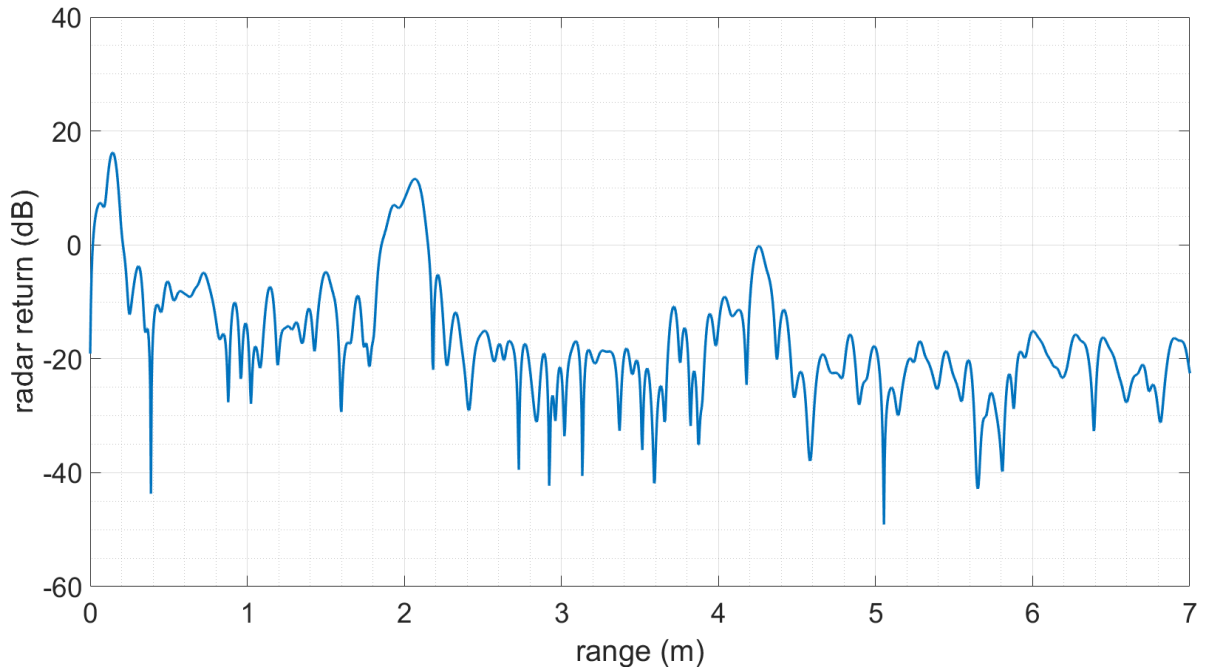
Figure 6-8. Example range plot of a single pixel with a corner reflector target.

corner reflector targets, as seen in Figure 6-7. In this configuration, an example range plot of a single pixel of the radar imager can be seen in Figure 6-8, exhibiting a Signal to Noise Ratio (SNR) of approximately 30 dB.

A point spread function (PSF) of an imager characterizes the imager's response to a single point target, analogous to a two-dimensional impulse response. A radar image of the above scene, with a single corner reflector target in the middle of the scene, serves as a measure of the point spread function. This point spread function image can be seen in Figure 6-9, which displays only the amplitude of the radar return, at the range of maximum return. The PSF exhibits undesired false returns aligned with the vertical axis, likely arising from imperfect calibration in the H-plane, as exhibited in radiation pattern measurements shown in Chapter 3.
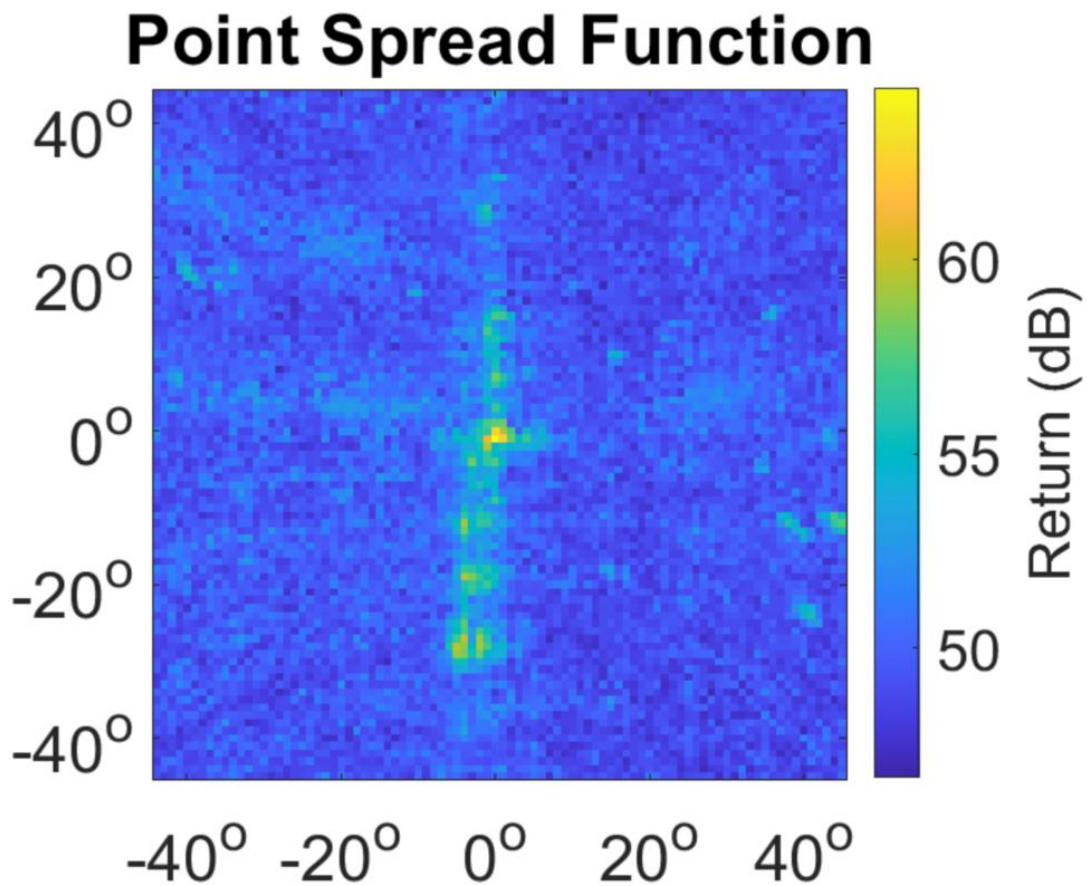
Figure 6-9. Point Spread Function of radar imager with target at 2 meters.

6.5. Imaging Results

In order to demonstrate imaging performance, the radar imager was exercised in a number of radar scenes with varying configurations of corner reflector radar targets, with imaging in both 2 dimensions and 3 dimensions.

In the first imaging scenario, the imager is configured to capture a 1-dimensional 1x80 image, with a beam sweeping in the horizontal axis in one degree increments from [-40 40] degrees. The radar scene with targets and the resulting radar image, in plan view, can be seen in Figure 6-10. In this scene, a number of targets are placed within 3 degrees of each other in order to exercise the narrow beam functionality of the radar. In the resulting image, each circle represents one pixel, arising from the
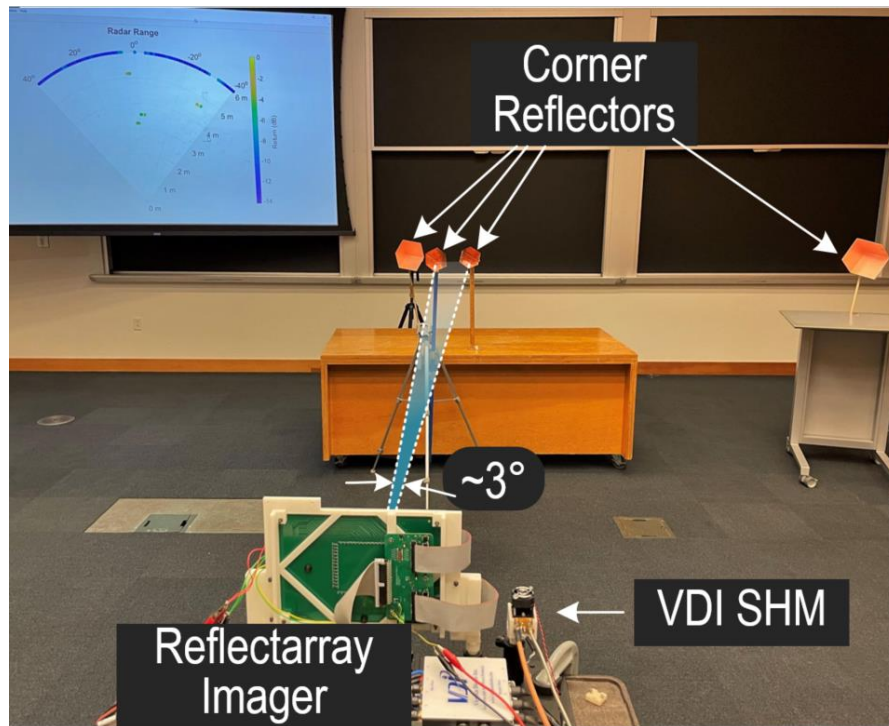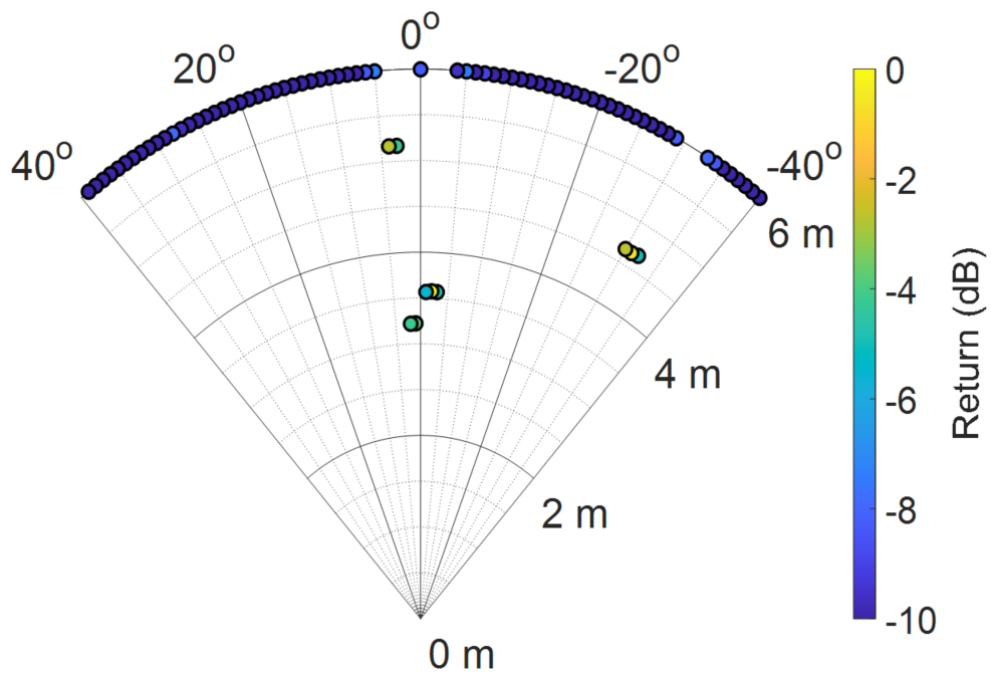
Figure 6-10. (top) Example radar scene with corner reflectors for 1 dimensional imaging radar demonstration. (bottom) corresponding radar image, in plan view.

reflectarray steering the 1 degree wide beam in a certain direction. The radar successfully distinguishes nearby targets, highlighting the high resolution nature of
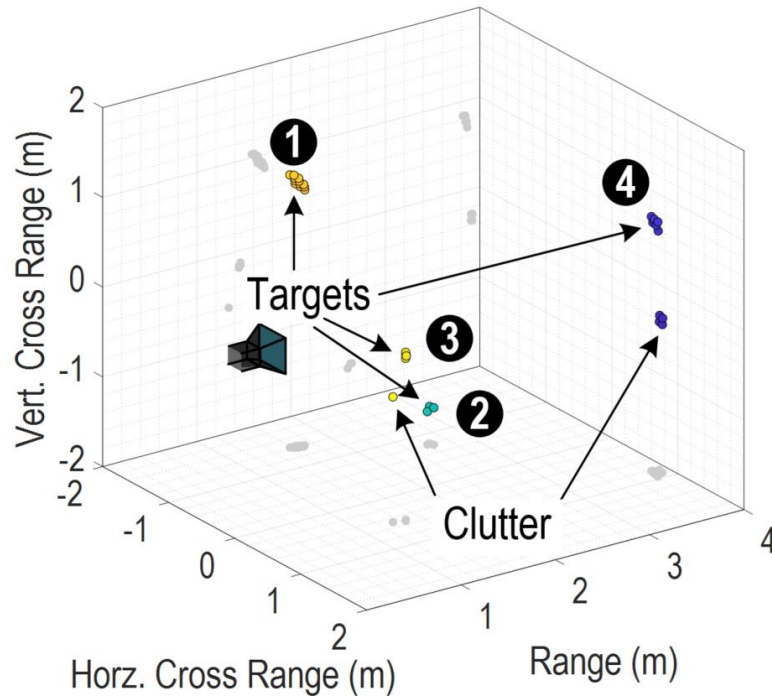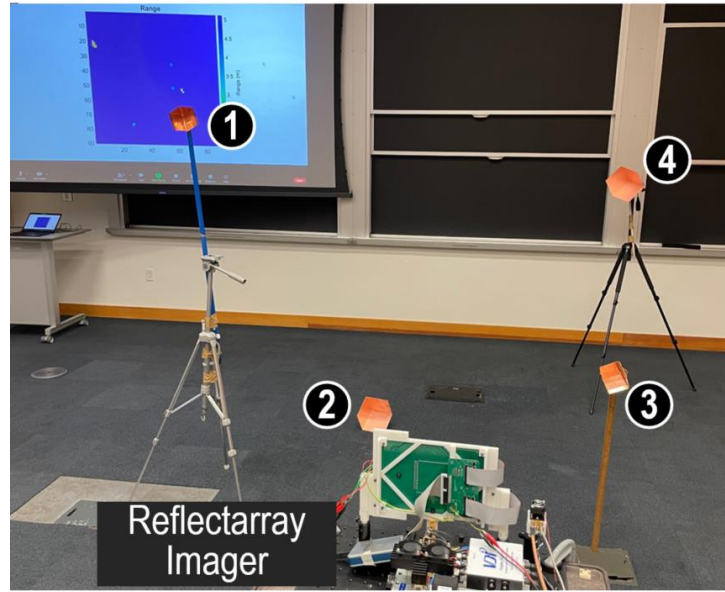
Figure 6-11. (top) Example radar scene with corner reflectors for 2 dimensional imaging radar demonstration. (bottom) corresponding radar image, in 3D view.

the imager.

In a second imaging scenario, a number of corner reflector targets are scattered in three dimensions around a scene, as seen in Figure 6-11, where radar targets are
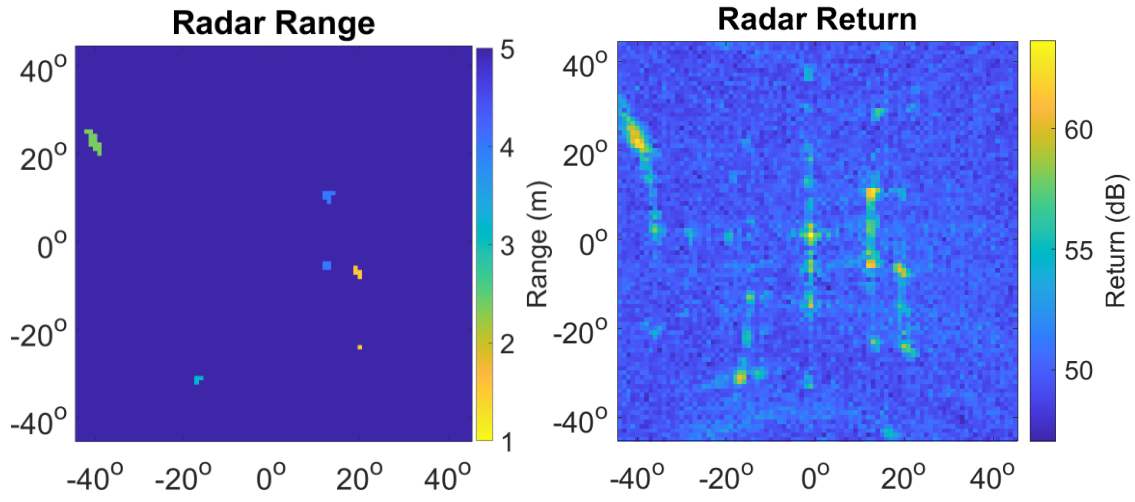
Figure 6-12. (left) Radar range image with color mapped to range. (right) Corresponding image of radar return amplitude. Note: vertical line aligned with 0° is due to reflections from back wall in radar test scene, which has been filtered out by range gating.

annotated with numbers for comparison to the radar image. The reflectarray imager is configured to sweep a one-degree wide beam in one degree increments over a viewing range of [-45 45] degrees in both axes, producing a 90 x 90 pixel 3 dimensional image. The resulting radar image is displayed in two ways. In Figure 6-11, a 3-dimensional view shows the physical location of objects in the scene. Figure 6-12 depicts the same data with range mapped to color in the left image, while the amplitude of the resulting radar image can be seen on the right. As discussed previously, a small number of false targets appear in the resulting images as clutter, likely arising from imperfect calibration in the imager's H-plane beam steering, leading to sidelobes and therefore false returns. The amplitude image seen in Figure 6-12 additionally includes a vertical line at 0 degrees, arising from reflections from the back wall in the radar test scene which are filtered out by amplitude gating.

In a third and final imaging scenario, a more real-world scene is used for imaging. Seen in Figure 6-13, the scene contains metal elevator doors and other structures, which are labeled for comparison to the resulting radar image. The resulting image
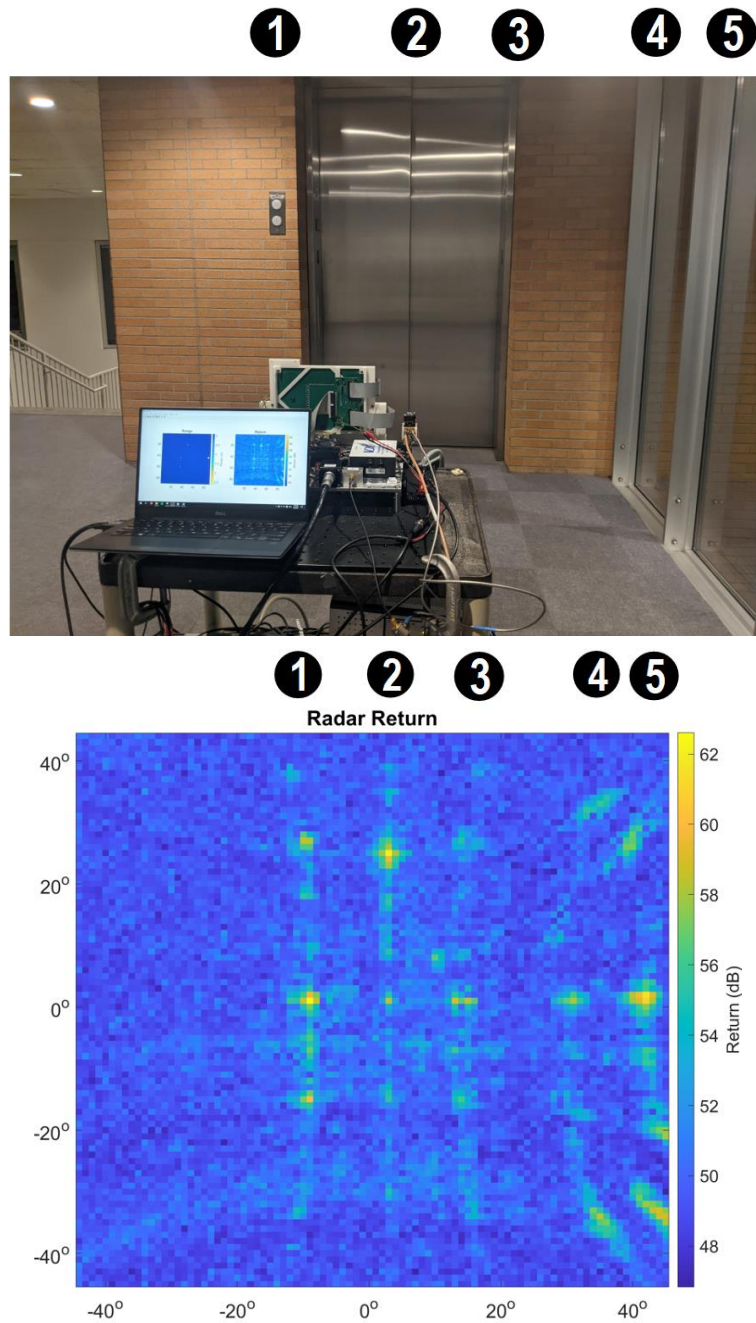
Figure 6-13. (top) Example test scene, with features numbered for correspondence. (bottom) corresponding amplitude image, with features numbered for correspondence.

is seen in Figure 6-13, which shows the amplitude of radar returns. Vertically aligned structures in the scene can be clearly distinguished.

In summary, this chapter demonstrates the utility of the high directivity reconfigurable THz reflectarray in radar imaging applications. By combining the

129

previously described reflectarray with a Terahertz transmitter and receiver, a narrow beam is swept across a scene with radar samples taken at each point to produce a 3 dimensional THz radar image. This proof of concept demonstrates the utility of the THz reflectarray approach described in this Thesis for solid state imaging applications, and any application requiring a high directivity electronically steerable THz beam.

Chapter 7

Summary and Future Directions

7.1. Thesis Summary

This thesis opens with a discussion on Terahertz systems and their advantages in a number of potential applications, with a focus on imaging. It describes THz antenna arrays and their potential for high performance, rapid electronic beam steering in a system that is smaller in size, weight and power, with the ability to penetrate certain dielectric objects due to the nature of Terahertz waves. It introduces Terahertz imaging radar and the need for narrow Terahertz beams for high image resolution. It discusses existing methods, mechanical and electronic, to steer Terahertz waves and their shortcomings with a number of examples drawn from existing works. In short, the existing solutions are limited by four primary challenges in building high angular resolution Terahertz antenna arrays. In short, these challenges include the losses of distributing Terahertz energy over large aperture sizes, scalability to the aperture sizes required for narrow beam generation, Terahertz phase shifters that are low-loss, low-power, and small area, and digital control over the large number of antenna elements required.

The thesis proceeds to introduce the design and fabrication of a 98 x 98 antenna array operating at 265GHz, the highest directivity and sharpest beam reconfigurable antenna array in the Terahertz range. The array's design includes elements to mitigate or eliminate the challenges in existing Terahertz antenna arrays. Terahertz distribution losses are mitigated by the adoption of a reflectarray architecture, where RF energy is distributed spatially by a feed antenna, which radiates quasi-optically the RF energy onto the antenna array, and each antenna receives, phase shifts, and

re-radiates the energy. Scalability designs are addressed with a chip architecture which is scalable and allows the chip to be tiled in arbitrarily-sized arrays to create large antenna arrays. The chip design allows for addressing on a chip-level, allowing malfunctioning chips to be bypassed with minimal performance loss. Challenges in Terahertz phase shifting are achieved by the introduction of a one-bit phase shifter which uses two MOSFET switches and exploits antenna symmetry to create a phase shifter which is a precise phase value, consumes no DC power, has low Terahertz loss, consumes negligible chip area, and is reciprocal, allowing it's use in monostatic radar applications with performance enhancement. Challenges in control of large-scale antenna arrays are addressed by the introduction of on-chip memory, where a sequence of phase states for each antenna are pre-computed and loaded onto the array at startup, allowing rapid switching between subsequent states.

The 98 x 98 antenna array operates at 265GHz and consists of a 14 x 14 tiling of 22nm FinFET chips, each measuring 4 x 4 mm^2 and containing 7 x 7 on-chip patch antennas. The 196 chips are stitched with approximately 2500 wirebonds. The antennas are spaced at nearly 0.5λ, where λ is the wavelength at the operating frequency of 265GHz. The antenna array consumes approximately 170mA at VDD=1V, nearly entirely from leakage in the shift register memory. Each antenna contains nearly 82k bits of shift register-based memory for storage of precomputed beam states. The unit cell antenna is implemented in the ultra-thick C4 layer for efficiency, with two MOSFET phase shifter producing a perfect 180 degrees with no DC power consumption and 3dB of THz loss. A low-profile feed antenna at a distance of 5.8cm provides the THz energy.

The array is measured at 265GHz to experimentally demonstrate a 1 x 1 degree wide beam with 42dBi of directivity at boresight, and the experimentally-demonstrated ability to electronically steer a beam over a [-60 +60] degree window in both axes. Measured radiation patterns align with analytical and numerical models. Leveraging in-antenna memory, two performance-enhancing algorithms were demonstrated experimentally. The first, a beam-squint mitigation algorithm for wideband FMCW radars, uses the internal memory to update phase settings mid-chirp to account for

varying frequency and correct for beam squint, improving effective resolution in imaging applications. The second, an adaptation of an existing sidelobe mitigation technique, improves upon existing hardware schemes and uses the built-in memory of the array to improve sidelobe performance by 4.6 dB in imaging radar applications by exploiting incoherence in quantization sidelobes in successive integrations.

The principles discussed and demonstrated in this work were demonstrated in a radar imaging application capable of producing both 2-dimensional and 3-dimensional radar images in real-world applications. A number of imaging exercises are demonstrated of both staged radar target scenes and real-world scenes to prove out the narrow beamwidth and high resolution nature of the radar imager.

Similar principles were applied in the development of a true one-bit phased array, capable of producing electronically beam-steered radiation of 265GHz energy without external feed antenna. Such a solution provides lower overall system volume, while trading off some of the performance benefits of the reflectarray architecture.

By utilizing the architectural, circuit-level, algorithmic and statistical methods presented here, this work demonstrates the sharpest beam and highest directivity beam-steerable Terahertz antenna array reported to date. Through 2-dimensional and 3-dimensional imaging demonstrations, this work shows the applicability of antenna arrays for Terahertz imaging applications as a more practical alternative to existing mechanical methods, and opens the door to a number of other real-world Terahertz use cases.

7.2. Informal Lessons Learned

This section, written informally, captures lessons learned during the research performed in this Thesis which are not captured elsewhere. This should serve as a guide for future researchers and engineers who pursue related work.

Significant challenges exist in the design and construction of the testbench for the reflectarray's radiation pattern. With a narrow one degree wide beam, extreme levels of precision are required when building mechanical fixtures for both feed structures

and measurement. The 3d printed supports used in this work for supporting the reflectarray and its feed included features to ensure the reflectarray is centered over the center of rotation of the rotation stage, which is eased by aligning the reflectarray in the center of the PCB (this was not done in this work, which added complications in fixture design). Furthermore, special care is required in aligning feed structures with the reflectarray, as any misalignment results in a static offset in beam direction, which complicates accurate placement of the receiver in radiation pattern measurements. In this work, 3d-printed fixtures were used to this end. In addition, with a wavelength of approximately 1mm, flexing and vibrations in the test structure can have meaningful effects on radiation pattern. Extra care is required in the fixture design to maximize rigidity and minimize vibrations during rotation.

On a higher testbench level, the reflectarray and feed were placed on an aluminum optical breadboard which was subsequently placed on a rotation stage. For cost reasons, a manual rotation stage (which was already in-hand in the lab) was paired with a stepper motor for computer control, with a motor coupling between the two, and an off-the-shelf motor driver controlled by an Arduino via PC. The heavy weight of the optical breadboard and it's cantilevered offset from the center of rotation of the rotation stage required a high-torque stepper motor. Many iterations were performed on this assembly, resulting in a planetary-geared stepper motor which provided both the torque and the fine step requirements. However, the maximum stepping rate of this limited the rate at which the radiation pattern can be measured to approximately 15 minutes for a [-90 +90] sweep, time which adds up over thousands of test sweeps. A higher torque stepper motor with lower gear ratio would mitigate this issue. In addition, the coupling between the stepper motor and rotation stage encountered small amounts of slip, resulting in minute angle errors of up to 5 degrees over a 180 degree sweep, which required a time-consuming angle calibration after each sweep. This could be addressed or mitigated by improved coupling, rotation stage, motor, or the inclusion of laser pointing or servo motors for closed-loop control.

Another significant challenge in the testbench is in the alignment of the receiver's height in Z to capture the one degree wide mainlobe of the radiation pattern. This is challenging due to the uncertainty in exact mainlobe direction due to errors in feed geometry and rotation stage angle. An iterative process was taken of programming the reflectarray to point the mainlobe towards the receiver, rotating the rotation stage, and manually moving and rotating the receiver until maximum received power was achieved. Although every effort was taken to mitigate these issues, higher precision in feed fixturing and rotation stage angle would ease testing.

In the testing, a distance of 1.6 meters is outside of the predicted reactive near field distance of ~0.4 meters but well within the predicted far field distance of ~11m. Despite this, both simulations and measurements showed that far-field assumptions can be made at a distance of 1.6m with little error. Efforts were taken to reduce reflections from nearby structures and their corruption of radiation pattern measurements by placing the test setup on top of a lab bench. Informal experiments of placing terahertz absorbing material on the bench itself showed that reflections off the bench did not contribute meaningfully to the radiation pattern measurement. Regardless, Terahertz absorber was used to mask the reflective optical breadboard used to align the rotation stage and receiver.

A number of lessons were learned on the system level design and assembly of the array. The 3d printed structure to protect the array was critical for protecting the array during storage and shipping, and protecting it from dust. Its height should be minimized to maximize viewing angle of the array. In addition, the spacing of the chips in the array is critical; the chip spacing must be such that an equal antenna spacing is maintained between chips. Otherwise, a periodicity in phase error causes significant coherent sidelobes. The dies size often varies from that of the design etch ring by both a static amount plus manufacturing variability which must be taken into account. Early concerns existed about coupling from wirebonds to nearby antennas and the associated angle-dependent periodic phase error, this effect was found to be negligible. The C4 layer in this process is intended for solder balls for flip-chip assembly and not wirebonding. To ease wirebonding, it is critical to remove

copper oxide layers by a formic acid reflow process. Despite this, wedge bonding was found to be extremely difficult in MIT labs, with the excessive ultrasonic power required often damaging fragile chip structures. The automated wirebonding process performed at Intel initially resulted in a number of failures of both open circuits and short circuits, which resulted in an iterative assembly-test procedure being developed to identify failures during assembly. Thermal cameras were used to spot locations of short circuited connections.

Due to the large number of wirebonds between chip and PCB, for high reliability an ENEPIG finish was used on the PCB. On the PCB, the absolute minimum amount of circuits was placed on the board containing the reflectarray chips given the high-risk and one-time nature of the reflectarray assembly. This led to a design with a second control PCB, with a large number of connections between the two. This could be significantly reduced in future more mature versions leading to a large performance improvement. The limiting factor in the programming time of the array was inductance in the IDC connections between the two circuit boards, which degraded signal integrity, leading to a maximum SPI programming speed of just 2.5MHz, resulting in a full-array programming time of 8-10 minutes. The IDC connection was chosen for its reliability and simplicity; future versions could use (for example) FFC or FPC connections. In addition, given the assembly challenges it's likely that a more reasonable approach uses PCBs with smaller subarrays of reflectors, and the PCBs themselves are tiled. This necessitates a PCB design that maintains equal antenna spacing between PCBs, a significant challenge. It also would likely require a shift to flip-chip assembly due to challenges wirebonding between multiple PCBs.

Finally, lessons learned in the chip design itself. A significant challenge in the chip and system level design was power integrity arising from the shift register memory's impulsive current profile, and the large power supply impedance seen by the chips at the center of the array. Significant modeling was performed to understand this with conservative measures taken in on-chip decoupling and shift register delays. Many of these issues would be eliminated in an SRAM-based design with much lower

current consumption, but it's believed that fusing current in the array's outermost VDD bond wires would be the second limiting factor in switching speed after connector inductance. In addition, ringing in bondwires and on-chip capacitance during a shift register switching event was of concern in the possibility of exceeding supply voltage limits, this was found to not be an issue.

7.3. Future Directions

A number of opportunities exist for the advancement of this research, both in terms of increasing the practicality, cost and performance of existing applications as well as opening doors to potential new applications.

In the existing design, the design decision to use shift registers is not an optimal one, and was driven by process limitations which existed at the time of chip development. A vastly superior design would replace shift register memory with Static RAM (SRAM) based memory. Not only would this improve memory density by approximately 10x, it would reduce power consumption to the low mW level. This allows not only more memory headroom for additional beam states and more advanced performance enhancing algorithms, it also improves array fabrication yield, with failed transistors only affecting individual memory addresses rather than entire sections of a given chip.

Given the above shift to SRAM based designs, the power consumption drops to the low mW (or even potentially sub mW) level. This opens the door for energy harvesting as a power source, with potential sources such as far-field THz radiation, acoustic energy, photovoltaic, vibrational and others. Self-powered reconfigurable Terahertz reflectors warrant additional exploration for future communications applications.

A number of opportunities exist for the improvement of loss and therefore SNR in THz applications. For example, the integration of a THz transceiver at the feed point and improvement of aperture efficiency from that reported in this work would

improve power by approximately 10dB in a bistatic radar application. Improvement in on-chip patch antenna radiation efficiency is possible and an essential component of SNR improvement. Given existing limits in Terahertz sources and receivers, improvement of end to end reflectarray losses is necessary to fully exploit the benefits of a monostatic radar design and the associated improvements in directivity, given that in a monostatic radar design the Terahertz energy passes through the reflectarray twice.

Given the large silicon area and advanced process node involved in this work, cost becomes a limiting factor in many applications; there exists an opportunity to reduce cost. For example, much of the silicon area between antennas is used for memory which may be superfluous; by eliminating some of this area and reducing total silicon area enormous cost reductions can be achieved. Such an approach with miniscule single-antenna dies may require alternative assembly methods similar to those used in microLED displays.

A significant opportunity for future work exists in the exploration of packaging for CMOS-based Terahertz antenna arrays. The wirebond-based approach used here is costly, time-consuming, error-prone and comes with a performance cost by interfering with antenna radiation patterns in poorly-controlled ways. There exist opportunities to explore alternative packaging, such as flip-chip approaches. Flip-chip approaches would reduce cost by enabling existing pick-and-place technology, but would require further exploration into PCB dielectric materials and their effect on Terahertz radiation, plus the existence of a superstrate and its effect on radiation pattern with surface waves, resonances and near-field coupling. Alternatively, Through-Silicon-Via approaches would allow flip-chip-like PCB assembly methods with I/O connections on the bottom of the chips and antennas on the top of chips, separating them physically and allowing for optimal performance in both I/O and RF aspects. Cost aside, it is likely this is the optimal architecture for large scale CMOS-based antenna arrays.

An alternative approach for cost reduction and simplification of array assembly, with potential performance benefits, is to use single-wafer techniques, as has been demonstrated in the context of digital systems [138]. In this approach, adjacent reticles in a single wafer are connected to create a single wafer-size antenna array. Not only does it avoid challenges in assembly, it also improves RF performance by eliminating variability in die-die spacing, the associated periodicity in phase error and the associated sidelobes in radiation pattern.

Being a CMOS-based approach, this work leverages the scaling and integration benefits of CMOS processes. In this work, these advantages are applied towards local memory for each antenna, for the storage of beam states. However, this chip area could alternatively be applied towards local computation. Such computation could include system modeling, calculation of locations of desired peaks and nulls in radiation patterns, security algorithms, or otherwise in cognitive radio applications. Such approaches could give CMOS based Terahertz antenna arrays an enormous performance advantage in future applications in communications and otherwise.

While the use of CMOS logic can enhance security of communications links using cryptographic methods, there exists an opportunity to use Terahertz reflectarrays to further enhance security by using physical methods such as Orthogonal Angular Momentum (OAM). Such methods have been demonstrated at lower frequencies and could be enhanced by the small physical sizes and large number of antennas possible in Terahertz systems. The use of Terahertz antenna arrays has the potential in a number of communications applications, including future 6G consumer applications, internet backhaul, point to point links and space-based applications. Reflectarrays are particularly applicable to space applications due to their flat shape, making it possible to easily unfold and deploy such systems [139], [140]. The possibility of using far field sidelobe mitigation methods, as discussed in Chapter 6, opens the door to reconfigurable reflectors for non-line of sight and cognitive radio applications as discussed in Chapter 6. With the increasing F_t of transistors, there is the additional possibility of the construction of active Terahertz reflectarrays, where a reflected signal is amplified by active electronics within the reflector.

The technologies developed in this Thesis could be readily adapted towards the application of low-cost focal plane arrays. The antennas and chip tiling scheme described in Chapter 3, combined with the Terahertz detector in Chapter 4 (or similar) could be combined to produce arbitrarily sized incoherent imagers. Combined with additional circuits integrated into the die, there is potential for low-cost fully integrated Terahertz focal plane arrays.

This work's choice to implement polarity-flipping antennas was driven by the desire to mitigate degradation in radiation pattern due to undesired reflections in supporting structures around the antenna array. Such reflections contribute to aperture efficiency losses and are caused by spillover of feed energy over the edges of the array. There exists opportunity to mitigate this through the use of low-cost metamaterial-type absorber approaches on the antenna array's printed circuit board, using (for example) PCB traces as absorptive dipole antennas to absorb spillover energy and mitigate the undesired reflections' performance degradation. Such approaches could improve performance, however they fail to recover the energy lost in the energy spillover and decrease in gain due to nonuniform illumination. Typical reflectarray designs assume single power-cosine feed antennas with well-known tradeoffs in system-level efficiency [43]; there exist opportunities to break these tradeoffs through the synthesis of more complex feed structures using metamaterial approaches or multiple coherent feeds to break these tradeoffs and both improve aperture efficiency and reduce undesired reflections.

Given the analogies between antenna arrays and digital to analog systems in terms of sampling theory and techniques such as delta-sigma modulation, there exists opportunity in the exploration of antenna arrays with more dense spacing than the typical limit of half lambda spacing. This has been shown to result in systems capable of producing more complex electromagnetic wavefront profiles and also further mitigate quantization noise in a manner similar to delta sigma samplers [97], [141]. There exist complex tradeoffs with antenna mutual coupling and more generally tradeoffs in choice of antenna array frequency, memory availability, packaging challenges, performance and cost.

Finally, more speculative future directions. Given the long history of reflector antennas in a multitude of frequency ranges and applications, it is worth exploring analogous existing reflector antennas for inspiration from adjacent fields. One example is the Beam Waveguide Antenna, which uses multiple reflectors to more efficiently incorporate antenna feed, among other advantages. Challenges exist in the potential implementation of a BWGA-style Terahertz reflectarray such as system alignment and the fabrication of the subreflector, however it has the potential for enhanced performance and additional design degrees of freedom. An additional speculative future direction improves directivity by further increasing aperture size. MIMO approaches are well known to synthesize large virtual apertures, but their drawbacks are well documented. This work uses a large physical aperture to produce a narrow beam, sidestepping the issues with MIMO techniques. However, it is possible that a blend of the two would yield synergistic performance benefits with ever-increasing directivity, potentially by combining multiple reflectarrays, each with their own transceiver, while coordinating multiple of these transceivers in a MIMO-style approach. Finally, exploring digital beam shaping algorithms is a vast and largely unexplored field in this context, especially given the possibility of expanded memory and local computation circuits. This work demonstrated sidelobe mitigation, and beam squint mitigation. However, more generalized time-varying phase sequences have the potential to provide further enhanced performance. Co-optimization of multiple sets of time-variant phases using algorithms such as simulated annealing provide the opportunity to further enhance performance.

References

[1]   H. Guerboukha, K. Nallappan, and M. Skorobogatiy, "Toward real-time terahertz imaging," *Adv. Opt. Photonics*, vol. 10, no. 4, p. 843, 2018.

[2]   A. Y. Pawar, D. D. Sonawane, K. B. Erande, and D. V Derle, "Terahertz technology and its applications," *DIT*, vol. 5, no. 2, pp. 157–163, 2013.

[3]   H. A. Hafez *et al.*, "Intense terahertz radiation and their applications," *J. Opt.*, vol. 18, no. 9, 2016.

[4]   K. Delfanazari, R. A. Klemm, H. J. Joyce, D. A. Ritchie, and K. Kadowaki, "and Coherent Terahertz Sources and Sensitive Detectors Based on Layered Superconductors," *Proc. IEEE*, vol. 108, no. 5, 2020.

[5]   M. H. Dahri, M. I. Abbasi, M. H. Jamaluddin, and M. R. Kamarudin, "A Review of High Gain and High Efficiency Reflectarrays for 5G Communications," *IEEE Access*, vol. 6, pp. 5973–5985, 2018.

[6]   M. H. Dahri *et al.*, "Polarization Diversity and Adaptive Beamsteering for 5G Reflectarrays : A Review," *IEEE Access*, vol. 6, pp. 19451–19464, 2018.

[7]   W.-T. Hung, J.-J. Tung, and S.-Y. Chen, "A focusing reflectarray and its application in microwave virus sanitizer," *Radio Sci.*, vol. 49, pp. 890–898, 2014.

[8]   C. Tienda, M. Younis, and P. Laskowski, "Ka-band Reflectarray Antenna System for SAR Applications," *8th Eur. Conf. Antennas Propag. (EuCAP 2014)*, no. EuCAP, pp. 1603–1606, 2014.

[9]   G. Ahmad, T. W. C. Brown, C. I. Underwood, and T. H. Loh, "An investigation of millimeter wave reflectarrays for small satellite platforms," *Acta Astronaut.*, vol. 151, no. June, pp. 475–486, 2018.

[10]   R. E. Hodges, N. Chahat, D. J. Hoppe, and J. D. Vacchione, "A Deployable High-Gain Antenna Bound for Mars," *IEEE Antennas Propag. Mag.*, vol. 59, no. 2, pp. 39–49, 2017.

[11]   R. R. Romanofsky, "Advances in scanning reflectarray antennas based on ferroelectric thin-film phase shifters for deep-space communications," *Proc. IEEE*, vol. 95, no. 10, pp. 1968–1975, 2007.

[12]   H. Gomez-Sousa and J. A. Martinez-Lorenzo, "Modeling and Imaging Security

Threats Using a Single-Frequency Adaptable Reflect-Array," in *2017 IEEE International Symposium on Technologies for Homeland Security (HST)*, 2017, pp. 1–7.

[13] J. J. Maciel, J. F. Slocum, J. K. Smith, and J. Turtle, "MEMS Electronically Steerable Antennas for Fire Control Radars," *IEEE Aerosp. Electron. Syst. Mag.*, vol. 22, no. 11, pp. 17–20, 2007.

[14] B. N. Lyons, E. Entchev, M. K. Crowley, B. N. Lyons, E. Entchev, and M. K. Crowley, "Reflect-array based mm-wave people screening system," vol. 890002, no. May, 2019.

[15] Y. Jiang, B. Deng, Y. Qin, H. Wang, and K. Liu, "A fast terahertz imaging method using sparse rotating array," *Sensors (Switzerland)*, vol. 17, no. 10, 2017.

[16] K. B. Cooper, R. J. Dengler, N. Llombart, A. Talukder, and A. V Panangadan, "Fast , high-resolution terahertz radar imaging at 25 meters," *Proc. SPIE*, vol. 7671, pp. 1–8, 2010.

[17] K. B. Cooper *et al.*, "Penetrating 3-D Imaging at 4- and 25-m Range Using a Submillimeter-Wave Radar," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 12, pp. 2771–2778, 2008.

[18] A. Siligaris *et al.*, "A 278 GHz heterodyne receiver with on-chip antenna for THz imaging in 65 nm CMOS process," *Eur. Solid-State Circuits Conf.*, vol. 2015-Octob, pp. 307–310, 2015.

[19] M. Alonso-delPino, C. Jung-Kubiak, T. J. Reck, N. Llombart, and G. Chattopadhyay, "Beam Scanning of Silicon Lens Antennas Using Integrated Piezo-Motors at Submillimeter Wavelengths," *IEEE Trans. Terahertz Sci. Technol.*, vol. 9, no. 1, 2018.

[20] L. Daniel, D. Phippen, E. Hoare, A. Stove, M. Cherniakov, and M. Gashinova, "Low-THz Radar, Lidar and Optical Imaging through Artificially Generated Fog," in *International Conference on Radar Systems*, 2017, pp. 1–4.

[21] M. Bijelic, T. Gruber, and W. Ritter, "A Benchmark for Lidar Sensors in Fog : Is Detection Breaking Down ?," in *2018 IEEE Intelligent Vehicles Symposium (IV)*, 2018.

[22] B. Baccouche *et al.*, "Three-Dimensional Terahertz Imaging with Sparse Multistatic Line Arrays," *IEEE J. Sel. Top. Quantum Electron.*, vol. 23, no.

4, 2017.

[23] B. Cheng *et al.*, "340-GHz 3-D imaging radar with 4Tx-16Rx MIMO array," *IEEE Trans. Terahertz Sci. Technol.*, vol. 8, no. 5, pp. 509–519, 2018.

[24] O. M. Bakr, "A Scalable and Cost Effective Architecture for High Gain Beamforming Antennas," University of California, Berkeley, 2010.

[25] B. Van Veen and K. M. Buckley, "Beamforming Techniques for Spatial Filtering." CRC Press, 2000.

[26] R. J. Mailloux, *Phased Array Antenna Handbook*, Second Edi., vol. 19. Norwood, MA: Artech House, 1999.

[27] H. Jalili and O. Momeni, "Scalable Wideband and Wide-Angle Beam Steering mm-Wave / THz Radiator and Phased Arrays in Silicon," in *2018 Asia-Pacific Microwave Conference (APMC)*, 2018, pp. 1157–1159.

[28] K. Sengupta and A. Hajimiri, "A 0.28 THz Power-Generation and Beam-Steering Array in CMOS Based on Distributed Active Radiators," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3013–3031, 2012.

[29] Y. Yang, O. D. Gurbuz, and G. M. Rebeiz, "An Eight-Element 370–410-GHz Phased-Array Transmitter in 45-nm CMOS SOI With Peak EIRP of 8–8.5 dBm," *IEEE Trans. Microw. Theory Tech.*, vol. 64, no. 12, pp. 4241–4249, 2016.

[30] M. Uzunkol, O. D. Gurbuz, F. Golcuk, and G. M. Rebeiz, "A 0. 32 THz SiGe 4x4 Imaging Array Using High-Efficiency On-Chip Antennas," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2056–2066, 2013.

[31] Y. Zhao *et al.*, "A 0.54-0.55 THz 2x4 coherent source array with EIRP of 24.4 dBm in 65nm CMOS technology," in *2015 IEEE MTT-S International Microwave Symposium*, 2015.

[32] R. Han and E. Afshari, "A CMOS High-Power Broadband 260-GHz Radiator Array for Spectroscopy," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3090–3104, 2013.

[33] X. Deng, Y. Li, J. Li, C. Liu, W. Wu, and Y.-Z. Xiong, "A 320-GHz 1x4 Fully Integrated Phased Array Transmitter Using 0.13μm SiGe BiCMOS Technology," *IEEE Trans. Terahertz Sci. Technol.*, vol. 5, no. 6, pp. 930–940, 2015.

[34] W. Shin, B. Ku, O. Inac, Y.-C. Ou, and Gabriel M. Rebeiz, "A 108 – 114 GHz 4x4 Wafer-Scale Phased Array Transmitter With High-Efficiency On-Chip Antennas," *IEEE J. Solid-State Circuits*, vol. 48, no. 9, pp. 2041–2055, 2013.

[35] Y. Tousi and E. Afshari, "A High-Power and Scalable 2-D Phased Array for Terahertz CMOS Integrated Systems," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 597–609, 2015.

[36] F. Golcuk, T. Kanar, and G. M. Rebeiz, "A 90-100 GHz 4 × 4 SiGe BiCMOS Polarimetric Transmit-Receive Phased Array with Simultaneous Receive-Beams Capabilities," in *2013 IEEE International Symposium on Phased Array Systems and Technology*, 2013, no. V, pp. 102–105.

[37] A. Tang *et al.*, "A 65nm CMOS 140 GHz 27.3 dBm EIRP Transmit Array with Membrane Antenna for Highly Scalable Multi-Chip Phase Arrays," in *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*, 2014, pp. 12–14.

[38] K. Guo, Y. Zhang, and P. Reynaert, "A 0.53-THz Subharmonic Injection-Locked Phased Array With 63-μW Radiated Power in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 54, no. 2, pp. 380–391, 2019.

[39] H. Jalili and O. Momeni, "A 0 . 34-THz Wideband Wide-Angle 2-D Steering Phased Array in 0.13-μm SiGe BiCMOS," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 2449–2461, 2019.

[40] S. Venkatesh, X. Lu, H. Saeidi, and K. Sengupta, "A high-speed programmable and scalable terahertz holographic metasurface based on tiled CMOS chips," *Nat. Electron.*, vol. 3, pp. 785–793, 2020.

[41] J. J. Lynch *et al.*, "Coded aperture subreflector array for high resolution radar imaging," in *SPIE Defense + Commercial Sensing*, 2019, vol. 1099405, no. May 2019, p. 18.

[42] J. Huang and J. A. Encinar, *Reflectarray Antennas*. Hoboken, New Jersey: John Wiley & Sons, 2008.

[43] P. Nayeri, F. Yang, and A. Z. Elsherbeni, *Reflectarray antennas : theory, designs and applications*. Hoboken, New Jersey: John Wiley & Sons, 2018.

[44] S. V. Hum, S. Member, J. Perruisseau-carrier, and S. Member, "Reconfigurable Reflectarrays and Array Lenses for Dynamic Antenna Beam Control: A Review," vol. 62, no. 1, pp. 183–198, 2014.

[45] N. Yu and F. Capasso, "Flat optics with designer metasurfaces," *Nat. Mater.*, vol. 13, no. February, pp. 139–150, 2014.

[46] L. Zhang, S. Mei, K. Huang, and C. Qiu, "Advances in Full Control of Electromagnetic Waves with Metasurfaces," *Adv. Opt. Mater.*, vol. 4, pp. 818–833, 2016.

[47] Z. Chang, B. You, L. S. Wu, M. Tang, Y. P. Zhang, and J. F. Mao, "A Reconfigurable Graphene Reflectarray for Generation of Vortex THz Waves," *IEEE Antennas Wirel. Propag. Lett.*, vol. 15, pp. 1537–1540, 2016.

[48] B. Mohammadi, J. Nourinia, C. Ghobadi, F. Alizadeh, and M. Karamirad, "Wideband Sub-Wavelength Orbital Angular Momentum Reflectarray Antenna," in *2019 IEEE 5th Conference on Knowledge Based Engineering and Innovation, KBEI 2019*, 2019, pp. 869–873.

[49] J. Yang, Y. Shen, S. Hu, and A. I. F. Reflectarray, "Highly-Integrated Folded Reflectarray for Generation of Bessel Beam Carrying Orbital Angular Momentum," *2018 Int. Conf. Electromagn. Adv. Appl.*, vol. 1, pp. 483–484.

[50] H. Huang and S.-N. Li, "High-efficiency planar reflectarray with small-size for OAM generation at microwave range," *IEEE Antennas Wirel. Propag. Lett.*, vol. 18, no. 3, pp. 432–436, 2019.

[51] C.-C. Li, L.-S. Wu, and W.-Y. Yin, "A dual-polarized and reconfigurable reflectarray for generation of vortex radio waves," *AIP Adv.*, vol. 8, p. 055331, 2018.

[52] D. Zhang *et al.*, "A Shared Aperture 1 Bit Metasurface for Orbital Angular Momentum Multiplexing," *IEEE Antennas Wirel. Propag. Lett.*, vol. 18, no. 4, pp. 566–570, 2019.

[53] S. Yu, L. Li, G. Shi, C. Zhu, X. Zhou, and Y. Shi, "Design, fabrication, and measurement of reflective metasurface for orbital angular momentum vortex wave in radio frequency domain," *Appl. Phys. Lett.*, vol. 108, no. 12, pp. 1–6, 2016.

[54] C. Apert, T. Koleck, P. Dumon, T. Dousset, and C. Renard, "Erasp: A new reflectarray antenna for space applications," in *2006 First European Conference on Antennas and Propagation*, 2006, pp. 1–5.

[55] E. Carrasco and J. A. Encinar, "Reflectarray antennas : A review," in *Forum for Electromagnetic Research Mehtods and Application Technologies*, 2016,

vol. 16, no. 1.

[56] S. V. Polenga, A. V. Stankovsky, R. M. Krylov, A. D. Nemshon, Y. A. Litinskaya, and Y. P. Salomatov, "Millimeter-wave waveguide reflectarray," in *International Siberian Conference on Control and Communications, SIBCON 2015 - Proceedings*, 2015, pp. 1–4.

[57] T. Cai, G.-M. Wang, X.-L. Fu, J.-G. Liang, and Y.-Q. Zhuang, "High-Efficiency Metasurface with Polarization-Dependent Transmission and Reflection Properties for Both Reflectarray and Transmitarray," *IEEE Trans. Antennas Propag.*, vol. 66, no. 6, pp. 3219–3224, 2018.

[58] R. Deng, F. Yang, S. Xu, and M. Li, "A 100-GHz Metal-Only Reflectarray for High-Gain Antenna Applications," *IEEE Antennas Wirel. Propag. Lett.*, vol. 15, pp. 178–181, 2016.

[59] Y. Sun and K. W. Leung, "Millimeter-Wave Substrate-Based Dielectric Reflectarray," *IEEE Antennas Wirel. Propag. Lett.*, vol. 17, no. 12, pp. 2329–2333, 2018.

[60] X. Pan, S. Wang, G. Li, S. Xu, and F. Yang, "On-chip Reconfigurable Reflectarray for 2-D Beam-steering at W-band," in *2018 IEEE MTT-S International Wireless Symposium (IWS)*, 2018, pp. 1–4.

[61] B. D. Nguyen and S. Van Tran, "Beam-steering reflectarray based on two-bit aperture-coupled reflectarray element," *J. Electromagn. Waves Appl.*, vol. 32, no. 1, pp. 54–66, 2018.

[62] T. Debogovic and J. Perruisseau-carrier, "Low Loss MEMS-Reconfigurable 1-Bit Reflectarray Cell With Dual-Linear Polarization," *IEEE Trans. Antennas Propag.*, vol. 62, no. 10, pp. 5055–5060, 2014.

[63] A. Luukanen *et al.*, "Rapid beamsteering reflectarrays for mm-wave and submm-wave imaging radars," in *Proc. SPIE 8022, Passive Millimeter-Wave Imaging Technology XIV*, 2011, no. 80220M.

[64] Y. Zhao *et al.*, "A 0 . 55THz Y-Vector Network Configured Beam Steering Phased Array in CMOS Technology," in *2018 IEEE/MTT-S International Microwave Symposium - IMS*, 2018, pp. 587–590.

[65] R. Pereira, R. Gillard, R. Sauleau, P. Potier, T. Dousset, and X. Delestre, "Dual Linearly-Polarized Unit-Cells With Nearly 2-Bit Resolution For Reflectarray Applications In X-Band," *IEEE Trans. Antennas Propag.*, vol.

60, no. 12, pp. 6042–6048, 2012.

[66] S. V Hum, M. Okoniewski, and R. J. Davies, "Realizing an Electronically Tunable Reflectarray Using Varactor Diode-Tuned Elements," *IEEE Microw. Wirel. Components Lett.*, vol. 15, no. 6, pp. 422–424, 2005.

[67] R. Sorrentino, R. V. Gatti, and L. Marcaccioli, "Recent Advances on Millimetre Wave Reconfigurable Reflectarrays," *2009 3rd Eur. Conf. Antennas Propag.*, pp. 2527–2531.

[68] H. Rajagopalan, Y. Rahmat-Samii, and W. A. Imbriale, "RF MEMS actuated reconfigurable reflectarray patch-slot element," *IEEE Trans. Antennas Propag.*, vol. 56, no. 12, pp. 3689–3699, 2008.

[69] X. Wan, M. Q. Qi, T. Y. Chen, and T. J. Cui, "Field-programmable beam reconfiguring based on digitally- controlled coding metasurface," *Sci. Rep.*, vol. 6, no. 20663, pp. 1–8, 2016.

[70] X. Tan, Z. Sun, D. Koutsonikolas, and J. M. Jornet, "Enabling Indoor Mobile Millimeter-wave Networks Based on Smart Reflect-arrays," in *IEEE INFOCOM 2018 - IEEE Conference on Computer Communications*, 2018, pp. 270–278.

[71] B. N. Lyons, E. Entchev, and M. K. Crowley, "Reflect-array based mm-wave people screening system," in *Proc. SPIE 8900, Millimetre Wave and Terahertz Sensors and Technology VI*, 2013, vol. 890002, no. October 2013.

[72] C. Huang, B. Sun, W. Pan, J. Cui, X. Wu, and X. Luo, "Dynamical beam manipulation based on 2-bit digitally-controlled coding metasurface," *Sci. Rep.*, vol. 7, no. 42302, pp. 1–8, 2017.

[73] H. Yang *et al.*, "A programmable metasurface with dynamic polarization, scattering and focusing control," *Sci. Rep.*, vol. 6, no. October, p. 35692, 2016.

[74] H. Kamoda, T. Iwasaki, J. Tsumochi, and T. Kuki, "60-GHz electrically reconfigurable reflectarray using p-i-n diode," *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 1177–1180, 2009.

[75] W. Xue, J. Han, C. Qiao, and L. Li, "Design of 1-bit Digital Coding Reconfigurable Reflectarray Using Aperture-Coupled Elements Controlled by PIN Diodes," *2018 Int. Conf. Microw. Millim. Wave Technol.*, pp. 1–3, 2018.

[76] S. Tian, H. Liu, and L. Li, "Design of 1-Bit Digital Reconfigurable Reflective Metasurface for Beam-Scanning," *Appl. Sci.*, vol. 7, no. 882, pp. 1–8, 2017.

[77] H. Xu *et al.*, "Tunable microwave metasurfaces for high-performance operations : dispersion compensation and dynamical switch," *Sci. Rep.*, vol. 6, no. 38255, 2016.

[78] M. Riel and J. Laurin, "Design of an Electronically Beam Scanning Reflectarray Using Aperture-Coupled Elements," *IEEE Trans. Antennas Propag.*, vol. 55, no. 5, pp. 1260–1266, 2007.

[79] F. Venneri, S. Costanzo, and G. Di Massa, "Design and validation of a reconfigurable single varactor-tuned reflectarray," *IEEE Trans. Antennas Propag.*, vol. 61, no. 2, pp. 635–645, 2013.

[80] O. Bayraktar, O. A. Civi, and T. Akin, "Beam switching reflectarray monolithically integrated with RF MEMS switches," *IEEE Trans. Antennas Propag.*, vol. 60, no. 2 PART 2, pp. 854–862, 2012.

[81] L. Marcaccioli, S. Montori, R. V. Gatti, E. Chiuppesi, P. Farinelli, and R. Sorrentino, "RF MEMS-reconfigurable architectures for very large reflectarray antennas," in *APMC 2009 - Asia Pacific Microwave Conference 2009*, 2009, no. January, pp. 766–769.

[82] A. S. Hedden, C. R. Dietlein, and D. A. Wikner, "Design of 220 GHz electronically scanned reflectarrays for confocal imaging systems," *Opt. Eng.*, vol. 51, no. 9, p. 091611, 2012.

[83] R. Marin, A. Moessinger, F. Goelden, S. Mueller, and R. Jakoby, "77 GHZ RECONFIGURABLE REFLECTARRAY WITH NEMATIC LIQUID CRYSTAL," in *The Second European Conference on Antennas and Propagation, EuCAP 2007*, 2007, pp. 1–5.

[84] G. Perez-palomino *et al.*, "Design and Demonstration of an Electronically Scanned Reflectarray Antenna at 100 GHz Using Multiresonant Cells Based on Liquid Crystals," *IEEE Trans. Antennas Propag.*, vol. 63, no. 8, pp. 3722–3727, 2015.

[85] A. Moessinger, R. Marin, S. Mueller, J. Freese, and R. Jakoby, "Electronically reconfigurable reflectarrays with nematic liquid crystals," *Electron. Lett.*, vol. 42, no. 16, pp. 3–4, 2006.

[86] J. Li, T. Jin, D. Erni, F. Meng, Q. Wu, and W.-N. Li, "Design and numerical demonstration of a 2D millimeter-wave beam-scanning reflectarray based on liquid crystals and a static driving technique," *J. Phys. D. Appl. Phys.*, vol. 52, no. 27, pp. 1–9, 2019.

[87] S. Bildik, S. Dieter, C. Fritzsch, W. Menzel, and R. Jakoby, "Reconfigurable Folded Reflectarray Antenna Based Upon Liquid Crystal Technology," *IEEE Trans. Antennas Propag.*, vol. 63, no. 1, pp. 122–132, 2015.

[88] W. Hu *et al.*, "Electronically reconfigurable monopulse reflectarray antenna with liquid crystal substrate," in *The Second European Conference on Antennas and Propagation, EuCAP 2007*, 2007, no. 1, pp. 501–501.

[89] R. R. Romanofsky, J. T. Bernhard, F. W. Van Keuls, F. A. Miranda, G. Washington, and C. Canedy, "K-Band Phased Array Antennas Based on Ba 0.60 Sr 0.40 TiO3 Thin-Film Phase Shifters," *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 12, pp. 2504–2510, 2000.

[90] E. Carrasco and J. Perruisseau-Carrier, "Reflectarray antenna at terahertz using graphene," *IEEE Antennas Wirel. Propag. Lett.*, vol. 12, pp. 253–256, 2013.

[91] S. R. Biswas *et al.*, "Tunable Graphene Metasurface Reflectarray for Cloaking, Illusion, and Focusing," *Phys. Rev. Appl.*, vol. 9, no. 3, pp. 1–12, 2018.

[92] Y. Shi and Y. Zhang, "Generation of Wideband Tunable Orbital Angular Momentum Vortex Waves Using Graphene Metamaterial Reflectarray," *IEEE Access*, vol. 6, pp. 5341–5347, 2017.

[93] S. Arezoomandan, H. O. Condori Quispe, N. Ramey, C. A. Nieves, and B. Sensale-rodriguez, "Graphene-based reconfigurable terahertz plasmonics and metamaterials," *Carbon N. Y.*, vol. 112, pp. 177–184, 2017.

[94] Y. C. Guo and M. S. Smith, "Sidelobe reduction for phased array antennas using digital phase shifters. Part 1: One bit phase weighting," *IEE Proc. H Microwaves, Opt. Antennas*, vol. 130, no. 5, pp. 343–351, 2010.

[95] K. Chang, G. E. Murdza, F. Beltran, and R. D. Foltz, "PHASE QUANTIZATION ERROR DECORRELATOR FOR PHASED ARRAY ANTENNA," 5,103,232, 1992.

[96] A. Toshev, "Suppression of phaser quantization lobes for large flat phased array antennas," in *IEEE Antennas and Propagation Society, AP-S International Symposium (Digest)*, 2003, vol. 2, no. i, pp. 488–491.

[97] J. D. Krieger, C. Yeang, and G. W. Wornell, "Dense Delta-Sigma Phased Arrays," vol. 61, no. 4, pp. 1825–1837, 2013.

[98] R. J. MAILLOUX, "Array Grating Lobes due to Periodic Phase, Amplitude,

and Time Delay Quantization," *IEEE Trans. Antennas Propag.*, vol. 32, no. 12, pp. 1364–1368, 1984.

[99] S. Holm and K. Kristoffersen, "Analysis of Worst-Case Phase Quantization Sidelobes in Focused Beamforming," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 39, no. 5, pp. 593–599, 1992.

[100] G. Ahmad, T. H. Loh, T. W. C. Brown, and C. I. Underwood, "On the Phase Selection of Millimeter Wave Quantized Reflectarrays," in *2017 International Applied Computational Electromagnetics Society Symposium (ACES)*, 2017, no. 1, pp. 1–2.

[101] H. Yang *et al.*, "A Study of Phase Quantization Effects for Reconfigurable Reflectarray Antennas," *IEEE Antennas Wirel. Propag. Lett.*, vol. 16, pp. 302–305, 2017.

[102] C. Hemmi, M. H. McCullough, and B. L. Ball, "Two-dimensional quantization method for phased-array scanning," *IEEE Antennas Propag. Mag.*, vol. 56, no. 5, pp. 43–59, 2014.

[103] D. Thompson, M. Yeary, C. Fulton, and B. Mcguire, "Optimized beam steering approach for improved sidelobes in phased array radars using a minimal number of control bits," *IEEE Trans. Antennas Propag.*, vol. 63, no. 1, pp. 106–112, 2015.

[104] A. B. Sripad and D. L. Snyder, "A Necessary and Sufficient Condition for Quantization Errors to be Uniform and White," *IEEE Trans. Acoust.*, vol. 25, no. 5, pp. 442–448, 1977.

[105] J. D. S. Krieger, "Architectures and System Design for Digitally-Enhanced Antenna Arrays," MIT, 2014.

[106] C. P. Yeang, G. W. Wornell, and L. Zheng, "Oversampling transmit and receive antenna arrays," *ICASSP, IEEE Int. Conf. Acoust. Speech Signal Process. - Proc.*, pp. 2522–2525, 2010.

[107] H. Kamoda, J. Tsumochi, and F. Suginoshita, "Reduction in quantization lobes due to digital phase shifters for phased array radars," *Asia-Pacific Microw. Conf. 2011*, pp. 1618–1621, 2011.

[108] "REDUCTION OF SIDE LOBES AND POINTING ERRORS IN PHASED ARRAY RADARS BY RANDOMIZING QUANTIZATION STEPS." Electronic Systems Division, United States Air Force, Bedford, MA, 1963.

[109] B. G. Kashyap, P. C. Theofanopoulos, Y. Cui, and G. C. Trichopoulos, "Mitigating Quantization Lobes in mmWave Low-Bit Reconfigurable Reflective Surfaces," *IEEE Open J. Antennas Propag.*, vol. 1, no. August, 2020.

[110] M. Smith and Y. Guo, "A Comparison of Methods for Randomizing Phase Quantization Errors in Phased Arrays," *IEEE Trans. Antennas Propag.*, vol. 31, no. 6, p. 821, 1983.

[111] T. Salim, J. Devlin, and J. Whittington, "Quantization Analysis for Reconfigurable Phased Array Beamforming.," in *International Symposium on Antennas and Propagation*, 2006, pp. 1–5.

[112] T. Jackson, H. Alsawaha, B. Lu, P. Hou, and Y. Mao, "DIGITAL DITHERING FOR REDUCTION OF QUANTIZATION ERRORS AND SIDE - LOBE LEVELS IN PHASED ARRAY ANTENNAS," US 10,374,663 B2, 2019.

[113] H. Zhang, X. Chen, Z. Wang, Y. Ge, and J. Pu, "A 1-Bit Electronically Reconfigurable Reflectarray Antenna in X Band," *IEEE Access*, vol. 7, pp. 66567–66575, 2019.

[114] H. Kamoda, T. Iwasaki, J. Tsumochi, T. Kuki, and O. Hashimoto, "60-GHz electronically reconfigurable large reflectarray using single-bit phase shifters," *IEEE Trans. Antennas Propag.*, vol. 59, no. 7, pp. 2524–2531, 2011.

[115] H. Yang *et al.*, "A 1600-element dual-frequency electronically reconfigurable reflectarray at X/Ku-band," *IEEE Trans. Antennas Propag.*, vol. 65, no. 6, pp. 3024–3032, 2017.

[116] H. Kamoda, J. Tsumochi, and F. Suginoshita, "Reduction in quantization lobes due to digital phase shifters for phased array radars," in *Asia-Pacific Microwave Conference 2011*, 2011, pp. 1618–1621.

[117] C. Hemmi, M. H. McCullough, and B. L. Ball, "Two-dimensional quantization method for phased-array scanning," *IEEE Antennas Propag. Mag.*, vol. 56, no. 5, pp. 43–59, 2014.

[118] P. Chen *et al.*, "MODULATION PATTERNS FOR SURFACE SCATTERING ANTENNAS," US 9,711,852 B2, 2017.

[119] H. Kamoda, J. Tsumochi, T. Kuki, and F. Suginoshita, "A STUDY ON ANTENNA GAIN DEGRADATION DUE TO DIGITAL PHASE," *Microw.*

Opt. Technol. Lett., vol. 53, no. 8, pp. 1743–1746, 2011.

[120] H. Kamoda, J. Tsumochi, and F. Suginoshita, "Experimental Verification of Novel Method to Reduce Quantization Lobes for Phased Array Radar," in *2012 9th European Radar Conference*, 2012, pp. 337–340.

[121] J. Song, J. Wang, K. Peng, C. Pan, and Z. Yang, "Quantization error reduction for the phased array with 2-bit phase shifter," *Wirel. Pers. Commun.*, vol. 52, no. 1, pp. 29–41, 2010.

[122] S. Ebadi, R. Gatti, and R. Sorrentino, "Linear reflectarray antenna design using 1-bit digital phase shifters," *Antennas Propagation, 2009. EuCAP 2009. 3rd Eur. Conf.*, pp. 3729–3732, 2009.

[123] N. M. Monroe, G. C. Dogiamis, R. Stingel, P. Myers, X. Chen, and R. Han, "Electronic THz Pencil Beam Forming and 2D Steering for High Angular-Resolution Operation: A 98×98-Unit 265GHz CMOS Reflectarray with In-Unit Digital Beam Shaping and Squint Correction," in *ISSCC*, 2022, pp. 15–17.

[124] C. Cheng and A. Abbaspour-Tamijani, "Evaluation of a Novel Topology for MEMS Programmable Reflectarray Antennas," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 12, pp. 3333–3344, 2009.

[125] J. Huang and J. A. Encinar, *REFLECTARRAY ANTENNAS*. Hoboken, New Jersey: John Wiley & Sons, 2008.

[126] R. Sorrentino, R. V. V. Gatti, and L. Marcaccioli, "Recent advances on millimetre wave reconfigurable reflectarrays," in *2009 3rd European Conference on Antennas and Propagation*, 2009, pp. 2527–2531.

[127] H. Yang *et al.*, "A 1600-Element Dual-Frequency Electronically Reconfigurable Reflectarray at X/Ku-Band," *IEEE Trans. Antennas Propag.*, vol. 65, no. 6, pp. 3024–3032, 2017.

[128] F. Yang *et al.*, "Reconfigurable Reflectarrays and Transmitarrays : From Antenna Designs to System Applications," in *12th European Conference on Antennas and Propagation (EuCAP 2018)*, 2018, pp. 1–4.

[129] Q. Yu *et al.*, "mmWave and sub-THz Technology Development in Intel 22nm FinFET (22FFL) Process," in *IEEE Intl. Electron Device Meetings (IEDM)*, 2020, pp. 1–4.

[130] P. Nayeri, A. Z. Elsherbeni, and F. Yang, "Radiation analysis approaches for

reflectarray antennas [antenna designer's notebook]," *IEEE Antennas Propag. Mag.*, vol. 55, no. 1, pp. 127–134, 2013.

[131] H. Jalili and O. Momeni, "A 436-to-467GHz Lens-Integrated Reconfigurable Radiating Source with Continuous 2D Steering and Multi-Beam Operations in 65nm CMOS," in *ISSCC*, 2021, pp. 326–328.

[132] H. Saeidi, S. Venkatesh, X. Lu, and K. Sengupta, "THz Prism: One-Shot Simultaneous Multi-Node Angular Localization Using Spectrum-to-Space Mapping with 360-to-400GHz Broadband Transceiver and Dual-Port Integrated Leaky-Wave Antennas," in *ISSCC*, 2021, pp. 314–317.

[133] X. Yi, C. Wang, X. Chen, J. Wang, J. Grajal, and R. Han, "A 220-to-320-GHz FMCW Radar in 65-nm CMOS Using A Frequency-Comb Architecture," *JSSC*, vol. 56, no. 2, pp. 327–339, 2020.

[134] Wei Jiang, Yanchang Guo, Tinghua Liu, Wenfei Shen, and Wei Cao, "Comparison of random phasing methods for reducing beam pointing errors in phased array," *IEEE Trans. Antennas Propag.*, vol. 51, no. 4, pp. 782–787, 2003.

[135] Q. Wu and R. Zhang, "Towards Smart and Reconfigurable Environment : Intelligent Reflecting Surface Aided Wireless Network," *IEEE Commun. Mag.*, vol. 58, no. 1, pp. 106–112, 2020.

[136] M. Di Renzo *et al.*, "Smart radio environments empowered by reconfigurable AI meta-surfaces : an idea whose time has come," *EURASIP J. Wirel. Commun. Netw.*, vol. 129, 2019.

[137] C. Liaskos, S. Nie, A. Tsioliaridou, A. Pitsillides, S. Ioannidis, and I. Akyildiz, "A New Wireless Communication Paradigm through Software-controlled Metasurfaces," *IEEE Commun. Mag.*, vol. 56, no. 9, pp. 162–169, 2018.

[138] "Wafer Scale Engine." [Online]. Available: https://cerebras.net/chip/.

[139] R. E. Hodges, N. Chahat, D. J. Hoppe, and J. D. Vacchione, "A Deployable High-Gain Antenna Bound for Mars: Developing a new folded-panel reflectarray for the first CubeSat mission to Mars," *IEEE Antennas Propag. Mag.*, vol. 59, no. 2, pp. 39–49, 2017.

[140] G. Ahmad, T. W. C. Brown, C. I. Underwood, and T. H. Loh, "An investigation of millimeter wave reflectarrays for small satellite platforms," *Acta Astronaut.*, vol. 151, no. May, pp. 475–486, 2018.

[141] G. W. Wornell and L. Zheng, "OVERSAMPLING TRANSMIT AND RECEIVE ANTENNA ARRAYS Chen-Pang," *2010 IEEE Int. Conf. Acoust. Speech Signal Process.*, pp. 2522–2525, 2010.