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Realization of In-Band Full-Duplex Operation at 300 K and 4.2 K Using Bilateral Single-Sideband Frequency Conversion

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***Abstract*— CMOS-integrated in-band full-duplex (IBFD) operation in wireless links and cryogenic quantum platforms was previously enabled by magnetic-free circulators using the phase non-reciprocity from spatial-temporal modulation. In this paper, we present an alternative and simple integrated circuit scheme, which not only realizes non-reciprocal signal flows required for IBFD operations, but also improves the isolation performance by completely eliminating any chip-level TX-to-RX coupling. The above functions are enabled by performing a direction/frequency-independent, single-sideband down-conversion to the counter-propagating TX and RX signals, which creates opposite deviations of on-chip TX and RX frequencies with respect to the antenna frequency. Such a principle also broadens the isolation bandwidth and enables integrated receiver down-mixing function. As a proof-of-concept, a 3.4∼4.6-GHz (30% fractional bandwidth) IBFD interface is implemented using a 65-nm bulk CMOS technology. The measured TX-to-RX isolation of the circuit is 32∼51 dB at 300 K, and 14∼29 dB at 4.2 K. The measured TX-to-ANT and ANT-to-RX insertion loss are 3.0 and 3.2 dB at 300 K, and 1.9 and 2.0 dB at 4.2 K. At 300 K, the measured TX-to-ANT and ANT-to-RX IIP3 are 29.5 and 27.6 dBm, respectively. The IBFD core of the chip occupies an area of 0.27 mm^2 and has a DC power (nominally consumed in an on-chip modulation clock generator) of 48 mW of at 300 K and 42.6 mW at 4.2 K.**

***Index Terms*—in-band full-duplex, magnetic-free circulator, non-reciprocal, bilateral frequency converter, isolation, coupling, wideband, cryo-CMOS.**

I. Introduction

THE ever-increasing demands for wireless communication speed and sensing capability call for RF systems with more efficient utilization of the congested electromagnetic spectrum. Compared with conventional half-duplex modes, such as time-division duplex and frequency-division duplex, in-band full-duplex (IBFD) mode potentially doubles the utilization efficiency of the spectrum and simplifies the transmission protocols [1], [2]. Non-reciprocal electronic devices, such as isolator, gyrator, and circulator, are critical for full-duplex operations and have been extensively utilized in wireless data links and monostatic radars. In addition, circulator capable of operating under cryogenic condition is critical in quantum computing platforms, in which a non-reciprocal path is needed to extract the weak qubit measurement signal while blocking any inverse disturbance from, for example, the pump signal of a parametric amplifier [3].

Shown in Fig. 1, a circulator is a three-port device which delivers signal to the next port in a certain rotation. It enables an IBFD system where the transmit (TX) and receive (RX) signals have identical frequencies on the chip and share a single antenna (ANT). Conventional ferrite circulators based on Faraday rotation are bulky and cannot be integrated on a chip. Recently, magnetic-free circulators have become attractive due to their compact size and compatibility with CMOS integrated circuit technologies [4]–[9]. Using time-variant devices, typically realized with clock-modulated switches in a N-path filter [2], such a component applies non-reciprocal phases to various signals at the same frequency; then, with another signal path through a delay line with reciprocal added phase, the circuit creates constructive addition to the desired signal at a certain port and cancellation to other undesired signals.

It is noteworthy that the TX-to-RX isolation is a key parameter to all full-duplex systems. However, a few imperfections may degrade the isolation. For example, the impedance mismatch at the antenna port causes part of the TX signal to be reflected to the RX port; this problem is normally alleviated by a post-fabrication/packaging impedance tuning at the antenna port. In the context of silicon integrated circuits, one critical limitation of isolation relates to the inevitable TX-to-RX coupling through the inter-inductor magnetic crosstalk, doped silicon substrate (especially in bulk CMOS processes with typically 10-Ω·cm resistivity), on-chip power lines, etc. In Fig. 2, a full-wave electromagnetic simulation shows that, on a silicon substrate with 10-Ω·cm resistivity, the coupling between two standard multi-coil inductors[1] at 4 GHz can be -20 dB or higher, when they are placed close to each other. It clearly indicates that a compact layout design poses

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[1]The simulation reflects a common scenario in an actual IBFD system that one of such inductors is used in a resonator circuit of the high-power TX chain, while the other inductor is used for the resonance in a sensitive RX chain.

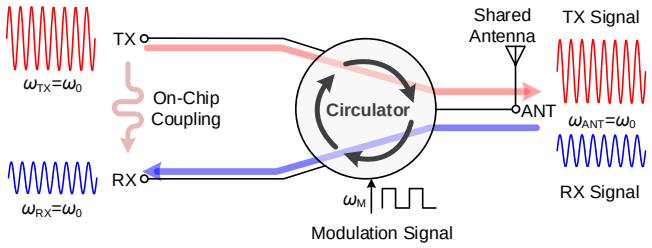


Fig. 1: Prior CMOS-circulator-based full-duplex interface: propagation and frequency allocation of the TX, RX and ANT signals.

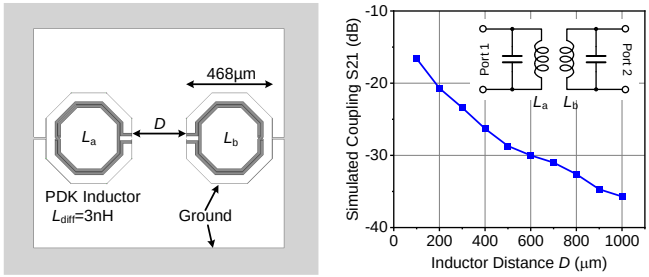


Fig. 2: The coupling between two standard inductors on a bulk CMOS substrate (10-Ω·cm resistivity) at 4 GHz. To mimic the normal application scenarios of inductors in RFICs, two capacitors (520 fF) are added to create resonance.

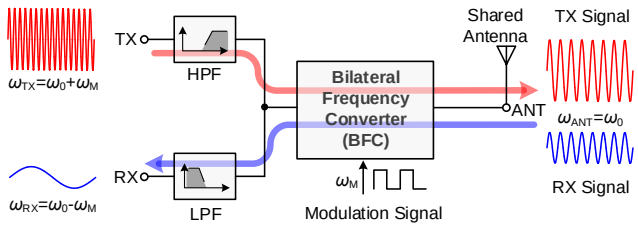


Fig. 3: Our BFC-based full-duplex systems: propagation and frequency allocation of the TX, RX and ANT signals.

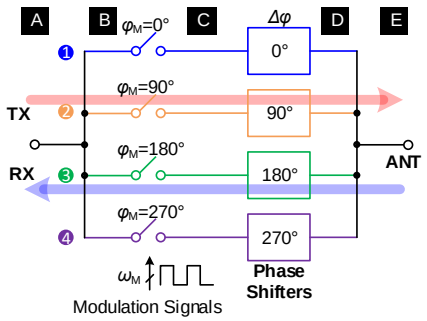


Fig. 4: Simplified schematic of the bilateral frequency converter (BFC).

significant challenges to a IBFD front-end circuit. Lastly, as described previously, the isolation of prior CMOS circulators relies on the cancellation of two precisely out-of-phase signals from two paths that are implemented with completely different manners. Correspondingly, the created isolation is narrowband in nature and is susceptible to non-ideal clocking and other amplitude/phase mismatches among the signal paths.

In this paper, we present a fully-integrated IBFD interface that utilizes a bilateral frequency converter (BFC) to realize non-reciprocity while addressing the above problems of CMOS circulators [10]. As shown in Fig. 3, the BFC is driven by a modulation signal ω_M and has two ports: one port is connected to the shared antenna (ANT), while the other port carries both the TX and RX signals. The key difference from a circulator (both standard and CMOS-based) is that, although the TX and RX frequencies are identical at the antenna interface (i.e. $\omega_{ANT}=\omega_0$), they are shifted to $\omega_0+\omega_M$ and $\omega_0-\omega_M$, respectively, inside the chip. The $2\omega_M$ separation is realized through a *signal & direction-independent downconversion process* in the BFC. The TX and RX signals can be then physically separated by a high-pass filter (HPF) and a low-pass filter (LPF). One clear advantage of this scheme, due to such a frequency split, is that the aforementioned chip-level TX-to-RX coupling in a normal IBFD system is eliminated. Moreover, our analysis to be given in this paper will also show that the TX-to-RX isolation of the circuit is wideband in nature and is robust against issues like device mismatch and non-ideal clocking.

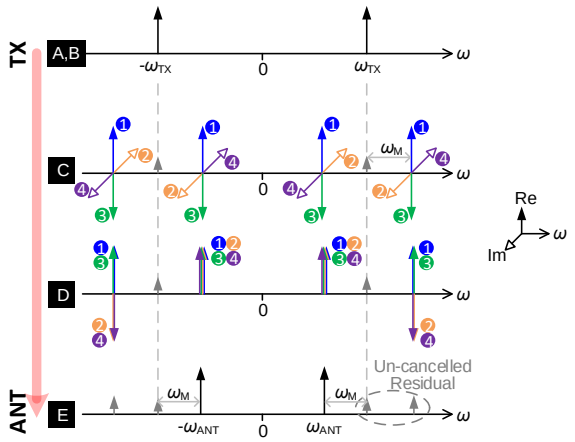
As a proof-of-concept, a 4-GHz front-end that uses a standard 65-nm bulk CMOS technology is demonstrated and characterized at both 300 K and 4.2 K. Effective isolation across ~30% fractional bandwidth is obtained. This paper is organized as follows. In Section II, a few key properties of a BFC are analyzed. Section III then presents the circuit implementation details of the 4-GHz IBFD interface. In Section IV, the measurement results are shown. Finally, a conclusion with a performance comparison with other CMOS circulators is given in Section V.

II. Bilateral Frequency Converter with Irreversible Spectral Shift

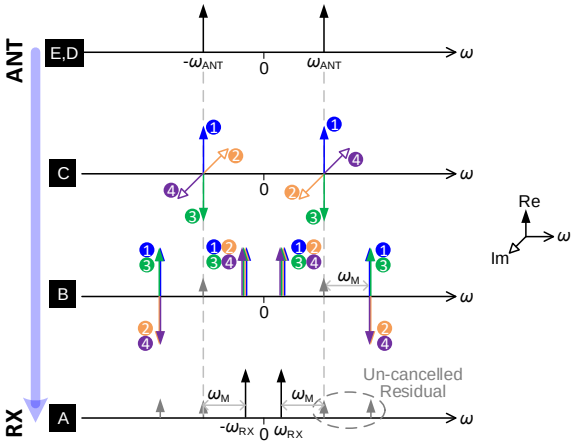
The simplified schematic of a two-port BFC is shown in Fig. 4. It consists of four parallel paths, and each path is a series connection of one switch and one phase shifter. The switches are driven by modulation signals with quadrature phases, and they introduce frequency and phase shifts to signals flowing along the paths. Albeit the resemblance to a passive single-sideband mixer, one important property of the presented topology that was unexplored before is its *irreversible* frequency conversion process, namely, the BFC always performs frequency downconversion regardless of the signal flow direction.

To understand that, we examine the phasor diagram of signals at various stages (i.e. A~E) of the schematic in Fig. 4[2]. Fig. 5a shows the signal flowing from TX to ANT. For simplicity, only the positive frequency components are described in the following. At Stage A and B, the TX signal at ω_{TX} is modulated with quadrature phases $\varphi_{M,\ i=1,2,3,4}$ of 0°, 90°, 180°, and 270° in Path 1~4 of Fig. 4, respectively. Thus, at Stage C, the two generated sideband frequency components

[2]For simplicity of the illustration, we assume that when a signal passes through a modulated switch, only the upper and lower sidebands remain, while the component at the original signal frequency vanishes. Strictly speaking, that is not true for the single-ended signaling in Fig. 4. But it does happen for the differential signaling in our actual design (Fig. 6).



(a)



(b)

Fig. 5: Phasor diagrams of the signals flowing from (a) TX to ANT, and (b) ANT to RX.

(ω_{TX}-ω_M and ω_{TX}+ω_M) in Path i (i=1,2,3,4) carry the following phases:

$$\begin{cases} \varphi_{C,\,i} = \varphi_{M,\,i} & \text{for the upper sideband} \\ \varphi_{C,\,i} = -\varphi_{M,\,i} & \text{for the lower sideband} \end{cases}. \quad (1)$$

Next, these signals flow through the phase shifters. The values of the applied phases are selected to compensate the phase differences of the lower sideband signals (i.e. $\Delta\varphi_i$=$\varphi_{M,\,i}$) among the four paths, so that after the signal summation, only such lower sideband component is preserved at the ANT port. As a result, the TX signal is shifted down by ω_M when flowing to ANT.

For a signal flowing backward (i.e. ANT to RX), similar phasor-diagram analysis can be applied. As shown in Fig. 5b, again only the lower sideband signal (ω_{ANT}-ω_M=ω_{RX}) presents at Node A on the left. A key observation to straightforwardly explain such an irreversible frequency conversion is that the condition listed in (1) is always valid, regardless of the signal frequency and its flow direction through the switches. Similarly, the additional phase $\Delta\varphi$ applied by the phase shifters is also independent of the signal frequency and direction. The above two-step manipulation then always leads to the in-phase summation of the lower-sideband component and out-of-phase cancellation of the upper-sideband component, hence an irreversible downconversion. As a result, the TX and RX signals have frequencies that are higher and lower than ω_{ANT} by ω_M, respectively, and can be easily diverted to two separate on-chip paths using a HPF for the TX port and a LPF for the RX port. Although the presented scheme does not deliver the exactly same function as a conventional circulator, it still enables IBFD operation in light of the identical TX and RX frequencies at a shared antenna interface; meanwhile, the TX/RX frequency split eliminates any coupling between the TX and RX blocks on the same die.

As described in Section I, isolation in prior magnetic-free circulators is prone to any incomplete out-of-phase cancellation of the TX signal within two different paths. Next, we discuss the robustness of isolation in our scheme. We first note that similar incomplete signal cancellation also happens with the inevitable presence of (1) different signal loss within the four paths, due to the mismatches of switch transistors and phase shifters, and (2) non-ideal duty cycle and quadrature phases of the modulation clock. Fortunately, as Fig. 5a indicates, the existence of the above problems only results in the un-cancelled TX-to-ANT signal residuals at ω_{ANT}+ω_M and ω_{ANT}+2ω_M, which is far away from ω_{ANT} and can be easily filtered. Similarly, for the ANT to RX direction (Fig. 5b), the residuals are located at ω_{RX}+ω_M and ω_{RX}+2ω_M, which can also be readily filtered out. Since none of the above residuals is located at ω_{RX}, the isolation performance is not degraded at all. We also note that such robust isolation applies to a broad operation band: although the phase $\Delta\varphi$ applied by each shifter only remains precise within a narrow band, the imperfect vector cancellation in Fig. 5 at large frequency offset does not lead to TX-to-RX leakage.

The presented circuit has a few more advantages in addition to the improved isolation and bandwidth. Firstly, the presented circuit uses only one set of switches (as opposed to two in [4]–[9]) in the signal paths, thus the linearity is improved. Secondly, cryogenic quantum platforms are highly sensitive to heat generation. Fewer transistor switches of our scheme lead to lower total clock signal dissipation at the gates of the transistors[3], which sets the intrinsic power consumption (i.e. generated heat) of the IBFD circuit. Thirdly, by choosing ω_M to be close to ω_0, the circuit can also perform additional function of receiver down-mixing; as a result, a dedicated down-conversion mixer succeeding the RX port is no longer needed. Alternatively, the BFC can also be designed to perform frequency up-conversion, which then makes it possible to incorporate the up-mixing function into the transmitter.

III. Circuit Implementations of a 4-GHz IBFD Interface

To experimentally demonstrate the presented scheme, a CMOS IBFD interface circuit with 4-GHz antenna frequency

[3]Note that it is different from the well-known dynamic power ($CV_{DD}^2 f_{CLK}$) of digital circuits, because the heat associated with that dynamic power is not generated within the switches (but in the clock generator which can be placed outside of the cryogenic environment). Instead, the dissipation referred here relates to the AC power loss of the clock signal in the switch transistors due to their gate and channel resistance.

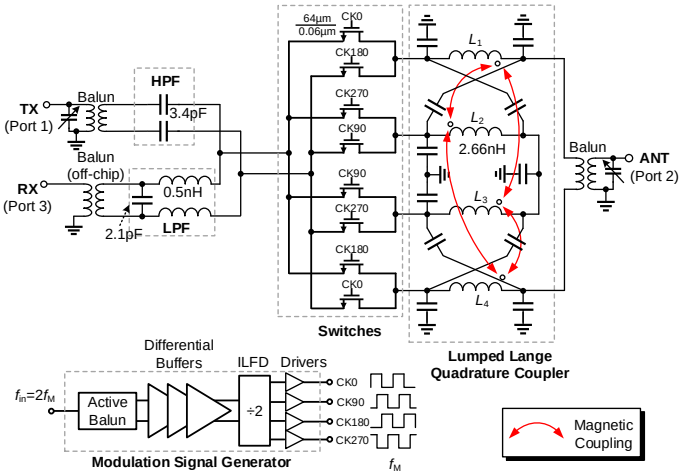


Fig. 6: Schematic of the 4-GHz BFC-based IBFD interface circuit.

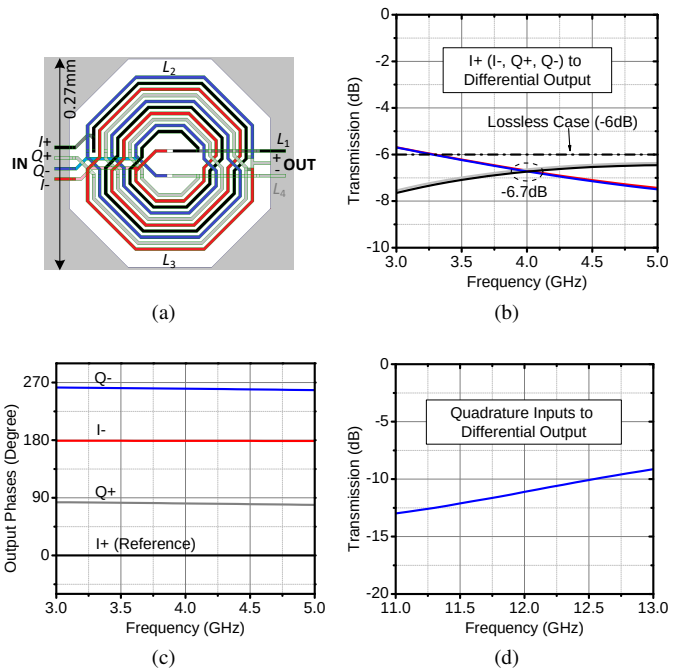


Fig. 7: The 4-GHz quadrature Lange coupler: (a) geometry, (b) & (c) simulated transmission amplitude and phase at f_{ANT}, and (d) simulated transmission of the upper-sideband frequency component at $f_{TX} + f_M$.

is prototyped. The full schematic of the chip is shown in Fig. 6. In this section, design details and simulation results are provided.

One goal of this design is to showcase an integrated *homodyne* down-mixing function; correspondingly, f_M is chosen to be f_{ANT}=4 GHz, and hence f_{TX} is f_{ANT}+f_M=8 GHz. To suppress undesired signal/clock feedthrough in the switches at f_{TX}, f_{ANT} and f_M, differential signaling is adopted in the circuit. Each differential switch pair in Fig. 6 has transistor size of 64μm/0.06μm. A pair of 3.4-pF MIM capacitors are used as the HPF at the TX port, and an *L-C* LPF is employed at the RX port. To facilitate the single-ended testing of the chip, two on-chip baluns are implemented at the TX and ANT ports, and one off-chip balun is used at the RX port. Each on-chip balun

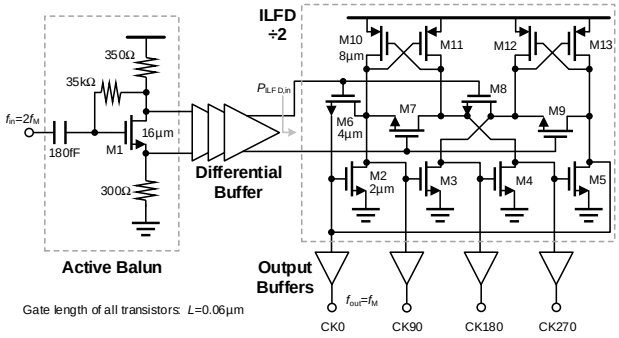


Fig. 8: Schematic of the 4-GHz modulation clock generator.

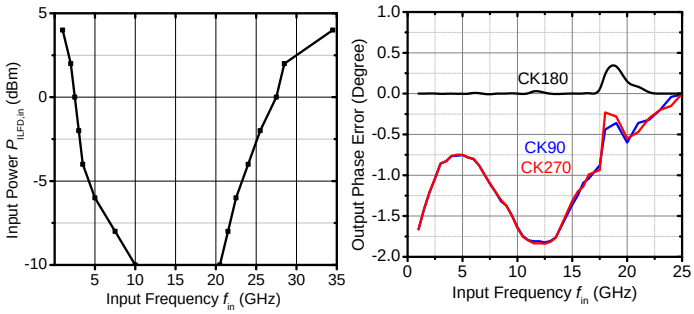


Fig. 9: Simulated (a) locking-range of ILFD and (b) output phase errors of the modulation clock generator.

is in shunt with a MOS varactor, in order to provide impedance tuning at the TX and ANT ports. For testing purposes, the chip also has a broadband integrated modulation clock generator to provide the quadrature signals to drive the eight switches.

A differential lumped Lange quadrature coupler is adopted to realize the quadrature-phase-shifting functions at f_{ANT}. Fig. 7 shows the layout of the coupler, which has an equivalent circuit given in Fig. 6. The design is similar to that in [11] but has a differential structure. By adopting both inductive and capacitive coupling, a highly compact size of 0.073 mm^2 is achieved. Shown in Fig. 7a, the Lange coupler consists of four coupled inductors and metal-oxide-metal (MOM) capacitors (placed under the inductors). The inductors are laid out symmetrically and each one has about 2.5 turns, so that the four quadrature ports are at one side of the coupler and the differential ports are at the other side. Fig. 7b∼7d presents the HFSS-simulated results of the quadrature coupler. The simulated conversion loss at 4 GHz is about 0.7 dB, and the simulated return loss is less than -10 dB for all ports.

In Fig. 5a, the frequency component at $\omega_{TX}+\omega_M$ (∼12 GHz) is cancelled upon the application of the phases in the shifters. In our circuit prototype, such an operation is instead realized by the band-pass characteristic of the quadrature coupler: shown in Fig. 7d, the transmission at 12 GHz is directly blocked by the coupler.

The modulation clock generator consists of one active balun, a three-stage differential buffer, an injection-locked frequency divider (ILFD), and output drivers as shown in Fig. 8. A self-biasing common-source/drain amplifier is used

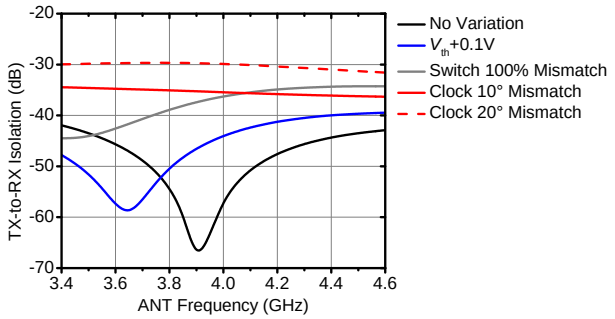


Fig. 10: Simulated TX-to-RX isolation of the core of the 4-GHz IBFD interface.

as a broadband active balun. The subsequent three-stage differential buffer then provides additional common-mode suppression. The divide-by-2 ILFD consists of two PMOS latches (M10∼M13), an NMOS ring oscillator (M2∼M5), and an NMOS injection network (M6∼M9). The PMOS latches provide a negative resistance for the ring oscillator. The injection network has four end-to-end connected transistors forming a ring. The symmetric topology of the circuit enables an ultra-wide operation range; as shown in Fig. 9a, the simulated input locking-range can be as wide as 1∼35 GHz, when the injected power is 4 dBm. The modulation clock generator is therefore capable of providing an output at 0.5∼12.5 GHz. Lastly, as Fig. 9b shows, the phase errors of the output across the wide operation frequency are below 2°, which is again mainly due to the symmetry of the circuit topology. The simulated DC power of the block is 42 mW. It is worth noting that this modulation clock generator is over-engineered, in light of the large operation temperature range and the unavailability of the device models under cryogenic conditions. In the future, more efficient (and narrowband) sources based on LC oscillators could be adopted, which should reduce the power to a few mW [12]. The simulated power dissipation of the IBFD core, which is essentially the net clock signal power injection into the eight switching transistors due to their gate and channel resistance, is 0.4 mW at f_{M}=4 GHz. That sets the ultimate limit of the presented scheme for the cryogenic cooling budget.

As discussed in Section II, our circuit is robust against to the process-voltage-temperature (PVT) variations. To verify that, the simulated TX-to-RX isolation of the IBFD core circuit with 50-Ω matching at the ANT port is shown in Fig. 10. The TX-to-RX isolation is better than 42 dB across the whole operation frequency. Fig. 10 also shows that, even with a 20° modulation clock mismatch among different paths, the isolation is still better than 30 dB. In another extreme case, where the size of half of the switches is increased by 100%, simulation shows that the isolation is still better than 34 dB. All these are strong indication about the robustness of the isolation. Lastly, to evaluate the impact of possible device behavior changes under cryogenic conditions (e.g. threshold voltage V_{th} increase as reported in [13]), we increase the V_{th} of transistors by 0.1 V, and observe that the minimum isolation degrades by only 3.7 dB. We are currently unable to estimate the impact of increased substrate resistivity due to the freeze-out at cryogenic condition, but we anticipate that the effect should improve the insertion loss of the circuit due to smaller signal leakage from the source/drain to the substrate.

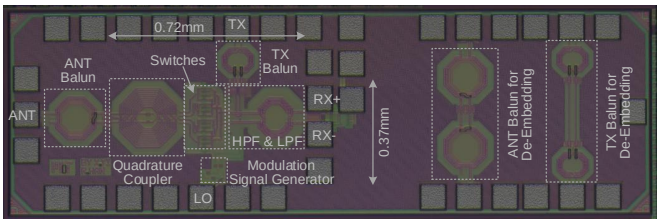


Fig. 11: Die photographs of the 4-GHz IBFD circuit, and the back-to-back balun structures for de-embedding.

IV. Measurement Results

The BFC-based full-duplex chip is fabricated using TSMC 65-nm bulk CMOS technology. The die photo is shown in Fig. 11. The core IBFD circuit including the quadrature coupler, switches, modulation signal generator, HPF, and LPF occupies an area of only 0.27 mm^2. When used in a complete wireless system, the baluns at three ports are not needed, because the antenna and the TX/RX circuitry are normally differential. So to test the performance of the core circuit of the chip, standalone structures consisting of back-to-back ANT and TX baluns are also fabricated for de-embedding purpose. The low-frequency off-chip balun at the RX port is also measured and de-embedded through a back-to-back structure on a PCB. The chip is characterized at both room temperature (∼300 K) and cryogenic temperature (∼4.2 K). Fig. 12a shows the setup for ANT-to-RX measurement at room temperature. In this setup, the RF performance is tested through the probing on the high frequency pads (ANT, TX, and LO). The low-frequency RX differential ports are wire-bonded to the PCB and connected to an off-chip balun. Power supplies and bias voltages are also wire-bonded and supplied externally.

A Keysight PNA-X network analyzer (N5245B) with a mixer-measurement configuration is utilized. The LO port of the PNA delivers the ∼8-GHz ($2f_{\mathrm{M}}$) modulation. To test the TX-to-ANT transmission, the other two ports of the PNA (Port 1 and 2) for cross-frequency S-parameter measurement are connected to the TX and ANT ports, respectively, and the RX port is terminated with 50 Ω. The measured ANT frequency is from 3.4 to 4.6 GHz. Shown in Fig. 13a are the measured *S*-parameters after de-embedding the loss of the baluns. The TX-to-ANT insertion loss extracted from S_{21} ranges from 3.0 to 5.8 dB across the 30% fractional bandwidth. As expected, S_{12} that represents the reverse insertion from ANT to TX is below -10 dB, hence the non-reciprocity. Next, the two PNA ports (dubbed as Port 2 and Port 3) are connected to the ANT and RX ports, respectively, and the TX port is terminated with 50 Ω. The measured *S*-parameters are shown in Fig. 13b. The ANT-to-RX insertion loss extracted from S_{32} ranges from 3.2∼6.1 dB. Similarly to the above case, the reverse RX-to-ANT transmission (S_{23}) is below -10 dB. Lastly, the TX-to-RX isolation is tested by connecting the two PNA cross-frequency ports with the TX and RX ports, respectively, while loading the probed ANT port with 50 Ω.

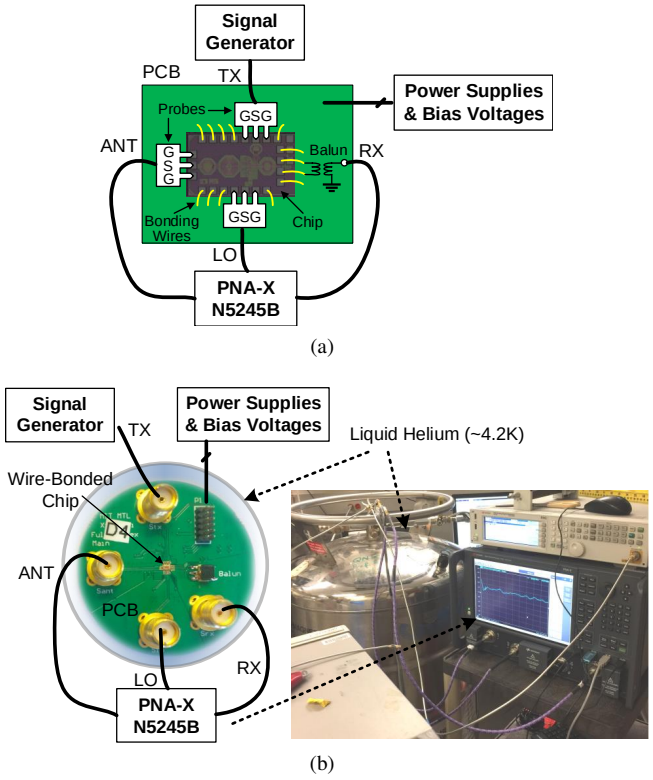


Fig. 12: Setups for the ANT-to-RX measurement at (a) room temperature (around 300 K) and (b) cryogenic temperature (around 4.2 K). The modulation signal is injected through the LO port.

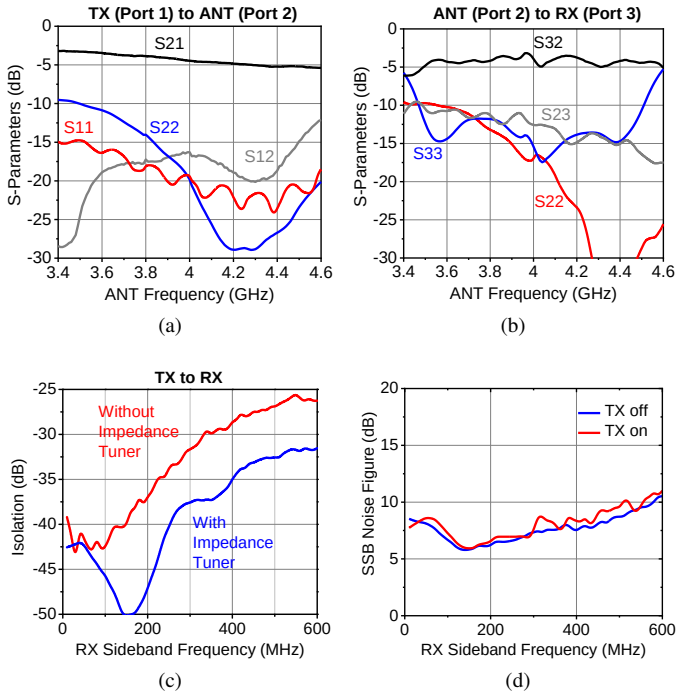


Fig. 13: Measured results at 300 K: (a) TX-to-ANT, (b) ANT-to-RX and (c) TX-to-RX paths, and (d) SSB noise figure of the ANT-to-RX path.

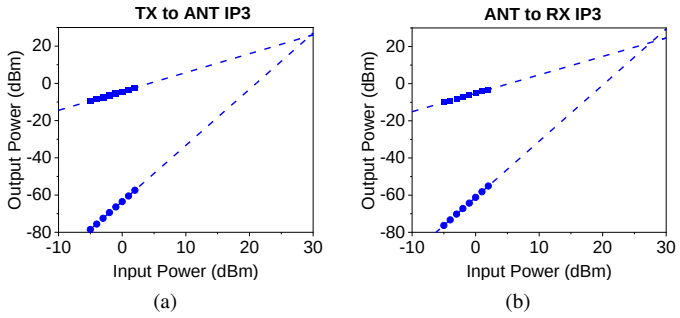


Fig. 14: Front-end measured IP3 of (a) TX-to-ANT and (b) ANT-to-RX paths.

Shown in Fig. 13c, across the 30% fractional bandwidth, the measured isolation ranges from 25.5 to 43 dB. Note that the balun loss which contributes to additional isolation has already been de-embedded. Similar to all other full-duplex systems, the wave reflection at the ANT port degrades the isolation performance. With a manual impedance tuning at the ANT port, the measured isolation improves to 32∼50 dB.

The setup shown in Fig. 12a is also used to test the noise figure (NF) performance of the chip. To emulate the full-duplex operation, an extra signal generator is also connected to the TX port to provide a simultaneously transmitted TX power of 0 dBm. With the TX power turned off, the measured NF shown in Fig. 13d has a minimum value of 5.8 dB. With the TX power turned on, unlike the significant NF degradation in full-duplex mode in [5], we only observe $<$1 dB NF degradation at some baseband frequencies. That again illustrates excellent isolation between the TX and RX paths. It is important to note that, since the presented circuit performs the homodyne down-conversion, the noise at both the upperside and lowerside bands around f_{ANT} is folded to the RX baseband output. Therefore, the data shown in Fig. 13d are in fact the single-sideband noise figure (SSB NF), which assumes that the input signal only lies at one sideband around f_{ANT}. That explains why the NF in Fig. 13d is on average ∼3 dB larger than the insertion loss in Fig. 13b. With additional filtering of the noise from one sideband, it is possible that the NF could be improved in future developments. Also note that due to the integrated receiver down-conversion function of our scheme, further baseband amplification beyond our IBFD interface would incur less additional noise/power penalty, compared to the RF amplification in traditional IBFD systems.

The linearity of the circuit is also measured by sweeping the input power of the setup. The measured results are given in Fig. 14, where the IIP3 for the TX-to-ANT and ANT-to-RX directions are 29.5 and 27.6 dBm, respectively.

To test the IBFD circuit performance under cryogenic condition, a setup shown in Fig. 12b is used, where a PCB with the wire-bonded chip is placed inside liquid helium (4.2 K) and is connected to the same Keysight PNA-X through cables. The measured results are shown in Fig. 15. Compared to the TX-to-ANT transmission at 300 K, the one at 4.2 K is improved to 1.9∼4.2 dB (Fig. 15a), which is probably due to the higher carrier mobility, higher substrate resistivity (hence lower leakage to substrate), and lower metal resistivity [14]. Similarly, the measured ANT-to-RX insertion loss is also improved to 2.0∼5.3 dB at 4.2 K. Since the ANT port is connected through a bond wire in Fig. 12b, rather than

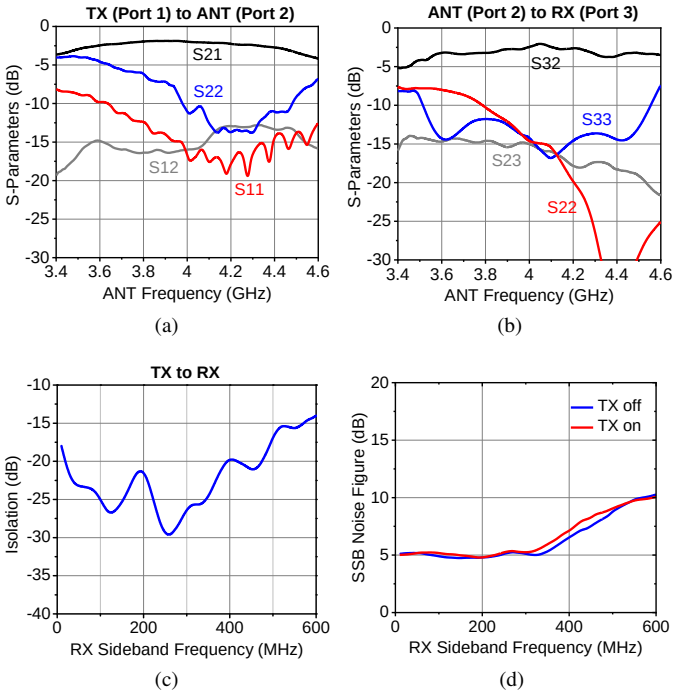


Fig. 15: Front-end measured S-parameters of: (a) TX-to-ANT, (b) ANT-to-RX and (c) TX-to-RX paths, and (d) noise figure of the ANT-to-RX path at 4.2 K.

through probing in the 300-K case, the bond wire inductance causes impedance mismatch that cannot be compensated by the impedance tuner. The associated wave reflection at ANT port therefore degrades the TX-to-RX isolation. Shown in Fig. 15c, the measured isolation ranges from 14 to 29.5 dB across the whole operation band. The measured minimum SSB NF is 4.8 dB, no matter whether the TX signal (0 dBm) is injected or not.

The power consumption of the chip, which is almost entirely from the integrated modulation clock generator, is 48 mW at 300 K and 42.6 mW at 4.2 K.

V. Conclusion

A new concept using frequency conversions of two counter-propagating signals is demonstrated, which performs non-reciprocity similar to that in circulators and enables in-band full-duplex systems in CMOS. In this paper, a 4-GHz IBFD front-end interface is implemented to demonstrate this scheme. Its performance is summarized in Table I, along with a comparison with other state-of-the-art integrated circulators in CMOS. One notable advantage of our front-end is the high TX-to-RX isolation across a wide operation frequency thanks to the widely separated TX and RX frequencies and the robustness against path mismatch and non-ideal clocking. Meanwhile, with only one set of switches in the signal path, high linearity is obtained without using a silicon-on-insulator (SOI) or high-voltage CMOS process. As described in Section III, the integrated broadband quadrature modulation clock generator is over-engineered, leading to higher DC power compared to some works in the table; the problem should be alleviated with a more optimized narrowband clock generator design or with a more advanced CMOS technology node. Similar to the situation of other CMOS circulator works, the heat dissipation of the passive IBFD core the circuit is low (∼0.4 mW in simulation), so the presented scheme may be applicable for quantum platforms when the clock generation is outside of the cryogenic fridge and/or is shared among multiple IBFD units. Lastly, it is also worth mentioning that, due to the simple construction of the presented scheme, a highly compact circuit area, when normalized to the square of wavelength, is achieved (Table I).

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TABLE I: Comparison with State-of-the-Art Integrated Circulators in CMOS

	This Work		[15]		[5]	[6]	[7]	[8]
	300K	4.2K	300K	4.2K				
Frequency (GHz)	3.4∼4.6		5.6∼7.4	5.8∼7.6	0.65∼0.85	0.86∼1.08	22.7∼27.3	50∼56.8
Fractional Bandwidth	30%		28%	26.9%	26.7%	17%	18%	14.6%
Minimum Isolation (dB)	32	14	18	17	15	25	18.5	20
Minimum TX-to-ANT Loss (dB)	3.0	1.9	2.2	1.3	1.7	2.1	3.3	3.6
Minimum ANT-to-RX Loss (dB)	3.2	2.0	2.2	1.3	1.7	2.9	3.2	3.1
Noise Figure (dB)	5.8/5.9$^{(a)}$	4.8/4.8$^{(a)}$	2.4	N.A.	4.3	3.2	3.3	3.2
TX-to-ANT IIP3 (dBm)	29.5	N.A.	>18.7	>18.1	27.5	50	20.1	19.4
ANT-to-RX IIP3 (dBm)	27.6	N.A.	>18.7	>18.1	8.7	30.7	19.9	19.0
Elimination of On-Chip TX-to-RX Coupling ?	Yes		No		No	No	No	No
RX Down-Mixing ?	Yes		No		Yes	No	No	No
Fully Integrated ?	Yes		Yes		No	Yes	Yes	Yes
DC Power $^{(b)}$ (mW)	48	42.6	12.4	10.5	59	170	78.4	41
Core Area (mm^2) (Wavelength Scale)	0.27 (λ^2/20778)		0.45 (λ^2/4727)		25 (λ^2/6390)	16.5 (λ^2/5789)	2.16 (λ^2/67)	1.72 (λ^2/18)
CMOS Technology	65-nm Bulk		40-nm Bulk		65-nm Bulk	180-nm SOI	45-nm SOI	45-nm SOI

$^{(a)}$ SSB mixer NF reported here. With TX off/on (0 dBm) and the homodyne RX down-conversion function included.
$^{(b)}$ Mainly from the modulation clock generator. The simulated power dissipation of our IBFD core circuit is ∼0.4 mW.

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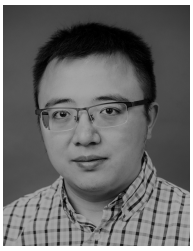

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