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Massachusetts Institute of Technology

Tungsten-Gated GaN/AlGaN *p*-FET with I_{max}>120 mA/mm on GaN-on-Si

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***Abstract*— This letter demonstrates Tungsten (W)-gated *p*-channel GaN/AlGaN heterostructure field effect transistors on a GaN-on-Si wafer grown by metal organic chemical vapor deposition (MOCVD). The choice of W as the gate metal over the more commonly used Mo induces larger turn-on voltage and lower gate leakage current. An annealing step at 500 °C in N_2 ambient was introduced to heal the damage introduced during the gate recess step which resulted in lower channel resistance. Long-channel W-gated *p*-FETs with $L_{SD} = 5.5$ μm and $L_G = 1.5$ μm exhibits an $I_{ON} \approx 25$ mA/mm, $I_{ON}/I_{OFF} > 10^3$. A scaled transistor of dimensions $L_{SD} = 1.2$ μm and $L_G = 100$ nm demonstrates an $I_{ON} \approx 125$ mA/mm, $I_{ON}/I_{OFF} \approx 10^4$, and $R_{ON} = 170$ Ω·mm.**

***Index Terms*— GaN, *p*-Channel, Transistor, CMOS**

I. Introduction

Over the last couple of years, development of high performance gallium nitride (GaN) CMOS technology has gained traction in pursuit of an energy-efficient GaN-based integrated circuits platform for power electronics, RF and harsh environment electronics [1], [2], [3], [4], [5], [6], [7], [8]. The primary bottleneck of the current approaches is the low current density of *p*-FETs which severely limits the operating speed of the circuits and thus the usability of such technology [9], [4], [5], [7]. Improving the current density of GaN *p*-FETs is an active area of research and has been quite challenging in particular on metal organic chemical vapor deposition (MOCVD)-grown GaN-on-Si devices [10], [11], [12], [13], [14], [15]. In most demonstrations, the current density is still below 10 mA/mm. Very recently, N. Chowdhury *et al.* used a self-aligned gate FinFET architecture to demonstrate a GaN *p*-FET based on GaN-on-Si with current density exceeding 100 mA/mm [16]. These transistors, though significantly advancing the state-of-the-art in GaN *p*-FET research, are extremely scaled with $L_G = 90$ nm and fin width of 40 nm, therefore severely limiting the operating voltage. In order to accommodate higher rail voltage operation for power and RF applications, there is a need to develop planar *p*-FETs with higher current density while maintaining reasonably scaled dimensions to ensure sufficient power handling capability.

Even though Metal-Oxide-Semiconductor (MOS) gated GaN *p*-FETs yield extremely low gate leakage in the range of few nA/mm, high ON-OFF ratio and enhancement mode (E-mode) operation, the maximum ON-current densities demonstrated in MOS GaN *p*-FETs thus far are limited to around tens of mA/mm [11], [15], [4], [12], [13]. In addition, for a typical MOS gate, trap charges at the oxide-semiconductor interface cause hysteresis in the current-voltage characteristics and significantly reduce the electrostatic control of the gate over the channel [5], [17], [18] hence the on-current density. The highest current densities in GaN *p*-FETs have so far been demonstrated using Schottky-gated FETs. K. Nomoto *et al.* reported a Mo Schottky gated *p*-FET with $I_{D,max} > 420$ mA/mm and f_T, $f_{max} \approx 20$ GHz using a molecular beam epitaxy (MBE)-grown GaN/AlN epitaxial structure with p^{++}-InGaN contacts and un-annealed Pd [19]. B. Reuters *et al.* demonstrated Mo gated *p*-FETs with > 40 mA/mm maximum drain current density utilizing MOCVD-grown GaN/AlInGaN heterostructure on sapphire substrate [20]. The use of gate metals with improved Schottky characteristics would increase the current density in these devices by improving the gate voltage drive.

In addition to the gate metal, the plasma-based etching typically needed during device fabrication has a strong impact on device performance. During the device fabrication, GaN *p*-FETs are typically exposed to two types of plasmas: (1) O_2 plasma during the resist cleaning steps (2) Cl_2/BCl_3-plasma during the recess step. It has been reported that Cl_2-based plasma induces damages to the *p*-GaN through the formation of nitrogen vacancies [21], [22], [23]. These etch-induced nitrogen vacancies not only compensate holes in the channel but also form a depletion region on the etched surface [22]. The oxygen plasma has been reported to induce shallow donor states which when ionized at room temperature not only compensate holes but also potentially make the *p*-GaN region weakly *n*-type [15]. Therefore, there is a need to develop a technology to heal the damages done by the plasma. This work proposes a post gate recess treatment with the intention of healing these damages.

The GaN/AlGaN platform on GaN-on-Si wafer has garnered significant attention for its ability to monolithically integrate GaN *p*-FETs with E-mode AlGaN/GaN *n*-FETs [16], [11], [15], [5], [10], [24]. This letter combines an improved Schottky gate metal, tungsten (W), with a high temperature healing process to demonstrate GaN *p*-FETs (Fig. 1(a)) on a GaN/AlGaN platform. To the best of the authors' knowledge, for the first time, a current density exceeding 100 mA/mm was demonstrated in planar GaN *p*-FETs on a MOCVD III-N platform.

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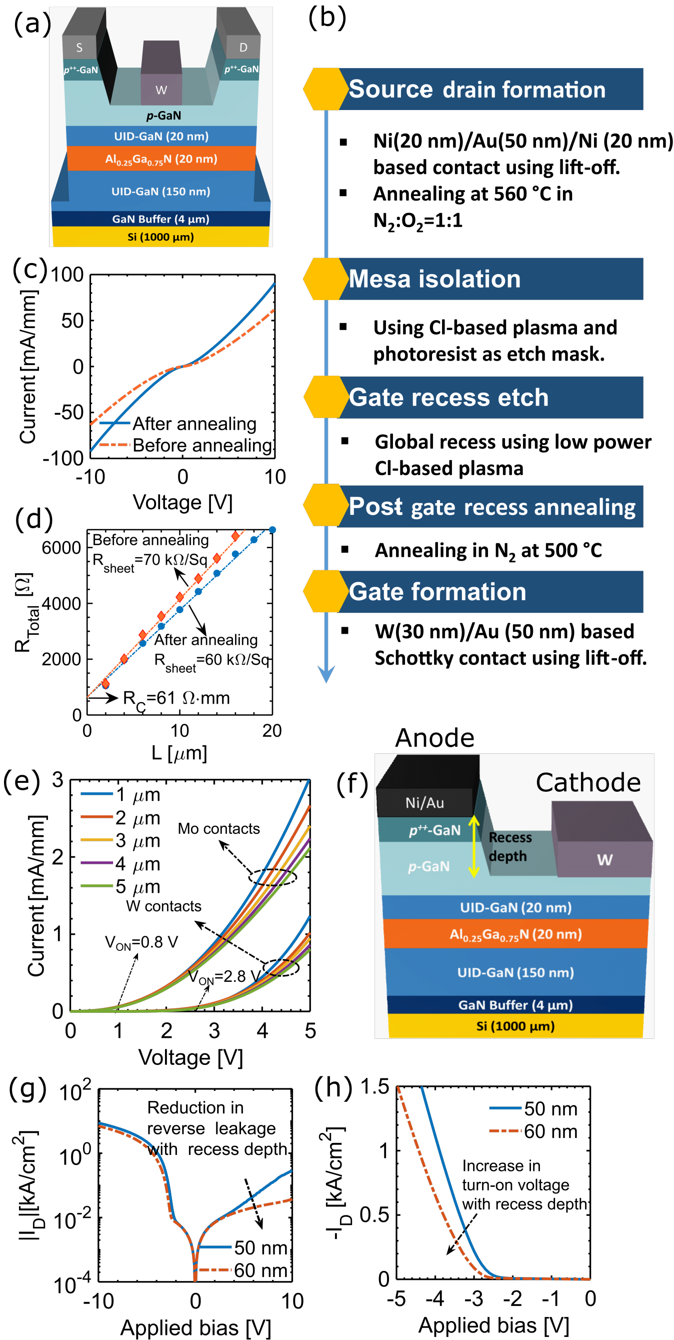

Fig. 1. (a) Schematic of the fabricated device structure. (b) Key processing steps for fabricating the Schottky-gated *p*-FET. (c) Current voltage characteristics of two ohmic contacts with channel recess depth of 55 nm and $L_{SD} = 1$ μm before and after annealing at 500 ℃ in N_2 environment. (d) Measurements of TLM structures with channel recess depth of 55 nm demonstrating an improvement in sheet resistance after the annealing. Current-voltage (I-V) characteristics of TLM structures based un-annealed Schottky contacts on p^{++}-GaN for different spacing (from 1 μm to 5 μm) (e) Mo *vs.* W. (f) Schematic of the fabricated *p*-type Schottky diode based on W-contacts. I-V characteristics of W contacts formed on *p*-GaN surface of different recess depth. (g) Semi-logarithmic scale showing a significant reduction in currents with recess depth. (h) Linear scale showing the increase in turn-on voltages with recess depth.

II. Epitaxial Structure and Device Fabrication

The epitaxial stack used in this work was grown by Enkris Semiconductor, Inc. on a 6 inch, 1-mm-thick Si (111) substrate using MOCVD method. The structure is as follows: 20 nm p^{++}-GaN (Mg: 6×10^{19} cm^{-3} with 2–3% activation at room temperature), 50 nm *p*-GaN (Mg: 10^{19} cm^{-3}), 20 nm unintentionally doped (UID)-GaN, 20 nm UID-$Al_{0.2}Ga_{0.8}N$, 150 nm UID-GaN, 3 μm buffer and Si substrate. The energy band diagrams and the details of the epitaxial structure can be found in Ref. [12], [13]. The two-dimensional hole gas density and hole drift mobility for the epitaxial structure are measured to be 8×10^{12} cm^{-2} and 15 cm^2/V·s, respectively, according to Hall measurements.

Fig. 1(b) shows the key processing steps. Source and drain contacts are first formed based on Ni (20 nm)/Au (50 nm)/Ni (20 nm) metal stack followed by thermal annealing in $N_2 : O_2 = 1 : 1$ environment at 560 °C for 40 min. During the annealing step, a 2 standard-liter-per-minute (SLPM) volumetric flow rate for both N_2 and O_2 was maintained. Due to the slightly Schottky character of the source and drain contacts, the contact resistance was found to be dependent on the voltage at which it is calculated. At around 10 V, the contact resistance obtained by linear transfer length method is found to be around 15 Ω·mm. Next, a blank etch is performed by Cl_2/BCl_3 Inductively Coupled Plasma-Reactive Ion Etching (ICP-RIE). This step forms the gate recess. Here, the top 20 nm Ni on the ohmic contacts serves as the etch mask and protects the ohmic region from the potential etch damage. The etch depth is controlled by the etch time. After the etch, a 500 °C annealing is performed in N_2 environment for 60 min. Fig. 1(c) shows the current-voltage characteristics of the ohmic contacts before and after the annealing step. Transfer length method (TLM) measurements were conducted on samples with channel recess depth of 55 nm, as shown in Fig. 1(d). After the N_2 treatment, the sheet resistance of the channel decreased by ∼15% to 60 kΩ/□, while the contact resistance remained constant at 61 Ω·mm. The channel sheet charge density was increased from to 5.9×10^{12} cm^{-2} (before annealing) to 7.0×10^{12} cm^{-2} (after annealing). The reduced channel resistance will allow for higher current levels in transistors. It is postulated that, the N_2 annealing step results in a reduction in the nitrogen vacancies that were originally formed during the gate recess etch step, reducing in this way the compensation of ionized Mg by nitrogen vacancies [22], [23]. Next, the Schottky gate was formed using a lift-off process.

In previous Schottky-gated *p*-FET demonstrations, Mo was used as gate metal [20], [25], [19]. According to Ref. [26], both Mo and W yield Schottky barrier heights in the range of 0.7 eV when deposited on a *p*-GaN surface. To experimentally study the Schottky characteristics (in terms of Schottky turn-on voltages and leakage currents) of these metals on p^{++}-GaN surface (which serves as the top layer of the epitaxial structure used in this work), W and Mo contacts were deposited on p^{++}-GaN and current-voltage characteristics of the gate electrodes were measured as shown in Fig. 1(e). It also shows that Mo and W yield turn-on voltages of 0.8 V and 2.8 V respectively. Moreover, the current density at a specific applied bias for W-contacts is lower than Mo-contacts. Since the Schottky gate will be made on the recessed *p*-GaN surface, it is necessary to study Schottky contacts formed on the etched surface. Towards that end, *p*-type Schottky diodes are fabricated with different

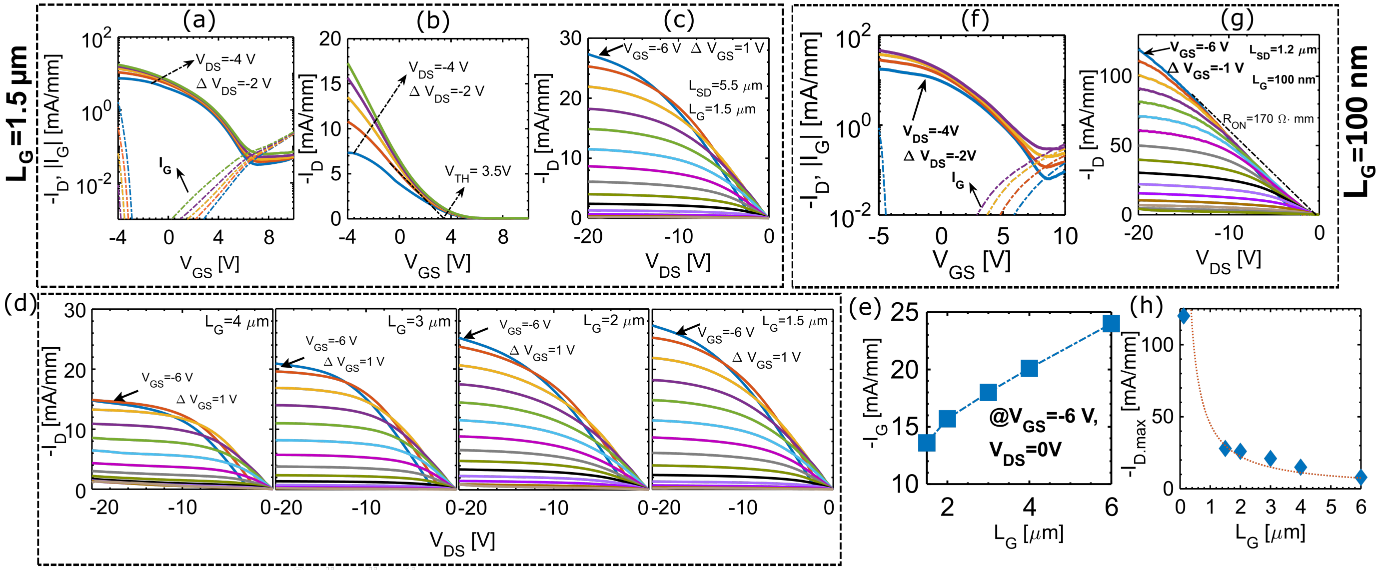

Fig. 2. (a)–(e) Long-channel, (f)–(g) short-channel W-gated GaN/AlGaN *p*-FETs. For long-channel transistors: (a) Semi-logarithmic plot of I_D *vs.* V_{GS} at different V_{DS} demonstrating an ON-OFF ratio of $> 10^4$. (b) I_D *vs.* V_{GS} characteristics in linear scale showing a threshold voltage of -3.5 V. (c) I_D *vs.* V_{DS} characteristics demonstrating an ON-current density of 25 mA/mm at $V_{DS} = -20$ V. (d) Output characteristics of *p*-FETs with different channel lengths showing the impact of scaling on the ON-current density. (e) Impact of channel length on the gate leakage of *p*-FET. For short-channel transistors: (f) Semi-logarithmic plot of I_D *vs.* V_{GS} at different V_{DS} demonstrating an ON-OFF ratio of $> 10^4$. (g) I_D *vs.* V_{DS} characteristics demonstrating record ON-resistance of 170 Ω·mm and ON-current density of 125 mA/mm at $V_{DS} = -20$ V. Finally, $I_{D,max}$ as a function of gate length scaling was summarized in (h).

recess depth (see Fig. 1(f) for diode schematic). Fig. 1(g)–(h) shows that the Schottky characteristics of the W contacts improves with the recess depth in terms of leakage current and turn-on voltages. These results clearly demonstrate that W yields a better Schottky behavior than Mo, hence it is chosen as the Schottky gate metal in this work.

III. Results and Discussion

Fig. 2(a) shows the I_D *vs.* V_{GS} characteristics of a long-channel device with $L_{SD} = 5.5$ μm and $L_G = 1.5$ μm, in semi-logarithmic scale exhibiting an ON-OFF ratio of $\sim 10^3$. It also shows that at highly positive gate voltages (channel depletion regime), the gate leakage dominates because of the current between the gate and the drain electrodes. A threshold voltage of 3.5 V was obtained, as shown in Fig. 2(b). Fig. 2(c) plots the I_D *vs.* V_{DS} characteristics of the device showing $I_{D,max}$ of 25 mA/mm at $V_{DS} = -20$ V and $V_{GS} = -6$ V. Fig. 2(d) highlights that, through channel length scaling, the current density of the transistors may be significantly improved. It is also observed that, gate leakage becomes dominant in long-channel transistors. Particularly for $L_G = 6$ μm, the transistors could not be turned off properly because of the large gate area leading to high gate leakage current. This is because gate leakage current scales with gate area ($W \times L_G$). For a fixed width (W) of the transistor gate, the gate leakage current can be significantly suppressed by scaling the L_G, as shown in the inset of Fig. 2(e).

To this end, aggressive gate length scaling was pursued. Fig. 2(f) shows I_D *vs.* V_{GS} characteristics of a short-channel transistor ($L_G = 100$ nm, $L_{SD} = 1.2$ μm) in semi-logarithmic scale with $I_{ON}/I_{OFF} > 10^4$. Although gate leakage current in this device is significantly suppressed compared to long-channel transistors thanks to the lower gate area, in all of these devices, the ON-OFF ratio is limited by the gate leakage current. Fig. 2(g) shows the output characteristics, exhibiting $I_{D,max} = 125$ mA/mm and $R_{ON} = 170$ Ω·mm. A breakdown voltage of 30 V was obtained. It should be noted that, the maximum negative gate voltage (V_{GS}) that can be applied to the reported *p*-FETs is -6 V whereas in previous Mo-based Schottky-gated *p*-FET demonstrations it was -2 V, thanks to the W-based Schottky contact. As shown in Fig. 2(h), The maximum drain currents of *p*-FETs in this study are found to roughly follow the classic $1/L_G$ scaling law. E-mode operation could be obtained through a deeper gate recess etch, or the introduction of hydrogen or oxygen plasma treatment in the gate region [11], [27], [15].

IV. Conclusion

This letter demonstrates scaled Schottky-gated *p*-channel GaN/AlGaN HFETs based on a GaN-on-Si wafer. Tungsten has been identified as a better gate metal than Mo because of its greater turn-on voltage and better Schottky characteristics. A post-gate-recess annealing at 500 °C in N_2 ambient is introduced to boost the current density of the *p*-FET by potentially healing the etch-induced damage. The reported scaled Tungsten-based Schottky-gated GaN *p*-FETs with $L_G =$ 100 nm and $L_{SD} = 1.2$ μm exhibits $I_{D,max} \approx 125$ mA/mm, $I_{ON}/I_{OFF} > 10^4$, and $R_{ON} = 170$ Ω·mm.

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