A 2-D-Scalable Third-Harmonic Radiator at 300 GHz in 22 nm FinFET technology

by

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Abstract

The Terahertz (THz) band exhibits potential for novel applications and improvements to existing systems such as spectroscopy, imaging, and high-speed communications. However, the lack of high-power sources at this frequency range hinders the wide-scale adoption of these technologies commercially. This THz gap exists due to the inability of electronic and optical techniques to generate high power levels at this frequency range. Novel generation techniques have been and continue to be investigated to improve the performance of these sources. In this work, we present a Terahertz (THz) radiator at 291.3 GHz. The footprint of the unit radiator is half-wavelength at the radiation frequency, which enables 2-D scalability. Passive coupling is implemented between the radiator elements for de-centralized phase locking and free-space power combining. The proposed radiator is implemented on Intel 22 nm FinFET (FFL) technology, which enables high-performance high-speed circuits. The presented radiator is an addition to the state-of-the-art radiators and combines several advantages of previous designs.

Thesis Supervisor: Ruonan Han
Title: Associate Professor of Electrical Engineering and Computer Science

Acknowledgments

I would like to thank prof. Ruonan Han for his support and guidance and granting me the opportunity to explore this direction of research.

Special thanks goes to the members of Terahertz Integrated Electronics Group; Mohamed, Nathan, Mina, Ibrahim, Eunseok, Xibi, and Jinchen, for the useful discussions, whether technical or not, and offering help and advice when needed.

The warmness and kindness of my friends have never failed to make me feel like I belong, and the casual walks and hang-outs have been essential to maintaining my balance and sanity. I would like to show my appreciation to the Egyptian community, the Sidney Pacific graduate community, and special thanks to my friend James.

Last but not least, I would like to thank my family for their never-ending trust and support.

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Chapter 1

Introduction

1.1 THz Waves

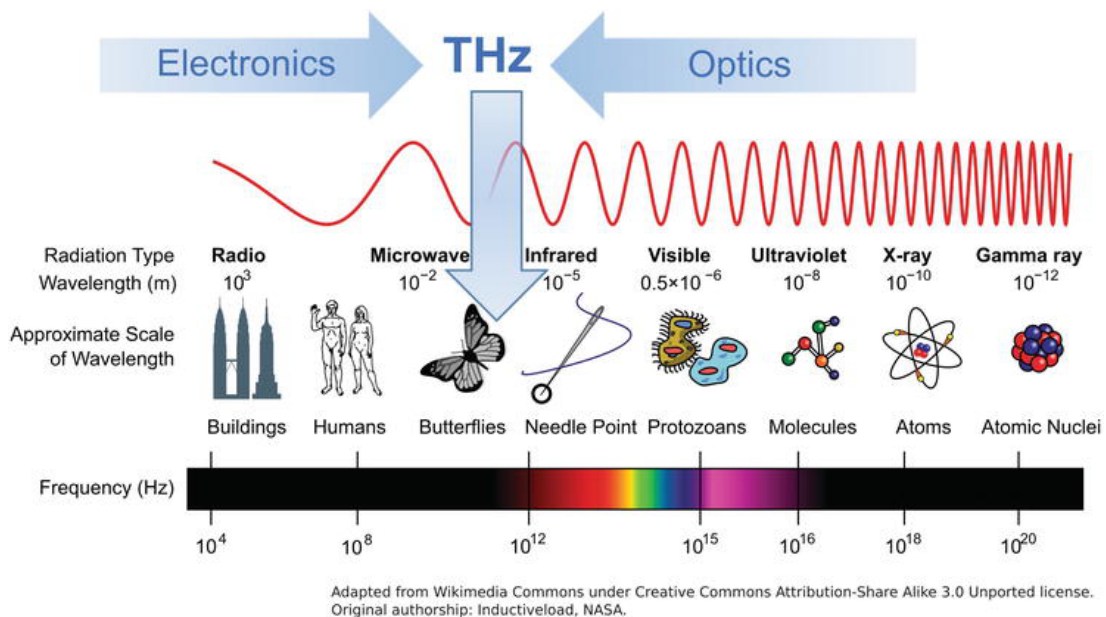Figure 1-1: The terahertz (THz) gap. Both electronics and photonics contributed to the development of THz technology.

THz waves are electromagnetic (EM) waves which lie between 300 GHz and 3 THz at the interface between electronic and optical design spaces as shown in 1-1. This frequency band offers unique opportunities which encourage the pursuit and adoption of THz systems for many applications. The small sub-millimeter wavelength

offers opportunities for integration and scalability, such as the realization of large-scale antenna arrays with true time-delay feeding networks. Integrating high-density electromagnetic structures on chip opens the door for more innovative EM-circuit co-designs in small cost-effective form factors which are suitable for commercial products. Another benefit of the diminishing size is the ability to include more functional blocks in the same area.

1.2   THz Waves Applications

The applications of THz waves span several domains due to some physical and chemical phenomena characteristic to that frequency range [1]. Solids exhibit lattice vibrations and polar materials have resonances in the THz band. THz waves also posses small wavelengths, hence offer small lateral resolutions for imaging purposes. Moreover, they can penetrate obscuring objects such as fabrics and plastics. The spectral fingerprints of some explosive materials and prohibited substances are among those detectable by THz spectroscopy. All of this has made THz a prime candidate for standoff security imaging [2].

The dielectric properties of water, a polar substance, at this frequency range yield easily measurable reflective properties of tissues based on hydration levels. This sensitivity to the water content and the non-ionizing properties of THz radiation enable the monitoring of the formation and development of skin burns, corneal pathologies and cancer [3].

Several specialized applications have been recently proposed [4]. For example, some materials exhibit sharp resonances at THz frequencies which enabled the realization of high precision clock systems [5]. The small wavelength and the large available bandwidth have been utilized to improve radar resolution [6], and to realize high-speed communication links [7]. THz imaging has also attracted a lot of interest especially, for security and space applications [8]. Moreover, the versatility of THz integrated systems on silicon technologies has been demonstrated in the construction of a beam steerable THz-ID tag with an integrated cryptographic processor for
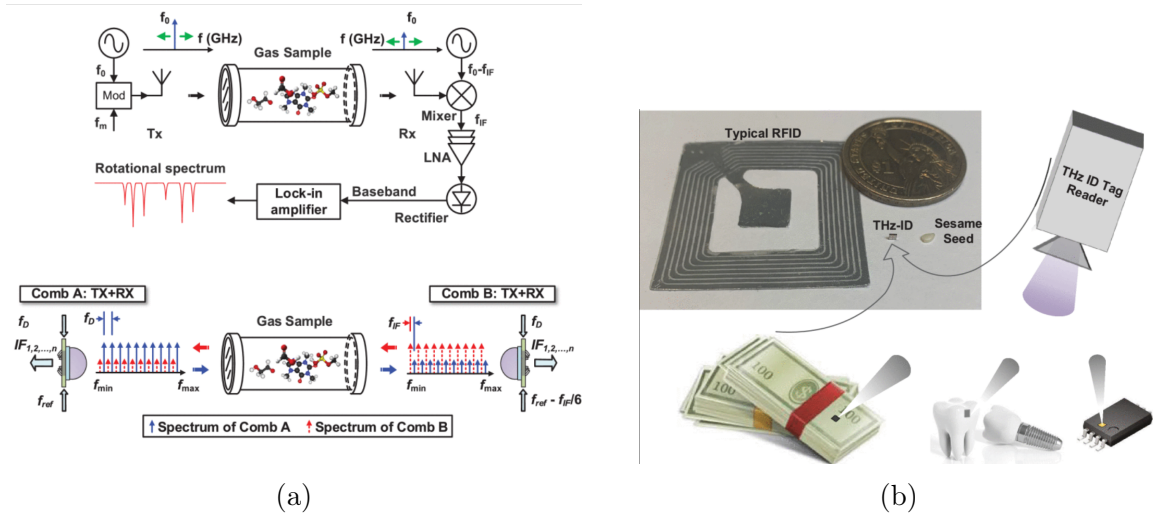
Figure 1-2: (a) Rotational spectrometer for molecular analysis [5]. (b) Cryptographic THzID tag [9]

additional security [9].

1.3   THz Waves Sources

As THz frequencies occupy an intermediate position between electronics and optics design spaces, it has leveraged techniques from both domains. Unfortunately, this adoption has found impeding challenges. As shown in 1-3, the power output from both solid-state and optical sources decreases when approaching the THz band, leading to what is known as the THz gap.

Currently, there are several ways to generate THz waves [10]. Thermal excitation leads to the emission of THz waves in the form of blackbody radiation. Optical techniques include lasers such as gas, semiconductor and quantum cascade laser. The mixing of two optical frequencies in a non-linear medium such that the generated beating frequency lies at the desired THz frequency. Vacuum electronics which rely on the synchronization between electron beams and electromagnetic waves to transfer the kinetic energy to the electromagnetic field are able to generate high powers at THz frequencies tunable over a broad bandwidth. Unfortunately, they suffer from the drawback of being 3-D bulky structures. Another technique is to use solid-state elec-
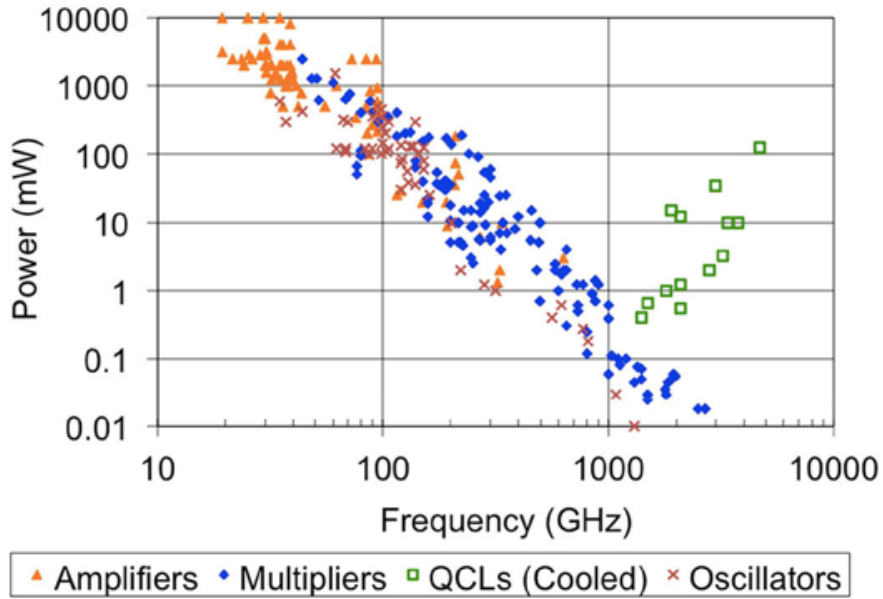
Figure 1-3: The terahertz (THz) gap. Both electronics and photonics contributed to the development of the THz technology [11].

tronics such as Gunn diodes and transistors. The recent developments in transistor technology have dramatically increased the cut-off frequencies of transistors either by using III-V materials or down-scaling the channel length. This has led to a surge in the integrated THz sources which will be discussed in the next chapter.

Chapter 2

Integrated circuits THz radiators
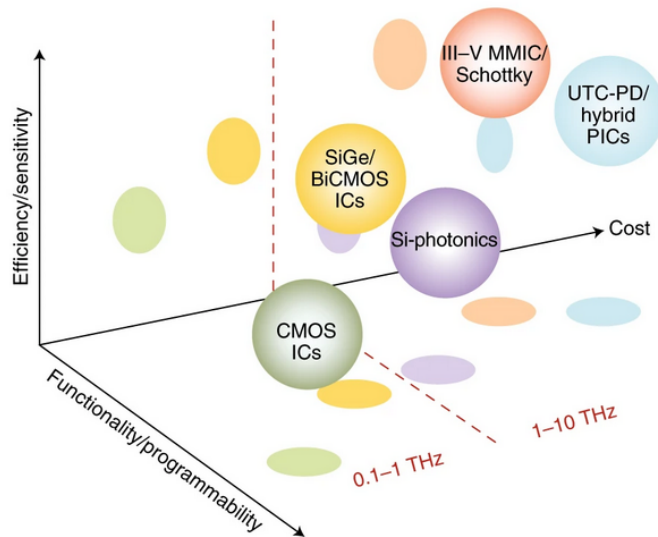
Figure 2-1: Progress of THz sources in the past decade showing how a selected set of integrated THz technology has evolved over the past ten years in its ability to generate continuous-wave THz signals at room temperature [12].

2.1 Non-linear harmonic generation in THz oscillators

One of the major obstacles slowing down the emerging THz systems is the lack of high-power THz sources.This bottleneck has steered researchers to the investigation and

the development of novel, more efficient power generation techniques. Intense efforts have been made to progress the state of the art on the electronics side, as they offer low-cost good efficiency platforms as shown in 2-1. In addition, the unoccupied area below and around the passive elements allows the inclusion of more active components to enable the integration of more advanced functionalities in order to realize complete chip-level systems.

A prevalent technique in solid-state THz sources is to leverage the non-linear behaviour of devices for harmonic generation. A low-frequency signal, generated either externally or on-chip, can be input to a chain of frequency multipliers to output a THz signal [13]. The design of these multiplier chains is challenging as their performance is strongly dependent on the process, the biasing conditions, and the input power. For on-chip oscillators, the periodic large-signal non-linear behavior of oscillators leads to the generation of the harmonics of the fundamental oscillation frequency. One way of implementing this is the extraction of the nth harmonic at the common node of an n-push oscillator, where at the common node all the harmonics cancel out except for the nth, which can then be drawn out by connecting it to a load, such as an antenna. One instance of this is the push-push oscillator in [14], which was able to generate a power of -47 dBm at 410 GHz on 45 nm low-leakage digital CMOS process, by extracting the second harmonic from the common node of a differential pair connected to an on-chip patch antenna as shown in 2-2a. In [15], it was shown that transistors have a favorable complex voltage gain which maximizes their performance, and hence, deviations from this operating point has major impact on the limits of the oscillation performance when placed in an oscillator. The triple-push oscillator, shown in 2-2b, was thus designed for optimal conditions to maximize the oscillation frequency and power, and a third-harmonic power of -7.9 dBm was extracted from the 482 GHz on 65 nm CMOS. In [16] the quadrature oscillator in 2-2c was operated as a quad-push oscillator and a fourth harmonic power of -36.6 dBm was extracted at 553 GHz on the low-leakage 45 nm CMOS process. Unfortunately, the aforementioned techniques face a constraint, as a single oscillator can only generate limited power, and the irregular layout of these architectures make them difficult to array, particularly in two

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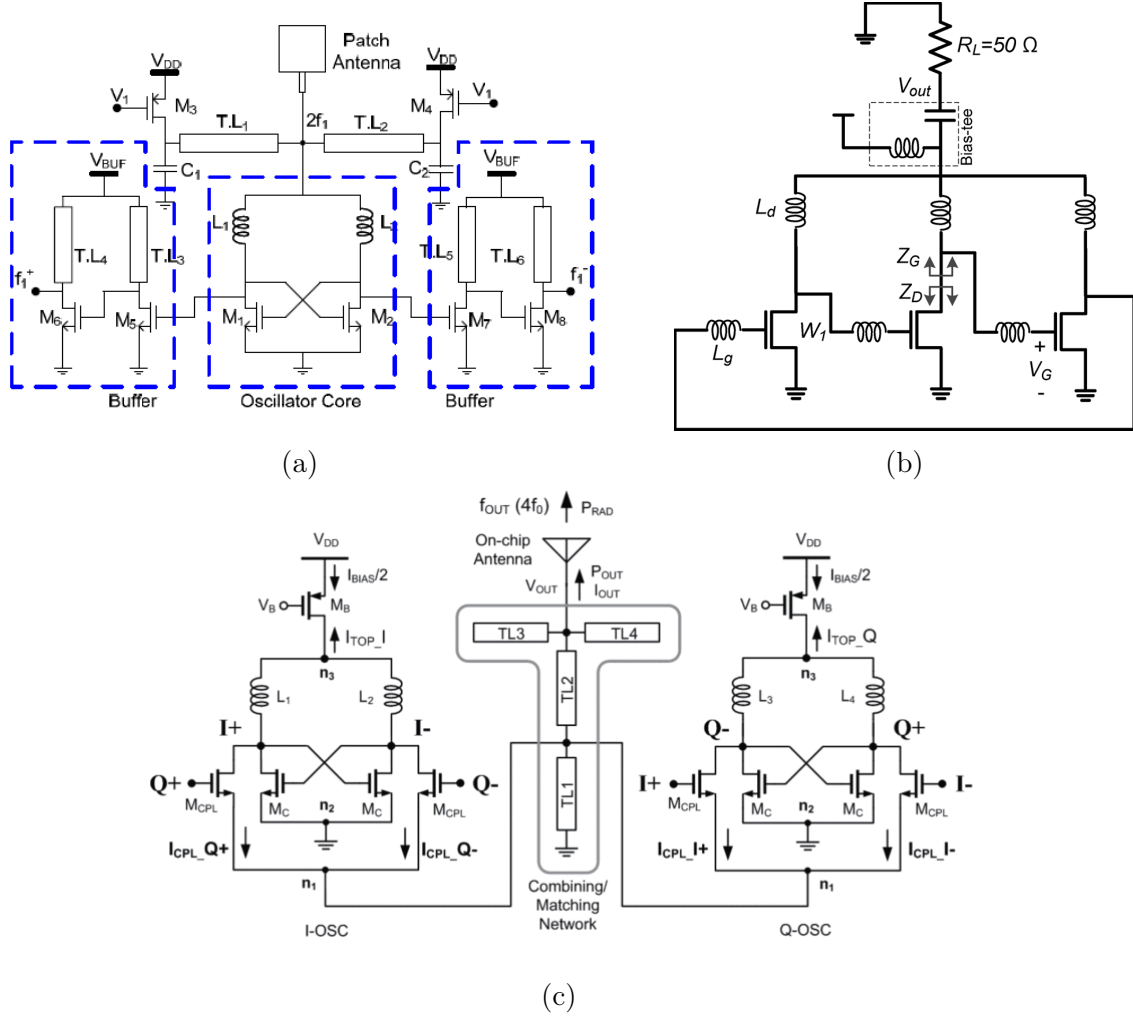
Figure 2-2: (a) Push-push [14] (b) Triple-push [15], and (c) Quad-push [16] oscillators exhibit the generated harmonics of oscillators for THz generation.

dimensions.

An alternative popular method of harmonic generation that overcomes this constraint is to integrate the transistors in a multi-functional electromagnetic structure. In this case, the EM structure acts as a low-loss resonator at the fundamental oscillation frequency but acts as an antenna at the harmonic of interest, which is then radiated to free space while suppressing the radiation at all the other harmonics. To build a successful radiator element, the electrical length of the pitch should be half wavelength at the radiation frequency, in the tiling direction, to eliminate grating lobes, as shown in 2-3a. The advantages of this approach are its scalability and efficiency. It avoids the requirements of having an external source and the non-efficient

Figure 2-3: (a) Conceptual 3rd harmonic unit radiator. (b) Array of radiators and free-space power combining. (c) Total coherent radiated power versus frequency for some THz radiators [4]

multiplier chains on one hand, and it has a regular layout compared to n-push oscillators. A unit radiator can be designed in a way that allows tiling and improves the effective isotropic radiated power (EIRP) two folds, once in terms of the radiated power and another in terms of the increased gain of the array factor. The increased n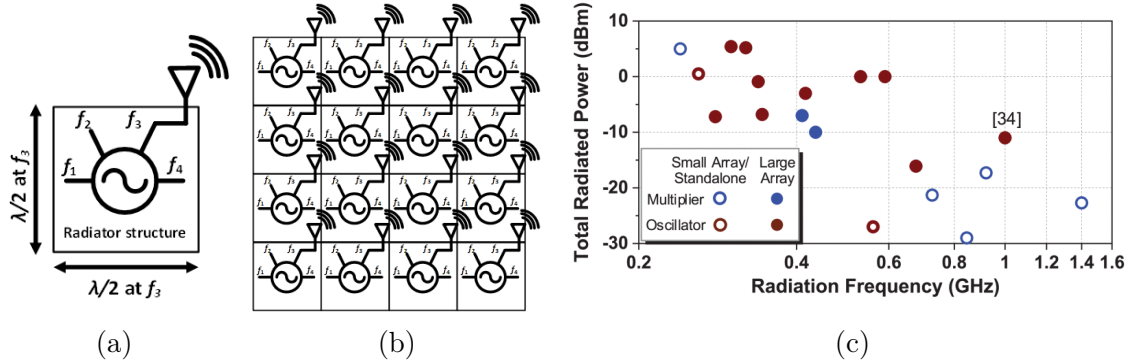umber of locked oscillator also the improves the phase noise of the generated signal as the array scales up. Maintaining a steady phase relationship between the radiators is essential for free-space power combining which eliminates the need for a power-combining network. Several locking mechanisms currently exist, either active locking using phase-locked loops [17] or passive coupling [18]. Fig. 2-3c shows the performance of several THz radiators in the literature employing the aforementioned techniques.

2.2   Return-path Gap Coupler

One successful way of building harmonic radiators is to use differential oscillators with a return-path gap coupler (RPGC). Fig. 2-4 shows the first radiator to use this technique. The gap coupler is a slotline in the feedback path of the transistors. This slotline can only sustain a differential mode in this frequency range, which forces the two oscillating transistors to oscillate differentially and suppresses common-mode oscillation as shown in 2-5a. The folded slots act as low-loss resonators at the funda-
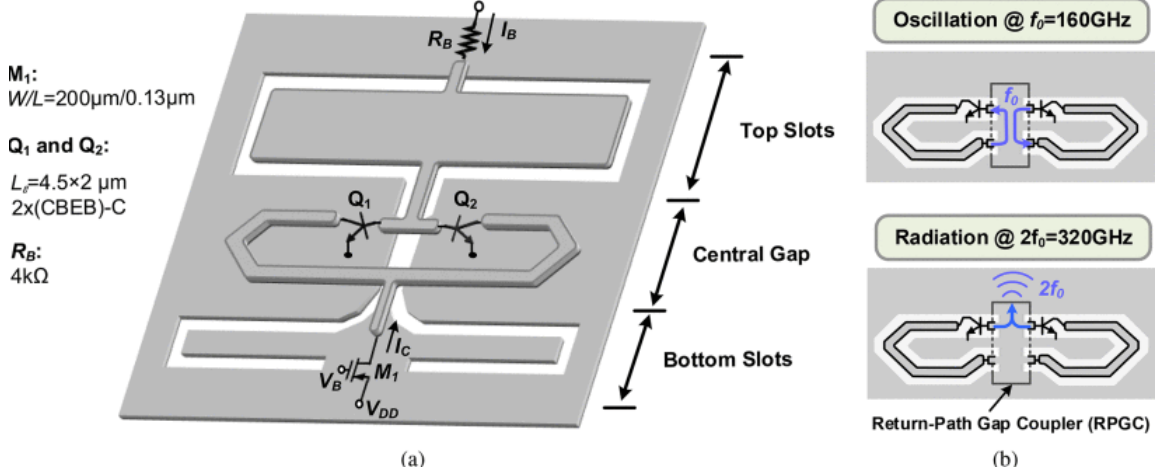
Figure 2-4: Second harmonic RGPC 320 GHz radiator

mental frequency, but the slot between the bases and the emitters operate as a folded slot antenna at the common-mode second harmonic. The differential operation allows us to apply a perfect-E symmetry plane at the fundamental frequency, and odd multiples, reducing the oscillator to the self-feeding oscillator in 2-5b which is designed for maximum oscillation activity. In order to maximize the oscillation power of the transistor, the voltage gain of the transistor should have a phase $\angle A$ equal to [17]:

$$\angle A = \angle - (Y_{21} + Y_{12}^*) \tag{2.1}$$

$$Z_0 \ sin(\phi_{TL}) = \frac{Im(A)}{Re(Y_{11} + A \ Y_{12})} \tag{2.2}$$

where Y_{ij} are the Y-parameters of the transistor, Z_0 and ϕ_{TL} are the characteristic impedance and electrical length of the feedback transmission line, with additional corresponding reactances, Y_1 and Y_2 at the base (gate) and the collector (drain), respectively.

In order to lock multiple radiators together to form an array, passive transmission line coupling has been used to lock their phases together in each row, while a PLL was used to synchronize the rows together. This lead to a 4×4 element radiator at 320 GHz with 3.3 mW of radiated power in 130 nm SiGe technology.

This concept of RPGC is the core principle behind several other radiators that have since emerged. Fig 2-6a shows a Fourth harmonic radiator at 1 THz [18]. The
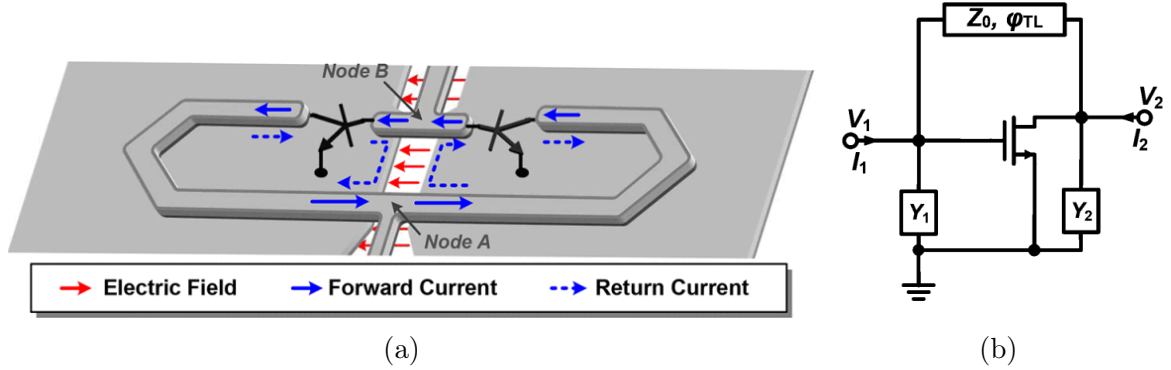
Figure 2-5: (a) Differential return gap-coupler operation for the feedback loop of the oscillator. (b) Simplified half-circuit model of the self-feeding oscillator.[17]

oscillator retained the differential fundamental oscillator but branched the EM structure so that radiation only happened at the fourth harmonic. The folding of the slots at the boundaries of the cell enabled passive coupling between unit-cells in both directions, to maintain phase locking without any additional active circuitry, which improved the power efficiency. The final radiator consisted of 6×7 radiators on a 130 nm SiGe technology, which radiated -10.9 dBm of power.

Another recent development is the third harmonic radiator shown in 2-6b [19]. The RGPC structure remained unchanged. However, the meandering of the slots in this configuration enabled radiation from the vertical slots only at the third harmonic. The output power at the third harmonic was boosted by using positive harmonic feedback between the first and third harmonics and the suppression of the second harmonic. Since the third harmonic operates differentially, there was possible loading from the gate to the drain through the feedback loop at the third harmonic. This has been circumvented by using the bottom resonator as an isolation stub for the gate at the third harmonic. One drawback of this structure was the large pitch in the vertical direction which made it untile-able and limited the output power. The final structure is a 4×2 array on 40 nm bulk CMOS technology which radiates -16.1 dBm of power at 670 GHz.

Given the previous designs, the harmonic to be radiated should be carefully chosen; the generated power generally decreases with increasing harmonic numbers, but using
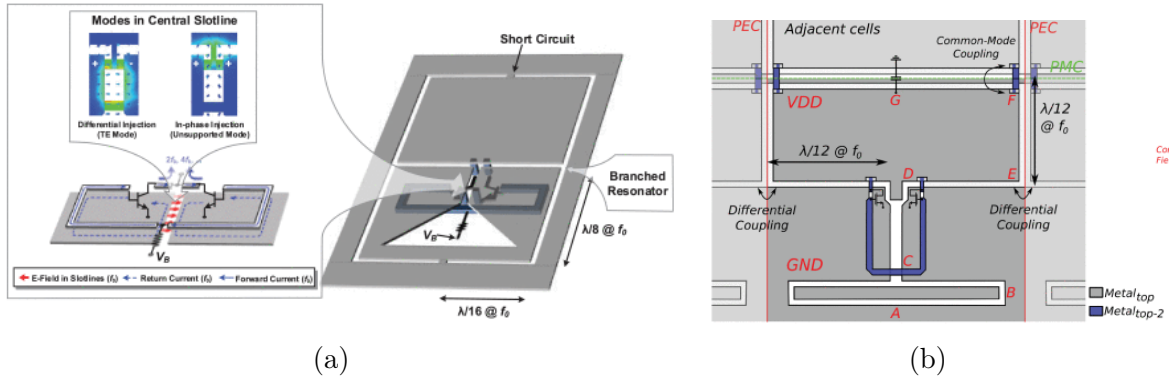
Figure 2-6: (a) Fourth [18] (b) Third [19] harmonic RGPC radiators.[17]

a small harmonic means that the oscillation happens close to f_{max} of the transistors, the maximum frequency at which the transistor is active. As the frequency of the fundamental oscillation approaches f_{max} the output voltage swing decreases, which in turn stifles the required non-linear behavior of the oscillator.

2.3   Intel 22FFL Technology
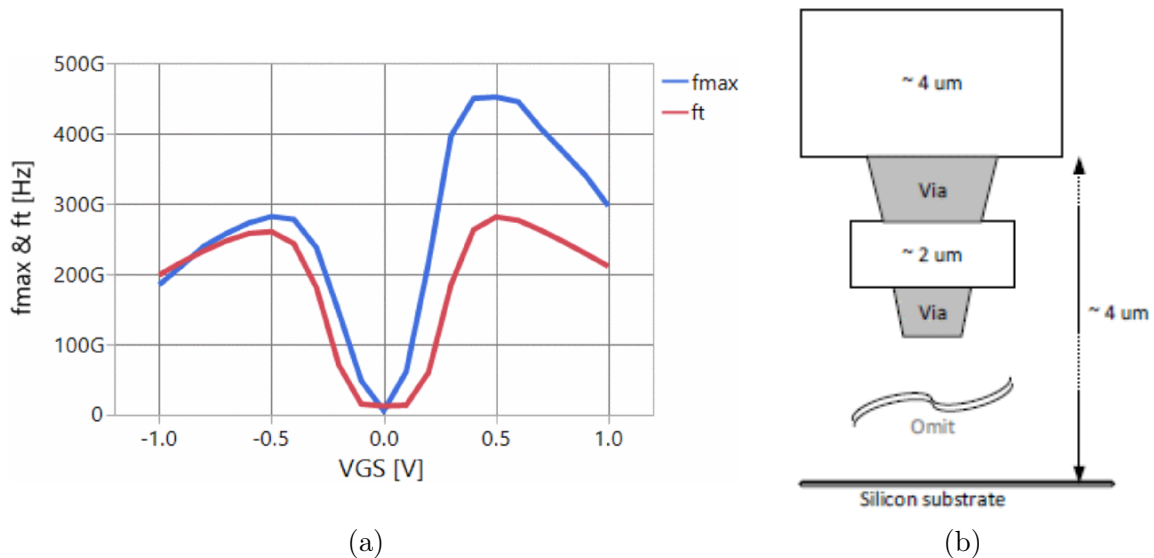
Figure 2-7: (a) f_{max} of 22FFL RF transistors (b) Intel 22FFL RF back end of line.[20]

The candidate technology for this project is Intel's recent 22FFL technology [20]. It boasts RF-specialized FinFETs with an f_{max} up to 450 GHz for the NFET, as shown

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in 2-7a. The metal stack, shown in 2-7b, offers one thick and one ultra-thick metal layers which enable the realization of EM structures with low conductor loss. This increases the quality factor of the resonator at the fundamental resonance, leading to a larger output swing and a higher frequency of operation. This also improves the radiation efficiency of the antenna mode at the 3rd harmonic. One challenge in this technology is the high loss in the silicon substrate as power is extracted from the substrate side in backside radiation, which is then coupled to free space using a silicon lens. This could could be mitigated by thinning the substrate to minimize these losses if they are found to be too detrimental. Another challenge of this technology is the limited supply voltage ($\leq 1V$). This poses a limit on the generated power from a single radiator unit and requires the inclusion of a large number of radiators to achieve a high output power at a significant area cost.

Chapter 3

Proposed radiator

3.1   Oscillator design

The proposed unit radiator is a pair of differentially oscillating transistors loaded by the multi-functional EM structure shown in 3-1a. At the fundamental frequency, the feedback path of each transistor is formed by the transmission line loop which is coupled to the slotline in the ground plane. This slotline can support only differential excitation in the frequency range of interest and hence the common mode oscillations are suppressed [17]. Fig. 3-1b shows the equivalent differential half circuit model. It is assumed that the slotline length enclosed in the feedback loop is of short electrical length and can be neglected. The EM structure resonates at the fundamental frequency ($\lambda/2$ mode) of the resonator.

The self-feeding oscillator maximizes the output power of the transistor which leads to the strong generation of harmonics [17]. For the current design the required angle for the voltage gain is 156°, and $Z_0 \sin \phi = 56.54$. A slotted-microstrip feedback transmission line of characteristic impedance 70 Ω is implemented which corresponds to an electrical length of 54°. This design point eliminates the need for the additional reactance at the gate. The required 30 fF capacitor at the drain can be obtained by slightly detuning the resonator off resonance.
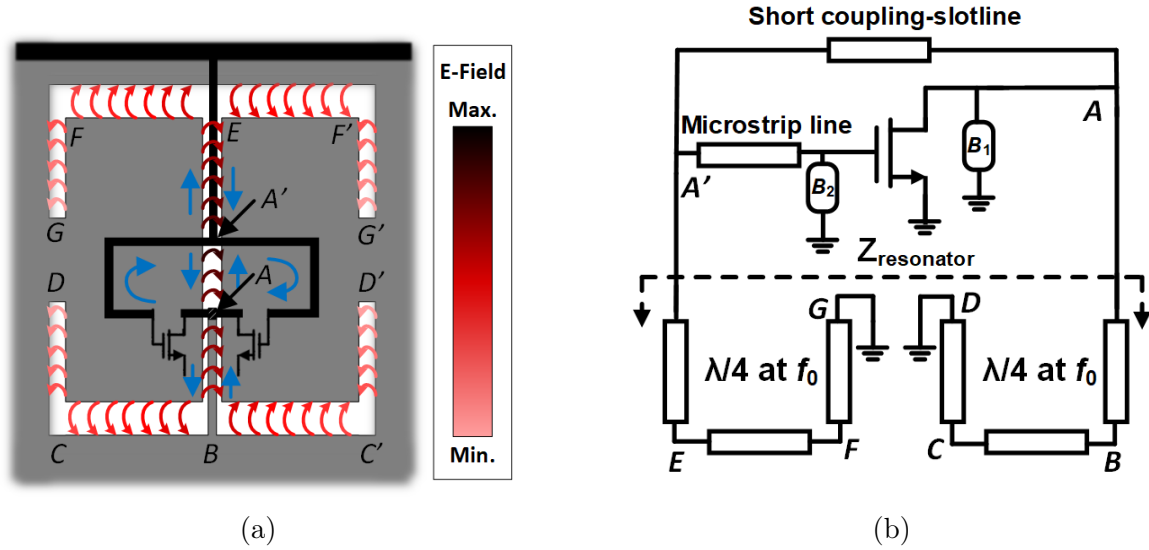
Figure 3-1: (a) Proposed simplified unit radiator; (b) Equivalent half circuit model.

3.2 Multi-functional electromagnetic structure design

Fig. 3-2a shows the field distribution of the vertical slots at the fundamental frequency to be out of phase with that of the central one, which increases the tank impedance by reducing the radiation loss. At the second harmonic, all the CPW lines carry the even mode which doesn't contribute to radiation as shown in 3-2b. Fig. 3-2c shows that at the third harmonic, the field distributions of the $(3\lambda/2)$ mode in all the vertical slots are in phase hence strong radiation is obtained. The proposed boundary conditions for the unit cell play two important roles. First, they cause each two adjacent horizontal slots of neighboring cells to support the even CPW mode which cancels out their radiation in the far field at all harmonics. In addition, they lock the phases of the oscillators together such that the vertical slots emit broadside backside radiation. The electrical length of the pitch in this case is $\lambda/2$ in both directions which suppresses the grating lobes in the array factor and enables 2-D scaling for a narrow beam.

The EM simulations for the unit radiator with the proposed boundary conditions are carried out in HFSS in 3-3a. The results in 3-3c show that the resulting differential peak impedance at the resonance is 150 Ω. The limited quality factor arises mainly from 3 sources. The first is the conductor loss which has already been minimized by
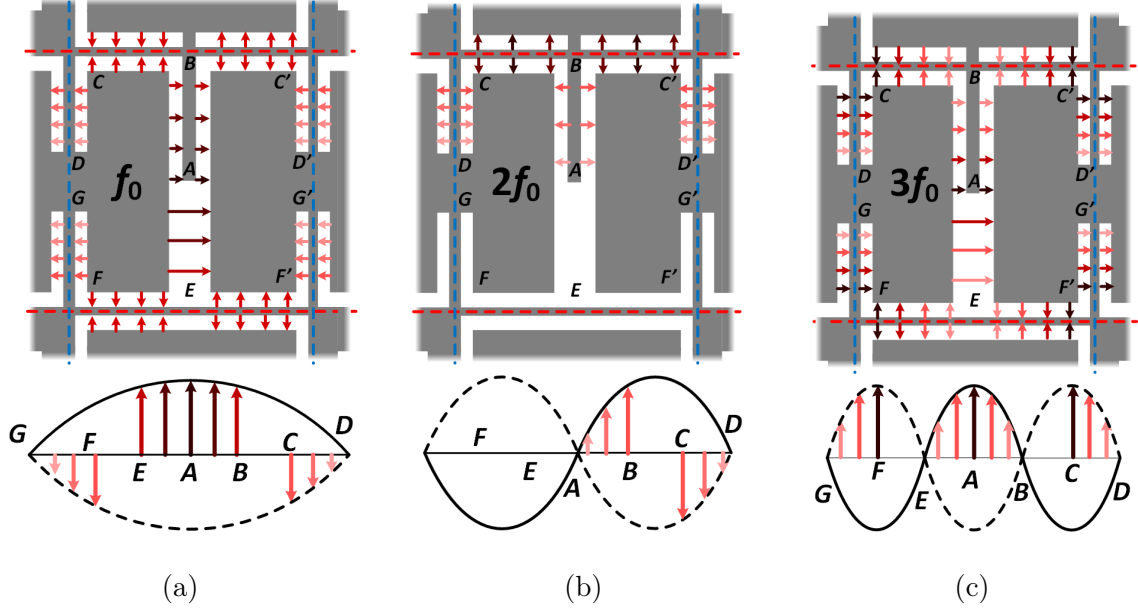
Figure 3-2: Resonator field distribution for the (a) First, (b) Second, and (c) Third Harmonics.

implementing the EM structure on the top, thickest metal layer. The second is the eddy current losses in the low-resisitivity silicon substrate which can only be improved by substrate-thinning, which will not be explored in this project. The third is the unequal field distribution at the central and outer vertical slots which leads to only a partial cancellation of the electric field and incurs additional losses through radiation. The structure in 3-3b compensates for this by shifting the outer slots to the inside on the upper side of the unit cell. The outer vertical slots are then elongated to enhance the cancellation. In this case, The differential tank resistance is in excess of 460 Ω which does not significantly load the transistors enables strong oscillations, while at the third harmonic the impedance is suitable for extracting power from the transistors. To understand the impact of the substrate losses, the elongated structure was simulated with a loss-free silicon substrate. The results in 3-3c show that the substrate losses are significant and further enhancement in radiation cancellation would lead to diminishing returns in terms of the total loss.

The feedback transmission line is implemented as a microstrip line on the two top thick metal layers to minimize the conductor losses in the line. The ground below the microstrip line is slotted as the proximity of the two metal layers requires slotting
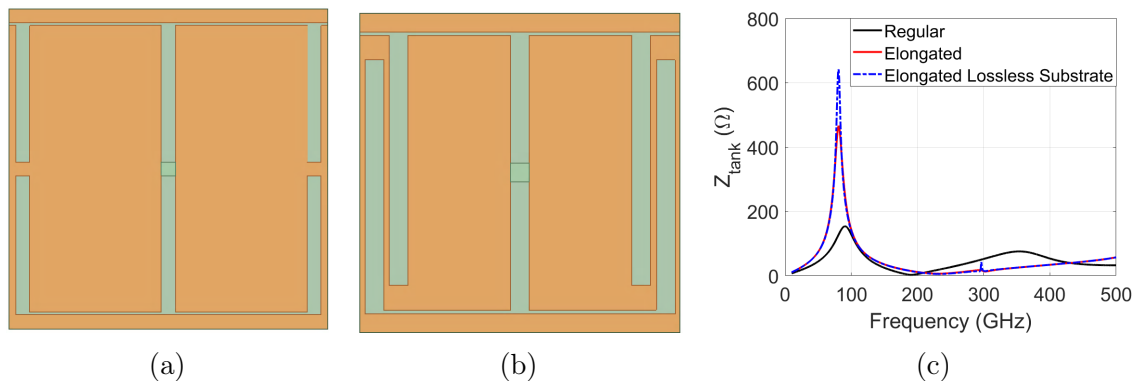
Figure 3-3: Simulation environment for (a) Regular (b) Elongated unit cells. (c) Tank impedances.

the ground to obtain a high characteristic impedance. Bridging strips are placed at discontinuities and long sections to suppress the excitation of the slot mode.

Passive coupling is used in the unit cells as it has the advantage of no power consumption and being 2-D scalable. The perfect H-boundary conditions are enforced by using air-bridges on a lower metal layer. The perfect-E boundary is enforced by extending the upper horizontal slot all the way to the edge of the unit cell. If any oscillation happens in the undesired modes, the boundary conditions greatly shift the fundamental resonance frequency of the tank, leading to the suppression of these oscillations as they happen far away from the maximum power conditions.

Extending the upper horizontal slots all the way to the edge of the cell enables the simple biasing of the transistors. As two back to back rows are formed by mirroring the unit cells. All the drains of the transistors of those two rows are connected to the floating strip using vias. The strip is then fed by pads on the two sides connected to the supply. The floating strip is built on a thick metal layer and is wide enough to support the large current required by the two rows of the radiating array. The other horizontal edge of the EM structure however is connected to the sources of each row of transistors, hence it is connected on both ends to the ground pads. Moreover, the grounds of all the array rows are connected using the air-bridges. This robust power routing network adds redundancy and further enables the scalability of the radiating structure and the integration of a large number of unit cells. The gates are connected

to a biasing line on the lower metal layers and are biased from the two pads at the bottom of the array.

3.3 Simulations and results

Both the drain and gate nodes generate signals at the third harmonic that are fed to the antenna. The transmission line loop provides about $3 \times 54° = 162°$ of phase shift between the drain and gate voltages, in addition to the transmission line losses between the gate and the antenna. This phase shift can lead to destructive interference between the radiated signals leading to a partial signal cancellation. Another concern is that the gates of the transistors provide a low impedance at the radiation frequency which can potentially load the drain and reduce the radiated power. To mitigate these issues, the positions of the drain and the gate with respect to the central slot are optimized such that the ratio between powers at the drain and the gate are maximized in the circuit-EM co-design. This means that the drain impedance is well matched to the resonator impedance at the third harmonic while the gate experiences a large mismatch and there is isolation between them without needing any additional elements.

The S-parameters of the EM structure are extracted and imported into Cadence Virtuoso as shown in 3-4a. The S-parameters block includes the interconnects between the transistors and the antenna. The large coupling capacitors in the simulations block the virtual short between the supply and the ground due to the applied perfect-E symmetry boundary in the EM simulations. Fig 3-4b shows the output power from the drain and gate terminals, the generated power per transistor from the drain and gate terminals is 454 and 70 uW, at a 20 mA input DC current. The phase difference between the generated voltages is $-60°$, which further mitigates the signal cancellation problem. The estimation of the actual radiated power should take into consideration the radiation efficiency from the transistor to the infinite silicon half space in the simulations, i.e., the conductor loss in the interconnects, antenna loss and the substrate propagation losses, and an additional factor of 0.7 of mismatch
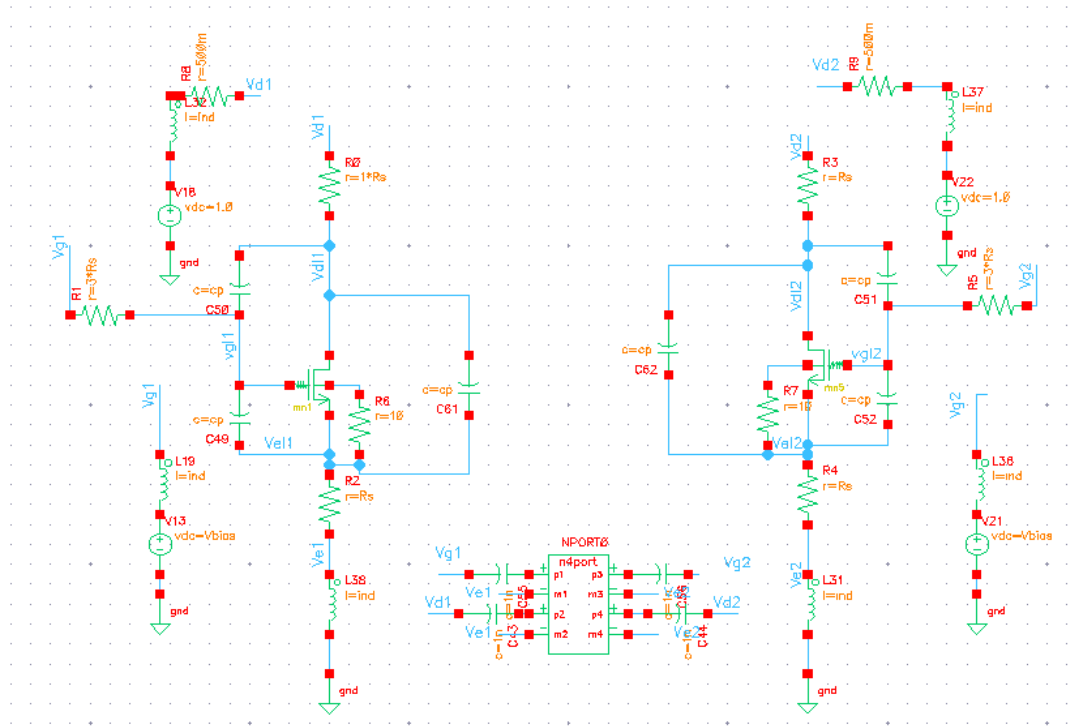
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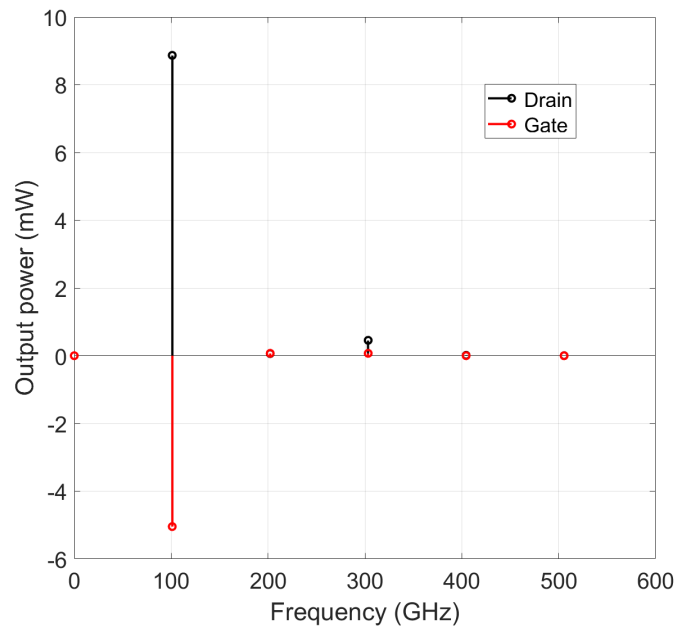
(b)

Figure 3-4: (a) Circuit simulation of unit radiator. (b) Output powers from the drain and the gate.
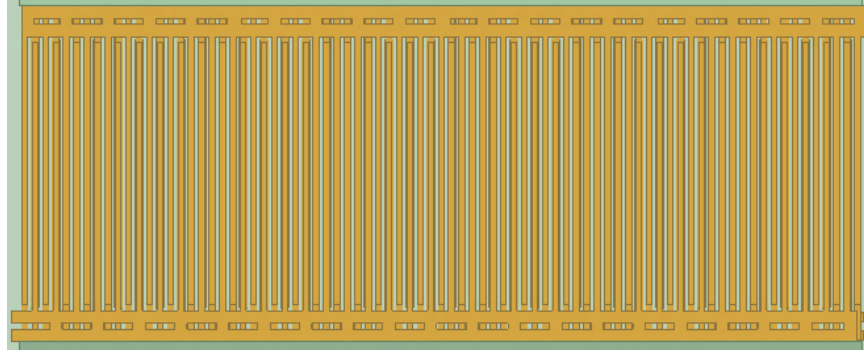
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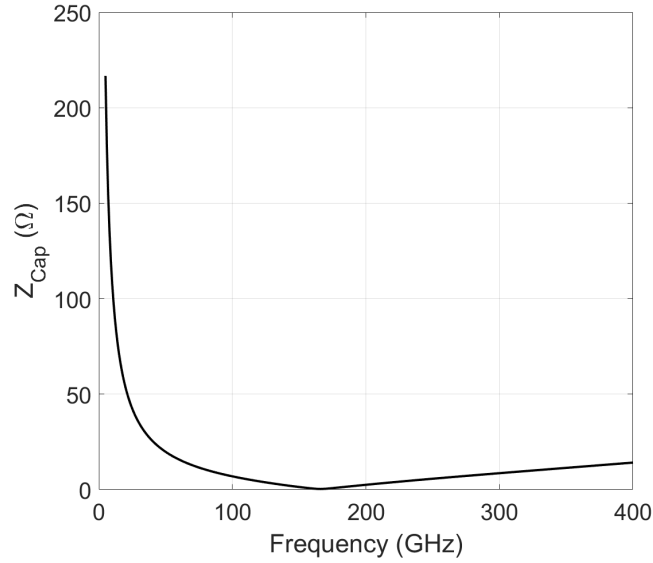
(b)

Figure 3-5: (a) Layout of the boundary metal-finger capacitor. (b) The simulated impedance of the capacitor.

between the silicon and air interface.

The edge unit cells are formed by removing the air-bridges on the perfect-H boundary, while the perfect-E boundary is mimicked by using a metal wall that goes from the bottom to the top metal layers. The boundary slot is terminated using the high-density custom metal finger capacitors shown in Fig. The low-frequency capacitance of the capacitors is 145 fF and 3-5a shows that these capacitors self-resonate at 150 GHz and provide low impedance at the fundamental and third harmonic frequencies. The gate biasing lines are decoupled at the edges using the same capacitors. All of this leads to the final structure shown in 3-6
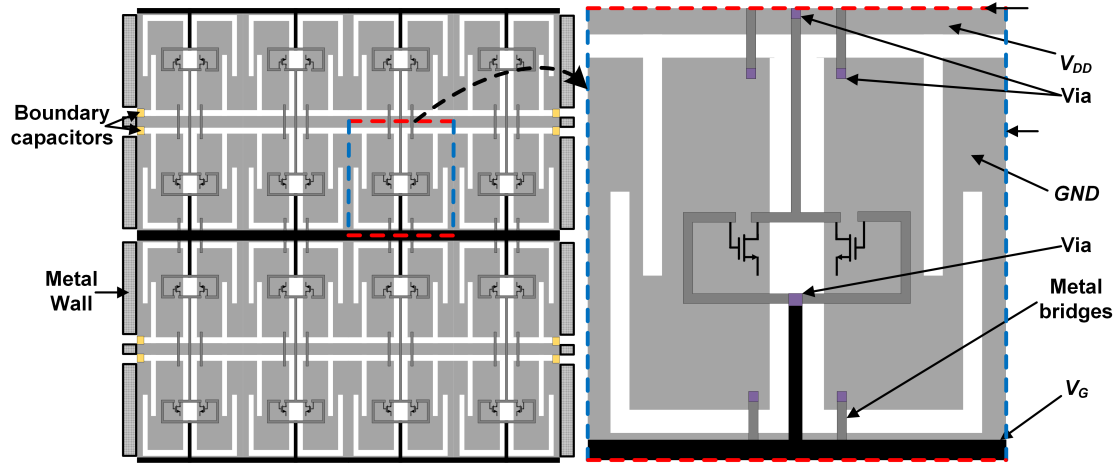
Figure 3-6: 4×4 2-D tiled radiator array

Chapter 4

Measurements
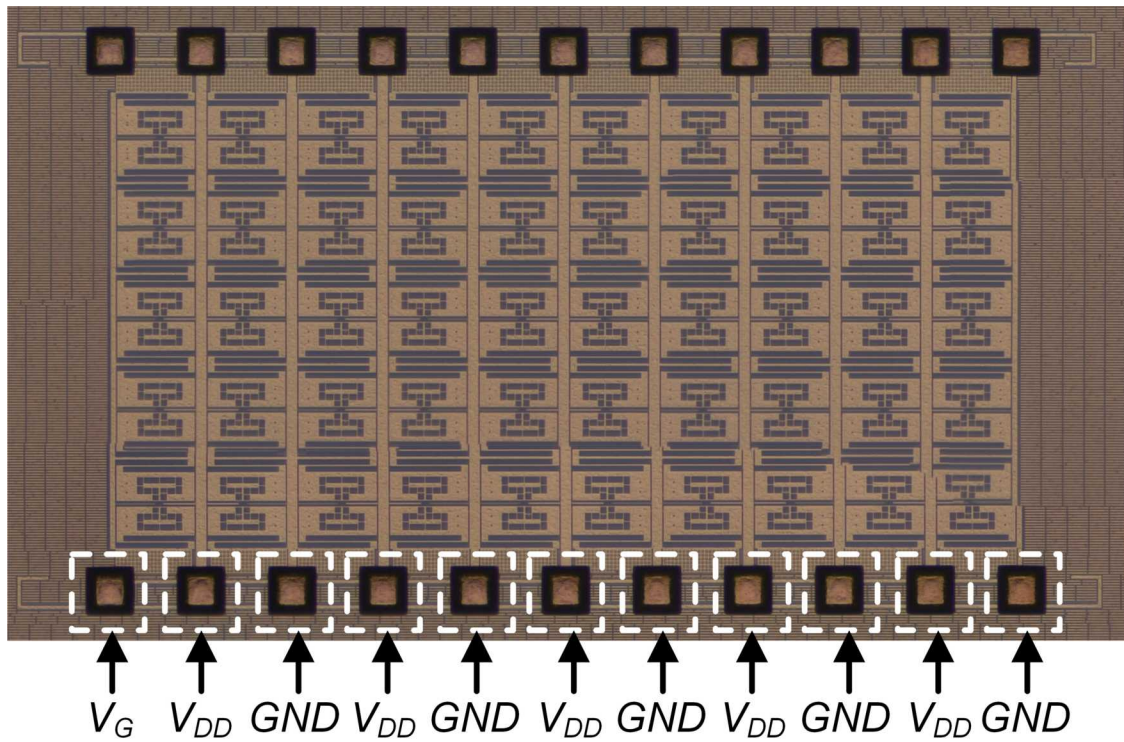
Figure 4-1: The die photo of the fabricated 10×5 element radiator with the biasing pads highlighted

We fabricated an array of 10×5 radiator elements, on Intel 22FFL technology. The fabricated chip in 4-1 is attached to a 525 μm-thick high-resistivity silicon-wafer which is then glued to the PCB. A hemispherical silicon lens is then mounted on the wafer using a movable fixture for alignment. The purpose of the lens is to release the
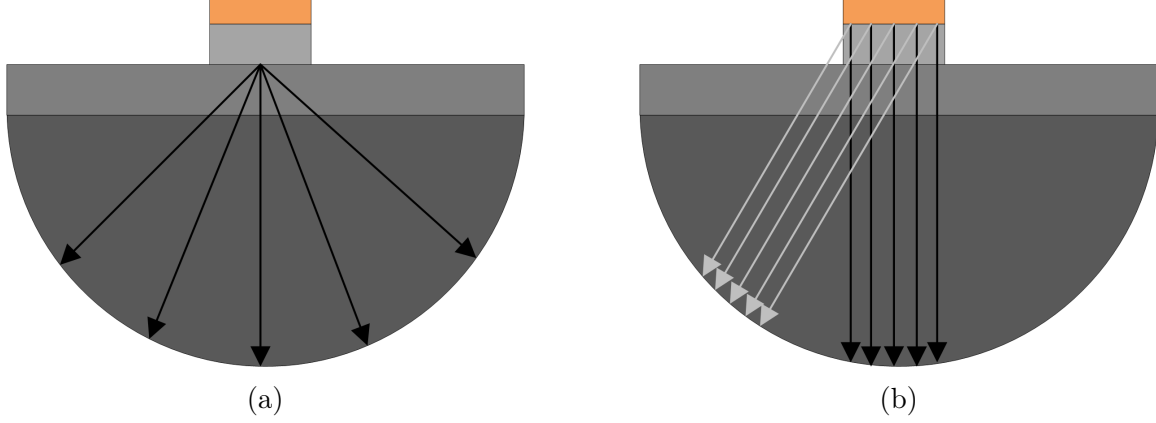
Figure 4-2: (a) Ideal point source assumption. (b) Non-idealities leads to the accural of additional phase shifts for off-center elements

generated power into air, with minimal coupling loss equal to the transmission loss factor due to the mismatch, and minimize the energy confinement in the substrate modes. Ideally, the incident rays are normal to the silicon-air interface and the the radiation pattern of the array is unaltered as shown in 4-2a. However, two things invalidate this assumption. The non-negligible substrate and spacer thicknesses at THz frequencies, which amount to an electrical length of several wavelengths in silicon. The other is the point-source assumption which is invalid in case of electrically large arrays. The radiation from the off-center elements observes different angles of incidence at the silicon-air interface and more importantly, they accrue additional phase shifts due to the different propagation lengths, as shown in 4-2b This has been studied in [21] where they confirmed that increasing the array size in such a situation can be detrimental to the directivity of the array and hence, they optimized the spacer and lens size for maximum directivity for a given array configuration.

4-3a shows the measurement setup; the readings are taken 10 cm away from the radiator which is well within the far-field region at 300 GHz ($\lambda = 1$ mm). First, The EIRP is measured using an Erickson PM5 power meter connected to a pyramidal WR-3.4 horn antenna accoring to:

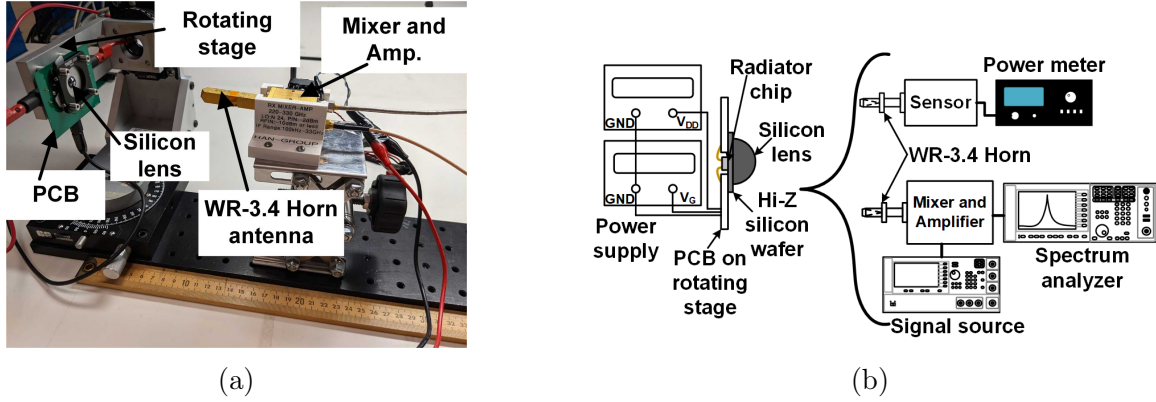$$P_r = EIRP \ G_r \ (\frac{\lambda}{4\pi r})^2 \qquad (4.1)$$

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Figure 4-3: (a) Measurement setup of the assmebled radiator board with the down-coversion mixer. (b) Schematics of the spectrum and power measurement setups.

Where G_r is the gain of the receiver, λ is the operating wavelength and r is the distance between the transmitter and the receiver. The power meter is then replaced by a VDI mixer fed by an external signal source, and the downconverted received signal is then used to determine the radiation frequency and spectrum.

Fig. 4-4a shows the measured radiation pattern in the E and H-planes of the radiator array. The directivity for large arrays can be computed by:

$$D \approx \frac{32400}{\theta_{1d}\theta_{2d}} \tag{4.2}$$

where θ_{1d} and θ_{2d} are the half-power beam widths in the E- and H- planes. Hence, the corresponding directivity is calculated to be 16.8 dB. The gate voltage is swept and the radiation frequency and EIRP are measured as shown in 4-4b and 4-4c. The output frequency changes by by 3 GHz, while The EIRP reaches a peak value of at 14.8 dBm at a gate voltage of 550 mV. Hence, the radiated power is determined by the difference between the EIRP and directivity to be -2 dBm. Fig. **??** shows the down-converted spectrum, taken at an RBW of 500 kHz. The phase noise at 1 MHz offset is -72 dBc/Hz while the phase noise at 10 MHz is -100 dBc/Hz.

Table 4.1 shows a comparison between the proposed radiator and the most relevant previous literature. It should be noted that the reported f_{max} for our design is for the smallest size transistor without interconnects. The actual value for the used transistor in the design including the interconnects drops down to 270 GHz, hence
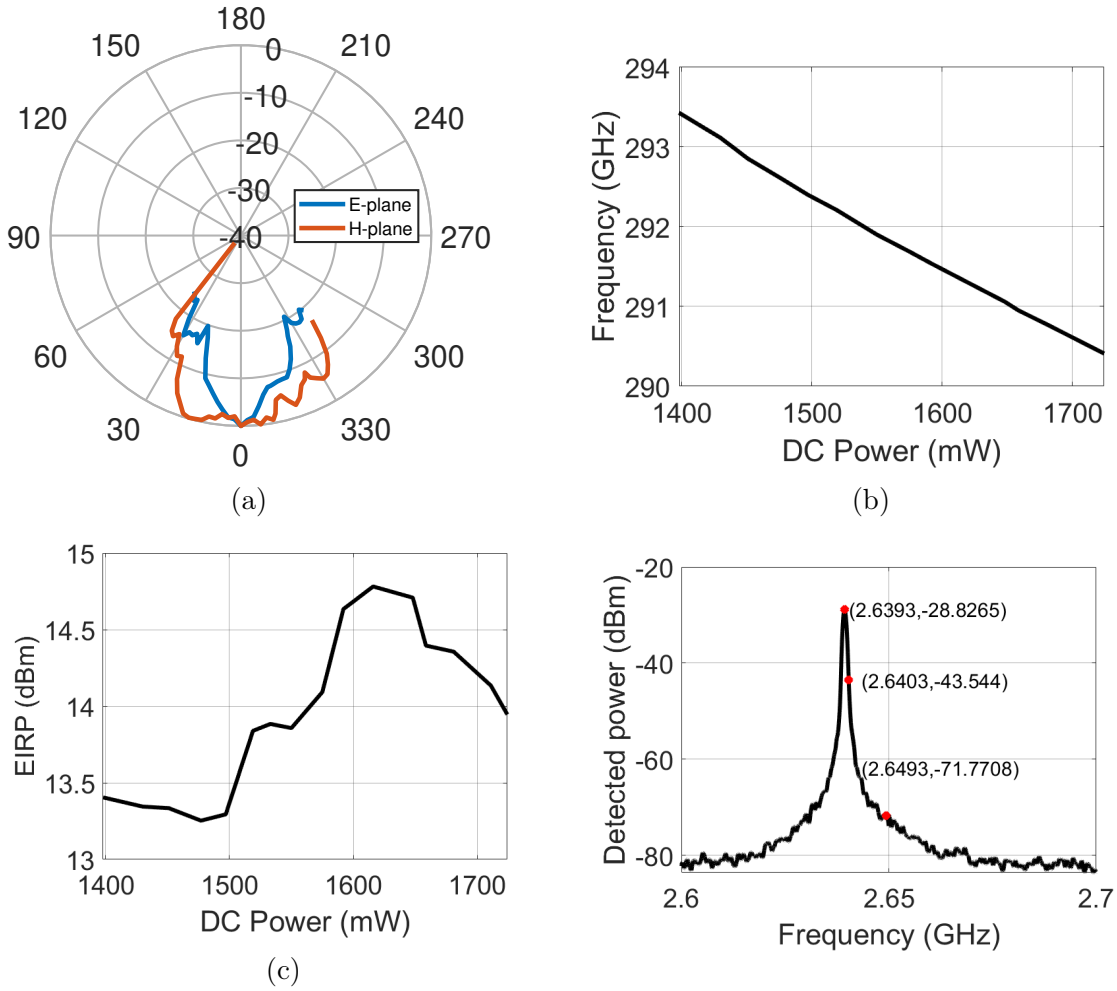
Figure 4-4: (a) Measurement setup (b) Radiation pattern (c) Output power and frequency (d) Spectrum and phase noise.

radiation takes place above f_{max}, justifying the need for harmonic radiation. The proposed radiator offers a good combination of radiated power, EIRP and efficiency within a compact footprint. The scalability of the structure offers a clear way to scale the radiated power and array directivity by increasing the number of unit radiators.

Table 4.1: Comparison with prior literature on THz radiators

	This Work	[17]	[19]	[21]	[22]	[23]	[24]	[25]	[26]
Frequency (GHz)	291.3	317	670	459	302 to 332	342	260	265	338
Power (dBm)	-2	5.2	-16.1	-1.8	-13.9 (Probed)	-10.5	0.5	—	-0.9
EIRP (dBm)	14.8	22.5	7.4	19.3	—	1.2	15.7	-6.6	17
Phase Noise (1/10MHz) (dBc)	-72 / -100	-79 / —	-69 / -93	— / -100.6	-79 / —	— / -98.2	-78.3 / —	-89.3 / —	-93 / —
DC Power (mW)	1620	610	99.7	1470	610	425	800	92	1540
DC-THz efficiency(%)	0.039	0.52	0.0246	0.045	0.0067	0.021	0.14	—	0.053
Area (mm^2)	1.6	0.85	0.86	3.94	0.85	1.33	2.3	1.56	3.9
Technology	Intel 22FFL (CMOS)	130nm SiGe	40nm CMOS	65nm CMOS	130nm SiGe	130nm SiGe	65nm CMOS	65nm CMOS	65nm CMOS
$f_{max}(GHz)$	450	280	300	350	280	215	250	—	250

Chapter 5

Conclusion

In this work, we have presented a Terahertz radiator at 291.3 GHz. The core oscillator is a differential pair coupled to a multi-functional EM structure. The EM structure consists of folded slots which suppress radiation at the 1st and even harmonics while radiating at the 3rd harmonic. The footprint of the unit radiator is $\lambda/2 \times \lambda/2$ at the radiation frequency, which suppresses the grating lobes and enables 2-D tiling for narrow-beam radiation. The slots at the boundaries of each element are coupled to the neighboring ones to maintain the phase relationship between the oscillators, and obtain coherent broadside free-space power combining. The proposed radiator consists of 10×5 units and is implemented in Intel 22nm FinFET (FFL) technology. The chip size is 1.6 mm^2 and radiates -2 dBm with 14.8 dBm EIRP at 1.62 W of DC power. This advancement in THz generation is a stepping stone for wider adoption of THz systems and technologies in daily life.

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