Carbon Nanotubes for Space Electronics: Enabling New Applications with Emerging Technologies

By

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B.A.Sc., The University of Waterloo (2017)

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Abstract

Physical scaling of silicon-based field-effect transistors (FETs) yields diminishing returns and continues to grow increasingly challenging. This has motivated the search for beyond-silicon technologies based on materials such as carbon nanotubes (CNTs) and transition metal dichalcogenides (TMDs). However, solely relying on new materials alone is insufficient to realize next-generation electronics. Therefore, we must coordinate advances across the entire computing stack whereby we leverage new materials and device architectures to enable new circuits and systems to ultimately realize new exciting applications. In this thesis, as a case study, we use CNT-based electronics, a promising technology projected to provide orders of magnitude energy-delay-product (EDP) improvement versus conventional silicon-based digital VLSI systems. I experimentally demonstrate new three-dimensional (3D) device and circuit architectures leveraging unique low temperature processing of CNTs, demonstrate the first CNT-based SRAM arrays, and realize new applications with CNT-based radiation tolerant electronics to drive future space missions.

Thesis Supervisor: Max M. Shulaker

Title: Associate Professor of Electrical Engineering and Computer Science

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Table of Contents

Table of Figures

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Kanhaiya, P.S., Hills, G., Antoniadis, D.A. and Shulaker, M.M., 2018. DISC-FETs: Dual independent stacked channel field-effect transistors. IEEE Electron Device Letters, 39(8), pp.1250-1253.

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Chapter 1: Introduction

1.1 Background

Physical scaling and equivalent scaling of silicon-based field-effect transistors (FETs) have been a major driving force to improve computing energy efficiency (quantified by the energy-delay product, EDP, the product of energy consumption and circuit delay) for decades [1], [2]. However, continued silicon scaling is becoming increasingly challenging while simultaneously yielding diminishing returns [3] – [6], thus motivating the search for beyond-silicon nanotechnologies such as one-dimensional carbon nanotubes (CNTs) or two-dimensional nanomaterials such as transition metal dichalcogenides (TMDs) [7] – [9]. Yet solely relying on new materials is insufficient for realizing the next generation of energy-efficient computing. Rather, coordinated advances across the entire computing system stack are required as their combined benefits are greater than the sum of their individual benefits. I combine multiple advances across the stack - leveraging new nanomaterials and new device geometries to realize new circuit and system demonstrations to ultimately develop electronics for new applications. In this thesis, we demonstrate that to build next-generation systems for new applications we (1) must elucidate benefits of these new technologies to inform target application selection, and (2) must simultaneously have a deep understanding of the challenges and requirements of the target application before choosing a technology.

As a case study, this thesis focuses on CNT-based electronics and the target application of radiation-tolerant electronics for future space missions. With humankind's desire to explore space continuously growing, ranging from ambitions of constructing permanent moon bases [10] to asteroid mining [11] to travelling to Mars [12], the electronics driving such missions must become increasingly energy-efficient (for increased local compute enabling greater autonomy) and simultaneously radiation-tolerant (for increased lifetime and reliability). To meet these needs, a wide range of emerging nanomaterials and nanodevices are currently being explored. For instance, CNTs, single sheets of carbon atoms rolled to form nanoscale cylinders with diameters of ~1 nm, are a leading contender for next-generation energy-efficient digital very-large-scale-

integrated (VLSI) circuits. Carbon nanotube field-effect transistors, CNFETs, are formed by multiple CNTs defining the channel whose conductance is modulated by a metal gate (Fig. 1). Moreover, owing to their ideal electrostatic control (due to the ultra-thin ~1 nm body) and high carrier transport, CNFETs are projected to provide an order of magnitude improvement in EDP versus today's silicon-based complementary metal-oxide-semiconductor (CMOS) technology [13]. Importantly, CNFETs can be fabricated at low processing temperatures (<400°) [14], [15], and therefore naturally enable new system architectures such as monolithic three-dimensional (3D) integration (whereby layers of circuits are fabricated sequentially and directly vertically overlapping one-another over the same starting substrate [15]). Such monolithic 3D integration enables new paradigms in designing heterogeneous nanosystems [15], allowing fine-grained integration of sensing, logic and memory circuit layers at the nanoscale.

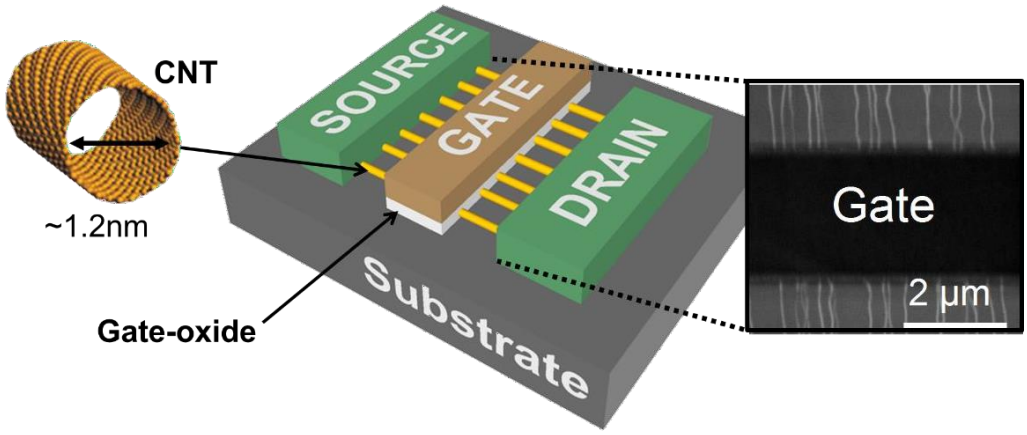

Figure 1.1. Schematic of CNFET with multiple parallel CNTs (nanocylinders made with atomically thin sheet of carbon atoms with diameter ~ 1 nm) bridging the source to drain contact.

CNFETs are a rapidly maturing technology, with experimental demonstrations ranging from digital logic gates [16] – [20], to complex analog and mixed-signal circuits [21], [22], to complete large-scale digital systems [14], [23] – [32]. However, although recent advances in CNFET technology have been significant, a critical component of digital systems – SRAM memory arrays – had never been demonstrated, and only limited studies on CNFET radiation tolerance have been performed [33] – [38]. Prior work has either realized only individual, isolated CNT-based SRAM cells [39], or has relied on processing that is not

compatible with silicon CMOS (e.g., relying on air-reactive, ionic, non-solid-state CNT doping processes). Furthermore, previous radiation-tolerant works do not study realistic (e.g., solid-state and VLSI-compatible) CNFET devices for next-generation electronic systems, and thus do not fully represent the potential benefits of a future CNFET radiation-tolerant technology [40] – [46].

This work shows the following:

1) New 3D FET architectures leveraging the low temperature processing requirements of CNFETs (e.g., <250 ºC): (1) Dual Independent Stacked Channel FET (DISC-FET). DISC-FET is comprised of two FET channels vertically integrated on separate circuit layers separated by a shared gate. This gate modulates the conductance of both FET channels simultaneously, although the stacked channels are independent, i.e., n-type or p-type with separate source and drain terminals separately accessed via routing. (2) X3D, which enables a wide range of semiconductors – including silicon (Si), III-V, and nanotechnologies such as carbon nanotubes (CNTs) – to be heterogeneously integrated together in monolithic 3D integrated systems. Such flexible heterogeneous integration has potential for a wide range of applications, as each layer of monolithic X3D integrated circuits (ICs) can be customized for specific functionality (e.g., wide-bandgap III-V-based circuits for power management, CNT field-effect transistors (CNFETs) for energy-efficient computing, and tailored materials for custom sensors or imagers).

2) The first static random-access memory (SRAM) arrays based on CNFETs. We demonstrate 1 kbit (1024) 6 transistor (6T) SRAM arrays fabricated with complementary metal-oxide-semiconductor (CMOS) CNFETs (totaling 6,144 p- and n-type CNFETs), with all 1,024 cells functioning correctly without any per-unit customization. Moreover, we show the first demonstration of CNFET CMOS 10T SRAM cells, capable of operating at highly-scaled voltages down to 300 mV. We characterize the CNFET CMOS SRAM and demonstrate robust operation by writing and reading multiple patterns (to both the kbit arrays as well as the 10T SRAM cells), measuring SRAM variations in read, write and

hold margins and repeat cycling of cells. Moreover, due to the low-temperature back-end-of-line (BEOL) compatible CNT-specific processing, CNFET SRAM enable new opportunities for digital systems, since: (1) CNFET SRAM can be fabricated directly on top of computing logic to realize three-dimensional integrated circuits, and (2) CNFET circuits can utilize metal routing both above and below the CNFET device layer (e.g., as in our demonstration which utilizes buried power rails, whereby the power rails are fabricated underneath the FETs while metal routing is fabricated above the FETs), providing opportunities for further SRAM density scaling.

3) How CNFETs can be strategically engineered to realize a robust radiation-tolerant technology. We demonstrate radiation-tolerant CNFETs by leveraging both *extrinsic* CNFET benefits owing to CNFET device geometries enabled by their low-temperature fabrication, as well as *intrinsic* CNFET benefits owing to CNTs' inherent material properties. By performing a comprehensive study and optimization of CNFET device geometries, we demonstrate record CNFET total ionizing dose (TID) tolerance (above 10 Mrad(Si)), and show transient upset testing on CMOS CNFET-based 6T SRAM memories via x-ray prompt dose testing (threshold dose rate = 1.3×10^{10} rad(Si)/s).

1.2 Outline

Chapter 2 presents new 3D FET architectures leveraging the low temperature processing requirements of CNFETs. In particular, we present Dual Independent Sacked Channel Field-Effect Transistors (DISC-FETs), a 3D FET architecture with a shared gate that controls two overlapping FET channels physically above and below the gate metal. Moreover, we present and experimentally demonstrate X3D, which enables a range of semiconductors (e.g. silicon, III-V, and nanotechnologies such as CNTs) to be heterogeneously integrated in monolithic 3D systems.

Chapter 3 details the first CNFET-based SRAM arrays every built. We experimentally demonstrate 1 kbit (1024) 6T SRAM arrays fabricated with CMOS CNFETs (totaling 6,144 p- and n-type CNFETs), with all 1,024 cells functioning correctly without any per-unit customization. Moreover, we show the first demonstration of CNFET CMOS 10T SRAM cells, capable of operating at highly-scaled voltages down to 300 mV.

Chapter 4 highlights how CNFETs can be strategically engineered to realize a robust radiation-tolerant technology. We demonstrate radiation-tolerant CNFETs by leveraging both *extrinsic* CNFET benefits owing to CNFET device geometries enabled by their low-temperature fabrication, as well as *intrinsic* CNFET benefits owing to CNTs' inherent material properties. We report a record high CNFET TID tolerance (10 Mrad(Si)), and detail the first transient upset of CMOS CNFET 6T SRAM memories via x-ray prompt dose testing (threshold dose rate = 1.3×10^{10} rad(Si)/s).

Chapter 5 shares ongoing work and preliminary experimental results of electrostatically doped NMOS CNFETs at cryogenic temperatures. Here, we highlight potential benefits of electrostatically doped FETs owing to the absence of dopant impurities and, therefore, absence of dopant freeze-out. To demonstrate the stability and resilience of CNFETs at cryogenic temperatures we measure device characteristics from 300 K down to 7 K.

Chapter 6 concludes this thesis by summarizing key results and discussing the broader impact of this work.

Chapter 2: CNTs Enabling New Device and Circuit Architectures

2.1 DISC-FETs: Dual Independent Stacked Channel Field-Effect Transistors

2.1.1 Introduction

As physical and equivalent scaling of silicon complementary metal-oxide-semiconductor (CMOS) grows increasingly challenging [3] – [6], alternative paths to improve energy efficiency of digital systems, e.g., by leveraging new materials, FETs, circuits, and architectures, are actively being pursued [47] – [51]. We present and experimentally demonstrate a 3D FET architecture: Dual Independent Stacked Channel Field-Effect Transistor (DISC-FET). As illustrated in Fig. 2.1, DISC-FET is a 3D FET architecture with a shared gate that controls two vertically overlapping FET channels physically located above and below the gate. DISC-FET has five terminals: source and drain for the lower-layer FET, source and drain for the upper-layer FET, and the shared gate. Due to the reduced footprint of two vertically overlapping channels, the 3D geometry of DISC-FETs enables new opportunities for area-efficient 3D circuit layouts [52], [53][1].

[1] For example, DISC-FET offers potential area benefits for technology node scaling by reducing the height of standard library cells with vertically overlapping NMOS and PMOS FETs as relative standard cell area is typically quantified by the product of the contact gate pitch (CGP), metal 1 pitch (MP), and number of metal routing tracks (T) [55]. Despite reduced standard cell area = CGP*MP*T, however, overall area benefits may be limited by back-end-of-line interconnect routing, which should be the focus of future analysis. Additionally, since DISC-FET circuits involve new layouts, parasitics should be extracted for these circuits depending on their precise 3D circuit structure. Importantly, these parasitics will also include coupling capacitance between the upper and lower FET layers, which will be an important aspect of analyzing DISC-FET circuit performance for future analysis.

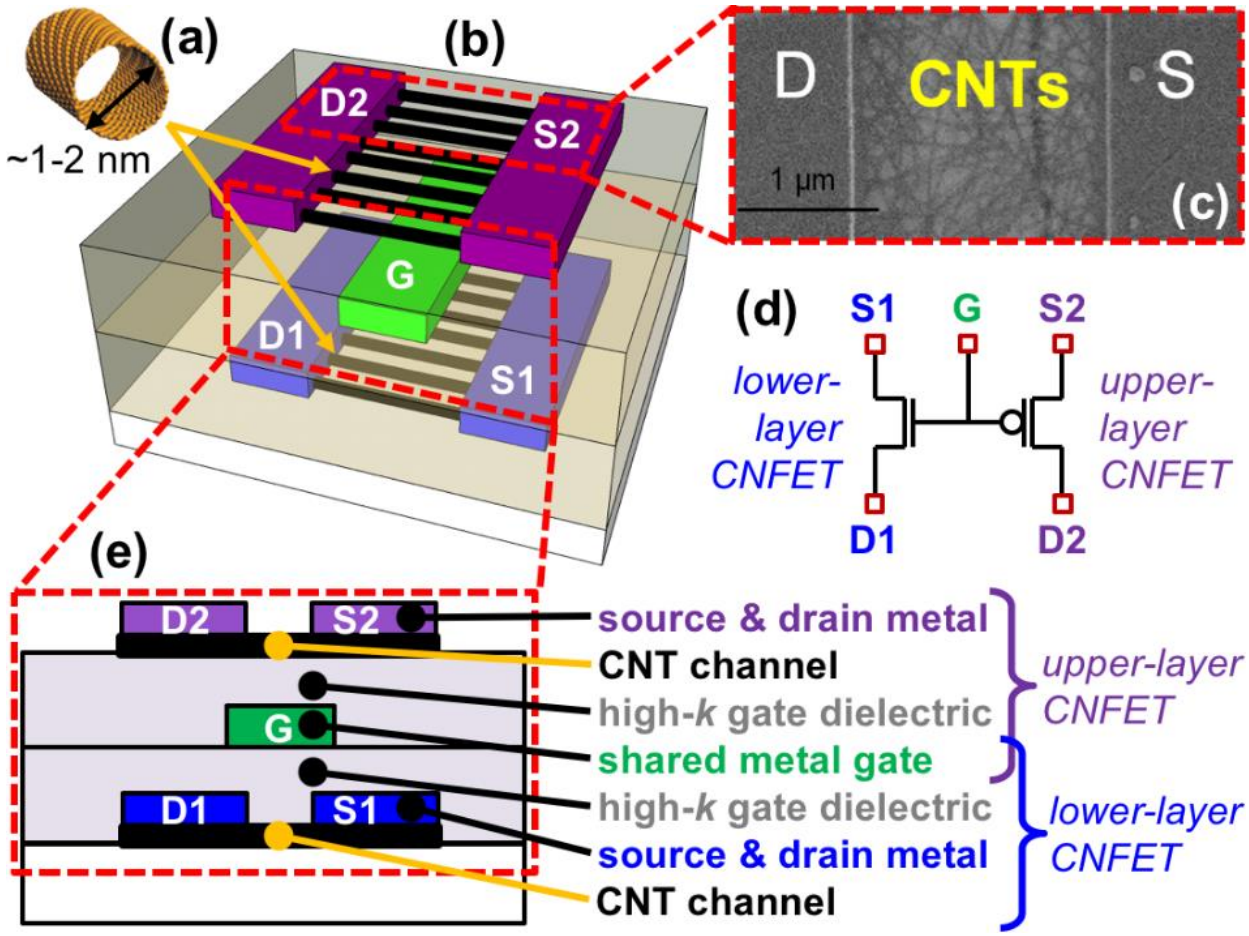

Figure 2.1. CNFET-based DISC-FET. (a) Carbon nanotube (CNT). (b) DISC-FET 3D illustration, including source and drain for the lower-layer CNFET ("S1" and "D1"), source and drain for the upper-layer CNFET ("S2" and "D2"), and shared gate ("G"). (c) Scanning electron microscope (SEM) image of the upper-layer CNFET. (d) 5-terminal circuit schematic of DISC-FET, including 1 PMOS FET and 1 NMOS FET, although each CNFET can be either NMOS or PMOS. (e) Cross-section showing vertically integrated layers.

However, physically realizing DISC-FETs poses inherent challenges for conventional silicon-based FETs: the fabrication of the upper FET channel must be low temperature (e.g., <400 °C) to avoid damaging the FETs and metal interconnects on the lower circuit layers [15], [53]. To overcome this challenge, we leverage CNTs as the channel material for both the upper- and lower-layer FETs, since CNFETs can be fabricated at low processing temperatures (e.g., <250 °C, process flow in Sec. II [14]), and so multiple layers of CNFETs can be built directly on top of each other over the same starting substrate, with conventional back-end-of-line (BEOL) inter-layer vias (ILVs) to connect the vertical circuit layers [15]. Moreover, CNFETs promise an order of magnitude improvement in energy delay product (EDP, a metric

of energy efficiency) vs. silicon FETs for digital VLSI circuits [8], [56]. Thus, this approach offers EDP benefits simultaneously with area-efficient 3D circuit layouts.

2.1.2 DISC-FET Process Flow

The process flow for a CNFET-based CMOS DISC-FET, i.e., with an upper-layer PMOS CNFET, and lower-layer NMOS CNFET, is shown in Fig. 2.2. A solution of purified CNTs, sorted to achieve >99.9% semiconducting CNT (s-CNT) purity [57], [58], is deposited over a starting SiO_2 substrate by submerging the substrate in the CNT solution at low temperature (25 ºC). Importantly, this solution-based process is key for decoupling the high temperature CNT synthesis (>1,000 ºC) from the final substrate used for DISC-FET fabrication [15][2]. Source and drain metal contacts for the bottom channel are defined by lithographic patterning and depositing Ti/Pt (1 nm/ 40 nm) using physical vapor deposition (PVD). CNTs outside the channel region of the lower-layer CNFET are then etched using oxygen plasma [56]. To fabricate the gate stack for DISC-FET – which comprises the high-*k* gate oxide for the lower-layer CNFET, the shared metal gate, and the high-*k* gate oxide for the upper-layer CNFET (as shown in Fig. 2.1e) – a 20 nm HfO_X film is first deposited through atomic layer deposition (ALD, at 200 ºC) directly over the CNTs, followed by lithographic patterning and PVD of Ti/Pt (1 nm/ 20 nm) to form the metal gate. This HfO_X electrostatically dopes the lower-layer CNFET channel, forming an NMOS CNFET [61]. The lithographic patterning and metal deposition for the metal gate is also used to form fine-grained ILVs to connect the lower-layer CNFET source and drain terminals to the upper-layer CNFETs [15]. 20 nm of HfO_X is then deposited directly on top of the existing metal gate, using ALD, forming the gate oxide for the upper-layer CNFET. This is followed by a second CNT deposition, using the same low temperature solution-based processing described above. The source and drain for the upper-layer PMOS CNFET are then formed using the same process as the lower-layer CNFET source and drain (1 nm Ti/ 40 nm Pt). CNTs outside of the upper-layer channel

[2] Aligned chemical vapor deposition (CVD)-grown CNTs can also be deposited over the substrate using previously developed low-temperature transfer processes [56], [62].

region are etched using oxygen plasma, and subsequent BEOL routing can continue.

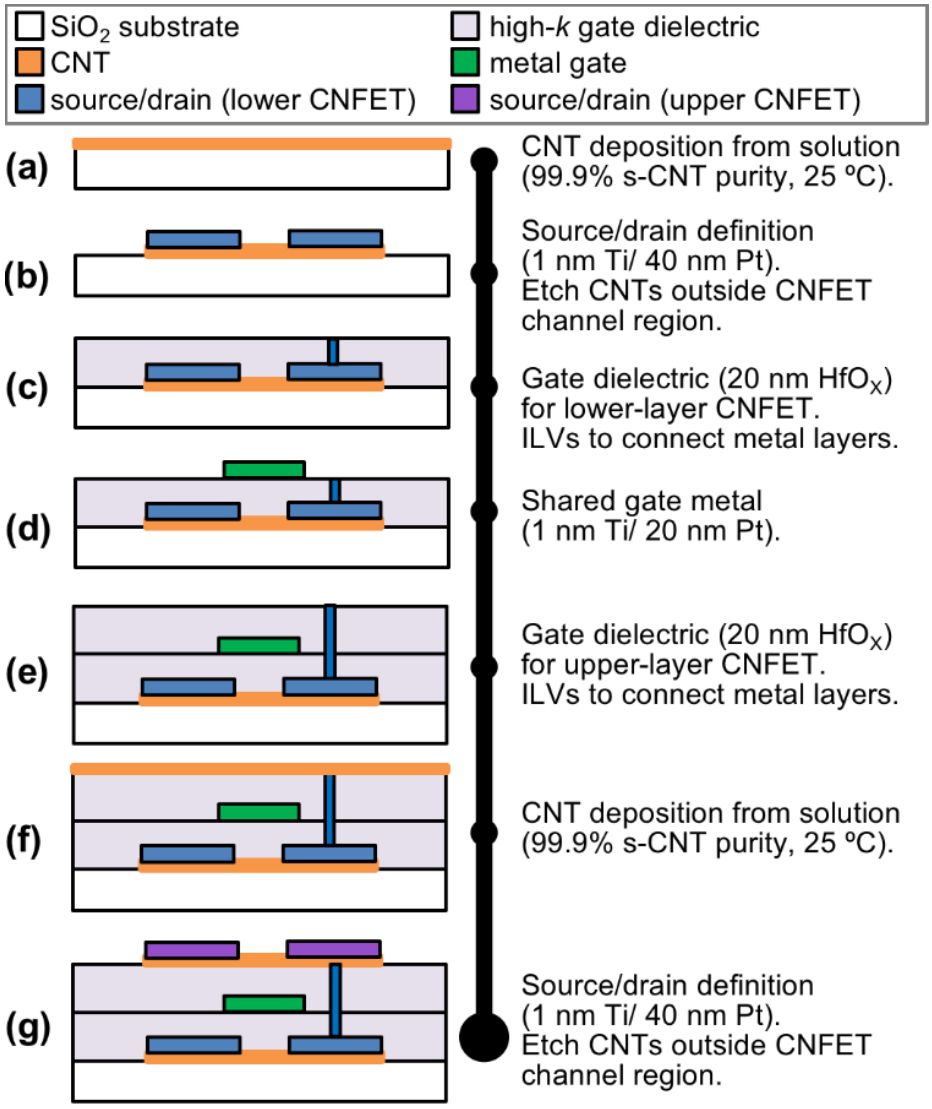

Figure 2.2. Process flow used to realize CNFET-based CMOS DISC-FETs.

2.1.3 Experimental Results

To experimentally demonstrate 3D circuit layouts enabled by DISC-FETs, we fabricate CNFET-based static CMOS DISC-FET inverters (INV) and 2-input “not-or” (NOR2) digital logic gates. Schematics and scanning electron microscopy (SEM) images of fabricated circuits are in Fig. 2.3. As a demonstration, lower-layer CNFETs are NMOS, and upper-layer CNFETs are PMOS, although CNFETs on each layer can be independently designed to be either NMOS or PMOS. As shown in Fig. 2.3, upper- and lower-layer

CNFETs are vertically overlapping and are controlled by a shared gate.

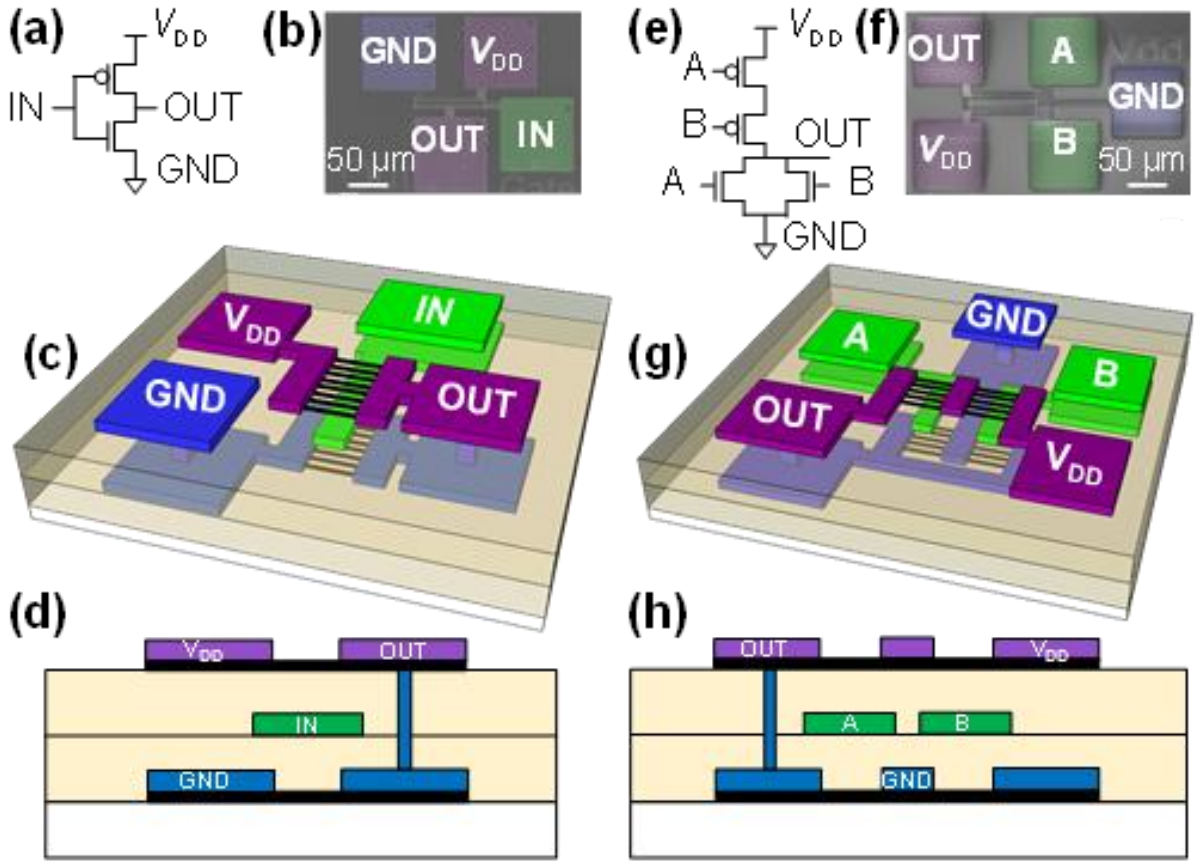

Figure 2.3. Fabricated CNFET-based static CMOS DISC-FET digital logic gates. (a) Inverter schematic, (b) SEM, (c) 3D illustration, and (d) cross-section. (e) 2-input NOR schematic, (f) SEM, (g) 3D illustration, and (h) cross-section.

CNFET-level characterization results are shown in Fig. 2.4: drain current vs gate-to-source voltage (I_D vs. V_{GS}) and drain current vs. drain-to-source-voltage (I_D vs. V_{DS}) for both the upper-layer PMOS CNFET and lower-layer NMOS CNFET in a typical 5-terminal DISC-FET. The shared metal gate modulates the conductance for both CNFETs simultaneously.

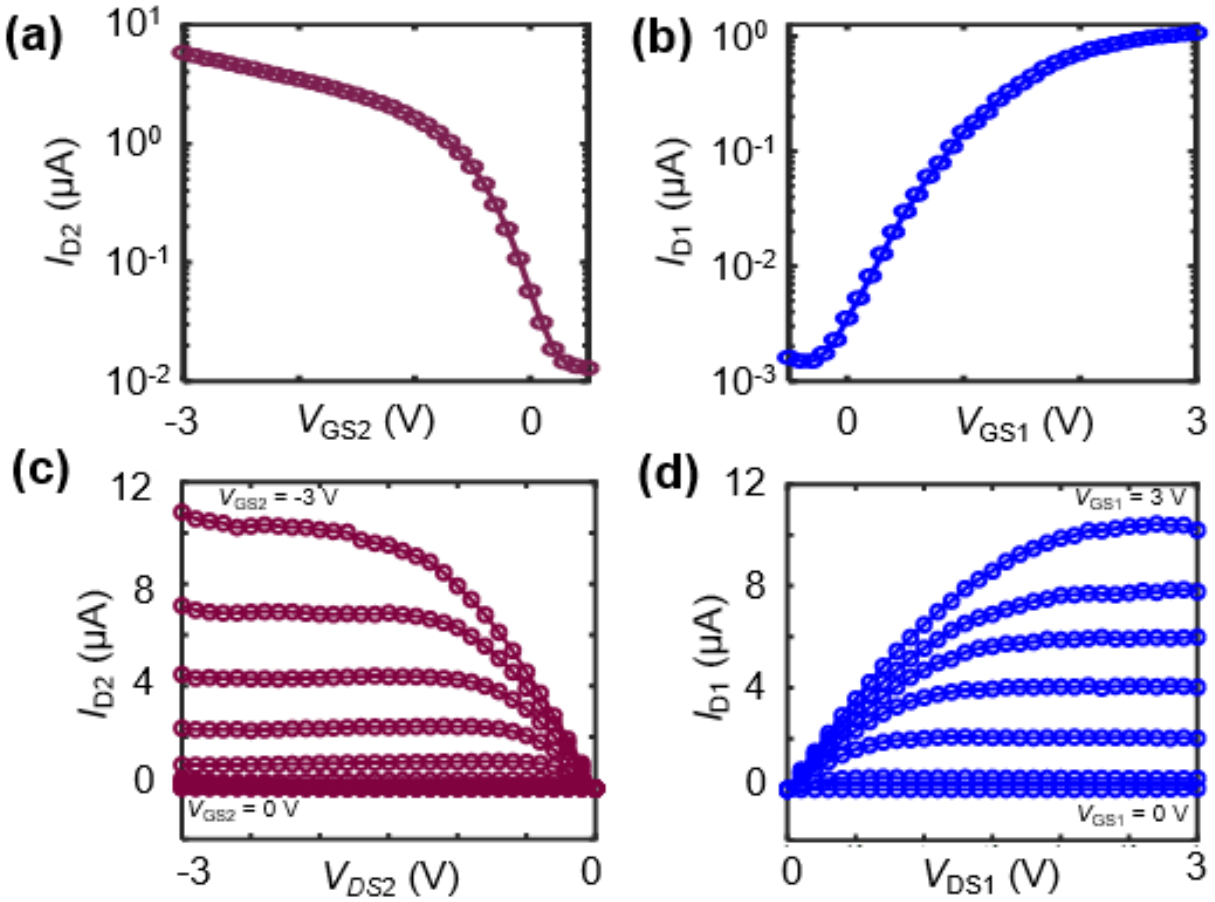

Figure 2.4. I_D vs. V_{GS} characteristics of a typical DISC-FET (schematic in Fig. 2.1). The CNT density is ~10 CNTs/μm. (a,c) Upper-layer PMOS CNFET, with source and drain terminals S2 and D2. V_{GS2} is the gate-to-S2 voltage, V_{DS2} (-3 V in (a)) is the D2-to-S2 voltage, and I_{D2} is measured at D2. (b,d) Lower-layer NMOS CNFET, with source and drain terminals S1 and D1. V_{GS1} is the gate-to-S1 voltage, V_{DS1} (3 V in (b)) is the D1-to-S1, and I_{D1} is the current measured at D1. The channel length and width are ~2 μm and 36 μm respectively for all devices. The dimensions of the DISC-FET are set by the limitations of an academic fabrication facility; prior work has demonstrated the scalability of CNFETs to sub-10 nm channel lengths [60]. Measurements are performed at 25 ºC in ambient. Importantly, the DISC-FET characteristics (such as drive current) can be improved by leveraging techniques that have been previously developed for optimizing CNFET device performance [56], [64]. Future work should continue to explore new methods for further improving CNFET performance and minimizing variations. For instance, improving the interface between the CNTs and high-*k* gate dielectrics would minimize interface traps that have been implicated as a dominant source of CNFET hysteresis and threshold voltage variation [65].

To characterize each digital logic gate (INV and NOR2), we experimentally measure the output voltage, V_{OUT}, as a function of the input voltage for each input of that logic gate: INV has a single input (voltage: V_{IN}), while NOR2 has two inputs, A and B (voltages: $V_{IN,A}$ and $V_{IN,B}$). For INV, we refer to the relationship between V_{OUT} and V_{IN} as the *voltage transfer curve* (VTC), and we measure it two separate cases: 1) forward

sweep: sweeping V_{IN} from 0 V to the supply voltage (V_{DD}), and 2) reverse sweep: sweeping V_{IN} from V_{DD} to 0 V. Ideally, the two cases would result in the exact same V_{OUT} vs. V_{IN} relationship; however, due to hysteresis, this is not necessarily the case (details below). Fig. 2.5a shows example INV forward and reverse sweep VTCs. For each NOR2 input (A and B), we measure the forward and reverse sweep VTCs while applying 0 V (digital logic "0") to the other input, so that the logic level of V_{OUT} is a function of the logic level of the input voltage. Fig. 2.5c shows example NOR2 forward and reverse sweep VTCs for input A (with $V_{IN,B}$ = 0 V). Fig. 2.5c also shows that for $V_{IN,B} = V_{DD}$, V_{OUT} correctly corresponds to logical "0" for 0 V ≤ $V_{IN,A} \leq V_{DD}$. For each VTC, we quantify the following performance metrics (illustrated in Fig. 2.5):

1) *Output voltage "swing" (V_{SWING})* – the difference between the maximum V_{OUT} and minimum V_{OUT} over all input voltages within the range 0 to V_{DD} (Fig. 2.5a).

2) *Gain* – the maximum value of $-\Delta V_{OUT}/\Delta V_{IN}$ (Fig. 2.5b).

3) *Hysteresis ($V_{HYSTERESIS}$)* – the difference in V_{IN} to achieve $V_{OUT} = V_{DD}/2$ for the forward and reverse VTCs (Fig. 2.5a).

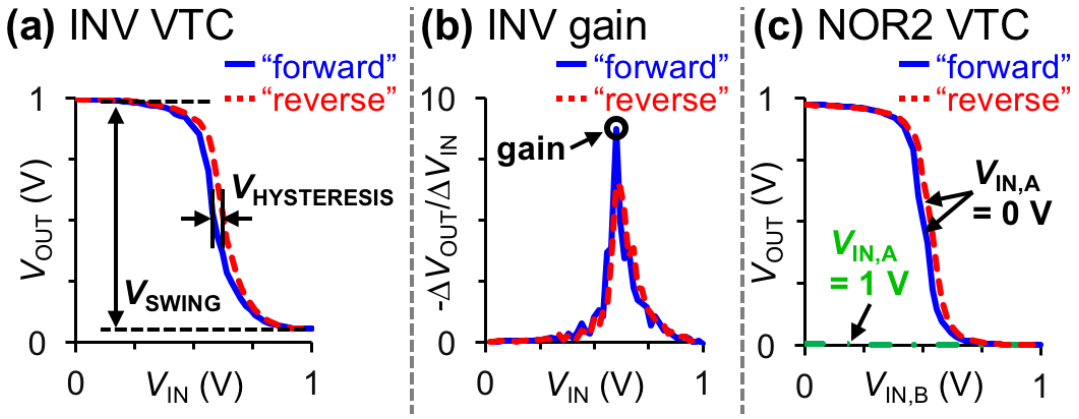

Figure 2.5. VTCs (forward and reverse sweeps) of CNFET-based DISC-FET logic gates, illustrating performance metrics for characterization (V_{DD} = 1 V). (a) INV: V_{SWING} = 94% V_{DD}, $V_{HYSTERISIS}$ = 4% V_{DD}. (b) INV $-\Delta V_{OUT}/\Delta V_{IN}$ (for fixed increments: ΔV_{IN} = 20 mV): gain – 8.7. (c) NOR2 VTCs for input A.

To experimentally demonstrate wafer-scale design and fabrication of CNFET-based DISC-FETs, we quantify V_{SWING}, gain, and $V_{HYSTERESIS}$ across 500 CNFET-based static CMOS DISC-FET NOR2 gates, measured with V_{DD} = 1 V. The VTCs corresponding to inputs A and B are shown in Fig. 2.6a and Fig. 2.6b,

respectively, with corresponding statistical distributions in Fig. 2.7 (reported V_{SWING} and gain correspond to the forward sweep VTCs). Averaged over 500 NOR2 gates, and including both inputs A and B, our experimentally measure results are as follows. Average V_{SWING}: μ_{SWING} = 94% V_{DD}, average gain: μ_{GAIN} = 6.3, and average $V_{HYSTERESIS}$, $\mu_{HYSTERESIS}$ = 2.3% V_{DD}.

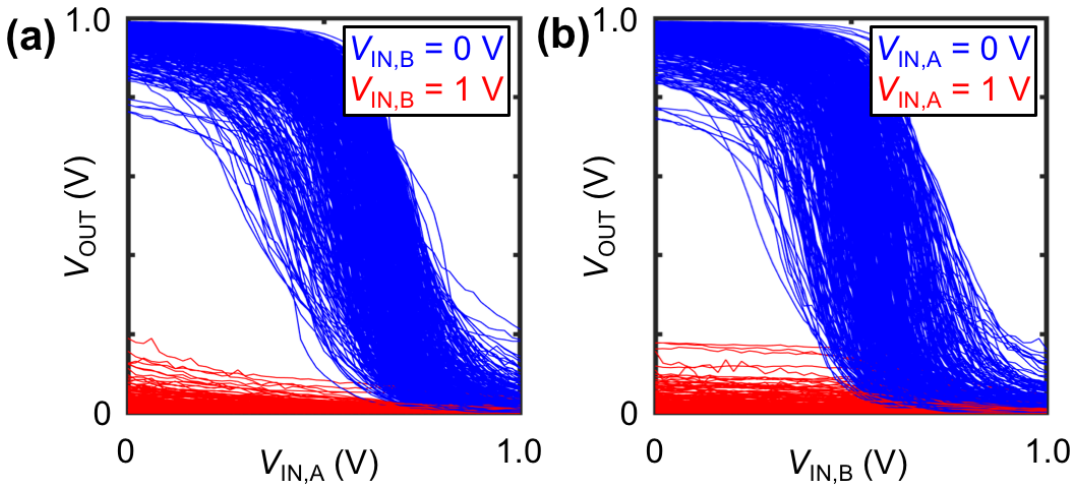

Figure 2.6. Forward sweep VTCs of 500 CNFET-based DISC-FET NOR2 gates (NOR2 design shown in Fig. 2.3e-f). (a) V_{OUT} vs. $V_{IN,A}$. (b) V_{OUT} vs. $V_{IN,B}$.

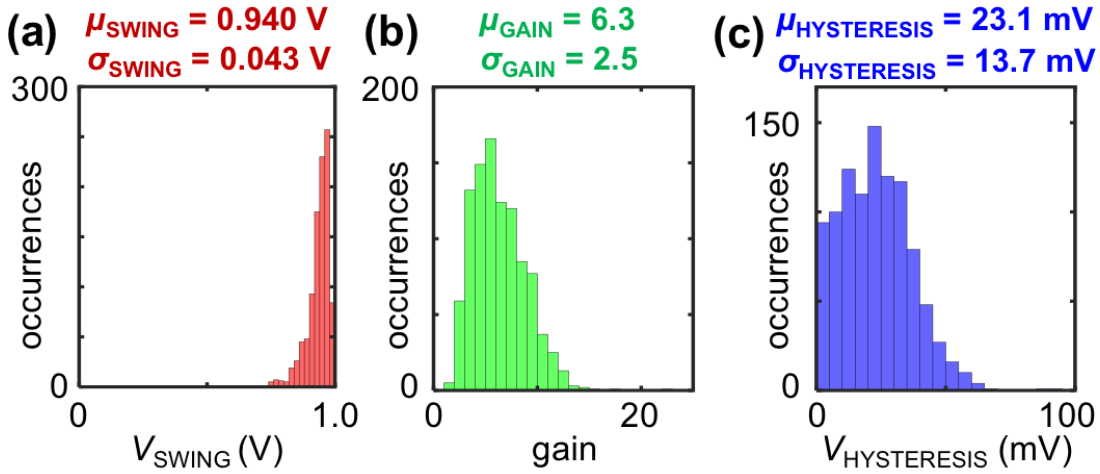

Figure 2.7. Statistical distributions of V_{SWING}, gain, and $V_{HYSTERESIS}$, measured from 500 CNFET-based static CMOS DISC-FET NOR2 digital logic gates, extracted from the VTCs in Fig. 2.6. (a) V_{SWING} mean (μ_{SWING}) and standard deviation (σ_{SWING}). (b) gain mean (μ_{GAIN}) and standard deviation (σ_{GAIN}). (c) $V_{HYSTEREIS}$ mean ($\mu_{HYSTERESIS}$) and standard deviation ($\sigma_{HYSTERESIS}$). Variability is primarily attributed to interface traps at the CNT/ high-*k* dielectric interface, as well as the fact that the upper-layer PMOS CNFETs are not passivated and exposed to ambient.

2.1.4 Conclusion

We experimentally demonstrate DISC-FET, a 3D FET architecture, using CNFETs. Importantly, DISC-FETs are naturally enabled by CNFETs due to low temperature requirements to fabricate multiple layers of CNFETs directly on top of one another over the same starting substrate. CNFET-based DISC-FETs can be used leveraged to realize new 3D circuit layouts, e.g. for digital logic circuits, and are thus a promising path for creating future generations of energy- and area-efficient very-large-scale integrated circuits.

2.2 X3D: Heterogeneous Monolithic 3D Integration of "X" (Arbitrary) Nanowires: Silicon, III-V, and Carbon Nanotubes

2.2.1 Introduction

As continued physical and equivalent scaling (e.g., Dennard scaling [2]) of silicon-based field-effect transistors (FETs) yields diminishing returns [64], multiple alternative paths for improving the energy efficiency of digital very-large-scale-integrated (VLSI) circuits and systems are being pursued. On one hand, improved FETs fabricated with beyond-silicon technologies ranging from III-V compound semiconductors to emerging nanotechnologies such as carbon nanotubes (CNTs) promise improved scalability and energy efficiency. For instance, digital systems fabricated from CNT FETs (CNFETs) versus silicon FETs promise a 10× improvement in energy-delay product (EDP: a metric of energy efficiency) [8], [14], [56], [68].

On the other hand, new integration techniques, such as three-dimensional (3D) integrated circuits (ICs), promise new computing architectures and further energy efficiency benefits. Monolithic 3D integration, whereby multiple layers of circuits are fabricated directly over one-another on the same starting substrate (i.e., no wafer bonding required), enables nano-scale inter-layer vias (ILVs) to connect vertical layers of a 3D IC providing fine-grained and dense vertical connectivity between circuit layers [69], [70]. Such massive physical connectivity can translate to large increases in data bandwidth between vertical layers, which can improve energy efficiency by >100× for abundant-data applications [15], [71].

Despite these promising directions, there are substantial challenges for realizing these future electronic systems. For instance, monolithic 3D integration requires that all processing on the upper layers must be low temperature (e.g., <400 °C), as higher temperatures damage lower-level FETs and destroy low-temperature back-end-of-line (BEOL) metal interconnects [15]. As a result, many technologies, including silicon and beyond-silicon semiconductors (such as III-V compound semiconductors), are challenging to

integrate in monolithic 3D systems, since they require high-temperature processing for both high-quality single-crystalline synthesis and high-temperature anneals (>1000 °C) for doping and junction formation in traditional FETs.

Here, we present a new paradigm for electronic systems: X3D. X3D enables a wide-range of semiconductors, including conventional silicon, next-generation III-V compounds (as an example, in this work we use GaAs), and nanotechnologies such as CNTs to be heterogeneously integrated over the same starting substrate in a monolithic 3D IC. Thus, X3D combines the energy efficiency benefits of beyond-silicon devices, the benefits of monolithic 3D integration, and the flexibility of customizing different vertical 3D layers enabled by a wide-range of semiconductors. Importantly, this work is in stark contrast to previous demonstrations of monolithic 3D integration of heterogeneous technologies (silicon and CNTs [15], [70]), as upper-layers of circuits were all constrained to CNTs; X3D enables arbitrary vertical interleaving of Si, III-Vs, CNTs, *etc*.

The key to X3D is using junctionless nanowire FETs (JNFETs) [72] in which: (1) the high temperature synthesis and uniform doping of each "X" semiconducting channel is performed on a donor substrate (i.e., which is separate from the substrate used for circuit fabrication), (2) the "X" nanowires (NWs, including CNTs and Si-/III-V-based NWs) are released in different solutions, and (3) for any circuit layer in the monolithic X3D IC, "X" NWs are deposited on the substrate using a low-temperature process (e.g., solution-based processing), followed by transistor fabrication (all <200 °C). Importantly, there are no additional high-temperature processing steps (e.g., doping) on the target substrate (X3D IC).

2.2.2 X3D Process Flow

The process flow for X3D decouples the nanowires' high-temperature synthesis, doping, and annealing fabrication steps from the low-temperature FET fabrication steps (Fig. 2.8). First, NW synthesis of "X"

technology is performed on a donor substrate. NWs are then uniformly-doped either by introducing the dopants during NW synthesis (in-situ doping) or post-synthesis (through gas-phase doping or implantation). Following these high-temperature processing steps – which are all performed on the donor substrate (i.e., not on the monolithic X3D IC) – the NWs are released into solution using ultrasonication. To fabricate an "X" layer within a monolithic X3D IC, the desired NW solution is deposited on the target substrate. This solution processing is performed at room-temperature. For FET fabrication, the source, drain, and gate are lithographically patterned, and all NW segments outside FET channel regions are etched away and thus are removed from the circuit. Due to the decoupled NW synthesis and lack of junction formation once on the monolithic X3D IC, all processing on the monolithic X3D IC is <200 °C, rendering the process monolithic 3D compatible as well as silicon CMOS compatible. Following fabrication of each monolithic X3D layer, inter-layer dielectrics (ILDs) are deposited, and ILVs used for metal routing are defined. Importantly, these ILVs can be >1,000× denser versus through-silicon vias (TSVs) owing to monolithic 3D integration, providing dense connectivity between vertical layers of the monolithic X3D IC [15], [69].

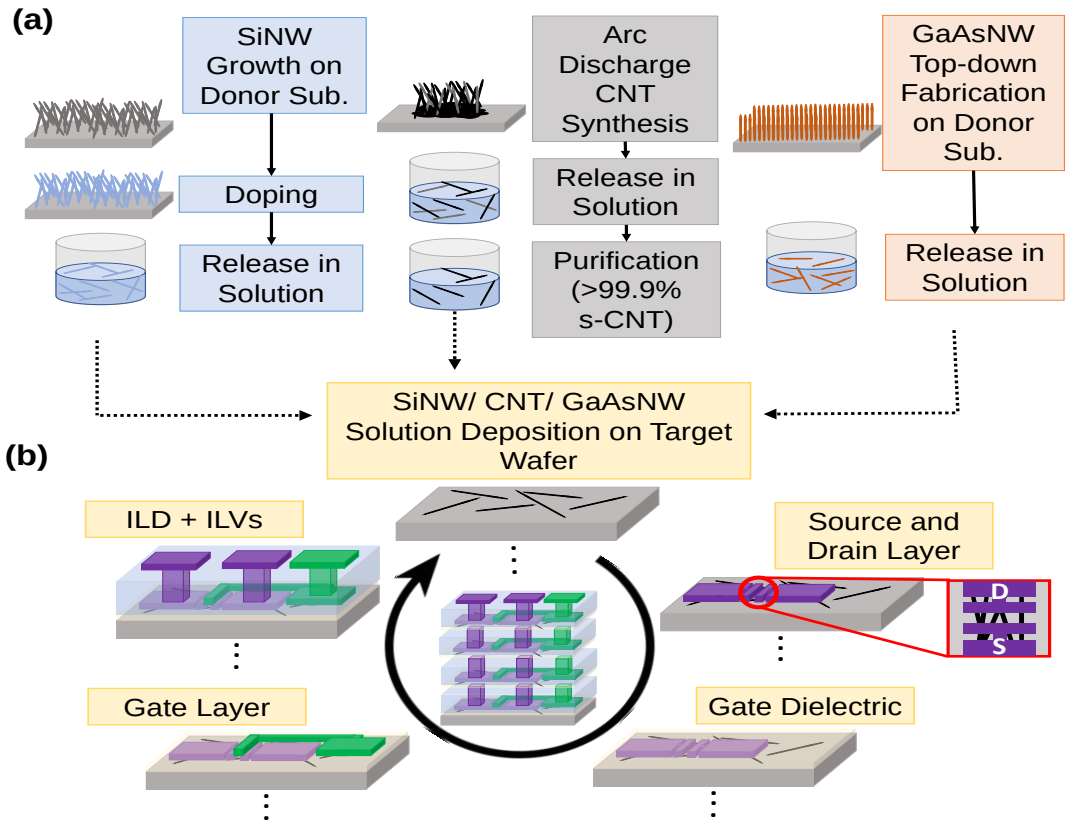

Figure 2.8. Process flow of X3D. (a) Schematic of NW and CNT synthesis and doping. (Left) SiNWs are synthesized and gas-phased doped post-synthesis on a donor substrate. Ultrasonication releases the SiNWs in IPA. (Middle) CNTs are grown via arc discharge, released in solution and sorted via density gradient centrifugation. (Right) GaAsNWs are synthesized through a top-down fabrication of a pre-doped GaAs substrate. Ultrasonication releases the GaAsNWs in IPA. (b) VLSI–scalable and CMOS compatible device fabrication flow of each X3D vertical layer. The "X" semiconductor solution is deposited, followed by PVD of source, drain, and gate (Ti/Pt) with ALD-deposited HfO_X as the high-*k* gate dielectric. Between each vertical layer, an inter-layer dielectric (PVD SiO_2) is deposited and ILVs (metal vias) are defined. These same steps are repeated for every layer in the X3D chip.

The use of NWs is essential, as it allows each of the "X" semiconductors to be released in solution for subsequent use in identical processing steps. JNFETs are essential as the entire NW can be uniformly doped; this enables the NWs to be placed in arbitrary locations across the substrate without requiring specific doping regions or precise alignment with the subsequent transistor formation (e.g., NPN aligning with source, gate, and drain). Moreover, the NWs and JNFETs are ideal pairings as the ultra-thin body thickness of the NWs are essential for JNFET electrostatic control [72], [73].

The detailed NW synthesis flow is shown in Fig. 2.9. SiNWs are grown in a low-pressure chemical vapor deposition (LPCVD) system via a vapor-liquid-solid (VLS) method [74]. CNTs are synthesized through arc discharge [75], and >99.9% semiconducting CNTs are sorted and released in solution via density gradient centrifugation [76], [77]. GaAsNWs are defined through top-down fabrication using precision reactive ion etching [78], [79]. To form either p-type or n-type JNFETs, the NWs are doped either before or during synthesis (e.g., GaAsNWs are defined in pre-doped GaAs substrate), through gas-phase doping post-synthesis (for SiNWs) [80], [81], or through field-effect doping (for CNTs) [60], [82], [83]. Post-doping, the NWs are deposited on the target layer of the monolithic X3D through solvent deposition. To do so, the NWs are dispersed in solvent (SiNWs and GaAsNWs in IPA, CNTs in toluene) through ultrasonication. The solution with suspended NWs is then drop-casted and dried on the monolithic X3D IC, depositing the NWs. While we leverage a simple drop-casting technique to deposit the NWs over the monolithic X3D IC for ease of integration, a range of techniques have demonstrated aligned and dense NW deposition from solution [84]-[88]. Once the doped NWs are deposited on the substrate, the JNFETs to

form the circuit on that layer of the monolithic X3D IC are defined. The source, gate, and drain (~1 nm titanium / ~30 nm platinum) are lithographically patterned, while the high-*k* gate dielectric (~25 nm HfO_x) is ALD-deposited (all processing <200 °C).

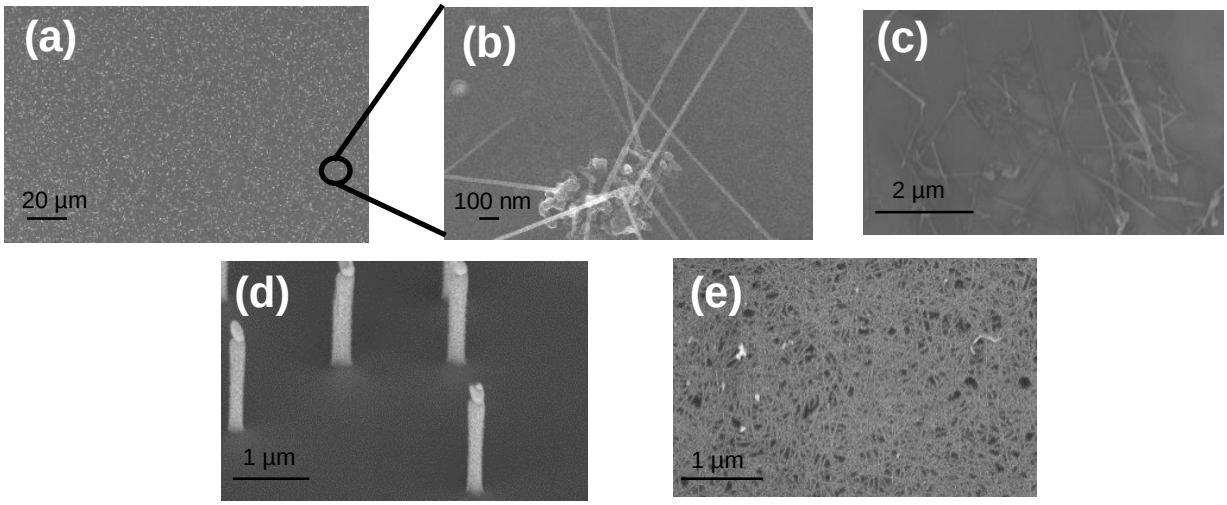

Figure 2.9. SEMs of donor and target substrates. (a-b) single-crystalline SiNWs on donor. (c) SiNWs deposited over the target X3D substrate. (d) GaAsNWs on donor. GaAsNWs are etched by ICP-RIE into an n-doped GaAs substrate. (e) CNTs deposited over the target X3D substrate.

2.2.3 Experimental Results

As an experimental demonstration of X3D, we fabricate a monolithic X3D IC with 5 vertical circuit layers comprising 3 different semiconductors (Si, III-V, and CNTs). As shown in Fig. 2.10, it comprises (from bottom to top): Si p-JNFETs, n-CNFETs, Si n-JNFETs, p-CNFETs, and III-V n-JNFETs. The ordering of the layers is chosen to explicitly demonstrate the ability to arbitrarily stack these technologies within the monolithic X3D IC: silicon (layer 3) is integrated over silicon (layer 1), CNT (layer 4) is integrated over CNT (layer 2), CNT (layer 2) is integrated over silicon (layer 1), silicon (layer 3) is integrated over CNT (layer 2), and III-V is integrated over both silicon (layers 1 and 3) and CNT (layers 2 and 4). The FETs shown in Fig. 2.10a are staggered for visibility; FETs can be vertically overlapping as well. To characterize the monolithic X3D process, we fabricate and measure the JNFETs across every layer of the monolithic X3D IC. To validate that the JNFETs can be vertically interleaved on arbitrary circuit layers, we measure

the JNFETs on each layer immediately after fabrication of that layer, as well as after the entire subsequent monolithic X3D processing (Fig. 2.11). As shown in Fig. 2.11c, the JNFETs on all layers exhibit negligible performance change due to subsequent monolithic X3D processing; the on-state drive current (I_{ON}, i.e., measured drain current when $|V_{GS}| = |V_{DS}| = V_{DD}$) of each vertical layer immediately after fabrication and post subsequent monolithic X3D processing exhibit insignificant change (we fail to reject the null hypothesis that the average I_{ON} are the same before and after monolithic X3D fabrication, using the two samples t-test for difference in mean with 95% confidence [89]).

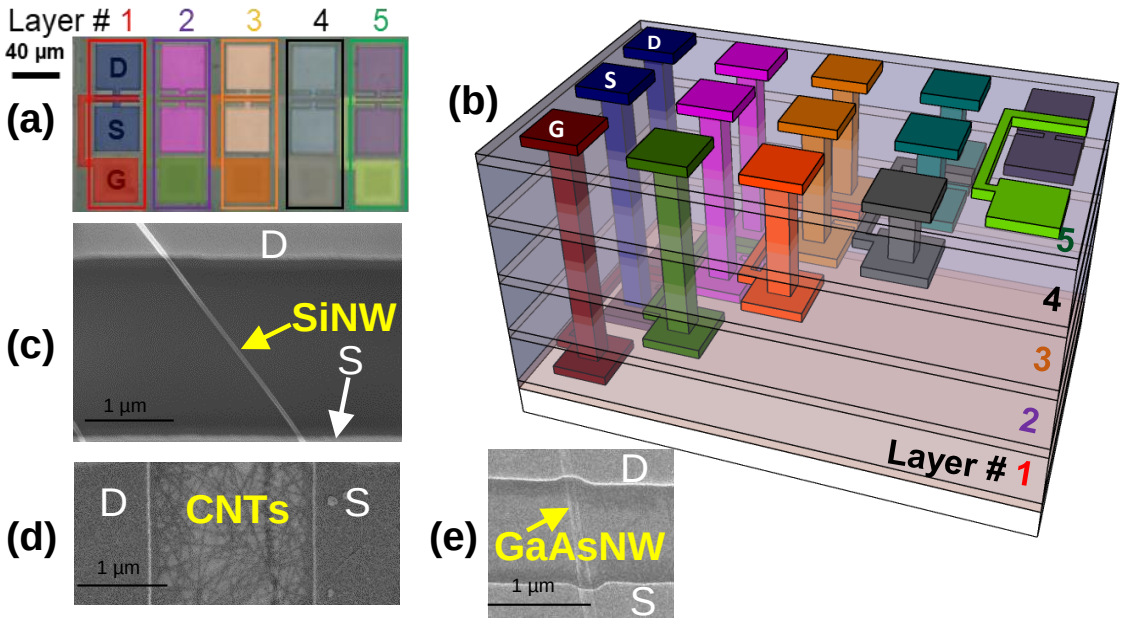

Figure 2.10. (a) Optical microscopy image of devices fabricated on each layer of the 5-layer X3D chip, with their respective source, drain, and gate metals highlighted. (b) 3D schematic of fabricated 5-layer X3D stack. SEMs of (c) SiNWs (d ~ 20 nm), (d) CNTs (d ~ 1 nm), and (e) GaAsNWs (d ~ 100 nm) bridging the source and drain contacts. All FETs are fabricated with a top-gate geometry, except for the p-CNFETs (layer 4) which use a local bottom-gate geometry. All FETs have 40 nm source and drain contacts (Pt), leverage a high-*k* metal gate stack (25 nm high-*k* HfO_X gate dielectric, 20 nm Pt gate). The inter-layer dielectrics (ILDs) are all 100 nm SiO_2.

As a demonstration, we experimentally show functional complementary digital logic circuits spanning multiple vertical circuit layers and semiconductor technologies: between Si p-JNFETs (layer 1) and n-CNFETs (layer 2), and between p-CNFETs (layer 4) and Si n-JNFETs (layer 3) (Fig. 2.12). As shown in

Fig. 2.12a, the source terminals of layers 1 and 2 are connected using ILVs to define the output terminal for inverter 1, and the gate terminals of layers 1 and 2 are likewise connected through ILVs to define the input terminal. The same case holds for inverter 2 spanning layers 3 and 4. Correct inverter logic functionality is illustrated in Fig. 2.5c when operating at a supply voltage of 1.8 V_{DD}, where logical low input signals return a logical high output and logical high input signals return a logical low output.

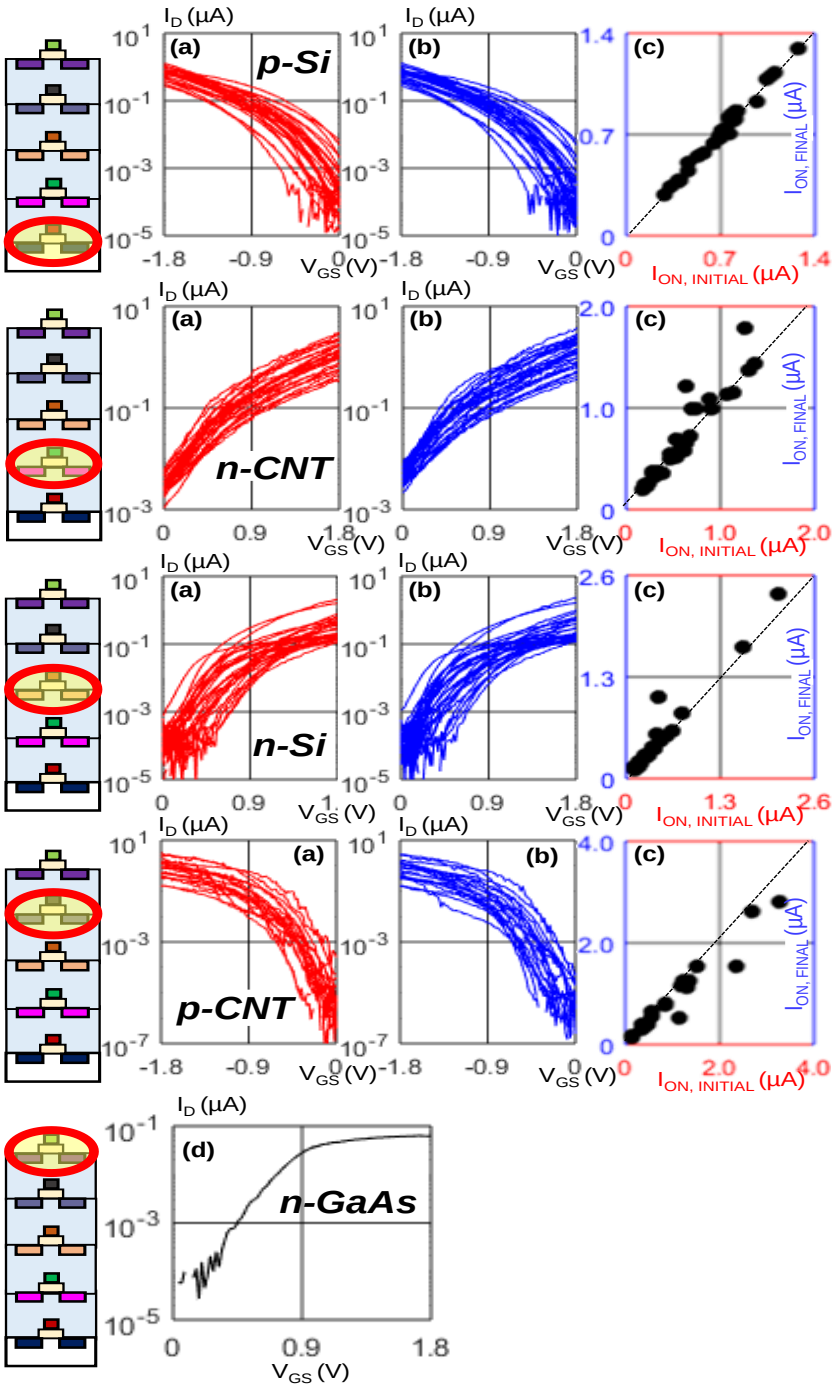

Figure 2.11. I_D – V_{GS} characteristics of first four layers of devices (30 FETs per layer). (a) measured immediately after fabrication, and (b) measured again after monolithic X3D processing. (c) I_{ON} pre- and post- monolithic X3D processing shows negligible change resulting from X3D processing. The line with slope of 1 is the ideal case. Subthreshold slopes ~100-200 mV/decade. (d) I_D – V_{GS} characteristic of a typical GaAs n-JNFET on the fifth layer of the monolithic X3D IC. Post- monolithic X3D processing I_D-V_{GS} are not shown as this is the final layer of the monolithic X3D stack. Si- and GaAs-based JNFETs have ~1-2 NWs per JNFET, while CNT-based JNFETs have ~30 CNTs/μm.

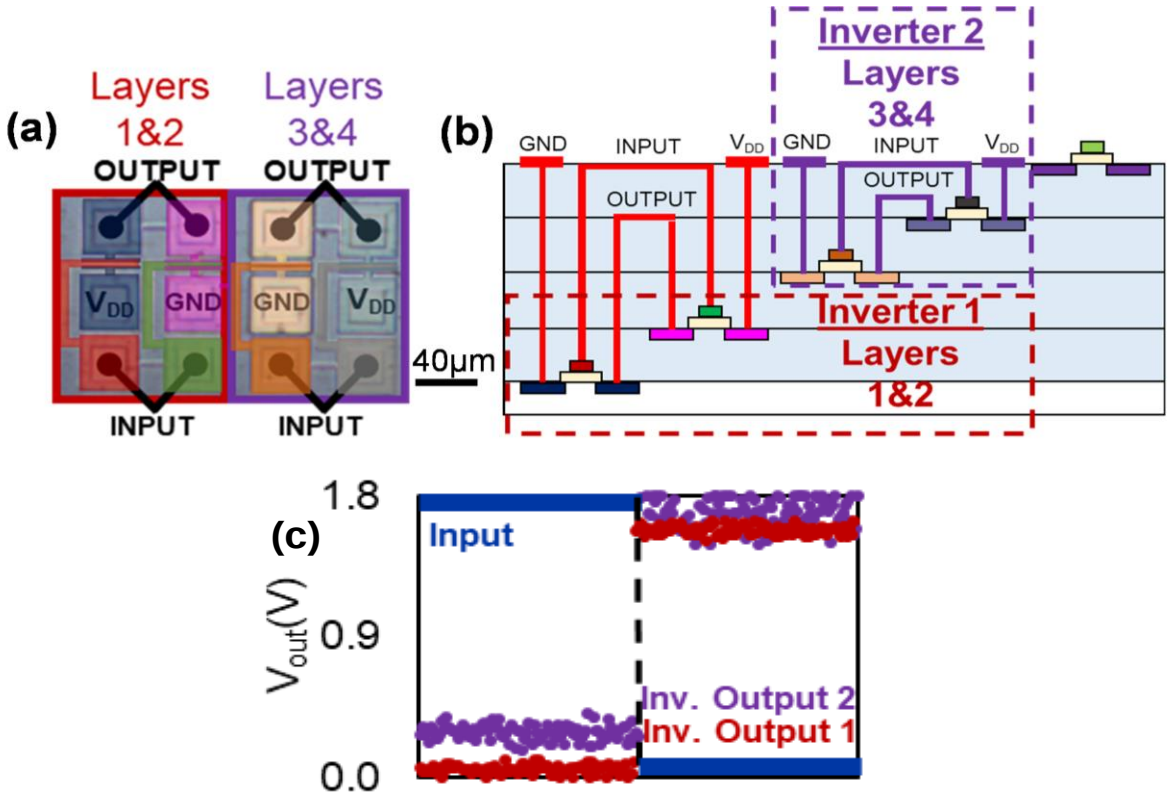

Figure 2.12. (a) Optical microscopy image of two fabricated monolithic X3D CMOS inverters, with inverter 1 spanning layer 1 (Si p-JNFET) and layer 2 (n-CNFET), and inverter 2 spanning layer 3 (Si n-JNFET) and layer 4 (p-CNFET). (b) Cross-sectional schematic of monolithic X3D inverters. (c) Output voltages given inputs toggled between 0 V and V_{DD} (1.8 V).

2.2.4 Conclusion

This work demonstrates X3D, a new paradigm for monolithic 3D integration, which enables heterogeneous integration of a wide range of nanowire-based semiconductors. With our first demonstration of X3D, we integrate three different technologies (silicon, CNTs, and III-Vs) spanning 5 vertically-interleaved layers, forming complementary digital logic. Importantly, X3D provides a framework that allows all layers to be fabricated with identical processing steps for ease-of-integration and allows arbitrary ordering of layers. While an example case-study, such flexible and customizable heterogeneous integration has potential for a wide range of applications. Each layer of monolithic X3D ICs can be customized for specific functionality; e.g., wide-bandgap III-Vs for power management, CNTs for energy efficient computing, and tailored bandgaps for specialized sensors or imagers. Thus, this work provides a new direction for future generations of electronic systems to grow in diversity and customization, integrating an increasingly wide range of new

technologies within ICs.

Chapter 3: CNT-based System Demonstrations: First CNT-based SRAM Arrays

3.1 Introduction

CNFETs are a promising emerging nanotechnology for next-generation energy-efficient digital very-large-scale-integration (VLSI) circuits. Owing to their simultaneously ideal electrostatic control (due to the ultra-thin ~1 nm diameter of a CNT) and high carrier transport [91], [92], it is projected CNFETs can improve the energy-delay product (EDP, a metric of energy efficiency) by an order of magnitude versus silicon CMOS [8], [13], [71]. In addition to these EDP benefits, CNFET digital logic has been fabricated at a record scaled 30 nm contacted gate-pitch (CGP, a key metric defining the area of a FET), demonstrating the potential to realize a sub-3 nm node technology [92]. Furthermore, CNFETs are a rapidly maturing nanotechnology, as complete digital systems [14], [26] - [29], [70], [93], and complex analog and mixed-signal circuits [21], [22] have been experimentally demonstrated.

Despite these increasingly complex CNFET demonstrations, a critical component of digital systems – SRAM memory arrays – had never been demonstrated. Prior work has either realized only individual, isolated CNT-based SRAM cells [39], or has relied on processing that is not compatible with silicon CMOS (e.g., relying on air-reactive, ionic, non-solid-state CNT doping processes [94] – [101]). Here we highlight the first demonstration of kbit 6T CNFET CMOS SRAM arrays. We demonstrate all SRAM cells within the array functioning correctly without relying on any customization, calibration, or correction of any sort. This is the largest reported CNFET CMOS circuit demonstrated to-date, containing 6,144 CMOS CNFETs. To further demonstrate the maturity of CNFET CMOS, we further demonstrate the first 10T CNFET CMOS SRAM cells, which can operate at highly-scaled supply voltages down to 300 mV. Importantly, all design and processing is (1) wafer-scale (performed on 150 mm substrates), (2) VLSI-compatible (no per-unit customization), and (3) silicon-CMOS compatible (leveraging only solid-state and silicon-compatible

materials and conventional fabrication process steps).

This work is an extension of the IEEE 2019 Symposium of VLSI Technology manuscript entitled, “1 Kbit 6T SRAM Arrays in Carbon Nanotube FET CMOS” [102]. In addition to summarizing those results, we include additional 6T SRAM characterization, as well as the first experimental demonstrations of CNFET CMOS 10T SRAM cells.

3.2 CNFET CMOS SRAM FABRICATION

The CNFET CMOS fabrication process flow is illustrated in Fig. 3.1. The starting substrate is a 150 mm silicon wafer with ~1 µm thermal SiO_2. Prior to any CNFET fabrication, we fabricate a bottom metal layer of metal as buried power rails. An inter-layer dielectric (ILD) is deposited followed by defining metal vias down to the buried power rails. The next metal layer is defined, which acts as both metal routing (for the wordlines) as well as the bottom metal gates for the CNFETs. To fabricate the CNFETs, a high-*k* gate dielectric (HfO_2) is deposited through ALD (200 °C), followed by CNT deposition. We deposit the CNTs uniformly across the 150 mm substrate through a solution-based deposition, whereby the wafer is submerged in a solvent containing dispersed CNTs (the CNTs are pre-purified within this solution to achieve >99.99% semiconducting CNTs see ref. [103], [104] for details). Following CNT deposition, the active area (e.g., channel area) of the CNFETs is defined through traditional photolithography and all CNTs outside of the active regions are etched away using oxygen plasma. The next metal layer (Pt) is defined, which acts as both the CNFET source and drain contacts for the p-type CNFETs as well as additional metal routing (bit/bit_b lines). The finished p-type CNFETs are protected and passivated with 100 nm SiO_2. To fabricate the n-type CNFETs, we deposit the next metal layer (Ti) as the n-type CNFET source and drain contacts, followed by ALD deposition of HfO2 (which electrostatically dopes the CNTs to achieve the correct threshold voltage, see ref. [83] for details). The HfO_2 electrostatic doping film is etched off of the p-type CNFETs (which are protected by the SiO_2 passivation), leaving our final CNFET CMOS. The full

process contains three metal layers, and uses only silicon-CMOS compatible materials. Key aspects of this fabrication process are:

1. The buried metal layers beneath the CNFET device layer can be fabricated using conventional BEOL metallization processes.
2. Such buried metal layers are very challenging to realize with conventional silicon CMOS due to high-temperature processing required for fabricating silicon CMOS (>1000 °C for steps such as dopant activation annealing [29]).
3. In contrast, the low-temperature (<400 °C) CNFET processing naturally enables such buried metal layers and new three-dimensional circuit architectures. Specifically, the room-temperature solution CNT deposition decouples the high-temperature CNT synthesis (typically >800 °C) from the wafer fabrication, and the CNFET CMOS doping process (leveraging both metal source and drain work function engineering as well as high-*k* electrostatic doping) never exceeds 250 °C.
4. While our experimental demonstration of CNFET CMOS SRAM only leverages a single buried metal layer (utilized as buried power rails), the same BEOL metallization process can be repeated to realize multiple buried metal layers (in addition to multiple conventional BEOL metal layers above the device layer as well).
5. The entire fabrication process is wafer-scale, solid-state, and BEOL compatible (<400 °C). Thus, while we fabricate our CNFET CMOS SRAM over silicon substrates, the substrate could be silicon CMOS circuitry, additional layers of CNFET CMOS circuitry, etc.

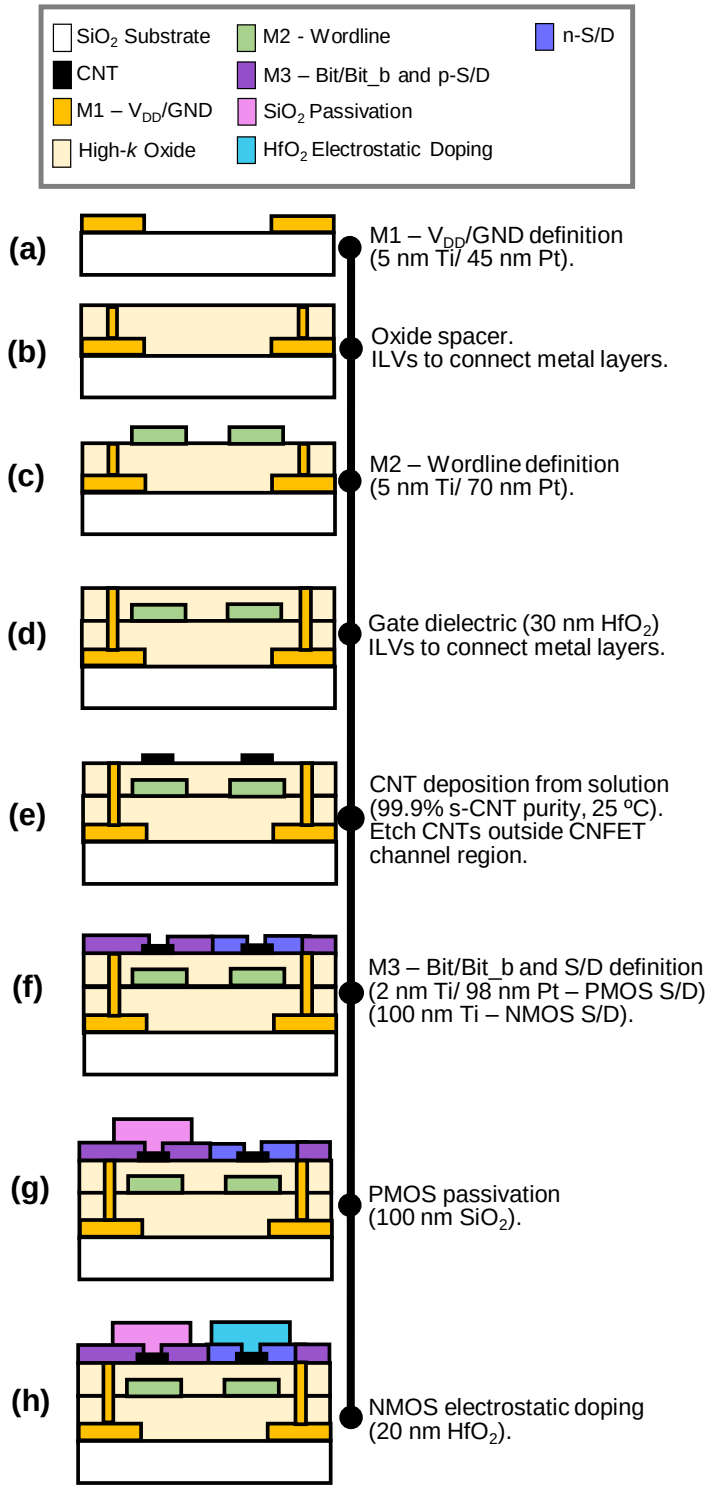

Figure 3.1. Process flow for the CNFET CMOS SRAM. (a) M1, the first metal layer, which consists of the V_{DD} and V_{SS} lines is defined (5 nm Ti/ 45nm Pt) via PVD. (b) Oxide spacer deposition followed by etch and metal fill for inter-layer via (ILV) definition. (c) M2, the second metal layer, is defined (5 nm Ti/ 70 nm Pt) for the wordlines and back gates of the CNFETs. (d) High-*k* gate dielectric deposition (30 nm HfO_2) via ALD, and additional ILV definition. (e) CNTs solution-deposited at room temperature uniformly across the wafer followed by oxygen plasma to etch away CNTs outside the active area (e.g. channel). (f) M3, the

third metal layer, consists of bit, bit_b and PMOS source/drain definition (2 nm Ti/ 98 nm Pt) as well as NMOS source/drain definition (100 nm Ti). (g) Passivation over the PMOS (100 nm SiO_2). (h) Electrostatic doping over the NMOS (20 nm HfO_2).

Fig. 3.2 shows the circuit schematic as well as a three-dimensional schematic of a single 6T CNFET CMOS SRAM cell. Fig. 3.3 shows scanning electron microscopy (SEM) images of a fabricated 1 kbit CNFET CMOS 6T SRAM array as well as a single 6T SRAM. Fig. 3.2 and 3.3 highlight the buried metal process whereby the power lines (V_{DD} and V_{SS}) are routed directly beneath the CNFET CMOS SRAM array, with the CNFETs and signal routing fabricated directly vertically overlapping (on the same substrate without any die- or wafer-bonding). Such three-dimensional circuit architectures can provide additional future opportunities for further SRAM density scaling and reduced routing congestion. The SRAM density in this demonstration is limited due to the fact that the CNFETs are fabricated at a relaxed ~1 µm technology; this is only due to the limitations of academic fabrication facilities, as this same CNFET fabrication process has been experimentally demonstrated to potentially scale to aggressive technology nodes (CGP = 30 nm).

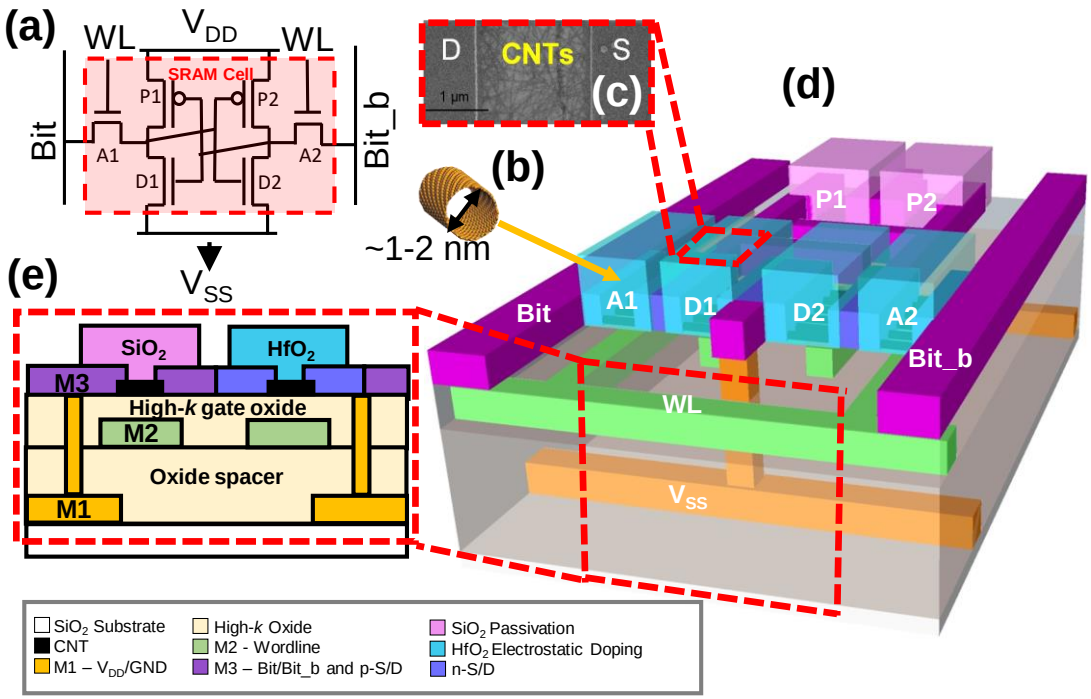

Figure 3.2. CNFET-based CMOS SRAM (a) Schematic of 6T SRAM cell. (b) Carbon nanotube (CNT). (c) Scanning electron microscope (SEM) image of D1 CNFET (fabricated at a ~1 µm technology node due to lithographic limitations in an academic fabrication facility, with a ~2 µm physical channel length). (d) 3D illustration of CNFET-based SRAM cell in an array, including the V_{DD} and V_{SS} lines in the first metal (M1) layer, wordline (WL) in the second metal (M2) layer, bit and bit_b lines, p-type and n-type CNFET

source/drain contacts in the third metal (M3) layer, and the SiO_2 passivation and HfO_2 electrostatic doping films for p-type and n-type CNFETs, respectively. (e) Cross-section showing all three metal layers and their vertical integration.

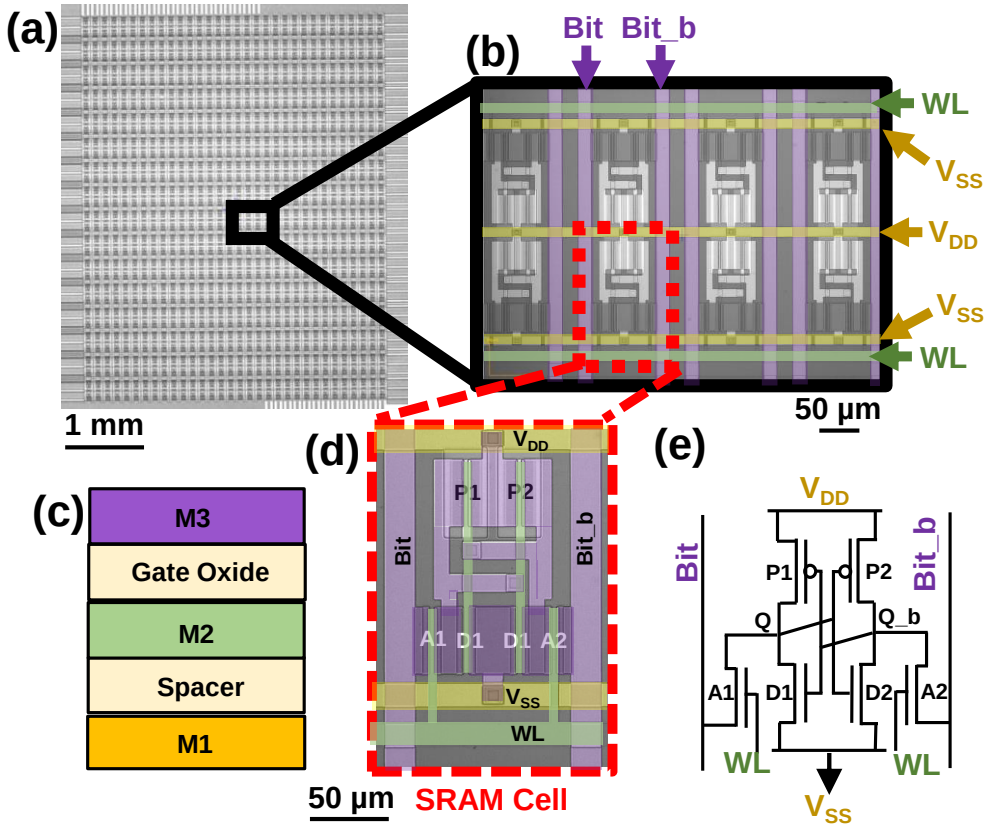

Figure 3.3. Scanning electron microscopy (SEM) images of the (a) fabricated 1 kbit CNFET CMOS 6T SRAM array, (b) sub-section of the SRAM array (2×4 SRAM cell segment), and (d) false colored SRAM cell from the full array based on the (c) metal layer sequence. Labelling of the false colored image is according to the (e) 6T SRAM cell schematic. The peripheral control and read-out circuitry is off-chip; future work will focus on integrating the peripheral control circuitry and read-out circuity on-chip on either the same CNFET CMOS circuit layer or on a layer of silicon CMOS or CNFET CMOS circuitry fabricated beneath the CNFET CMOS SRAM array.

3.3 Experimental Results: CNFET CMOS 6T SRAM

6T Array-level Testing (Fig. 3.5): To illustrate the robust CNFET CMOS process, we fabricate 1 kbit CNFET CMOS 6T SRAM arrays; this is the largest reported CNFET CMOS circuit demonstrated to-date, containing 6,144 CMOS CNFETs. A packaged die micrograph of a fabricated CNFET CMOS 1 kbit SRAM array is shown in Figure 3.4. To test the functionality of the fabricated SRAM arrays, we first write the entire array, and then read the entire array. All of the bits are initially written, and then all of the bits are read, highlighting the ability to non-destructively read from the SRAM array. The measured results of

various patterns (e.g., checkerboard, inverted checkerboard, and the letters M, I, and T) are shown in Fig. 3.4. These patterns test every possible SRAM cell in the array at both values (both with the cell programmed at logical value “1” and at logical value “0”), illustrating correct functionality of every cell in the array simultaneously (we also read the array multiple times to ensure ability to perform non-destructive repeated reads).

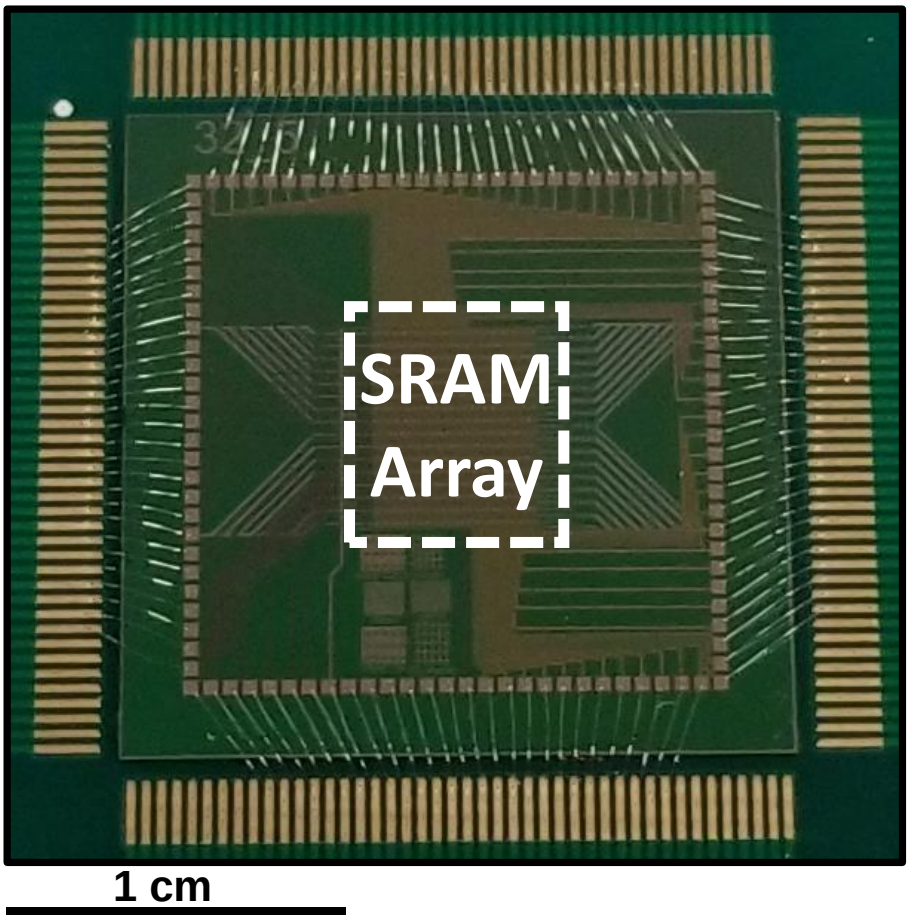

Figure 3.4. Packaged kbit CNFET CMOS 6T SRAM array prior to testing. Conventional wirebonding is used to access pads on the die.

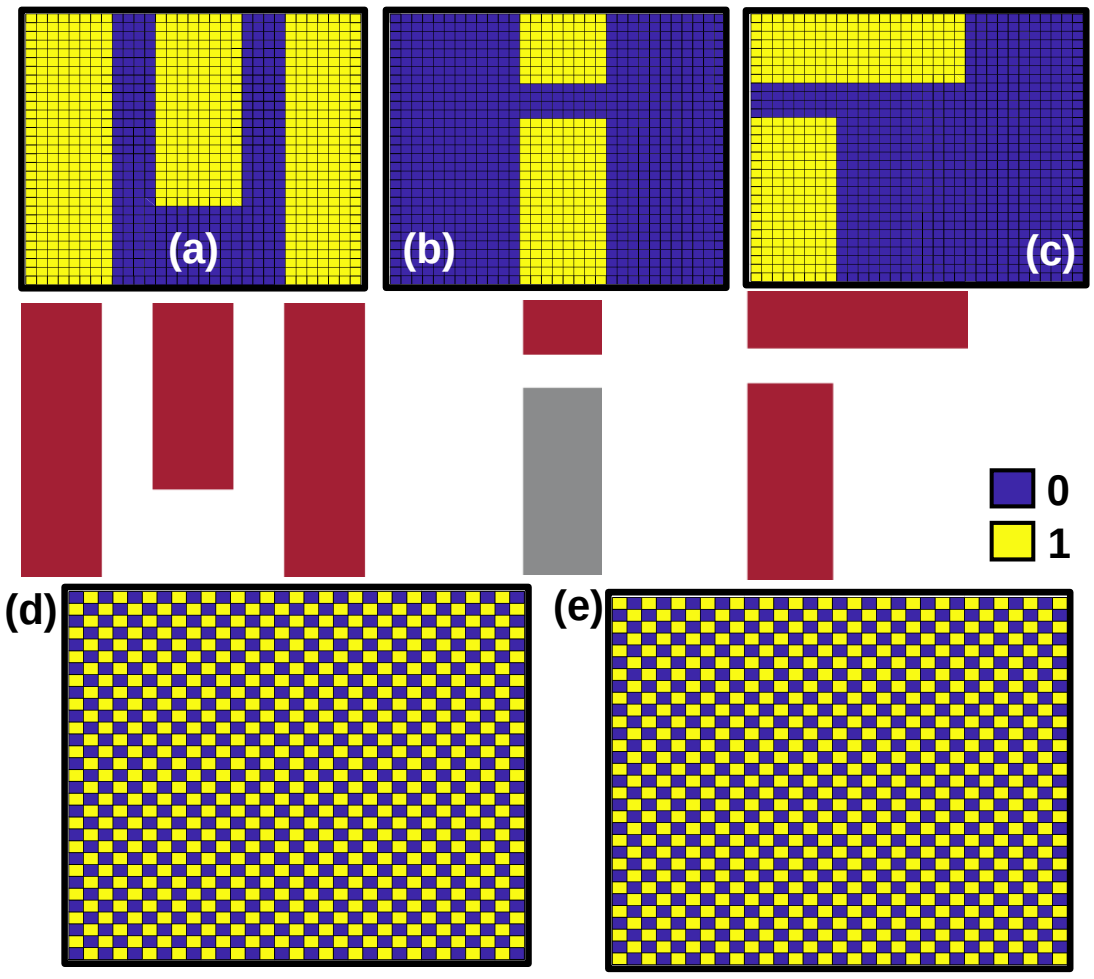

Figure 3.5. Array-level testing of the fabricated kbit CNFET CMOS 6T SRAM arrays (V_{DD} = 1.8 V). Various patterns (e.g., (a – c) letters spelling out MIT, (d) checkerboard, (e) inverted checkerboard) were written to- and subsequently read out from the array to demonstrate complete functionality. Bit values of 1 and 0 are shown as yellow and blue pixels respectively. Supply voltage (V_{DD}) = 1.8 V.

6T Cell-level Characterization (Fig. 3.6): In addition to array-level testing to show functionality, we fabricate individual CNFET CMOS 6T SRAM cells to both characterize the variability and demonstrate the robustness of the cells. Fig. 3.6a shows an SEM of a single isolated 6T SRAM cell (labels correspond with labels in Fig. 3.2 and 3.3), while Fig. 3.6b shows typical p-type and n-type CNFET I_D-V_{GS} curves highlighting the well-matched CMOS CNFETs with I_{ON}/I_{OFF} ratios of >1,000. The measured distributions of the write, read, and hold margins for a set of 6T SRAM cells are shown in Fig. 3.6g-i. These metrics are defined as followed (Fig. 3.6c-e):

1. *Write margin* (Fig. 3.6e) – Let the tripping point (V_{TP}) be where bit = Q_b = V_{TP} with WL = V_{DD}

(Fig. 3.6e) [105]. The write margin (WM), write margin high (WMH), and write margin low (WML) are defined in (1)-(3) as:

$$\text{WML} = V_{TP} - V_{SS} \quad (1)$$

$$\text{WMH} = V_{DD} - V_{TP} \quad (2)$$

$$\text{WM} = \min(V_{TP} - V_{SS}, V_{DD} - V_{TP}) \quad (3)$$

2. *Read margin* and *hold margin* (Fig. 3.6c and 3.6d) – The read margin and hold margins extractions are from the relationship between *Q_b* and *Q* referred to as the *voltage transfer curve* (VTC): *Q_b* vs. *Q*, with bit = V_{DD}, bit_b = V_{DD}, and with WL = V_{DD} (for read margin VTCs) and WL = V_{SS} (for hold margin VTCs) [105], [106]. Let ($V_{IL}^{(dr)}$,$V_{OH}^{(dr)}$) and ($V_{IH}^{(dr)}$,$V_{OL}^{(dr)}$) be the points on the VTC$^{(dr)}$ where the slope of *Q_b* vs. *Q* is -1, and let ($V_{IL}^{(ld)}$,$V_{OH}^{(ld)}$) and ($V_{IH}^{(ld)}$,$V_{OL}^{(ld)}$) be the points on the VTC$^{(ld)}$ (i.e., the mirrored VTC: V_{in} vs. V_{OUT}) where the slope of *Q_b* vs. *Q* is -1. For their respective VTCs, the read/hold margin (RM/HM), the read/hold margin high (RMH/HMH), and read/hold margin low (RML/HML) are defined in (4)-(6) as:

$$\text{RMH or HMH} = V_{OH}^{(dr)} - V_{IH}^{(ld)} \quad (4)$$

$$\text{RML or HML} = V_{IL}^{(ld)} - V_{OL}^{(dr)} \quad (5)$$

$$\text{RM or HM} = \min(V_{OH}^{(dr)} - V_{IH}^{(ld)}, V_{IL}^{(ld)} - V_{OL}^{(dr)}) \quad (6)$$

Fig. 3.6f shows 1,000 repeated write measurements of the same 6T SRAM cell. The cells exhibit minimal drift and hysteresis over continuous biasing and time (>12 hours), as the absolute maximum and minimum write margins differ by <10 mV (performed with V_{DD} = 1.8 V) across all 1,000 repeated write cycles.

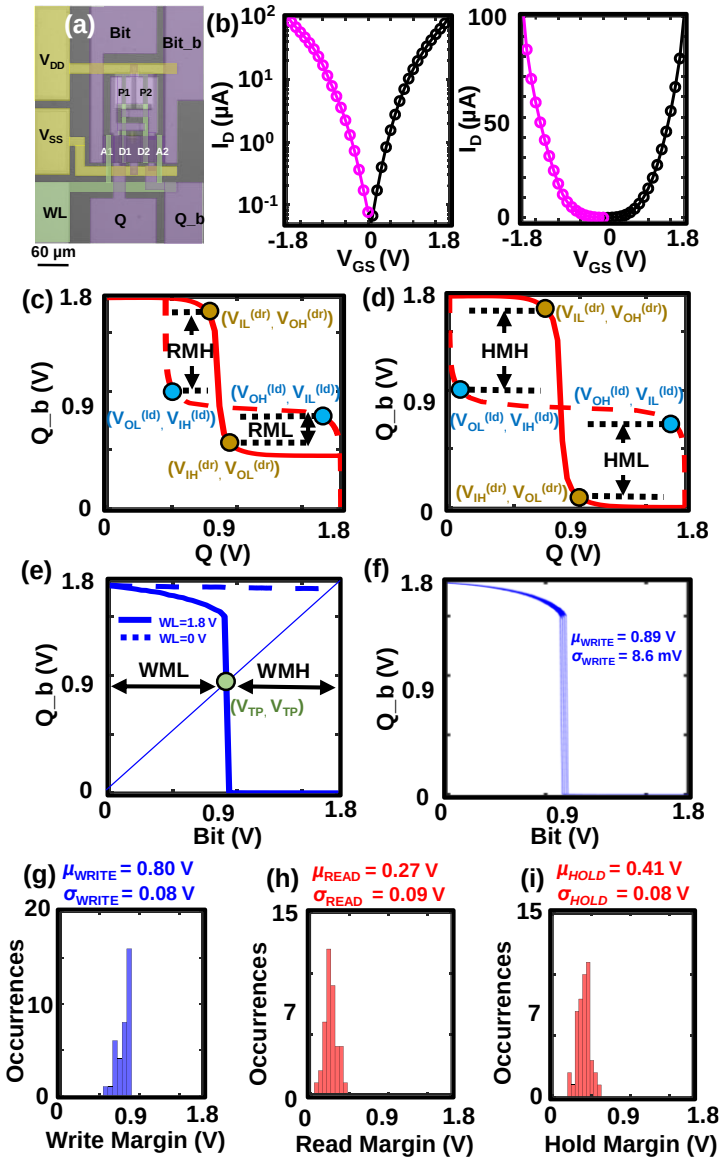

Figure 3.6. 6T Cell-level characterization. (a) False colored optical microscopy image of CNFET CMOS 6T SRAM cells fabricated for cell characterization. A sizing ratio of 2.25:1.5:1 (D1/D2:A1/A2:P1/P2) was used. (b) I_D vs. V_{GS} characteristics, in semi log and linear scale, of a typical PMOS (purple) and NMOS (black) CNFET (channel length = 2 µm, channel width = 40 µm, CNT density ~ 20 CNTs/µm), with V_{DS} = 1.8 V for NMOS and V_{DS} = 1.8 V for PMOS. (c) Read margin, (d) hold margin and (e) write margin measurement from a typical CNFET CMOS 6T SRAM cell. (f) 1,000 overlaid write measurements. Statistical distributions of (g) write margin (h) read margin, and (i) hold margin from 40 CNFET CMOS 6T SRAM cells, as well as their respective mean and standard deviations (write margin mean and standard deviation - μ_{WRITE} and σ_{WRITE}, read margin mean and standard deviation - μ_{READ} and σ_{READ}, hold margin mean and standard deviation - μ_{HOLD} and σ_{HOLD}).

3.4 Experimental Results: CNFET CMOS 10T SRAM

Beyond the first 6T SRAM arrays, we experimentally demonstrate the first 10T CNFET CMOS SRAM

cells to highlight the potential for CNFET CMOS circuits to operate at scaled supply voltages [107]. Owing to 10T SRAM cell circuit architecture, we demonstrate their ability to operate at highly-scaled supply voltages down to 300 mV. This is the most scaled operating voltage demonstrated for any CNFET-based SRAM or CNFET-based sequential logic.

10T Cell-level Characterization: The circuit schematic and SEM of a fabricated 10T SRAM cell is shown in Fig. 3.7. The measured characteristics of the 10T SRAM cell are shown in Fig. 3.8. Fig. 3.8a-b shows typical write and read margins for a 10T SRAM cell (measured at V_{DD} = 1 V). In Fig. 3.8c-d, we show time-dependent waveforms of a typical 10T cell. To demonstrate cell functionality, we exercise every potential write and read combination: we first write a "1" to the cell and read it multiple times (to demonstrate non-destructive reads), followed by writing a "0" to the cell and reading it multiple times. Fig. 3.8c shows the measured waveform with V_{DD} = 1 V, while Fig. 8d shows the measured waveform for the same 10T SRAM cell with V_{DD} = 300 mV (for comparison, the CNFET CMOS 6T SRAM cells can operate with a minimal V_{DD} of ~ 1 V).

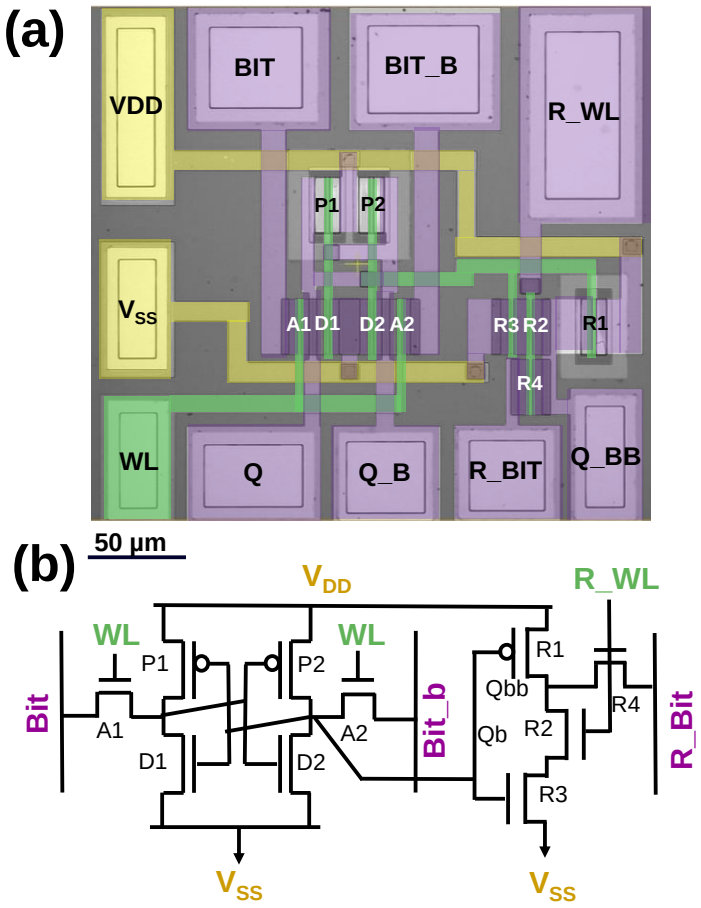

Figure 3.7. False colored scanning electron microscopy (SEM) image of the (a) fabricated 10T CNFET CMOS SRAM cell, and the (b) 10T SRAM cell schematic.

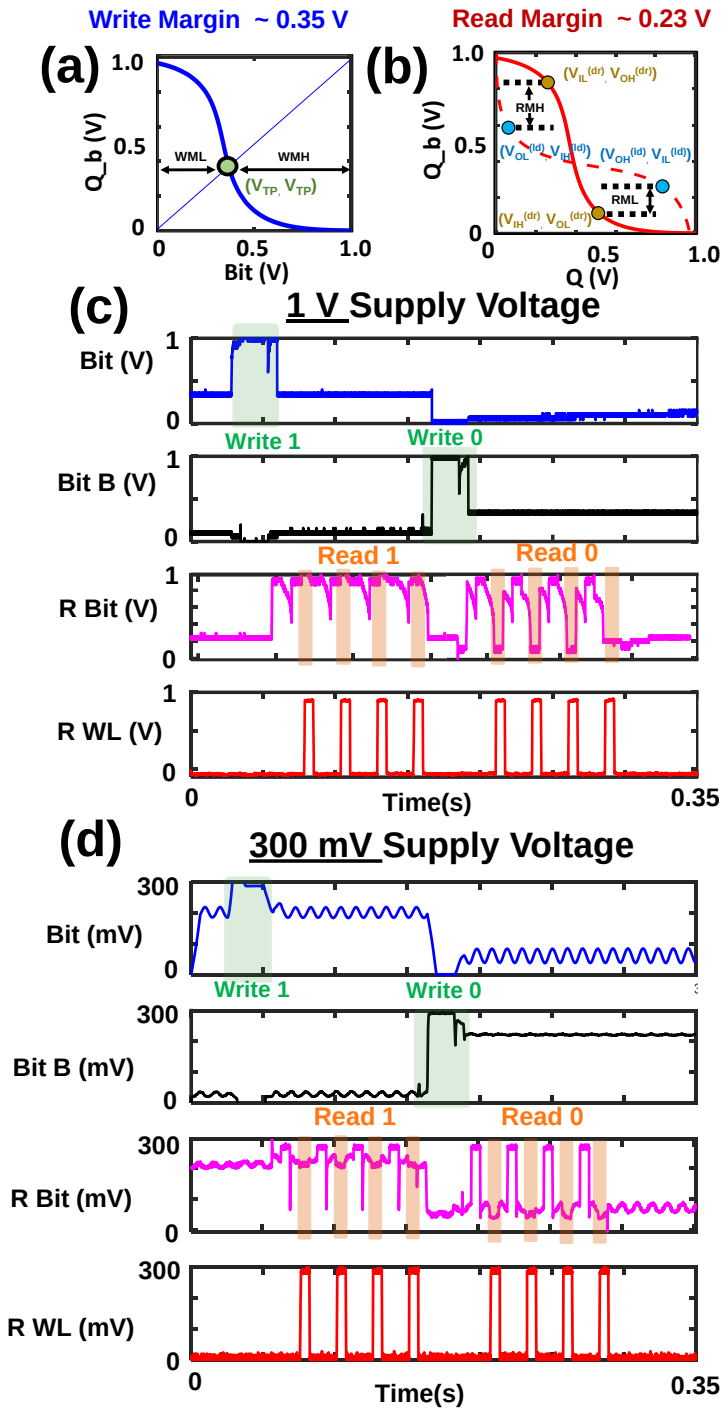

Figure 3.8. 10T Cell-level characterization. (a) Write margin (~ 0.35 V) and (b) read margin (~0.23 V) from a typical CNFET CMOS 10T SRAM cell (V_{DD} = 1 V). Time-dependent waveforms at (c) 1 V V_{DD} and (d) 300 mV V_{DD}. There is still positive read and write margins at V_{DD} = 300 mV, a requirement for digital logic (~0.13 V and ~0.02 V, respectively). Below 300 mV, noise margin violations results in incorrect operation. Clock frequency is limited by the off-chip data acquisition setup that records the output waveform. The measurements in (c) and (d) show first writing a "1" followed by four non-destructive reads, followed by writing a "0" followed by four non-destructive reads. The noise in the waveform is from measuring the cell

while the bit lines are floating, illustrating that the access transistors (CNFET “A1” and “A2” in Fig. 7b) provide ideal electrical isolation of the cell from the bitline.

3.5 Conclusion

This work realizes the first CNFET CMOS SRAM arrays (1 kbit 6T SRAM) comprising 6,144 CMOS CNFETs, as well as the first 10T CNFET CMOS SRAM cells operating at highly scaled supply voltages down to 300 mV. We also demonstrate buried power rails for further SRAM density scaling opportunities. Taken together, this work is a major step towards demonstrating the feasibility of a future CNT-based technology, realizing a critical component of future energy-efficient CNT digital systems.

Chapter 4: New Applications: Radiation-tolerant Electronic Systems for Future Space Missions

4.1 Introduction

Humankind's desire to explore space continues to grow: ambitions range from constructing permanent moon bases to asteroid mining to travelling to Mars [10] – [12]. Yet a critical limitation in space missions today is the underlying electronics driving them: electronics deployed in space today are damaged and eventually destroyed by the harsh radiation environment[3]. Simply relying on computing back on Earth is insufficient as the energy and time required to communicate from deep space to Earth represents the ultimate "communication wall[4]". Thus, enabling future space missions require electronics that are both increasingly energy-efficient (for increased local compute enabling greater autonomy) and simultaneously radiation-tolerant (for increased lifetime and reliability).

To meet these needs, a wide range of emerging nanomaterials and nanodevices are currently being explored. For instance, carbon nanotubes (CNTs, single sheets of carbon atoms rolled to form nanoscale cylinders with diameters of ~1 nm) are a leading contender for next-generation energy-efficient digital very-large-scale-integrated (VLSI) circuits. Owing to their ideal electrostatic control (due to the ultra-thin ~1 nm body) and simultaneously high carrier transport, carbon nanotube FETs (CNFETs, Fig. 4.1) are projected to provide an order of magnitude improvement in energy-delay product (EDP, a metric of energy efficiency) in comparison to today's silicon complementary metal-oxide-semiconductor (CMOS) technology [13]. Moreover, CNFETs are a rapidly maturing technology, with experimental demonstrations ranging from

[3] Ionizing radiation in deep space comprises of heavy ions and cosmic rays (*i.e.* high-energy protons, electrons and atomic nuclei). ~ 99.9% of the ionizing radiation is shielded by Earth's magnetic field. The energy of the ~ 0.1 % that passes through the magnetic field is significantly attenuated by the Earth's atmosphere which provides additional protection [108], [109].

[4] The memory wall refers to limited physical interconnects and therefore data bandwidth for transmitting data between heterogeneous parts of a chip (*e.g.*, between off-chip memory and compute). In space, the energy and time required to transmit a bit of information is many orders of magnitude more than that of accessing a bit of information from off-chip DRAM (>$1x10^4$× energy and >$1x10^9$× time, see Supplemental Information)

digital logic gates [16] – [20], to complex analog and mixed-signal circuits [21], [22]. to complete large-scale digital systems [14], [23], [25] - [32], [71], [101], [102]. However, although recent advances in CNFET technology have been significant, only limited studies on their radiation tolerance have been performed [40] – [45]. Moreover, these works do not study realistic (*e.g.*, solid-state and VLSI-compatible) CNFET devices for next-generation electronic systems, and thus do not fully represent the potential benefits of a future CNFET radiation-tolerant technology (see Supplemental Information for a full discussion on prior works).

Here we present the first comprehensive study and optimization of CNFET device geometries for radiation-tolerance. Through this detailed analysis, we experimentally demonstrate that while CNTs themselves offer some material-level intrinsic radiation-tolerance benefit, a robust CNFET technology requires additional engineering to exploit unique device geometries enabled by CNT-specific fabrication. Specifically, we elucidate the following key sources of CNFET radiation-tolerance (illustrated in Fig. 4.1):

1. *Extrinsic* benefits: CNFETs can be fabricated at low-temperature (<400 °C), which naturally enable unique device geometries that can be engineered to realize radiation-tolerance to total-ionizing dose (TID) effects. TID effects refer to cumulative long-term ionizing damage; as illustrated in Fig. 4.1, incident radiation strikes can generate trapped holes (h+) within dielectrics surrounding the channel (such as within field oxides or the buried-oxide layer (BOX) in silicon-on-insulator (SOI) devices). The accumulation of trapped h+ causes inadvertent shifts in threshold voltages, resulting in increased leakage current for NMOS devices, decreased leakage current for PMOS devices, and eventual incorrect logic functionality due to noise margin violations. Here we show that while conventional top-gate geometries (metal gate fabricated after and above the channel) have typical TID tolerance of <1 Mrad(Si), bottom-gate geometries (metal gate fabricated before and beneath the channel) can achieve TID tolerance of ~ 2 Mrad(Si), and dual top- and bottom-gate CNFETs can achieve extreme TID tolerance of >10 Mrad(Si). This record CNFET TID tolerance is due to the metal

gates surrounding and extending across the entire length of the channel, providing complete electrostatic shielding from trapped h+[5].

2. *Intrinsic* benefits: In addition to the extrinsic benefit described above, the material properties of CNTs themselves provide intrinsic radiation-tolerance for transient upsets (such as glitches in logic or memory cells). As illustrated in Fig. 4.1a, transient upsets can occur when ionizing radiation strikes the semiconducting channel in a device. The energy imparted from the ionizing strike results in large electron (e-) and h+ generation within the semiconductor. Within certain regions of the semiconductor (*e.g.*, regions with electric fields such as depletion regions, referred to as the "collection volume" [111]), the resulting charge disturbance creates transient current fluctuations that can cause transient upsets (Fig. 4.1). The probability of a transient upset is therefore proportional to semiconductor volume within a device – the larger the collection volume, the higher the chance an ionizing strike will generate a large enough charge disturbance to cause a glitch in logic or a memory cell. As illustrated in Fig. 4.1, the collection volume of a CNFET is over an order of magnitude reduced versus a typical silicon FET owing to CNTs' ultra-thin body (~1 nm thin CNT vs. multi-nanometer thick SOI) and their simultaneously reduced cross-section (most of the CNFET channel area is empty: <10% of the channel cross-section is covered by CNTs[6]). To gather preliminary data on CNFET's transient upset tolerance benefit (due to their reduced collection volume), we perform the first transient upset testing on CNFET circuits (CMOS CNFET-based 6 transistor (6T) static random-access memory (SRAM)) *via* x-ray prompt dose testing, and experimentally demonstrate a threshold dose rate of 1.3×10^{10} rad(Si)/s.

[5] A TID tolerance of > 10 Mrad(Si) is the highest reported in literature for solid-state CNFETs (*i.e.*, excluding liquid/gel-based non-solid state devices that use CNTs as a channel material, which are not applicable to realizing integrated circuits, ICs).

[6] For optimal EDP, maximum CNT density is ~200-250 CNTs/um, while best experimental CNFETs achieve ~100 CNTs/um. At 100 CNTs/um, nominal CNT spacing is 10 nm, resulting in only ~10% of the channel area comprising CNTs, the other ~90% of the channel is empty. In contrast, 100% of the channel in a typical silicon FET is semiconducting channel.

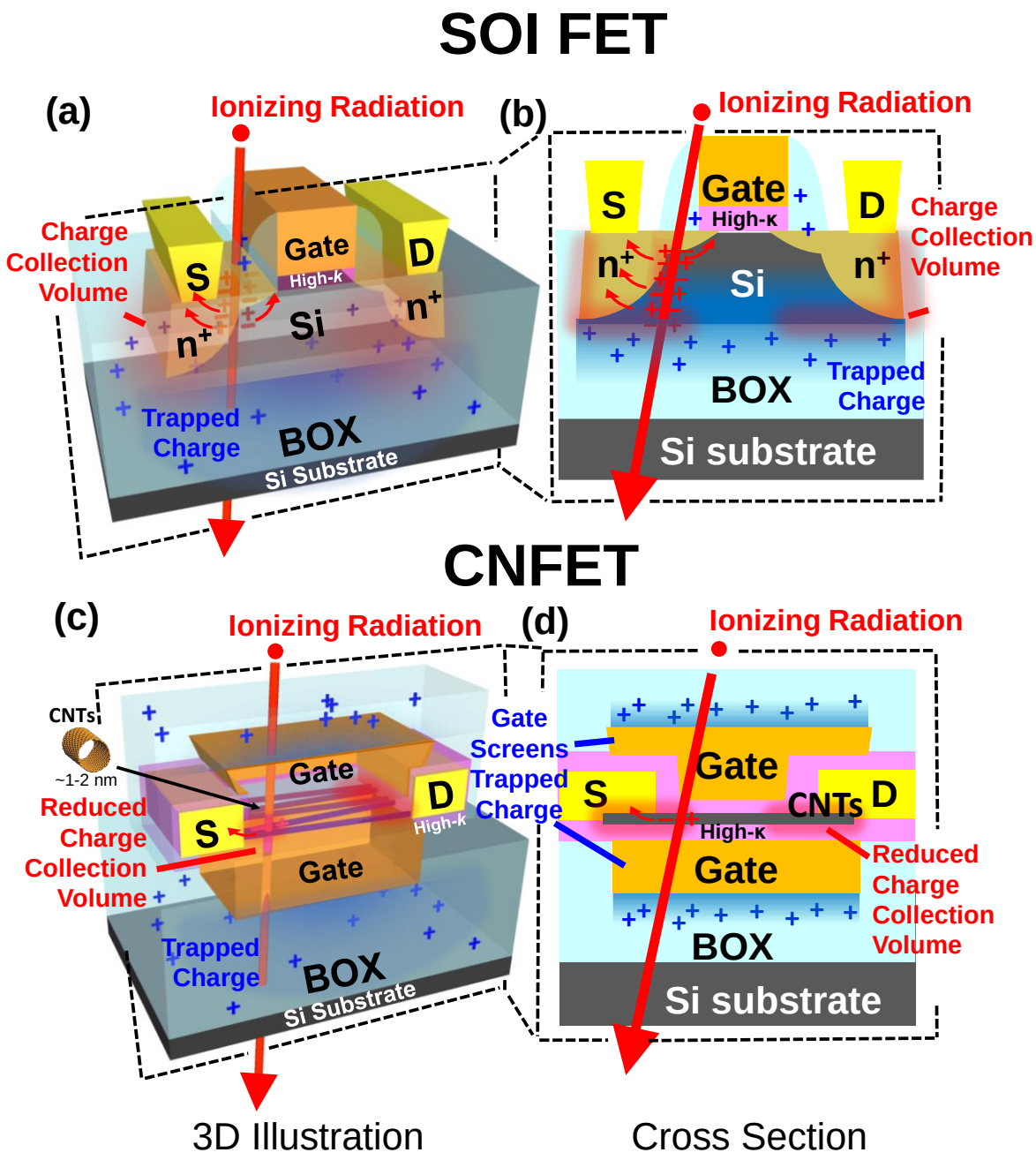

Figure 4.1. 3D illustration and cross section of a silicon-on-insulator (SOI) FET (a,b) and a dual-gate CNFET (c,d). The electrons (e-) and holes (h+) generated in the semiconductor from the incident ionizing radiation strike are highlighted in red, with red arrows indicating how the charges are swept by the local electric fields near the depletion region. Such charge collection near the depletion regions leads to transient current fluctuations that can cause transient upsets if sufficiently large. CNFETs provide intrinsic radiation-tolerance against transient upsets owing to highly-scaled collection volume. This collection volume reduction is attributed to both the channel's reduced cross-section (< 10% CNT coverage of the channel, as shown in (c)) and CNTs' ultra-thin body (~ 1 nm, as shown in (d)). The trapped h+ charges responsible for

TID effects (*i.e.* shifts in V_T, increased leakage energy and incorrect logic functionality) are highlighted in dark blue. It is important to note that trapped h+ charges are observed in oxides with higher e- mobility than h+ mobility, which is the instance depicted here. Given that CNFETs can be fabricated on arbitrary substrates, the BOX material (and its corresponding e- and h+ mobilities) determine if trapped h+ charges or e- charges accumulate. Dual-gate CNFETs, a device geometry naturally enabled by CNFETs' low temperature processing, provides protection through electrostatic shielding against the trapped h+. (d) The bottom and top metal gates electrostatically shield the semiconducting channel and the Schottky contacts from the trapped charges generated in the BOX and the surrounding oxides.

Taken together, this work demonstrates the promise of a future CNFET radiation-tolerant technology, with TID tolerance and prompt dose thresholds competitive with commercial radiation-hardened silicon technology. By performing the first comprehensive characterization of multiple variants of CNFET device geometries, we elucidate the sources of these benefits, providing lessons and insights that can be applied to a wide-range of emerging technologies.

4.2 Results and Discussion

4.2.1 Extrinsic CNFET Benefits

As described above, CNFETs can be fabricated at low-temperature (<400 ℃), which naturally enables unique device geometries that can be engineered to realize a radiation-tolerant technology. Fig. 4.2 shows the schematics of the diverse range of CNFET geometries we fabricate and test: global bottom-gate (the entire wafer substrate acts as a global bottom gate for all CNFETs on the wafer), conventional top-gate (the gate is fabricated on top of a pre-formed semiconducting channel), local bottom-gate (the semiconducting channel is layered over a pre-fabricated gate stack), and dual top- and bottom-gate (metal gates are fabricated on top and underneath the entire length of the channel). Importantly, unlike all prior CNFET radiation studies, all CNFET fabrication in this work is wafer-scale (implemented across 150 mm substrates) and silicon CMOS compatible (both in terms of materials and processing, see Methods for details). A scanning electronic microscopy (SEM) image of a typical bottom-gate CNFET is shown in Fig. 4.2e, where CNTs bridge the source and drain metal terminals.

TID testing was conducted at Kirtland Air Force Base (AFB), a United States Air Force base located in

Albuquerque, New Mexico, USA. Two ionizing radiation sources were used: (1) ^{60}Co γ-ray source for TID tests from 0 Krad(Si) to 800 Krad(Si) (Fig. 4.2i), and (2) Low Energy X-ray Radiation (LEXR) source for TID tests up to 10 Mrad(Si) (Fig. 4.2j)[7]. Fig. 4.2e - Fig. 4.2h shows a typical CNFET chip containing an array of CNFETs for TID characterization. To initially explore the impact of CNFET device geometry on TID response, we expose arrays of CNFETs fabricated with all of the geometries described above to the ^{60}Co source (dose rate = 56 rad(Si)/s) for TID ranging from 100 Krad(Si) up to 800 Krad(Si). For worst-case analysis, we bias the CNFETs with $V_{GS} = -V_{DD}$ (- 1.8 V) and $V_{DS} = 0$ V throughout the irradiation (the gate bias drives the trapped h^+ charges towards the channel, resulting in worst-case threshold voltage shifts (V_T shifts) [112]). Immediately after irradiation, *I-V* characteristics (I_D vs. V_{GS}) of the irradiated CNFETs are measured. The same CNFET arrays are then subjected to progressively higher TID and subsequently re-measured. To minimize inter-sample radiation variability across CNFET chips, all samples were irradiated simultaneously in the same chamber from the same source.

[7] While ^{60}Co is a conventional ionizing radiation source for TID tests, LEXR is capable of delivering much higher doses in shorter time intervals, thus enabling TID testing >10Mrad. Kirkland AFB has previously demonstrated device response to LEXR correlates strongly with device response to ^{60}Co for all x-ray energies [113]. In addition, we perform additional TID testing to validate LEXR extrapolation above ^{60}Co: refer to supplementary information to see continuity of the $|V_T$ shift| as the TID source changes from ^{60}Co to LEXR for CNFETs.

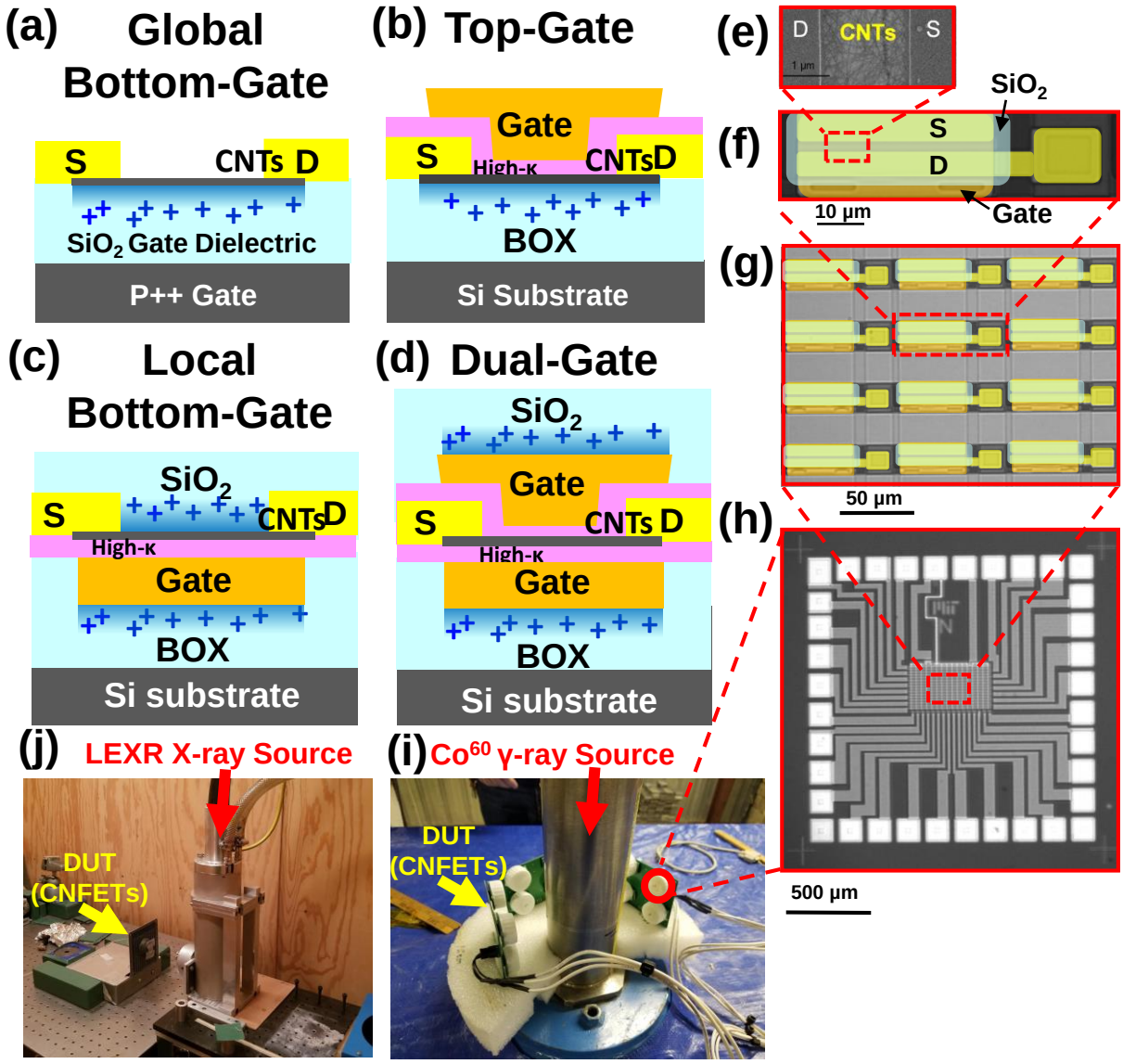

Figure 4.2. TID testing for characterizing CNFET radiation-tolerance. (a) Global bottom-gate (with thick ~ 200 nm thermal SiO_2 gate dielectric) fabricated on highly doped P^{++} silicon, and (b) top-gate, (c) local bottom-gate, (d) dual-gates fabricated on ~1 μm thermal SiO_2. CNTs are solution-deposited at room temperature, CNTs outside the active region (*e.g.*, channel) of the CNFET are removed through oxygen-plasma etching. The high-*k* gate dielectric is deposited through atomic-layer deposition (ALD). The bottom-gate and dual-gate geometries are passivated with 100 nm SiO_2. (e-h) Scanning-electron microscopy (SEM) images of typical dual-gate CNFET array used in TID testing. An identical array configuration is used for TID testing the other device geometries. SEM images of (e) CNTs bridging the source and drain metals, (f) the dual gate CNFET, (g) subsection of the array (256 CNFETs), and the (h) full die with the input/output pads placed around the periphery. TID testing facilities in Kirtland Air Force Base: (i) ^{60}Co γ-ray source for doses ranging from 0 Krad(Si) to 800 Krad(Si), and (j) LEXR x-ray source for doses extending to 10 Mrad(Si).

Typical *I-V* characteristics of the four device geometries (global bottom-gate, top-gate, local bottom-gate, and dual-gate) are shown in Fig. 4.3a – Fig. 4.3d. To characterize TID damage, the $|V_T$ shift| is extracted from the *I-V* characteristic from 256 CNFETs per sample. Fig. 4.3e summarizes the mean $|V_T$ shift| and the 95 % confidence intervals for top-gate, local bottom-gate, and dual-gate CNFET arrays for TID of 100 Krad(Si) up to 800 Krad(Si) (refer to Appendix 1.4 in the Supplemental Information for a typical V_T distribution across all 256 CNFETs within a sample, illustrating the high reproducibility and reliability of the CNFETs and their response to irradiation). As illustrated in Fig. 4.3a, the TID damage is highly dependent on CNFET geometry. For instance, global bottom-gate CNFETs exhibit significant sensitivity to radiation damage, with TID of even 100 Krad(Si) resulting in severe device damage (I_{OFF} increases by over an order of magnitude, and an accurate V_T is unable to be extracted due to substantial distortion in the *I-V* characteristic). Such significant radiation damage is due to the thick SiO_2 (~ 200 nm) gate dielectric which stores the trapped h^+ charges directly underneath the CNT channel and contacts[8].

The TID response of the global bottom-gate CNFETs demonstrate a critical point: that CNTs do not provide inherent protection against TID effects and therefore require additional device geometry engineering. For instance, Fig. 4.3b illustrates that modifying CNFET geometry to a conventional top-gate geometry offers substantially improved robustness to TID effects due to the top gate metal electrostatically shielding the trapped h+ above the channel. Despite the improvement, top-gate CNFETs still suffer from a significant $|V_T$ shift| at 800 Krad(Si) TID (~ 600 mV) because of the lack of electrostatic shielding underneath and next to the source/drain junctions. Moreover, as the source and drain junctions (*i.e.*, the locations of the Schottky barriers from the metal contacts to CNT channel) are the most critical regions of the CNFET (as they are Schottky-barrier FETs [114]), electrostatically-shielding these regions are key for protecting against TID effects. To provide shielding in these regions of the CNFETs, Fig. 4.3c shows the TID testing results for local bottom-gates CNFETs. Unlike top-gates, the metal bottom gate is on a different physical plane as the

[8] Similarly, in modern SOI CMOS devices (*i.e.* with thin gate dielectrics) the trapped h+ primarily responsible for device characteristic shifts are also generated in the BOX underneath the channel and source/drain contacts [115].

source/drain contacts, allowing the gate to extend under the entire region channel, including the Schottky contacts. Due to additional shielding, such geometries provide further TID protection, with a $|V_T \text{ shift}|$ of only ~ 80 mV at 800 Krad(Si).

Although local bottom-gates provide protection from trapped h+ underneath the channel, they are still susceptible to trapped h+ generated above the channel. Therefore, for complete electrostatic shielding, we combine top- and bottom-gate geometries to form dual-gate CNFETs. Because of such complete shielding, our dual-gate CNFETs exhibit extreme TID tolerance: with $|V_T \text{ shift}|$ of ~ 13 mV at 800 Krad(Si) (~ 50× less than the $|V_T \text{ shift}|$ in top-gate CNFETs at the same dose). Importantly, such bottom-gate and dual-gate geometries are naturally enabled by the low-temperature CNFET fabrication whereby CNTs are deposited *via* a room-temperature solution-based deposition and all subsequent CNFET processing is <400°C (see Methods for CNFET fabrication process flow). In contrast, these bottom-gate and dual-gate geometries are challenging to realize with conventional silicon CMOS as the >1000 °C processing steps for silicon channel formation (*e.g.* dopant activation, annealing) would damage or destroy the pre-fabricated metal gate-stack underneath.

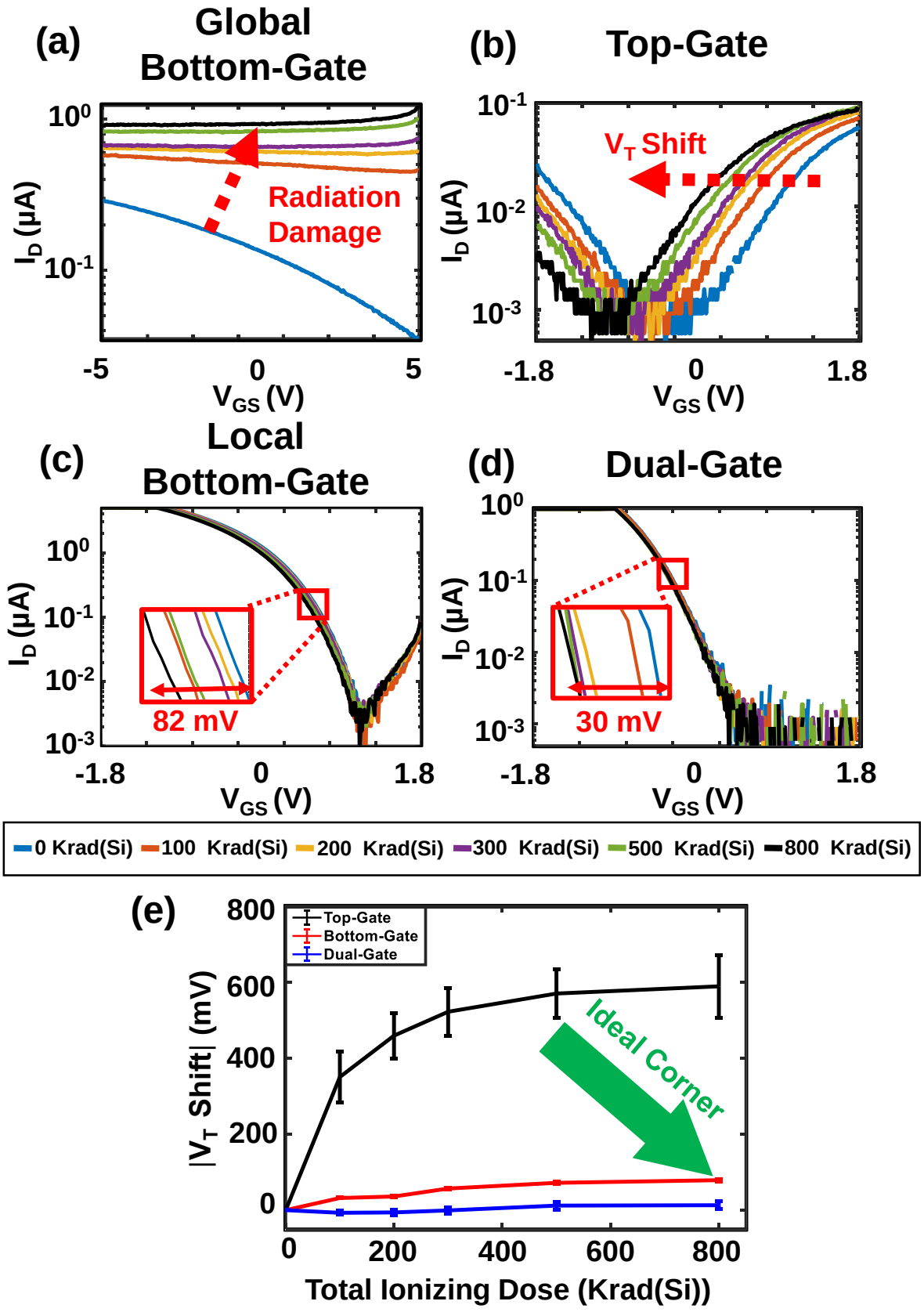
(a)
Global
Bottom-Gate
Radiation
Damage
I_D (μA)
V_{GS} (V)
(b)
Top-Gate
V_T Shift
(c)
Local
Bottom-Gate
82 mV
(d)
Dual-Gate
30 mV
0 Krad(Si)
100 Krad(Si)
200 Krad(Si)
300 Krad(Si)
500 Krad(Si)
800 Krad(Si)
(e)
Top-Gate
Bottom-Gate
Dual-Gate
Ideal Corner
$|V_T$ Shift| (mV)
Total Ionizing Dose (Krad(Si))

Figure 4.3. CNFET TID testing with γ-ray irradiation from ^{60}Co source. Typical *I-V* characteristic (I_D vs. V_{GS}) of (a) global bottom-gate, (b) top-gate, (c) local bottom-gate, and (d) dual-gate CNFETs before γ-ray irradiation (0 Krad(Si)) and after progressively higher γ-ray doses (up to 800 Krad(Si)). Channel length and width are 50 μm and 3 μm for all CNFET device geometries. The global bottom-gates exhibit the largest radiation damage with even 100 Krad(Si) resulting in I_{OFF} increasing by over an order of magnitude. Insets in (c) and (d) highlight the $|V_{GS}$ shift| for a bottom-gate and dual-gate CNFET (82 mV and 30 mV at 0.1 μA, respectively). (e) Mean $|V_T$ shift| versus TID summary plot extracted from the *I-V* characteristics of top gate, bottom-gate, and dual-gate CNFETs (see Appendix 1.4 for a typical V_T distribution). Error bars correspond to 95% confidence intervals; sample size for each CNFET geometry is 256 CNFETs.

To further explore the extent of TID tolerance, we subject the most promising CNFET geometries (local bottom-gate and dual-gate CNFETs, the two device geometries with greatest robustness to TID effects) up to 10 Mrad(Si) TID *via* LEXR (refer to Supplementary Information to see the close continuity of the $|V_T$ shift| as the TID source changes from ^{60}Co to LEXR for CNFETs, validating the LEXR TID testing). Fig. 4.4 shows their respective mean $|V_T$ shifts|. Similar to the testing with the ^{60}Co source, for worst-case analysis we bias the CNFETs with $V_{GS} = -V_{DD}$ (-1.8 V) and $V_{DS} = 0$ V. At the record-high CNFET TID dose of 10 Mrad(Si), the local bottom-gate and dual-gate CNFETs $|V_T$ shift| ~440 mV and ~340 mV, respectively. To further optimize and demonstrate the limit of CNFET TID robustness, we repeat these measurements with a thinned high-*k* gate dielectric gate stack. Because thinning the gate dielectric reduces the number of trapped h+ charges and increases the oxide capacitance, we observe improved TID performance (*i.e.* reduced $|V_T$ shifts|) [116]. At 10 Mrad(Si), thinning down the gate dielectric from an EOT of ~7 nm to ~2 nm results in an average $|V_T$ shift| of ~80mV for the local bottom-gate CNFETs, and an average $|V_T$ shift| of ~50mV for the dual-gate CNFETs (<5% and <3% of V_{DD}, respectively). In addition to exhibiting record CNFET TID tolerance, such high TID dose tolerance is competitive with even commercial silicon-based radiation-hardened-by-process metrics.

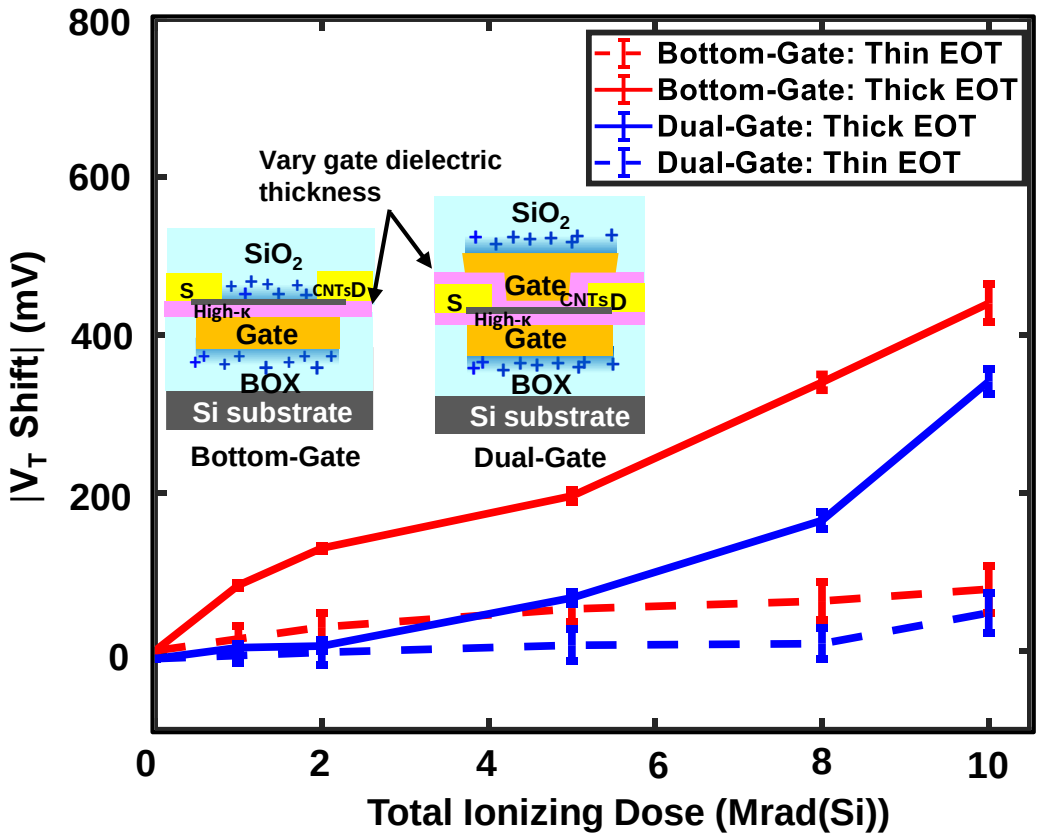

Figure 4.4. Mean $|V_T$ shift| of 256 local bottom-gate (red) and 256 dual-gate (blue) CNFETs up to 10 Mrad(Si) x-ray irradiation from LEXR source. Error bars correspond to 95% confidence intervals. Extended TID testing was done on local bottom-gate and dual-gate CNFETs with EOT of 7 nm ("thick", solid) and ~2 nm ("thin", dashed) gate dielectric thicknesses. Thinning down the high-*k* dielectric from an EOT of ~7 nm (thick) to ~2 nm (thin) resulted in ~ 6× and ~ 7× reduction in $|V_T$ shift| (at 10 Mrad(Si)) for the local bottom-gate and dual-gate CNFETs, respectively.

4.2.2 Intrinsic CNFET Benefits

In addition to TID tolerance, electronic systems must be tolerant to another category of radiation effects: transient upsets. Such transient upsets can result in catastrophic system failure, either by causing incorrect logic functionality (*e.g.*, if an instruction bit flips and the program jumps to an incorrect instruction address [117]) or corrupting memory. Typically, to determine transient upset tolerance electronic systems are irradiated by heavy ions. However, despite the importance of transient upset tolerance, no prior CNFET radiation studies have performed any type of transient testing. To gather preliminary data for CNFET transient upset tolerance, we explore CNFETs' radiation tolerance against transient upsets for the first time

via x-ray prompt dose testing. To characterize CNFET-based circuits, we perform x-ray prompt dose testing on CNFET CMOS 6T SRAM (a dense SRAM variant typically used for volatile on-chip, high-speed, low-level caches).

We fabricate the CNFET SRAM by leveraging a full CMOS low-temperature (< 400 °C) process flow shown in Fig. 4.5. Importantly, the process flow is silicon CMOS compatible with no additional fine-tuning or post-fabrication customization (see Appendix 1.5 for full details, and references [102] and [110] for further CNFET CMOS SRAM specifications). To achieve an ideal balance between fabrication simplicity and TID robustness we implement the CNFET CMOS SRAM with the local bottom-gate geometry (the local bottom-gate geometry process flow benefits from requiring only 5 lithography layers, while maintaining high TID robustness competitive with commercial silicon-based radiation-hardened by process technology.

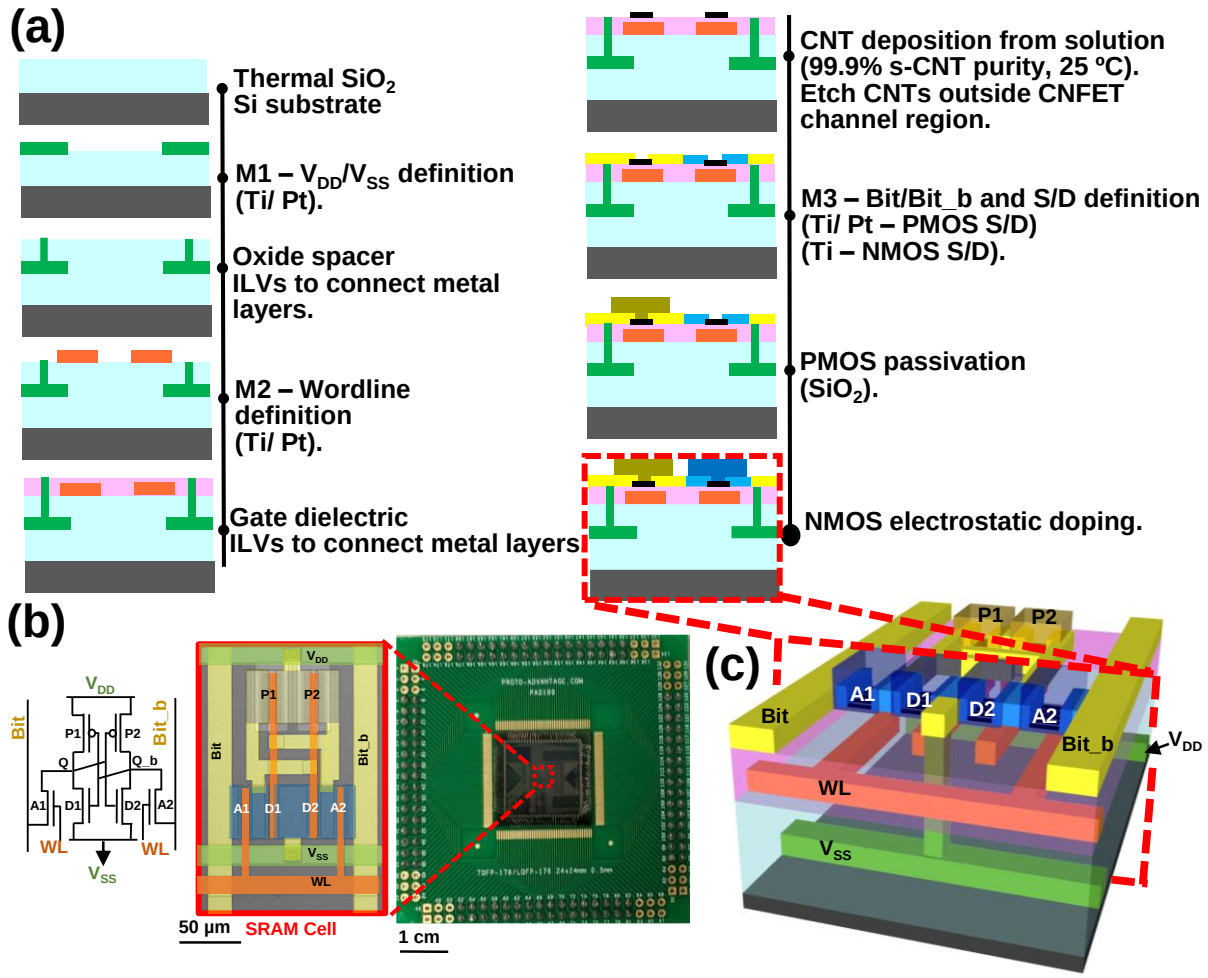

Figure 4.5. (a) Wafer-scale CMOS process flow for CNFET 6T SRAM. The fabrication process leverages a three-metal layer process whereby the metals are defined *via* physical vapor deposition (PVD) and separated by oxide spacers, vertically connected by etch and metal fill for inter-layer *via* (ILV) definition. The high-k dielectric is deposited *via* atomic layer deposition (ALD). CNTs are solution-deposited across the wafer at room temperature followed by oxygen plasma to etch the CNTs outside the active area (*e.g.* channel). The first metal layer (M1) defines the V_{DD} and V_{SS} lines, the second metal layer (M2) defines the WL and the bottom gates of the CNFETs, the third metal layer (M3) defines the bit, bit_b, the PMOS source/drain contacts (Ti/ Pt) as well as the NMOS source/ drain contacts (Ti). To complete the CNFET CMOS SRAM process the PMOS are passivated (100 nm SiO_2), and the NMOS are electrostatically doped (see ref. [83] for details). (b) Circuit schematic and scanning electron microscopy (SEM) images of the CNFET SRAM (false colored according to the cross section in (a)), as well as the packaged CNFET CMOS 6T SRAM which uses conventional wirebonding to access the pads located around the perimeter. (c) 3D illustration of the CNFET CMOS 6T SRAM.

The x-ray prompt dose testing was conducted at Cobham Rad, Colorado. The x-ray flash generator, the mounted CNFET SRAM, and the SRAM read-out peripherals are shown in Fig. 4.6a – Fig. 4.6c. To ensure the CNFET SRAM chips were the only component irradiated by the x-ray pulses (thereby isolating transient

errors to the CNFET SRAM itself), the CNFET SRAM was fabricated on-chip and exposed to the radiation while the peripherals used to write to- and read out from the CNFET SRAM were off-chip and protected from any radiation exposure. To precisely determine the prompt dose rate for each test, a calibrated p-type-insulator-n-type stack (PIN) diode was placed behind the CNFET SRAM and recorded for each test. To perform the x-ray prompt dose testing, we first write the SRAM to store logic value "1" or "0". The SRAM cells are biased to retain their state (*e.g.*, standby mode) for 6 seconds. During standby mode, the SRAM is irradiated with a 20 ns x-ray pulse at a given prompt dose rate. Following irradiation, the state of the SRAM cells is read out and a bit flip is detected if the state of the SRAM cell after irradiation has erroneously flipped to the incorrect value. To prepare for the next x-ray pulse, the same SRAM cells are re-written to store logic values "1" or "0" demonstrating that these upsets are not irreversible. The probability of SRAM cell bit flip vs. prompt dose rate is shown in Fig. 4.6. As is typical, there is a clear dose rate threshold which when surpassed results in an exponential increase in bit flips: ~1.3×10^{10} rad(Si)/s. The bit flips measured before the dose rate threshold is noise, and is attributed to the periphery circuitry located off-chip. This is confirmed by the same constant percentage of bit flips occurring at a prompt dose rate of even 0 rad(Si)/s (*i.e.*, when the SRAM is not irradiated). Moreover, to demonstrate reproducibility and robustness of the testing, the prompt dose testing is performed across three different CNFET CMOS SRAM dies, all yielding similar dose rate thresholds. Such values are competitive with silicon radiation-tolerant by-design dose rate threshold metrics (*e.g.*, silicon-based SRAM that are specifically optimized for radiation tolerance both through processing as well as through specialized circuit design)[9].

[9] Though we did not perform specific testing for latch-up immunity, no latch-up was ever detected during the prompt dose testing. This is as-expected, as the CNFETs benefit from complete isolation (*e.g.*, the semiconducting channel of the transistor, the CNTs, are only within the channel of the CNTs and are etched and removed everywhere else on the wafer. Thus, all CNFETs are completely isolated from one-another. In contrast to complex isolation methodologies with silicon and other bulk technologies, CNFETs achieve isolation through a simply oxygen-plasma etch).

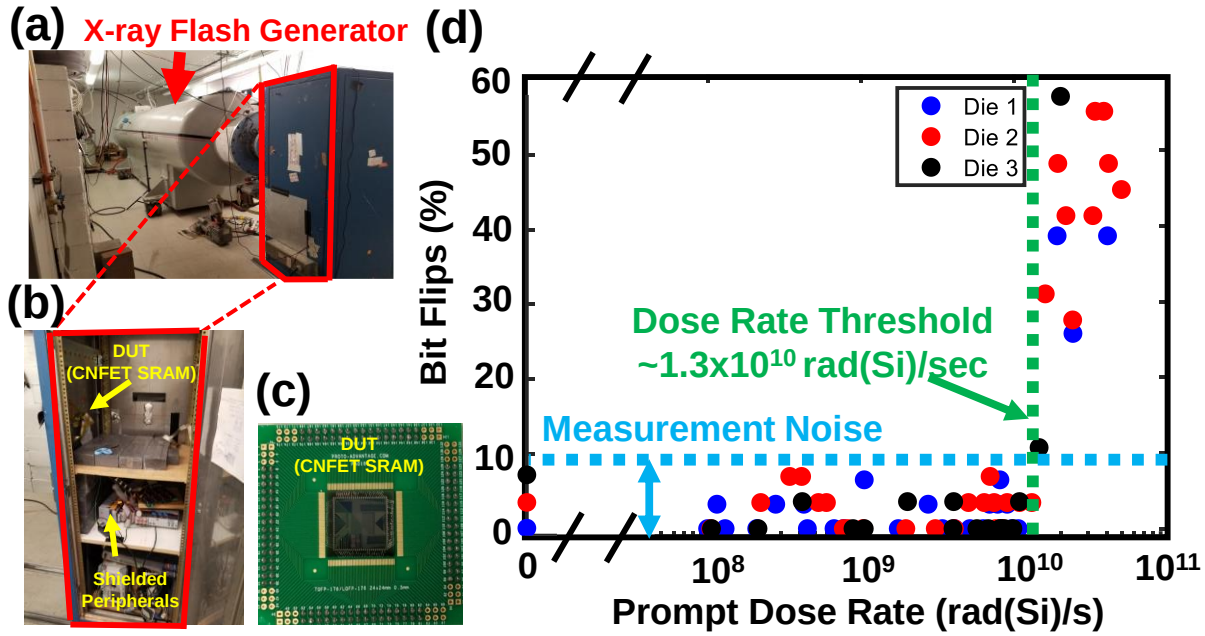

Figure 4.6. CNFET transient upset characterization *via* x-ray prompt dose testing of CNFET CMOS 6T SRAM. (a-c) X-ray prompt dose testing is performed at Cobham Rad, Colorado. (a) shows the x-ray flash generator, (b) shows the off-chip peripherals used to write to- and read out from the CNFET SRAM, and (c) shows the mounted CNFET SRAM. Bit flip percentages of three separate dies were measured from 0 rad(Si)/s to $5x10^{10}$ rad(Si)/s. The CNFET SRAM cells were first written to with bit value 1, irradiated with a 20 ns x-ray pulse while on standby mode (WL = V_{SS}, effectively turning off the access CNFETs "A1" and "A2", electrically isolating the cell from the bit and bit_b lines), and then read-out to determine the number of SRAM bits flipped. The dose rate threshold is ~$1.3x10^{10}$ rad(Si)/s. The transient upsets observed prior to the dose rate threshold are due to noise and the periphery circuitry being located off-chip (to isolate the radiation effects to the SRAM arrays itself), confirmed by the nonzero bit flips at 0 rad(Si)/s.

4.3 Conclusion

We demonstrate that CNFETs are a promising technology for next-generation space applications by leveraging extrinsic CNFET benefits owing to unique device geometries enabled by their low-temperature fabrication, and intrinsic CNFET benefits owing to CNTs' inherent material properties. We thoroughly analyze and compare the TID tolerance of various CNFET geometries. The local bottom-gate and dual-gate CNFETs, both enabled by the low-temperature fabrication, provide significant TID tolerance (record high CNFET TID tolerance of >10 Mrad). Moreover, the inherent material-level benefits of CNTs (ultra-thin body and reduced cross section in the channel) provide CNFET-based circuits protection against transient upsets. To demonstrate transient upset tolerance, we perform the first transient upset testing of CNFET

circuits (CNFET CMOS 6T SRAM) *via* x-ray prompt dose testing, and experimentally demonstrate a threshold dose rate of $1.3x10^{10}$ rad(Si)/s. This work showcases CNFETs as a promising radiation-tolerant technology for next-generation space applications, and by elucidating the source of their benefits we provide lessons that can be applied to a wide-range of emerging nanotechnologies as well.

Chapter 5: Ongoing Work: Electrostatically Doped Transistors at Cryogenic Temperatures

5.1 Introduction

To enable future space mission, electronics driving these missions must also withstand extreme temperature swings (hardware for space exploration missions could experience cryogenic temperatures to >100 ^{o}C [118] – [120]. In this ongoing work, we focus on electronic operation at cryogenic temperatures although electronic operation at high temperatures is also an active area of research [121] – [123]. To maintain operating temperature for electronics for cold environments in deep space, critical for mission success, radioisotope heating units (RHUs) can be used[10]. Despite the benefit of RHUs, they are expensive, require containment structures, and introduce a substantial weight penalty [124]. Therefore, electronics that operate at cryogenic temperatures promise a potential reduction in total system size and weight by minimizing the need for RHUs and associated structures.

Conventional silicon-based MOSFETs exhibit device-level benefits with decreasing temperatures such as: improved subthreshold slope (S.S.), lower off current (I_{OFF}), high mobility (μ_{eff}) via reduced lattice scattering, higher transconductance (g_m) due to improved μ_{eff} , and higher saturation drive current ($I_{D,SAT}$) [125] – [126]. However, despite these benefits, significant challenges still exist compromising the reliability of silicon-based electronic systems at cryogenic temperature operation. For instance, dopant freeze-out significantly increases the resistance of the semiconducting silicon channel [127]. Therefore, to ensure constant system performance the system V_{DD} must also increase. This can result in increasing total power consumption and power dissipation, which, coupled with worsened self-heating effects at cryogenic temperatures [128], could result in catastrophic temperature gradients across the chip. Moreover, dopant freeze-out in silicon-based FETs contribute to kink phenomena at sufficiently high V_{DS} in the saturation

[10] There are electronics that do not benefit from RHU temperature regulation resulting in extreme temperatures swings from day to night.

region [129]. At sufficiently low cryogenic temperatures, an accumulation of charges (h^+ in silicon) form in the body due to the high resistance in the channel (a result of dopant freeze-out). To minimize the impact of kink effects, the silicon body is thinned to promote h^+ being swept to the source without accumulating in the body.

Electrostatic doped Schottky barrier FETs, like NMOS CNFETs (Fig 5.1), promise potential benefits at cryogenic temperatures owing to the mechanism and physics to set their threshold voltages and polarity. Specifically, to dope a CNFET from PMOS to NMOS, we leverage a combined doping strategy that relies on (1) fixed charges in a nonstoichiometric dopant oxide (NDO) to electrostatically dope the CNTs, and (2) work-function engineering by selecting different metals as the CNFET source and drain metal contacts [83]. The absence of dopant impurities removes the possibility of dopant freeze, and therefore, inadvertent increases in channel resistance. Furthermore, owing to the ultra-thin body of CNTs, the impact of kink effects is potentially reduced as accumulated h^+ are promptly away swept to the source and do not accumulate in the body.

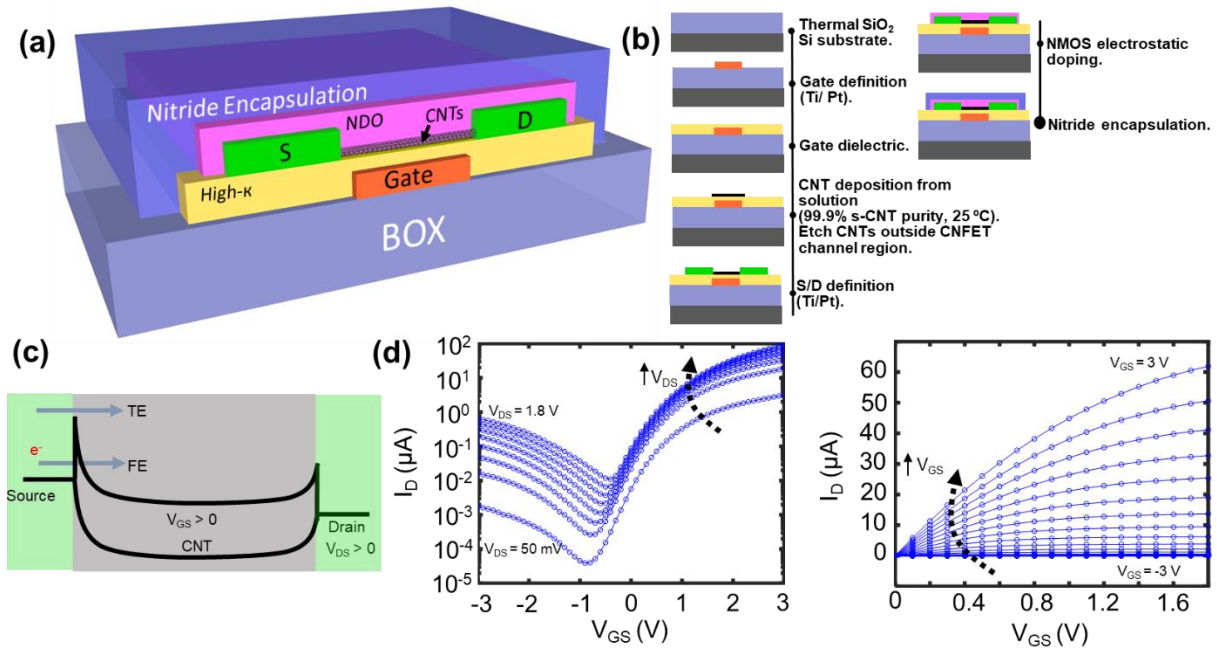

Figure 5.1. (a) 3D illustration of a local back-gate, nitride encapsulated, electrostatically doped NMOS

CNFET. (b) Wafer-scale process flow for NMOS CNFETs. (c) CNFET energy band diagram highlighting field-emission (FE) and thermionic emission (TE) modes of electron (e^-) transport across the Schottky barrier. (d) Typical experimental room temperature and pressure I_D-V_{GS} and I_D-V_{DS} plots for local back-gate, nitride encapsulated NMOS CNFETs (channel length and width are 3 µm and 30 µm, respectively).

5.2 Experimental Results

To perform preliminary testing on electrostatically doped CNFETs and verify their stability at cryogenic temperatures, we measure CNFETs using a Lakeshore manual probe station and maintain stable cryogenic temperatures via liquid helium (Fig. 5.2). To ensure good thermal contact, the CNFET dies are mounted and secured on the probe station stage with Apiezon N grease [130] and copper tape. The chamber is then pumped to high vacuum (<10^{-6} Torr), and baseline $I_D - V_{GS}$ characteristics are measured at room temperature (~300 K) from 50 mV V_{DS} to 1.8 V V_{DS}. By adjusting the flow of liquid helium and tuning the probe station heater parameters, the chamber temperature is controlled and stabilized to 50 K, 30K and 7 K before subsequent $I_D - V_{GS}$ characteristic measurements of the same CNFETs. Before venting to atmosphere at room temperature, we re-measure and observe nearly identical $I_D - V_{GS}$ characteristics to the baseline. These nearly identical curves demonstrate the resilience of electrostatically doped CNFETs to extreme temperature swings (from 7 K to 300 K) (Fig. 5.2a).

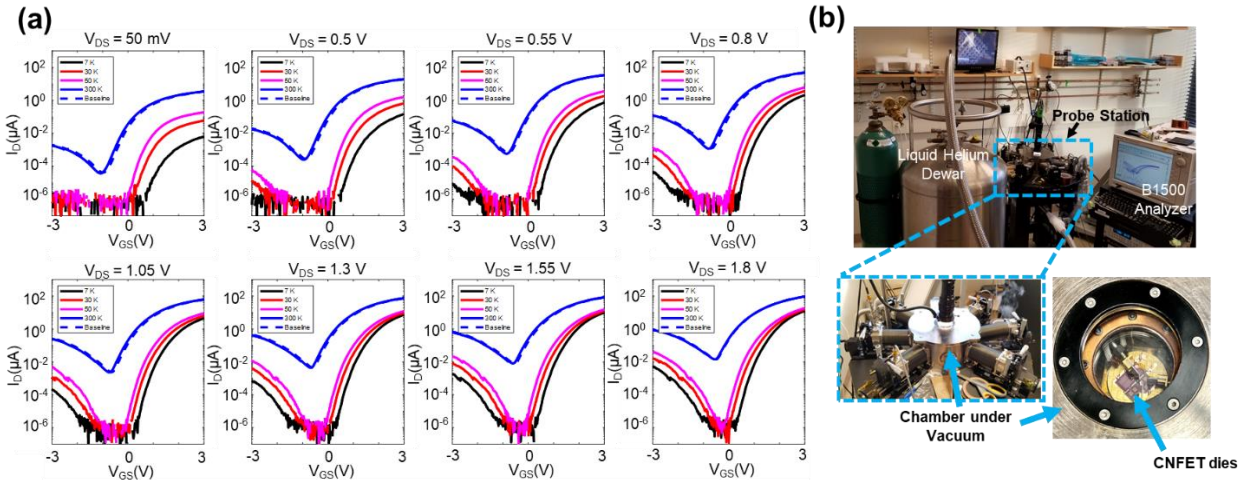

Figure 5.2. (a) $I_D - V_{GS}$ characteristics for a typical NMOS CNFET (channel length and width are 3 µm and 30 µm, respectively) at room temperature (300 K) and cryogenic temperatures (50 K, 30 K and 7 K) from low to high V_{DS} (50 mV to 1.8 V). (b) Cryogenic measurement experimental setup highlighting the liquid helium dewar, Lakeshore manual probe station, B1500 semiconductor parameter analyzer, and chamber under vacuum which houses the CNFETs.

To demonstrate reproducibility, $I_D - V_{GS}$ characteristics of multiple CNFETs (N=24) were measured at 300 K, 50 K, 30 K, and 7 K. A summary of preliminary results highlighting several key device characteristics is shown in Fig. 5.3. We observe a stronger temperature dependence for drive current ($I_{D,\ Vgs\ =\ 1.8V}$) at lower V_{DS} owing to the increasingly dominant thermionic emission (T.E.) contribution to $I_{D,\ Vgs\ =\ 1.8V}$. Conversely, at high $V_{DS,}$ there is a weaker temperature dependence for $I_{D,\ Vgs\ =\ 1.8V}$ because of the larger contribution from tunneling (field emissions, F.E.). A substantial improvement in I_{ON}/I_{OFF} and S.S. is also observed at cryogenic temperature which promises total static power dissipation reduction and improved transitions between off and on states at these lower temperatures.

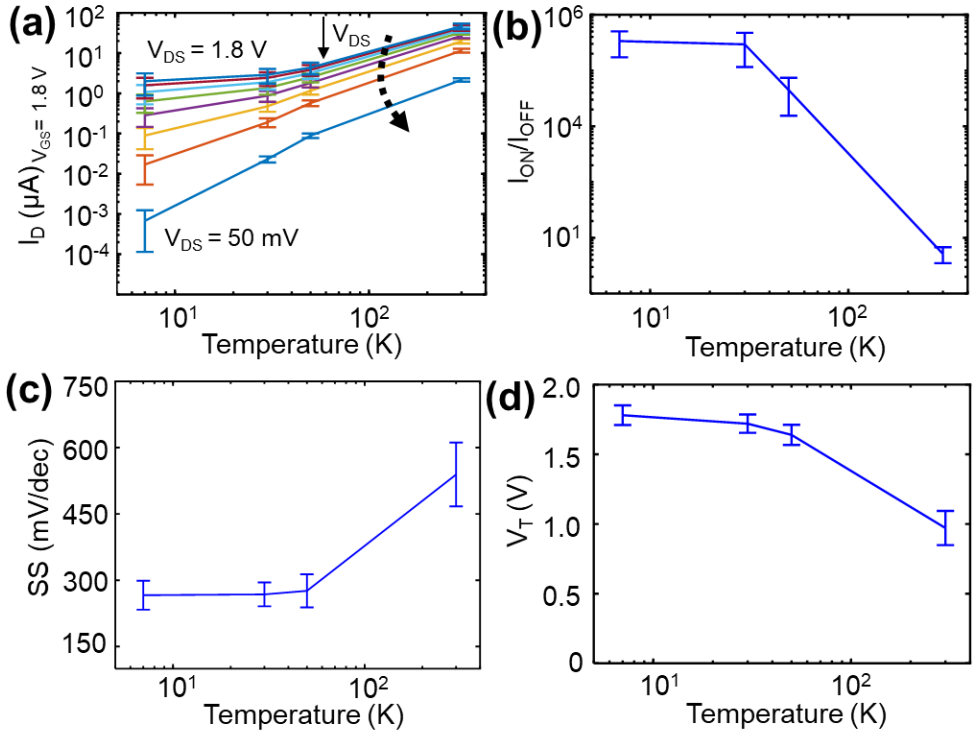

Figure 5.3. (a) Mean I_D (V_{GS} = 1.8 V) extracted from 24 NMOS CNFET $I_D - V_{GS}$ characteristics at room temperature (300 K) and cryogenic temperatures (50 K, 30 K, and 7 K) from low to high V_{DS} (50 mV to 1.8 V). A stronger I_D dependence on temperature demonstrates a decreasing field emission contribution at lower V_{DS} biases (i.e. thermionic emissions dominant at lower V_{DS}).(b) Mean I_{ON}/I_{OFF}, (c) mean subthreshold swing (S.S.), and (d) mean V_T extracted from the same NMOS CNFET $I_D - V_{GS}$ characteristics at high V_{DS} (1.8 V). All error bars correspond to 95% confidence intervals.

5.3 Conclusion

In this ongoing work, we experimentally demonstrate the stability and resilience of CNFETs, and specifically electrostatic doping, at cryogenic temperatures. The $I_D - V_{GS}$ characteristics of multiple CNFETs (N=24) were measured at 300 K, 50 K, 30 K, and 7 K, while also extracting and summarizing key device characteristics. In addition to experimental results, we elucidate the potential benefits of CNFETs at cryogenic temperatures such as no dopant freeze-out due to the absence of dopant impurities (fixed charges in the NDO and work function contact metal engineering set and tune the V_T), and minimal kink effects owing to the ultra-thin body (~ 1 nm) of CNTs.

Chapter 6: Concluding Remarks

Continued silicon scaling is becoming increasingly challenging and yielding diminishing returns [3] – [6], which has sparked the search for beyond-silicon nanotechnologies such as one-dimensional carbon nanotubes (CNTs) or two-dimensional nanomaterials such as transition metal dichalcogenides (TMDs) [7] – [9]. However, relying on just new materials has been insufficient and coordinated advances across the entire computing system stack are required. In this thesis, I combined multiple advances across the stack - leveraging new nanomaterials and new device geometries to realize new circuit and system demonstrations to ultimately strategically engineer electronics for new applications.

As a case study, this thesis focused on CNT-based electronics and the target application of radiation-tolerant electronics for future space missions. CNTs were chosen as they are a leading candidate amongst nanotechnologies for next-generation of electronic systems. CNFETs, owing to their ideal electrostatic control (due to the ultra-thin ~1 nm body) and high carrier transport, CNFETs are projected to provide an order of magnitude improvement in EDP versus today's silicon-based complementary metal-oxide-semiconductor (CMOS) technology [10]. CNFETs can also be fabricated at low processing temperatures (<400°) [11], [12], and therefore naturally enable new system architectures such as monolithic three-dimensional (3D) integration (whereby layers of circuits are fabricated sequentially and directly vertically overlapping one-another over the same starting substrate [12]).

Despite the recent advances in CNFET technology, CNFET-based SRAM arrays have never been demonstrated and only limited studies on CNFET radiation tolerance have been performed [30] - [35]. Prior work has either realized only individual, isolated CNT-based SRAM cells [36], or has relied on processing that is not compatible with silicon CMOS (e.g., relying on air-reactive, ionic, non-solid-state CNT doping processes). Furthermore, previous radiation-tolerant works do not study realistic (e.g., solid-state and VLSI-

compatible) CNFET devices for next-generation electronic systems, and thus do not fully represent the potential benefits of a future CNFET radiation-tolerant technology [37] – [43].

This work showed 1) new 3D FET architectures leveraging the low temperature processing requirements of CNFETs (e.g., <250 ºC): (i) Dual Independent Stacked Channel FET (DISC-FET), which comprises of two FET channels vertically integrated on separate circuit layers separated by a shared gate. (ii) X3D, which enables a wide range of semiconductors – including silicon (Si), III-V, and nanotechnologies such as carbon nanotubes (CNTs) – to be heterogeneously integrated together in monolithic 3D integrated systems. 2) The first SRAM arrays based CNFETs and the first demonstration of CNFET CMOS 10T SRAM cells, capable of operating at highly-scaled voltages down to 300 mV. 3) How CNFETs can be strategically engineered to realize a robust radiation-tolerant technology by leveraging both *extrinsic* CNFET benefits owing to CNFET device geometries enabled by their low-temperature fabrication, as well as *intrinsic* CNFET benefits owing to CNTs' inherent material properties. All in all, this work provides a blueprint on how to build next-generation systems for new applications, where we (1) must elucidate benefits of these new technologies to inform target application selection, and (2) must simultaneously have a deep understanding of the challenges and requirements of the target application before choosing a technology. Beyond this thesis, my hope is that this same methodology of uncovering and leveraging the benefits of a technology to build specialized electronics for new applications can be applied to the ever-expanding range of new material systems and technologies into the future.

Appendix A1: Extended Discussion on Radiation-Tolerant Electronic Systems for Future Space Missions

Appendix A1.1: Energy and Time Comparisons

To illustrate the growing "communication wall" that exists for all deep space missions between spacecrafts and Earth, we compare the energy (E_b) and time (t) to transmit a bit of data back to Earth to the energy and time needed for off-chip DRAM access from compute. E_b is a function of the transmitter power on the spacecraft (P_T) and the transmitted data rate (f_b), while t is a function of the distance between the spacecraft and the Earth (D) and the speed of light (c). It is important to note that we assume that the energy and time needed to move a bit from the on-chip computer to the spacecraft's transmitter is negligible, and therefore ignore them in our calculations. E_b and t are defined as follows [1]:

$$E_b = P_T/f_b \text{……(1)}$$

$$t = D/c \text{…….....(2)}$$

For this approximate analysis, we choose P_T and f_b values for 2020 spacecraft capabilities (f_b = 1.2 Gbps, P_T = 180 W) stationed around Mars (0.6 Astronomical Units (Au) from Earth). [2] Given these values, we approximate E_b and t to be $1.5x10^5$ pJ/bit and $3x10^2$ s, respectively, and the energy-delay product (E_b*t) to be $4.5x10^7$ pJ*s/bit. From our calculations, we project the energy and time to be orders of magnitude more than that of accessing a bit from off-chip DRAM (>$1x10^4$ x more energy, >$1x10^9$x more time, and >$1x10^{14}$ x more in energy-delay product). These values are summarized in the table and figure below:

	Energy per bit (pJ/bit)	**Time (s)**	**Energy-Delay Product (pJ*s/bit)**
Mars (0.6 Au) [2]: f_b= 1.2 Gbps P_T = 180 W	1.5×10^5	$3x10^2$	$4.5x10^7$
Off-chip DRAM [3]	2	$6x10^{-8}$	$1.2x10^{-7}$

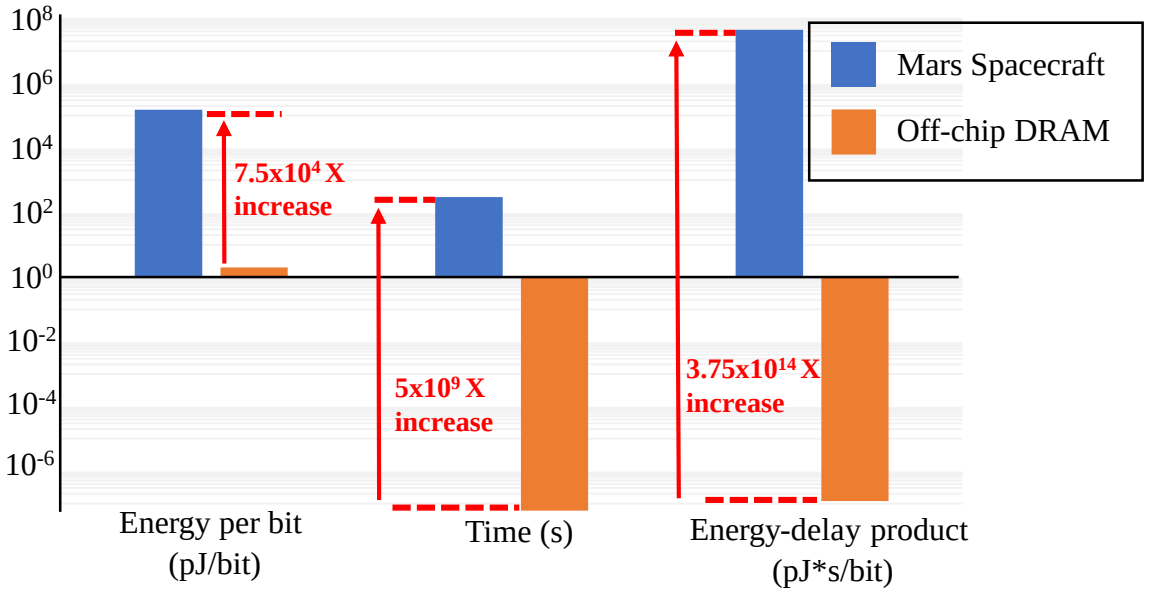

Figure A1.1.1: Bar chart comparing the energy per bit, time, and energy-delay product between transmitting a bit of information from a Mars spacecraft back to Earth versus off-chip DRAM access from compute.

Appendix A1.2: Prior CNFET Radiation Studies

A detailed summary and comparison of prior CNFET radiation work is given in the table below:

Ref.	**Device Geometry**	**Circuits**	**Type of logic**	**Silicon-CMOS Compatible?**	**TID Testing**	**Transient Testing**
This Work	Global Bottom-Gate, Local Bottom-Gate, Top-Gate, Dual-Gate	6T SRAM	CMOS	Yes	10 Mrad(Si)	Dose rate threshold = ~ 1.3 x 10^{10} rad(Si)/s
[4]	Local Bottom-Gate	Inverters	CMOS	No, Non-solid-state materials used (*e.g.* photoresist as PMOS passivation)	2 Mrad	None
[5]	Top-Gate	6T SRAM	CMOS	No, Scandium NMOS source/drain contacts	2.2 Mrad	None
[6]	Global Bottom-Gate	None	only PMOS	Yes	10 Mrad(Si)	None

[7]	Top-Gate	None	only PMOS	No, Non-solid-state materials (*e.g.* $BaTiO_3$/PMMA as gate dielectric)	- 150 Krad	None
[8]	Global Bottom-Gate, Local Bottom-Gate	None	only PMOS	Yes	1 Mrad(Si)	None
[9]	Local Bottom-Gate	Inverters	CMOS	Yes	5 Mrad(Si)	None
[10]	Top Gate	Inverters	Pseudo CMOS (ambipolar CNFETs as PMOS and NMOS)	No, Non-solid-state materials (ion gel film as the gate)	15 Mrad(Si)	None

Appendix A1.3: Methods/Experimental Fabrication Process

All processing steps are wafer-scale, silicon CMOS compatible, and low temperature (< 400°C). Additionally, all process flows consist of a room temperature solution-based CNT deposition whereby the entire 150 mm wafer is submerged in a CNT dispersion with the CNTs already pre-purified to achieve >99.99% semiconducting CNTs (modified IsoSol-S100 from NanoIntegris). Moreover, with the exception of the global bottom-gate CNFETs, the ALD-deposited high-*k* dielectric for all process flows is HfO_2.

Global Bottom-Gate CNFET:

Starting with a highly doped P++ silicon wafer (as the global bottom gate), deposit 200 nm of the thermal SiO_2 gate dielectric. CNTs are then solution-deposited and etched *via* oxygen plasma to define the channel. To complete the fabrication, source/drain metals are defined (Ti/ Pt).

Top-gate CNFET:

We begin with a CNT solution-based deposition on a ~ 1 µm SiO_2 on silicon wafer followed by an oxygen plasma to define the channel. The source/drain metals are then defined *via* PVD (Ti/ Pt). A high-*k* gate dielectric is ALD-deposited (EOT ~ 7 nm) and subsequently RIE-etched to contact the source/drain

metals. To complete the gate stack, the top gate metal is defined (Ti/ Pt).

Local Bottom-Gate CNFET:

The gate stack is first fabricated on ~1 μm SiO_2 on silicon wafer by first defining the bottom mate gate (Ti/ Pt) and then ALD-depositing the high-*k* gate dielectric (EOT ~ 7 nm or ~ 2 nm depending on TID testing performed). RIE etching is performed to access the bottom gate metal contacts. After the gate stack fabrication, CNTs are solution-deposited and oxygen plasma etched to define the channels of the CNFETs. The local bottom-gates are completed by source/drain metal definition (Ti/ Pt) followed by 100 nm of SiO_2 passivation

Dual-Gate CNFET:

Beginning with fabricated local bottom-gate CNFETs (pre-SiO_2 passivation), ALD-deposit a high-*k* gate dielectric (EOT ~ 7 nm or ~ 2 nm to match bottom gate dielectric already deposited). RIE etching of the top gate dielectric is performed to contact the bottom gate and source/drain metals. Similar to the top-gate CNFET, the top gate metal is defined (Ti/ Pt) to complete the dual gate CNFET fabrication.

CNFET CMOS 6T SRAM:

Starting with a 150 mm silicon wafer with ~ 1 μm thermal SiO_2, we define the first metal layer (M1) consisting of the power rails (V_{DD} and V_{SS} lines). Inter-layer dielectric (ILD) layer is then deposited, followed by metal *via* definition. The second metal layer (M2) is deposited for the wordlines (WLs), routing, and the bottom metal gates for the CNFETs. Subsequently, a high-k gate dielectric with an EOT of ~7 nm is ALD-deposited, which is followed by a uniform blanket CNT solution-based deposition across the entire wafer. CNTs that do not define the active area (*e.g.* channel area) are etched away using traditional photolithography and oxygen plasma. The third metal layer (M3) defines PMOS CNFET source/drain contacts as well as metal routing for the bit/bit_b lines (Ti/ Pt). The PMOS CNFETs are completed after they are passivated with 100 nm SiO_2. To finish the NMOS CNFETs, Ti is deposited for the source/drain contacts, and a high-*k* dielectric is ALD-deposited in order to electrostatically dope the CNTs to set the V_T.[40] The final step is etching the electrostatic doping film over the PMOS CNFETs which are protected by SiO_2 passivation. The 150 mm wafer is then diced, and the individual dies are wirebonded

for x-ray prompt dose testing.

Appendix A1.4: Supplemental Data from our Radiation Testing

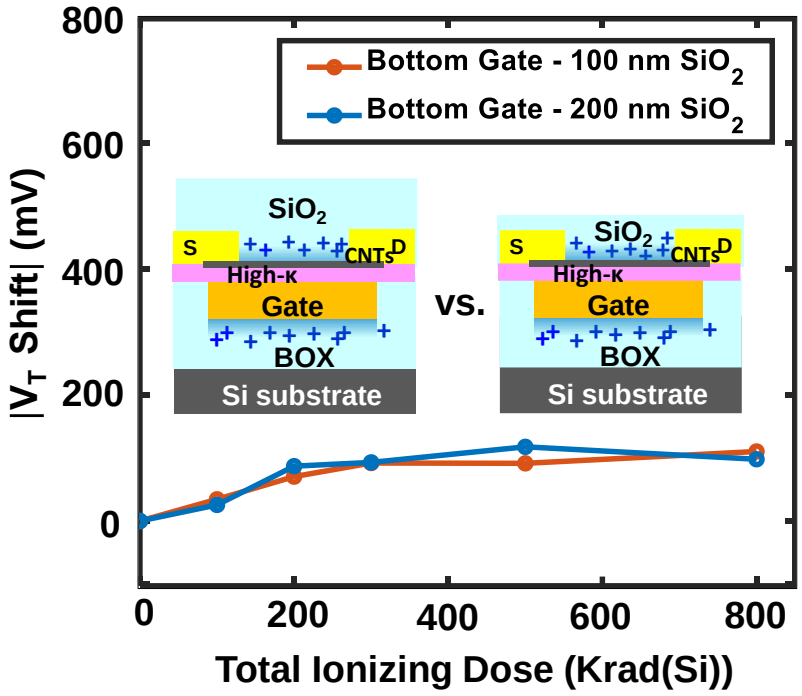

Figure A1.4.1: $|V_T$ shift| *versus* TID (up to 800 Krad(Si) irradiation), for a typical local bottom gate (gate dielectric EOT = ~ 7 nm) CNFET with SiO_2 passivation of 100 nm (orange) and 200 nm (blue). There is negligible difference between the two cases ranging from 0 Krad(Si) to 800 Krad(Si).

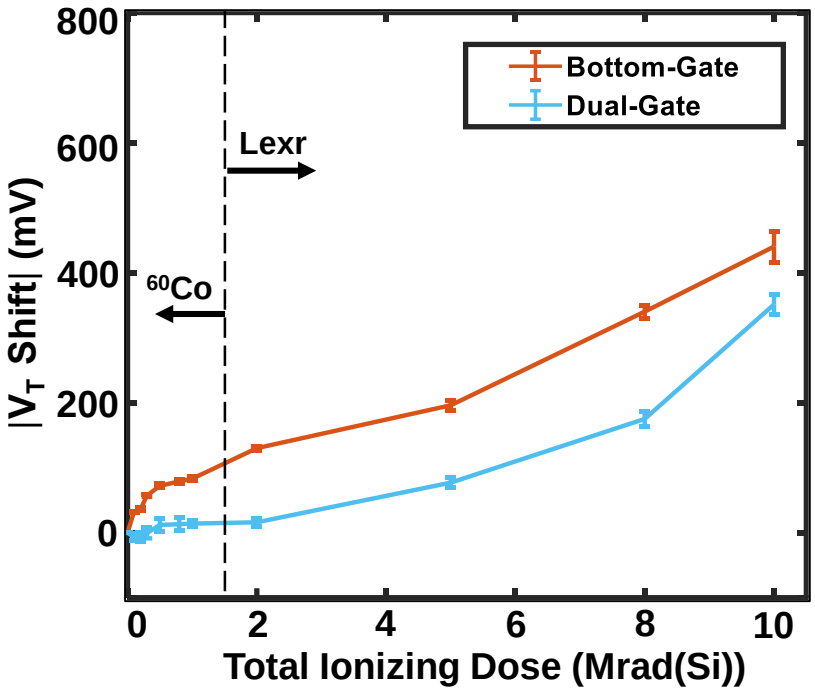

Figure A1.4.2: Mean $|V_T$ shift| of 256 local bottom-gate (orange) and 256 dual-gate (blue) CNFETs (gate dielectric EOT = ~ 7 nm) versus TID. The results from the LEXR source are appended to the results from the ^{60}Co source to confirm continuity between the LEXR and ^{60}Co sources. The error bars correspond to 95% confidence intervals.

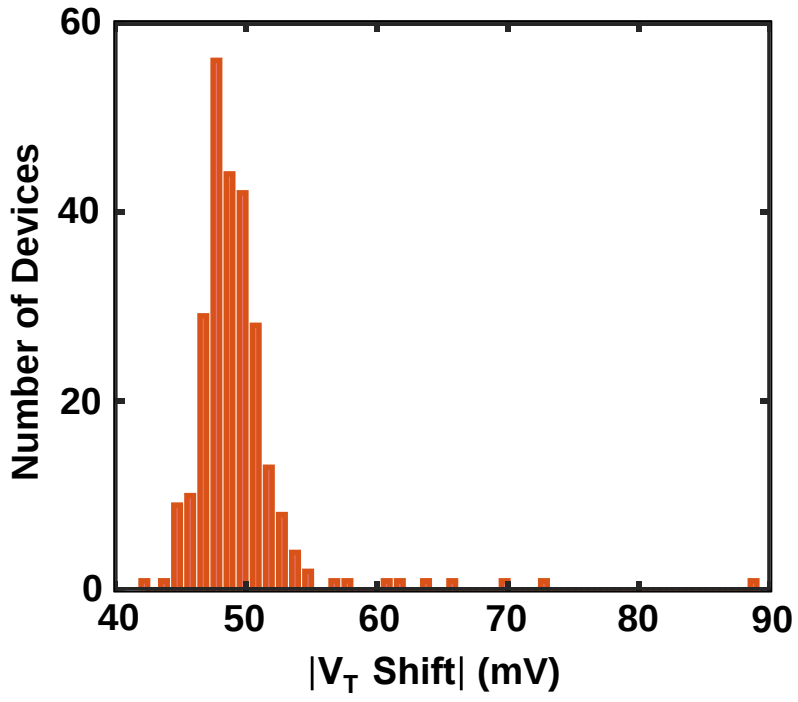

Figure A1.4.3: Statistical distribution of $|V_T$ shift| measured at 100 Krad(Si) γ-ray TID for a typical local

bottom-gate CNFET array (N=256).

Appendix A1.5: CNFET CMOS 6T SRAM Characterization

To ensure 6T SRAM functionality (V_{DD} = 1.8 V), we experimentally measure the write margin, read margin, and hold margin (Fig. 2f – Fig. 2h). These metrics are defined as followed [11-12]:

1) *Write Margin* (Fig. 2f): The tripping point (V_{TP}) is when bit = Q_b = V_{TP} with WL = V_{DD}. The write margin (WM), write margin (WMH), and write margin low (WML) are defined in (1) – (3) as:

$$\text{WML} = V_{TP} - V_{SS} \quad (1)$$

$$\text{WMH} = V_{DD} - V_{TP} \quad (2)$$

$$\text{WM} = \min(V_{TP} - V_{SS}, V_{DD} - V_{TP}) \quad (3)$$

2) *Read Margin and Hold Margin* (Fig. 2g and Fig. 2h): Both are extracted from the voltage transfer curve (VTC): *Q_b versus Q*, with bit = V_{DD}, bit_b = V_{DD}, WL = V_{DD} (read margin extraction), and WL = V_{SS} (hold margin extraction). We define ($V_{IL}^{(dr)}$,$V_{OH}^{(dr)}$) and ($V_{IH}^{(dr)}$,$V_{OL}^{(dr)}$) be the points on the VTC$^{(dr)}$ where the slope of *Q_b vs. Q* is -1, and let ($V_{IL}^{(ld)}$,$V_{OH}^{(ld)}$) and ($V_{IH}^{(ld)}$,$V_{OL}^{(ld)}$) be the points on the VTC$^{(ld)}$ (*i.e.*, the mirrored VTC) where the slope of *Q_b vs. Q* is -1. The read/hold margin (RM/HM), read/hold margin high (RMH/HMH), and read/hold margin low (RML/HML) are defined in (4) – (6) as:

$$\text{RMH or HMH} = V_{OH}^{(dr)} - V_{IH}^{(ld)} \quad (4)$$

$$\text{RML or HML} = V_{IL}^{(ld)} - V_{OL}^{(dr)} \quad (5)$$

$$\text{RM or HM} = \min(V_{OH}^{(dr)} - V_{IH}^{(ld)}, V_{IL}^{(ld)} - V_{OL}^{(dr)}) \quad (6)$$

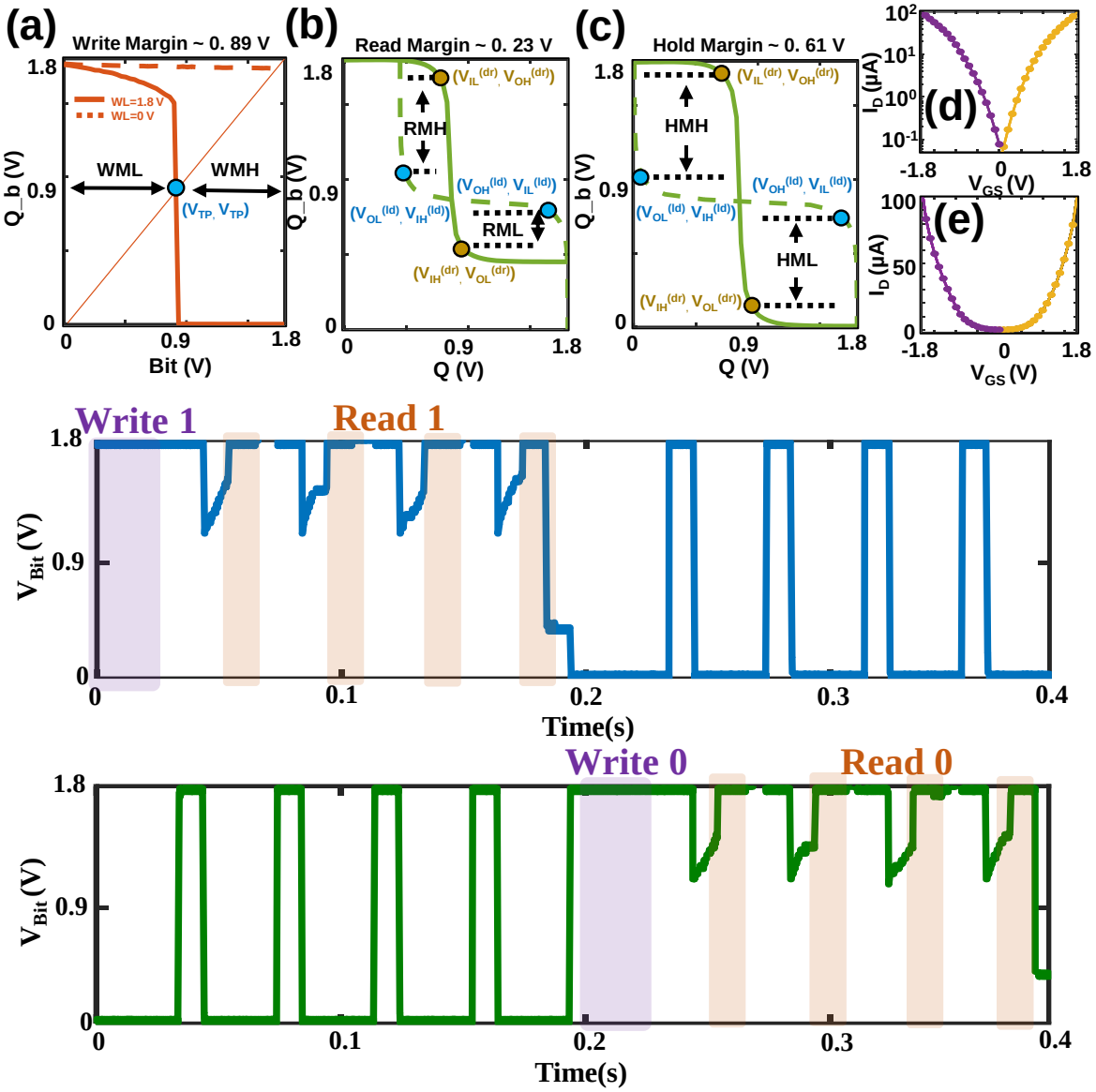

Figure A1.5.1: (a) Write margin, (b) read margin, and (c) hold margin measurements for a typical CNFET CMOS 6T SRAM (sizing ratio of 2.25:1.5:1 (D1/D2:A1/A2:P1/P2)) at 1.8 V V_{DD}. Typical PMOS (purple) and NMOS (gold) CNFET I_D *vs.* V_{GS} characteristics in (d) semilog and (e) linear scale (channel length = 2 µm, channel width = 40 µm, CNT density ~ 20 CNTs/µm) at 1.8 V V_{DS}. (f) Time-dependent waveforms at 1.8 V V_{DD} of a CNFET CMOS 6T SRAM cell (one write operation (purple) followed by four non-destructive read operations (orange)).

Appendix A1.6: Additional Considerations

When discussing CNFETs' intrinsic radiation-tolerance for transient upsets, it's important to shed light on the small cost due to CNT's reduced bandgap (Eg_{CNT} = ~1 eV *versus* Eg_{Si} = 3.6 eV). A reduced bandgap results in more charge being generated and potentially collected per ionizing radiation strike, thus increasing the likelihood of a transient upset to occur. However, this relatively small cost is outweighed by the substantial benefits CNTs provide owing to their ultra-thin body (1 nm) and reduced cross-section (CNFETs channel cross-section only <10 % CNTs).

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