Ground Station Mixed-Signal PCB and SFP Ethernet-to-Optical Connector for the Deployable Optical Receiver Aperture (DORA) CubeSat

by

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Abstract

The Deployable Optical Receiver Aperture (DORA) project at the Jet Propulsion Laboratory (JPL) in collaboration with Arizona State University (ASU) aims to demonstrate 1 Gbps data rate for crosslink communications among small spacecraft. There are numerous applications for this technology, including satellite swarms/ constellations, and surface to orbit communications. DORA allows a satellite's primary mission to continue without requiring the satellite to reorient for communication, thus enabling missions to use low-cost, off-the-shelf Altitude and Determination Control Systems (ADCS). DORA meet these specifications by replacing the spacecraft's traditional receiving telescope with incident-angle sensitive photodiodes to steer the onboard transmitting laser in the corresponding direction. The DORA optical ground terminal (OGT) will be stationed on the ground to communicate with the DORA CubeSat in flight. This thesis project will address the ground station analog and digital electronics and data transfer needed to deliver data received from the DORA CubeSat to its final destination for processing and storage. The ground station mixed-signal PCB (GS-MSPCB) will serve as the interface between the terminal's FPGA and the optical ground station control components. The FPGA will connect via an enhanced small form-factor pluggable (SFP+) port to an SFP switch and Wifi-6 router so that data may be accessed wirelessly.

Thesis Supervisor: Gim P. Hom
Title: Senior Lecturer

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Contents

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List of Acronyms

ADC	analog-to-digital converter
ADCS	altitude and determination control systems
AoA	angle of arrival
API	application programming interface
ASU	Arizona State University
BBB	BeagleBone Black
BER	bit-error rate
BSP	board support package
CLI	command line interface
CLICK	CubeSat Laser Infrared CrosslinK mission
COTS	commercial off-the-shelf
DoD	Department of Defense
DMA	direct memory access
DORA	Deployable Optical Receiver Aperture
EMI	electromagnetic interference
EPS	electrical power system

FAA	Federal Aviation Administration
FFC	flat flexible cable
FPGA	field-programmable gate array
FSM	fast steering mirror
FTP	file transfer protocol
Gbps	Gigabit per second
GPIO	general-purpose input/output
GPS	Global Positioning System
GTP	gigabit transceiver
GS-MSPCB	ground station mixed-signal printed circuit board
HDL	hardware design language
ILA	integrated logic analyzer
IP	Intellectual Property
IR	infrared
ISOC	inter-satellite omnidirectional optical communicator
JPL	Jet Propulsion Laboratory
JSON	JavaScript Object Notation
LA	limiting amplifier
LEO	low Earth orbit
MBM2	Motherboard Module 2
Mbps	Megabits per second

MSA	multi-source agreement
MSPCB	mixed-signal printed circuit board
OBC	on-board computer
OCSD	Optical Communications and Sensor Demonstration
OGT	optical ground terminal
PCB	printed circuit board
PHY	physical layer
POF	fiber optic
PPM	pulse position modulation
RTL	register-transfer level
SFP	small form-factor pluggable
SFP+	enhanced small form-factor pluggable
SiPM	silicon photomultiplier
SMA	SubMiniature version A
SNR	signal-to-noise ratio
SoC	system-on-chip
SOM	system-on-module
SPI	Serial Peripheral Interface
TIA	transimpedance amplifier
TRL	technology readiness level
UART	universal asynchronous receiver-transmitter

UHF ultra-high frequency

VLC visible light communication

YP Yocto Project

Chapter 1

Mission Concept and Project Overview

1.1 DORA Mission Objectives

As exploration of our universe expands outward, low data transfer rates limit the applications and mission operations of small satellites. Possible communication technologies for this data transfer include visible light communication (VLC), laser, and RF. Laser communication has the benefit of large bandwidth, a license-free spectrum, a high data rate, less power, and low mass requirements. However, there are several technological challenges that must still be addressed in order to make full use of laser communication. Earth's atmosphere causes absorption and scattering losses, attenuation due to various weather conditions, and atmospheric turbulence caused by variations in the temperature and pressure of the atmosphere along the propagation path of optical and infrared (IR) communication. There is also background noise from the Sun and other stars and pointing loss due to satellite vibration or imperfect tracking and stabilization mechanisms to consider. [11] Narrower beams enable higher data rates, but they require increased pointing knowledge and stability on both ends. Existing optical communication terminals need precise pointing on the order of arcseconds to align the narrow optical laser beam between terminals–a laser transmitter in low Earth orbit (LEO) may yield a footprint less than 100 meters

wide at its receiving ground station. [12] These requirements may be relaxed with ground station networks or portable stations, which introduce their own engineering challenges such as accurate calibration. [7] Due to these challenges, RF historically has been the transfer method for ground to CubeSat communications. [11]

CubeSats and small satellites offer many advantages, including their feasibility for swarm configurations. Swarms can serve as redundant multi-node distributed sensor networks, be a synthetic aperture for radar, do astronomical imaging, or provide navigation timing. [13] New small satellite constellation concepts often have competing requirements necessary to execute their mission. For example, cross correlation requires many links to a central processor station. If the data is sent to Earth to be cross correlated, it is highly decimated. Correlation could be completed in orbit if laser communication transferred all data to a correlator station, or the need for a central processor was eliminated with many simultaneous connections to all nodes. However, nodes must also maintain their orientation towards their astronomical target, so any solution must be independent of spacecraft attitude. In addition, relaxing the typically strict pointing requirement reduces mission cost and difficulty. A multi-directional laser terminal addresses these pointing requirements while enabling simultaneous node connections. [7]

The Deployable Optical Receiver Aperture (DORA) project at the Jet Propulsion Laboratory (JPL) in collaboration with Arizona State University (ASU) aims to address these challenges and improve on current data rates by demonstrating 1 Gigabit per second (Gbps) data rate for crosslink communications among small spacecraft, especially for those forming a swarm or a constellation, and for surface to orbit communications. Enhancing the data rate to a Gbps or more over long distances will benefit communications for future space missions, such as the connection between lunar assets (such as astronauts, rovers, instruments) and the lunar gateway in the LunaNet network. [6] DORA also allows a satellite's primary mission to continue without reorienting for communication, thus enabling satellite missions to use low-cost, off-the-shelf altitude and determination control systems (ADCS). [12] DORA leverages five receiver panels that are populated with fast photodiodes and use power

combining to simulate a larger aperture. Each panel is orientated at different angles in order to calculate the angle of arrival (AoA). A high power laser diode and a beam steering mirror are used to accurately point the transmission signal to the optical ground terminal (OGT) using the calculated AoA. The OGT has a similar architecture as the DORA payload, but exploits the advantage of low constraints on size, volume, and weight. [6]

The primary goal of the DORA mission is to demonstrate a 1 Gbps link at up to 1000km distance with a coarse bus pointing requirement of 5°, with the eventual goal to demonstrate cross-link communication between spacecraft. For this mission, only a single satellite will be deployed and DORA will test communications between low Earth orbit (LEO) and Earth. Results from this mission may then be expanded upon for future multiple-satellite missions. The target transmitter design uses an 850 nm laser assembly with an opening angle of 20 arcseconds and provides a 1 Gbps link at 2 W with a spot size of 500 m at 1000 km. A successful demonstration will raise the technology readiness level of widefield optical technology to technology readiness level (TRL) 7. [7]

Key performance parameters are listed in Table 1.1. The results of link performance will depend on several factors, including background light rejection and the repeatability of panel deployment angle, which will impact angular determination and the precision of AoA determination. In order to close the uplink, all the panels will need to be exposed to the incoming laser due to the angular control requirement. [7]

This mission will use open source subsystems, including radio, software system, and UHF antenna. In addition, the goal of a 1 Gbps data rate adds a requirement for an internal 1 Gbps link between the laser terminal and the central flight computer, which limits the selection of commercially available computers with flight heritage. [7]

1.1.1 Related and Previous Work

Previous attempts at laser communication onboard CubeSat platforms similar to the DORA mission have been made, including multi-link connection nodes and a

Key Performance Parameters	**Required**	**Target**
#1 - Rx AoA accuracy	20" (96 μr)	5" (24 μr)
#2 - Tx pointing accuracy	20" (96 μr)	5" (24 μr)
#3 - Allowed bus drift rate	0.1°/s	1°/s
#4 - Allowed off-axis angle	5°	36°
#5 - Sustained data rate	0.5 Gbps	1 Gbps
#6 - Bit error rate	10^{-8}	10^{-9}
Other Parameters		
Transmit Power	1 W	2 W
Wavelength	850 nm	850 nm
Opening Angle	100"	20"

Table 1.1: Performance metrics for the DORA system

demonstrated laser communication downlink from LEO to sea level.

The DORA payload is preceded by the inter-satellite omnidirectional optical communicator (ISOC) developed at JPL. The ISOC is an omnidirectional optical terminal designed with spacecraft constellation communications in mind, and has a truncated icosahedral geometry with an array of miniature laser telescopes and optical detectors. The optical connectors are well suited to the application because they can receive a signal from any direction and can be used to calculate the AoA of the incoming signal. The array placement allows for full sky coverage and multiple simultaneous links. The ISOC has undergone in-laboratory testing for a TRL of 3. [12][14][15]

The Aerospace Corporation, under the NASA Optical Communications and Sensor Demonstration (OCSD) program, completed a demonstration of an optical communications downlink from a low-earth orbiting free-flying CubeSat at 200 Megabits per second (Mbps) with a bit-error rate (BER) less that 1E-5 using a 1064-nm laser transmitter operating at 2 W. The vehicle used on-board star trackers for pointing accuracy which simplified the design and operation of the ground station. Limitations in the scope of the program precluded the development of ground station electronics needed to process data at rates beyond 200 Mbps. [8][10] The CubeSat Laser Infrared CrosslinK mission (CLICK) aims to demonstrate a 20 Mbps crosslink at ranges from 25 km to 580 km and operate full-duplex at 1537 nm and 1563 nm with 200 mW of transmit power. The mission aims to demonstrate communication

between two nanosatellites and a portable optical ground station. [3] Phase I of the Starlink global internet constellation is planned to use laser crosslinks, which provides an opportunity to look at the different types of links that can be made between satellites in the same and different orbital planes, which will play a role in designing low-latency paths for future satellite networks. [4]

1.1.2 Optical Communication Principles

Familiarity of the concepts of optical communications will allow the design a functional and robust system. DORA utilizes power combining, angle of arrival sensing, and background light mitigation, while also accounting for external factors that affect optical communications from Earth's orbit like legal regulations, weather, and atmospheric conditions.

Photodetector Arrays for Satellite Swarms

Spacecraft swarms provide many mission benefits while introducing challenges in regards to the power needed to operate at high speed and the increased pointing accuracy requirements due to the necessity of maintaining line-of-sight between nodes. A system can use a lens or larger aperture detector to gather enough power by increasing the irradiance of the signal on the detector. However, the bandwidth is inversely proportional to the area, which limits how large the detector can be, which in turn limits the power. The collecting area of the lens is also limited by the aperture, and due to its focal length, the lens has a narrow field of view which reduces the pointing accuracy of the system. DORA addresses these constraints by implementing an array of photodetectors arranged to have angular dependency based on their placement to improve the pointing accuracy requirement. Specifically, the photodetectors are placed in a spherical configuration to simultaneously achieve a wide field of view. In order to receive more power, deployable receiver panels will increase the receiver's aperture size once the CubeSat has reached its orbit. [6]

Link Budget

In order to calculate the requirements for the receiver and transmitter lenses over the desired distance, the following calculations can be done for the received power, gain and the capacity of the Poisson pulse position modulation (PPM) channel to attain the desired data rate.

We have two optical terminals separated by a distance of R, as shown in Figure 1-1. The transmitting telescope has a laser diode and a transmitting, or collimating, aperture. The receiver has a photodetector and a receiving lens.

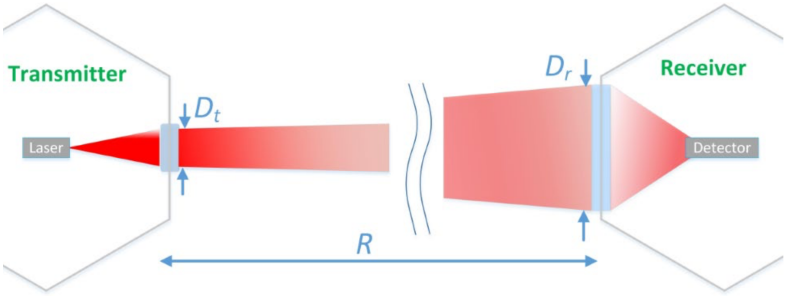


Figure 1-1: Transmitter and receiver terminals parameters

The effective isotropic radiated power E, the receiver gain G, and the space loss L with the transmitted power P_t, the effective aperture diameters for transmitting and receiving D_t and D_r, and the operating wavelength λ, respectively are

$$E = P_t \left(\frac{\pi D_r}{\lambda}\right)^2, G = \left(\frac{\pi D_r}{\lambda}\right)^2, L = \left(\frac{\lambda}{4\pi R}\right)^2 \tag{1.1}$$

Equation 1.2 calculates the received power P_r for the optical terminal (with neglected losses) with the system efficiency η.

$$P_r = EGL\eta \tag{1.2}$$

Thus, with the PPM order M, the slot width T_S, and the energy per photon $E_\lambda = hc/\lambda$ where h is Planck's constant and c is the speed of light, the capacity of

the PPM channel is

$$C_{OPT} = \frac{log_2(M)}{MT_S}\left[1 - e^{-MP_rT_S/E_\lambda}\right] \tag{1.3}$$

The maximum processing speed of the transmitter and receiver, the laser pulse width, and clock accuracy typically limit the maximum supportable bandwidth, $1/T_S$. The parameters for the DORA system are $\lambda = 850$ nm, $P_t = 250$ mW, $D_t = 1.5$ cm, $\eta = 0.025$, $T_S = 0.5$ ns, and M = 2. Figure 1-2 shows the possible capacity, equivalent to the data rate, possible for a ground station receiver aperture diameter D_r of 10 and 20 cm. Either of these options will support a data rate of 1 Gbps for distances up to approximately 1800 km. [12]

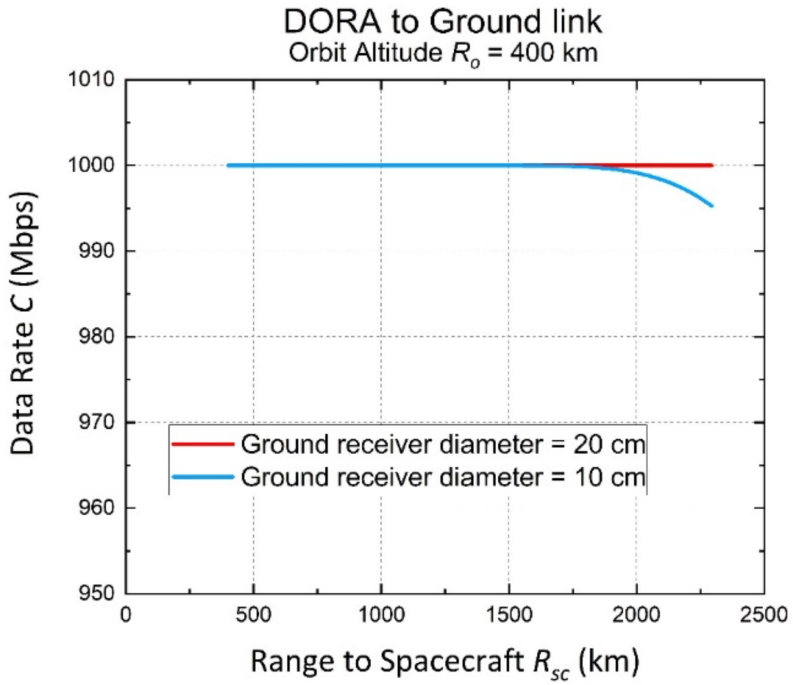


Figure 1-2: PPM channel capacity as a function of range for payload to ground station

Power Combining

DORA's optical system is designed with an array of silicon photomultiplier (SiPM)s, which are similar to avalanche photodiodes, but the SiPMs have two outputs at different time resolutions. A transimpedance amplifier (TIA) is used to provide additional gain and convert the output current signal to a voltage to be sampled by an analog-

to-digital converter (ADC). The fast outputs of the SiPMs are connected to an RF combiner before reaching the TIA in order to improve signal-to-noise ratio (SNR) by increasing the peak of the output pulse. This also provides isolation that lowers the sum capacitive load when the outputs are brought together. The output of the TIA connects to a comparator which converts the analog output signal of the TIA into a digital signal. [12]

Finding Angle of Arrival

The DORA payload will determine the incoming laser AoA using the direction dependent response of the SiPMs. The SiPM sensitivity decreases for arrival angles away from the boresight direction with cosine dependence. The deployable panels, shown in Figure 1-3 will be tilted relative to each other (and the top face) to provide varying SiPM orientations. This will enable the two-dimensional AoA to be calculated from the relative incoming laser strength seen by each panel.

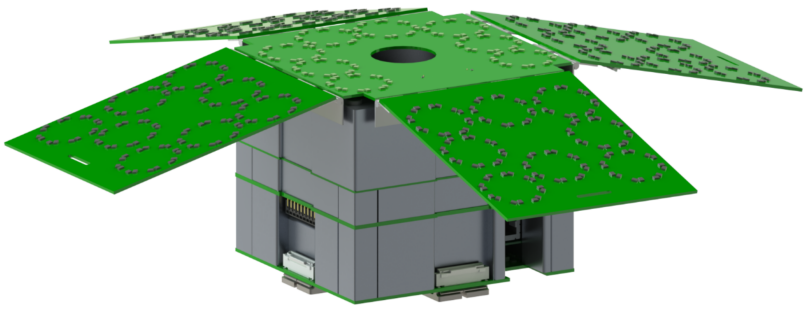


Figure 1-3: DORA payload showing deployed receiver array

Background Light and Weather Considerations

The DORA receivers will be more susceptible to background light in comparison to a narrow field system due to their large field of view (about π steradians). This means bright sources are more likely to be in field of view and diffuse background emission will integrate to larger power than for narrow field of view systems. Wide field infrared receivers have trouble in particular, with noise contributions from sunlight, moonlight, Earth and Moon thermal emission, artificial lights, and atmospheric

emission lines. SiPM have a broadband response to light across much of the visible and near-IR spectrum, which can be addressed using narrowband filtering to block everything except the monochromatic laser signal to increase the SNR. This high level of sensitivity makes only nighttime operations possible, even with filtering. This also affects spacecraft attitude control as it removes sun sensors as a possible control input. Another factor to consider for DORA operations is the transmission path between LEO and Earth's surface. The opaqueness of clouds and distortion from the atmosphere can disrupt transmission. Observatories pre-selected for good seeing, dry weather, and low light pollution make a good option when considering locations for the ground station. Portability introduces challenges with logistics and calibration, but provides benefits with seasonal variation, cost saving, and flexibility. A low cost and portable ground station will allow operation in multiple sites during testing and general operation. [7][12]

Regulations

In terms of regulations in the airspace, laser communications are able to share space due to narrow beam width but have a higher power density that necessitates federal safety regulation. The 2W infrared laser planned for DORA is in the highest class 4 category requiring strict safety measures during lab testing and on orbit operations. Outdoor laser use must be coordinated with the Federal Aviation Administration (FAA) which requires geographic airspace limits, plane spotters, and similar measures to operate safely. Operations will be coordinated with the Department of Defense (DoD) Laser Clearinghouse which manages potential conflicts. [7]

1.2 DORA Cubesat Subsystems

1.2.1 DORA Bus

DORA is a 3U CubeSat shown in Figure 1-4, with roughly 1U designated for the optical terminal payload. The avionics stack occupies 1.5U with two radios, attitude

control, central computer and batteries. A circularly polarized quadrupole antenna will be deployed from the opposite end of the payload with redundant burn resistors. DORA has 4U of body-mounted solar panels and an additional 4U of deployed panels, which will need at least 60 Wh of power storage to make it through a long pass above 60% depth of discharge.

Parts were selected to meet mission requirements while also maintaining sustainable CubeSat development. This included avoiding parts with high cost, closed software, or requiring significant legal or contractual restrictions, while parts with open source software and interfaces are preferred. [7]

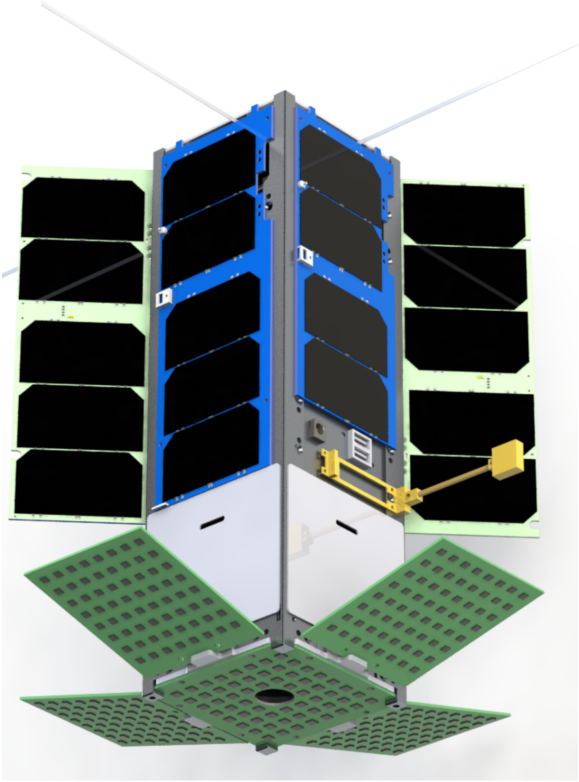


Figure 1-4: DORA CubeSat rendering in flight-deployed position

Mechanical

The structure of the body is a custom-machined set of rails and brackets similar to that manufactured for ASU's Phoenix CubeSat, with updates based on past experience. The avionics will be mounted in a single stack using threaded spacers with PC104 as

an interconnect. A custom enclosure might be added if cross interference is observed during electromagnetic interference (EMI) compatibility testing. [7]

Computer

The highest importance requirement for the on-board computer (OBC) is to accept 1 Gbps Ethernet traffic from the payload while managing telemetry, command and control, and mission scripting. The BeagleBone Black (BBB) is an open-source design, single board computer with a 1 Gbps Ethernet interface. Pumpkin has adapted the BBB as a daughter module on the Motherboard Module 2 (MBM2), which uses a custom fabrication of the BBB with parts selected to tolerate an extended temperature range. The MBM2 also has an SD card slot for additional storage and a hardware watchdog to reset the computer as necessary. According to the vendor, the MBM2 has been used successfully on orbit. The MBM2 acts as an interface for all other connections between the BBB and the rest of the spacecraft via a PC104 header and an additional 25-pin physical layer (PHY) connector. The PC104 header is part of a family of embedded computer standards that define the form factor and computer bus, particularly for specialized environments where a small, rugged computer system is required. The standard is modular, which allows commercial off-the-shelf (COTS) products to be combined from different manufacturers. The PC104 header is the main interface for the spacecraft stack, while the PHY connector will communicate directly with the payload. [7]

Software

Kubos is a custom Linux operating system that targets BBB and has added software layers that provide process management, inter-process communication, and basic hardware interfaces. The Linux build uses Busybox, which provides compact versions of standard Linux programs and the Device Tree system for managing hardware interfaces. The Kubos software layers are written primarily in the programming language Rust, which is similar to C/C++, but with added layers of fault tolerance and error handling. [7]

Power

The electrical power system (EPS) consists of three major parts: the conversion and distribution board, batteries, and solar panels. Batteries will be Clydespace 30Wh packs that include independent charge and discharge management circuits. There are eight fixed and eight deployed solar panels supplied by Pumpkin that will provide 23.5Wh per orbit. The power budget is summarized in Table 1.2. The laser terminal is a high power device but will be operated at low duty cycle, so it will draw 8.1W during normal operation. The payload will only operate for one to two passes per day, 15 minutes per pass, as it passes over the ground station in the southwestern United States at nighttime. Otherwise, the spacecraft will be in standby charge mode drawing approximately 6W, transmitting a periodic health beacon and tracking the Sun to orient the solar panels at the Sun and the payload at the ground.

The CubeSat generates up to 18 W when in full sunlight, and a typical standby orbit adds about 5 Wh to the battery energy. An orbit that includes a payload test pass is also power positive, but adds less than 3 Wh to the battery energy. A safe mode is engaged when the battery passes below a preset depth of discharge threshold, and pointing, Global Positioning System (GPS), and other non-critical services are disabled. [7]

Property	**Value**
Peak solar power	18W
Orbit-average solar power	9W
Power used in safe mode	4W
Power used in standby mode	6W
Power used in payload test mode	16W
Battery size	30Wh
Charge time from flat (standby)	6 orbits
Energy per payload test (15 minutes)	4Wh
Battery level after payload test	87%
Recharge time after payload test	1 orbit

Table 1.2: DORA power budget

Pointing

One of the goals of the DORA system is to reduce the pointing requirements required for laser communications, thus minimizing cost and complexity. The CubeADCS was selected to balance pointing requirements after comparing several off-the-shelf options. The system will fix positions using Sun trackers, each of which has a datasheet accuracy of $<10°$during day-time parts of the orbit, and many sensors combined have an accuracy better than 1°. A GPS will add orbit knowledge, which will further improve the accuracy of target tracking. [7]

Radios

The primary radio link is dedicated to sending telemetry and receiving commands or software updates. It can also downlink data that has been uplinked via the laser when in receive only mode. This laser-to-radio loop mode provides a third layer of redundancy to test the success of laser operations, in addition to the bidirectional laser link and on-board hashing to assess bit error rates. The selected "Open LST"radio is compatible with the existing ASU ultra-high frequency (UHF) ground station, and data rates of 9600 baud are easily achievable at UHF using a range of modulation schemes. The UHF antenna is a quadrupole circularly polarized turnstile with Nitinol wire elements. A GlobalStar simplex radio will provide an additional backup health beacon system. The simplex broadcasts information to the GlobalStar satellite constellation, which will serve as a way to externally monitor spacecraft health and plan ahead for short pass operations. [7]

1.2.2 DORA Payload

The on-board 1U payload is comprised of five detector panels, the transmitting telescope, and processing unit. The goal is to provide duplex connectivity between the payload and ground station, and eventually other identical satellites in a swarm, at rates up to 1 Gbps over 1000km links. The terminal consumes 2.1W in receive mode and 8.1W when transmitting. [12]

Mechanical Design

The payload stack of five boards is mounted in an aluminum enclosure that provides thermal and mechanical stability. Boards are interconnected via a combination of pin headers and cables, and the deployable receiver boards are connected via flat flexible cable (FFC)s.[7] DORA will be launched with the receiver panels in a stowed configuration against the sides of the 3U body, held by nylon lines internal to the payload and deployed by passing current through Nichrome wires to melt the nylon. The accuracy of the panel deployment angle will be an important factor in the accuracy of AoA determination. [6]

FPGA Design

A Xilinx Kintex-7 field-programmable gate array (FPGA) is the communications controller for the DORA payload. The FPGA sits on a Trenz Electronic TE0741 system-on-module (SOM), which also contains three high-density board-to-board connectors for various carrier card connections. A custom carrier card provides several interfaces, including RS-422, Ethernet, a microSD card, a 512Mbit Cypress HyperRAM, and an additional high-density board-to-board connector for connecting the carrier card to the mixed-signal printed circuit board (MSPCB). The RS-422 interface is used for command and control, and report telemetry to the CubeSat's OBC using JavaScript Object Notation (JSON) messages. Files are transferred via file transfer protocol (FTP) from the OBC to the FPGA's on-board memory for later transmission via Ethernet. Test files for transmitting over the optical link are stored on the microSD card. The Cypress HyperRAM is used as a data buffer during an optical link. The board-to-board connector routes control signals for the MSPCB's ADC and for actuating the Optotune dual-axis voice-coil fast steering mirror (FSM), as well as high-speed differential signals for modulating the communications laser, and for receiving data from the SiPM panels.

The payload has several operating modes for the expected sequence of orbital operations, including contingencies. This includes passive acquisition where telemetry

and high speed data are read out but the transmitter is inactive, active upload where uplinked data is stored in high speed memory, and bi-directional loopback where received data is retransmitted. These modes fulfill minimal mission requirements but do not enable full data interfaces, which is a stretch goal. The payload accepts commands via serial bit encoding and an application programming interface (API) with key variable pairs in the JSON format, with similar formatting for the telemetry output.

A MicroBlaze soft-core processor running FreeRTOS is at the center of the FPGA system. The TCP/IP stack, RS-422 command parser, and a universal asynchronous receiver-transmitter (UART) command line interface (CLI) are implemented as independent tasks in FreeRTOS. The ADC controller module receives samples from an Analog Devices AD7606C-18 simultaneous sampling ADC (which is connected to the SiPM panels). In turn, the pulse detector module monitors the ADC samples to look for a pulse above the noise floor. Once a pulse is detected, the averages of the ADC values during that pulse are calculated. These values are sent to the AoA calculator after the pulse ends. After calculating the AoA, the AoA module sends an interrupt to the MicroBlaze to steer the FSM using the new estimated AoA values. [6]

Panels

The DORA payload has five panels deployed to an oblique angle to increase field of view and allow AoA measurement. The angle is determined by comparing signal amplitude between different panels against a model for the angular dependence of the sensor response.

Each panel is a separate receiver with three main circuits: biasing, communications, and AoA. Each panel also contains SiPMs in an array to mimic a large optical receiver aperture. The SiPM outputs are brought together with power combiners tuned to provide a matched impedance at GHz speeds. The biasing circuit has a DC-DC converter that steps down the supplied 5 V to -30 V with a thermistor as a feedback resistor in order to change the bias voltage. The SiPM gain is dependent with temperature, so a constant gain requires a temperature dependent bias. The

communications circuit combines each detector output into the data signal via the power combiner. This output is connected to a TIA that boosts the current signal to a readable voltage signal. Next, a limiting amplifier (LA) caps the maximum signal power over a frequency range, regardless of the input signal strength. This effectively converts the analog voltage signal to a digital signal for the FPGA by switching between ground and logic voltage according to the input analog signal. The AoA circuit combines the slow output of the detectors that is fed to a separate TIA. The output of this TIA is read by the ADC for each panel simultaneously. The power and input/output signals of each panel are connected to the MSPCB via an FFC. The outputs and power of each receiving panel are routed on the MSPCB, as well as the FPGA and burn wire connections.

The transmitter laser is set into the center panel, where the 850nm laser passes through a 3X bi-confocal lens and then reflects off a 45°FSM. This FSM is steered by voice coils with a 35° steering range and large surface area. The telescope with an actuated mirror will enable the terminal to transmit off boresight and track a target. [6]

1.2.3 DORA Optical Ground Station

The DORA OGT enables high speed uplink and downlink with the DORA payload. It echoes the design of the payload and was developed in parallel to ensure maximum optimization of the transceiver system, but it does not need to satisfy a size constraint beyond portability, unlike the payload.

Optical Design

The main receiving aperture of the OGT has a 20 cm diameter lens focused onto a single SiPM receiver inside the station body. This lens has a comparable collecting area relative to the deployable panels, but reduces the number of SiPMs needed to reduce total cost. The transmitter is a replica of the 2W laser transmitter in the CubeSat payload, due to its steering and correction abilities separate from the OGT

gimbal. This duplication will also provide a technology demonstration of the potential interaction of two identical CubeSats for future missions. 20 SiPM sensors circle the lens to provide a coarse AoA reading that steers the telescope mounted on a gimbal. [6][7]

FPGA and PCB Design

Similar to the DORA payload, the ground station also contains a Kintex-7 FPGA on a Trenz Electronic TE0741 SOM to control the optical communications link. The SOM sits on the ground station mixed-signal printed circuit board (GS-MSPCB), which interconnects the FPGA carrier card, laser transmitter, ADCs, and FSM carrier board, SiPMs and receiver. Each of the 20 photomultiplier outputs are routed via an FFC connector to ADCs that pass the digitized signal to the system FPGA on the carrier board. Each photomultiplier has circuitry to bias and monitor it, also via an FFC connector. The signal from the receiving lens is passed directly to the FPGA carrier board. Two SubMiniature version A (SMA) connectors pass data and power to the laser transmitter. The FSM carrier board receives Serial Peripheral Interface (SPI) signals to command the FSM that steers the transmitter laser beam. The board is supplied with 5 volts, and the FPGA will provide 3.3V drive voltage for the ADCs.

SFP+ Connection

In addition to controlling the GS-MSPCB, the FPGA will configure data for access via enhanced small form-factor pluggable (SFP+) device using the 10G Ethernet Subsystem (10GBASE-R) Intellectual Property (IP) in Vivado. Physical small form-factor pluggable (SFP) modules are used to interface with optic fiber or copper cable, and the SFP+ standard can transfer data at speeds up to 16 Gbps. The SFP+ device will connect the OGT to an SFP switch. This switch will be connected to a Wifi-6 router that has a 10G SFP+ port, so that data from the OGT may be accessed wirelessly via laptop.

Software

Ground station software is implemented as an application-oriented design in Rust. The software uses a basic terminal for commanding and receiving, with additional applications to store and display data. A local PostgreSQL database stores telemetry data that is displayed using the open-source system, Grafana. Logs received from the spacecraft are stored separately from the telemetry in an influx database and similarly visualized using Chronograf. Each application is independent to increase the degree of fault containment. For example, if an error occurs with the database, then commanding/receiving, log storage, and visualization are all unaffected and the Grafana dashboard would cease to update since there is no new telemetry being stored. [6]

Chapter 2

Design

2.1 GS-MSPCB

The ground station mixed-signal PCB (GS-MSPCB) will serve as the interface between the terminal's FPGA and the optical ground station control components.

2.1.1 Function and Requirements

The GS-MSPCB interconnects the FPGA carrier card, laser transmitter, ADCs, and FSM carrier board, SiPMs and receiver as laid out in Figure 2-1. The ground terminal has 20 SiPMs used for calculating the signal AoA and a 200 mm diameter lens that focuses all the signal power on the receiver board at the lens focal point. Each of the 20 SiPM outputs are routed via a FFC connector to ADCs that pass the digitized signal to the system FPGA on its carrier board. Each SiPM will need circuitry to bias and monitor them, also via an FFC connector. The signal from the large lens is passed directly to the FPGA carrier board. Moving clockwise to the next component, the transmitting board has two SMA connectors to pass data and power to the laser transmitter. The FSM carrier board receives SPI signals to command the FSM to steer the transmitter laser beam. The board is supplied with 5 volts, and the FPGA provides a 3.3V drive voltage for the ADCs. The Kintex-7 FPGA on a Trenz Electronics TE0741 SOM commands the signals for the various

system components. The TE0741 will sit on the TEBA0841 carrier board, which includes an SFP+ port to be used for project development and testing. The carrier card connects to the GS-MSPCB using a 60-pin Samtec Razor Beam High-Speed connector. The high-speed GTX transceivers of the Kintex-7, along with several general-purpose input/output (GPIO) and an SPI interface, are routed through this connector. The GTX transceivers are used to modulate the transmit laser, and to recover data from the OGT.

In addition to interfacing with the GS-MSPCB, the FPGA serves to configure data to travel via enhanced small form-factor pluggable or SFP+ device using the 10G Ethernet MAC IP and the 10G Ethernet PCS/PMA (10GBASE-R) IP in Vivado. SFP modules are used to interface with optic fiber or copper cable. The SFP standard can transfer data up to 1 Gbps and SFP+ modules can do up to 16 Gbps.

2.1.2 Ground Station Circuit Design

In order to meet the requirements discussed in Section 2.1.1, the circuit design for the ground station is as follows. Power is supplied from the CubeSat bus at 5V, which is filtered before dispersing to the components on the board. This involves several capacitors in parallel of values 10nF, 0.1uF, 1uF, and 10uF to damp noise at a range of frequencies, followed by a ferrite bead inductor in series.

The FPGA connector is a 60 position self-mating connector in hermaphroditic surface mount gold. It is non-gendered (it mates with an identical connector) which simplifies design and ordering logistics in coordination with attached FPGA carrier card. The top four pins are dedicated to GTX connections with the transmitter and FSM. Eight pins are designated for each data channel and twelve pins carry control signals for the ADC. Six pins are used for the FSM. The FPGA also delivers 3.3V on two pins that is filtered by three parallel capacitors of 10nF, 0.1uF, and 1uF.

The FSM connector is a 10+2 position male signal and power vertical through-board connector with jackscrews to re-enforce the physical connection to the board. It carries eight control signals to the mirror carrier board that originate from the FPGA, as well as 5V from the power source. The PCB fabricated and discussed in

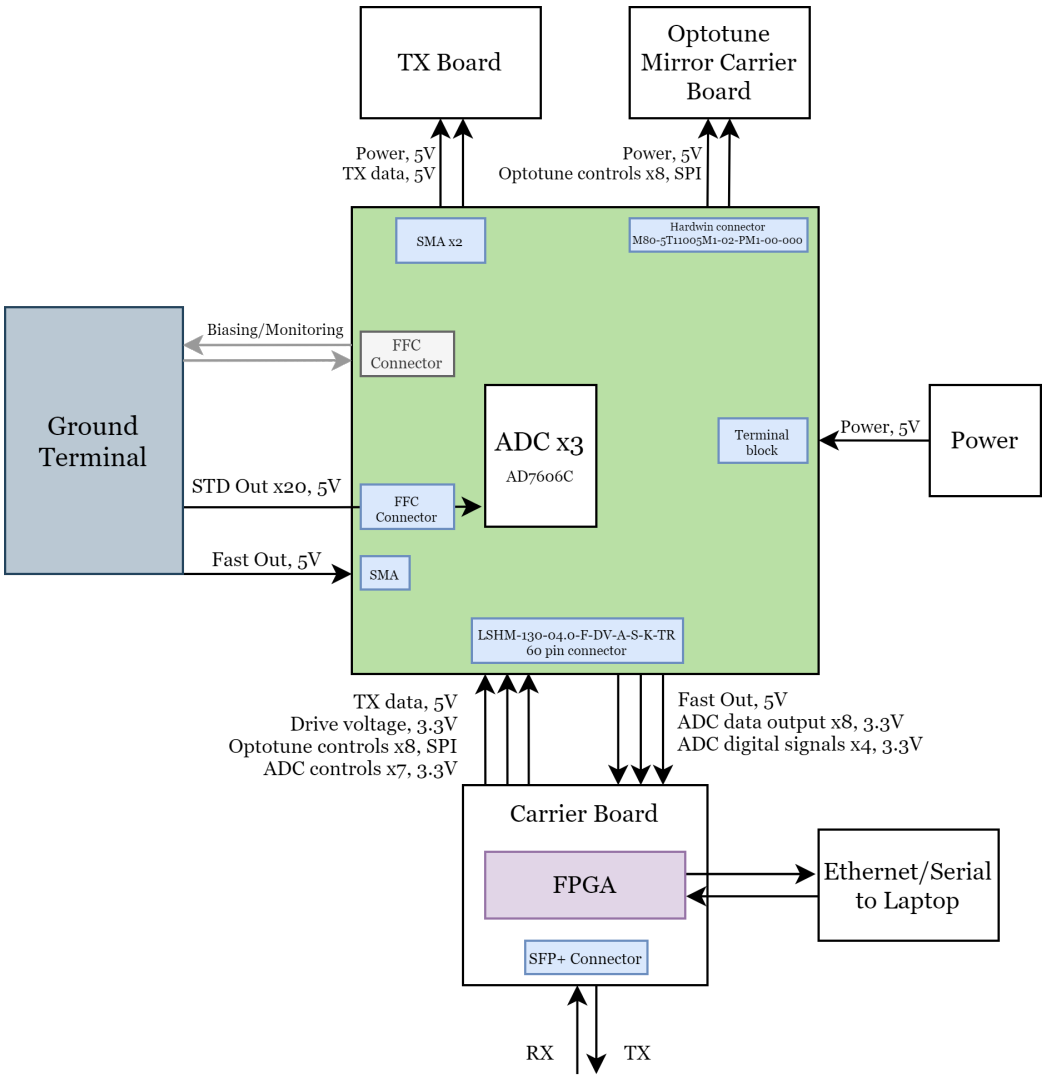


Figure 2-1: GS-MSPCB block diagram

this thesis is missing the Harwin FSM connector because the FPGA connector didn't have enough pins available on the current iteration of the mounted carrier card. The next iteration will have more layers on carrier card to properly route all of the FSM control signals. Thus, the Harwin connector was removed for this iteration due to production cost and simplicity, but will be straightforward to add back in the future.

The laser transmitter board receives data to be transmitted from the FPGA that is passed via SMA connector to the board, as well as 5V. The FFC connector receives analog readings from the twenty SiPm boards on the sensor array placed to determine AoA. Each of these are routed to the ADCs to be converted to a digital signal that

is passed to the FPGA for AoA calculations. The signal from the main receiving lens is connected via SMA and sent directly to the FPGA.

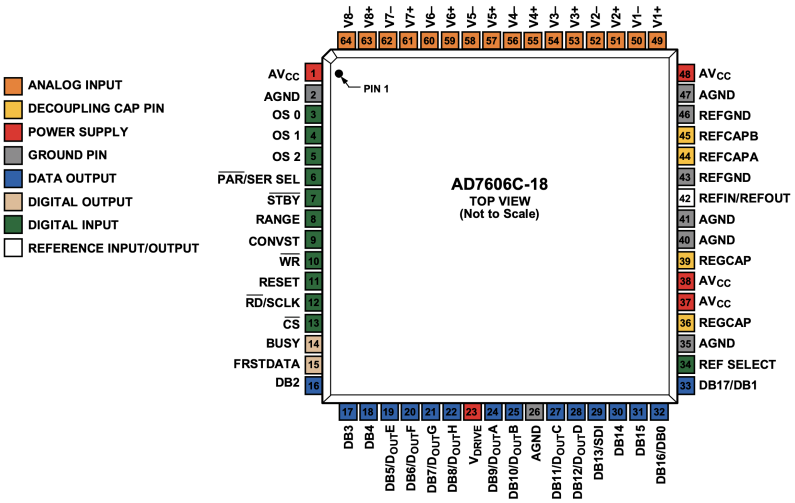


Figure 2-2: AD7606C-18 pinout from datasheet

The pin connections for the AD7606C-18s (Figure 2-2) are easily determined from the datasheet. [5] AV_{CC} and V_{DRIVE} are 5V and 3.3V respectively, so that logic level is 3.3V with the FPGA. Internal/external reference selection logic input, REF SELECT, is tied to logic high so that the internal reference voltage is selected and enabled. The oversampling Mode Pins, OS0 to OS2, are tied to logic high to enter software mode so that the ADC is configured by the corresponding registers accessed via the serial or parallel interface. Parallel/serial interface selection input, PAR/SER, is tied to logic high so that the serial interface is selected. The analog input range selection input, RANGE, is not needed due to being in software mode so it is tied to ground. Parallel write control input, WR, is tied to ground since the ADC is in serial mode and thus the pin is unused. Standby mode input, STBY, is tied to logic high per datasheet recommendation although it is unused. DB2, DB3, DB4, DB14, DB15, DB16/DB0, and DB17/DB1 are connected to AGND since their parallel interface functions are not used for this implementation.

CONVST, RESET, FRSTDATA, DoutA to DoutH, SDI, and RD/SCLK are all connected to GPIO pins of the FPGA and can be shared by the three ADCs. Chip select, CS, and busy output, BUSY, are also connected to GPIO pins but they are

unique to each of the three chips since the software uses CS and BUSY to cycle through each ADC and select which chip the FPGA is listening to at a given time. [5]

2.1.3 Layout Techniques and Best Practices

In order to optimize the performance of the PCB, many best practices were incorporated into the design process for traces, vias, ADC wiring, and other design choices.

Traces are the most fundamental part of the PCB, and a successful design relies on traces that perform as close to ideal as possible where the potential for real-world noise is avoided. First, the current return loop for each trace was considered during layout and routing to avoid multiple loops overlapping in the ground plane. During the layout process, the overlapping of analog and digital traces was avoided as much as possible. When crossovers of traces on layers in close proximity are necessary, it is best for traces to cross orthogonally, to reduce the effect of feedthrough through the board.

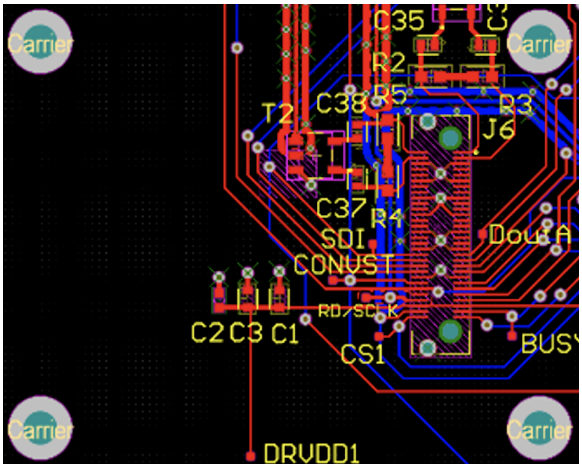


Figure 2-3: FPGA connector layout on the GS-MSPCB

For the board traces, each trace is distanced by at least 20 mils (twice the 10 mil trace width for most traces) from all other traces unless it is absolutely not possible. Trace widths for traces that carry a large amount of power were checked with a current tolerance calculator for printed circuit board (PCB) traces to ensure

the traces were large enough for the amount of current in every node. It is important to keep traces straight or at 45°angles to facilitate the smoothest movement of current possible. A teardrop shape was used to move between different trace widths instead of a sudden cutoff to provide a smoother transition. In addition, the pads of the ADC were connected outside of the ADC footprint to ensure successful fabrication and avoid soldering issues.

For time-sensitive traces running in parallel, such as clocks and sensor outputs, it was crucial to make sure the traces were similar in length to ensure every signal arrived at the destination synchronously. The frequency for the various traces affected ranged from 200 MHz to 1 GHz, so 200 mils difference ensured that a signal wouldn't surpass another by more than 1/60th of a wavelength. The layout software featured a tool that was used to tune trace lengths within this parameter.

In addition to trace length matching, it was also necessary to shield the ADC clock signals CONVST and RD/SCLK to avoid radiating noise to other sections of the board and ensure that the traces do not run near analog signal paths. This was done via a network of grounded, one-deep vias surrounding the length of the traces to protect them from interference from other traces.

Another consideration was between differential and single ended traces for the more critical signals. Differential traces preserve signal integrity better and are more resistant to EMI interference, but take up space on the PCB. Single ended traces are more prone to noise but take less surface space. Thus, the laser receiver output and the transmitter data output are differential signals to preserve information as much as possible. Both traces are converted to single-ended before reaching the FPGA since the FPGA does not have any differential paired pins. This is accomplished with a balun and matching network of resistors of 50 ohms each to match the FPGA impedance with the 50 ohm differential trace and SMA connector. The differential traces are each 50 ohms, with a trace width of 23.6 mils based on the layer dielectric material and thickness. The footprint of one of these matching networks can be seen to the left of the FPGA connector in Figure 2-3. Additionally, the ground plane on layer two was modified to extend to the edges of the PCB to improving the

impedance matching for the edge-mounted SMA connectors. Edge-mounted SMA connectors were used in good engineering practice because they typically have better performance than other types of SMA mounting, but this benefit was negligible at the operating frequency of this project.

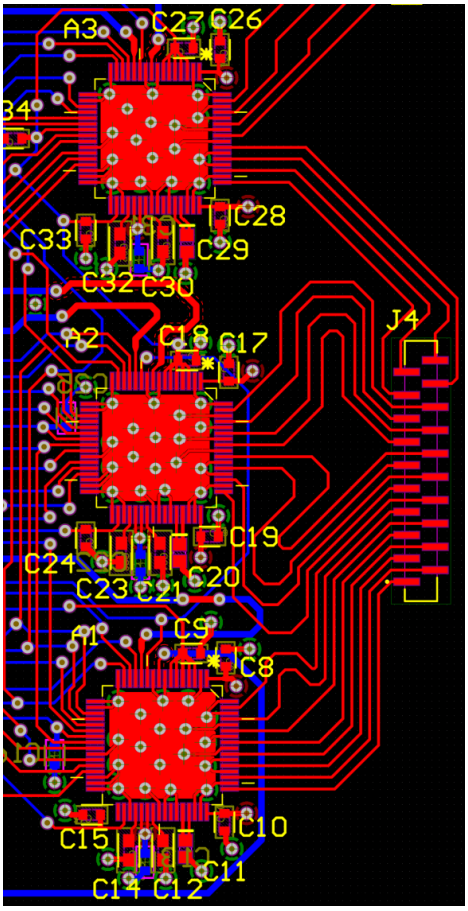


Figure 2-4: ADCS layout on the GS-MSPCB

In order to maintain a stable connection with the ground plane, via connections should be used frequently with a much greater magnitude of capacity than necessary for the actual current. The default in via size for this project was 20 mil holes, with a 40 mil diameter. The smallest possible via option for hole size would be the width of the trace, which was generally 10 mils. To avoid signal interference, traces should not wrap or run closely around vias.

This project utilized three AD7606C-18s, and 8-channel, 8-bit 1 MSPS bipolar input, simultaneous sampling ADC. Its datasheet has extensive layout guidelines that

were implemented here. First, for a system with multiple devices that require analog-to-digital ground connections like this one, a solid ground plane (without splitting between analog and digital grounds) should be used. The layout avoids using one connection for multiple ground pins, and instead each pin has multiple or individual vias to the ground plane. No digital traces run under the ADCs to avoid coupling noise on die. The analog ground plane does run underneath each ADC to prevent noise coupling. The power supply lines to AV_{CC} and V_{DRIVE} use a large trace to provide low impedance paths and reduce the effect of glitches on the power supply lines. AV_{CC} is delivered via a power plane, with stable connections and at least one via per supply pin. The decoupling capacitors are as close as possible to the supply pins and their corresponding ground pins, and on the same side of the board as their pins when possible. The layout between the three ADCs was made symmetrical between the three devices to ensure stable device-to-device performance matching, as can be seen in Figure 2-4.

2.1.4 GS-MSPCB Layout

The final layout in Altium for the first version of the GS-MSPCB can be seen in Figure 2-5. The final dimensions of the GS-MSPCB are 87mm by 53mm. The top left has the power supply input as a terminal block for benchtop testing. Three SMA connectors are edge-mounted to the top edge, connecting 5V and transmitter data to the TX board and the input from the receiver lens. The ADCs are to the right of the board, laid out symmetrically. The FFC connector is on the far right edge, where it leads to the 20 silicon photomultipliers on the OGT. The carrier card will sit on the bottom left, where the FPGA connector is carefully placed underneath to line up with the card.

Figure 2-6 shows the 3D rendering generated by Altium to check the expected size and heights of components and to envision the final product before fabrication and assembly. Figure 2-7 shows the fabricated and assembled GS-MSPCB ready for testing. All the vias are through-hole with no via fill. The layer stack is shown in Figure 2-8 with Elite Materials laminate, EM-827. The core is made of RO4003C. The

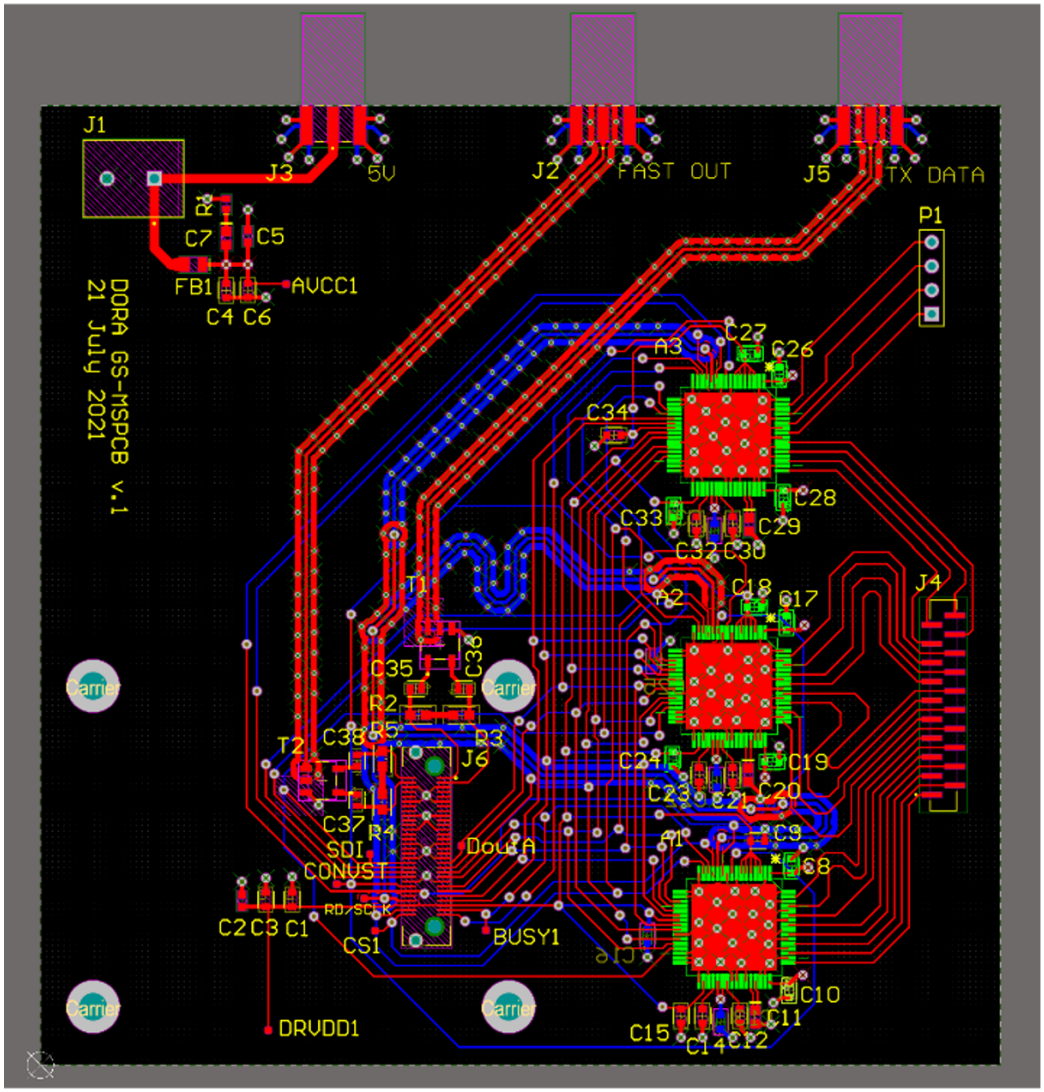
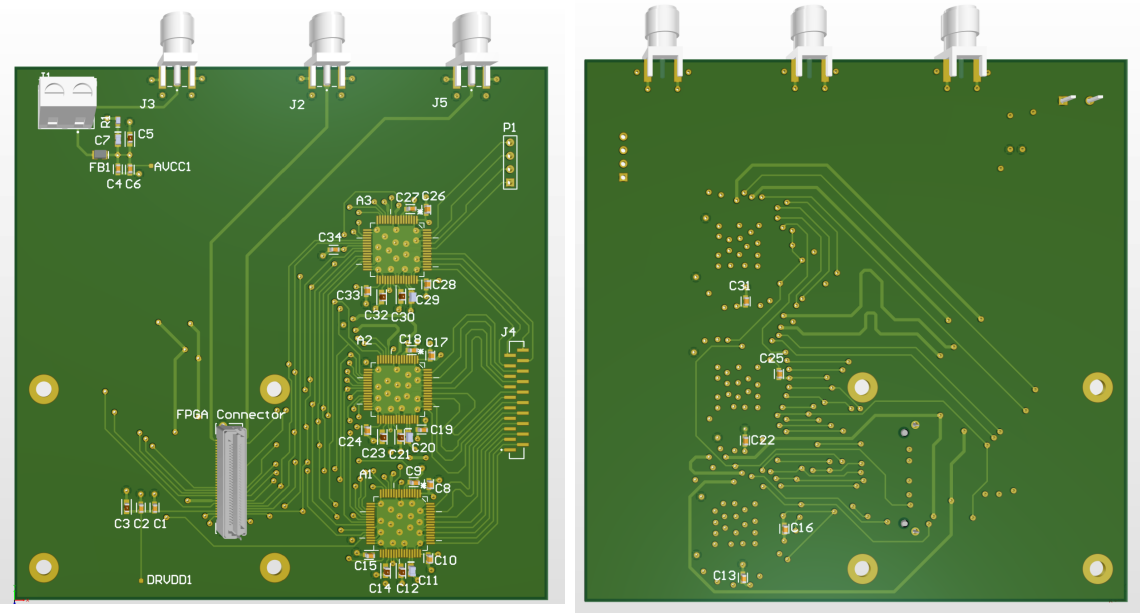


Figure 2-5: GS-MSPCB layout in Altium

prepreg material selection was left to the manufacturer to fulfill the total thickness requirement of 50 mils. The surface finish is ENIG.

2.1.5 Breakout Board Layout

The breakout board was designed to temporarily replace the carrier card on top of the GS-MSPCB in order to facilitate testing. The intended layout for the breakout board is shown in Figure 2-9. A Samtec FPA connector is affixed to the bottom of the board to couple with the GS-MSPCB. An FFC sits on top to connect with the FFC on the GS-MSPCB for the silicon photomultipliers. Three terminal blocks are used



(a) Top face

(b) Bottom face

Figure 2-6: 3D GS-MSPCB rendering in Altium

to break out these two connectors so that each may be wired by hand to an FPGA for software testing. Six U.Fl connectors are attached to the FPGA connector to test the impedance matched inputs and outputs. While U.Fl connectors have a shorter lifespan measured by number of connections, they are smaller and cheaper than SMA connectors. This breakout board was size-limited, so U.Fl connectors were suitable for this application. The breakout board also has U.Fl connectors connected via a short, and open, and 50 ohms impedance for calibration purposes.

Figure 2-10 first shows the top and bottom face of the breakout board as laid out in Altium. The bottom two subfigures show the fabricated and assembled breakout board ready to be used in testing.

The coupled GS-MSPCB and breakout board are shown in Figure 2-11.

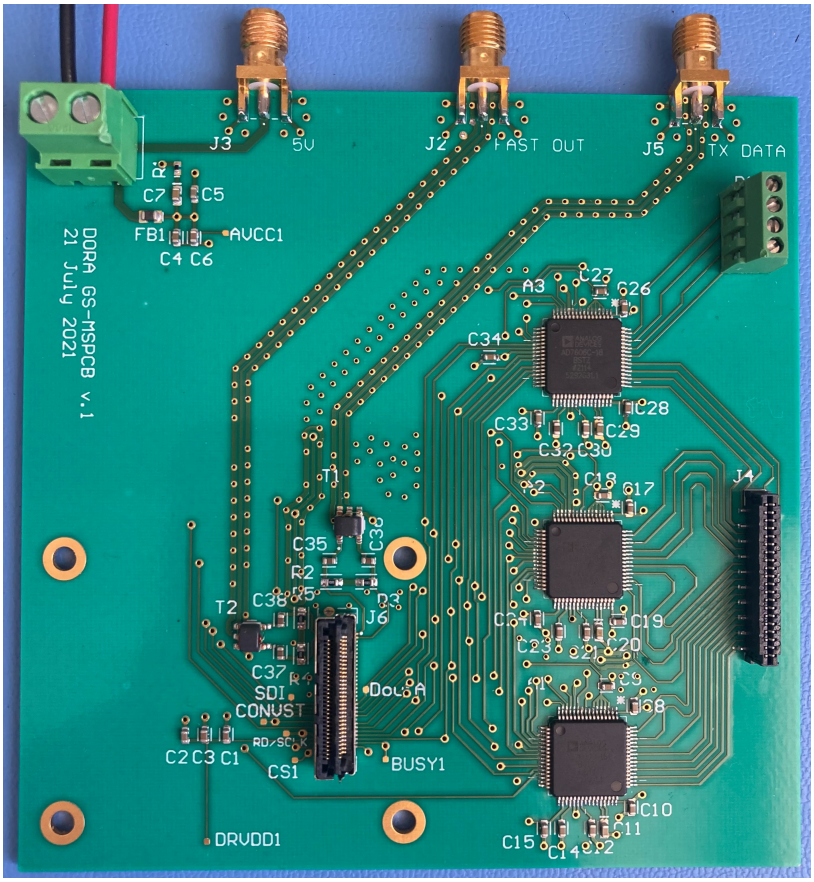


Figure 2-7: Fabricated and assembled GS-MSPCB

2.2 SFP Ethernet-to-Optical Connector

2.2.1 Concept and Requirements

The second half of this project aimed to design an Ethernet-to-optical transceiver device to facilitate the transfer of data from optical ground station to a router, so that the data could be accessed wirelessly. The SFP module is a compact, hot-pluggable network interface module. The SFP interface on networking hardware is a modular slot for a media-specific transceiver in order to connect a fiber-optic cable or sometimes a copper cable. SFP is capable of a 1 Gbit/s data rate, and SFP+ (enhanced small form-factor pluggable) is an enhanced version of the SFP that supports data rates up to 16 Gbit/s. The SFP protocol is common in the telecom industry, so this would provide a seamless method to connect to an optical network. The Small Form Factor Committee regulates the specifications by a multi-source agreement (MSA) for the

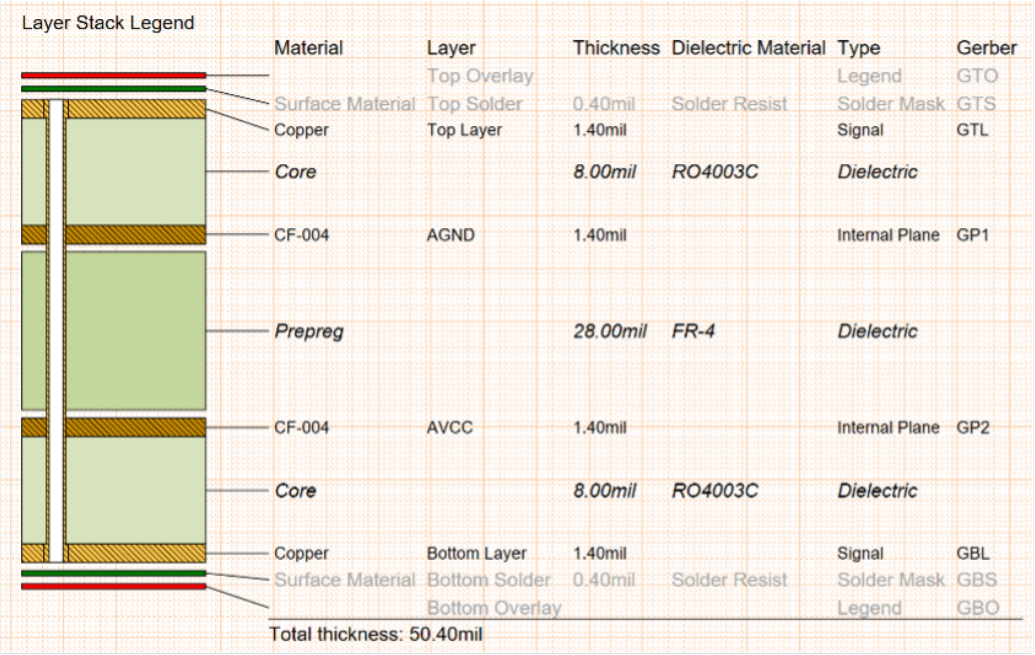


Figure 2-8: Layer stack of GS-MSPCB

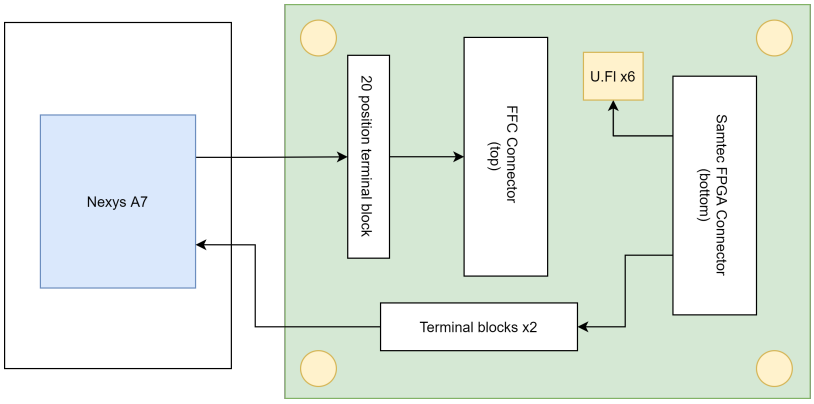
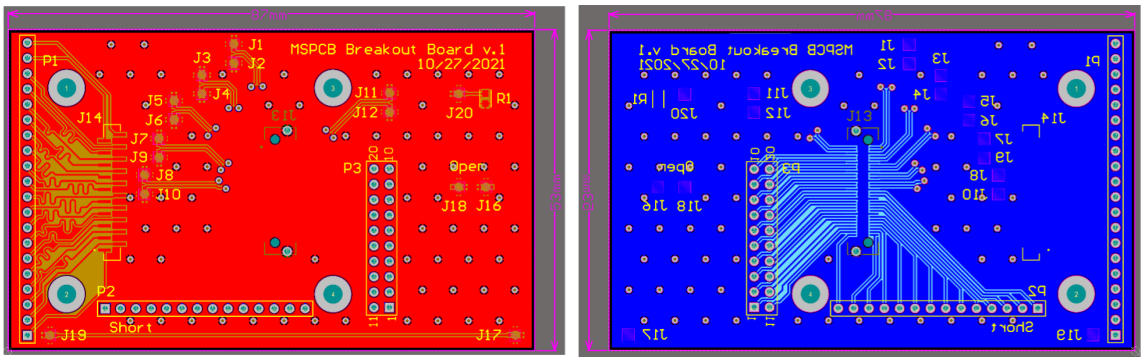


Figure 2-9: GS-MSPCB breakout board block diagram

SFP form factor and electrical interface. [1] The host's network card manages the communication between the host PC (or server) and the transceiver, which is usually PCI-e, or RGMII (for embedded systems). This means the SFP module doesn't need to have any information about host computer or the TCP/IP stack. It just receives the data stream that need to be sent and provides the data that it received.

The goal of this project is to create a small communications device that can fit in an SFP port to act as an Ethernet-to-Optical transceiver. The TCP/IP stack, the device driver, PCIe, the OS kernel, etc do not need to be considered due to the



(a) Board layout, top face

(b) Board layout, bottom face

(c) Assembled board, top face

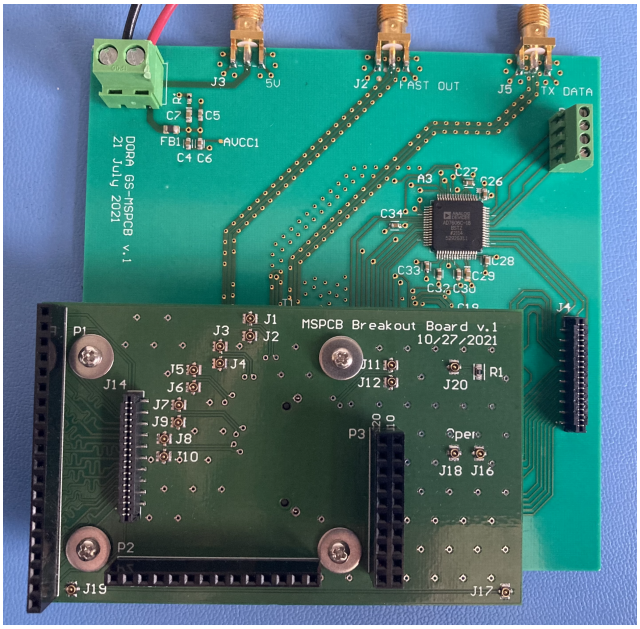
(d) Assembled board, bottom face

Figure 2-10: Breakout board in design stages

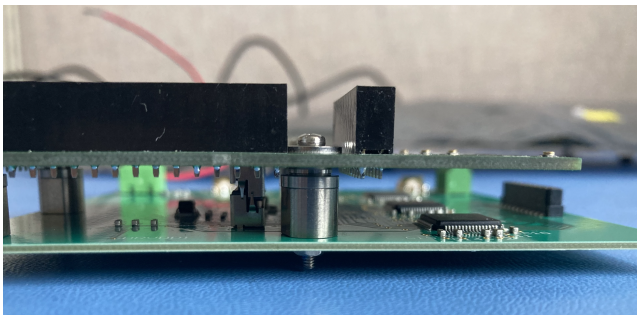
design of the SFP protocol, which leaves the network card to manage these instead. Ideally, the FPGA PCB and any necessary components would fit in the SFP form factor. The FPGA will be responsible for managing the Ethernet communication, and it will have Linux integrated into the system for more flexibility and capability in communication and data processing.

There are two options to implement a processor on an FPGA. The first is to select an FPGA that is paired with a processor, such as the models in the Zynq series that are paired with an ARM processor. The other option is to include a soft-core processor, such as the Microblaze processor for Xilinx hardware. This processor is programmed on the actual FPGA and can be optimized for the minimum requirements for the task at hand to conserve space and power.

In order to implement Linux on an FPGA, there are many available options with varying levels of difficulty and cost. These methods include using PetaLinux, Yocto, open source Linux, commercial Linux, and real-time Linux. PetaLinux tools make it



(a) Top view of breakout board mounted on GS-MSPCB



(b) Side profile of breakout board mounted on GS-MSPCB

Figure 2-11: Breakout board mounted on GS-MSPCB

easy for developers to configure, build and deploy essential open source and systems software to Xilinx silicon. The Yocto Project (YP) is an open source collaboration project that helps developers create custom Linux-based systems. The PetaLinux tools are built on top of the YP infrastructure. This project selected PetaLinux for its wide range of tools to configure Linux. [2]

Figure 2-12 shows the intended use of the SFP+ device to connect the OGT to an SFP switch. This switch will be connected to a Wifi-6 router with a 10G SFP+ port. At the time of this research, these routers were surprisingly rare. The RT-AX89X has the necessary 10G SFP+ port, and was the only router available on the market

with this port. The router enables data from the OGT to be accessed wirelessly via laptop.

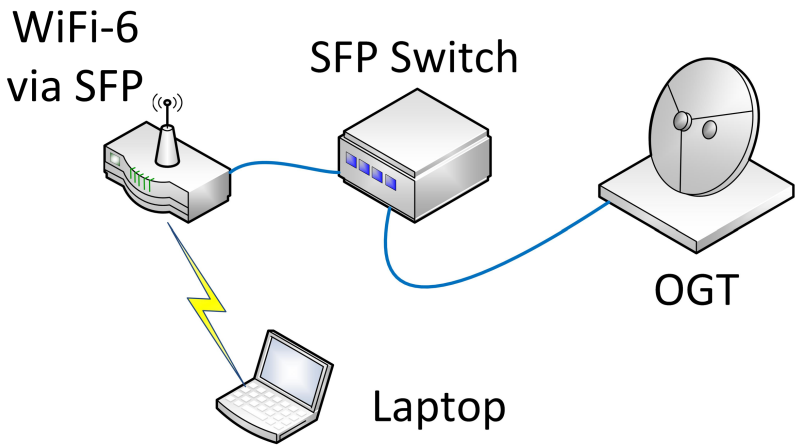


Figure 2-12: Ethernet-to-optical transceiver system implementation

2.2.2 FPGA/SOM Model Comparisons and Selection Considerations

Each FPGA and SOM come with their own strengths and weaknesses that must be evaluated for their suitability to the project at hand. Below are the models considered for this project, and the considerations that went into the final selections. Xilinx is the main FPGA manufacturer considered, and they have several series and models available with different features.

The 28nm 7 series architecture made several improvements in power reduction, price performance, and system performance over the previous 6 series. The 20nm Ultrascale architecture improves integration and capability while delivering ASIC-class system level performance for projects with massive I/O and memory bandwidth, massive data flow, DSP, and packet processing. The 16nm Ultrascale+ architecture has greater system-level performance/watt over 28nm devices, far more systems integration and intelligence, and the most security and safety. Within each of these architectures, there are four devices available to choose from. The Artix has the lowest price and power for high volume and consumer applications, the Kintex has the

best price per performance, and the Virtex has the highest performance and capacity. The Zynq family integrates an ARM-based processor with an FPGA for better performance than with the MicroBlaze soft-core, and leaves programmable logic still available to use for register-transfer level (RTL) modules.

Trenz Electronic develops, manufactures, integrates and sells FPGA and system-on-chip (SoC) modules with a focus on application specific hardware design language (HDL) and FPGA design and hardware and software development. All of their modules are developed and manufactured in Germany. Several different modules from Trenz were considered for their various capabilities.

The TE0725 is a small Artix-7 100T FPGA with 8MB HyperRAM and an optional fiber optical adapter. However, the FPGA on this board does not have any gigabit transceiver (GTP)s that are needed for the high speed communication in this project. The fiber optic (POF) module on these boards is simply connected to regular high range pins on the FPGA. The maximum data rate supported by the POF transceiver is 250 MB/s, but the actual data rate would probably be lower due to the use of the high range pins. This board would be challenging to use due to limited data rate and lack of previously existing communications layer.

The TE0741 is another SOM, which has a Kintex-7 device with 8 GTX transceivers. All 8 are wired directly to connectors JM1 and JM3, and there are 4 clocks that are associated with the transceivers. Two of the clocks are connected directly to JM3, while the other two are derived from the clock generator. However, the TE0741 does not support Linux since there is not enough BRAM to run it. As an alternative, the TE0841 has a Kintex Ultrascale FPGA, which is more powerful and thus able to outperform this issue, but would need an implementation of the Microblaze processor.

Turning to other options, the TE0713 has a small form factor (4x5cm), 100T and 200T size options, 200 MHz fabric clock, 1 GB DDR3L RAM, and 32 MB QSPI FLASH. The TE0712 has a small form factor (4x5cm), 100T and 200T size options, 50MHz fabric clock, 1 GB DDR3 RAM, 32 MB QSPI FLASH, and an on-board Ethernet PHY, but comes at a higher cost and lacks the necessary PCS/PMA IP module. The TE0714 has the smallest form factor (4x3cm), a size of 50T, 25 MHz

fabric clock (which would need to be multiplied internally), no RAM, 16 MB QSPI FLASH, and has the lowest cost of the three. In terms of clock speed, the TE0714 has one 125 MHz oscillator for the transceiver clock, or an external clock could feed the internal clock via connector. The TE0714, TE0712, and TE0713 all have transceiver pins that could be used for the intended high speed data transfer. Trenz offers base boards as a carrier for their SOM cards that include an SFP connector, such as the TEBA0841 for 4x5 SOMs.

During research, an implementation very similar to the desired end product was found [9]. It was built with a Zynq UltraScale+ on the ZCU102, which makes it easier to implement Linux on the FPGA with the built-in processor rather than the Microblaze soft-core. Thus, an UltraSOM+ model from Trenz was also considered, such as the TE0808.

Due to budget constraints and manufacturing delays, experimentation was carried out on a VC707 Virtex-7 evaluation kit already available in the lab from previous work. This meant a soft-core MicroBlaze processor would need to be implemented instead of using the processor included on a Zynq chip. Upon completion of a successful design, this could be scaled down to a less powerful, less expensive, smaller module with lower power consumption that still fit size requirements for long-term implementation, with a device such as the TE0841. The TE0808 would also be a good choice as a Zynq UltraSOM+ card to quickly implement the existing design that is made for the separate processor.

IPs and Vivado Block Diagram

The DORA payload uses Ethernetlite IP, which implements a simple AXI4 interface without any streaming ports. This directly connects the Ethernetlite to the MicroBlaze's AXI Interconnect and avoids additional complexities, but the Ethernetlite only supports 10/100Mbps. For the 10G Ethernet MAC, the interface is more complicated due to the higher data rate. In order to connect the Ethernet Subsystem to the MicroBlaze processor (MicroBlaze), the AXI direct memory access (DMA) is needed.

The block diagram for the SFP system is shown in Figure 2-13. The MicroBlaze

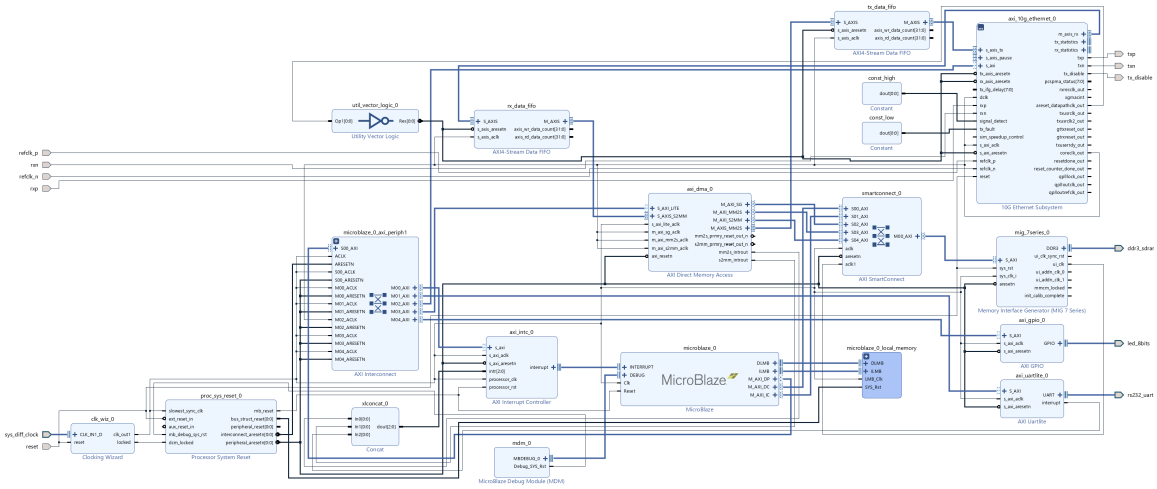


Figure 2-13: System block diagram of IP connections in Vivado

processor has several components necessary to implement the processor at the center of the design. The main MicroBlaze block connects to its local memory block and the debug module, with inputs and outputs for the AXI communication with other blocks.

The Interconnect and Smart Connect IP enable the connection of heterogeneous main/secondary AXI4-Stream protocol compliant endpoint IP. Each interconnect can route connections between multiple main and secondary blocks at a time.

The 10G Ethernet Subsystem IP integrates both the Ethernet 10G MAC and the Ethernet 10G PCS/PMA and is used to connect the SFP+ with the appropriate protocol. The high speed data streaming is supported by the MIG, AXI DMA and the FIFO buffer. The Memory Interface Generator (MIG) combines the controller and physical layer (PHY) for interfacing the design and the AXI4 secondary interfaces to the DDR3 SDRAM device. The AXI DMA provides high-bandwidth direct memory access between memory and AXI4-Stream-type target peripherals. The AXI4-Stream Data FIFO allows memory mapped access to a AXI4-Stream interface.

Once the system architecture was built, this was built in Vivado as a bitstream file and hardware .xsa file to be exported to Petalinux for the next step of the project.

```
julia@julia-VirtualBox:~/sfp$ petalinux-config --get-hw-description /home/julia
[INFO] Sourcing buildtools
INFO: Getting hardware description...
INFO: Renaming greetings_earth_wrapper.xsa to system.xsa
[INFO] Generating Kconfig for project
INFO: Updating the flash partition size to 0x1360000 bytes, based on the bitstre
am in the XSA
[INFO] Menuconfig project


*** End of the configuration.
*** Execute 'make' to start the build or try 'make help'.

[INFO] Sourcing build environment
[INFO] Generating u-boot configuration files
[INFO] Generating kernel configuration files
[INFO] Generating kconfig for Rootfs
[INFO] Silentconfig rootfs
[INFO] Generating plnxtool conf
[INFO] Generating workspace directory
```

(a) Running petalinux-config command

```
julia@julia-VirtualBox:~/sfp$ petalinux-build
[INFO] Sourcing buildtools
[INFO] Building project
[INFO] Sourcing build environment
[INFO] Generating workspace directory
INFO: bitbake petalinux-image-minimal
NOTE: Started PRServer with DBfile: /home/julia/sfp/build/cache/prserv.sqlite3,
IP: 127.0.0.1, PORT: 34667, PID: 7228
Loading cache: 100% |                                                | ETA:  --:--:--
Loaded 0 entries from dependency cache.
Parsing recipes: 100% |#########################################| Time: 0:04:25
Parsing of 3476 .bb files complete (0 cached, 3476 parsed). 5133 targets, 693 sk
ipped, 0 masked, 0 errors.
NOTE: Resolving any missing task queue dependencies
Initialising tasks: 100% |#####################################| Time: 0:00:02
Checking sstate mirror object availability: 100% |#############| Time: 0:07:34
Sstate summary: Wanted 153 Found 12 Missed 141 Current 970 (7% match, 87% comple
te)
NOTE: Executing Tasks
NOTE: Tasks Summary: Attempted 3506 tasks of which 3019 didn't need to be rerun
and all succeeded.
INFO: copy to TFTP-boot directory is not enabled !!
[INFO] Successfully built project
```

(b) Running petalinux-build command

```
julia@julia-VirtualBox:~/sfp$ petalinux-package --boot --fpga /home/julia/sfp/pr
oject-spec/hw-description/greetings_earth_wrapper.bit --uboot --kernel --force
[INFO] Sourcing buildtools
WARNING: Auto detecting MMI file with XSA
INFO: Creating download.bit...
INFO: Fpga bitstream: /home/julia/sfp/project-spec/hw-description/greetings_eart
h_wrapper.bit
INFO: Fpga bitstream MMI file: /tmp/tmp.8iLdtngpye/greetings_earth_wrapper.mmi
INFO: Fsbl file: /home/julia/sfp/images/linux/fs-boot.elf
INFO: Output download.bit: /home/julia/sfp/images/linux/download.bit
INFO: Getting system flash information...
INFO: User hasn't specified flash size, will use the auto detected system flash
size: 0x20 MBytes.
INFO: User hasn't specified flash interface, will use the auto detected one BPIx
16.
INFO: Add bitstream "/home/julia/sfp/images/linux/download.bit" to 0.
ERROR: Size of bitstream "/home/julia/sfp/images/linux/u-boot-s.bin" is 401564 l
arger than the boot partition size 0x40000.
```

(c) Running petalinux-package command

Figure 2-14: Command sequence excerpt for using PetaLinux tools

2.2.3 Petalinux Functions and Design

In order to build Linux on the FPGA system, PetaLinux tools provide an embedded Linux development solution, including for MicroBlaze designs implemented in fully FPGA chips. PetaLinux runs on varieties of Ubuntu, Red Hat and CentOS. Thus, a virtual machine running Ubuntu 18.04.4 was set up with Oracle VM VirtualBox Manager. The Xilinx PetaLinux Tools Documentation Reference Guide [16] details the steps necessary to utilize PetaLinux. The first step is to configure the environment

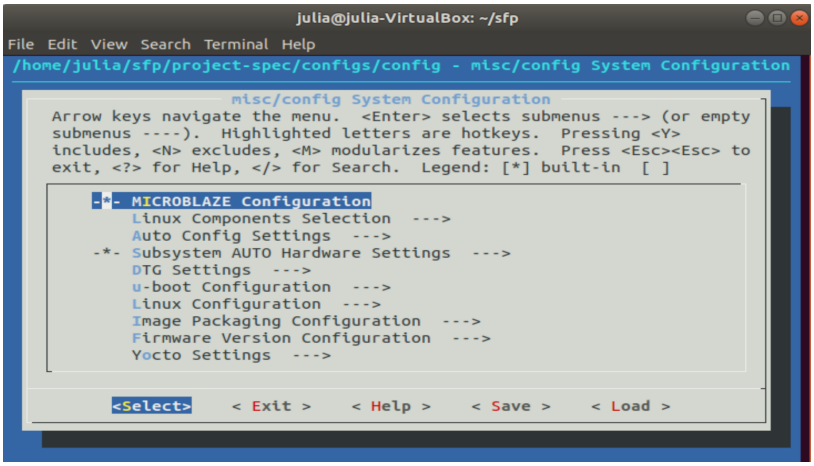


Figure 2-15: PetaLinux configuration menu

by installing PetaLinux, downloading the extensive dependencies, and setting the bash and source settings.

The next step is to begin a new project or use a reference design provided in a board support package (BSP) available from the Xilinx website. Unfortunately, a BSP was not available for this FPGA model so the project was built from scratch.

The next three steps create a kernel, file system, first stage and second stage boot loaders, and device tree compiled and ready to be deployed to the hardware target. First, running `petalinux-config` with the appropriate argument and path as shown in Figure 2-14a opens the configuration menu for the system shown in Figure 2-15. For this project, all options were left to default. Next, `petalinux-build` does not require any arguments, and sets the files based on the configuration from the previous step as shown in Figure 2-14b. Finally, `petalinux-package` should create the necessary BOOT.bin and U-boot files to transfer to the SD card. However, the error message shown in Figure 2-14c was unavoidable despite many different combinations of command arguments. The error message was "Size of bitstream "/home/julia/sfp/images/linux/u-boot-s.bin" is 401564 larger than the boot partition size 0x40000." Multiple settings, memory allocations, and partition sizes were implemented with similar results. It is possible that the Virtex-7 is not large enough to hold Linux, which could be confirmed by building the system in Vivado for a different FPGA model and trying again in PetaLinux. This stalled the project indefinitely

until time ran out, and will need to be addressed in future work. The final step would be to move the generated BOOT.bin and image.ub files onto an SD card to be connected to the FPGA.

Chapter 3

Implementation

3.1 GS-MSPCB

3.1.1 Analog Testing

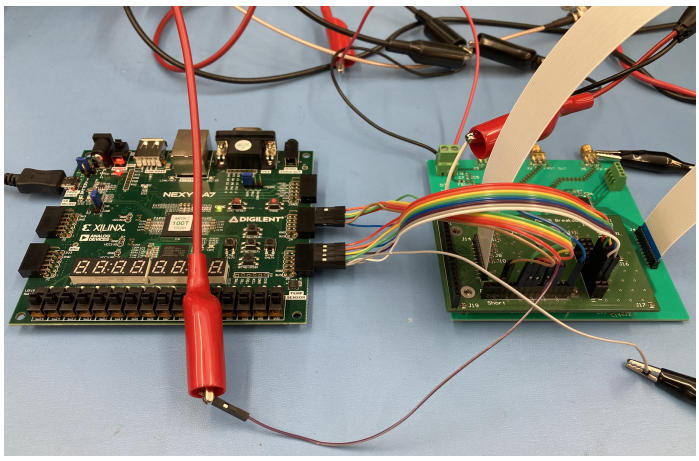
Once the PCB was fabricated and assembled, a series of benchtop tests were carried out to ensure expected functionality of the design. One of the first checks was to ensure that the carrier card fit properly on the GS-MSPCB. The board lined up well between the FPGA connector and the four standoffs that securely hold the two boards together, as can be seen in Figure 2-11.

The next test was to connect 5V to the input block to check the connections and ensure all nodes were at the correct voltage as expected without any components becoming unusually hot or sustaining damage. This test was repeated with 3.3V from the FPGA. Additionally, all ground nodes were tested as well to make sure all components were properly grounded.

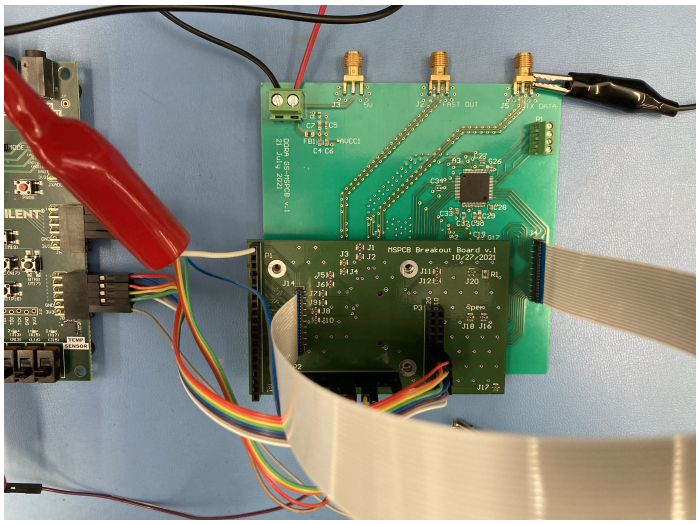
The next step for these tests would be to measure impedance matching with a Vector Network Analyzer (VNA). Due to time constraints, these tests were not carried out during the project duration, but the breakout board was fabricated to make this experiment possible. The breakout board contains three traces dedicated to calibration. The first one provides a short connection via a quarter-wavelength 50 ohm trace between two U.Fl connectors. The second is an open trace via two

U.Fl connectors mounted to the board with appropriate grounding but otherwise unconnected. The third calibration trace for 50 ohm impedance matching consists of one U.Fl connector connected to a 50 ohm resistor. These traces are intended to calibrate the VNA. The VNA may then used to measure the impedance matching for traces connecting the transmitter and receiver data lines, since accurate data transfer is essential to the system.

3.1.2 Digital Testing



(a) Connecting Artix-7 FPGA to test setup



(b) GS-MSPCB test wiring

Figure 3-1: GS-MSPCB test setup and lab bench configuration

One of the central functions of the GS-MSPCB is the analog-to-digital conversion

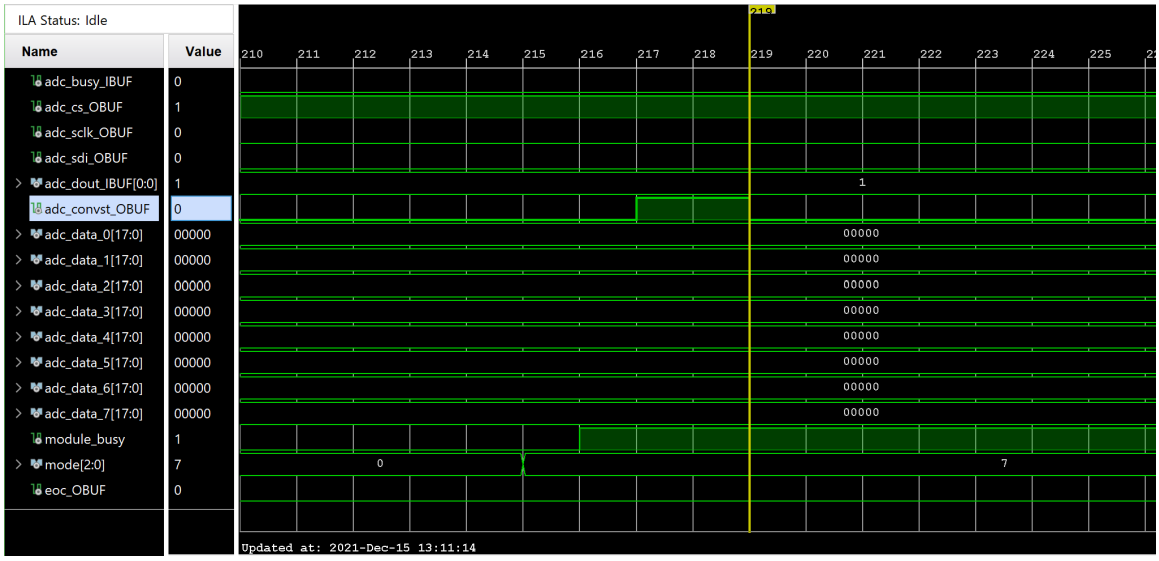


Figure 3-2: ILA results from testing the GS-MSPCB

of the array of SiPMs on the optical ground terminal. In order to test the ADCs that perform this function, a Nexys A7 FPGA was programmed with a design previously written for the AD7606. The setup for this test may be seen in Figure 3-1. An external power supply provided 5V and the FPGA provided the 3.3V logic level voltage. The FPGA is connected by individual pins to the breakout board headers. A function generator was connected to simulate the SiPM outputs. The function generator could also be replaced by an actual SiPM, available in the lab, for future experiments. This input is passed to one of the breakout board headers that is connected to the FFC connector on the breakout board, which is wired to the FFC connector on the GS-MSPCB. This data is then converted by the ADCs and read back by the FPGA through the FPGA connector. The ADCs respond to the input control signals provided by the FPGA. The input and output signals are visualized with the integrated logic analyzer (ILA) in Vivado. An example of results can be seen in Figure 3-2.

It can be noted in Figure 3-2 that the `adc_data` channels are consistently reading 0's despite the input of non-zero data, which was not the expected behavior. In addition, the power consumption was expected to be 115 mW maximum per ADC according to the datasheet. However, the power consumption was rapidly varying in

the Watt range, with a very high current draw for the entire board. This concerning behavior could be temporarily mitigated by shorting the pins of the ADC connected to coupling capacitors, but when the "convert start" signal, `CONVST`, would transition to begin the data conversion, the FPGA did not receive a busy signal back from the ADCs.

Investigation of these issues revealed that the ADCs were soldered to the board ninety degrees off from the correct orientation since the chip form factor is rotationally symmetric. This error could have been avoided by noting the orientation on the schematic for assembly. It took several days to have the ADCs de-soldered and re-soldered in the correct orientation due to the size and quantity of the pins, which was not completed until after the project timeline had expired.

3.2 SFP Ethernet-to-Optical Connector Results

In pursuit of an SFP Ethernet-to-Optical connector, a functional FPGA system architecture with a soft-core MicroBlaze processor was developed. The next step was to build Linux on this processor using PetaLinux tools. This half of the project was stagnated by the error message returned when `petalinux-package` was run when using PetaLinux tools as discussed in Section 2.2.3. This command should create the necessary BOOT.bin and U-boot files to transfer to the SD card. However, the error message shown in Figure 2-14c was unavoidable despite many different combinations of command arguments. Multiple settings, memory allocations, and partition sizes were implemented with similar results. Methods to move past this block are discussed in Section 4.2 that could not be pursued in the time span of this project.

Chapter 4

Conclusions

4.1 Contributions

In summary, this work has resulted in a fabricated and assembled PCB that is the core of the optical ground station for the DORA project. Initial testing has indicated that the PCB design is sound and no layout mistakes were made. A thorough test procedure has been constructed in order to test ADC function as soon as the PCB assembly error can be corrected.

In addition, this work has made significant progress on the implementation of a Ethernet-to-Optical transceiver device. The high data rate requirement imposes large constraints on this challenge that is lacking in similar previous work. In particular, the lack of device heritage for the FPGA models that were available due to manufacturing holds caused a considerable barrier. Building Linux on an FPGA without a premade BSP can result in a very long chain of errors to address that extended beyond the timeline of this project. In addition to documentation on streamlining the process for creating this system, potential solutions and next attempts have been detailed in Section 4.2.

4.2 Future Work

For the GS-MSPCB, the next step is to complete testing of the ADCs with the already configured test setup once their orientation has been corrected. Following this, the next design iteration will need to include biasing and monitoring for the TIAs with the SiPMs, as well as an additional connector. This connector will transmit the control signals for the FSM carrier board, and has not been integrated yet due to the design of the carrier card that sits on the GS-MSPCB. The carrier card's first version was manufactured with as few layers as possible to save cost, but this did not include connections for the FSM from the FPGA to the FPGA connector.

In regards to the SFP+ transceiver device, there are several ways to circumvent the current block in development. With the work done here, future development should proceed smoothly by avoiding the pitfalls already discovered. The first method is to acquire an FPGA in the Zynq family so that it has an ARM processor separate from the FPGA. This would allow the quick implementation of an already existing example project that centers around the Zynq processor. Another option is to choose another Xilinx FPGA that has an existing BSP. This avoids the need to go through the entire PetaLinux design flow by supplying a solution that should be ready to boot. The third option is to back away from Linux and turn to a baremetal solution. If the requirements for the transceiver became more defined, software could be written directly in Vitis and loaded onto the FPGA instead of building an entire OS.

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