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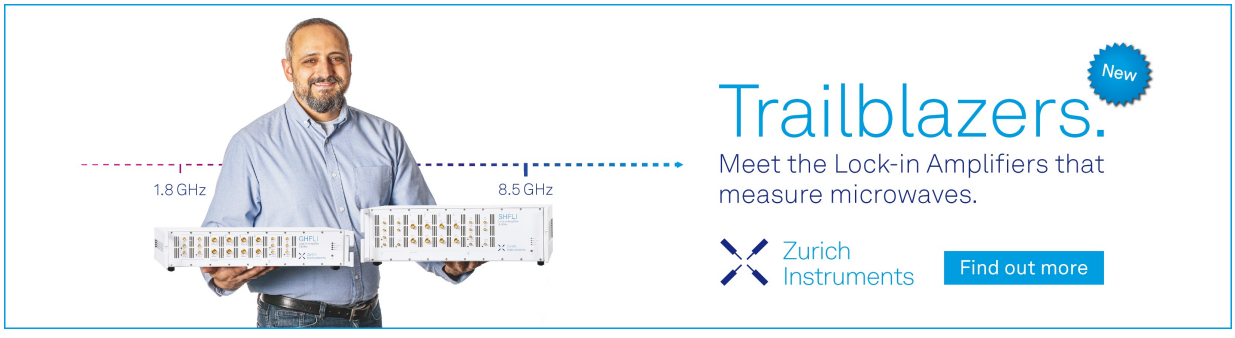
Ethan S. Lee, Jungwoo Joh, Dong Seup Lee, et al.



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Ethan S. Lee,[1,a)] Jungwoo Joh,[2] Dong Seup Lee,[2] and Jesús A. del Alamo[1]

AFFILIATIONS

[1]Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, USA
[2]Analog Technology Development, Texas Instruments, Dallas, Texas 75243, USA

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[a)]**Author to whom correspondence should be addressed:** ethanlee@mit.edu

ABSTRACT

In this Letter, we experimentally investigate the impact of gate geometry on forward operation of Schottky-gate p-GaN high electron mobility transistors (HEMTs). In particular, we analyze devices with changing gate-metal/p-GaN junction area and p-GaN/AlGaN/GaN heterostructure area in the linear regime. These devices exhibit unique threshold voltage and subthreshold swing scaling dependence with gate geometry that is in contrast with classic field-effect transistors. On the other hand, peak transconductance and ON resistance are found to scale classically. We find that these results arise from the fact that with a Schottky contact to the p-GaN layer, under steady-state conditions, the p-GaN layer voltage is set by current continuity across the gate stack. Furthermore, a detailed scaling study of the gate current reveals that current flow across the p-GaN/AlGaN/GaN heterostructure is not uniform—instead, it preferentially flows through the ungated portion of the p-GaN layer. Our study concludes that in Schottky-type p-GaN gate HEMTs, the respective areas of two junctions constitute an additional design degree of freedom to fine-tune device performance.

In recent years, there has been growing focus on enhancement-mode GaN high electron mobility transistors (HEMTs) for power electronic applications. Among several possible designs, inserting a p-doped GaN layer in the gate stack of an AlGaN/GaN HEMT has been found to be particularly promising. p-GaN HEMTs, as they are commonly known, are rapidly attracting commercial interest for power management applications due to simpler circuit design and inherently safe operation that stems from their positive threshold voltage, while preserving the efficiency and high performance associated with the AlGaN/GaN heterostructure.[1–4]

In p-GaN HEMTs, the gate metal/p-GaN junction can either be designed to be an Ohmic contact or a Schottky junction depending on material choices and processing conditions. In the case of an Ohmic gate contact, in what is known as a gate injection transistor (GIT), the gate voltage needs to be kept within a narrow range or large gate leakage current flows with undesirable consequences.[3] On the other hand, a Schottky junction acts as a reverse biased diode when the device is turned on, substantially limiting the gate leakage current. Therefore, growing emphasis is being placed on Schottky-gated p-GaN transistors for power applications.

In a Schottky-type p-GaN HEMT, the gate stack consists of two diodes in a back-to-back configuration: the metal-gate/p-GaN Schottky junction and the p-GaN/AlGaN/GaN heterostructure, which acts as a p–i–n diode.[5–7] In consequence, the p-GaN layer is electrically floating leading to complex and hard to model gate operation. In this transistor structure, a design degree of freedom is the relative area of the two junctions in the gate stack. It has been found that to limit leakage through the p-GaN sidewall as well as to improve gate reliability, a portion of the p-GaN layer must be left uncontacted by the gate metal.[8–11] However, the broader impact of changing the relative areas of the two junctions on device operation is not well understood. Addressing this void is the goal of this work.

In this Letter, we study p-GaN HEMTs with different gate geometries. We find unusual dependences of device figures of merit—threshold voltage and subthreshold swing—on gate geometry. These dependences are consistent with gate electrostatics, which are determined by a current continuity requirement across the gate stack rather than by a capacitive divider. An additional factor in the impact of gate geometry is an anomalous scaling of the gate current with the length of the uncontacted portion of the p-GaN layer. Our results should be

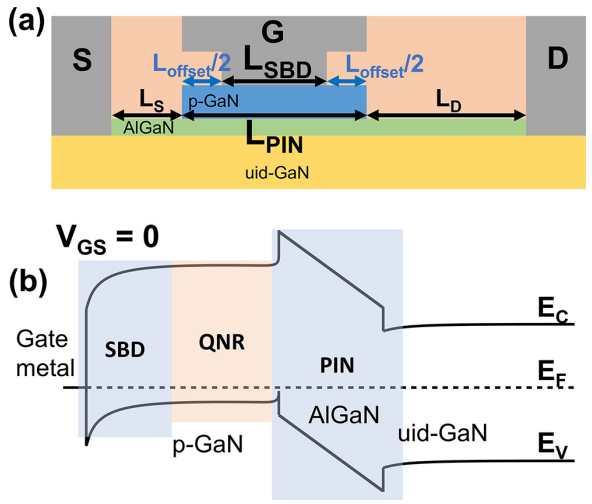


FIG. 1. (a) Schematic cross section of devices studied here. All dimensions are fixed across devices except L_{SBD}, L_{PIN}, and therefore, $L_{offset} = L_{PIN}$-L_{SBD}. (b) Band diagram at $V_{GS} = 0$ V across the gate stack.

instrumental in developing a deeper understanding of p-GaN HEMT device physics, reliability, and the construction of device models for circuit design.

A schematic cross section of the studied devices is shown in Fig. 1(a), and an energy band diagram at $V_{GS} = 0$ V across the intrinsic gate stack is depicted in Fig. 1(b). These devices are pre-production prototype p-GaN-gated HEMTs grown on a Si substrate. Devices with different gate dimensions are studied. The source to p-GaN edge distance, L_S, the drain to p-GaN edge distance, L_D, and the width of the device, W, are identical across all devices. The length of the gate-metal/p-GaN junction, L_{SBD}, and the length of the p-GaN/AlGaN junction, L_{PIN}, are varied across devices, where L_{PIN} is always greater than L_{SBD}. We define the length of the uncontacted portion of the p-GaN layer, $L_{offset} = L_{PIN} - L_{SBD}$. This offset is split evenly on either side of the gate metal. Devices with L_{SBD} from 0.7 to 10 μm and L_{offset} from 0.4 to 1.9 μm in 0.3 μm steps are studied. These devices represent an area ratio between the two junctions from nearly 1 to 3.7.

The drain current, I_D, from linear-regime transfer sweeps ($V_{DS} = 50$ mV) for devices with the same $L_{SBD} = 0.7$ μm but changing L_{PIN} is shown in Fig. 2(a). There is a clear positive shift in the threshold voltage, V_t, as L_{PIN} increases. For a uniform definition across devices with widely different gate dimensions, we define V_t as the value of V_{GS} for which the product of I_D and the channel length, L_{PIN}, are constant and equal to 10^{-8} A × mm. This corresponds to a channel density on the order of 10^9 cm^{-2}. Figure 2(b) shows V_t defined this way as a function of L_{PIN} with L_{SBD} as a parameter. A remarkable geometrical dependence is observed whereby for a constant L_{SBD}, V_t rapidly shifts positive as L_{PIN} increases. The change of V_t with L_{PIN} is fairly similar across devices with different L_{SBD}. This is all unlike ideal metal-oxide-semiconductor field-effect transistors (MOSFET), where in the absence of short channel effects, V_t should be largely independent of L_{PIN}. This puzzling gate geometry dependence is also shown as a

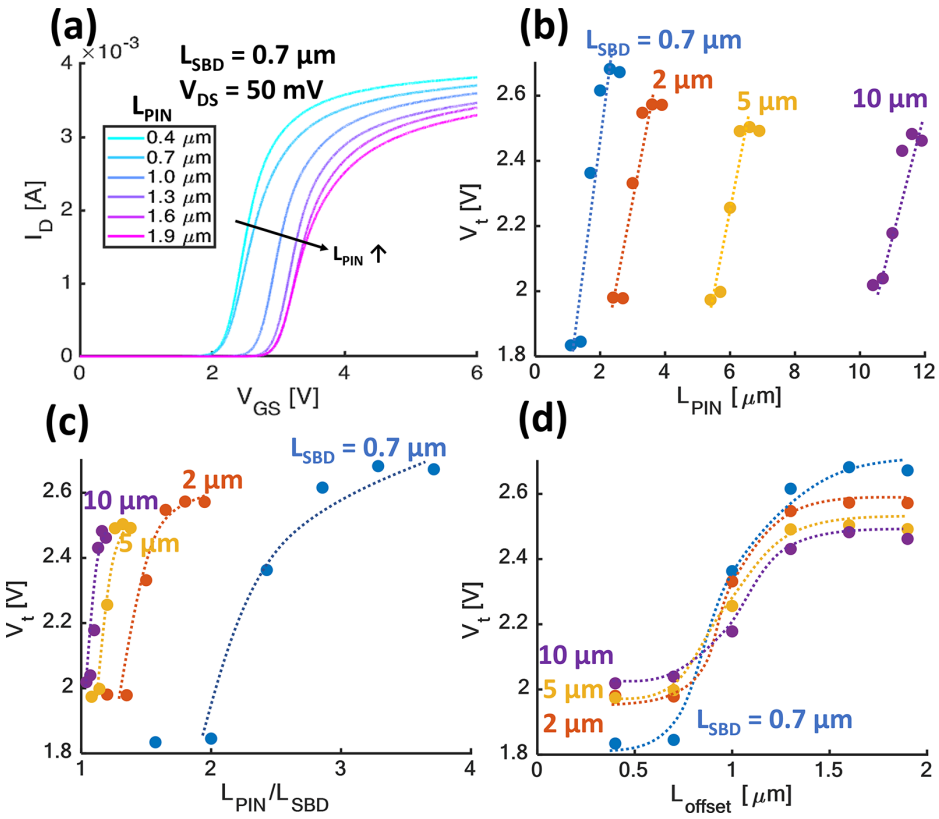


FIG. 2. (a) Transfer sweep with $V_{DS} = 50$ mV for devices with $L_{SBD} = 0.7$ μm and different values of L_{PIN}. As L_{PIN} increases, the curves shift positive. (b) V_t extracted at $I_D \times L_{PIN} = 10^{-8}$ A × mm for all devices studied vs L_{PIN}. (c) V_t in (b) plotted instead vs L_{PIN}/L_{SBD}. No universal ratio dependence arises. (d) V_t vs offset length, L_{offset}.

function of the ratio of the two junctions in Fig. 2(c) and L_{offset} in Fig. 2(d) and discussed in detail below.

Figure 3(a) shows the subthreshold swing (SS) at the same bias point of V_t for all devices. In an ideal MOSFET without short-channel effects, SS is independent of the gate geometry. In contrast to this, in our devices, we also find a pronounced geometrical dependence. For constant L_{SBD}, SS decreases quickly as L_{PIN} increases. This dependence is, however, not monotonous: the value of SS depends not only on L_{PIN} but also on L_{SBD}, something that is not expected. This is all inconsistent with normal FET behavior.

These observations around threshold are in interesting contrast with the electrical characteristics for the same devices in the ON regime, that is, above threshold. Figures 3(b) and 3(c) show the evolution of the linear regime peak transconductance, $g_{m,peak}$, and ON-resistance, R_{on}, respectively, for all transistors. These data reveal classic transistor scaling behavior, where $g_{m,peak}$ goes as $1/L_{PIN}$ and R_{on} is linear on L_{PIN}, just as expected.[12]

Our study of gate geometry scaling of transistor electrical characteristics reveals an interesting behavior. While the linear-regime peak transconductance and ON-resistance, extracted above threshold, follow classical transistor scaling, the threshold and subthreshold figures of merit feature geometrical dependences with no clear analogues to conventional FETs. What is behind this strange geometrical dependence?

The floating p-GaN node in the back-to-back diode configuration of the gate and an unexpected non-uniform gate current density distribution across the PIN barrier are responsible for the behavior that we observe.

In steady state, the potential at the p-GaN node is established by the need to maintain current continuity across the PIN and SBD junctions.[13,14] Under the assumption that the p-GaN layer is thick enough to support a quasi-neutral region between the two barriers, the applied gate-to-channel voltage must be dropped across the SBD and the PIN barriers such that the current flow across the diodes, I_{SBD}, and I_{PIN}, respectively, is equal [Fig. 1(b)]

$$V_{GS} = V_{SBD} + V_{PIN}, \quad (1)$$

$$I_G = I_{SBD} = I_{PIN}. \quad (2)$$

Furthermore, the channel density, n_{2DEG}, is controlled by the voltage drop across the p-GaN/AlGaN/GaN heterostructure, V_{PIN}.[15,16] An important conclusion of this is that at a constant n_{2DEG}, or $I_D \times L_{PIN}$, V_{PIN} is the same across all devices.

This realization explains the V_t dependence on L_{PIN} at fixed L_{SBD} of Fig. 2(b). For constant $I_D \times L_{PIN}$ and, therefore, constant V_{PIN}, a longer L_{PIN} implies larger I_{PIN} and, therefore, larger I_{SBD}. Since L_{SBD} is fixed and the SBD is reverse biased, this demands a larger V_{SBD} and all together a larger V_{GS}, consistent with experiments.

A consequence of this hypothesis is that for uniform current density across the p-GaN/AlGaN/GaN heterostructure, V_t should depend on the ratio of the two areas, L_{PIN}/L_{SBD}. This is because at constant V_{PIN}, the junction area ratio would determine the required current density across the metal/p-GaN Schottky junction and, therefore, V_{SBD}. Yet, Fig. 2(c) shows no universal trend between V_t and the device L_{PIN}/L_{SBD} ratio. This suggests that the L_{PIN} scaling of $I_G = I_{PIN}$ does not follow a simple linear law.

Toward understanding the scaling of I_{PIN}, we examine the I_G-V_{GS} characteristics of all devices. Figure 4(a) plots these data for devices with $L_{SBD} = 0.7\ \mu m$. I_G exhibits an unusual geometrical dependence: at a constant L_{SBD}, I_G decreases with increasing L_{PIN}, contrary to what one would expect. This apparent anomalous geometrical scaling disappears if we examine I_G vs $I_D \times L_{PIN}$, as shown in Fig. 4(b). We see here that at a constant $I_D \times L_{PIN}$, and therefore, V_{PIN}, I_G increases as L_{PIN} increases. This is what is expected. This result further suggests that I_G is not set by a p-GaN/passivation sidewall leakage current since this current component should decrease as L_{PIN} increases. Yet, when we extract I_G for all devices at a value of $I_D \times L_{PIN} = 10^{-8}$ A × mm (corresponding to our choice of V_t), an unusual set of dependencies emerges, as illustrated in Fig. 4(c).

Ideal scaling behavior for I_G at constant $I_D \times L_{PIN}$ should be a linear increase with L_{PIN}. This is exactly what is observed in Fig. 4(c) for each value of L_{SBD}. However, I_G under the same conditions should not change with L_{SBD}, unlike what we observe. For example, at $L_{PIN} = 2.5\ \mu m$, devices with $L_{SBD} = 0.7$ and $2\ \mu m$ differ in I_G by a factor of 4. In fact, the dominant dependence of I_G in Fig. 4(c) is on L_{offset}. For any given L_{SBD}, as L_{offset} increases, I_G increases very quickly.

I_G then can be understood as consisting of two components: one that scales roughly linearly with L_{SBD} (green dotted line) and a much larger one that increases with L_{offset} (brown dotted lines). This can only be interpreted as one component flowing through the contacted

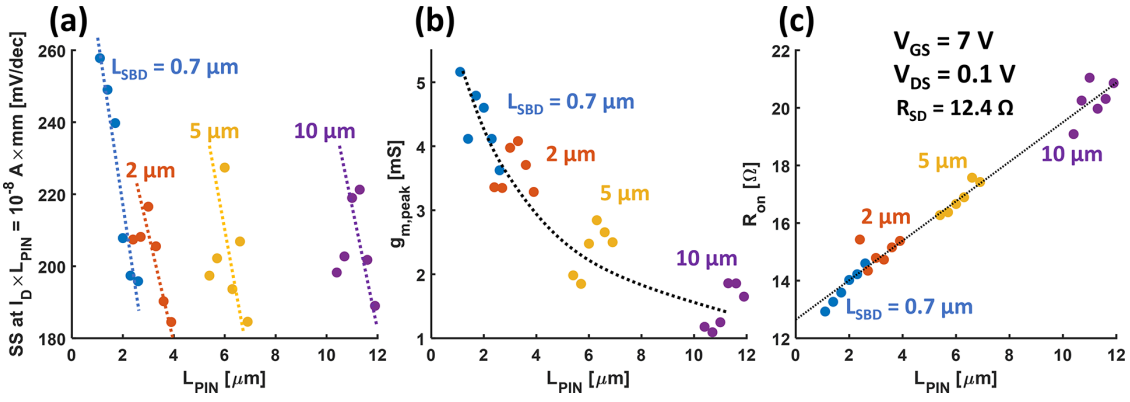


FIG. 3. (a) Subthreshold swing (SS) vs L_{PIN} at V_t for all devices. (b) Peak transconductance ($g_{m,peak}$) in the linear regime for all devices. (c) ON-resistance (R_{on}) defined at $V_{GS} = 7$ V and V_{DS} 0.1 V. Extracted $R_{SD} = 12.4\ \Omega$.

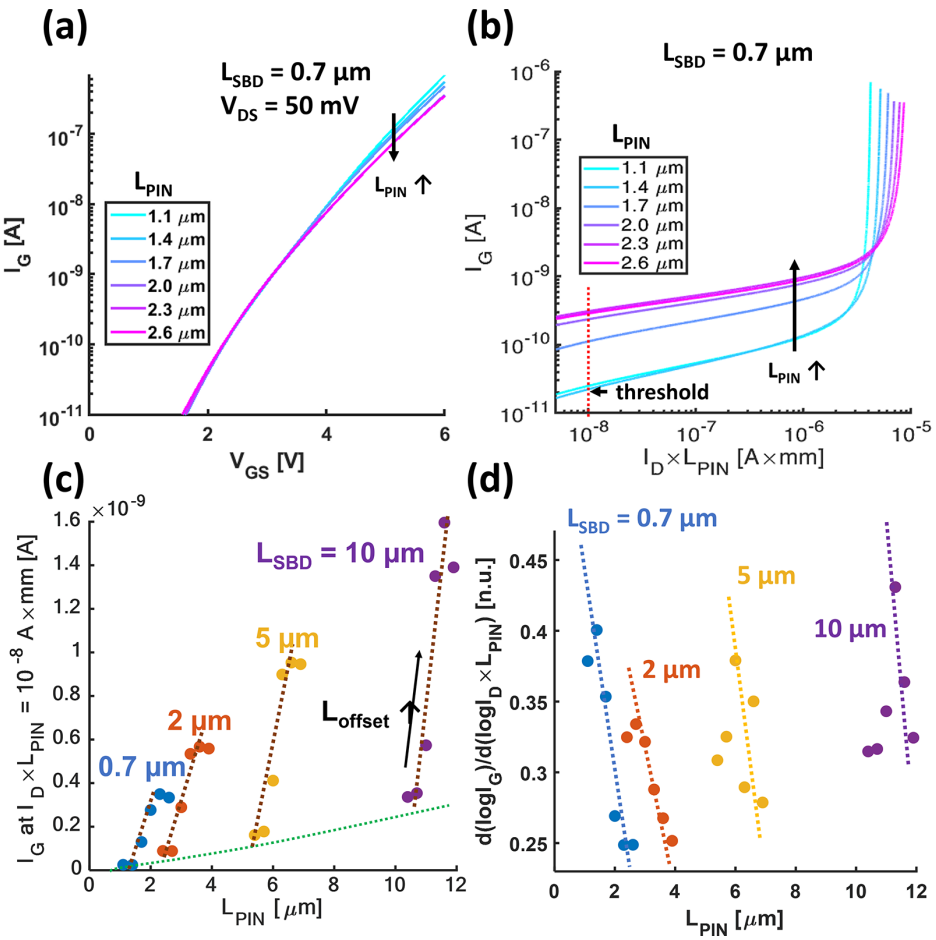


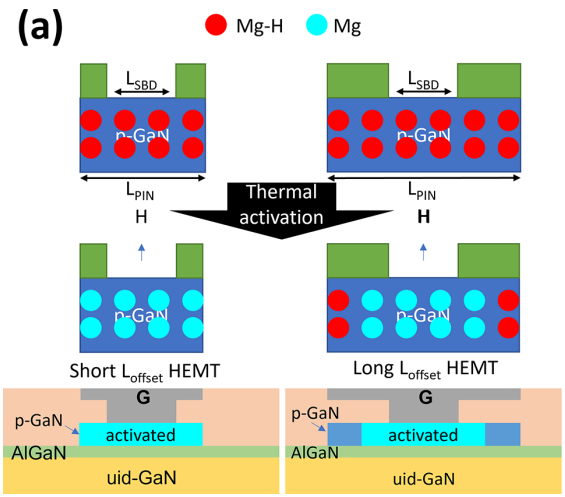
FIG. 4. (a) I_G measured during transfer sweep. (b) I_G vs $I_D \times L_{PIN}$ for $L_{SBD} = 0.7\ \mu m$. (c) I_G at constant $I_D \times L_{PIN} = 10^{-8}$ A × mm. (d) Logarithmic slope of I_G with respect to $I_D \times L_{PIN}$ at V_t.

(intrinsic) portion of the gate of length L_{SBD} and another much larger component flowing through the uncontacted offset region of the gate. This is a surprising result with a possible origin that is discussed below. With this two-component I_{PIN}, it now becomes clear why V_t does not follow simple junction area ratio scaling. With the I_G through the offset region of the gate being much larger than that flowing through the intrinsic portion of the gate, it is the offset current that largely dictates the current density flowing through the Schottky junction and, therefore, V_{SBD} and V_t. The dominant impact of L_{offset} on V_t is clearly observed in Fig. 2(d).

We now turn our attention to the scaling of the subthreshold swing of Fig. 3(a). Understanding the physics of SS in a device where gate current continuity sets the gate electrostatics requires that we focus on *the change* of I_G as V_{GS} changes. For this, we return to Fig. 4(b) where we plot I_G vs $I_D \times L_{PIN}$. An observation in this figure is that not only I_G but also the slope of I_G vs $I_D \times L_{PIN}$ depend on L_{PIN}: it decreases as L_{PIN} increases. This is more clearly seen for all devices in Fig. 4(d) that plots the unitless slope of log I_G vs log ($I_D \times L_{PIN}$) at V_t. Here, we clearly see that for a given L_{SBD}, this slope decreases quickly as L_{PIN} increases.

With this observation, we can now understand the gate geometry dependence of SS in Fig. 3(a). SS describes the change in the gate voltage required to produce a certain change in the drain current. As noted above, in the absence of short-channel effects, SS in a MOSFET is independent of lateral gate geometry. This is because the vertical MOS electrostatics are set by a gate oxide/substrate capacitive divider. In our devices with a back-to-back diode configuration in the gate, under quasi-static conditions, the gate electrostatics are instead determined by gate current continuity. As a result, SS is determined by the sum of the change in the voltages across the two junctions that are required to accommodate the I_G change necessary to induce a given change in the channel current. As observed in Fig. 4(d), at constant V_{PIN}, longer L_{PIN} devices have smaller relative increase to I_G with gradual increase in V_{PIN}. Following gate current continuity, the smaller relative I_G change then results in a smaller V_{SBD} change. Thus, longer L_{PIN} devices result in smaller V_{GS} change for gradual increase in V_{PIN}, resulting in a smaller subthreshold swing. This is consistent with the observations in Fig. 3(a). In fact, there is a remarkable mapping among the data sets graphed in Figs. 3(a) and 4(d).

We have explained the unusual gate geometry scaling properties of our Schottky-gate p-GaN HEMTs around threshold in terms of current continuity. A question to be examined is why the device characteristics in the ON regime, R_{on} and $g_{m,peak}$, appear to follow ideal



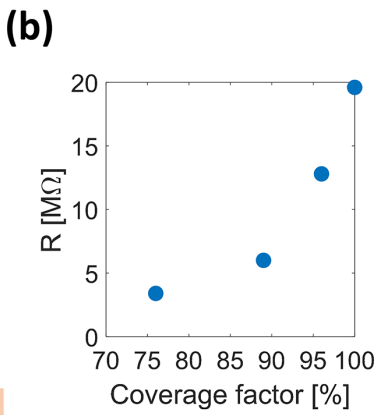


FIG. 5. (a) Schematic of the Mg activation process. In the offset regions of the p-GaN layer, incomplete Mg activation is expected. (b) p-GaN TLM resistance vs % dielectric coverage during annealing.

MOSFET behavior [Figs. 3(b) and 3(c)]. The difference here is that in an ideal FET in the absence of short-channel effects, V_t and SS are independent of gate geometry while $g_{m,peak}$ and R_{on} both exhibit inverse-linear and linear, respectively, dependences on the gate length, or L_{PIN} in this case. In the context of this dominant L_{PIN} dependence, an additional L_{SBD} dependence that might emerge from the gate current continuity arguments above is bound to be comparatively minor and easily masked by other factors such as device to device variability.

Our research shows that the role of I_G is critical in understanding the gate geometry scaling of our p-GaN HEMTs. As Fig. 4(c) reveals, I_G flows preferentially through the uncontacted portion of the PIN barrier. The origin of this is not completely understood, but a possible explanation relies on incomplete Mg activation in this region. During fabrication, Mg dopants are activated through a thermal annealing step that relies on the dissociation of the Mg–H complex.[17–19] At this point in the process, the offset is covered by a dielectric while the intrinsic region remains uncovered [Fig. 5(a)]. Dielectric capping of the offset region might prevent H from escaping and in this way hamper Mg activation or further encourage formation of the Mg–H complexes.[20] This should result in a lower doping level in the capped region and vulnerability to defect related issues. SIMS measurements in the gate stack further show that Mg is present in the AlGaN barrier. Incomplete Mg activation could then impact the band structure and the leakage current over the barrier in the offset vs intrinsic region of the gate.[15,18,21]

Toward verifying this hypothesis, we have electrically characterized Schottky-gate/p-GaN transmission-line model (TLM) test structures with various fractions of passivation capping during the Mg activation anneal. These measurements reveal that the greater the p-GaN layer fraction covered during the annealing process, the higher the p-GaN lateral resistance [Fig. 5(b)]. Since the layer resistance is roughly inversely proportional to the hole density, the higher resistance indicates a lower acceptor activation in p-GaN.

Our research reveals a rich gate geometry dependence of the electrical characteristics of Schottky-gate p-GaN HEMTs. We show that the unique scaling behavior of the threshold voltage and the subthreshold swing that we observe arise from the back-to-back diode nature of the gate stack that leaves the p-GaN layer largely floating. Under quasi-static conditions, the voltage drop across the PIN and SBD junctions is set by the need to provide gate current continuity across both junctions. An additional element of relevance to the geometrical dependences observed here is the preferential flow of the gate current across the PIN barrier in the offset or uncontacted portion of the gate. Our study concludes that the lengths of the PIN and SBD junctions provide another degree of freedom for device engineers to design for desired characteristics, further highlighting the benefits of p-GaN gated enhancement-mode technology.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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