Between AB and D:

A New Class of Audio Amplifier

by

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With Love, Signature redacted

Kenneth Arnold Granderson

P.S. It's still a beautiful world. Keep Smiling!!!

An electric amplifier, in the most general sense, is an electrical device with at least three (3) classes of terminals; inputs, outputs and power source terminals. The input signal (a voltage and/or current) is used to modulate the flow of energy from the power terminals to the output terminals in a predetermined and repeatable fashion (see Fig. 1). Although they may be used in other modes, amplifiers are usually designed to provide linear amplification of some kind; that is, the output signal (current and/or voltage) is constrained to be a replica of the input signal, scaled by a numerical constant which may be real or complex.

Audio amplifiers, one of which is the subject of this thesis, fall into the above category -- they are designed to produce an output voltage which is a linear multiple of the input voltage. Thus, I have just stated the first three constraints on systems that may be utilized for audio signal amplification. The amplifier must have a linear input/output transfer characteristic, and the input and output signals will be voltages. More specifically, the output characteristics of the amplifier must approximate that of an ideal voltage source whose amplitude at any given time is the amplitude of the input voltage, scaled by a fixed or variable gain factor. Mathematically, this relationship is represented by the equation $v_o = A_v v_i$ (see Fig. 2) where v_i and v_o are the input and output voltages, respectively, both referenced to a common ground, and A_v is the voltage gain factor (assumed to be >1).

The discussion of audio amplifier characteristics to this point has focused exclusively on the input and output voltages. However, the input and output currents, although they are not the parameters of interest, cannot be ignored, for it is the relationship between the input and output currents which separate amplifiers from transformers. A transformer can supply voltage

gain, but it does this at the expense of a proportional decrease of output current. As shown in Fig. 3, through magnetic inductance, an ideal transformer may induce a current to flow in its secondary which will cause a voltage drop of $A_v v_i$ across a load resistor, but it cannot simultaneously produce a larger voltage and current than that which are applied to the primary coil. This is because there is no additional source of power (vi) to the system, so $v_{in}i_{in} = v_{out}i_{out}$. Contrast this situation with the amplifier representation shown in Fig. 4. Here, the input power may be infinitesimal, as the amplifier may easily have high-impedance inputs. However, the amplifier selectively channels off power that is available from an unlimited source (i.e., your wall socket) to pump enough current into whatever load resistance you have connected to the output such that the desired voltage transfer $v_o = A_v v_i$ is satisfied. It can easily be seen, even without knowing that R_L's less than 10 ohms are standard in audio applications, that $v_o i_o >> v_i i_i$ in any normal case (i.e., nonzero and finite parameters). Thus, $P_o > P_{in}$, and we have achieved the characteristic of amplifiers that sets them apart from transformers, and that is power gain.

The concept of power gain, alluring as it may be, is nonetheless somewhat misleading. The term 'power amplification' only applies to the ratio of power delivered to the load, referred to power taken from the signal source. The extra power is being taken from the supply terminals, and as any student familiar with the concepts of energy conservation will tell you, there is no such thing as a free lunch. Not only do you have to supply the extra power from the supply terminals, but every electronic circuit requires a certain amount of power to keep it running. This power is dissipated (lost) as heat, and it is time to introduce the concept of efficiency.

The concept of power gain looks good on paper, but is rather meaningless in a practical sense, as the power gain of almost any circuit can be pushed towards infinity by using a high-enough impedance buffer between the signal source and the circuit with low power gain. The buffer, of course, will get its additional power from the supply rails. The concept of efficiency more realistically deals with the issue of power out vs. power in. The efficiency of an electrical amplifier is the ratio of power out vs. total power in -- from the supply rails, as well as any and all signal sources. The efficiency of any system (averaged over time if it stores energy) can never exceed or even equal 1, as everything needs at least a little bit of energy to run off of. Conventionally designed audio amplifiers are notorious for wasting energy. The circuit I will be introducing is an attempt to solve the efficiency problem while avoiding the other problems associated with some of the present solutions to the issue of efficiency.

To ensure the reader of a thorough understanding of this new system, I will first discuss the concepts behind conventionally designed solid state amplifiers and develop further the issue of efficiency as it relates to the circuits that will be examined. Then, the new system will be described and analyzed in the same fashion, although in much greater detail, so that an intelligent and comprehensive comparison may be made. Before jumping into the subject of conventional amplifier circuits, though, I will introduce the limited but sufficient transistor model which will be in the center of the following analyses. Shown in Fig. 5 is a schematic symbol for an npn bipolar transistor and the associated model which will be used to describe its operation (a pnp transistor has all voltage polarities and current directions reversed). Note the terminal current and voltage parameters and their relationships with each other. The stated relationships only apply when

the transistor is operated in the linear region, so called because of the approximately linear base and collector current relationship which only exists when the device is operated within certain current and voltage limits. When operated within these limits, the transistor can be used as a linear amplifier by exploiting the current transformations between the collector or emitter currents and the base current. Since the relationship of emitter or collector current to base current is linear, connecting either the collector or the emitter to an appropriate energy reservoir allows us to use the base as our control valve to selectively source or sink as much current as we want such that the transistor satisfies the criteria initially discussed to qualify as a linear amplifier.

For operation in the linear region, various voltage constraints must be observed: First, V_{BE} must be greater than zero (forward biased). As the model shows, there is effectively a diode between the base and emitter terminals. Thus, the forward bias on the base-emitter junction is limited to about .6V (for silicon devices). If V_{BE} falls too far below .6V or goes negative, the transistor is said to be in cutoff.

When in cutoff, the transistor acts somewhat like a 3-terminal open circuit (see Fig. 6a). Small but finite currents do flow between the terminals in reality, though. These are called leakage currents, and are not of interest to this discussion. What is of interest, however, is the fact that at least to a first approximation, the collector current I_C is zero when the transistor is in cutoff. Although the base-emitter junction must be forward-biased for linear operation, keep in mind that there is a real diode between the terminals which is constrained by a real diode's i-v characteristic. Therefore, connecting an ideal voltage source from the base to emitter may have catastrophic

effects, as sufficient current to destroy the device may flow if a voltage larger than .7V is applied to the terminals. Remember, the bipolar transistor is a current-controlled current source. The terminal voltages simply constrain (or are constrained by) its mode of operation.

In contrast to the base-emitter junction, the junction between the base and collector must be reverse-biased for proper transistor operation. For an npn transistor, this means that the collector should be at a higher potential than the base. Like a reverse-biased diode, the amount of reverse bias on the junction does not change the state of the device until some breakdown voltage is reached, at which point massive current flows. Unlike the reverse-biased diode, however, current does flow through the reverse-biased collector junction before breakdown. This current is a direct consequence of the 'magic' of transistor action, and has the desired characteristic of being proportional to the base current by the current gain factor, β. The important voltage considerations to note are that the collector-base voltage has maximum and minimum limits, and when operated within these limits, the collector current is (approximately) independent of V_{CB}. If the collector-base junction becomes forward biased, then transistor action ceases and the transistor is said to be saturated. In the saturated state, the device can be modelled (to first-order) as in Fig. 6b. In this state, the voltage from collector to emitter (labelled V_{CE}) is very small in practice (on the order of 1V), and zero in the model.

Before introducing any amplifier circuits, two more constraints must be discussed, as they are not included in the model and are the most constraining factors in high-power solid-state design. In our simple model, the collector current in the active region is given as $I_C = \beta I_B$. Of course,

this can only hold true if the various impedances to which the transistor is connected allow, but there is an upper limit on I_C. If this limit is exceeded, the wires which connect the actual slab of silicon to the case pins may melt down and open circuit.

The model also neglects the effects of dropping a voltage from the collector to the emitter while passing a current through the junction. The product of collector current and collector-emitter voltage has the dimensions of power and is the primary source of power dissipation in the transistor. The total power dissipated in the device is given by $P_D = I_C V_{CE} + I_B V_{BE}$, but the latter term is usually ignored, assuming that β is large ($I_C = BI_B$) and V_{BE} is small. In practice, the β of power transistors is not really that large, but I will use the approximation nonetheless, as it is a best-case model which will highlight the futility of trying to achieve efficiency in classical output stages even if we had perfect transistors; furthermore, it makes the equations simpler.

Every transistor can dissipate a certain amount of power, and if forced to exceed its capacity, catastrophic failure (destruction) may occur. To make matters worse, bipolar transistors have an intrinsic ability to blow themselves up via a process called thermal runaway. It works like this. Remember when I said that B was approximately linear? Well, it has a positive temperature coefficient, and power dissipation generates heat. So, at a given V_{CE}, the collector current I_C causes $V_{CE}I_C$ watts of power to be dissipated at the collector junction, which generates heat. This heat raises β a little, and if I_B is constant, $I_C = \beta I_B$ goes up a little, raising P_D, and so on. If not kept in check by careful design of bias networks, this positive feedback process can result in blowing the transistor. Depending

on the amplifier circuit and the mechanism leading to the untimely devise of the power transistors, blowing up your output stage can often damage or destroy your power source (supply) and/or destination (speakers), to boot. Thus, it is easy to understand why control of power dissipation is a matter of prime concern in high-power amplifier design.

On to circuits. Fig. 7a shows one of the most widely-used (and least efficient) amplifier topologies to date. It is called a Class A amplifier, and it does a Class A job of wasting power. Here's how it works. V_{BQ} sets the no-signal (quiescent) collector voltage, and v_s is the signal voltage which makes the base voltage v_B wiggle around V_{BQ}. Under quiescent conditions, the base is at V_{BQ}, which means that (assuming V_{BQ} is large enough to turn the transistor on) $V_E = V_{BQ} - .6V$. Thus, $I_E = \frac{\beta+1}{\beta} I_C = (V_{BQ} - .6V)/R_E$, and so $V_{CQ} = V_{CC} - \frac{\beta}{\beta+1} \frac{R_C}{R_E} (V_{BQ} - .6V) = V_{CC} - \frac{R_C}{R_E} (V_{BQ} - .6V)$ for transistors with a healthy β. Under these steady-state conditions, $V_o = 0$ as the voltage across C is not changing. Now, let V_s come into the picture. As V_s wiggles up and down, the transistor sees a modulation in the base voltage. Any change in the base voltage is carried through to the collector node, with a factor of $-\frac{R_C}{R_E}$ to boot. Changes in the collector voltage cause currents to flow through the capacitor, which in turn modulates V_o. The circuit is much more effectively analyzed in terms of the incremental circuit shown in Fig. 7b, which treats all fixed sources as zero references and only concerns itself with the deviations from the quiescent points (that is, all of the currents and voltages in this model refer to deviations from the quiescent total variable quantities). Conveniently, since $V_{OQ} = 0$ anyway, this method gives us the voltage produced across the load resistor exactly. As long as the transistor is kept out of the cutoff and saturation regions, the

model gives us $V_o = -R_C/R_E \frac{sR_LC}{s(R_C+R_L)C+1} V_s$ where I have used s-plane notation to describe the capacitor, as all inputs and outputs are assumed to be sinusoidal. Now, the capacitor's function is purely to keep dc currents out of the load (assumed to be a loudspeaker). Thus, we will say that it is large enough to be considered a short to signals, and the expression becomes $V_o = \frac{R_C}{R_E} \cdot \frac{RL}{RC+R_L} V_s$.

Under no-load conditions (i.e., when the amplifier is feeding a high Z_{in} second stage), R_L goes to infinity, and the V_o-V_s relationship is $V_o = \frac{-RC}{R_E} V_s$. This is a much more familiar result than the one shown above, as Class A stages are usually used strictly as voltage gain stages. Their high level of inefficiency all but banishes them from use in output stages of any real magnitude, except for use in purist power amps designed to capitalize on the handful of distortion maniacs who must have their distortion ratings in the parts-per-million range. Since transistors operating Class A are always turned on, they do produce less distortion than Classes B and AB, which operate at or near cutoff during portions of each cycle, but most mere mortals cannot detect distortion levels lower than .1% (point one percent) of the output signal. Please keep in mind that all of the circuits analyzed have load impedances connected, so all equations shall reflect operation under loaded conditions. Thus, the voltage gain of the Class A circuit (defined as signal voltage out/signal voltage in) is $Av = - \frac{R_C}{R_E} \frac{R_L}{R_C+R_L}$.

On to power considerations. Throughout this entire thesis, all input and output signals are assumed to be composed of one or more sinusoidal waveforms, so standard complex analysis applies. Given an output signal of amplitude V_o, that is, $v_o(t) = V_{ocos}$ (wt + ø), the instantaneous output

power delivered to the load is $P_o(t) = V_o(t)\ I_o(t) = \frac{V_o^2}{R_L}\cos^2(wt + \phi)$. (Note: The load impedance is assumed to be resistive for analysis purposes. Loudspeakers also have reactive components to their impedances, but the resistive model is sufficient for present purposes.) The average output power (which is what is really of interest, as it is the average power-dissipations which indicate how much energy is being wasted) is $\bar{P}_o = \frac{V_o^2}{2R_L}$. The instantaneous input power, ignoring the signal input for now, is $P_i(t) = V_{CC}(t) \cdot I_{CC}(t)$ $= \frac{V_{CC}^2}{2R_C} - \frac{V_{CC}V_o}{R_L}\cos(wt + \phi)$, where the former term comes from quiescent power dissipation, assuming that the standard Class A bias point of $V_{CQ} = V_{CC}/2$ has been chosen to allow maximum output voltage swing in both directions. The latter term vanishes upon integration, as the circuit supplies signal power to the load only on the positive half-cycles. On the negative half-cycles, power is delivered back into the circuit. Thus, the average input power to the circuit is $\bar{P}_i = \frac{V_{CC}^2}{2R_C}$. The average efficiency is then $\bar{\eta} = \bar{P}_o/\bar{P}_i = \frac{R_C}{R_L}\frac{V_o^2}{V_{CC}^2}$. As $\bar{\eta}$ is proportional to V_o^2, it is evident that the maximum efficiency will be obtained for a maximum output signal. As the transistor is the only active element in the circuit and the circuit is not oscillatory, the peak-to-peak output voltage cannot exceed V_{CC}, and if the system were unloaded, the output voltage would indeed be of swinging from $-\frac{V_{CC}}{2}$ to $+\frac{V_{CC}}{2}$, saturation voltages notwithstanding.

However, there is a load resistance R_L connected to the output, so $V_{omax} = \frac{R_L}{R_C + R_L}\frac{V_{CC}}{2}$. Using this figure and basic calculus, it is determined that $\bar{\eta}$ is maximized for $R_C = R_L$ (how convenient). So, $\bar{\eta} = \frac{V_o^2}{V_{CC}^2}$, and V_{omax} $= \frac{V_{CC}}{4}$. Thus, $\bar{\eta}_{max} = \frac{V_{o2max}}{V_{CC}^2} = \frac{1}{16} = 6.25\%$. Right about now, you must be asking, "what happened to the other 93.75% of the power?" Well, look back to the expressions for $P_i(t)$ and $\bar{P}_i$. With no signal, the circuit is burning up $\frac{V_{CC}^2}{2R_C} = \frac{V_{CC}^2}{2R_L}$ watts of power. This is kind of like having your car idling at 4000 rpms. The circuit gets more efficient with higher output amplitudes,

but the output is limited by the output resistor loading effects. About half of the output power is burned up in R_C, and the transistor and R_E take care of most of the rest. As we can find power resistors of virtually any voltage, the power dissipated in the transistor will be the final issue of interest concerning Class A amplifiers. The expressions for $P_D(t)$ and $\bar{P_D}$ involve R_E, which has not really been considered till now. R_E is used in conjunction with V_{BQ} to set I_{CQ}, but more importantly is inversely proportional to the voltage gain A_V of the circuit. Thus, eliminating R_E so as to use A_V as a parameter gives us $\bar{P_D} = [\frac{5}{10} - \frac{3}{15A_V}] V_{CC}2/R$, and it is evident that there is a tradeoff between voltage gain and transistor power dissipation.

By now, you must feel that only a fool would use Class A circuitry. This is not true, for the stated results only apply to circuits driving low impedances such as loudspeakers. As intermediate gain stages, Class A circuits are used all of the time, as they are relatively easy to design, and they are also good for low-power amplifiers, where efficiency is less of a concern as are bias considerations.

For power stages, which are the issue of concern here, the goal of efficient power transfer is much more effectively achieved with the Class B or AB circuit. A version of this type of circuit suitable for amplifying only positive signals is shown in Fig. 8a for analysis purposes. When functioning strictly Class B, the circuit operation is as follows; $V_{BQ} = 0$. Therefore, for $V_S < .6V$, the transistor is off. For signal voltages above .6V, $V_O = V_S - .6V$, and the transistor draws a current I_B from the source such that $I_O = (\beta + 1)\ I_B = V_O/R_L$. Thus, the higher the input voltage, the closer the Class B circuit approximates a voltage follower, as the .6V offset becomes a smaller percentage of the output voltage. However, for

$V_S < .6V$, there is no output, so if two complementary transistors are connected in parallel to drive both halves of the waveform (as necessary, as each transistor can only source or sink current in the direction of its emitter arrow), there is no output for $|V_S| < .6V$, and a sinusoidal input produces an output as in Fig. 8c (see Fig. 8b for circuit). Obviously, the waveform is being grossly distorted, and this particular type of distortion, called notch distortion, is actually audible and is therefore to be avoided.

Going back to Fig. 8a, if we let $V_{BQ} = .6V$, then for positive V_S the circuit will operate much more like a voltage follower, as the output will follow the input with the .6V offset compensated out of the picture. This is the concept behind Class AB operation, where the AB notation implies operation somewhere between Classes A (biased always on) and B (biased at cutoff). The amount of no-signal bias applied trades off certainty of freedom from cutoff against no-signal dc output current. Class AB also dissipates a bit more power than Class B, as the transistor is biased slightly on. A practical example of a circuit containing drivers for negative as well as positive excursions is shown in Fig. 8d. Here, the bias resistors R_B provide a current path through the diodes to maintain a 1.2V drop across the pair. Modulating V_S makes the voltages at the bases of Q_1 and Q_2 $(V_S + .6V)$ and $(V_S - .6V)$, respectively, and for positive inputs Q_1 conducts, as does Q_2 for negative signals. This biasing method has the additional feature of good temperature stability, as the diodes will track the transistor V_{BEon} as long as they are of the same material (i.e., silicon) and are at the same temperature (i.e., close together). Often, the single diodes in the diagram will be replaced by a pair in series on either side of V_S, as to bias the transistors further from the edge of cutoff.

Before exploring the efficiency of the Class AB circuit in action, first note what is happening at the extremes of the operating range. Using Fig. 8a as our theoretical circuit, with V_{BQ} = .6V and $V_S > 0$, note that at $V_S = 0$ the transistor is on the verge of cutoff, or $I_B = I_C = I_E = 0$. Therefore, P_D, the power dissipated by the transistor, is $P_D = V_{CE}\, I_C = 0$.

Likewise, for excessive input signals (on the order of V_{CC}), the transistor is driven into saturation, and $P_D = V_{CE}\, I_C = 0$ again. Between these two limits is the region of linear amplification, and the power dissipation in the linear region is most definitely nonzero.

When operating Class AB, each output transistor conducts only over one half of each cycle. Therefore, when calculating $\bar{P}_o$, I will only consider the average power delivered to the load over the half cycle that either transistor is turned on, so as to maintain a meaningful interpretation of $\bar{\eta}$. I could alternatively average $\bar{P}_o$ over an entire cycle and then find $\bar{P}_i$ by using $P_i(t)$ from both the positive and negative supplies. In forming the ratio $\bar{P}_o/\bar{P}_i$, the relative factors of 2 (two) would just cancel anyway.

So, going back to Fig. 8a, as the npn transistor conducts only on the positive half-cycles, $V_o(t) = V_o \sin \omega t$ for $[0 < t < T/2]$ and 0 for $[T/2 < t < T]$. Thus, $\bar{P}_o = V_o^2/4R_L$. In estimating $\bar{P}_i$, I will use the $\beta \gg 1$ approximation as a best-case situation. (In practice, β can be as low as 3 for power transistors operating at high currents.) Then, $P_i(t) = V_{CC}\, I_C(t) = V_{CC}\, \frac{V_o(t)}{R_L}$ and $\bar{P}_i = \frac{\omega}{2\pi} \int_0^{\pi/\omega} \frac{V_{CC} V_o}{R_L} \sin \omega t\, dt = \frac{1}{\pi}\, \frac{V_{CC} V_o}{R_L}$. Therefore, $\bar{\eta} = \bar{P}_o/\bar{P}_i = \pi\, V_o^2/4V_{CC}V_o = \frac{\pi}{4}\, \frac{V_o}{V_{CC}}$. Ignoring saturation voltage, $V_{omax} = V_{CC}$, so $\bar{\eta}_{max} = \frac{\pi}{4} = 78.5\%$. It should come as no surprise now to hear that Class AB output stages are the most widely used for power amplification.

To find the maximum power dissipated by the Class AB stage, from

$$P_D(t) = V_{CE}(t)\ I_C(t) = (V_{CC} - V_o(t)) \cdot \frac{V_o(t)}{R_L} = \frac{V_{CC}V_o \sin wt}{R_L} - \frac{V_o{}^2 \sin^2 wt}{R_L},$$

$\bar{P}_D = \frac{1}{\pi} \frac{V_{CC}V_o}{R_L}$, then, $\frac{d\bar{P}_D}{dV_o} = \frac{1}{\pi} \frac{V_{CC}}{R_L} - \frac{V_o}{2R_L}$, so $\bar{P}_D$ has a maximum at $V_o = \frac{2}{\pi} V_{CC}$, at which point $\bar{P}_D = \frac{1}{\pi^2} \frac{V_{CC}{}^2}{R_L} = \bar{P}_o$, as $\bar{\eta} = 50\%$ at this point. Below this point, $\bar{P}_D > \bar{P}_o$, or $\bar{\eta} < 50\%$, and above this point, $\bar{\eta} > 50\%$, $\bar{P}_o > \bar{P}_D$, as shown in Fig. 9.

At either limit of output voltage amplitude, $\bar{P}_D$ approaches zero. For no signal, $\bar{P}_D$ is determined by the bias point, and at the upper limit, the saturation voltage of the transistor comes into play. ($\bar{P}_{Dmax} = \frac{(6.273V_{CC} - V_{CEsat})}{R_L}$) The inherent nature of this circuit makes it more efficient than the Class A circuit, as the transistor is working along with the output signal rather than against it.

Although the Class B/AB circuit does not provide voltage gain ($A_V < 1$, but is pretty darn close to 1), there is definitely current gain, so the circuit does provide power gain. A typical amplifier may use Class A stages as input and driver stages for voltage gain, and then finish off the job with a Class AB output stage. The push-pull design, as in Fig. 8d, also allows direct coupling of the amp to the loudspeakers. The transistors, if carefully biased, will both be equally turned on at no-signal conditions, and if Q_1 and Q_2 are matched well enough, V_o can be made to equal ground potential when equal bias currents are flowing through Q_1 and Q_2. This eliminates the need for output capacitors, as zero dc current flows through the speakers at no signal. In addition to these considerations, the output impedance is very small as the circuit effectively places R_C in parallel with an impedance of magnitude $R\pi/(\beta + 1)$ where $R\pi$ is a linear incremental resistance parameter for the base-emitter junction.

So far, we have analyzed the operations and efficiencies of the Class A and Class B/AB amplifier circuits. As these circuits operate on principles as old as the first vacuum tubes, they are in widespread use in most of the amplifiers ever made. The next system that will be examined is the Class D or switching amplifier. Although the theory behind the Class D circuit has been around for a while, the practical Class D amp is a relatively new animal, as the theory had to wait for the industry to produce devices which were compatible to the demands of the switching amplifier.

The Class D system takes advantage of the fact that Class B circuits dissipate very little power when they are cutoff or saturated, as we have already seen. (An ideal switch dissipates no power, as $V_{CE} \cdot I_C$ is always zero in either state.) The driving force behind the switching amplifier is the pulse-width modulator (PWM). The PWM is a circuit designed to produce a square-wave at its output with a duty cycle which is a function of a modulating input signal. A PWM is easily produced with a few off-the-shelf components. A voltage comparator, which may be an op-amp operated open-loop, is a good place to start building a PWM. A comparator's function is to output one of two voltages as a function of its input voltages (see Fig. 10a). If $V_+ > V_-$, then $V_o = +V_{CC}$, and if $V_+ < V_-$, $V_o = -V_{CC}$.

If an op-amp used, then the operation is the same, except that the op-amp is designed to produce an output ($V_o = A_v v_i$) which is a linear multiple of the difference between the inputs, $V_i = V_+ - V_-$ (Fig. 10b). The catch is, A_v is usually in excess of 10^4, so the range of $V_+ - V_-$ which will produce an intermediate voltage is on the order of $V_{CE}/10^4$, or usually a few millivolts. In standard op-amp connections which utilize negative feedback, part of the output signal is fed back to the V_- terminal, which decreases the output, and this process forces V_- to come close enough to V_+ to keep the op-amp

in the linear range. For our purposes, there is no feedback, so the op-amp acts essentially as a comparator.

Now consider what happens if we connect V_+ to zero volts and V_- to a triangle-wave oscillator of frequency f_{osc}. The comparator compares the two inputs, and outputs $+V_{CC}$ when the triangle wave input is negative, and $-V_{CC}$ when the triangle wave is positive. As the triangle wave is positive for one half of the period and negative for the other, V_o is a square wave of amplitude V_{CC} and frequency f_{osc}. The duty cycle of the square wave, defined as ton/T (see Fig. 10c), is .5 or 50%, as the triangle wave is assumed to have a 50% duty cycle also. A square wave can also be interpreted as a train of pulses. In this case, all of the pulses have the same width, but that is about to change.

Take a look at Fig. 10d, and study it carefully. It illustrates the relationships between V_+, V_- and V_o for our PWM when V_- is at a nonzero positive level close to V_m, the amplitude of the triangle wave. For the majority of each period T, the V_+ input is greater than the level of the triangle wave. Thus, $V_o = +V_{CC}$ for those times. The output waveform is still periodic, and can still be considered a pulse train, but the width of the pulses have been modulated by the voltage at V_+ - hence, the description of the circuit as a pulse-width-modulator.

Using a triangle wave as the oscillator input to the comparator produces a neat, simple relationship between the modulating input and duty cycle (DC) output. Because the triangle wave varies linearly with time over every halfperiod, $DC_{(in\ \%)} = 50\ (1 + \frac{V_+}{V_m})$, where it is assumed that $-V_m<V+<V_m$ at all times.

So now we are experts on PWMs, but you are wondering what square waves or pulse trains with variable duty cycles have to do with sound amplification, which concerns sinusoidal waveforms. Simple. If we calculate the time-average of $V_o(t)$, the output of our PWM, we get $\bar{V}_o = \frac{1}{T}\int_0^T V_o(t)dt = \frac{1}{T}\int_0^{t_{on}} V_{cc}dt + \frac{1}{T}\int_{t_{on}}^T (-V_{cc})dt = \frac{V_{cc}}{T} t_{on} - \frac{V_{cc}}{T}(T - t_{on}) = \frac{V_{cc}}{T}(2t_{on} - T) = V_{cc}(\frac{2t_{on}}{T} - 1) = V_{cc}(2DC - 1)$.

Converting our expression for DC from a percentage to fractional notation gives $DC = 1/2(1 + \frac{V_+}{V_m})$, and it is evident that $\bar{V}_o = \frac{V_{cc}}{V_m} V_+$. Therefore, if the modulating voltage at V_+ is a sinusoid of frequency small enough compared to the oscillator frequency that it can be approximated as a DC level over an oscillator period or two, the average value of the PWM output will be a sinusoid, amplified by the factor of V_{cc}/V_m. An op-amp or comparator consumes power on the order of mW, and if the comparator drives a pair of transistors operating as switches (either saturated when on, or in cutoff), they consume no power (ideally), so if we can find a way to synthesize the average of $V_o(t)$ without consuming any power, we will have an amplifier operating at nearly 100% efficency! (See Fig. 10e). Synthesizing a time-average is rather difficult to do without more complicated circuitry, as the definition of a time-average voltage $\bar{V} = \frac{1}{T}\int_0^T V(t)dt$ implies some kind of clear or reset operation every T seconds. However, if V(t) is of sufficiently high frequency, a low-pass filter will produce a good approximation of the average value at the input, and (ideally) lossless filters can be built using purely reactive components, such as an L-C combination. As the low-pass filter only gives an approximation of the desired output signal, one more op-amp can be added before the PWM to compensate at the PWM input by using negative feedback from the amplifier output (See Fig. 10f). Thus, we seem to have designed the perfectly efficient amplifier, as the power conversion from supply to load is accomplished by switching

the necessary amounts of energy into and out of a reactive network at the correct times so as to save precious energy from being wasted as heat to burn up our transistors and raise out electric bill.

In practice, well-designed switching amplifiers (much more complicated than this simple example) can operate at efficiencies approaching 95%. However, there is one small drawback to the Class D design, and that concerns the output network. The output impedance of the Class D amp is almost purely imaginary and thus the compatibility of the amplifier to many of the diverse and esoteric loudspeaker systems available today is hampered. The amplifier is more sensitive to reactive components in the load than directly-coupled circuits. In actuality, this shortcoming is probably too minor for any normal person to worry about, but these are the types of issues and considerations that keep the minds and wallets of audio design engineers in good shape, as the quest for the perfect amplifier continues.

What may very well be the latest chapter in this quest is a new circuit which I call the Class K amplifier, named after Kevin G. Rhoads, who originated the idea. I have analyzed the concepts and have done some theoretical work on the circuit, but a prototype of the design is yet to be developed.

The Class K circuit attempts to combine the advantages of resistive output impedance and the excellent low-frequency reponse associated with Class AB designs with the efficiency that can only come from a device operating in switching (Class D) mode. It does this by powering a conventional Class AB output stage with a power supply that is essentially a pair of Class D amplifiers, one handling each polarity of supply voltage.

The concept behind the circuit's operation takes advantage of certain aspects of the circuits already covered to this point. The Class AB circuit provides a low output impedance and direct coupling, but can waste as much

as half the available output power in the transistor at certain output levels. Near the extremes of linear operation, as the transistor approaches the region of switching operation, the dissipated power $\bar{P}_d$ approaches zero, as I_C or V_{CE} approach zero when the device nears cutoff or saturation, respectively.

Comparing these two conditions, only the former - when the transistor is near cutoff - imposes any great limitation on the possible output signals, as I_C is very small. The assertion that V_{CE} is approaching zero implies absolutely nothing about I_C, nor the absolute magnitudes of V_C and V_E at that point. Only their difference, V_{CE}, has been constrained. In real life, V_{CE} has a nonzero saturation value called the saturation voltage; it is usually denoted as V_{CEsat} and for bipolar silicon power transistors is appoximately one volt. Thus, if the Class AB amplifier is operated with a variable power supply which tracks the output voltage and maintains V_{CC} say, 2 volts above the signal output , then the transistor will still be operating in the linear amplification region, and will be dissipating energy at the rate $P_d(t) \simeq 2V \cdot I_C = 2V \cdot I_o(t)/R_L$ watts. This implies that $\bar{P}_d = V_o \frac{2V}{\pi R_L}$ $= \frac{4V}{\pi\sqrt{R_L}}\sqrt{\bar{P}_o}$. So, the power dissipated in the transistor is proportional to the <u>square-root</u> of the output power. This result has far-reaching consequences, as the other systems considered (except of course, the Class D) have power dissipations which are linearly related to the output and/or power supply output power. Thus, the power burned up in the transistor when delivering 1kW of power to a load is only ten times that dissipated for a 10W output.

'This sounds good,' you say, 'but how can you vary a power supply voltage like that?' Again, the question has already been answered by previous circuits. Remember, as long as the collector voltage of the Class AB circuit is maintained high enough to keep the transistors out of saturation, linear amplification is possible. And, two Class D circuits, one designed solely for the amplification of positive signals, and the other negative, comprise the power supplies

for the Class AB circuits. Each Class D amp has as its input a half-wave rectified version of the audio input signal, offset by a bias voltage sufficient to keep the outputs of the Class Ds two volts above (or below, as the case may be) the output of the Class AB circuit. The system is schematically diagrammed in Fig. 11.

I will not attempt detailed numerical analysis of the circuit, as the nature of the pulse-width modulator requires the heavy use of state equations or signal processing theory which would simply confuse the intent of this thesis, which is to assert that the circuit works. Nevertheless, a physical prototype of a theoretical design must be built with actual, nonideal devices, so let us go step-by-step through the design of a Class K amplifier.

We are designing a power amplifier, so the first parameter we will decide is the output power capability of the circuit. Before doing this, though, we must realize that the output power is the product of the output voltage and current, which are related to each other by Ohm's Law, $V = iR$. The situation is further complicated by the fact that loudspeakers are not resistors, as they have reactive components which will keep the output voltage and current almost always out of phase with each other. I will attack these issues in the following manner: as most loudspeakers contain coils, their primary source of reactance is inductive in nature. Therefore, band-limiting the input signal and using the amplifier strictly as a bass amp tends to make the resisitive load model more applicable, as if the speaker impedance can be approximated as $Z_L = R_L + jwL$, limiting w limits the latter term and lets R_L dominate.

The decision to band-limit has other fringe benefits. The success of the PWM technique relies on the input signal varying so slowly compared to the switching frequency that the input looks like a constant dc level to the PWM. Now assume a sinusoidal imput signal with an amplitude of one

volt and frequency of 20kHz, i.e. $v_i(t) = \sin 2\pi(20 \cdot 10^3 \text{ sec}^{-1})t$. This signal varies as $\frac{dv_i}{dt} = 2\pi(20 \cdot 10^3 \text{ sec}^{-1})\cos 2\pi(20 \cdot 10^3 \text{ sec}^{-1})t$, or when crossing zero, is changing at the rate of 125,000 V/sec. This means that it would take 8μS to change 1 volt (if it continued slewing at that rate).

Arbtrarily picking the limit of 5% of the maximum input (i.e. 50mV) as the highest tolerable change in input voltage over one cycle, this implies that the PWM period must be no greater than 400nS, or the PWM frequency must be at least 2.5MHz. Besides limiting the selection of components that we can easily obtain to perform this task, a circuit that will switch several amperes through a couple of dozen volts at 2.5MHz goes by another name. It is called a radio transmitter, and operating something like this in your home will completely mess up your TV and radio reception, as well as your neighbors, etc., and the FCC will politely drop by and lock you up.

Limiting the input frequency to 1kHz, for instance, allows you to lower the PWM frequency by a factor of 20 to 125KHz, which is a lot easier to manage. This also eliminates the problem of intermodulation distortion, which occurs when an amplifier simultaneously produces signals that are of markedly different frequencies, such as a 20kHz signal riding on a 20Hz wave. This form of distortion is alleged to actually be audible in many real amplifiers by real people, unlike the Total Harmonic Distortion (THD) that is at least an order of magnitude under audibilty in all but the most generic amplifiers today. Band limiting also puts the power where it is needed, as each halving of frequency requires twice the power to produce a given output, and limiting also allows you to drive your woofers directly, instead of using a passive crossover (remember direct coupling?).

Now that we have decided to band-limit, let the design continue. The amplifier will be designed to drive an 8 ohm load, and will be able to deliver 100 watts rms to that load. As $P = i^2R = V^2/R$, this means that that output

must be able to source or sink 3.5 amps rms (5A peak) at 28.28 volts rms (40V peak). The power supply rails will be ±45V, and the supply must be able to source at least 6A of current per side.

As we have already determined that a Class AB output stage will be used, a 2N3055/2955 pair are selected for use as emitter- followers in a push-pull configuration, as shown in Fig. 12a. These transistors can take an I_C of 15A continuously, and can handle 100V from collector to base, as well as having a saturation voltage of $1.1V_{max}$. Unfortunately, β is only guaranteed to be as high as 20, so we must be able to pump $5A/20 = 250mA_{peak}$ into (or out of) the output transistors. Thus, the Darlington connection of Fig. 12(b) will be used. Qd_+ and Qd_- may be any npn and pnp transistors which have a healthy β (>100), can source or sink 250mA with no compromise of gain, can withstand V_{CC} volts from collector to emitter, and have small saturation voltages, as these connections alter the limits on V_{CC} to no closer than the V_{BE} of the output devices plus the saturation voltages of the driver transistors (Qd's). (Note: As the circuit is symmetrical, only the positve side will be used for analysis in most cases.)

The D40D8 and D41D8 by General Electric satisfy these requirements easily, with β's of 120_{min}, I_{Cmax} of 1A, and V_{CEsat}s of .5V. The next step is the bias network. Although the network in Fig. 11 is sufficient (with the addition of two more diodes to compensate for the two driver transistor V_{BE}s), much better bias stability is obtained by replacing the bias resistors R_B with current sources, as in Fig. 12(c). FETs connected as shown make good current sources, and the R_Bs are adjusted for I_{BIAS} = 4mA so that there will be no shortage of bias current. The FETs should be able to handle a V_{DS} of $V_{SS} + V_{CC}$, as either drain will swing about $V_{SS} + V_{CC}$ away from its source on maximum excursions of output voltage. Siliconix' CR390 Current Regulator Diodes are internally set to source 3.9mA, and easily satisfy

these requirements.

The choice of an amplifier stage to drive the power stages is a little more difficult. As the Darlington connection gives us 'unlimited' current at the expense of an extra V_{BE} drop from input to output, the preamp stage must be able to put out $41.2V_{peak}$ to satisfy the 100W criteria safely. Rather than design an amplifier with discretes, today it is usually quicker, faster and easier to debug the circuit when prepackaged operational amplifiers are used, as their performance is more than satisfactory for this and even more demanding applications. However, locating an op-amp that will put out 41.2 volts severely limits our choices.

If you are willing to accept a derating of output power, National Semiconductor's LM144 op-amps operate with supplies up to ±40V and boast a = ±25V typical output voltage swing. Motorola's MC1536 will swing ±32V running off of ±36V, but for performance up to and well exceeding our specs, take a look at the Analog Devices Model 171 module or one of Burr-Brown's 3580 series op-amps. Analog Device's 171 will run off of ±150V (±15V min), and guarantees an output swing of
$\pm(|V_S| - 10V)$ minimum. Burr-Brown's 3582J and 3583J op-amps are rated at

$\pm V_{CC}$ from ±40 to ±150VDC, with ouput currents of ±15mA and ±75 mA, respectively. These devices would be perfect even for higher power amplifier circuits, but for our purposes, the 3581J, which takes supplies from ±32VDC to ±75VDC and will put out ±30mA, with no compromise on conventional op-amp characteristics, is perfect. Thus, connecting the 3581J in the non-inverting amplifier mode as shown in Fig. 12d completes the core of the Class AB amplifier. The bandlimiting is achieved by first feeding the input signal through a 12dB/octave low-pass filter, as also shown in Fig. 12d.

So now we have designed a skeleton version of the core of our circuit, as standard Class AB amp. A practical circuit would necessarily include several types of protection circuits to protect the amplifier and/or loudspeakers from the various failure modes that can easily destroy both parts of your sound reproduction system. This additional circuitry would only confuse the issues at hand; I refer the reader to the bibliography for further information on suitable protection circuitry.

In designing the Class-D style circuits that will supply the necessary current at the desired voltage loads to the Class AB circuit, we must first take note of the necessary deviations from normal Class D operation required to make everything work. Look at Fig. 8 and examine the psuedo block diagram of the system to date. There are two Class-D style circuits in our model, one for each polarity of supply voltage. Once again, the following analyses will focus on the positive supply as we just have to invert all polarities of parameters and devices to realize the negative supply.

Now consider the requirements of the positive power supply. It must supply whatever current is necessary as dictated by the Class AB circuit, and maintain its output voltage at a designer-specified positive offset from the final output voltage, for $V_o > 0V$. For negative output voltages, $+V_{CC}$ will stay at the
V_o = Ov level to make the next zero crossing of V_o easier.

These voltage constraints imply a slight redesign in PWM circuitry from that considered before. As each supply voltage is of only one polarity, the PWM output stage should be connected between a large positive voltage

(V_{SS}) and ground, as opposed to a connection between bipolar supplies. This also means that the pulldown device should not have to sink as much current as the pullup, as the output is unipolar, and the pulldown serves to draw off "extra" energy for each cycle. In fact, the pulldown will be a diode, as the inductor will force the PWM output to go negative when the pullup switch open-circuits.

Power MOSFET transistors will be used for all active drivers for a number of reasons. Bipolar transistors are current-controlled current sources, while FETs (Field Effect Transistors) are voltage-controlled current sources. As voltages, in general, are much easier to program and determine than currents, the ability to use a voltage rather than a current as your control input is a major advantage. As a consequence of the nature of the FET, the input draws no current except when in the process of switching, when the gate-source capacitance must be charged or discharged (see Fig. 14). Because of this fact, power FETs exhibit switching times an order of magnitude or more faster than comparable bipolars, which greatly reduces power dissipation. In the steady state, a transistor switch consumes very little power, but the power consumption goes up as the transistor is switched from one binary state to the other through the linear region. Thus, the faster the switching time, the less time spent in the linear region, and the less power is wasted over time.

The slow switching speed of bipolar transistors is one of the problems that stood in the way of Class D technology for years. The other problem was the inavailability of MOSFETs, until recently, that could handle the current requirements of switching power circuits. Fortunately, these problems have been solved with the latest generation of power FETs, most notably International Rectifier's HEXFETs, which utilize a hexagonal geometry for efficient

current flow control and heat dissipation.

The piece de resistance (pun intended) of the case for power FETs is their saturation characteristic. Saturated FETs exhibit a resistive I_D vs. VDS characteristic, and HEXFETs with on-resistances as low as .055 ohms max are readily available.

For our purposes, we need power FETs that will source or sink up to 5A, can easily withstand a V_{DS} of 42V, and will switch quickly enough to be used in a 125kHz system. International Rectifier's IRF133 (n-channel) and IRF9533 (p-channel) HEXFETs are rated, respectively, at V_{DS}max of plus and minus 60V, continuous on-state I_{DS} of 12A and -10A minimum, and maximum total switching times
($t_{d(on)} + t_r + t_{d(off)} + t_f$) of 450nS and 480nS, 240nS typically for both devices. The period of the PWM will be $^1/_{125kHz}$ = 8μS, so the maximum switching times comprise 5% of a period. The other specs easily satisfy our requirements, and these devices are near the bottom of the HEXFET product line.

Having specified the PWM driver devices, let us return to the evaluation of the balance of PWM specifications and parts. In a nutshell, the entire PWM circuit will be shifted up in voltage from the analyses of Fig. 10. The oscillator and comparator lower limits will be readjusted to ground potential, and the new range of operation will be 0% < DC < 100% for
0V < V = < V_m, or
DC = $100^{V+}/_{V_m}$.

The entire Class K circuit is diagrammed in Figure 14. The PWM com-

parator and timing circuitry is all generated by the Motorola MC3590 Switch-mode Regulator Control Circuit, which is specifically designed for use in PWM systems. The PWM control voltage comes in at pin 6. The DC out/control voltage in transfer function has a negative slope; thus, the feedback connection to the positive op-amp terminal. The oscillator frequency is determined by the resistance and capacitance connected from pins 1 and 2, respectively, to ground. Pin 9 is a reference voltage, which is used to supply 2.2V to pin 7, the Dead Time Adjust pin. The Dead Time Adjust is used because pins 11 and 13 are both open-collector npn transistor outputs which are out of phase with each other and each exhibit a maximum duty cycle of 50%. Connecting them in parallel allows you to synthesize a 0% - 100% duty cycle PWM, and the Dead Time Adjust is used to limit the maximum output duty cycle so that the circuit can never just latch up. A 2.2V input to pin 7 limits the maximum duty cycle to 90%.

Pin 15 is an Inhibit input, and it is used in this application to effect what is called a 'soft-start.' On power-up, the voltage at pin 15 is zero volts and the PWM is shut off. As the capacitor charges up, the PWM turns on when the voltage at pin 15 reaches five volts. This technique prevents large inrushes of current to the circuit on power-up. The balance of the connections to the MC3520 are power connections and wirings applicable to this particular type of function, as the chip is designed to control various types of PWM circuits.

With the addition of a few components and circuits around the PWM, our skeleton Class K amplifier model is complete. In Fig. 14, I have connected the L-C network necessary to smooth out the PWM output, and used the filtered output as a feedback signal to compare with the signal presented to the PWM via yet another op-amp. This op-amp is sourced by a differential amp, which sums a rectified version of the band-limited audio signal (precision-

rectified by the previous stage)

with the bias voltage V_B necessary to keep the Class AB circuit out of saturation.

Once again, the complete schematic of the skeleton version of the Class K amplifier is shown in Fig. 19. Please remember that this model has been built only on paper to date, and I have probably overlooked some of the real-world considerations that will only become apparent in the laboratory. Please also note that this is a skeleton version designed to introduce you to the concepts behind the design and construction of such an amplifier. A physical realization of this device would have to have protection circuitry included to ward off the various evils that could befall any such system in real use. The bibliography lists sources of information which may be of assistance in the design and construction of this device, in addition to hints as to the pros and cons of various protective circuitry that could be employed.

This amplifier is designed for efficiency, but due to the theoretical nature of the device, the efficiency can only be approximated. For $V_O(t) = V_o \sin \omega t$ across the load resistor R_L, $P_O(t) = \frac{V_O^2(t)}{R_L} = \frac{V_o^2}{R_L} \sin^2 \omega t$ and $\bar{P}_o = V_o^2/4R_L$ The power input to the Class AB subsystem (over one-half period, ignoring bias current) is $P_{i_{AB}}(t) = V_{CC}(t) \cdot I_C(t) = (2V + V_O(t)) \cdot I_C(t) = \frac{2V}{R_L} V_o \sin \omega t + \frac{V_o^2}{R_L} \sin^2 \omega t$, where I have used $V_{CE}(\text{ideal}) = 2V$. Thus, $\bar{P}_{i_{AB}} = \frac{2V \cdot V_o}{\pi R_L} + \frac{V_o^2}{4R_L}$

In approximating the power dissipated in the PWM, it can be easily shown that the losses associated with switching times are too negligible to be considered. The primary source of dissipation will be conduction loss; that is, the $I_D^2 R_{ON}$ dissipated while the FET is turned on. Now, if the circuit is working efficiently, the energy which flows through Q_3 during

t_{on} of every cycle is being channelled to the load for the most part, and during t_{off}, D_5 pulls off a small amount of excess energy to stabilize the feedback system. Thus, Q_3 dissipates $I_D^2 Ron$ watts of power for t_on seconds every period T, or $I_D^2 RonDC$ watts every period. As $DC = \frac{Vin}{Vm}$, the ratio Vin/Vm is analogous to $\frac{Vo(t)}{Vomax}$, so $P_{D_{FET}}(t) = \frac{I_D^2 Ron}{Vomax} Vo \sin\omega t$, $\bar{P}_{DFET} = \frac{I_D^2 Ron}{\pi Vss} Vo$

thus, $\bar{\eta} = \frac{\bar{P}_{in}}{\bar{P}_{total}} = \frac{\frac{Vo^2}{4R_L}}{\frac{2V \cdot Vo}{\pi R_L} + \frac{Vo^2}{4R_L} + \frac{I_D^2 Ron}{\pi Vss} Vo} = \frac{Vo}{\frac{1}{\pi}\left[\frac{I_D^2 Ron R_L}{Vss} + 8V\right] + Vo}$ which, for I_D = 6A, R_{on} = .25 , R_L = 8 and V_{SS} = 45V, $\bar{\eta} = \frac{Vo}{3.05V + Vo}$, so 50% efficiency is achieved for $V_o > 3V$, a at $V_o = V_{omax} = 40V$, $\bar{\eta}$ = 93%. At the Class Ab trouble point of $V_o = \frac{2}{\pi} V_{SS}$ = 28.65V, $\bar{\eta}$ = 90.4%. Thus, it appears that the desired goal of efficiency wihtout sacrificing direct-coupling may be achieved. Of course, I must stress again that these figures are theoretical, but they are definitely a confident indication of the possibilities which still exist for the advancement of the state-of-the-art of high fidelity.

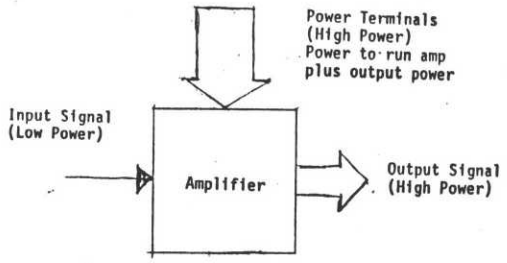


FIGURE 1 - Schematic Representation of an Amplifier

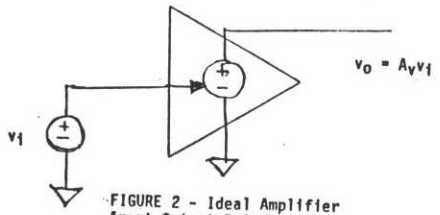


FIGURE 2 - Ideal Amplifier Input-Output Relationship

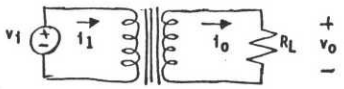


FIGURE 3 - Transformer Relationships

$P_{out} = P_{in}$ (ideal)

$P_{out} < P_{in}$ (actual)

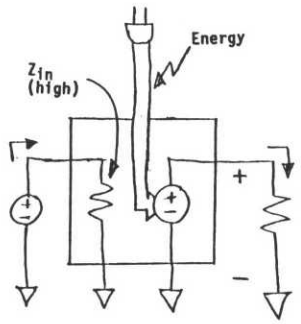


FIGURE 4 - Ideal Amp (Again)

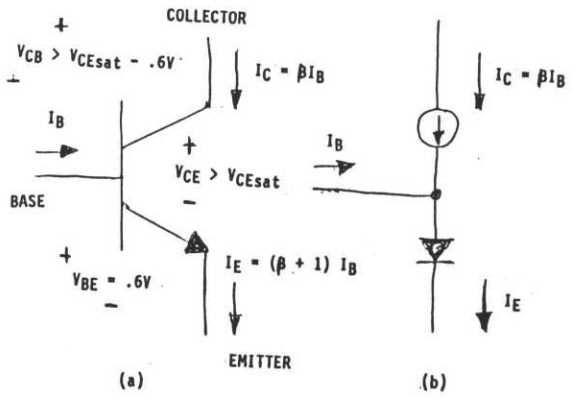


FIGURE 5 - NPN Transistor Models

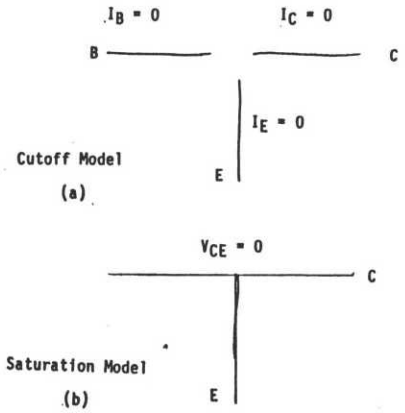
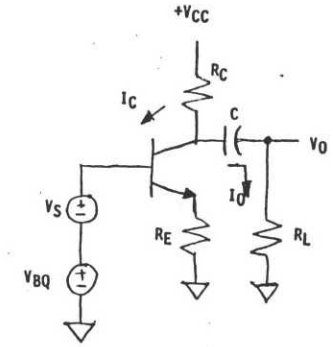
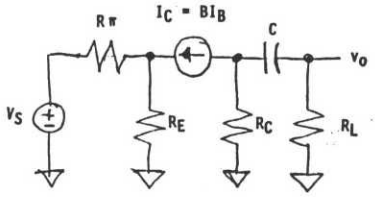


FIGURE 6 - Transistor Cutoff and Saturation Models

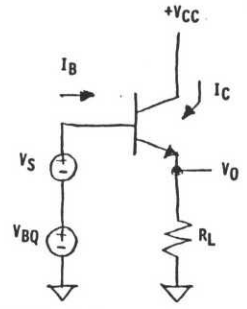


(a)
Large-Signal Model

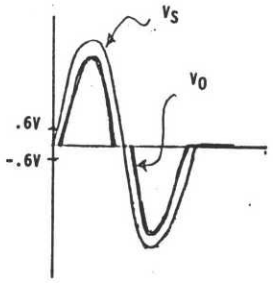


(b)
Small-Signal
(Incremental) Model

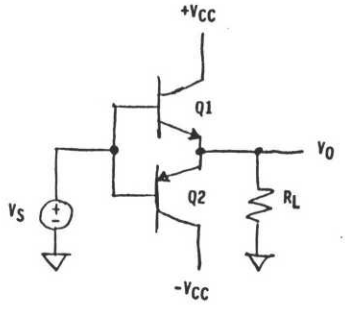
FIGURE 7 - Class A Amplifier Circuits



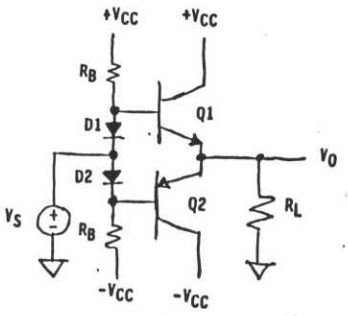
(a) Basic Concept, Unipolar



(c) Class B Notch Distortion



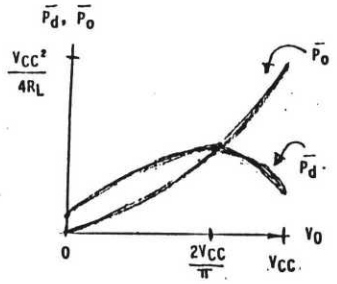
(b) Class B, Bipolar Signals

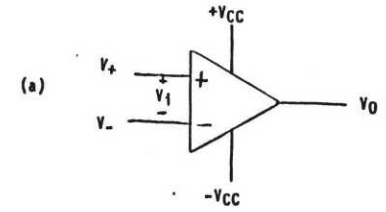


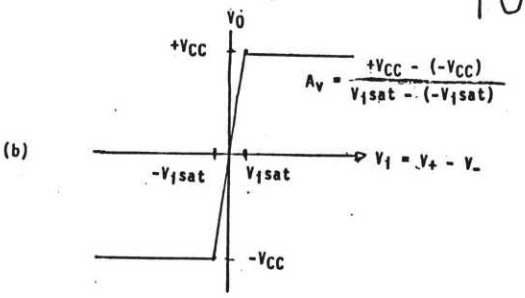
(d) Class AB Amplifier

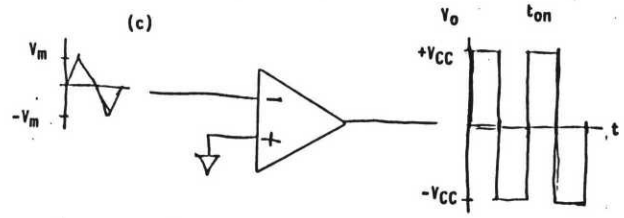
FIGURE 8 - Class B/AB Amplifier

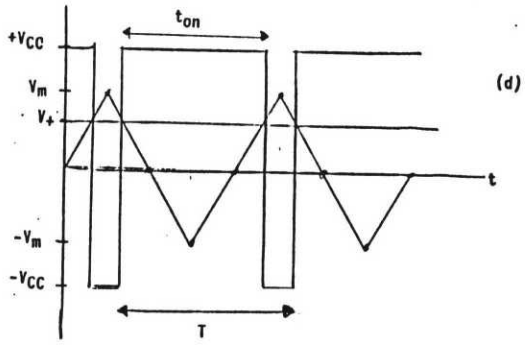
Figure 9 - $\overline{P_d}$ and $\overline{P_o}$ of Class AB Amplifier

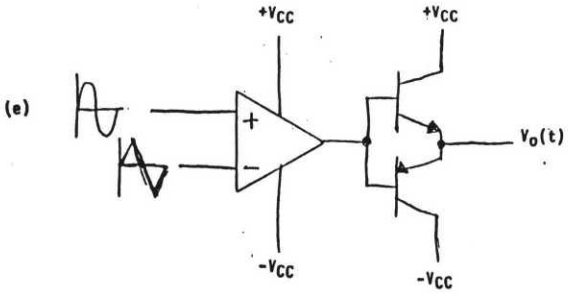












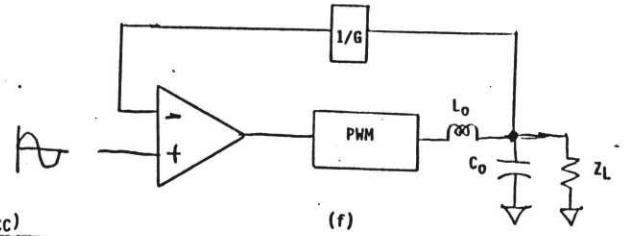


Figure 10 - PWM Circuits and Waveforms

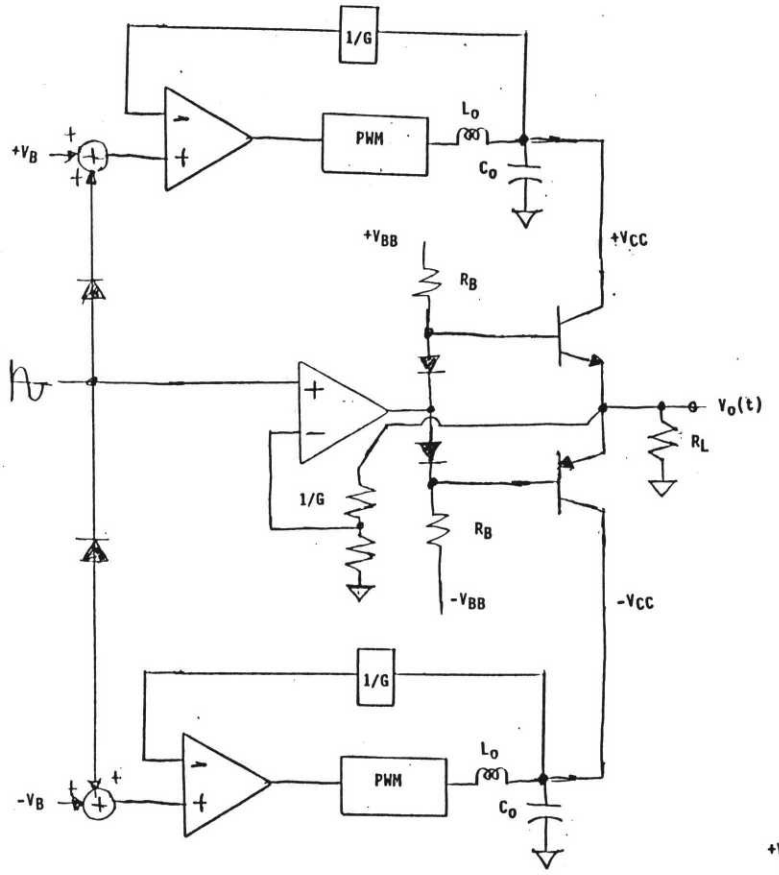


Figure 11 - Class D Amplifier Schematic Representation

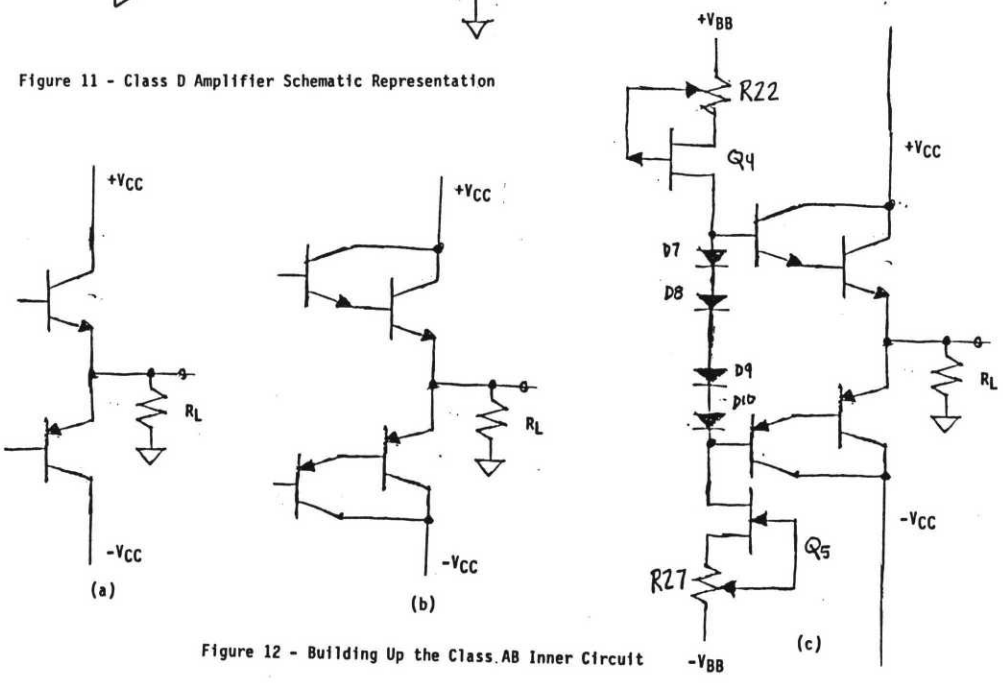
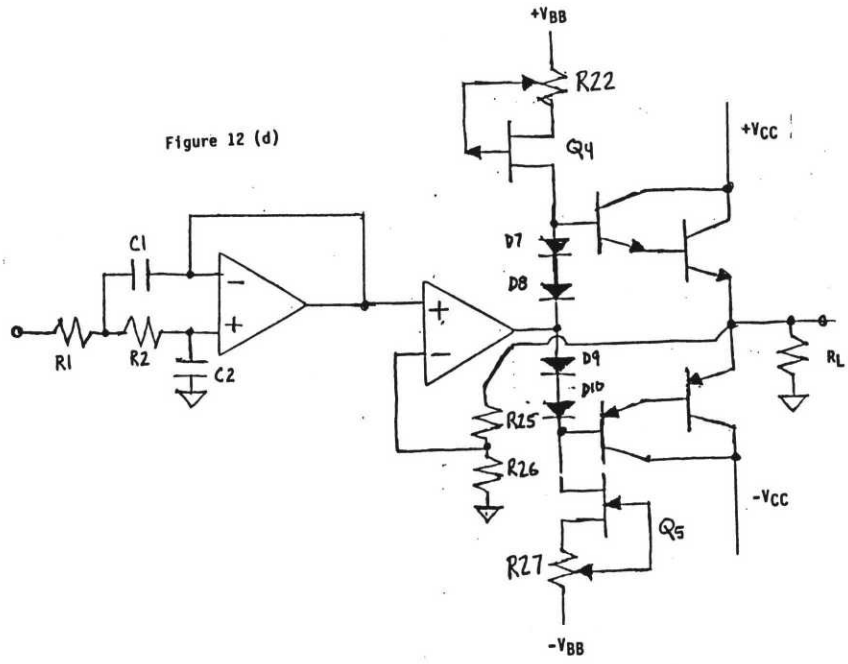
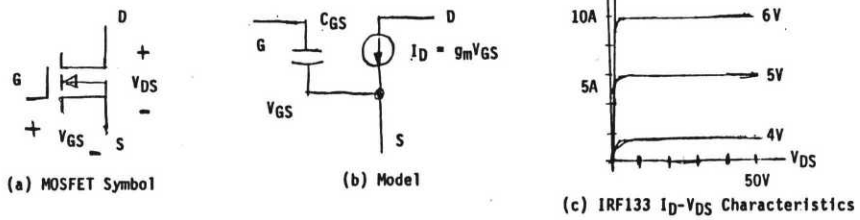


Figure 12 - Building Up the Class AB Inner Circuit

Figure 12 (d)





(a) MOSFET Symbol

(b) Model

(c) IRF133 I_D-V_{DS} Characteristics

Figure 13 - N-Channel Power MOSFET Data

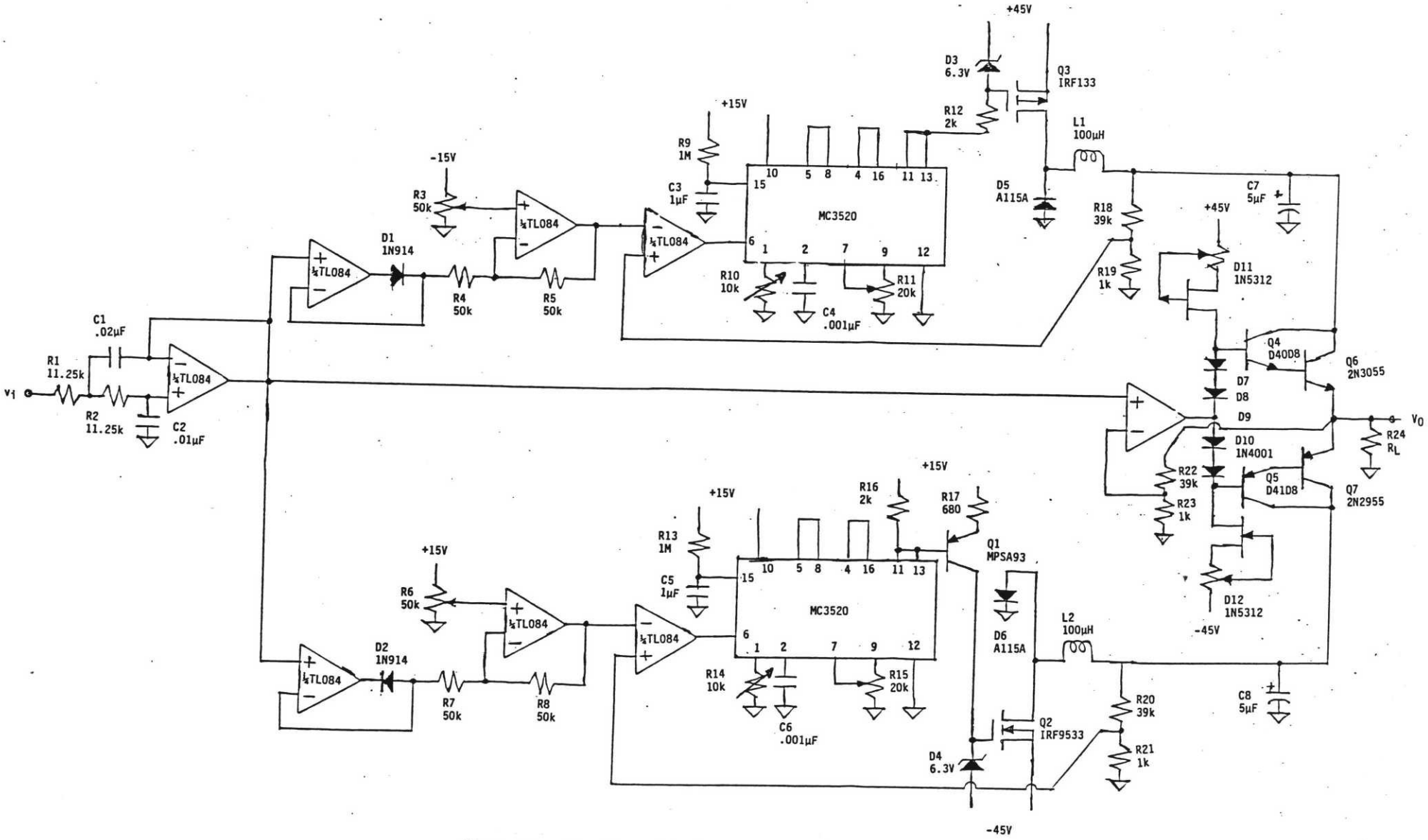


Figure 14 - The Class K Amplifier - One Channel

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