Nanosystems: From the Lab to the Fab

by

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Abstract

Exponential improvements in computing performance have impacted and improved nearly every aspect of our lives: from education to transportation to healthcare. And with continued gains, applications which were once science fiction – from fully-autonomous vehicles to personalized healthcare – will soon be a reality. Yet at the exact moment these next-generation applications are poised to once again revolutionize our lives, gains in computing performance are slowing. The conventional approaches relied on to improve computing – mainly relentless physical and equivalent scaling of devices – are reaching fundamental limits, and while progress will undoubtedly continue, the rate of gains has already slowed dramatically over the last decade. Therefore, to enable these next-generation applications, new approaches to computing systems are required. Rather than rely on a single approach, coordinated advances across the system stack – from new technologies to new system architectures – are required to overcome today's challenges. This is embodied by "Nano*Systems*", which use emerging nanotechnologies to realize new system

architectures to enable new applications.

Yet however intellectually compelling or interesting nanosystems are, the problems facing computing today are very real and very current. Unfortunately, despite the promise of nanosystems, nanosystems were exclusively of academic interest. All nanosystem demonstrations were fabricated in academic labs, and there were many challenges that prohibited nanosystems from transferring into industry and thus into the real world.

This thesis addresses this critical problem. By demonstrating the world's first adoption of nanosystems within industry, this thesis provides both a specific path forwards as well as a general approach of how to transform promising nanosystems in theory into practical systems that can impact our daily lives. To transform nanosystems from the "lab" to the "fab", this thesis must address challenges that span the entire stack: from low-level material optimizations, to semiconductor device engineering, to circuit and system design, up to architectures and application implementation. As a case-study, this thesis focuses on carbon nanotubes and monolithic three-dimensional integration as the specific implementation of a nanosystem, yet the lessons and conclusions from this work are applicable to a broad set of emerging nanotechnologies and nanosystems. Beyond technology, this thesis shows unequivocally that nanosystems should – and can - be transferred from academic "labs" into commercial "fabs", providing a realistic and feasible path forwards for computing to continue to improve and revolutionize the world we live in.

Thesis Supervisor: Max Shulaker

Title: Associate Professor of Electrical Engineering and Computer Science

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It was February 4, 2016 10.30 PM at Kharagpur, West Bengal, India when I received my acceptance letter from EECS, MIT. I was thrilled to get an opportunity to study at the best engineering school in the world. However, when I visited Boston a month later, I witnessed Massachusetts winter in full swing and, I was not sure if Boston would be the right place for me. While I was toying with alternate options, it was early April when I received an email from Prof. Max Shulaker, then still a graduate student at Stanford. As an incoming faculty at MIT, he said he was interested in my application and would love to schedule a meeting. In our first conversation over skype I was excited to witness that he had all the qualities that I could wish for in an advisor: a willingness to take risks in novel technologies, a willingness to ask difficult questions, and a strong desire to solve grand challenges that the world faces today. That's why I chose to do my PhD at MIT.

As an aspiring academic, I wanted to work in a new group so that I learn from the same challenges that a new faculty faces and Max gave me the perfect opportunity to do that. Grad school was like a roller coaster ride with some solid highs and then sudden lows, but through it all I always felt supported. One thing that made Max stand out as an advisor was empathy during tough times. He taught me how to write papers, give talks and foremost how to conduct research. Prof. Shulaker, I am incredibly grateful to be advised by you with all the help you have provided me from every single presentation and paper to working late at night in Kyoto to make my demo work at VLSI'2019.

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- **Srimani, T.***, G. Hills*, M. Bishop, C. Lau et al. "Heterogeneous Integration of BEOL Logic and Memory in a Commercial Foundry: Multi-tier Complementary Carbon Nanotube Logic and Resistive RAM at a 130 nm node" *(Joint Focus in circuits and technology)* In *2020 IEEE Symp. on VLSI Tech. and Circ*.
- **Srimani, T.**, J. Ding*, A. Yu* et al. "Comprehensive Study on High Purity Semiconducting Carbon Nanotube Extraction" *in submission (2021)*

Chapter 1: Introduction

1.1 Background

I have vague memories of the first day I saw a computer. It was sometime in 1999, while I was still in kindergarten. However, I distinctly remember my feeling that day. I was completely in awe when I saw my teacher play the game Mario in a heavily pixelated color monitor. And then the journey began – from bulky desktops with floppy disk readers to handheld smartphones where I can edit word documents, trade stocks, learn from MOOCs and even have telemedicine appointments in zoom.

In the past few decades, exponential gains in computing system performance have enriched nearly every aspect of our lives. And with continued gains, applications which were once science fiction – from fully-autonomous vehicles to personalized healthcare – will soon be a reality. At this very moment when improvements in technology brings us great promises, gains in computing performance have been slowing down.

So, *how are we going to continue this*?

The first option is to continue with what has worked in the past - relentless miniaturization of transistors, known today as Moore's Law. Yet continued device scaling is already resulting in diminishing returns, as Dennard Scaling (which describes the gains afforded by physical and equivalent scaling of devices) has already plateaued over a decade ago.

The second option is to use new and improved transistor technologies. For instance, emerging nanomaterials and nanodevices promise devices with improved device characteristics that can also scale even beyond the limitations of today's silicon devices [Brady 2016]. Yet it is critical to recognize that device performance alone does not solely dictate system performance: in fact, device inefficiencies often account for a small portion of total system-level inefficiencies.

Particularly for future big and abundant-data applications, the majority (>80%) of energy and time spent in "computing" is actually energy and time spent moving data between off-chip memory and on-chip compute (referred to as the "memory wall"). Thus, improving the underlying devices alone does not address other system challenges, and thus even the best device in the world would only realize limited benefits for end-applications.

The third option is to rely on architectural "tricks" such as designing multiprocessors and application specific accelerators. Yet such techniques are widely in use today, and there are only a limited number of "tricks" that can be employed (e.g., applications can only leverage a limited amount of parallelism, or the accelerator itself will become constrained by how fast it can receive data from off-chip memory as well, another instance of the memory wall).

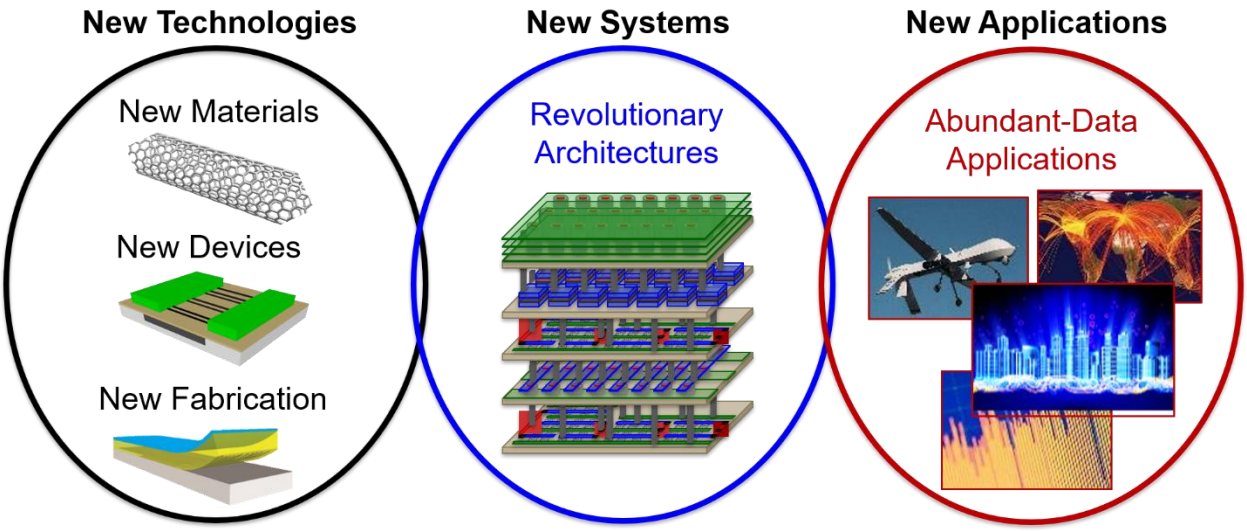


Fig. 1.1 Nano*Systems* : Nanosystems use emerging nanotechnologies to realize new system architectures targeting future abundant-data applications

While any of the above options may solve one of these "walls" (such as the scaling wall, power wall or the memory wall), it almost certainly will fail to solve all of the challenges simultaneously. Thus, it is evident that conventional approaches will not be sufficient to meet the demands of the next wave of computing. As a result, we need coordinated advances across the entire system stack-

starting from material technologies to system architectures, in order to enable the next generation of computing systems. The solution is what we call "Nano*Systems*". Nanosystems use emerging nanotechnologies to realize new system architectures to address many of the problems that computing systems face today (such as the scaling wall, power wall, memory wall etc.) simultaneously enabling orders of magnitude gains in system performance (characterized by energy-delay product, or, EDP [Shulaker 2017, Sabry 2015]).

Unfortunately, despite the promise of nanosystems, there are still many obstacles that prevented nanosystems from being realized in the real world, in commercial facilities. Firstly, there are challenges in material synthesis (many new materials cannot be synthesized or deposited uniformly in large area substrates or with high reliability). Secondly, at the device-level, new fabrication techniques are required for these new materials and devices. Thirdly, at the system level, new design and fabrication techniques are needed for new system architectures such as new three-dimensional (3D) integration techniques, which further impact the device and material level requirements. And finally, all of the above must be done in a compatible way with existing industry infrastructure to allow for a foundry integration of these new technologies. Due to all of these challenges, nanosystems have only been demonstrated in academic facilities.

1.2 Contributions

In this thesis, I will present my work leading to the first demonstrations of nanosystems in the real world, building these systems in commercial fabrication facilities and foundries for the first time. To make this concept a reality, I have relied on new coordinated approaches that span the entire system stack – starting from new technologies such as carbon nanotubes that enable improved transistors [Hills 2018] to new system architectures such as monolithic 3D integration [Sabry 2015] that enables dense integration between compute and memory. Therefore, in this

thesis, I touch on every level of the computation stack from improving material technologies to device engineering to system and architecture design –

(a) **Material Level Improvements:** Starting at the material level, I show a reliable path towards extracting high purity solution processed semiconducting CNTs (s-CNTs) with a 99.99% s-CNT purity required for fabricating carbon nanotube field-effect transistor (CNFET) based digital VLSI systems. Using extensive electrical testing of transistors (spanning 10,000 CNFETs with over 10 million CNTs per solution), I find the best combination of CNT synthesis source as well as polymer wrapping for the solution processed s-CNT extraction process. In addition, this work also analyzes key device metrics (I_{ON}, I_{OFF}, threshold voltage, etc.) of CNFETs fabricated using these high purity s-CNT solutions, showing how the choice of the CNT synthesis source can be decoupled from the choice of the polymer in the sorting process.

(b) **Transistor Level Improvements:** In this thesis, I show the impact of CNFET device geometry engineering on digital VLSI energy efficiency (characterized by energy-delay product, EDP) as well as scaling. This work demonstrates how back-gate CNFETs enable: 1) >1.6× EDP benefit for CNFETs due to reduced parasitic capacitances (versus top-gate CNFETs), 2) aggressive FET scaling to sub-3-nm technology nodes. Additionally, I investigate the underlying physics of off-state leakage behavior in CNFETs through experiments and experimentally-calibrated simulations and demonstrate paths for mitigating this leakage by further modification of the back-gate FET geometry.

(c) **New System Architectures (Monolithic 3D Integration):** Taking the CNFET technology one step further, I demonstrate a hardware prototype of a monolithic three-dimensional (3D) imaging system that integrates CNFET computing layers directly in the back-end-of-

line (BEOL) of a conventional silicon imager. Such systems can transform imager output from raw pixel data to highly processed information. To realize the imager, I fabricated three vertical circuit layers directly on top of each other: a bottom layer of silicon pixels followed by two layers of CMOS carbon nanotube FETs (CNFETs) (comprising 2,784 CNFETs) that perform in-situ edge detection in real-time, before storing data in memory. This approach promises to enable image classification systems with improved processing latencies.

(d) **Foundry Integration:** Finally, as a result of these material, device and system level advances, this work enabled a foundry transfer of the underlying CNFET technology, showing back-end-of-line (BEOL) integration of multi-tier CNFET logic with non-volatile resistive memory (RRAM) within a commercial foundry. The foundry process uses back-gate CNFETs fabricated with the improved high purity s-CNTs as demonstrated in this thesis. These CNFETs and RRAM arrays are then used to realize monolithic 3D integrated circuits at a commercial 130 nm node technology. This is the first emerging nanotechnology to ever reach this level of maturity.

1.3 Impact

The impact of this thesis is three-fold – (1) I show improvements in the state-of-the-art of the exact technologies used to demonstrate nanosystems (CNTs, monolithic 3D integration) (2) the knowledge gained in the specific technologies can be translated to other emerging materials, as the same take-aways can be applied to other low-dimensional materials, and (3) I show how nanosystems in general are a promising and feasible approach that can transfer from academic "labs" to commercial "fabs", in order to achieve continued gains in computing system performance.

1.4 Outline

Chapter 2 shows how to reliably extract high-purity semiconducting CNTs and is partly reproduced from [Srimani 2021]. Chapter 3 is based on [Srimani 2018] and presents back-gate FET geometries to realize highly scaled CNFETs beyond the scope of conventional top-gate and gate-all-around FETs with simultaneous energy efficiency benefits in digital VLSI circuits. Chapter 4 is based on [Srimani 2019a] and reveals the underlying physics behind excess leakage current in CNFETs and presents techniques which can further improve this leakage behavior with additional improvements in digital circuit EDP. Chapter 5 goes beyond CNFETs and demonstrates a monolithic 3D IC with multi-tier CNFET circuits directly integrated over a Si CMOS imager. This chapter has been partly reproduced from [Srimani 2019b]. Chapter 6 is based on [Srimani 2020] and presents foundry integration of CNFETs and demonstrates the first monolithic 3D ICs manufactured in a commercial foundry. Chapter 7 concludes the thesis.

Chapter 2: Comprehensive Study on High Purity Semiconducting Carbon Nanotube Extraction

2.1 Background

Physical and equivalent scaling of silicon-based field-effect transistors (FETs) has been a major driving force to improve computing energy efficiency for decades. However, continued silicon scaling is growing increasingly challenging [Kuhn 2012, Bardon 2016], motivating work on emerging nanotechnologies. For instance, one-dimensional carbon nanotubes (CNTs) are cylindrical nanostructures comprised of a single atomic layer of carbon atoms and have exceptional electrical, mechanical and thermal properties. Carbon nanotubes can be used to form carbon nanotube FETs (CNFETs), which are a leading candidate for realizing energy-efficient digital circuits [Wei 2009, Chang 2012, Franklin 2012b, Chen 2008, Baughman 2002, Javey 20003]. CNFETs (illustrated in Figure 2.1) follow the same general structure as traditional silicon metal-oxide-semiconductor FETs (MOSFETs), but with CNTs forming the channel of the transistor with lithographically defined source, drain and gate regions [Shulaker 2013, Brady 2016, Liu 2020, Srimani 2018, Hills 2018]. Owing to CNT's ultrathin body as well as superior carrier transport [Javey 2003, Brady 2016], digital VLSI circuits made from CNFETs are projected to achieve >7× energy efficiency benefit (characterized by energy-delay product, or, EDP) over similar systems made using silicon FETs even when compared at futuristic highly-scaled 2 nm technology node [Gilardi 2021, Hills 2018, Sabry 2015]. Moreover, rapid progress has demonstrated high performance CNFETs as well as CNFET based CMOS digital circuits, progressing from a single-bit turing-complete computer to a complete 16-bit RISC-V microprocessor [Hills 2019, Brady 2016, Liu 2020, Shulaker 2013, Cao 2017, Shulaker 2017, Amer 2019, Ho 2019, Srimani 2019b, Kanhaiya 2019].

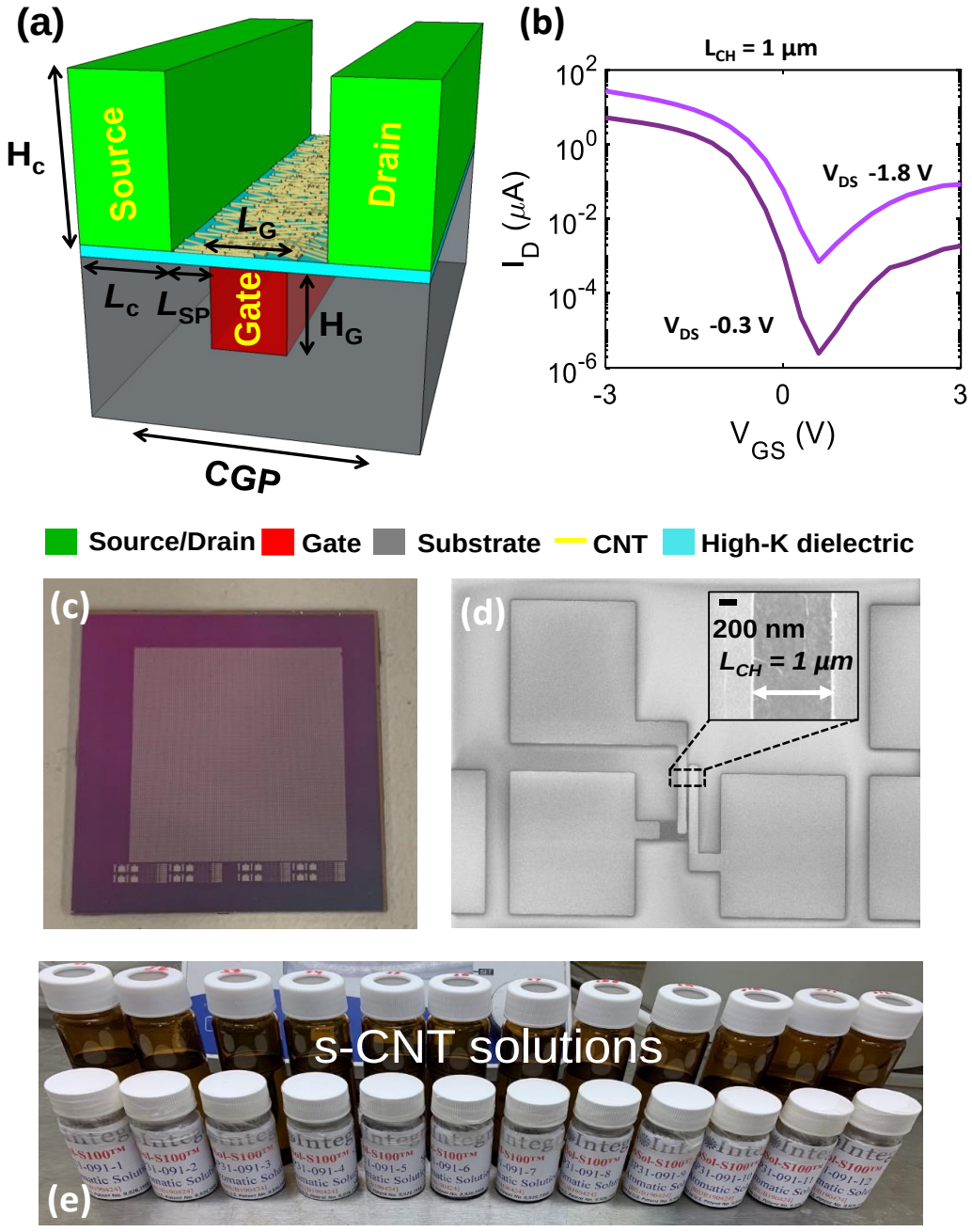


Fig. 2.1. (a) Schematic of back-gate CNFET. L_{CH} is the physical channel length, L_{SP} is length of the intrinsic CNT region. (b) Experimentally measured I_D-V_{GS} characteristics for a transistor with L_{CH}=1 µm (measured at room temperature). Device parameters listed in Table 2.1. (c). Die Micrograph (d) Scanning Electron Microscopy (SEM) images of fabricated CNFETs (channel zoomed in top right). (e) s-CNT solutions tested for understanding the impact of precursors (CNT source, polymers etc).

Yet despite this progress, experimental measurements of CNFETs often exhibit substantial off-state leakage current (I_{OFF}) due to presence of metallic CNTs. If such CNFETs are fabricated within circuits, they result in substantially increased leakage power and potential incorrect logic functionality [Hills 2019, Zhang 2012, Hills 2015, Shulaker 2015]. To address this major challenge, recent work [Hills 2019] has developed a circuit design technique known as *Designing REsliency Against Metallic CNTs* (*DREAM*), which reduces the s-CNT purity requirement of a digital VLSI circuit from 99.999999% to 99.99%, without imposing any additional processing steps. To meet this requirement, a wide variety of techniques have been investigated. For instance, multiple works have attempted to modify CNT synthesis conditions to primarily synthesize s-CNTs. While successful, the highest purity reported is only ~99% s-CNT purity (measured optically) on only small-area substrates [Samanta 2014, Yang 2017]. Thus, significant work has attempted to remove remaining m-CNTs post-synthesis, primarily through solution-based sorting [Samanta 2014] (ranging from gradient-density centrifugation to DNA assisted chromatographic purification to aqueous two-phase separation to conjugate polymer extraction). Yet despite years of progress, no approach has been shown to meet all requirements, as it either does not achieve sufficient s-CNT purity[a], it introduces contaminants which prohibit use within commercial semiconductor manufacturing facilities, or it is difficult to scale to high-volume production. Exacerbating progress is the fact that even with a single approach, there are multiple parameters that can be tuned independently, creating a massive design space of permutations which is challenging to explore. For instance, for conjugate polymer extraction, different CNT synthesis

[a] The best reliable solution sorting techniques report a s-CNT purity estimate of around 99.9% optically [Ding 2015]. Approaches that involve electrical testing of CNFETs to characterize the s-CNT purity [Liu 2020, Tulevski 2013, Lei 2019], either use measurements at low drain bias (V_{DS}) which improves the I_{ON}/I_{OFF} ratios [Brady 2016, Srimani 2019b], or does not use a large enough sample size of transistors to measure purity accurately. These techniques although correct in theory leads to very optimistic estimates of solution-based s-CNT purity.

sources can be initially used to generate the raw starting materials, and then different conjugate polymers can be used to selectively sort for the s-CNTs.

In this work, we demonstrate for the first time that conjugate polymer extraction (the *only* commercially available approach that has been integrated within commercial silicon foundries and major semiconductor manufacturing facilities [Bishop 2020, Srimani 2020]) can achieve the required >99.99% s-CNT purity for VLSI systems – confirmed through extensive electrical measurements and characterization. This is accomplished by systematically synthesizing, fabricating, and characterizing permutations of CNT synthesis sources and conjugate polymer choices, resulting in the optimal CNT solution. Moreover, through this detailed analysis, we also elucidate that the ideal CNT synthesis source as well as the ideal conjugate polymer used for sorting are independent from one-another. This important observation enables both to be optimized independently, greatly simplifying future CNT solution optimization work.

2.2 Carbon Nanotube FET fabrication process

The CNFET fabrication process has been reported previously and is described in [Hills 2019]. Figure 2.1a-b shows the schematics and measured electrical transfer characteristics (I_D-V_{GS}) of a typical back-gate p-channel CNFET. We use back-gate CNFETs for this study since they follow the fabrication process that is integrated in commercial foundries at a scaled ≤130 technology nm node and have been used to realize uniform and reproducible CNFETs and CNFET logic over 200 mm substrates [Bishop 2020, Srimani 2020]. s-CNTs dispersed in a solvent (described below) are deposited at room temperature directly onto pre-fabricated high-k dielectric/ metal gate stack on silicon substrates. Typical SEMs after deposition can be seen in Figure 2.2e-f (more SEMs in Figure 2.3). Following deposition of the CNTs, CNTs outside of the channel region of the CNFETs are removed by etching in oxygen plasma. Finally, source and drain contacts are aligned to the

pre-fabricated gate stack and lithographically defined. A detailed process flow is shown in appendix A1.2.

2.3 High Purity Semiconducting CNT extraction process

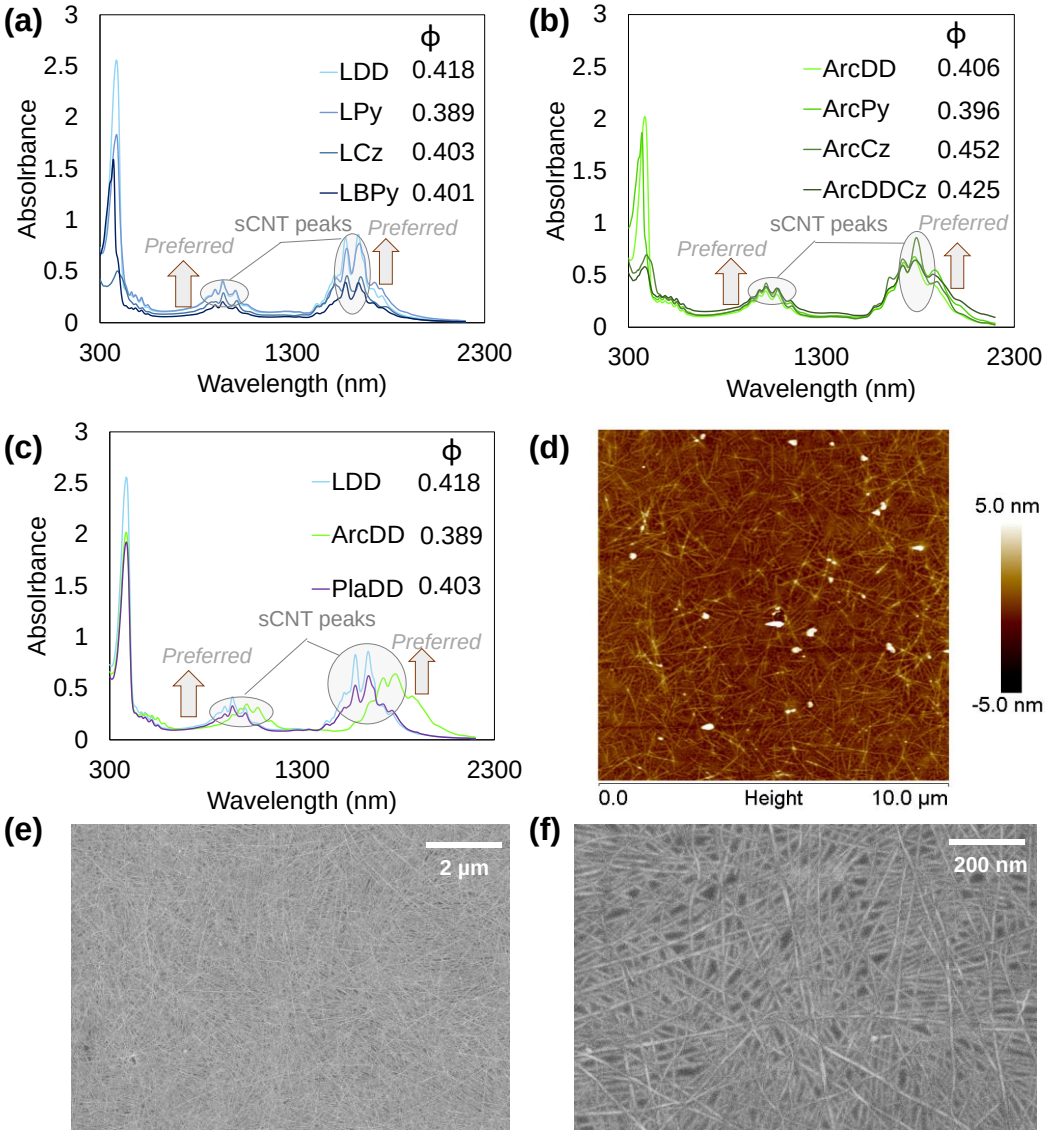


Fig. 2.2. UV-Vis-NIR spectroscopy of sCNT solutions (solution followed by acronyms are listed in Table 2.2) (a) for laser ablation CNTs wrapped with PFDD, PFPy, PCz and PFBPy (for more details about polymers see Table 2.2) (b) for arc discharge CNTs wrapped with PFDD, PFPy, PCz and a mixture of PFDD and PCz (c) for laser ablation, arc discharge and plasma CNT sources wrapped with PFDD. Measured absorption peak ratios (ϕ) from UV-Vis-NIR spectrum for each solution is reported in the legend

as a qualitative optical estimate of the solution s-CNT enrichment (more details in prior works [Ding 2015]). Although higher ϕ may indicate higher s-CNT content, it cannot differentiate between low band-gap CNTs and metallic CNTs. (d) AFM characterization of CNT length for laser ablation CNTs (LDD solution, same method is applied to estimate CNT length for each solution, more information in Figure A10.1-3). (e-f) SEM characterization of uniform CNT deposition on top of die surface for laser ablation CNTs (LDD solution).

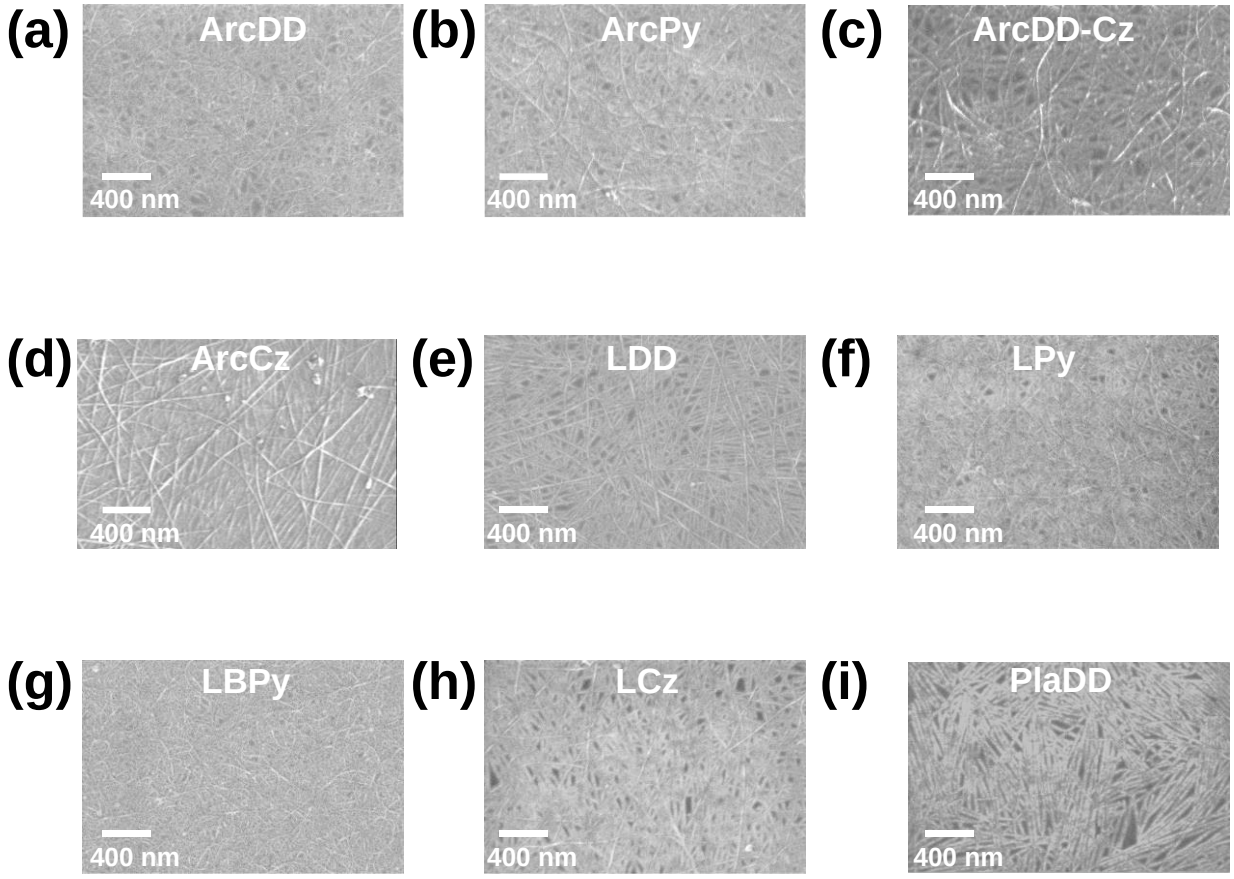


Fig. 2.3.: SEMs of different CNT solutions after deposition on wafer, using semiconducting CNT (sCNT) solutions extracted from different CNT sources and polymers - (a-d) arc discharge CNTs (e-h) laser ablation CNTs (i) plasma CNTs. Table 2.2 lists all the different CNT sources and polymer types.

For the CNT solutions, as described previously, an extremely diverse combination of CNT synthesis sources and conjugate polymers have been investigated in literature. Here, we restrict our analysis to the leading contenders based on literature [Wang 2015, Samanta 2014]. For the starting CNT material, the CNT synthesis source is chosen to be either Arc Discharge, Laser

Ablation, or Plasma. For the conjugate polymer, we use either PFPy, PFDD, PCz, or PF12BPy (listed in Table 2.2, see further details in appendix, Figure A9.1). As the preparation of the CNT solutions is a critical aspect of this work, we detail the process flow below:

The enhanced hybrid conjugate polymer extraction (eh-CPE) process includes a traditional hybrid conjugate polymer extraction (h-CPE) and then a final conditioning treatment [Ding 2015]. The eh-CPE process is started by dispersing a mixture of acid treated raw SWCNTs (obtained from different synthesis sources) with the polymer PFDD (or PCz) in toluene at ~1/1 of polymer to CNT (P/CNT) ratio in all the different starting solutions. Each solution went through a sonication step (30-minute tip sonication) followed by an ultracentrifugation step (30 minutes, 12500 rpm, RCF:23700g). The extracted solution (i.e., the supernatant) was mixed with silica gel, sonicated (30 minutes), and then centrifuged (30 minutes, 12500 rpm). The supernatant collected from this centrifugation step was filtered using a PTFE membrane to collect a black film of PFDD (or PCz) wrapped CNTs with a polymer/CNT ratio of ~1/1. For the samples with a polymer other than PFDD or PCz (i.e., PFPy and PFBPy), a polymer exchange step was performed on a PFDD wrapped CNT, to completely replace PFDD with the corresponding polymer (i.e., PFPy and PFBPy). The polymer exchange [44] step was performed as follows. First, PFPy (or PFBPy) was mixed with a PFDD/CNT and then thoroughly dispersed in toluene by bath sonication (2h), and filtered using a PTFE membrane to collect a PFPy/CNT film. These two steps were repeated again to complete the polymer replacement. After all of the polymer-wrapped CNT samples were generated, the films were re-dispersed in toluene to undergo a set of additional conditioning treatments to further improve the s-CNT purity as well as solution stability. It was done by adding extra wrapping polymer to adjust the polymer/CNT ratio to ~4/1 from ~1/1 and then undergoing a 2nd hybrid process with a centrifugation (12500 rpm, 30 mins) to yield pure s-CNT solution. These

pure s-CNT solutions were purged and sealed under nitrogen ambient before deposition on pre-fabricated high-k dielectric/metal gate stacks for CNFET fabrication. A more detailed version of this eh-CPE process can be found in appendix, Figure A9.1.

Figure 2.1e shows the s-CNT solutions (all dispersed in toluene) used for this experiment. UV-Vis-NIR absorption spectrum for the solutions were performed using a spectrophotometer (Cary 5000, Varian) over a wavelength range from 300 to 2100 nm (Figure 2.2 a-c). CNT length post-sorting is measured using AFM (sample AFM for laser ablated CNTs wrapped in PFDD in Figure 2.2d, length distributions in appendix, Figure A10.1-3).

2.4 Experimental Results

To compare the permutations and impact of CNT synthesis sources and conjugate polymers, we fabricated and electrically characterized 10,000 CNFETs for each CNT solution. Each CNFET is fabricated with a 20 μm width to contain an average of 1000 CNTs (confirmed through SEMs, Table 2.1 shows further details of the transistor geometries fabricated for these measurements). Thus, a total of 10 million CNTs were measured for each CNT solution, enabling accurate extraction of s-CNT purity (see appendix A8 for further details).

To characterize the CNFETs, we measure the I_D-V_{GS} transfer characteristics of all 10,000 CNFETs per solution, enabling the extraction of key device metrics such as on-current (I_{ON}), off-current (I_{OFF}), I_{ON}/I_{OFF} ratio and threshold voltage (V_T) (Figure 2.5a-e). Importantly, we characterize the CNFETs with a drain bias up to V_{DS}=-1.8V in stark contrast to many prior works that characterize and claim s-CNT purity based on low V_{DS} [Liu 2020, Tulevski 2013, Lei 2019] (sometimes using V_{DS} <50mV). This distinction is critical, as binning CNTs between two binary bins of m-CNT vs.

s-CNT (as is conventional in the field) leaves substantial grey area for small bandgap CNTs[b]. With small V_{DS}, small bandgap CNTs can still have high I_{ON}/I_{OFF} ratio, and thus appear more as a s-CNT. Yet at high V_{DS}, small bandgap CNTs have low I_{ON}/I_{OFF} ratios [Brady 2016, Srimani 2019] often <10, and thus essentially act as m-CNTs within circuits. While CNFETs in circuits have a range of V_{DS} applied across them at any given time, the negative impact of m-CNTs appear primarily at high V_{DS}, and thus we pessimistically characterize our s-CNT purity similarly with a high V_{DS}, essentially binning small bandgap CNTs as m-CNTs (as this realistically is how they negatively impact a circuit). Figure 2.4a-h shows typical I_D-V_{GS} characteristics of 500 p-channel CNFETs with channel length (L_{CH}) of 1 μm for a drain bias, V_{DS} = -1.8V (measurements at ~23 °C) measured from CNFETs fabricated using different CNT solutions (Table 2.2). Additionally, figure 2.5f shows the cumulative distribution function (cdf) of the I_{ON}/I_{OFF} ratio as obtained from characterizing 10,000 CNFETs measured at a V_{DS} of -1.8 V. We use the cdf of I_{ON}/I_{OFF} ratios to analyze the efficacy of the solution sorting process, as solutions with higher s-CNT content would result in more transistors with higher I_{ON}/I_{OFF} ratios leading to the cdf plots shifting to the right (Figure 2.6b-d). Mean I_{ON} and I_{OFF} measured at a V_{DS} of -1.8 V extracted from I_D-V_{GS} characteristics of 10,000 CNFETs for each CNT solution is plotted as I_{ON}-I_{OFF} scatter plots (Figure 2.6a) with a preferred solution having a higher I_{ON} at a lower I_{OFF}.

From Figure 2.6a, we observe s-CNT solutions prepared from laser ablation CNTs outperform s-CNT solutions prepared from other CNT sources based on relative mean I_{ON} and I_{OFF}. This point is further clarified in Figure 5d which shows that CNFETs fabricated with laser ablation CNTs have an improved cumulative distribution of I_{ON}/I_{OFF} ratios (as measured from I_D-V_{GS} characteristics of ~10,000 CNFETs at V_{DS} = -1.8 V) compared to arc discharge and plasma CNTs.

[b] Bandgap of a CNT is determined by its diameter and chirality [Dresslhaus 1995]

Additionally, from Figure 2.6c, we see that PFDD wrapped laser ablation CNTs have an improved I_{ON}/I_{OFF} ratio distribution compared to laser ablation CNTs wrapped with other polymers such as PFPy, PFBPy and PCz (s-CNT purity estimate for each solution is shown in appendix, Figure A7.1, Table A7.1). Figure 2.6b demonstrates a similar trend for arc discharge CNTs where PFDD wrapped CNTs outperform PFPy or PCz wrapped CNTs.

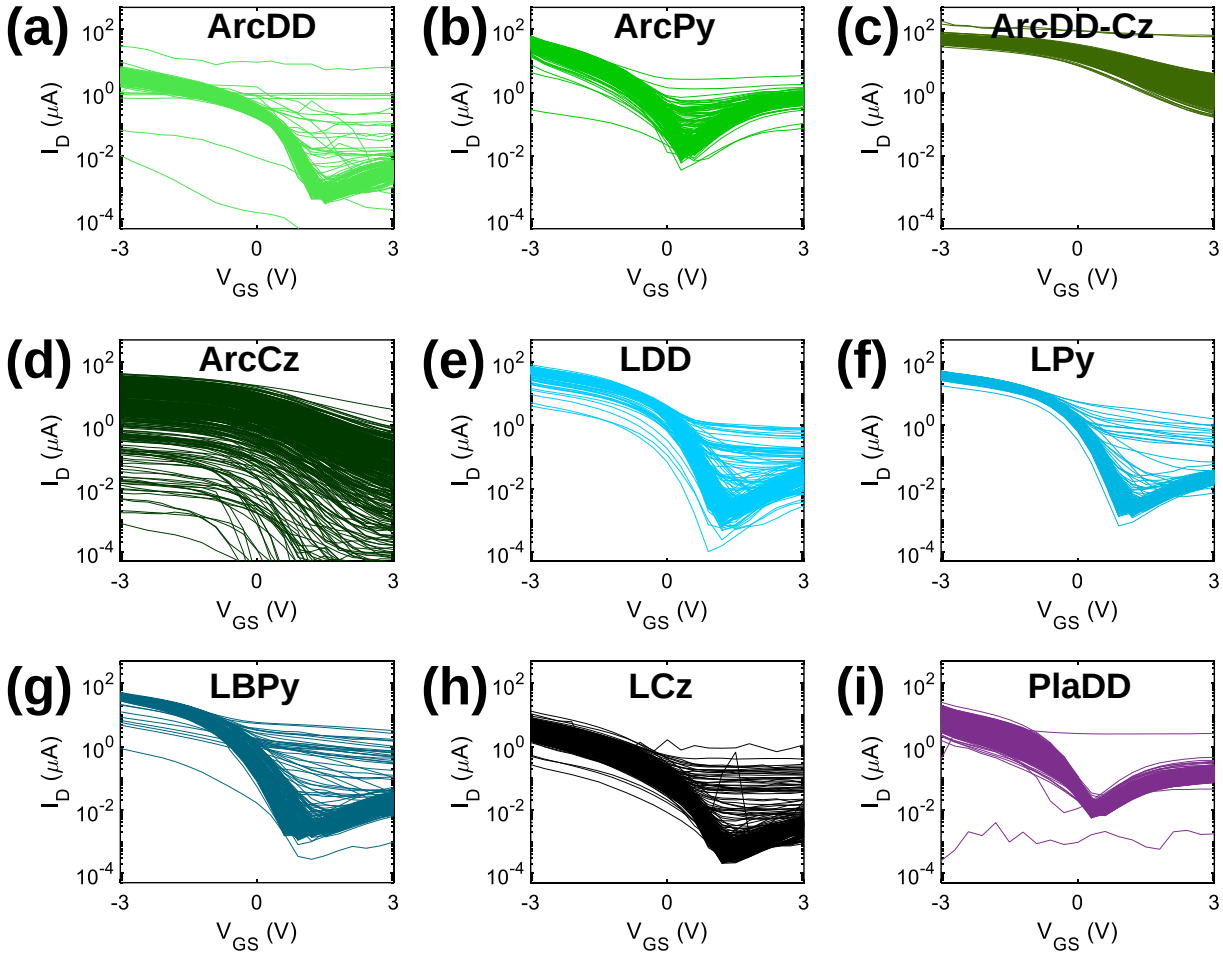


Fig. 2.4. Typical I_D-V_{GS} characteristics of 500 CNFETs fabricated using semiconducting CNT (sCNT) solutions extracted from different CNT sources and polymers - (a-d) arc discharge CNTs (e-h) laser ablation CNTs (i) plasma CNTs. Table 2.2 lists all the different CNT sources and polymer types. Transfer characteristics are color coded to match Figure 2.2,2.5 and 2.6.

It is critical to note that Figure 2.6a-d shows how the CNT precursor and the wrapping polymer can be optimized separately for maximizing s-CNT purity. For instance, Figure 2.6a and 2.6d

illustrates for any particular polymer, the trend in ideal CNT source selection is always laser ablation, then arc discharge, then plasma. Similarly, Figure 2.6b and 2.6c shows for a particular CNT source (e.g. laser ablation or arc discharge), the trend in ideal polymer selection is always PFDD, then PFPy, then PCz. These observations illustrate experimentally that the ideal CNT synthesis source and ideal polymer used for the sorting process are independent from one-another, and thus can be optimized separately.

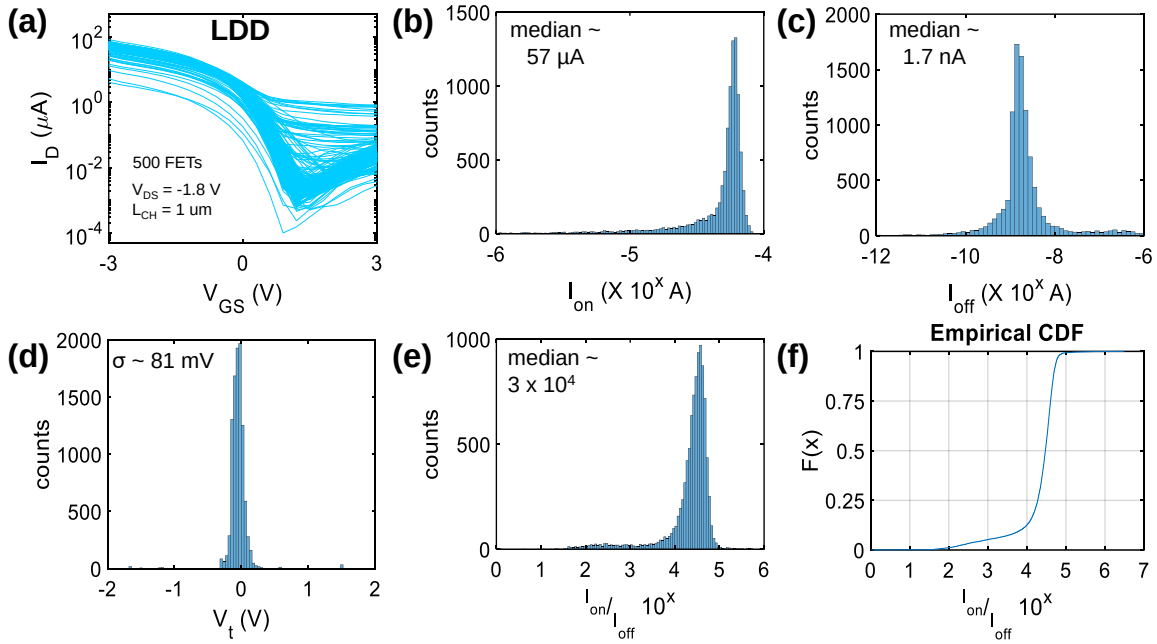


Fig. 2.5. (a) Experimental I_D-V_{GS} characteristics of 500 CNFETs measured at room temperature at V_{DS} = -1.8 V for laser ablation CNTs wrapped with PFDD. Histograms of key device metrics obtained from 10,000 CNFETs measured at V_{DS} = -1.8 V - (b) I_{ON} (c) I_{OFF} (d) V_T and (e) I_{ON}/I_{OFF} ratio. (f) cumulative distribution function of I_{ON}/I_{OFF} ratio.

Finally, we demonstrate how the best combination – laser ablated CNTs wrapped with PFDD achieves a s-CNT purity of 99.9953%, (an estimate of s-CNT purity is computed for each solution in appendix, Figure A7.1, Table A7.1), above the 99.99% threshold (as required by *DREAM* design methodology) also achieving a median on-current of ~57 μAs per FET (L_{CH} = 1 μm) and a mean I_{ON}/I_{OFF} ratio of 3×10^4 at a V_{DS} of -1.8 V. Importantly, the synthesis process for laser ablated

CNTs is slower than other techniques (e.g. arc discharge, plasma etc). Thus, future work should focus on scaling up the manufacturing process for PFDD sorted laser ablated CNTs for realizing energy efficient CNFET based digital VLSI systems.

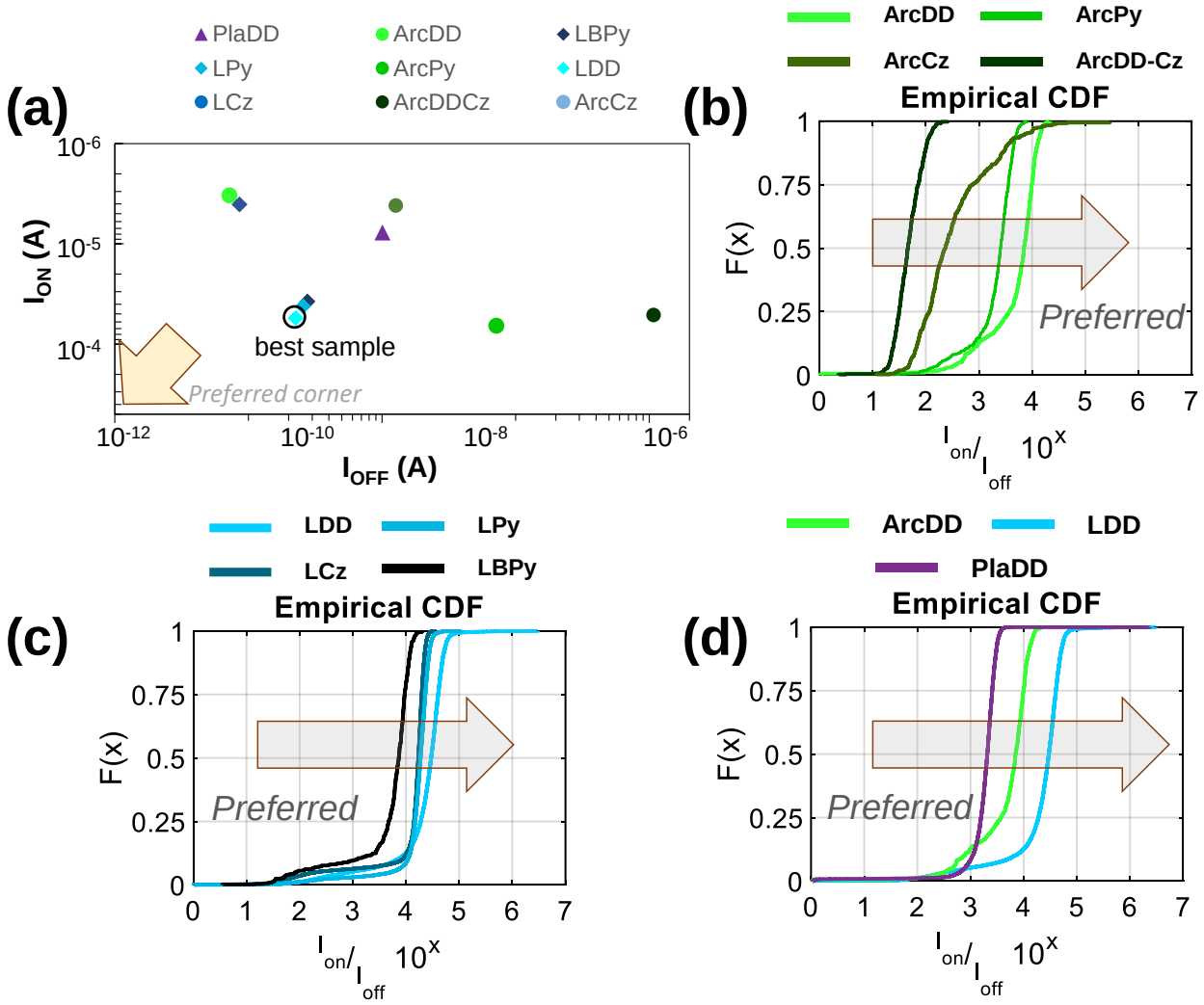


Fig. 2.6. (a) Mean I_{ON}-I_{OFF} scatter plot for each solution as listed in Table 2.2, extracted from I_D-V_{GS} characteristics of 10,000 CNFETs for each solution (totaling 10 million CNTs per solution) measured at a V_{DS} of -1.8 V. All solutions are color coded to match Figure 2.2, 2.4 and 2.5. Comparison of I_{ON}/I_{OFF} ratios for different s-CNT solutions by characterizing the cumulative distribution function of I_{ON}/I_{OFF} ratio (10,000 CNFETs per solution) for (c) arc discharge CNTs wrapped with different polymers (c) laser ablation CNTs wrapped with different polymers and (d) PFDD wrapped laser ablation CNTs, arc discharge CNTs and plasma CNTs. Details of polymers and CNT sources listed in Table 2.2.

2.5 Summary

In this work, we experimentally investigate the impact of CNT sources and polymers chosen as initial precursors for the solution based conjugate polymer extraction of semiconducting CNTs on the electrical performance CNFETs by performing extensive electrical characterization of 10,000 CNFETs for each solution. Additionally, we show that for such solution sorted s-CNTs, impact of the polymer choice on the electrical performance of CNFETs remains same irrespective of the source of the CNTs. Finally, we demonstrate a combination of CNT and polymer - laser ablation CNTs wrapped with PFDD polymer – that can achieve the >99.99% s-CNT purity required to realize arbitrary digital VLSI systems. Thus, this work addresses a key challenge facing CNFET-based electronics, and demonstrates a promising path towards extraction of ultra-high purity carbon nanotubes for energy efficient digital VLSI systems.

Table 2.1: Transistor Parameters

L_{CH} (μm)	1
L_G (μm)	3
L_C (μm)	3
H_G (nm)	20
H_C (nm)	45
T_{OX} (nm)	30
Width (μm)	20

Table 2.2: Solution Properties

Sample	CNT source	Polymer	Solution Φ[c] (from UV-Vis-NIR data)
LDD	Laser Ablation	PFDD	0.418
LPy	Laser Ablation	PFPy	0.389
LCz	Laser Ablation	PCz	0.403
LBPy	Laser Ablation	PFBPy	0.401
ArcDD	Arc Discharge	PFDD	0.406
ArcPy	Arc Discharge	PFPy	0.396
ArcDDCz	Arc Discharge	PFDD and PCz	0.425
ArcCz	Arc Discharge	PFDD	0.452
PlaDD	Plasma	PFDD	0.405

1. PFDD: poly(9 9-di-n-dodecylfluorene-2 7-diyl)
2. PFPy: poly[(9,9-di-n-dodecylfluorenyl-2,7-diyl)-alt-(2,6-pyridine)].
3. PFBPy: poly[(9,9-di-n-dodecylfluorenyl-2,7-diyl)-alt-(5,5'-(2,2' bipyridine)].
4. PCz: poly[9-(1-octylnonyl)-9H-carbazole-2,7-diyl]

[c] Solution Φ refers to the absorption peak ratios calculated from UV-Vis-NIR data. Higher Φ may qualitatively indicate higher s-CNT purity optically, however it cannot conclusively differentiate between lower band-gap CNTs and pure metallic CNTs. Hence, extensive electrical characterization of a statistically-significant sample size of transistors is necessary for measuring s-CNT purity of a solution accurately.

Chapter 3: Engineering Device Geometries for Scaling and Increased Energy Efficiency

3.1 Background

As scaling FET contacted gate pitch (CGP) becomes increasingly challenging, paths for continued scaling to 3 nm technology nodes and beyond remain unclear [Liebmann 2016, ITRS]. Additionally, larger parasitic capacitances due to thinning spacers between the gate and source/drain degrade energy efficiency [Kuhn 2012], further limiting CGP scaling [Bardon 2016]. This has motivated a search for emerging nanotechnologies to supplement or replace silicon FETs. For instance, carbon nanotubes (CNTs) can be used to form CNT FETs (CNFETs), which promise an order of magnitude EDP benefit for digital VLSI systems compared to silicon CMOS [Wei 2009, Tulevski 2014].

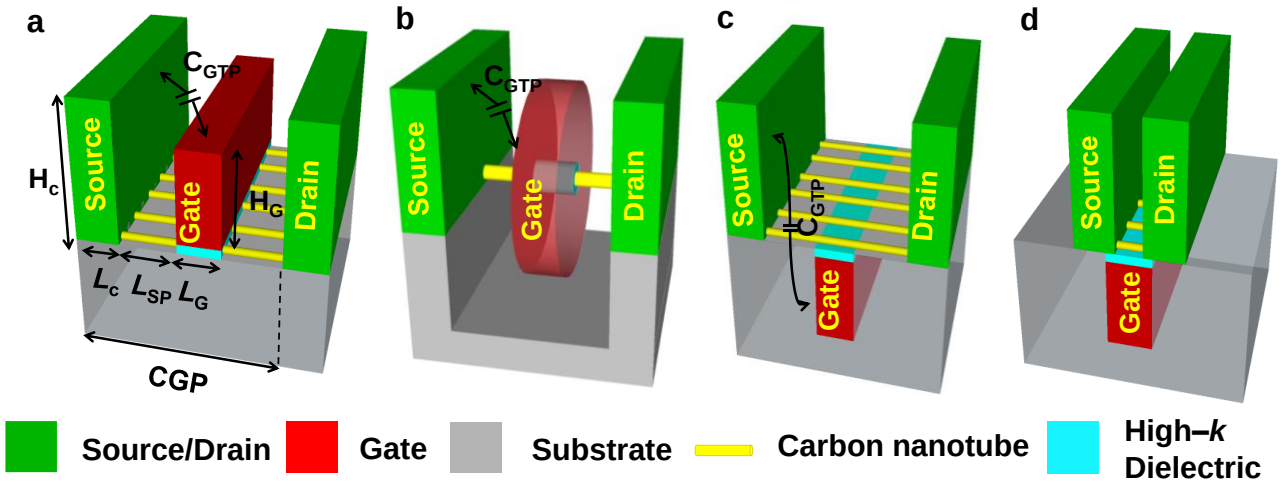


Fig. 3.1: Different FET geometries (illustrated with CNTs as the FET channel). (a) Conventional top-gate FET geometry. (b) Gate-all-around FET geometry. (c) Back-gate FET geometry. (d) Back-gate FET with negative L_{SP}

Figure 3.1 shows schematics of three different CNFET geometries: top-gate, gate-all-around (GAA) and back-gate FETs. Despite significant efforts to realize increasingly sophisticated FET

geometries (such as gate-all-around (GAA) [Franklin 2012, Chen 2008, Franklin 2013]), here we show that back-gate FET geometries provide major advantages that have not been exploited for highly scaled technologies: (1) back-gate FETs enable physical scaling beyond the limits of both top-gate and gate-all-around FET geometries, and (2) back-gate FETs provide significant additional EDP benefits owing to reduction in parasitic capacitances compared to top-gate and GAA FETs.

3.2 Back-Gate FET Geometry Benefits

First, back-gate FETs enable physical scaling beyond both top-gate and GAA FETs for further reduced CGP, enabling more highly-scaled technology nodes. CGP corresponds to the gate pitch between two or more FETs connected in series with a shared source/drain contact; it is equal to the sum of the source/drain contact length (L_C), the physical gate length (L_G), and the two spacer regions ($2L_{SP}$) that separate the gate from the source/drain (Eq. 1).

Eq. 1: $$CGP = L_C + L_G + 2L_{SP}$$

For back-gate FETs, the spacer regions are not necessary to avoid unintended electrical contact between the gate and the source/drain (i.e., electrical shorts), since the back-gate is on a physically separate plane beneath the source/drain [Tulipe 2008, Doris 2015]. Therefore, there can be intentional overlap between the gate and the source and drain (which mathematically corresponds to $L_{SP} < 0$ in Eq. 1, shown in Figure 3.1d). Thus, CGP can be reduced by decreasing L_{SP} (e.g., below zero) – even without improving fabrication techniques for scaling L_C and L_G.

3.3 Experimental Demonstration: 30 nm CGP CNFETs & Digital Logic

As an experimental demonstration, we fabricate back-gate CNFETs and digital logic from FETs that fit within a record-scaled CGP = 30 nm (Figure 3.2). We use CNFETs because (1) the CNTs

can be deposited over the pre-fabricated gate stack at room temperature (e.g., through solution-based processing [Cao 2013], in contrast to silicon channels which can require temperatures >1000 °C) [Vinet 2011, Sabry 2015], and (2) CNFETs are a leading and rapidly maturing contender for energy-efficient computing as high-performance devices and complete digital systems have been experimentally demonstrated [Wei 2009, Tulevski 2014, Sabry 2015, Shulaker 2017].

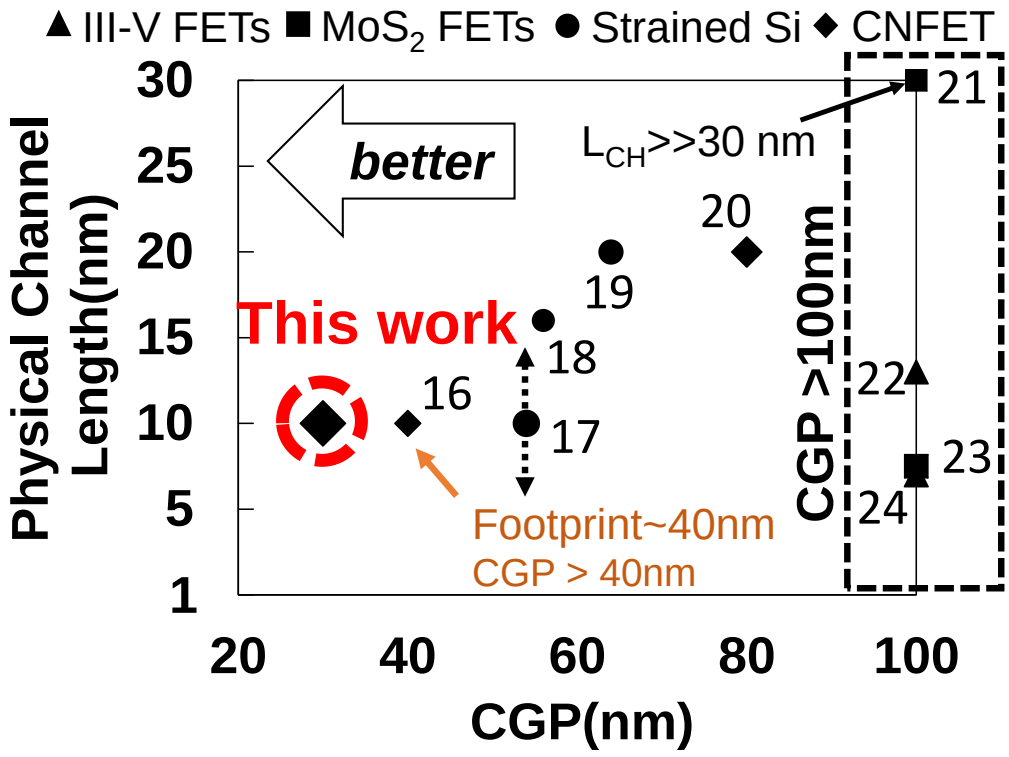


Fig. 3.2: Benchmarking current work with respect to contacted gate pitch across best reported scaled technologies in literature, references [16]-[24] are [Cao 2017, Mistry 2017, Narasimha 2017, Seo 2014, Qiu 2017, Desai 2016, Hahn 2017, Nourbakhsh 2016, Zhao 2017] respectively. [16] reports footprint, [17] doesn't report L_G or L_{eff}, [18] reports L_{eff}, [19] reports the gate length, [20-24] CGP data extracted from SEMs reported in respective papers.

The fabrication flow for a back-gate CNFET is shown in Figure 3.3. To achieve a CGP of 30 nm, the CNFETs are patterned with L_C = 20nm, L_G=18nm, and L_{SP}=-4nm (i.e., 4 nm intentional overlap of the back-gate with the source and the drain), with a physical channel length (L_{CH}=CGP-L_C) of

10 nm. Scanning electron microscopy (SEM) and transmission electron microscopy (TEM) images of the fabricated devices are shown in Figure 3.4. Importantly, this CGP scaling is achieved without additional scaling of L_G and L_C. This highlights how this approach can decouple the conflicting constraints on L_C and L_G (longer Lc and L_G can result in improved contact resistance and electrostatic control) from the constraints imposed by needing to aggressively scale CGP (ideally scaling both L_C and L_G). Figure 3.5 shows electrical characterization of typical CNFETs and the measured voltage transfer curve from a CNFET inverter fabricated from 30 nm CGP CNFETs, illustrating functional operation. This digital logic comprises of FETs with the most-scaled CGP ever realized to date (Figure 3.2).

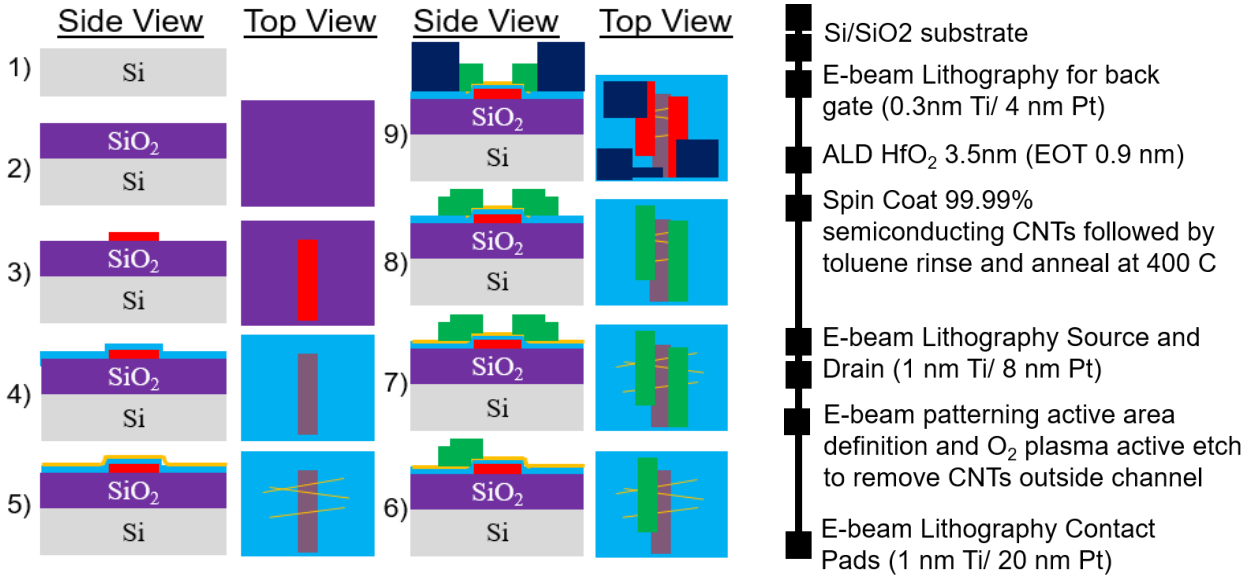


Fig. 3.3: Process flow of back-gate CNFETs. While back-gates are not embedded within the substrate, a conventional damascene process can be used to achieve the reduced parasitics for back-gate FET geometries. E-beam photoresist thickness (< 40nm) limits the metal thickness in our experimental demonstration to <10 nm.

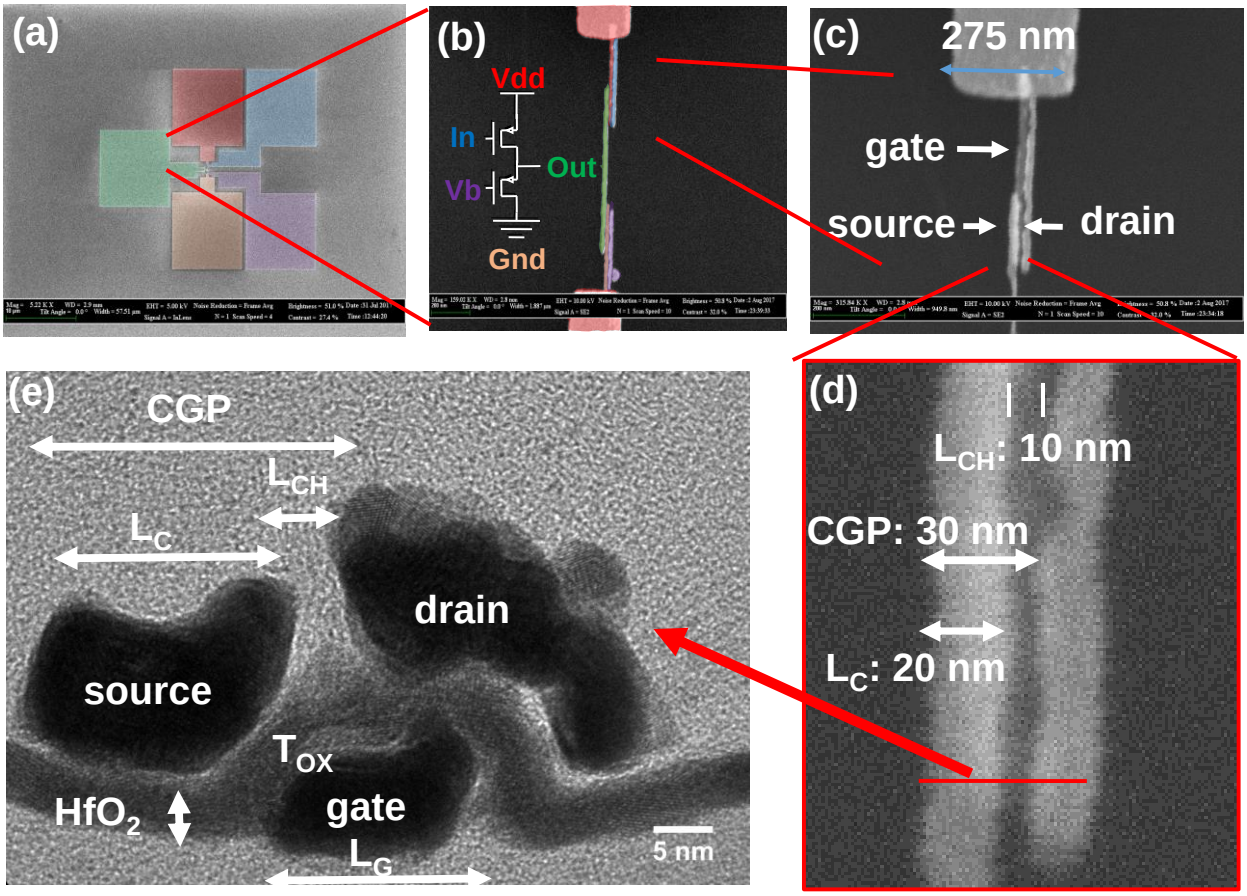


Fig. 3.4. Fabricated back-gate CNFETs with 30 nm CGP. (a-d) Top view scanning electron microscopy (SEM) images of typical 30 nm CGP back-gate CNFETs and CNFET digital logic (inverter). (a) Probe pad layout for the CNFET inverter (false colored). (b) Magnified view of a typical CNFET inverter, false colored to match the inverter schematic in (b), and the pads in (a). the image in (b) shows an inverter before the pads shown in (a) are deposited, since the pads cover some of these features. (c) Magnified view of a typical back-gate CNFET comprising a CNFET inverter (shown in (b)). (d) Magnified view of the CNFET channel region. L_C is 20 nm and L_{CH} is 10 nm, resulting in a 30 nm CGP. The L_G is 18 nm, and overlaps both with the source (left contact) and drain (right contact) by ~4 nm. (e) Cross-section transmission electron microscopy (TEM) image of a back-gate CNFET with nominal 30 nm CGP.

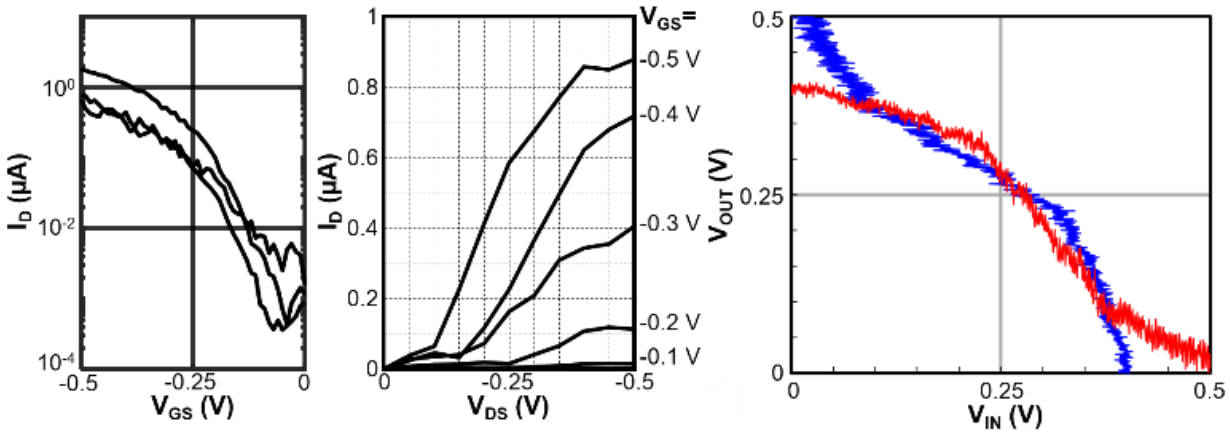


Fig. 3.5: (left) I_D-V_{GS} characteristics of multiple 30 nm CGP CNFETs, achieving subthreshold-swings (SS) of ~125 mV/dec (at V_{DS}=-0.5V). (middle) I_D-V_{DS} characteristic of sample 30 nm CGP CNFET. (right) Voltage transfer curve of a 30 nm CGP CNFET inverter, implemented using depletion load PMOS logic with V_{OH} = 0.4V V_{OL}= 0.05V respectively.

Importantly, the benefits of back-gate CNFETs extend beyond enabling continued scaling. Back-gate FET geometries simultaneously reduce parasitic capacitances (e.g., gate –to source/drain capacitance), resulting in additional EDP benefits for digital VLSI circuits. The reduced parasitic capacitances are due to decreased electrical coupling of the gate beneath the source/drain. As shown in Figure 3.6, the parasitic capacitances for back-gate FETs is further reduced as CGP continues to scale (for the parameters in Table 3.1), resulting in major EDP benefits for digital VLSI circuits. To quantify these EDP benefits, we analyze physical designs of VLSI digital circuits from the processor core of OpenSPARC T2 [OpenSparc] and a 32-bit commercial processor core (Figure 3.7). These processor cores incorporate many effects present in realistic VLSI circuits that do not appear in small circuit benchmarks *e.g.*, physical placement and routing congestion, wire parasitics, and buffer insertion to meeting circuit-level timing constraints [Hills 2015]. Due to reduced parasitic capacitances, back-gate CNFETs offer an average of 1.6× EDP benefit vs. top-

gate CNFETs and 2.2× vs. GAA CNFETs. Importantly, these benefits are *in addition* to the substantial EDP benefits that top-gate CNFETs offer vs. Si FETs [Wei 2009, Tulevski 2014].

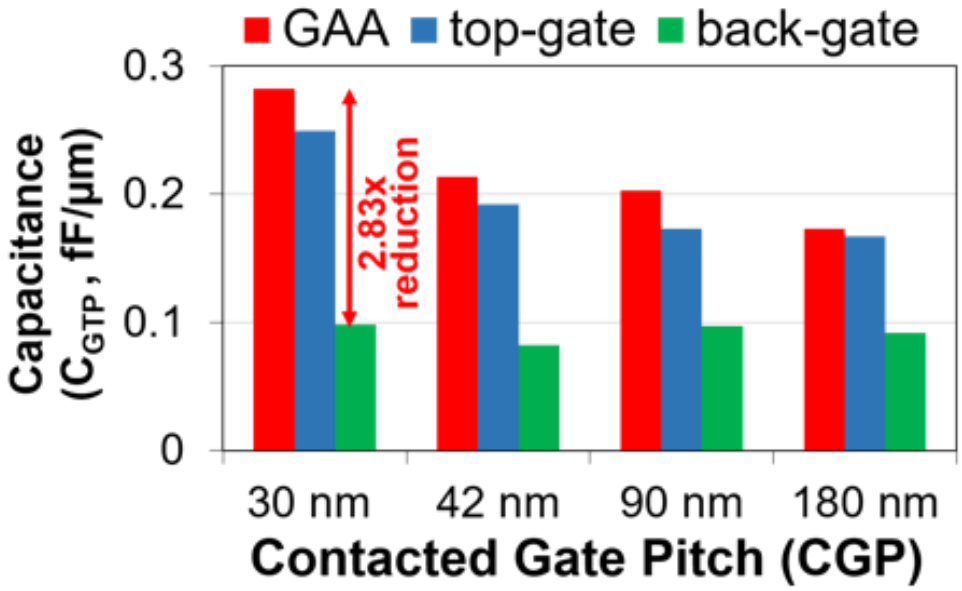


Table 3.1

CGP (nm)	30	42	90	180
L_G (nm)	9	9	24	45
L_{SP} (nm)	6	12	20	45
L_C (nm)	9	9	26	45
H_G (nm)	20	30	40	90
H_C (nm)	40	60	80	180
T_{OX} (nm)	2	2	3	4
K_{SPACER}	5.5	5.5	5.5	5.5
K_{OX}	10.3	10.3	10.3	10.3

Fig. 3.6: (top) Parasitic capacitances (gate-to-plug capacitance, C_{GTP} (Fig. 2.1) for back-gate vs. top-gate and GAA FET. Back-gate FETs reduces parasitics by >2.5× vs. top-gate and by >2.8× vs. GAA for a 30 nm CGP (suitable for a sub-3 nm node). Benefits of parasitic reduction increases as CGP scales. Intrinsic

parasitics are determined using TCAD Sentaurus (Synopsys) and verified using COMSOL Multiphysics (COMSOL, Inc.) (with a discrepancy of <0.3% across all simulations). (bottom) Table 3.1: Device parameters used for analysis. CGP values of 30 nm, 42 nm, 90 nm, and 180 nm correspond to 3 nm, 7 nm, 22 nm, and 45 nm technology nodes, respectively [ITRS, Mistry 2017].

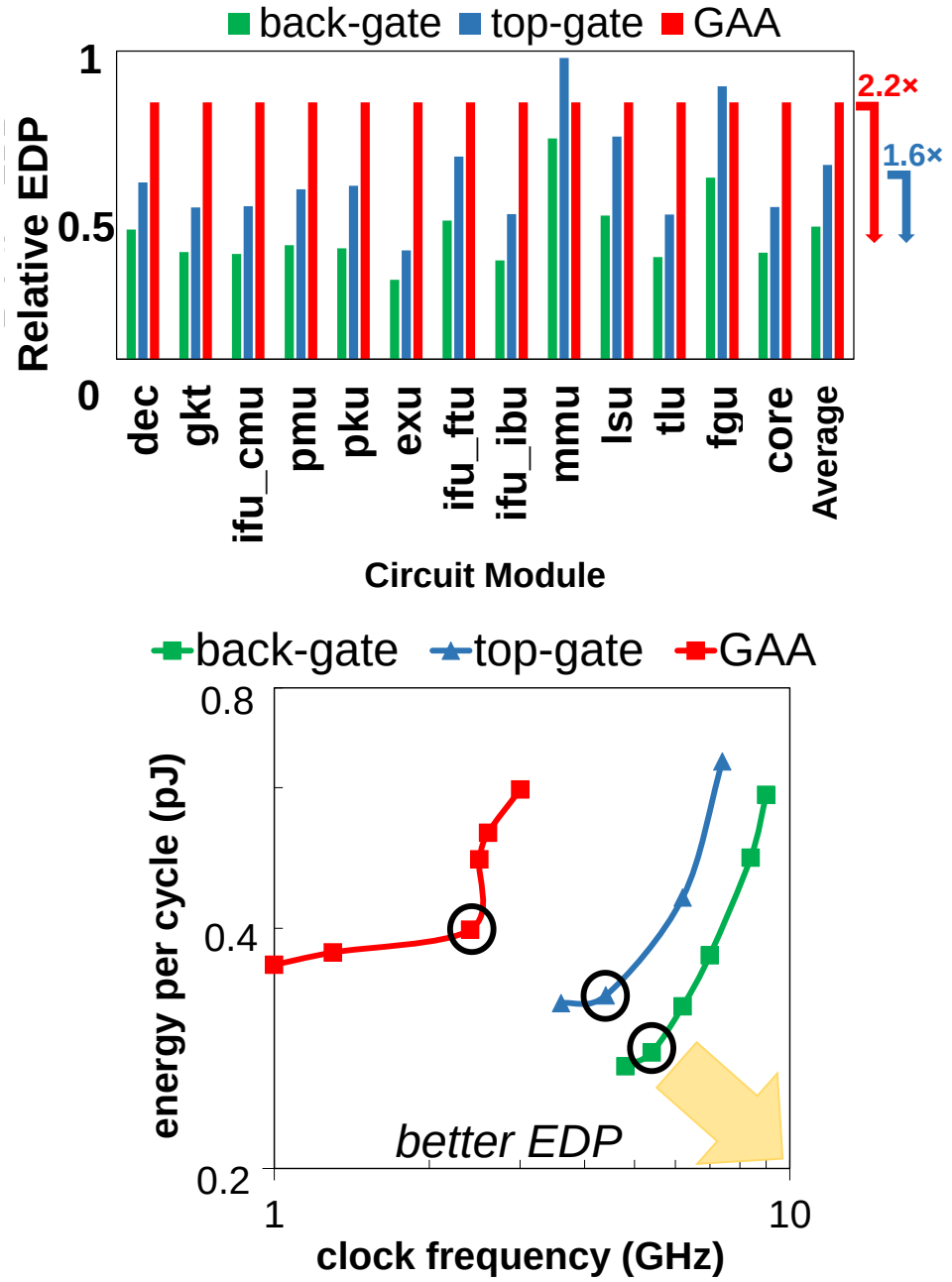


Fig. 3.7: (top) Optimized EDP (normalized with respect to the optimized EDP for the GAA CNFET for each module) across modules from the OpenSparc T2 core and a 32-bit commercial processor core. Average EDP benefit of back-gate vs. GAA is 2.18×, and 1.6× vs. top-gate. (bottom) Total energy vs. frequency of

the 32-bit commercial processor core, showing the pareto-optimal EDP trade-off curves for back-gate, top-gate, and GAA CNFETs. Left figure is extracted from these EDP trade-off curves. All simulations are done with respect to a 30nm CGP device with parameters listed in Table 3.1, Figure 3.6. Importantly, EDP benefits are maintained even with low-k spacers (e.g., with a k=4.4 spacer [Yakimets 2017], EDP benefits decrease by <10% (dec module of OpenSparcT2). Moreover, for many existing standard cell libraries, the same physical layouts can be used for FETs with back-gate geometries without any adjustments to the locations of FETs or to the metal routing within standard library cells (specifically for standard cell layouts in which vias to contact FET gates are located outside of the active region of the FETs).

3.4 Additional Considerations

The EDP benefits resulting from reduced parasitics (above) outweigh potential gains stemming from improved electrostatic control for GAA geometries (*e.g.*, the subthreshold-swing (SS) for the back-gate CNFET can degrade from ~60 mV/decade to ~100 mV/decade, while still maintaining EDP benefits compared to GAA CNFETs with nearly ideal SS approaching 60 mV/decade as demonstrated in Figure 3.8)

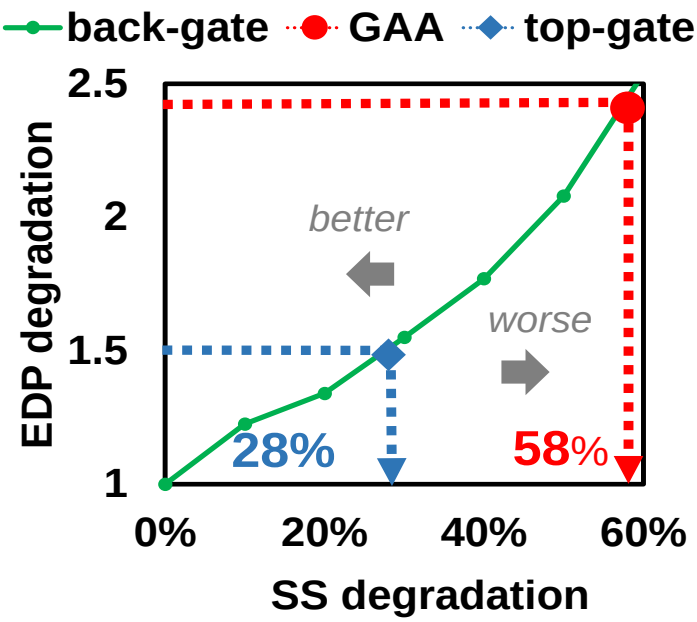


Fig. 3.8: EDP benefits resulting from reduced parasitics outweigh potential gains stemming from improved electrostatic control for GAA geometries. Subthreshold swing (SS) can degrade by > 58% (resulting in SS

= 100mV/dec), while still maintaining the EDP benefits compared to GAA CNFETs with assumed ideal SS approaching 60 mV/dec. Importantly, experimental demonstrations of CNFETs with L_{CH} = 9nm have leveraged back-gate geometries and reported a SS better than 100 mV/dec (94 mV/dec), highlighting feasibility of this approach [Franklin 2012a].

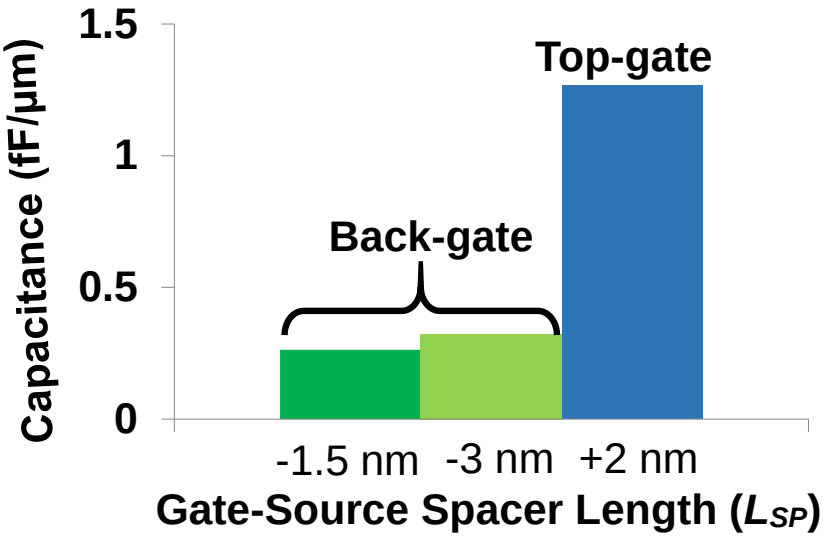


Table 3.2

CGP (nm)	15	15	15
L_G (nm)	9	9	5
L_{SP} (nm)	-1.5	-3	+2
L_C (nm)	9	9	6
H_G (nm)	15	15	15
H_C (nm)	30	30	30
T_{OX} (nm)	2	2	2
K_{SPACER}	5.5	5.5	5.5
K_{OX}	10.3	10.3	10.3

Fig. 3.9: Paths for realizing 15 nm CGP. Extraction of parasitic capacitance (C_{GTP}) for the top-gate FET, as well as back-gate FETs assuming a 3 nm overlap between the gate and source/ drain and 1.5 nm overlap between the source/ drain. Even with overlap, back-gates will yield >3× reduced parasitic capacitances at scaled nodes. Table 3.2 shows device parameters used for Figure 3.9.

In addition to showing scalability to a 30 nm CGP, this approach allows scaling to sub-20 nm CGP, using technology parameters that have already been achieved experimentally (Figure 3.9). For instance, a 9 nm L_G [Franklin 2012a], a 9 nm L_C [Cao 2015], and an overlap of the gate and the source and drain ($-L_{SP}$) of 3 nm would result in a CGP of 15 nm. Importantly, even when assuming an overlap of the gate with the source and drain (the key to achieving a scaled CGP) for back-gate FETs, the parasitics can still be less compared to a conventional top-gate FET at the same CGP (Figure 3.9). The overlap of 3 nm is chosen because (1) it enables 15 nm CGP given experimentally realized dimensions for L_C and L_G and (2) it exceeds the projected lithographic overlap accuracy [ITRS], ensuring that some section of the gate will be under the entire channel to maintain electrostatic control. For such aggressively scaled sub-20 nm CGPs, EDP benefits degrade compared to 30 nm CGP, though still maintain EDP benefits compared to 30 nm CGP top-gate CNFETs (Figure 3.10).

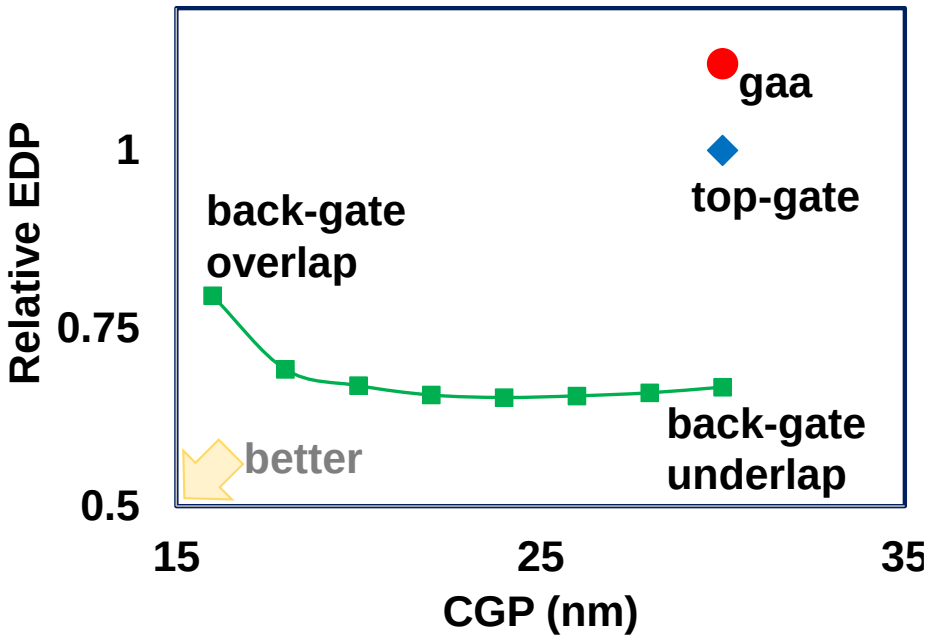


Fig. 3.10: Comparison of relative EDP of a fan-out 4 (FO-4) inverter (normalized to EDP of CGP 30nm top-gate CNFET) vs CGP of back-gate CNFETs (all devices have contact length of 9nm and gate length of 9nm, L_{SP} is varied to reduce CGP).

3.5 Summary

We experimentally demonstrate record-scaled 30 nm CGP FETs and digital logic, leveraging back-gate CNFETs. We rigorously quantify the benefits of back-gate CNFETs by analyzing physical designs of digital VLSI circuits, showing that this approach provides additional EDP benefits vs. top-gate and GAA CNFETs due to reduced parasitic capacitances. Furthermore, this approach is applicable to a wide range of FETs using emerging channel materials (such as 1D and 2D nanomaterials) provided that: 1) they can be fabricated at low temperatures (*e.g.*, <400 °C, including channel deposition and subsequent FET processing), and 2) the channel is nanometer-thin for ideal electrostatic control using the back-gate. Thus, we demonstrate significant benefits of back-gate FETs, illustrating that they should be seriously considered for future highly-scaled and energy-efficient digital electronics.

Chapter 4: Gate geometry engineering for improved CNFETs

4.1 Background

While physical and equivalent transistor scaling has been a major driving force for improved energy efficiency, continued scaling is becoming increasingly challenging and no longer yields the same historical energy efficiency benefits [Kuhn 2012, Bardon 2016]. This has promoted the search for emerging nanotechnologies as potential supplements to silicon, such as one-dimensional and two-dimensional materials. For instance, one-dimensional carbon nanotubes (CNTs) are cylindrical nanostructures comprised of a single atomic layer of carbon atoms and have exceptional electrical, physical and thermal properties [Riichiro 1998, Wei 2009, Chang 2012, Franklin 2012b, Chen 2008, Baughman 2002]. A CNT field-effect transistor (CNFET) is formed by using multiple parallel semiconducting CNTs as the channel of the transistor with traditional lithographically defined source, drain and gate [Javey 2003, Shulaker 2013, Shulaker 2017]. Owing to the simultaneously ideal electrostatic control (owing to their ultra-thin body, set by the ~ 1 nm diameter of a CNT) and superior carrier transport, digital VLSI systems fabricated with CNFETs are projected to achieve an order of magnitude improvement in energy-delay product (EDP, a metric of energy efficiency) compared to silicon CMOS [Wei 2009, Tulevski 2014].

Figure 4.1a shows the schematics and measured electrical transfer characteristics (I_D-V_{GS}) of a typical back-gate CNFET. All CNFETs in this work are fabricated as back-gate CNFETs, using >99.9% pure semiconducting CNTs [Nanointegris]). CNTs dispersed in solution are deposited at room temperature over a pre-fabricated high-k metal gate stack (defined by electron-beam lithography). Following deposition of the CNTs, source and drain contacts are aligned to the pre-fabricated gate stack and lithographically defined. CNTs outside of the channel region of the

CNFETs are removed by etching with oxygen plasma. A detailed process flow is shown in appendix, Fig. A1.1.

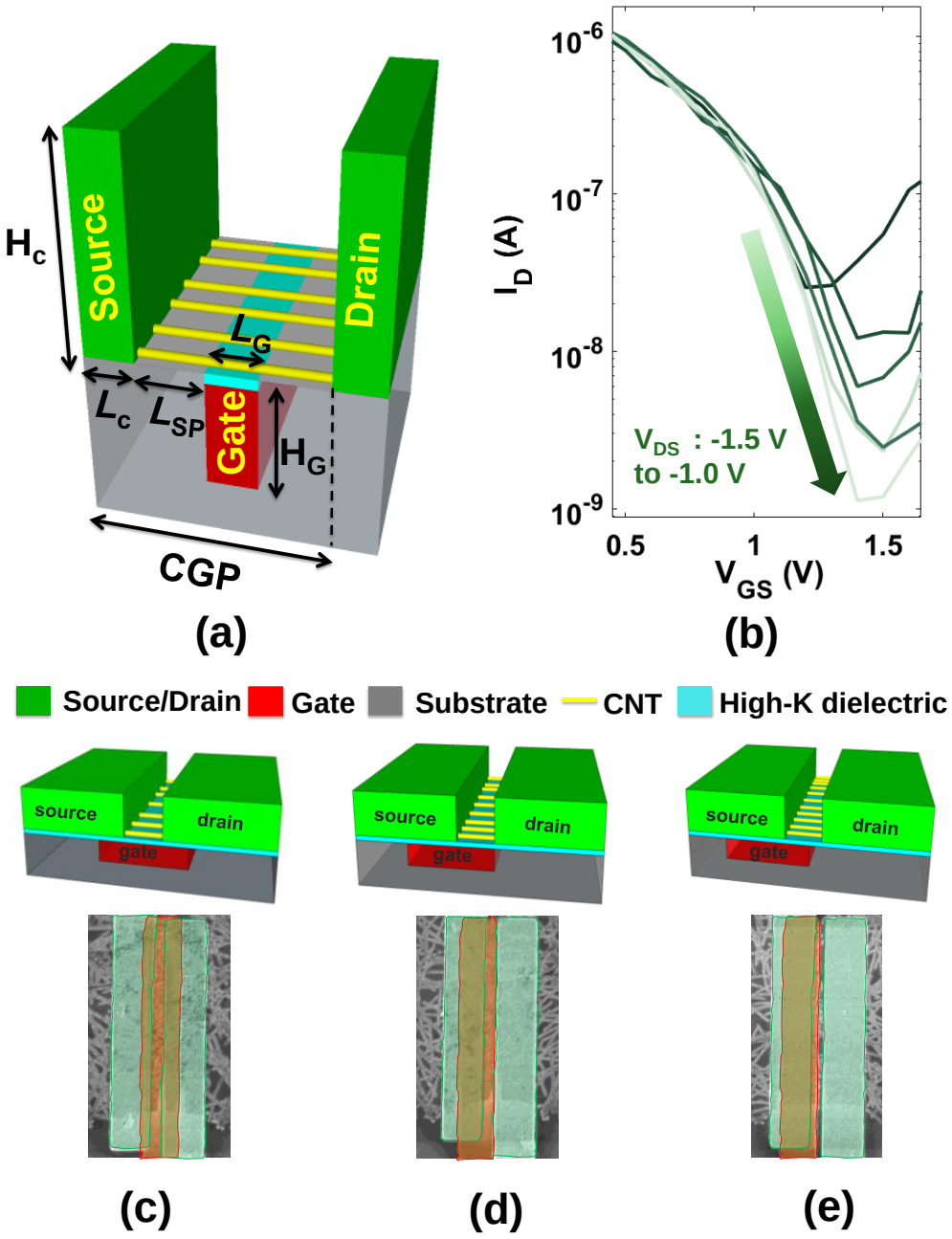


Fig. 4.1. (a) Schematic of back-gate CNFET. LCH is the physical channel length, Lsp is (use definition from text), etc.. (b) Experimentally measured I_D-V_{GS} characteristics for a transistor with L_{CH}=180nm (measured at room temperature). Device parameters listed in Table 4.1. (c-e). Schematics of symmetric vs asymmetric

CNFETs, together with matching scanning electron microscopy (SEM) images of fabricated CNFETs. (c) Symmetric back-gate CNFET with the gate overlapping the source and drain, (d) Asymmetric back-gate CNFET with the same gate length and contacted gate pitch (CGP) as (c), but with the gate laterally shifted to achieve zero overlap between the gate and drain, (e) Asymmetric back-gate CNFET with the same gate length and contacted gate pitch (CGP) as (c), but with the gate laterally shifted to achieve an intrinsic CNT region between the gate and drain.

4.2 Leakage Current in CNFETs

Although CNFETs are a rapidly maturing contender for energy efficient computing [Wei 2009, Shulaker 2017, Tulevski 2014, Chang 2012, Sabry 2015], measurements of experimental CNFETs often exhibit significant off-state leakage current. This leads to increased leakage power dissipation and potential incorrect logic functionality. To understand this off-stage leakage behavior, we characterize CNFETs across a range of different biasing conditions (gate potential, V_{GS}, and drain potential, V_{DS}) and physical geometries (channel lengths, L_{CH}). Figure 4.2a-e shows the I_D-V_{GS} characteristics of CNFETs with L_{CH} spanning 2 μm down to 180 nm. As is typical, all of the CNFETs demonstrate exponential rise in off-state leakage current with increasing V_{DS} [Brady 2016, Qiu 2017]. While this off-state leakage current is often attributed to short channel effects[d] (such as drain-induced barrier lowering, DIBL), short channel effects cannot be the predominant source of the increased off-state leakage current due to: (1) increasing off-state leakage current does not occur in tandem with degrading inverse subthreshold slope[e] ; in contrast, inverse subthreshold slope remains constant, and (2) increasing off-state leakage current with

[d] Short-channel effects such as drain-induced barrier lowering (DIBL), velocity saturation, hot carrier injection, etc., degrade electrical characteristics in MOSFETs and occur when the channel length is comparable to the depletion width of source and drain junctions. [Veeraraghavan 1989]

[e] Inverse sub-threshold slope is defined as the inverse of rate of change of I_D with V_{GS} in transfer characteristics.

increasing V_{DS} occurs independent of the CNFET channel length (and occurs even at large channel lengths of >1 µm).

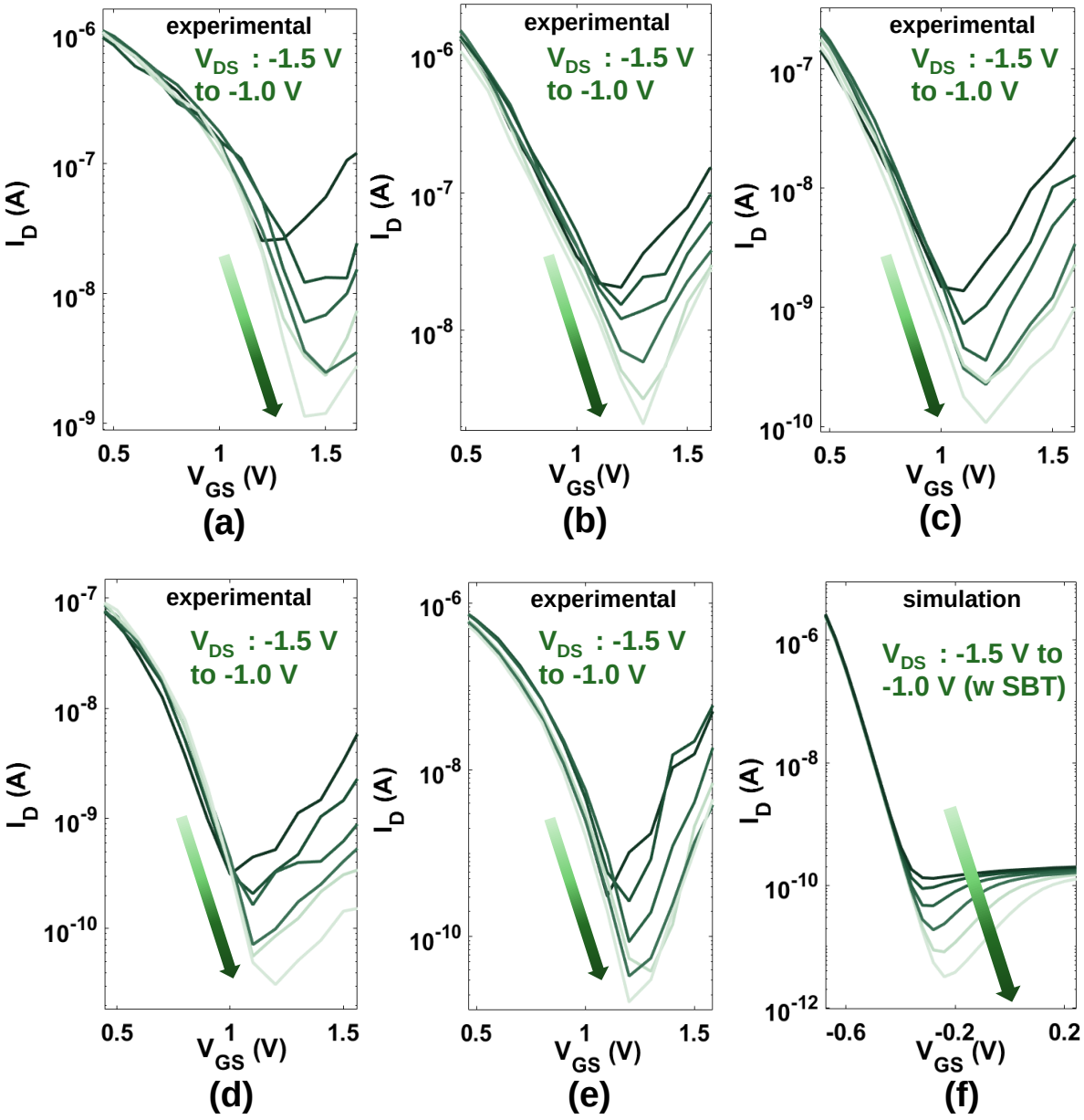


Fig. 4.2. (a-e) Experimental room temperature I_D-V_{GS} plots for CNFETs fabricated with a range of different channel lengths (L_{CH}). From (a) through (e), the channel lengths are: 180 nm, 500 nm, 1 µm, 1.5 µm, and 2 µm, respectively. The V_{DS} varies from -1.8 V to -0.1 V (dark green to light green curves), and Table 4.1 lists the device parameters. (f) Simulated I_D-V_{GS} of a CNFET with L_{CH} =180nm using TCAD Sentaurus. The simulated device structure has the same dimensions as the experimental device shown in Figure 4.2a with

L_{CH} = 180nm [experimental parameters listed in Table 4.1, device parameters used listed in Table 4.2]. The simulated CNFET exhibits the same trends in I_{OFF} as the measured CNFETs.

Rather, this increased off-state leakage current is indicative of Gate-Induced Drain Leakage (GIDL, Figure 4.3). GIDL occurs at large gate-to-drain bias, when there is sufficient energy-band bending near the drain of the channel that valence band electrons can tunnel into the conduction band (referred to as band-to-band tunneling, BTBT, illustrated in appendix A6). In schottky barrier FETs [Zhang 2002, Lin 2001, Tsui 2005, Husain 2009] (such as CNFETs where the conduction of the FET is determined by the height of the schottky barrier of the metal to the semiconducting channel), this GIDL behavior is caused by parasitic schottky barrier tunneling [Zhang 2002, Lin 2001, Tsui 2005, Husain 2009] near the drain end of the channel (appendix A6). Illustrated in Figure 4.3a, parasitic schottky barrier tunneling occurs when a large gate-to-drain bias reduces the schottky barrier tunneling width, resulting in exponentially increasing electron injection through the schottky barrier (even when the FET is biases in the off-state). These tunneling current resulting from GIDL result in the exponentially increasing off-state leakage current at large gate-to-drain biases.

While GIDL has been studied extensively in bulk semiconductors (such as silicon, silicon-germanium, and III-V compound semiconductors), this GIDL-induced leakage behavior exhibited by CNFETs has not been previously discussed or incorporated into device-level models [Lee 2015, Deng 2007, Wei 2009, Luo 2013]. To investigate the detailed physics responsible for this excess off-state leakage current, we develop a CNFET model in TCAD sentaurus [Sentaurus] which includes the effect of this GIDL-induced leakage behavior[f] (Supplemental Information). Figure

[f] Sentaurus device [Sentaurus] solves a system of coupled poisson, electron and hole continuity equations in presence of Hurkx tunneling model [Hurkx 1992], to estimate the parasitic schottky barrier tunneling near the drain end and model this GIDL like behavior (more discussion in supplementary information).

4.2f shows the I_D-V_{GS} characteristics of the back-gate CNFET device model from Sentaurus Device. Our simulations (Figure 4.2f) closely match experimental I_D-V_{GS} characteristics (Figure 4.2a), with exponential rises of I_{off} with increasing gate-to-drain baises. Thus, it indicates GIDL is responsible for this excess off-state leakage current.

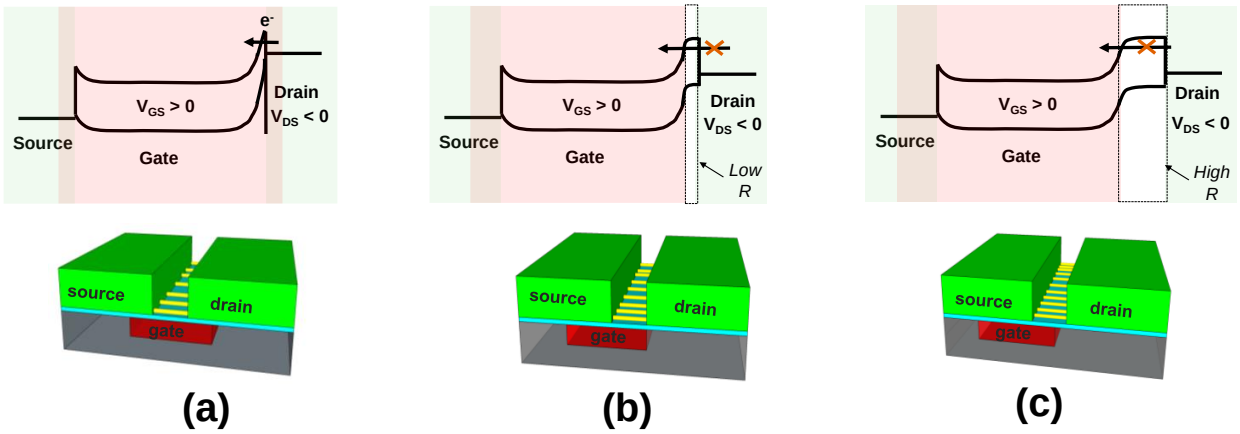


Fig. 4.3. (a-c) Energy band diagrams for a symmetric, asymmetric gate CNFET (with a thin intrinsic CNT region) and asymmetric gate CNFET (with a large intrinsic CNT region). The energy-band diagrams are shown for $V_{GS} > 0$ V and $V_{DS} < 0$ V to highlight the presence (or lack there-of) of GIDL (e.g., the difference in tunneling width through the schottky barrier and consequently lower I_{OFF} for the asymmetric CNFETs).

4.3 Asymmetric Back-Gate CNFETs

With understanding of the source of off-state CNFET leakage current, we next propose and experimentally demonstrate a path for overcoming it. Several approaches for overcoming GIDL have been pursued with current silicon and III-V based technologies, all with the aim of reducing the electric field near the drain. For instance, FETs with relaxed access regions (*i.e.*, extension regions) or, undoped spacer regions [Zhang 2002, Lin 2001, Lin 2013, Kerber 2013, Chen 1992, Yuan 2008, Lee 2013, Choi 2003] limit the electric field near the drain end of the channel (appendix A6), thereby suppressing this excess off-state leakage current. However, these techniques suffer from several drawbacks: they require complicated dopant profile engineering [Lin 2013, Kerber 2013, Chen 1992, Yuan 2008, Lee 2013, Choi 2003] accomplished through

interstitial doping [Beyer 1977], and increase the total device footprint area due to the additional spacer regions between the gate and the drain (defined by contacted gate pitch[g] (CGP) [Lin 2001, Lin 2013, Lee 2014]). Moreover, carbon nanotubes cannot be doped using interstitial doping [Appenzeller 2005] as it damages the pristine CNT lattice, making these previous techniques non-applicable to CNFETs.

Here we demonstrate that GIDL can be successfully overcome by engineering asymmetric gate geometries within CNFETs. The key advantages of this approach is that it does not require any complex dopant profiles nor does it impact the total device footprint area. Figures 4.1c-e illustrate a range of CNFETs with different gate geometries. Figure 4.3a shows a conventional CNFET with a *symmetric* gate geometry whereby the gate spans the entire CNT channel, overlapping equally with the source and drain electrodes [Shulaker 2013, Shulaker 2017]. It is this overlap in the gate and drain that results in large electric fields in the schottky barrier near the drain contact (Figure 4.3a), leading to excess off-state leakage current. In contrast, Figure 4.3b-c illustrate CNFETs with *asymmetric* gate geometries, whereby the gate is shifted away from the drain towards the source. With enough lateral shift, the gate eventually does not overlap at all with the drain, resulting in an intrinsic section of CNTs self-aligned to the drain contact. This section of intrinsic CNT prevents the high electric field near the drain even at large gate-to-drain biases, suppressing GIDL-induced leakage (Figure 4.3b-c). Importantly, this approach is accomplished without any additional processing steps as it is implemented entirely during the lithographic patterning of the gate and drain which occurs regardless.

[g] Contacted Gate Pitch or CGP is defined as the sum of the source/drain contact length (L_C), the physical gate length (L_G), and the two spacer regions ($2L_{SP}$) that separate the gate from the source/drain (Eq. 1, Figure 4.1).

Eq. 1: $$CGP = L_C + L_G + 2L_{SP}$$

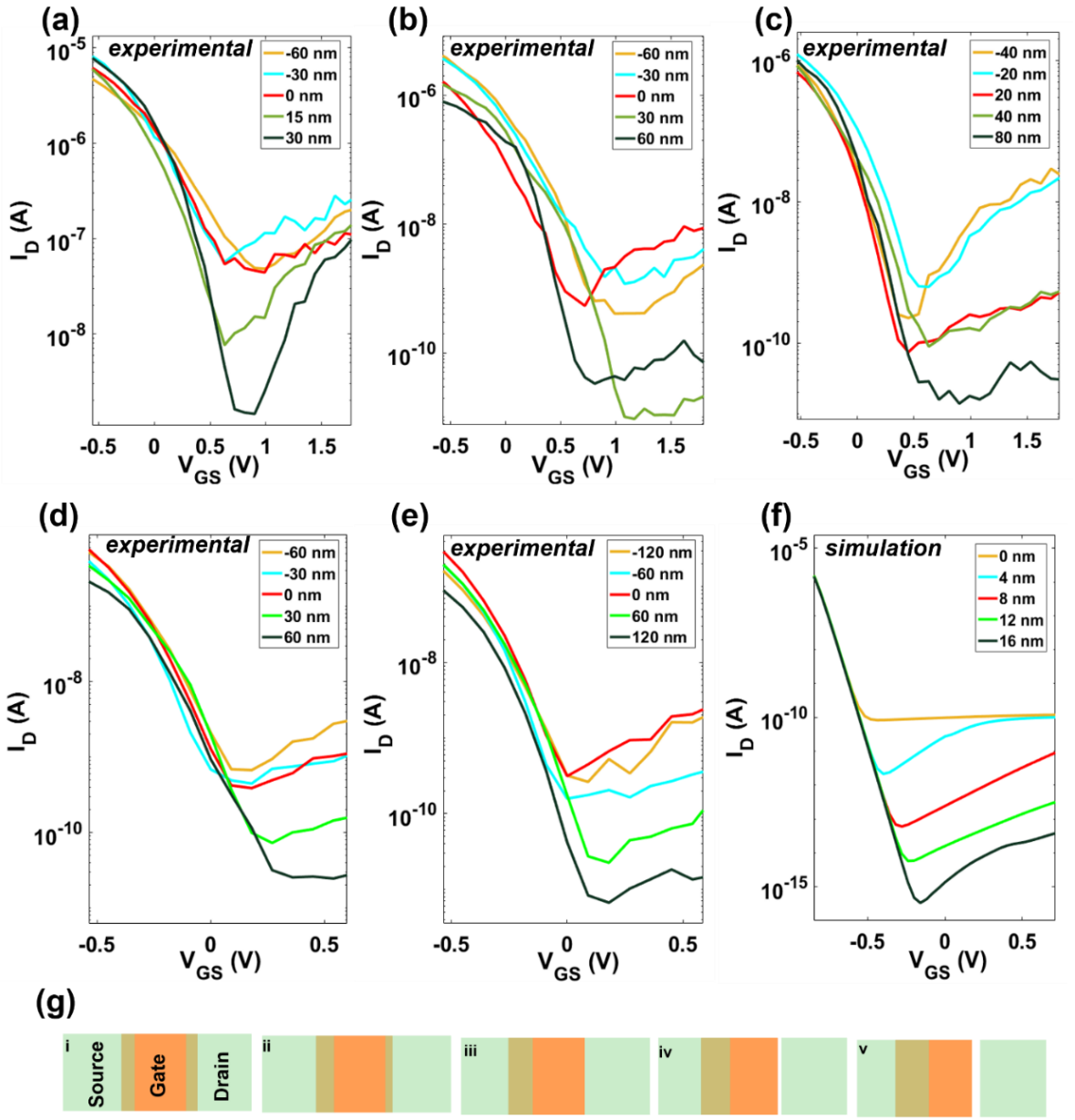
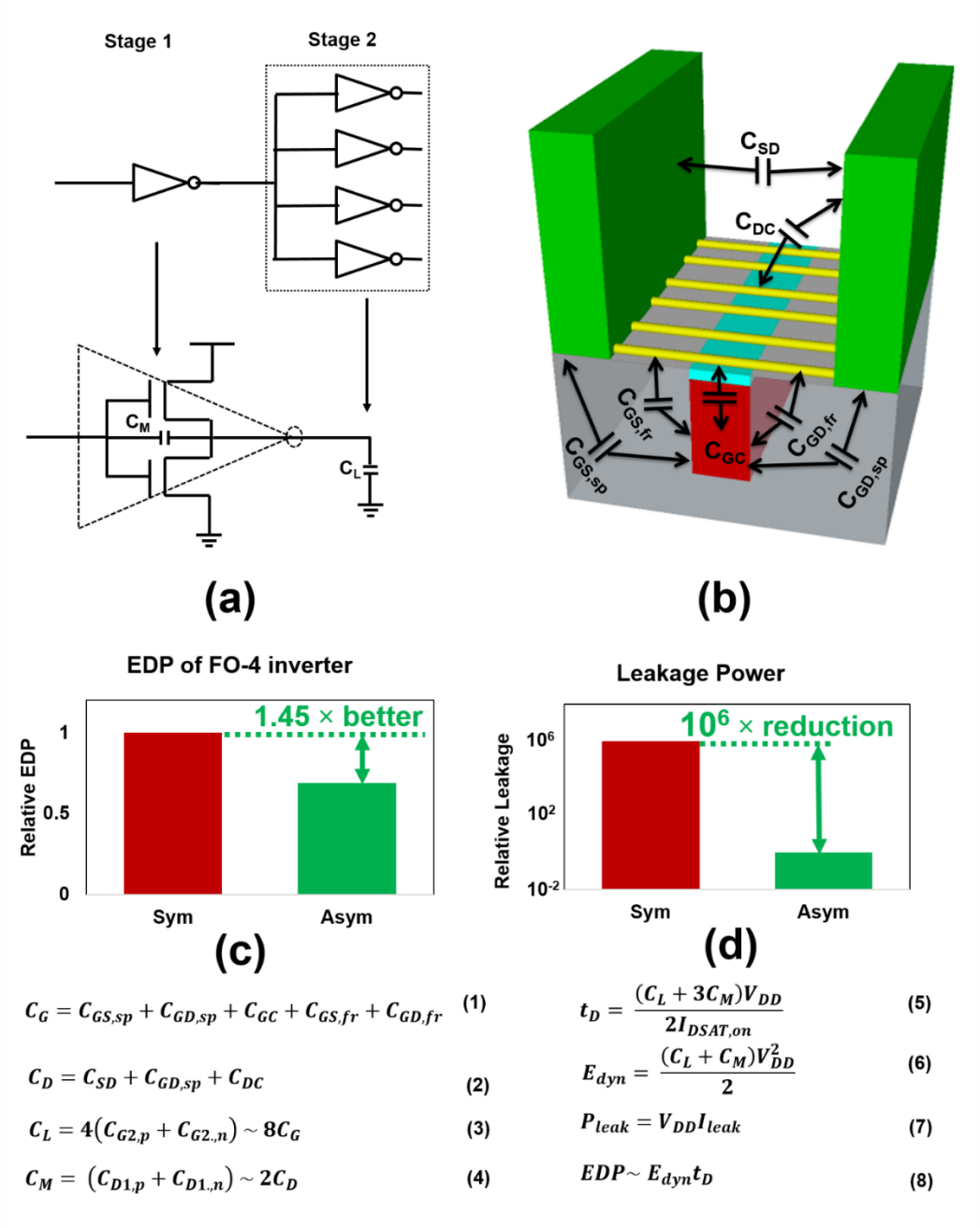


Fig. 4.4. (a-e) Experimental I_D-V_{GS} characteristics of back-gate CNFETs with varying L_{SP} [defined in Figure 4.1a], showing an average reduction of I_{off} by ~60×, and with average improvement in I_{on}/I_{off} by ~30×. Similar to Fig. 4.2, from (a) through (e), the channel lengths are: 180 nm, 500 nm, 1 µm, 1.5 µm, and 2 µm, respectively. (f) Simulated I_D-V_{GS} characteristics of the symmetric vs progressively asymmetrically back-gate CNFETs with varying L_{SP}. Table 4.2 lists the device parameters used for the device model. (g) Schematic of symmetric vs asymmetric back-gate CNFETs for the different CNFETs plotted in (a) through (e).

Scanning electron microscopy (SEM) images of fabricated CNFETs ranging from symmetric gate CNFETs to CNFETs with varying degrees of asymmetry in the gate structure (*i.e.*, varying amounts of lateral shifts away from the drain) are shown in Figure 4.1c-e. The varying amounts of lateral shifts are introduced during lithographic patterning of the gate, and are quantified by the length of the intrinsic CNT region (L_{SP}, Figure 4.1a) separating the gate and drain. Similar to Figure 4.3, we measure the experimental I_D-V_{GS} characteristics for CNFETs with varying channel lengths (L_{CH} = 2 μm down to 180 nm). Figure 4.4 shows typical I_D-V_{GS} characteristics for these devices, including both symmetric and asymmetric CNFETs. As illustrated in Figure 4.4, all symmetric CNFETs (and all CNFETs where there is no CNT intrinsic region) suffer from substantial GIDL-induced off-state leakage current. In stark contrast, asymmetric gate CNFETs (with $L_{SP} > 0$ near the drain), have reduced off-state leakage current: the average I_{OFF} reduction exceeds 60× compared to symmetric gate CNFETs, demonstrating the benefits of this approach. Importantly, having large ungated intrinsic CNT regions near the drain introduces additional channel resistance which degrades on-state current (I_{ON}). However, the overall I_{ON}/I_{OFF} ratio, a key metric for device performance, improves by over an order of magnitude: the 60× reduction in I_{OFF} corresponds with an average I_{ON} degradation of <2×, resulting in an overall benefit in I_{ON}/I_{OFF} by >30× (supplemental information). Additionally, we replicate these results with our CNFET model that captures GIDL, simulating matching symmetric and asymmetric gates as our experimental CNFETs in Figure 4.4. Our simulation results validate the experimental data (Figure 4.4a), predicting substantial decreases in off-state leakage current at a minor cost in on-state current. In fact, the model predicts gains can potentially exceed $>10^6$× improvement in I_{ON}/I_{OFF} ratio (assuming ideal CNFET performance).

4.4 Additional Benefits: Energy Efficiency



$$C_G = C_{GS,sp} + C_{GD,sp} + C_{GC} + C_{GS,fr} + C_{GD,fr} \quad (1)$$

$$C_D = C_{SD} + C_{GD,sp} + C_{DC} \quad (2)$$

$$C_L = 4\left(C_{G2,p} + C_{G2.,n}\right) \sim 8C_G \quad (3)$$

$$C_M = \left(C_{D1,p} + C_{D1.,n}\right) \sim 2C_D \quad (4)$$

$$t_D = \frac{(C_L + 3C_M)V_{DD}}{2I_{DSAT,on}} \quad (5)$$

$$E_{dyn} = \frac{(C_L + C_M)V_{DD}^2}{2} \quad (6)$$

$$P_{leak} = V_{DD}I_{leak} \quad (7)$$

$$EDP \sim E_{dyn}t_D \quad (8)$$

Fig. 4.5. (a) Schematic of a FO-4 (fan-out 4) inverter with highlighted load capacitance and miller capacitances. (b) Schematic of a back-gate CNFET, highlighting parasitic source and drain capacitances (C_{GS} and C_{GD} respectively). (d) Energy-delay product (EDP) of a FO-4 inverter design with symmetric and asymmetric gate CNFETs. EDP defined in Equation 8. Equations 1-7 are used to calculate dynamic energy, delay and leakage power (considering miller capacitances [Sedra 1998, Rabaey 2002, Andreev 2006]).

Improvement in the miller capacitances (Fig. 3.5c) for asymmetric CNFETs lead to a 1.45× improvement in EDP. (e) Comparison of simulated leakage power of a FO-4 inverter for the symmetric vs asymmetric gate technologies. Figure 4.5(c-e) are calculated using extracted device parameters from Sentaurus device simulations for a symmetric and asymmetric back-gate CNFET. For the symmetric back-gate CNFET, we assume 120 nm gate overlap with the source and drain, whereas for the asymmetric back-gate CNFET, the gate is offset from the drain by 16 nm (e.g., L_{SP} = 16 nm).

Moreover, the asymmetric gate geometry also affects the parasitic capacitances of the CNFETs. As the gate laterally shifts further from the drain towards the source, the parasitic source capacitance increases while the parasitic drain capacitance decreases (Figure 4.5). To analyze the circuit-level impact of these asymmetric gates, we analyze a fan-out 4 inverter (Figure 4.5a) using extracted device parameters from the TCAD Sentaurus simulations. Due to the reduced parasitic drain capacitance (the effect of which is amplified as the impact this capacitance has on the circuit is amplified due to the Miller Effect [Sedra 1998, Rabaey 2002, Andreev 2006]), the asymmetric CNFETs actually yield a slight (~1.45×) benefit in energy-delay product (EDP, a metric of energy-efficiency) versus symmetric CNFETs[h].

4.5 Summary

In this work, we experimentally reveal the significant impact of GIDL on CNFETs, and provide an experimentally-calibrated model that closely matches our measured results. Moreover, we demonstrate a path for mitigating this off-state leakage current by engineering CNFET geometries with asymmetric gates. We experimentally demonstrate this approach reduces off-state leakage current by >60× while our calibrated models show potential benefits exceeding 10^6×. Thus, this

[h] Here, we analyze the impact for fan-out 4 inverters, although digital systems would also account for Miller Effect in other combinational and sequential logic gates. However, it is important to note that we show there is not an EDP degradation due to the change in capacitances for asymmetric FETs.

work addresses a key challenge facing CNFET-based electronics, and demonstrates a promising path towards realizing energy efficient CNFET VLSI digital circuits.

Table 4.1. Device Parameters used in experiment

L_{CH}(μm)	0.09	0.18	0.5	1	1.5	2
L_G (μm)	0.33	0.42	0.74	1.24	1.74	2.24
L_C (μm)	0.5	0.5	2	3	3	3
H_G (nm)	15	15	15	15	15	15
H_C (nm)	25	25	25	25	25	25
T_{OX} (nm)	10	10	10	10	10	10
Width(μm)	2	2	2	2	2	2

Table 4.2. Device Parameters used in simulation

L_{CH}(μm)	0.18
L_G (μm)	0.42
L_C (μm)	0.5
H_G (nm)	15
H_C (nm)	25
T_{OX} (nm)	10
K_{SPACER}	5.5
K_{OX}	10.3

Chapter 5: Monolithic 3D Imager

5.1 Background

Real-time, low-latency object classification from images or video is critical for a myriad of next-generation applications ranging from autonomous driving to robotics to augmented reality [Lecun 2015, Ren 2015]. However, such data-intensive applications are severely limited by the "communication bottleneck": where the performance (e.g., speed and energy-efficiency) of such systems are dominated not by capturing the image itself but instead by the rate at which data can be read from the pixel array, stored in memory, read from the memory by a processor, and then classified (Figure 5.1) [Horowitz 2014, Rogers 2009]. To overcome this challenge, significant work today focuses on integrating imagers, memory, and logic through chip-stacking, whereby heterogeneous chips are stacked and bonded over one-another, using through-silicon vias (TSVs) to connect vertical layers [Gagnard 2010, Tsugawa 2017].

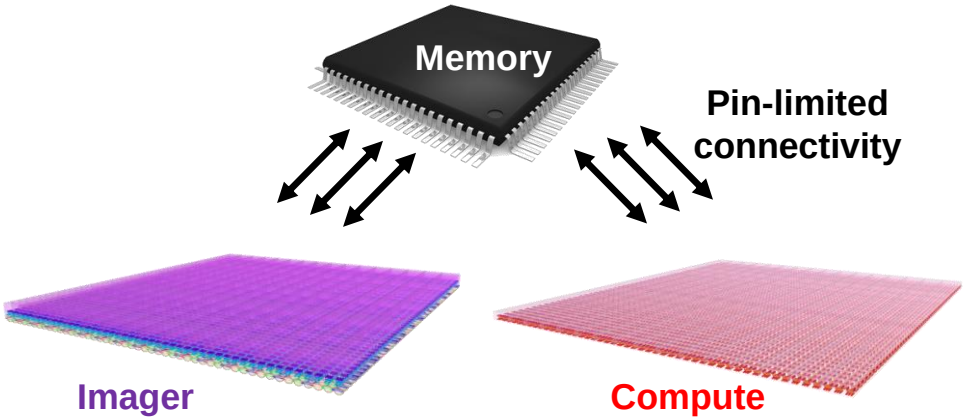


Fig. 5.1. 2D Image sensor with separate memory and compute ICs. The imager has to send data to a separate compute chip through a separate memory chip where data movement is limited by the pin-limited connectivity of the ICs

While TSV-based approaches can provide benefits, they face several limitations (Figure 5.2): (1) the imager material is limited to substrates that have similar thermal expansion rates as silicon to

avoid failure during wafer bonding to memory or logic dies/wafers (which are made from silicon), (2) TSVs require large keep-out-zones (KOZ), limiting the fill-factor of the pixels, memory, and/or logic layers, and (3) TSV dimensions (on the order of µms) limit via density and thus bandwidth between vertical layers.

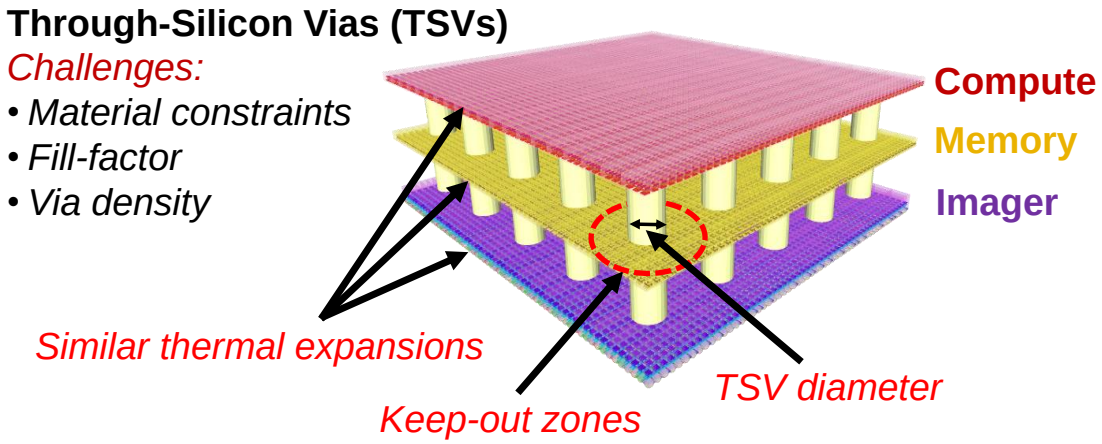


Fig. 5.2. Modern 3D integrated Imagers where different layers – imager, memory and compute ICs are integrated using through-silicon-vias (TSVs). Such imagers are often constrained by material choices (different TSV integrated ICs have to fabricated on the same material substrate to avoid wafer bonding failures). Additionally, due to the large size of the TSVs (~µms), they impose restrictions on the fill-factor of each pixel in the imager, simultaneously having much lower density compared to conventional back-end-of-line (BEOL) vias.

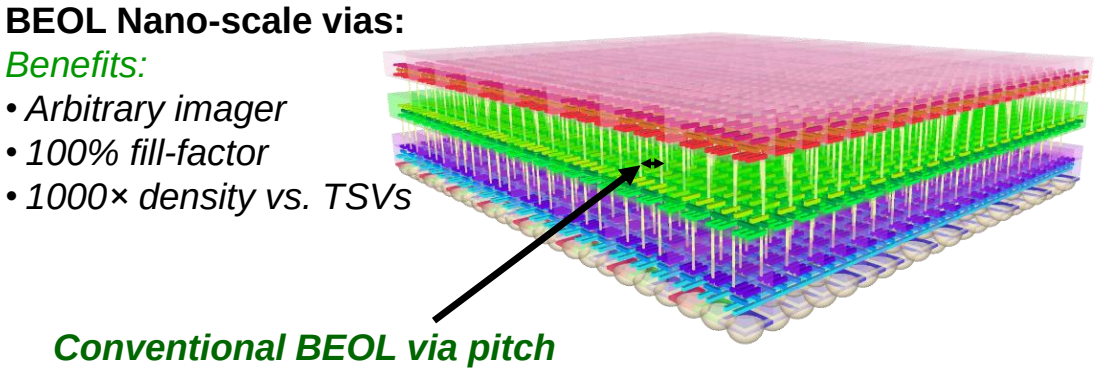


Fig. 5.3. Dream Monolithic 3D Imager Chip – where various layers of imager and compute are densely integrated by conventional BEOL vias. The imager can send data directly to compute without needing to store frames in an intermediate memory layer. Such imagers can capture and compute on all the pixels in

parallel with significantly lower latency, where the output of the imager is highly processed information instead of raw pixel data.

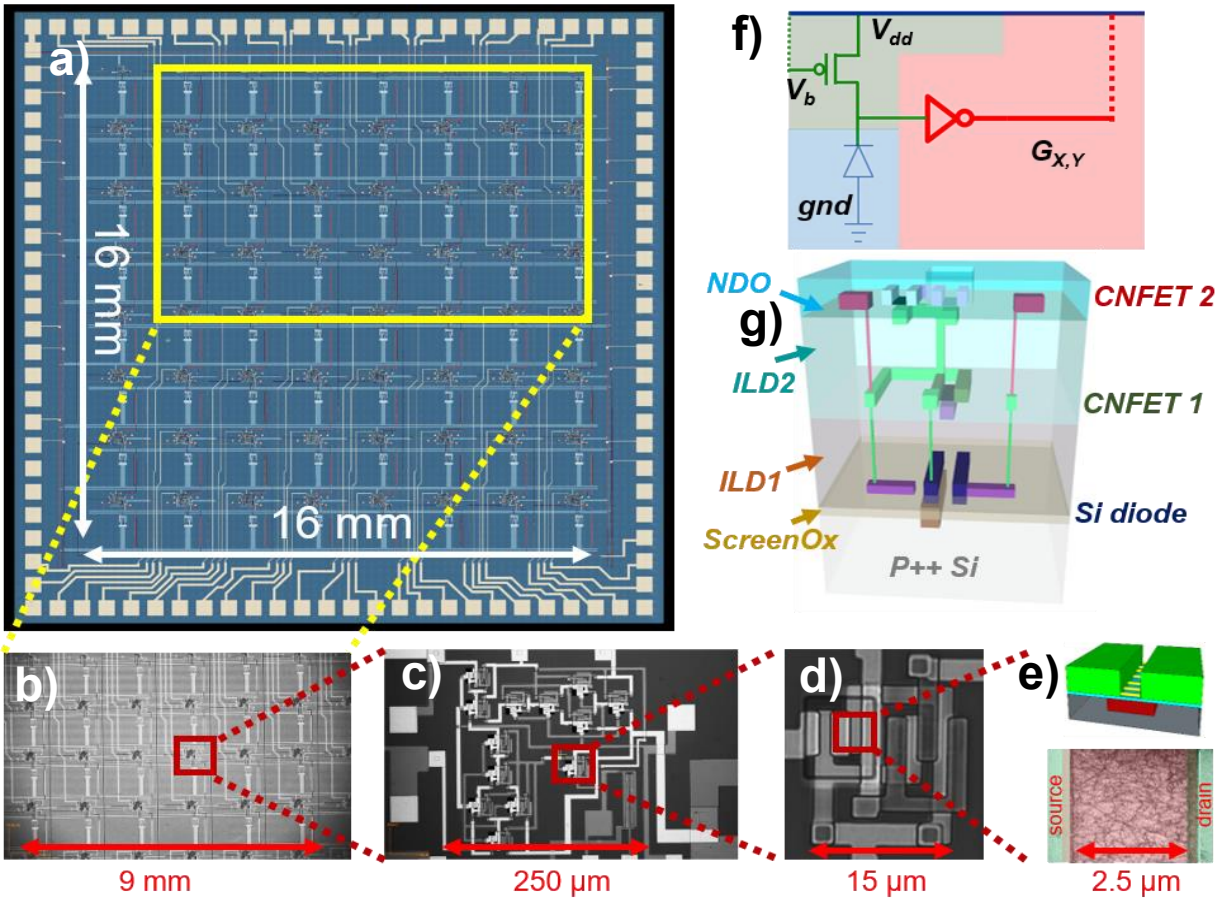


Fig. 5.4. (a) 3D imager micrograph (b) magnified optical microscopy image of sub-circuit, (c) edge-detector logic block with load CNFET, (d) CMOS CNFET inverter and (e) a typical CNFET, (3D model with SEM of channel, false colored to match the model). (f) Schematic and (g) 3D model of a Si photodiode (layer 1, highlighted in blue) monolithically integrated with a load CNFET (layer 2, highlighted in green) for transducing the current signal to voltage signal and a CMOS CNFET inverter (layer 3, highlighted in red) for digitizing the voltage output.

To overcome these challenges, we experimentally demonstrate a prototype monolithic 3D imaging system with layers of computing circuits fabricated directly vertically over the imager substrate without any die- or wafer-bonding (Figure 5.3-4). This eliminates the need for serially reading the pixel array data to/from memory before classification. By monolithically integrating layers of

computing circuits (e.g., analog-to-digital converters and digital logic) directly in the back-end-of-line (BEOL) over the imaging pixels, such monolithic 3D imagers can capture and compute on all of the pixels in parallel with significantly lower latency (without requiring costly serial accesses to memory). This transforms the imager output from raw pixel values to highly-processed information: the output from the camera system itself is object detection, classification, etc. Moreover, compared to conventional chip-stacking, our monolithic 3D approach (1) can be fabricated over arbitrary imaging substrates (Si, Ge, III-Vs, etc.), (2) requires no KOZ and thus the imagers and logic can realize nearly 100% fill-factor, and (3) can realize >1,000× vertical interconnect density (and thus increase in data bandwidth between layers) (BEOL nano-scale vias (ILVs) used for monolithic 3D can be >1,000× denser than TSVs, Figure 5.3) [Sabry 2015].

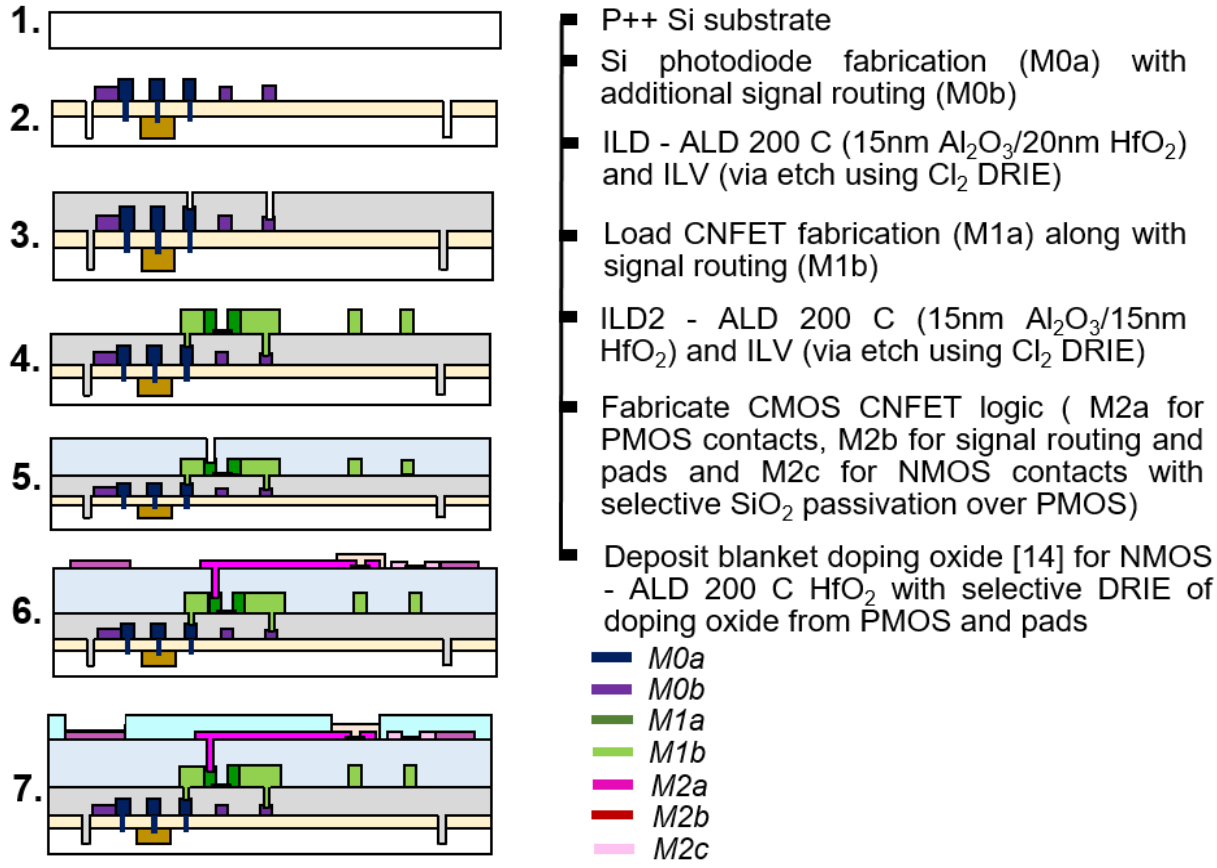


Fig. 5.5. 3D imager process flow with description (right). All patterning is done using MLA-150 direct write photolithography and all metal deposition done using electron beam evaporation and liftoff. Horizontal p-n

Si photodiodes were fabricated by implanting Sb (1e14 cm^{-2} , 60 KeV, 7° tilt) over a P++ Si wafer with 30 nm screening ox (950C, 1 hr). Back-gate CNFETs [Srimani 2018, Lau 2018] were fabricated by a gate-before-channel CMOS CNFET process [14] using solution-based CNT deposition (99.9% pure semiconducting CNTs [Nanointegris]).

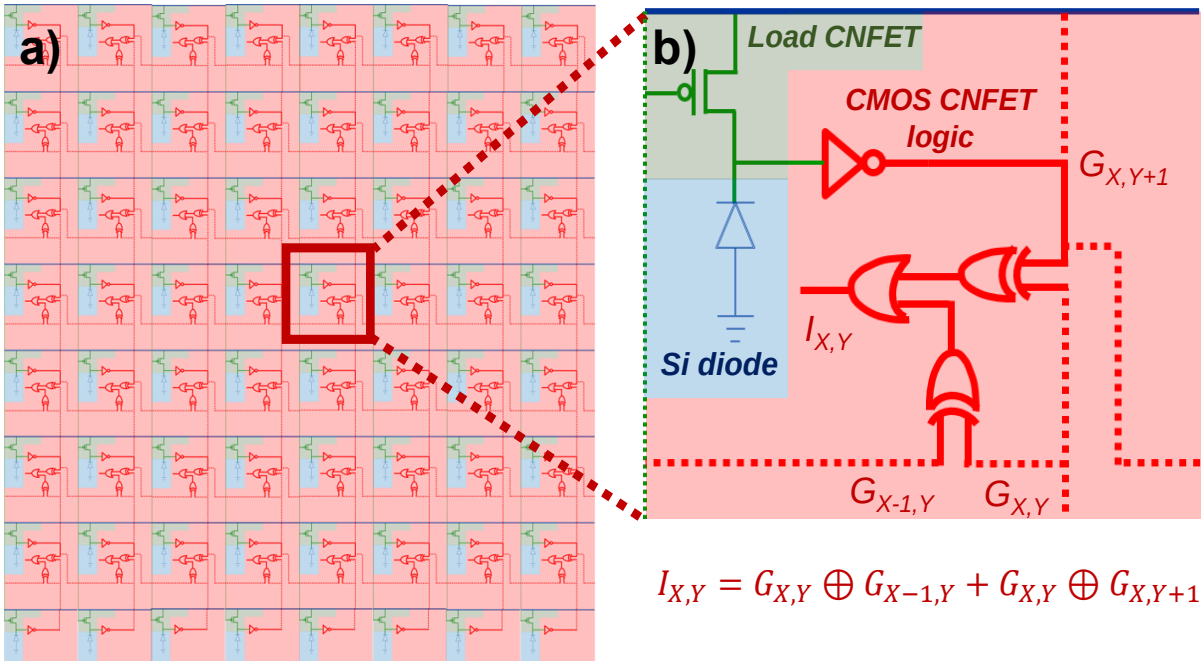


Fig. 5.6. (a) 8x8 3D imager schematic (b) edge-detector sub circuit highlighting different layers of active devices showing bitwise horizontal and vertical XOR operation summed up using OR gates leading to edge detection. Schematic is color coded to highlight the different physical layers of devices to match Fig 1. Layer 1 (blue) comprises of an 8x8 array of p-n Si photodiodes, connected to layer 2 (green) consisting of PMOS CNFETs transducing the current signal to a voltage output finally connected to layer 3 (red) with CMOS CNFET inverters digitizing the output from the load CNFETs and XOR based edge detector circuit.

5.2 Hardware Prototype

While realizing monolithic 3D is challenging with Si CMOS due to its high temperature process (>1,000 °C, which can damage bottom layer devices and interconnects, [Vinet 2011]), we naturally enable such systems by using CNFET CMOS. We use CNFETs for upper-layers of logic because (1) their low-temperature processing (<300 °C) is within the BEOL thermal budget, and (2) CNFETs promise a ~10× benefit in energy-delay product (EDP) versus silicon CMOS [Hills

2018]. Our hardware prototype is shown in Figure 5.4. It consists of three monolithically integrated vertical layers: layer #1: a traditional Si imager using p-n junction photodiodes, layer #2: programmable digitization of the analog pixel output, layer #3: CNFET logic performing edge detection. As a demonstration, the prototype monolithic 3D imager is an 8×8 pixel array and comprises 2,784 CMOS CNFETs; all design and fabrication is wafer-scale (150 mm substrates) and VLSI- and silicon-CMOS compatible (process flow in Figure 5.5 [10]).

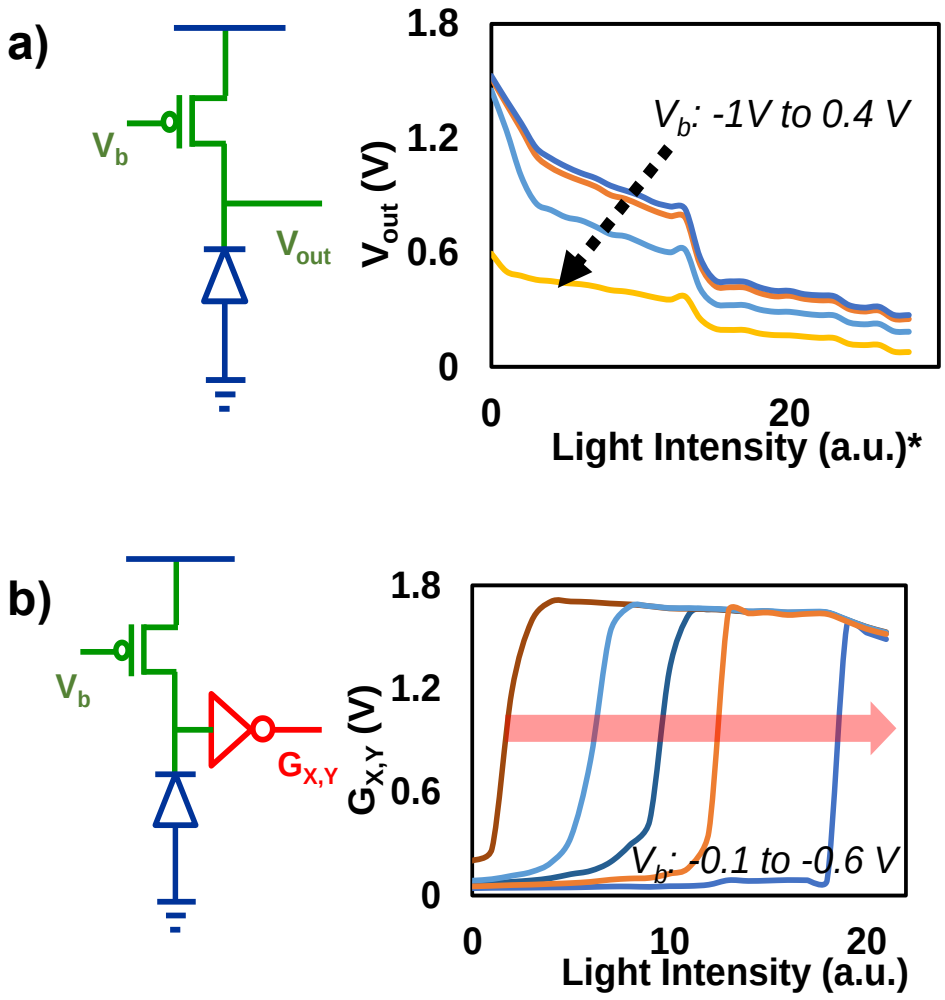


Fig. 5.7. (a). Si photodiode with load CNFET (schematic and electrical response) (b). Si photodiode with the digitizer (schematic and electrical response). Individual circuit components color coded to match Figure 5.4. *Light intensity scaled to the output power of the light source.

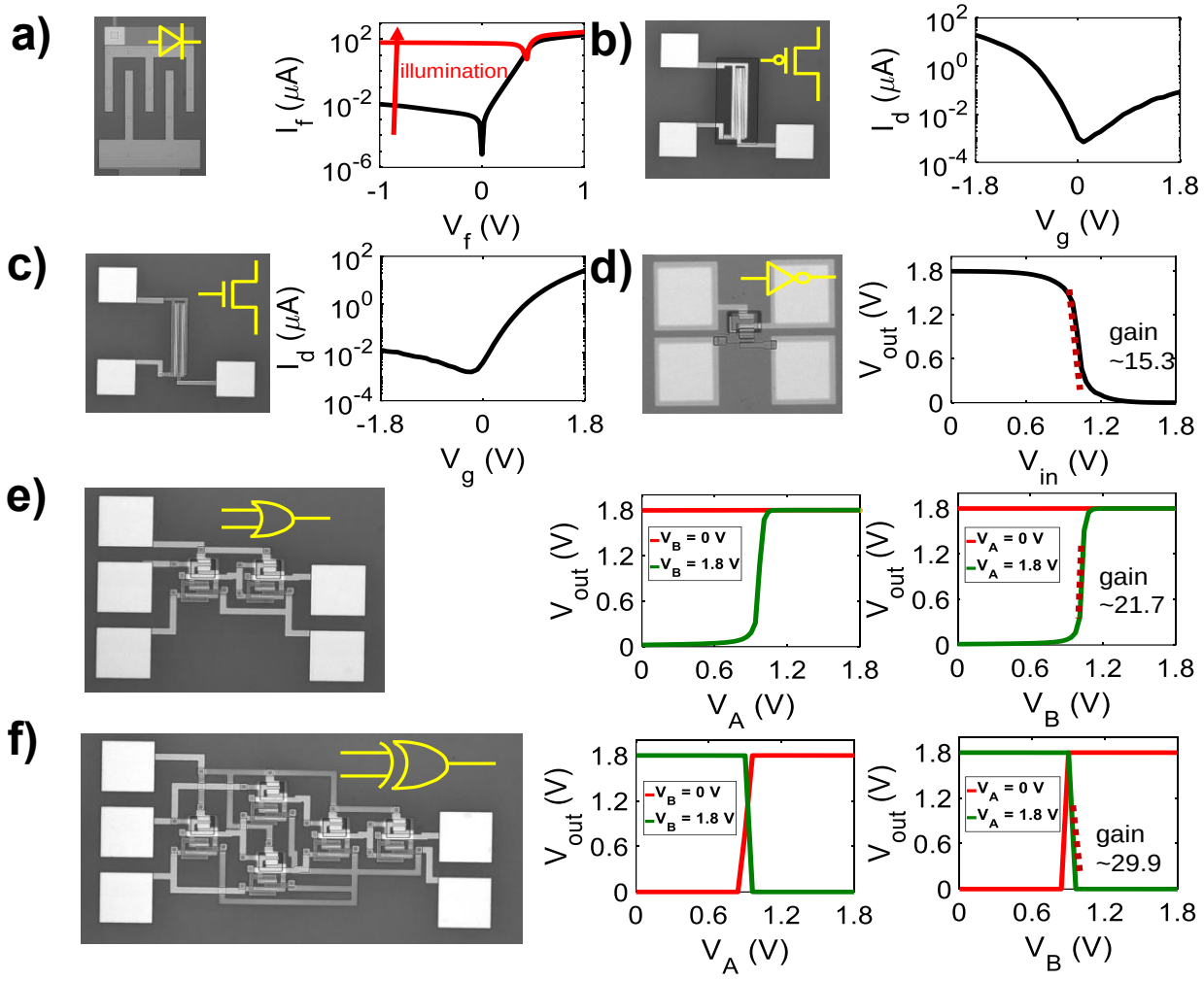


Fig. 5.8. Individual circuit components – optical microscopy images (with circuit symbol) and typical electrical response (a) p-n Si photodiode (b) PMOS CNFET (c) NMOS CNFET (d) CMOS CNFET inverter (>97.7% signal swing) (e) CMOS CNFET OR gate (>98% signal swing) and (f) CMOS CNFET XOR gate (>99.86% signal swing). For (b) and (c) I_D-V_{GS} characteristics is measured at V_{DS} = -1.8 V

Figure 5.6 shows the circuit schematic of a monolithic 3D pixel cell, as well as the full imager architecture. Data from all Si pixels on layer #1 are read in parallel through conventional ILVs used in the BEOL to layer #2 (i.e., no TSVs). On layer #2, a CNFET load transistor (with an adjustable gate bias) converts the pixel current to a voltage (Figure 5.6b). Again, in parallel, all

pixel voltages are passed to layer #3 through ILVs, where CNFET CMOS logic then: (1) digitizes the voltage through a CNFET inverter, and (2) performs edge detection across the entire image (horizontal and vertical XOR operations are summed using OR gates to perform the edge detection). Thus, the imager output is edge detection rather than the raw pixel data (image output in Figure 5.9). Although we implement edge detection on our monolithic 3D prototype, our approach demonstrates the feasibility of large-scale monolithic 3D imaging systems, e.g., with high-resolution imagers integrated directly underneath a computing system implementing a convolutional neural net for low-latency image classification.

5.3 Experimental Results

Figure 5.7 and Figure 5.8 provide measured characteristics of the sub-systems and circuits comprising the imager. Figure 5.7 shows the digitized output response of a single monolithic 3D pixel cell comprising the Si pixel (layer 1), CNFET voltage converter (layer 2), and CNFET inverter for digitization (layer 3); by adjusting the biasing voltage, we can select the threshold for the digitization). Voltage transfer curves (VTCs: output voltage vs. input voltage) for all of the CNFET CMOS logic gates are shown in Figure 5.8. Figure 5.9 (Imager demo setup in Figure A10.1) shows the output of the full imager. We physically mask off different regions of the imager and illuminate the system with light. An image of the mask and the subsequent readout from the imager shows functional edge detection for a variety of shapes.

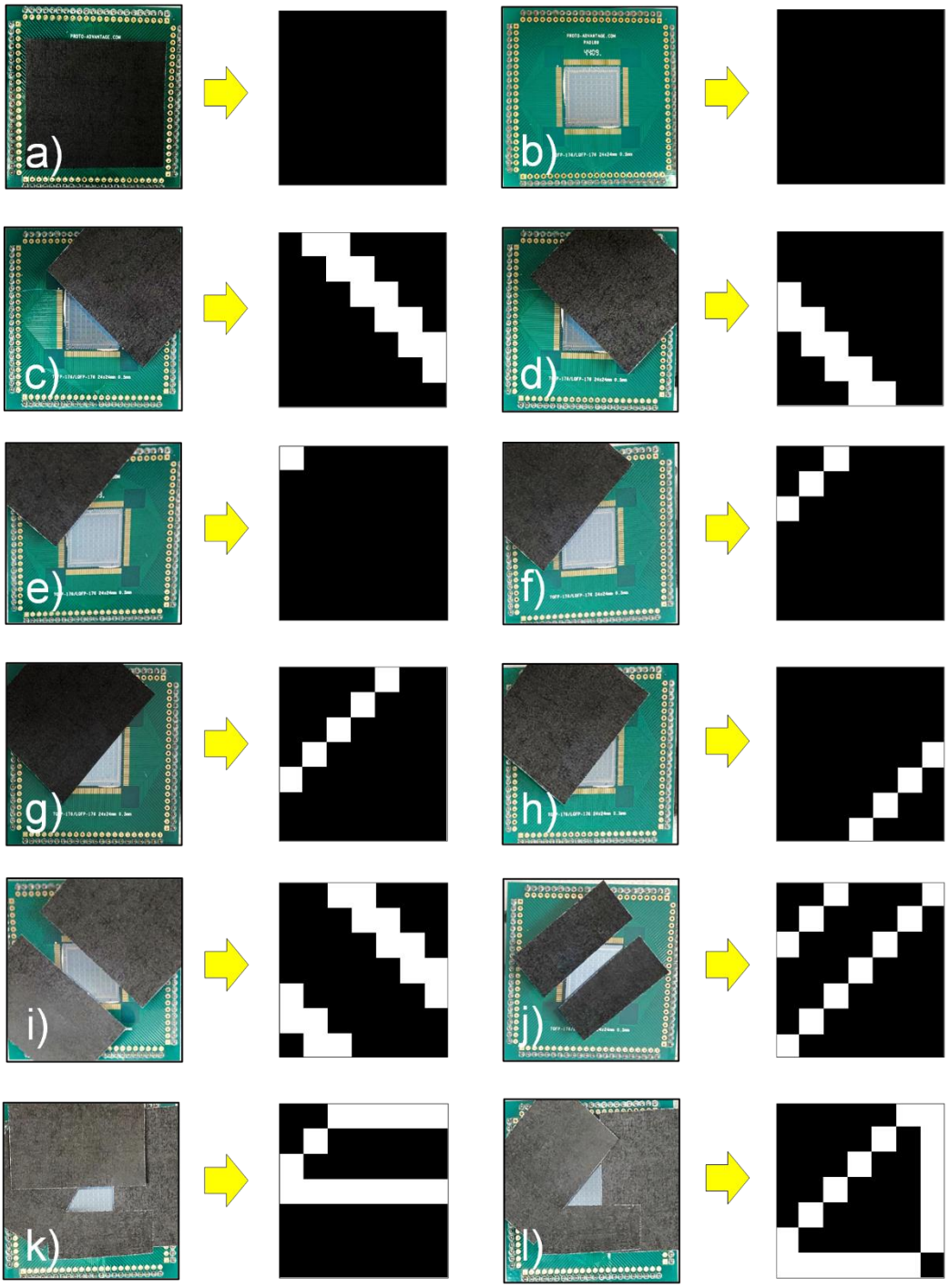


Fig. 5.9. Experimental output response ($I_{X,Y}$) of the edge-detector circuit for (a)-(b) dark and illuminated backgrounds, (c)-(h) single lines in different directions moved spatially, (i)-(j) multiple lines, (k) trapezium and (l) triangle

5.4 Summary

We demonstrate a monolithic 3D imager comprising 3 vertically-integrated circuit layers: 2 layers of CNFETs over a conventional silicon imager substrate. While our hardware prototype performs edge detection, such systems pave the way for additional computing layers to perform critical tasks such as object detection or classification; transforming sensor outputs from raw data to actionable information.

Chapter 6: Foundry Transfer

6.1 Background

The inevitable slowing of two-dimensional scaling is motivating efforts to continue scaling along a new physical axis: the 3rd dimension. Here we report back-end-of-line (BEOL) integration of multi-tier logic and memory established within a commercial foundry. This is enabled by a low-temperature BEOL- compatible complementary carbon nanotube (CNT) field-effect transistor (CNFET) logic technology, alongside a BEOL- compatible Resistive RAM (RRAM) technology. All vertical layers are fabricated sequentially over the same starting substrate, using conventional BEOL nano-scale inter-layer vias (ILVs) as vertical interconnects (e.*g.*, *monolithic* 3D integration, rather than chip-stacking and bonding). In addition, we develop the entire VLSI design infrastructure required for a foundry technology offering, including an industry-practice monolithic 3D process design kit (PDK) as well as a complete monolithic 3D standard cell library. The initial foundry process integrates 4 device tiers (2 tiers of complementary CNFET logic and 2 tiers of RRAM memory) with 15 metal layers at a ~130 nm technology node. We fabricate and experimentally validate the standard cell library across all monolithic 3D tiers, as well as a range of sub-systems including memories (BEOL SRAM, 1T1R memory arrays) as well as logic (including the compute core of a 16-bit microprocessor) – *all of which is fabricated in the foundry within the BEOL interconnect stack*. All fabrication is VLSI-compatible and leverages existing silicon CMOS infrastructure, and the entire design flow is compatible with existing commercial electronic design automation tools.

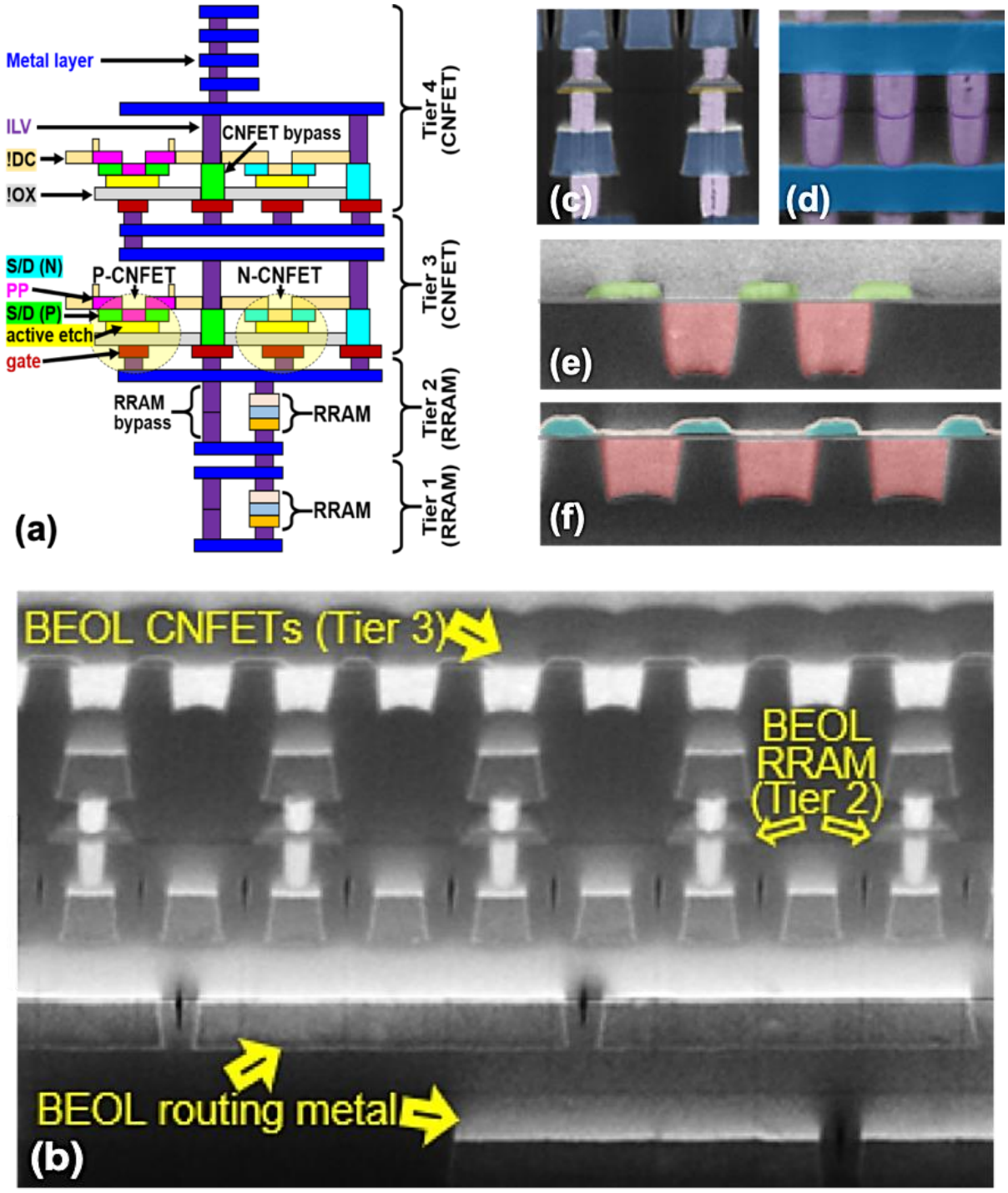


Fig. 6.1: BEOL Multi-Tier CNFET Logic + RRAM process in a commercial foundry. (a) Schematic of the process (from the PDK) established within the foundry. Process includes 4 device tiers (2 bottom tiers of RRAM memory and 2 top tiers of CNFET CMOS logic) and 15 metal layers. (b) Cross-section SEM illustrating section of the stack, showing BEOL CNFETs fabricated directly over BEOL RRAM memory cells with routing above and below. In this cross-section, bottom metal layers show dummy metal fill

(automatically performed using the PDK, Figure 6.5). (c) Magnified view of tight-pitched RRAM (d) Pass-through vias through a device layer, illustrating how any unused device tiers can be leveraged as additional routing resources. (e) NMOS (top) and (f) PMOS (bottom) CNFETs, highlighting CMOS processes using work function source/drain engineering +electrostatic doping through oxide deposition over the NMOS. (c-f) are false-colored to match corresponding coloring in (a).

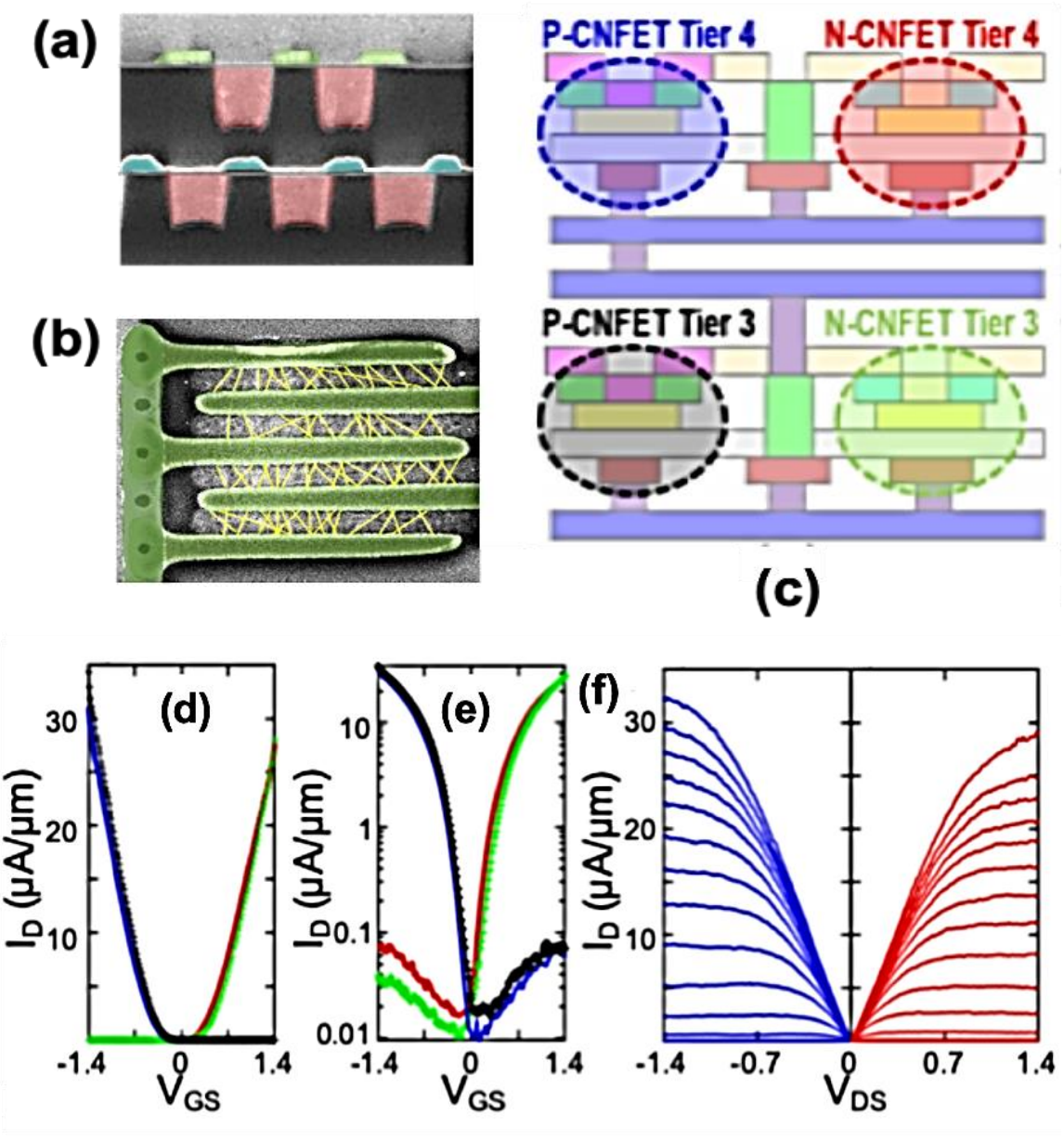


Fig. 6.2: BEOL CNFET CMOS at the 130nm node. (a) Cross-section SEM of two tiers of CNFET CMOS fabricated directly vertically overlapping in the BEOL. (b) Top view SEM of series CNFETs. (c-f) Characterization. (c) shows the physical layout of the BEOL CNFETs. (d-f) show typical I-V curves of P-CNFETs and N-CNFETs fabricated on different layers in the BEOL (colors correspond to colors in (c)),

illustrated matching P- and N-CNFETs, as well as similar characteristics regardless of which layer in the BEOL the CNFETs are fabricated.

6.2 Technology Foundations

Complementary CNFET logic:

CNFETs promise a 10× energy-efficiency benefit versus silicon CMOS [Hills 2018], and our low-temperature CNFET fabrication process (≤425 °C) naturally enables integration in the BEOL [Shulaker 2017]. Figures 6.2 and 6.6 shows the first BEOL complementary CNFET logic within a foundry, leveraging a back-gate geometry with high-*k* / metal gate stack, and follows the "Manufacturing Methodology for CNTs" to overcome inherent CNT defects and variations [Hills 2019]. Purified >99.99% semiconducting CNTs are deposited through solution-based deposition, and any remaining metallic CNTs are addressed through the DREAM design methodology [Hills 2019, Bishop 2020]. To realize a robust wafer-scale complementary CNFET process, we leverage both metal contact work function engineering (to form both PMOS and NMOS) as well as electrostatic doping (to tune threshold voltage [Hills 2019, Lau 2018]). Cross-section images, typical characteristics and additional details are shown in Figures 6.1, 6.2, and 6.6.

CNFET/RRAM memory:

RRAM is a promising non-volatile BEOL-compatible (≤425 °C fabrication) memory with the potential for multi-bit storage [Hsieh 2019]. The RRAM is fabricated in a 1T1R topology, where the selector transistor (CNFET) and RRAM cell (bipolar RRAM with a TiN/HfOX/Ti stack) are fabricated directly vertically overlapping in a monolithic 3D fashion. Cross-section images, typical characteristics, and additional details of the 1T1R monolithic 3D CNFET/RRAM cells are shown in Figures 6.1 and 6.3-4.

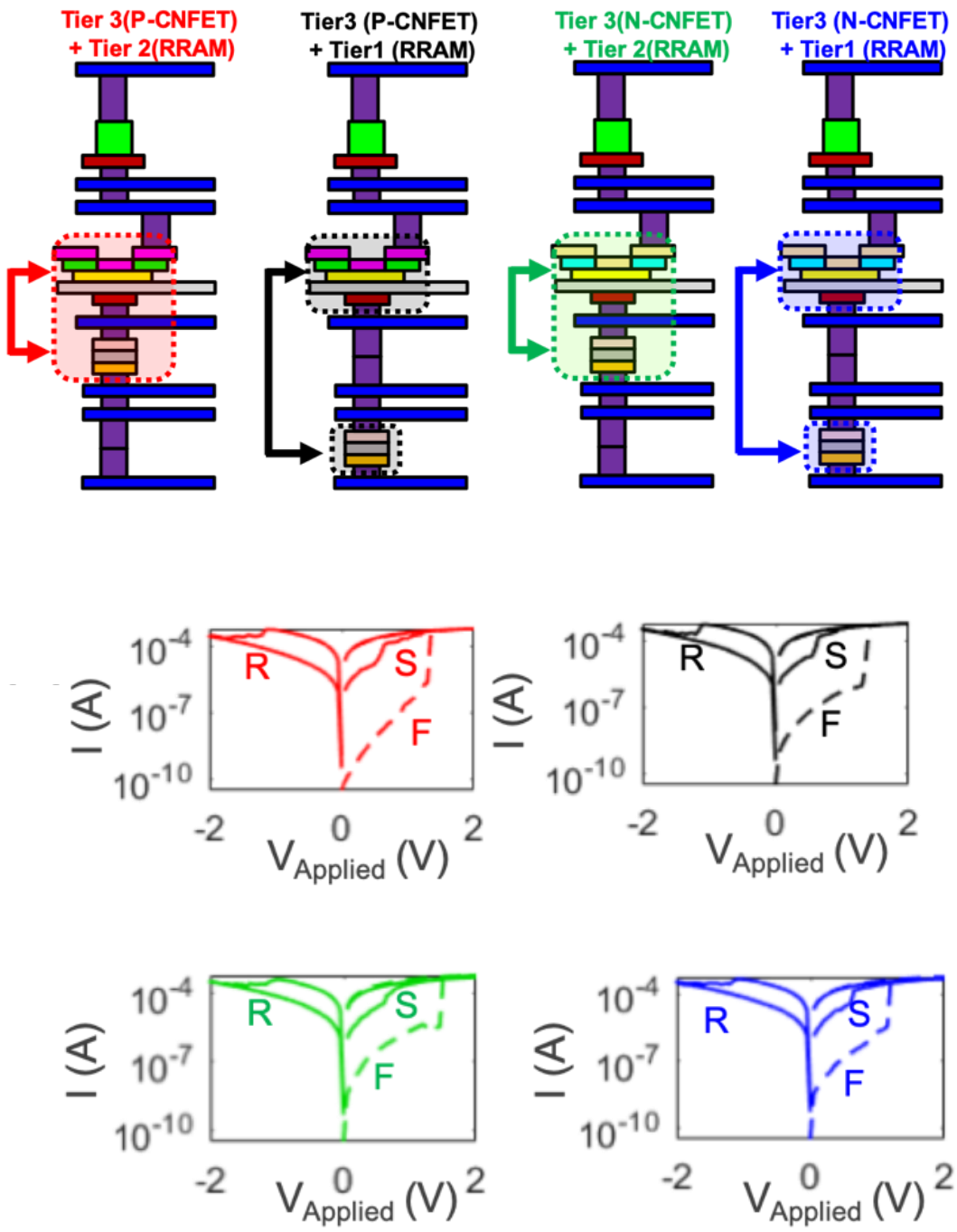


Fig. 6.3: BEOL CNFET/RRAM monolithic 3D memory array characterization. (top) 1T(CNFET)-1R(RRAM) memory arrays are fabricated across different tiers of the monolithic 3D IC, using both PMOS and NMOS CNFETs as the selector. (b) Typical I-V characteristics of a 1T-1R cell, showing the form (F), set(S), and reset(R) of the RRAM cell through the CNFET selector (fabricated directly over the RRAM cell). Colors for (b) correspond to coloring in (a), showing which layers of the monolithic 3D IC the BEOL memory spans.

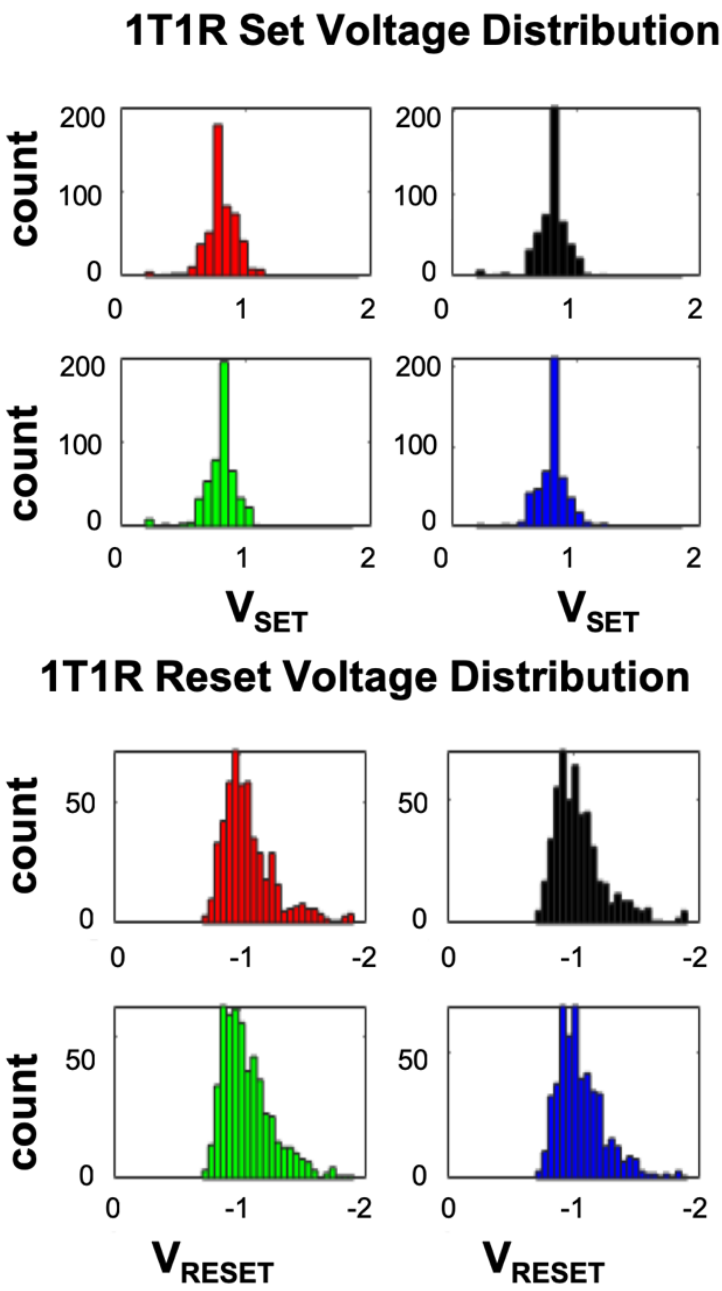


Fig. 6.4: BEOL CNFET/RRAM monolithic 3D memory array characterization. (top and bottom) Distributions of the set and reset voltages for 512-bit arrays fabricated across different BEOL layers within the monolithic 3D IC. Colors correspond to coloring in Figure 6.3, showing which layers of the monolithic 3D IC the BEOL memory spans.

Monolithic 3D:

Integrating devices directly within the BEOL enables tight-pitch vertical interconnects using existing nano-scale ILVs. The resulting dense and fine-grained connectivity between BEOL tiers

of logic and memory promise substantial (>100×) energy efficiency benefits for challenging abundant-data applications. However, such BEOL integration requires low-temperature fabrication to avoid damaging previously fabricated tiers of devices and interconnects (a major challenge for conventional silicon CMOS, which requires >1,000 °C fabrication [Shulaker 2017]). CNFETs and RRAM naturally enable monolithic 3D integration due to their low-temperature fabrication and provides simultaneous device-level as well as system-level energy-efficiency benefits [Shulaker 2017, Sabry 2015].

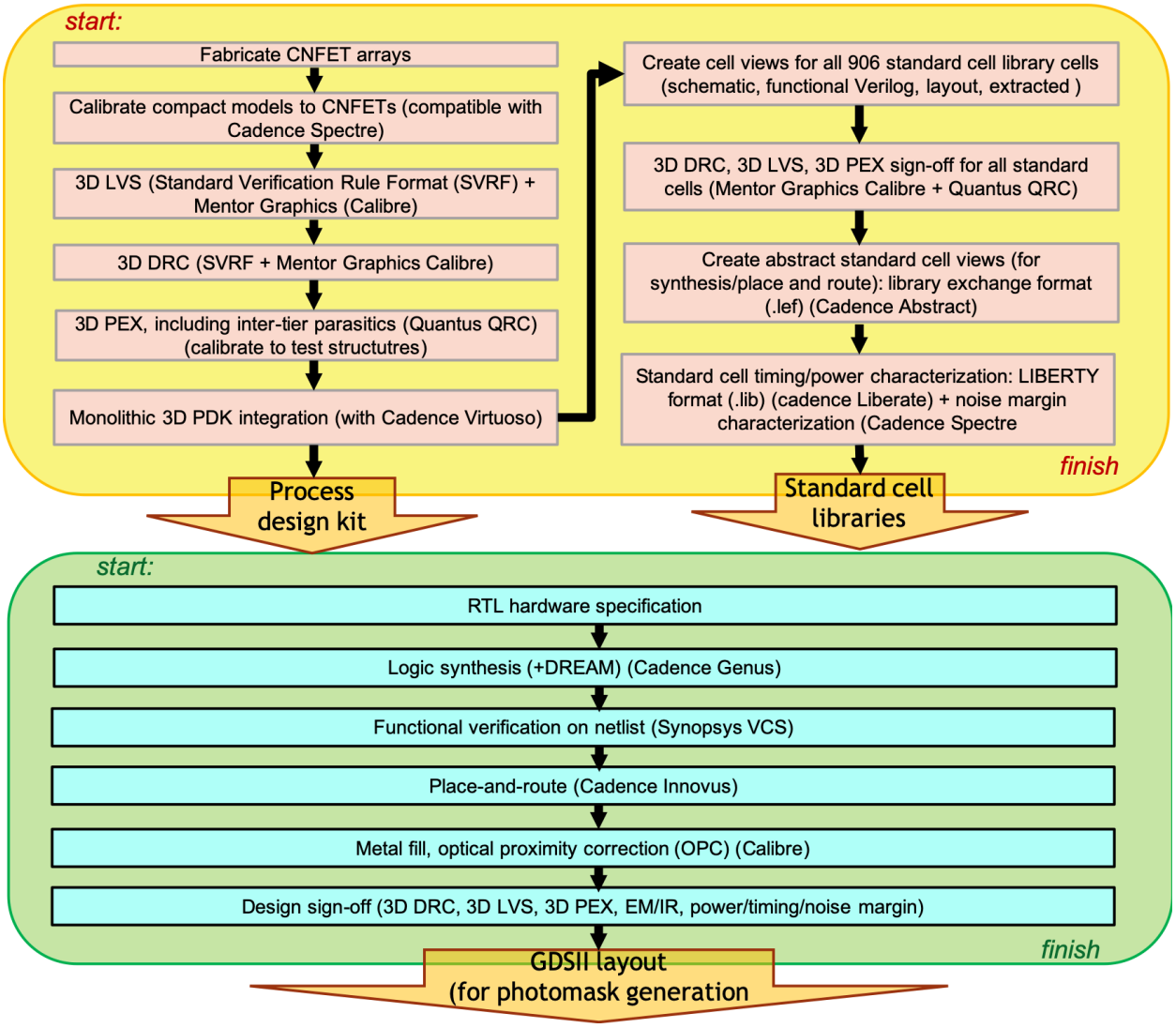


Fig. 6.5: Design infrastructure (+Monolithic 3D PDK) & example physical design flow. Using only industry-standard EDA tools (e.g. Cadence®, Mentor Graphics®).

6.3 Foundry Integration: Process + Design

VLSI Processing:

The initial foundry process is implemented at a ~130 nm technology node across industry-standard 200 mm substrates. The full process (Figure 6.1 shows the full monolithic 3D stack, integrating 4 device tiers distributed throughout the BEOL metal stack) offers 15 metal layers on 13 different physical layers, using 42 mask layers. Owing to the monolithic 3D integration, maximum vertical connectivity between tiers is >11 million vertical interconnects per mm^2 (ILV pitch of ~300 nm, at a ~130 nm node). All fabrication is wafer-scalable without any per- unit customization, leveraging existing silicon CMOS high-volume manufacturing processing and infrastructure.

VLSI Design:

Figure 6.5 summarizes the industry-practice VLSI design flow. The commercial grade PDK includes calibrated compact models for each technology, a 3D design-rule checker (DRC), a 3D layout-vs.-schematic (LVS) checker, 3D parasitic extraction (PEX), *etc*. The 3D PEX accounts for all inter-tier parasitics between all device tiers (CNFETs and RRAM; this is in contrast to prior works which often partition a design across tiers and design each tier independently). The library contains 906 standard cells (distributed across all of the multiple tiers), including high-density, high-speed, and low-leakage standard cell variants. Importantly, our design flow uses existing commercial tools and performs all steps required to transform high-level description to final reticles (synthesis, place&route, EMIR, OPC, metal fill, *etc*.).

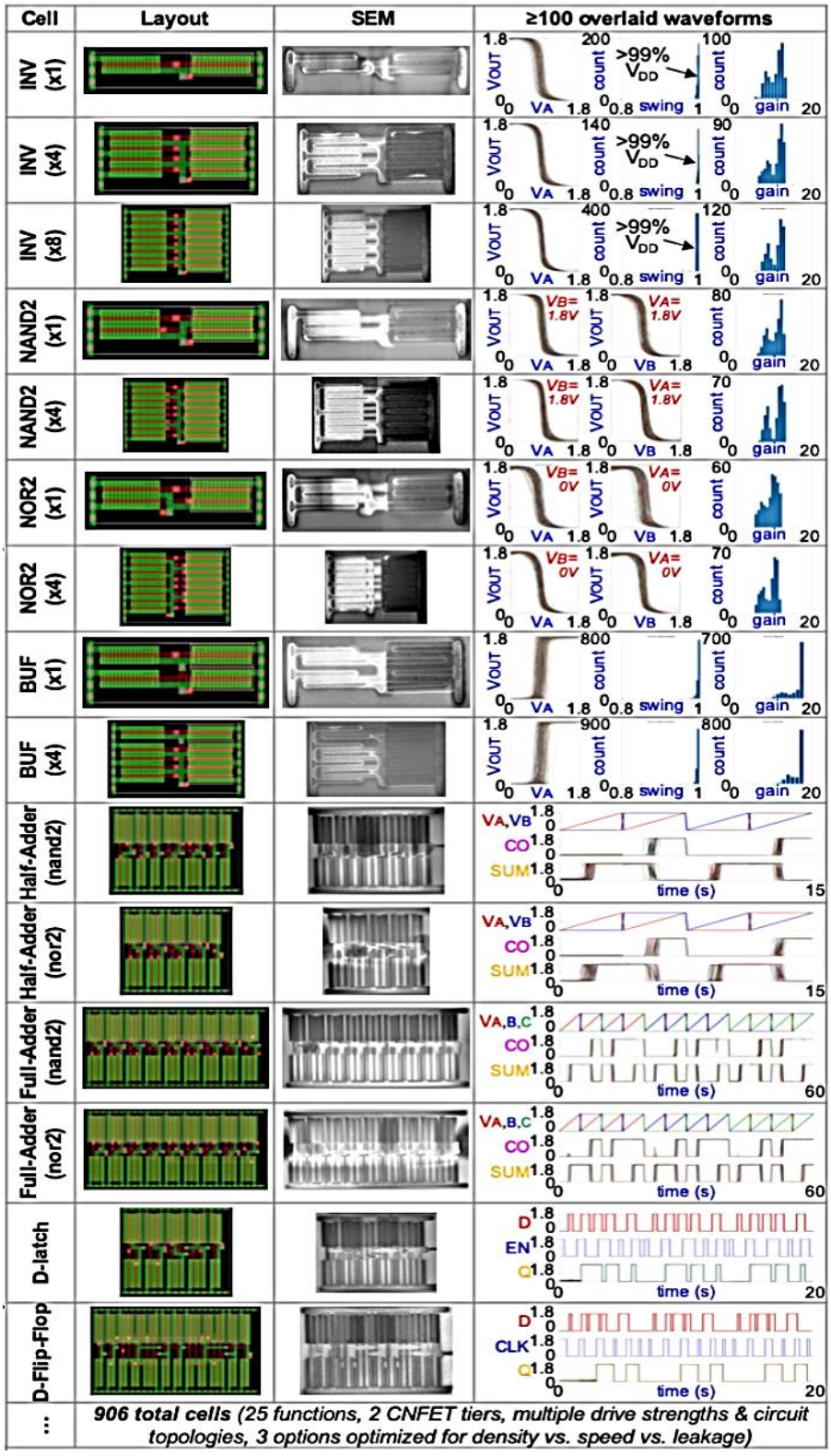


Fig. 6.6: Standard Library Cells, including GDS layout view, SEM microscopy image, and electrical measurement results for most-commonly used cells. For the measured results, each plot shows at least

100 overlaid output waveforms measured from different fabricated cells, demonstrating the reproducibility and robustness of the process. Gain (maximum absolute value of $\Delta V_{OUT}/\Delta V_{IN}$) is ~10 for single logic stages (e.g. INV, NAND2, NOR2) and is higher for cascaded logic stages (e.g. BUF); swing (difference between maximum V_{OUT} and minimum V_{OUT}) is ~99% of the supply voltage (V_{DD} = 1.8V) for all cells. Additional library cell functions include (but are not limited to: D-flip-flops with asynchronous reset, D-flip-flops with scan, clock gating cells, multiplexors, exclusive-OR, exclusive-NOR, fill cells (to connect power rails during the place-and-route), and decap cells (to increase capacitance between power/ground supply rails). Established process is at a ~130 nm technology node.

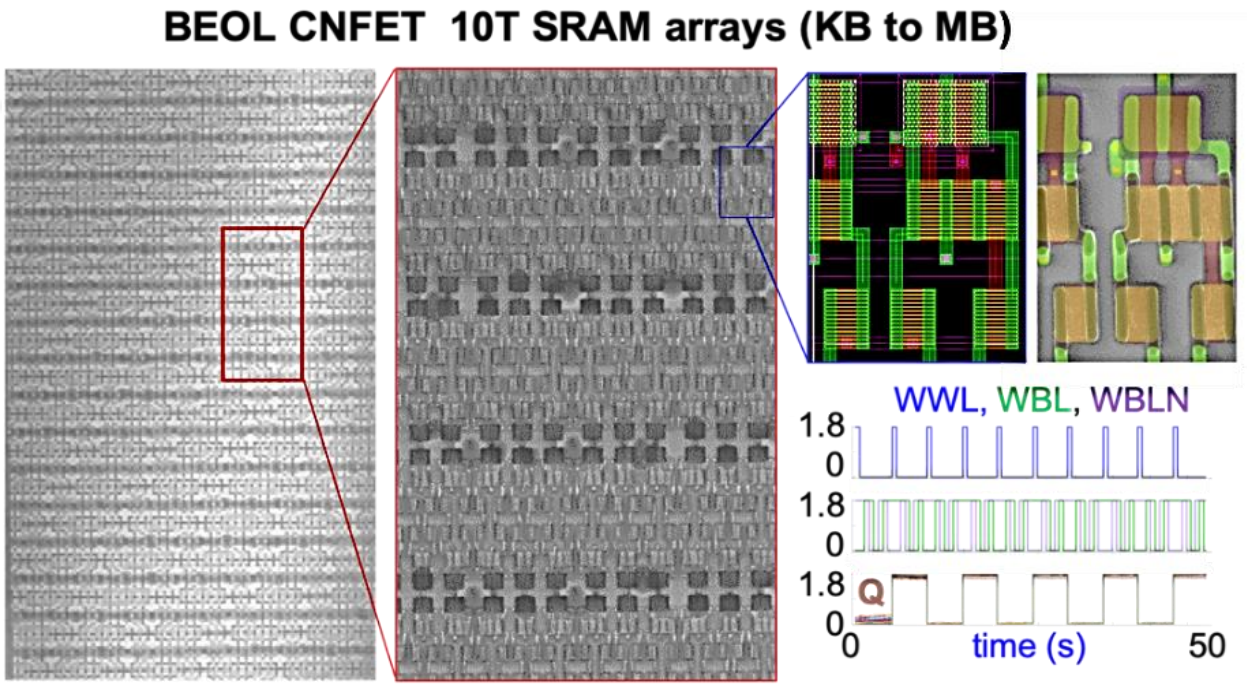


Fig. 6.7: CNFET CMOS 10T SRAM. Complete SRAM memory design, including address decoder, pre-charge, and sense-amp circuitry, designed using custom memory compiler in conjunction with design flow in Figure 6.5. (bottom right) Electrical characterization results from measuring 1Kbit of 10T SRAM cells; the Write Word Line (WWL) assigns the value of the Write Bit Line (WBL, complement = WBLN) to Q (internal node).

6.4 Hardware Experimental Results

To validate the standard cell library and characterize the technologies, Figure 6.6 shows measured waveforms for a subset of the standard cells (combinational blocks such as full adders, sequential blocks such as flip-flops, etc., totaling >10,000 measured standard cells demonstrating

reproducibility and robustness); typical gain is >10 with rail-to-rail output voltage swing (>99% V_{DD}). Additional fabricated and measured results are in Figures 6.3-4, 6.6-8 (for instance, Figure 6.3-4 shows measured BEOL 1T1R memory arrays fabricated across multiple vertical tiers of the monolithic 3D IC, demonstrating arbitrary layering and connectivity). As an additional demonstration, we show BEOL CNFET 10T SRAM arrays (Figure 6.7) as well as the compute core a 16-bit microprocessor (containing 1,570 logic gates, Figure 6.8). All of the above is fabricated entirely within the BEOL as described previously and designed using the flow shown in Figure 6.5.

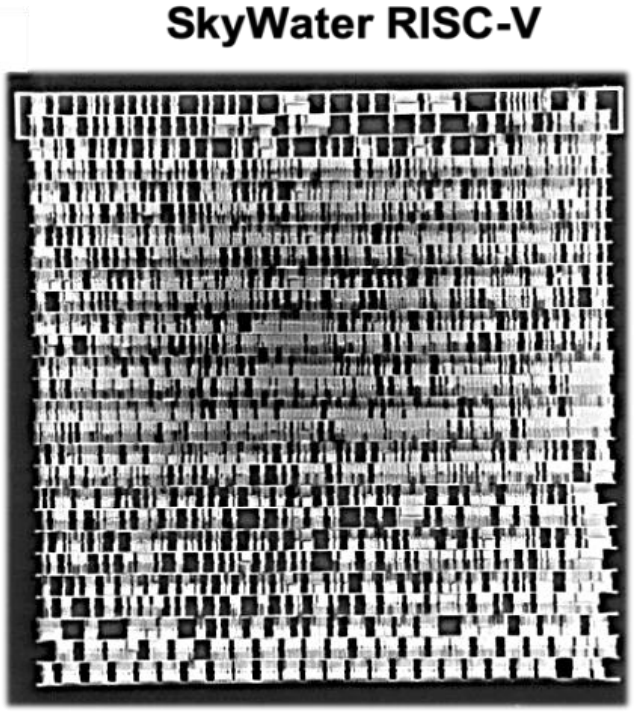


Fig. 6.8: 16-bit microprocessor, fabricated from CNFET CMOS completely in the BEOL (design flow in Figure 6.4). We confirm functionality through random test pattern generation, and compare all output bits to simulation results.

6.5 Summary

This work establishes, for the first time, heterogenous integration of logic and memory within the BEOL within a commercial foundry leveraging emerging nanotechnologies. This is enabled by

transferring a complementary CNFET technology within the foundry and developing the full VLSI processing and design flows to support this new process. This represents a promising path for next-generation nanoelectronic systems.

Chapter 7: Concluding Remarks

As physical and equivalent scaling of silicon transistors is becoming increasingly challenging, "NanoSystems" offer the ability to address many of the challenges that conventional approaches face today (such as the scaling wall, power wall and the memory wall), simultaneously promising significant benefits in computing performance and energy efficiency. Unfortunately, despite the promise of nanosystems, all nanosystem demonstrations were fabricated in academic labs, and there were many challenges that prohibited nanosystems from transferring into industry and thus into the real world.

This thesis addresses this critical problem. By demonstrating the world's first adoption of nanosystems within industry, this thesis provides both a specific path forwards as well as a general approach of how to transform promising nanosystems in theory into practical systems that can impact our daily lives. To transform nanosystems from the "lab" to the "fab", this thesis addresses challenges that span the entire stack: from low-level material optimizations, to semiconductor device engineering, to circuit and system design, up to architectures and application implementation. As a case-study, this thesis focuses on carbon nanotubes and monolithic three-dimensional integration as the specific implementation of a nanosystem, yet the lessons and conclusions from this work are applicable to a broad set of emerging nanotechnologies and nanosystems. Beyond technology, this thesis shows unequivocally that nanosystems should – and can - be transferred from academic "labs" into commercial "fabs", providing a realistic and feasible path forwards for computing to continue to improve and revolutionize the world we live in.

Appendix:

A.1: Process Flow for baseline back-gate CNFETs at MIT

Process Flow for back-gate CNFETs (with channel length >1 µm):

The starting substrate for the back-gate CNFETs is silicon (resistivity of ~100 ohm-cm) with 800 nm thermal oxide. To pattern the metal gate, the wafer is coated with a bilayer PMGI SF5 and SPR 700 photoresist (~200 nm PMGI SF5 + 1000 nm SPR), and photolithography (with a Heidelberg maskless aligner) is used to define the gate electrode. Exposed photoresist is developed at room temperature (~21 °C) using CD-26. Electron beam (ebeam) evaporation is used to deposit 20 *Å of Titanium followed by 18 nm Platinum, followed by lift-off. Atomic layer deposition (ALD) is used to deposit 10nm* Al_2O_3 *followed by 10nm* HfO_2 *over the gate metal at 200 C.* Following gate-stack fabrication, photolithography is performed using positive photoresist SPR to pattern contact holes to the gate metal electrodes, and a dry Cl_2-based plasma etch is used to etch through the HfO_2. The SPR is stripped in CD-26 followed by oxygen plasma. To prepare the wafer for CNT deposition, the surface is functionalized with hexamethyldisilazane (HMDS). The wafer is then submerged in s-CNT solutions of toluene (CNT incubation[31]) containing >99.9% pure semiconducting CNTs (modified Nanointegris[36] and NRC supplied sCNT solutions) for 48 hours. To make the deposition uniform and reproducible we use a CNT concentration of 2 µg ml^{-1} for our deposition. After CNT incubation we perform a solvent cleaning step (coat pieces in PMGI SF5, bake at 235 C and sonicate pieces in NMP) to remove CNT aggregates from the surface of the die (RINSE[1]). After RINSE, SPR is patterned to cover the transistor channel regions, and oxygen plasma removes all excess CNTs (outside the channel region). Finally, the source and drain (5 *Å Ti*/ 45 nm Pt) are defined and patterned similar as the gate electrode.

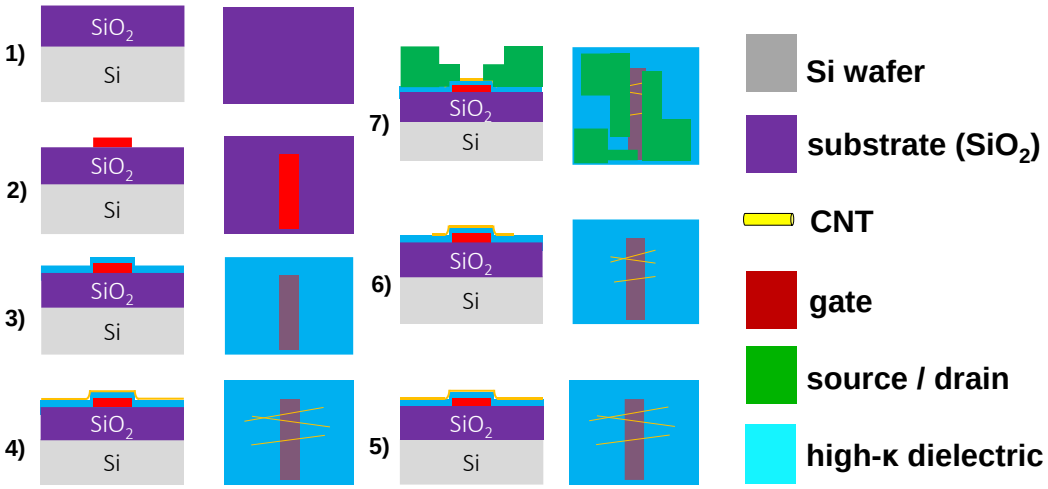


Fig. A1.1: Process flow of back-gate CNFETs. (1) Si/SiO_2 substrate. (2) photo lithography patterning, e-beam metal evaporation and liftoff for back-gate (2 nm Ti/ 18 nm Pt). (3) 15nm Al_2O_3 15 nm HfO_2 gate dielectric (eot ≈ 7.5 nm). (4) Submerge die in purified semiconducting CNTs dispersed in toluene. (5) Die Clean through NMP solvent rinse. (6) oxygen plasma etch to remove CNTs outside of transistor channel region. (7) source/drain patterning through photo lithography patterning, e-beam metal deposition and liftoff (0.5 nm Ti/ 45 nm Pt).

Table A1.1 Process flow for back-gate CNFETs at MIT (with channel length >1 µm)

Process Name and No.	Process Step	Machine Used
1. Lithography for Local Back Gate	a. HMDS Bake (10 sec program)	HMDS-TRL
	b. Spin PMGI SF5 and bake at 235C	TRL Coater and hotplates 1/2
	c. Spin SPR 700 and bake at 90 C	TRL Coater and hotplates 1/2
	d. Expose with Maskless Aligner or iStepper	MLA 150 TRL or iStepper in ICL
	e. Post Exposure Bake 115C	Developer Brewer Vacuum Hot Plate TRL
	f. develop for 70s	Developer Brewer TRL
	g. quick O_2 plasma descum	TRL Asher
2. Deposit Gate contact metal	1 nm Titanium (for adhesion), 20 nm platinum	EBEAM-AU Temescal Model VES2550 TRL
3. Lift Off	a. Sonicate in Acetone beaker for 1.5 minutes, b. Transfer new Acetone beaker and sonicate again for 1.5 minutes c. Rinse with IPA d. Sonicate in NMP for 15 minutes at 60 C e. rinse with IPA then immerse wafer in IPA beaker for 1.5 minutes	Solvent Bench Au
4. ALD HfO_2 Gate Dielectric	ALD 200 degrees (inner chamber) 15nm oxide	ALD (Cambridge Nanotech) ICL
5. Characterize film thickness	**Measure HfO2 film thickness**	**TRL Ellipsometer**
6. Lithography for Oxide Etch Vias	a. HMDS Bake (10 sec program)	HMDS-TRL
	b. Spin SPR 700 and Bake at 90 C	TRL Coater and hotplates 1/2
	c. Expose with Maskless Aligner	MLA 150 TRL or iStepper in ICL
	d. Post Exposure Bake (standard bake times)	Developer Brewer Vacuum Hot Plate TRL
	e. Develop with CD 26 for 70 sec	Developer Brewer TRL
7. Etch Oxide for vias	Etch HfO_2 (15nm) stop on metal (CHLORINE Based Etch)	Samco (TRL)
8. Strip PR	a. Sonicate in Acetone beaker for 10 minutes, b. Rinse with IPA c. Sonicate in NMP for 15 minutes at 60 C d. rinse with IPA then immerse wafer in IPA beaker for 1.5 minutes	Solvent Bench Au
9. Check etching depth	Measure via depth with AFM	AFM in ICL

10. Surface Descum	Active O_2 plasma for surface cleaning	TRL Matrix Asher
11. Deposit CNTs	a. Solution based CNT deposition	CNT incubator (Teflon containers) in Shulaker Lab
	b. Anneal at 500 C for 5 mins 10^-6 Torr	Shulaker Lab vacuum furnace
12. Lithography for CNT Active Etch (Etch away CNTs from unwanted regions)	a. HMDS Bake (10 sec program)	HMDS-TRL
	b. Spin SPR 700 and bake at 90 C	TRL Coater and hotplates 1/2
	c. Expose with Maskless Aligner or iStepper	MLA 150 TRL or iStepper in ICL
	d. Post Exposure Bake 115C	Developer Brewer Vacuum Hot Plate TRL
	e. develop in CD-26 for 70s	Developer Brewer TRL
13. Etch away CNTs	Quick O_2 Plasma Descum	Asher TRL
14. Strip PR	a. Sonicate in Acetone beaker for 10 minutes, b. Rinse with IPA c. Sonicate in NMP for 15 minutes at 60 C d. rinse with IPA then immerse wafer in IPA beaker for 1.5 minutes	Solvent Bench Au
15. Lithography for S/D contacts for PMOS	a. HMDS Bake (10 sec program)	HMDS-TRL
	b. Spin PMGI SF5 and bake at 235C	TRL Coater and hotplates 1/2
	c. Spin SPR 700 and bake at 90 C	TRL Coater and hotplates 1/2
	d. Expose with Maskless Aligner or iStepper	MLA 150 TRL or iStepper in ICL
	e. Post Exposure Bake 115C	Developer Brewer Vacuum Hot Plate TRL
	f. develop for 70s	Developer Brewer TRL
16. Deposit S/D contact metal for PMOS	0.5 nm Titanium (for adhesion), 40 nm platinum	EBEAM-AU Temescal Model VES2550 TRL
17. Lift Off	a. Sonicate in Acetone beaker for 1.5 minutes, b. Transfer new Acetone beaker and sonicate again for 1.5 minutes c. Rinse with IPA d. Sonicate in NMP for 15 minutes at 60 C e. rinse with IPA then immerse wafer in IPA beaker for 1.5 minutes	Solvent Bench Au

Process Flow for back-gate CNFETs (with channel length <1 µm):

The starting substrate for the back-gate CNFETs is silicon (resistivity of ~100 ohm-cm) with 800 nm thermal oxide. To pattern the metal gate, the wafer is coated with a single layer PMMA positive photoresist (~200 nm 495k PMMA A4), and electron-beam (ebeam) lithography is used to define the gate electrode. PMMA is patterned with room temperature development at 21 °C using 3:1 IPA:MIBK. Electron beam (ebeam) evaporation is used to deposit 10 *Å of Titantium followed by 15 nm Platinum, followed by lift-off. The area dose for e-beam lithography is carefully optimized by simulating the electron back-scattering effects in a stack of PMMA-SiO_2 and PMMA-HfO_2 in TRACER. Atomic layer deposition (ALD) is used to deposit 10nm HfO_2 over the gate metal.* Following gate-stack fabrication, photolithography with Maskless Aligner (MLA) is done using positive photoresist SPR to pattern contact holes to the gate metal electrodes, and a dry Cl_2-based plasma etch is used to etch through the HfO_2. The SPR is stripped in remover 1165 followed by oxygen plasma. To prepare the wafer for CNT deposition, the surface is functionalized with hexamethyldisilazane (HMDS, a common photoresist adhesion promoter). The wafer is then submerged in a solution of toluene containing >99.9% pure semiconducting CNTs (Nanointegris supplied IsoSol-S100) for 10 hours. To disperse CNTs in toluene, the CNTs go through several sonication steps to wrap the CNTs in a polymer to disperse them within the toluene, followed by several ultracentrifugation steps to remove non-dispersed CNTs and excess polymer. The source and drain are defined and patterned similar as the gate electrode. A last photo lithography step using bilayer resist (SPR+PMGI SF5 lift off layer), ebeam evaporation, and lift-off is performed to define larger probe pads and interconnect wires. After CNFET fabrication, SPR is patterned to

cover the transistor channel regions, and oxygen plasma removes all excess CNTs (*e.g.*, CNTs outside of the transistor channel region, and therefore not protected by the SPR).

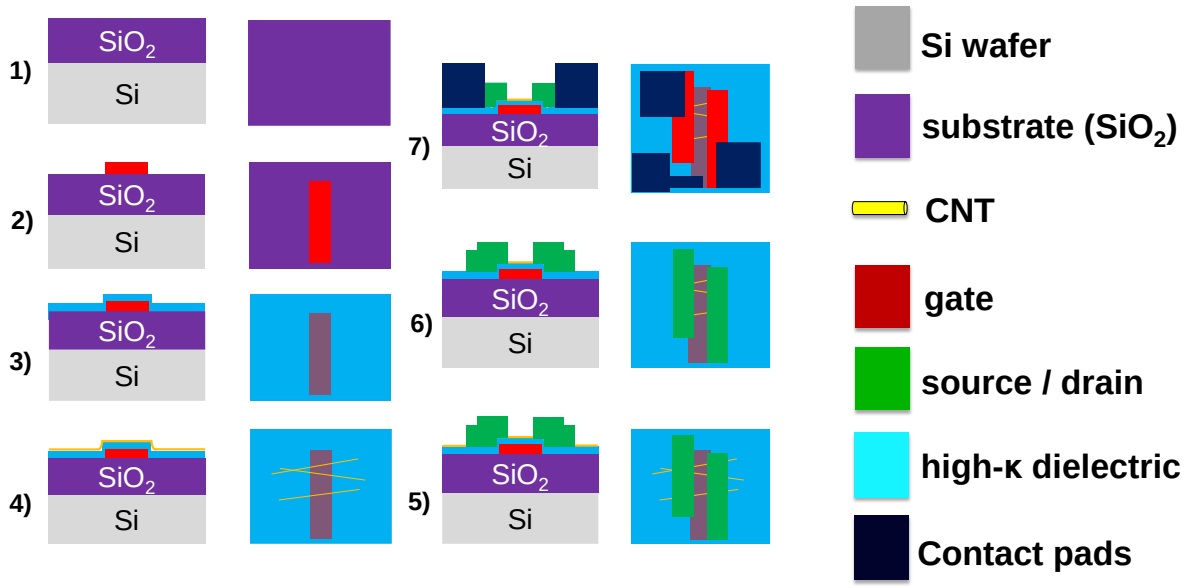


Fig. A1.2. Process flow of scaled back-gate CNFETs. (1) Si/SiO_2 substrate. (2) electron-beam(e-beam) lithography patterning, e-beam metal evaporation and liftoff for back-gate (1 nm Ti/ 15 nm Pt). (3) 10 nm HfO_2 gate dielectric (eot ≈ 2.5 nm). (4) Submerge die in purified >99.9% pure semiconducting CNTs dispersed in toluene solution. (5) source/drain patterning through e-beam lithography patterning, e-beam metal deposition and liftoff (1 nm Ti/ 25 nm Pt). (6) oxygen plasma etch to remove CNTs outside of transistor channel region. (7) probe pad deposition defined through photolithography (maskless aligner), e-beam metal evaporation and liftoff (10 nm Ti/ 40 nm Pt).

The starting substrate for the back-gate 30 nm CGP CNFETs are silicon substrates (resistivity of ~100 ohm-cm) with 800 nm thermal oxide. To pattern the metal gate, the wafer is coated with a single layer PMMA positive photoresist (~45 nm PMMA A1), and electron-beam (ebeam) lithography is used to define the gate electrode (L_G ~18 nm). PMMA is patterned with cold development at -3.5 °C. Electron beam (ebeam) evaporation is used to deposit 3 Å of Titantium followed by 4 nm Platinum, followed by lift-off in heated 1-methyl pyrrolidone at 60 C

in a water bath. The area dose for e-beam lithography is carefully optimized by simulating the electron back-scattering effects in a stack of PMMA-SiO_2 and PMMA-HfO_2 in TRACER[26]. Following gate-stack fabrication, PMMA and ebeam lithography is again used to pattern contact holes to the gate metal electrodes, and a dry Cl_2-based plasma etch is used to etch through the HfO_2. The PMMA is stripped in hot acetone followed by oxygen plasma. To prepare the wafer for CNT deposition, the surface is functionalized with HMDS. The wafer is then submerged in a solution of 1,2-Dichloroethane (DCE) containing >99.9% pure semiconducting CNTs for 10 minutes. To disperse CNTs in DCE, the CNTs go through several sonication steps to wrap the CNTs in a polymer to disperse them within the DCE, followed by several ultracentrifugation steps to remove non-dispersed CNTs and excess polymer. Following CNT deposition, the wafer is rinsed in hot Toluene for 60 minutes, followed by vacuum annealing at $<10^{-5}$ Torr for >30 minutes. The source and drain are defined and patterned similar as the gate electrode, but are done in two separate steps to increase minimum resolution. A last ebeam lithography step, ebeam evaporation, and lift-off is performed to define larger probe pads and interconnect wires. After CNFET fabrication, PMMA is patterned to cover the transistor channel regions, and oxygen plasma removes all excess CNTs (*e.g.*, CNTs outside of the transistor channel region, and therefore not protected by the PMMA).

Table A1.2 Process flow for scaled back-gate CNFETs at MIT

Process Name and No.	Process Step	Machine Used
1. Cleaning Si Wafer	RCA clean	RCA clean (SC1 + SC2) TRL
2. SiO_2 Growth	500nm thermal oxide	Furnaces – MRL Industries Model 718 system- TRL A1 GateOx
3.Lithography for Local Back Gate with lift off	a. Spin 40nm 950k PMMA A1 and bake (for 30nm CGP FET); 495k PMMA A4 200nm for higher technology nodes	TRL Coater and hotplates 1/2
	b. E-beam lithography – 3KeV Aperture 10 um Area Dose = 600 uC/cm.^2 Line Dose – 1.4 – 3.0 nC/cm (or vary current in pA regime for getting small features)	Elionix FS-125
	c. Cold Development -15 C IPA:MIPK – 1:3 5s and 15s IPA rinse and nitrogen dry for scaled nodes/ room temperature 90s development using IPA:MIBK for higher technology nodes	Solvent Bench Au, and hotplate TRL
	d. Quick O2 plasma/ Forming Gas Anneal	Matrix Asher 106/ Tube B1 TRL
4. Deposit Gate contact metal	0.3 nm Titanium (for adhesion), 4 nm platinum (for 30nm CGP) FET) 1 nm Ti/ 15 nm Pt for higher nodes.	EBEAM-AU Temescal Model VES2550 TRL
5. Lift Off	a. First, soak in acetone until all lift-off complete. Without letting it dry, move it quickly into IPA for a minute, then take out and dry. Check under microscope to make sure lift-off is complete.	Solvent Bench Au
6. ALD Al_2O_x/ high-K dielectric	ALD 200 degrees 5 nm oxide	Cambridge Nanotech ICL
7. Etch for contact holes	a. HMDS coat	TRL HMDS coater
	b. Spin PR and bake	TRL Coater and hotplates 1/2
	c. E-beam lithography	Elionix FS-125
	d. Develop PMMA room temp and descum entire wafer(1 minute low temp O_2 Plasma/ forming gas anneal)	Solvent Bench Au and O2 plasma in Matrix 106 Asher/ Tube B1 TRL

	e. Etch contact holes through oxide using Cl_2/BCl_3 etch stop on metal and quick HF dip	Oxford-100 TRL/ RCA station for HF dip TRL
8. Surface Descum	Active O_2 plasma for surface cleaning	
9. CNT deposition	Substrate taken to Shulaker lab for solution based deposition of CNTs (99.9% isosol-100 from nanointegris)	Chemical hood, Shulaker lab
10. Lithography for S/D contacts with lift off	a. Spin 40nm 950k PMMA A1 and bake (for 30nm CGP FET); 495k PMMA A4 200nm for higher nodes	TRL Coater and hotplates 1/2
	b. E-beam lithography	Elionix FS-125
	c. Cold Development -15 C IPA:MIPK – 1:3 5s and 15s IPA rinse and nitrogen dry	Solvent Bench Au, and hotplate TRL
11. Deposit S/D contact metal	1 nm Ti and 8 nm Pt for scaled node and 1 nm Ti / 25 nm Pt for higher nodes	EBEAM-AU Temescal Model VES2550 TRL
12. Lift Off	First, soak in acetone until all lift-off complete. Without letting it dry, move it quickly into IPA for a minute, then take out and dry. Check under microscope to make sure lift-off is complete. If finished, put in solvent to remove the lift-off layer	Solvent Bench Au
13. Pattern Active Region	a. Prep Wafer with HMDS	HMDS coater TRL
	b. Spin on PMMA and Bake	TRL PR coater hotplates 1/2
	c. Ebeam exposure	Elionix FS-125
	d. Develop room temp.	Solvent Bench Au
	e. quick O_2 plasma descum/ forming gas anneal	Matrix Asher 106/ Tube B1 TRL
	f. Strip PR in strong solvent	Solvent Bench Au TRL

A.2: CNFET CMOS Process Flow

Process Flow for CMOS back-gate CNFETs:

The baseline CNFET CMOS process at MIT (Table A2.1) uses the same underlying back-gate CNFET process (Table A1.2) and then uses a conjunction of contact metal work function engineering and electrostatic doping to achieve symmetric p and n type transistors [Lau 2018]. Contact work function engineering involves a high work function metal Platinum for PMOS and low work function metal Titanium for NMOS. Finally, to finely control the threshold voltage (V_{TH}), different encapsulating oxides are used to electrostatically dope the transistors. Typically, we use evaporated non-stoichiometric silicon oxide (SiO_X) for PMOS and ALD deposited non-stoichiometric hafnium oxide (HfO_X) for NMOS. Finally, we use a back-end dielectric encapsulation (PECVD Silicon Nitride and TEOS) to protect the devices from humidity.

Skywater Technology Foundries uses this CMOS process with a few modifications -

a) Local Bottom Gates or Back Gates are embedded back-gates made using W CVD fill and CMP.

b) Gate dielectric comprises of a high-k dielectric which is primarily hafnium oxide.

c) CNT deposition process is done in a Si CMOS foundry compatible manner in a custom built high-throughput CNT deposition tool [Bishop 2020]

d) A commercial Si CMOS compatible back-end-of-line dielectric is used to encapsulate the CNTs after deposition of passivation and doping oxides.

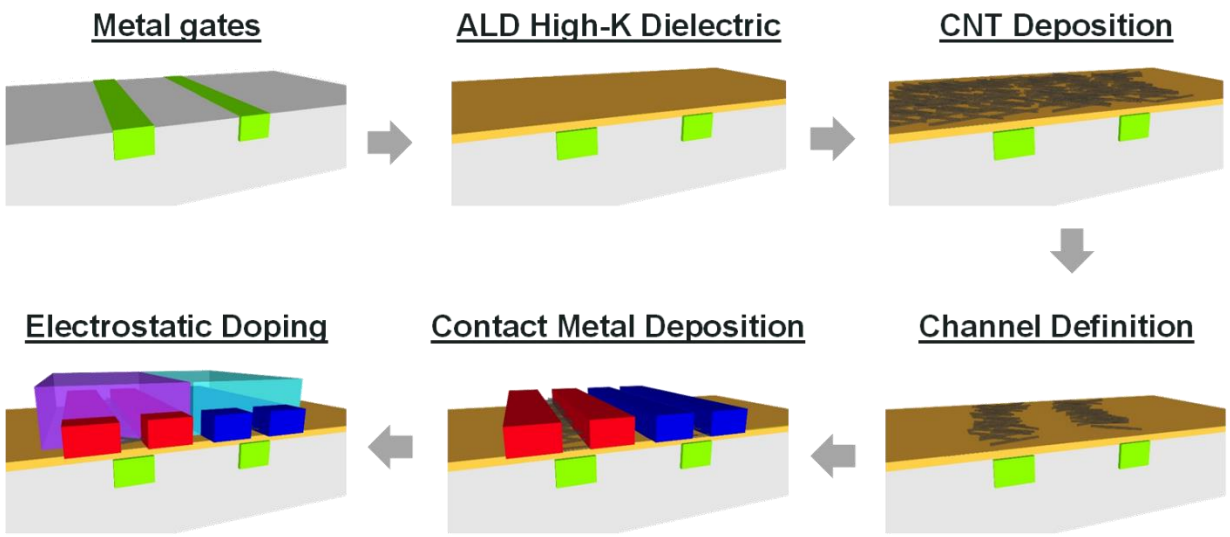


Figure A2.1: CMOS CNFET process flow. The process follows the baseline back-gate CNFET process with contact work function engineering for PMOS and NMOS and then using different encapsulating oxides for finely tuning the threshold voltage of the PMOS and NMOS transistors.

Electrical Characterization of CMOS CNFET inverters:

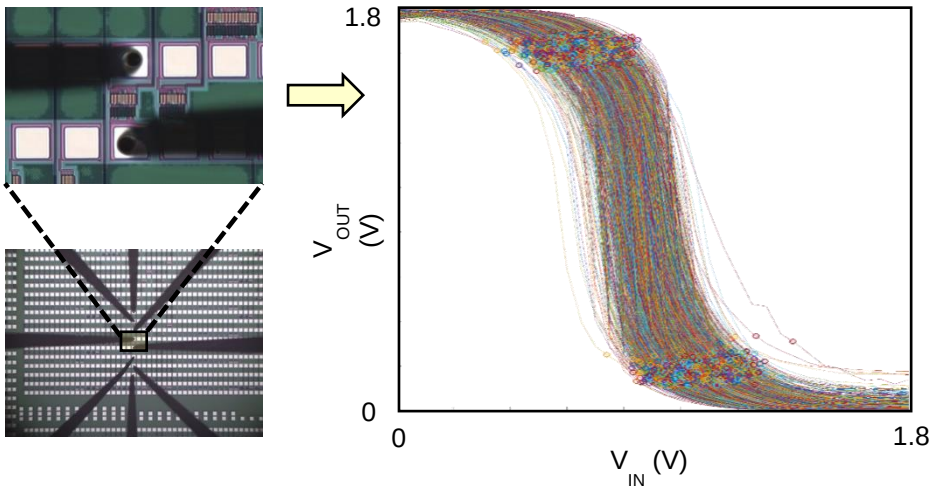


Figure A2.2: Electrical characterization of CMOS inverters, fabricated using a 130 nm CNFET CMOS process. Sample size is 1000 inverters measured from different dies spanning an entire 200 mm wafer, showing uniformity of the CNFET CMOS process.

Table A2.1 Process flow for CMOS back-gate CNFETs at MIT*

Process Name and No.	Process Step	Machine Used
1. Lithography for Local Back Gate	a. HMDS Bake (10 sec program)	HMDS-TRL
	b. Spin PMGI SF5 and bake at 235C	TRL Coater and hotplates 1/2
	c. Spin SPR 700 and bake at 90 C	TRL Coater and hotplates 1/2
	d. Expose with Maskless Aligner or iStepper	MLA 150 TRL or iStepper in ICL
	e. Post Exposure Bake 115C	Developer Brewer Vacuum Hot Plate TRL
	f. develop for 70s	Developer Brewer TRL
	g. quick O_2 plasma descum	TRL Asher
2. Deposit Gate contact metal	1 nm Titanium (for adhesion), 20 nm platinum	EBEAM-AU Temescal Model VES2550 TRL
3. Lift Off	a. Sonicate in Acetone beaker for 1.5 minutes, b. Transfer new Acetone beaker and sonicate again for 1.5 minutes c. Rinse with IPA d. Sonicate in NMP for 15 minutes at 60 C e. rinse with IPA then immerse wafer in IPA beaker for 1.5 minutes	Solvent Bench Au
4. ALD HfO_2 Gate Dielectric	ALD 200 degrees (inner chamber) 15nm oxide	ALD (Cambridge Nanotech) ICL
5. Characterize film thickness	**Measure HfO2 film thickness**	**TRL Ellipsometer**
6. Lithography for Oxide Etch Vias	a. HMDS Bake (10 sec program)	HMDS-TRL
	b. Spin SPR 700 and Bake at 90 C	TRL Coater and hotplates 1/2
	c. Expose with Maskless Aligner	MLA 150 TRL or iStepper in ICL
	d. Post Exposure Bake (standard bake times)	Developer Brewer Vacuum Hot Plate TRL
	e. Develop with CD 26 for 70 sec	Developer Brewer TRL
7. Etch Oxide for vias	Etch HfO_2 (15nm) stop on metal (CHLORINE Based Etch)	Samco (TRL)
8. Strip PR	a. Sonicate in Acetone beaker for 10 minutes, b. Rinse with IPA c. Sonicate in NMP for 15 minutes at 60 C d. rinse with IPA then immerse wafer in IPA beaker for 1.5 minutes	Solvent Bench Au

9. Check etching depth	Measure via depth with AFM	AFM in ICL
10. Surface Descum	Active O_2 plasma for surface cleaning	TRL Matrix Asher
11. Deposit CNTs	a. Solution based CNT deposition	CNT incubator (Teflon containers) in Shulaker Lab
	b. Anneal at 500 C for 5 mins 10^-6 Torr	Shulaker Lab vacuum furnace
12. Lithography for CNT Active Etch (Etch away CNTs from unwanted regions)	a. HMDS Bake (10 sec program)	HMDS-TRL
	b. Spin SPR 700 and bake at 90 C	TRL Coater and hotplates 1/2
	c. Expose with Maskless Aligner or iStepper	MLA 150 TRL or iStepper in ICL
	d. Post Exposure Bake 115C	Developer Brewer Vacuum Hot Plate TRL
	e. develop in CD-26 for 70s	Developer Brewer TRL
13. Etch away CNTs	Quick O_2 Plasma Descum	Asher TRL
14. Strip PR	a. Sonicate in Acetone beaker for 10 minutes, b. Rinse with IPA c. Sonicate in NMP for 15 minutes at 60 C d. rinse with IPA then immerse wafer in IPA beaker for 1.5 minutes	Solvent Bench Au
15. Lithography for S/D contacts for PMOS	a. HMDS Bake (10 sec program)	HMDS-TRL
	b. Spin PMGI SF5 and bake at 235C	TRL Coater and hotplates 1/2
	c. Spin SPR 700 and bake at 90 C	TRL Coater and hotplates 1/2
	d. Expose with Maskless Aligner or iStepper	MLA 150 TRL or iStepper in ICL
	e. Post Exposure Bake 115C	Developer Brewer Vacuum Hot Plate TRL
	f. develop for 70s	Developer Brewer TRL
16. Deposit S/D contact metal for PMOS	0.5 nm Titanium (for adhesion), 40 nm platinum	EBEAM-AU Temescal Model VES2550 TRL
17. Lift Off	a. Sonicate in Acetone beaker for 1.5 minutes, b. Transfer new Acetone beaker and sonicate again for 1.5 minutes c. Rinse with IPA d. Sonicate in NMP for 15 minutes at 60 C e. rinse with IPA then immerse wafer in IPA beaker for 1.5 minutes	Solvent Bench Au
18. Lithography for passivation layer	a. HMDS Bake (10 sec program)	HMDS-TRL

	b. Spin PMGI SF5 and bake at 235C	TRL Coater and hotplates 1/2
	c. Spin SPR 700 and bake at 90 C	TRL Coater and hotplates 1/2
	d. Expose with Maskless Aligner or iStepper	MLA 150 TRL or iStepper in ICL
	e. Post Exposure Bake 115C	Developer Brewer Vacuum Hot Plate TRL
	f. develop for 70s	Developer Brewer TRL
19. Deposit passivation layer	Deposit 40 nm SiO_2	EBEAM-AU Temescal Model VES2550 TRL
20. Lift Off	a. Sonicate in Acetone beaker for 1.5 minutes, b. Transfer new Acetone beaker and sonicate again for 1.5 minutes c. Rinse with IPA d. Sonicate in NMP for 15 minutes at 60 C e. rinse with IPA then immerse wafer in IPA beaker for 1.5 minutes	Solvent Bench Au
21. Lithography for S/D contacts for NMOS	a. HMDS Bake (10 sec program)	HMDS-TRL
	b. Spin PMGI SF5 and bake at 235C	TRL Coater and hotplates 1/2
	c. Spin SPR 700 and bake at 90 C	TRL Coater and hotplates 1/2
	d. Expose with Maskless Aligner or iStepper	MLA 150 TRL or iStepper in ICL
	e. Post Exposure Bake 115C	Developer Brewer Vacuum Hot Plate TRL
	f. develop for 70s	Developer Brewer TRL
22. Deposit S/D contact metal for PMOS	40 nm Titanium (for adhesion)	EBEAM-AU Temescal Model VES2550 TRL
23. Lift Off	a. Sonicate in Acetone beaker for 1.5 minutes, b. Transfer new Acetone beaker and sonicate again for 1.5 minutes c. Rinse with IPA d. Sonicate in NMP for 15 minutes at 60 C e. rinse with IPA then immerse wafer in IPA beaker for 1.5 minutes	Solvent Bench Au
24. ALD HfO_2 for NMOS doping layer	ALD 250 degrees 30 nm HfO_2	Cambridge Nanotech ICL
25. Lithography for probing pad contact holes	a. HMDS Bake (10 sec program)	HMDS-TRL

	b. Spin SPR700 and Bake at 90 C	TRL Coater and hotplates 1/2
	c. Expose with Maskless Aligner	MLA 150 TRL or iStepper in ICL
	d. Post Exposure Bake (standard bake times)	Developer Brewer Vacuum Hot Plate TRL
	e. Develop with CD26 for 70 sec	Developer Brewer TRL
26. RIE Etch for pad contact holes	f. Etch HfO_2 and Al_2O_3 in exposed region. Stop etch on metal (CHLORINE Based Etch)	TRL Oxford 100
27. Strip PR	a. Sonicate in Acetone beaker for 10 minutes, b. Rinse with IPA	Solvent Bench Au
28. Deposit SiN protective layer	Deposit 200 nm SiN followed by PECVD at 250C	ICL Oxford 100 PECVD
29. Deposit TEOS spacer	Deposit 400 nm of TEOS spacer 250 C	ICL Oxford 100 PECVD
30. Lithography for contact holes / SiN + TEOS etch	a. HMDS Bake (10 sec program)	HMDS-TRL
	b. Spin SPR700 and Bake at 90 C	TRL Coater and hotplates 1/2
	c. Expose with Maskless Aligner	MLA 150 TRL or iStepper in ICL
	d. Post Exposure Bake (standard bake times)	Developer Brewer Vacuum Hot Plate TRL
	e. Develop with CD26 for 70 sec	Developer Brewer TRL
31. Etch contact holes through SiN + TEOS	$CF_4 + O_2$ etch	ICL Oxford 100 RIE
32. Strip PR	a. Sonicate in Acetone in a beaker for 10 minutes b. Rinse with IPA and blow dry	Solvent Bench Au

* Skywater Technology Foundry uses the same CMOS process, with a few changes as listed in the paragraph above the table.

A.3: Physical Design Flow for EDP analysis

The physical design flow for VLSI circuits is as follows. We quantify circuit-level performance metrics for physical designs for each VLSI-scale circuit module (*i.e.*, from the OpenSparc T2 processor core and for the 32 bit commercial processor core) at the 5 nm node (details in Table S1) across multiple device-level performance metrics, including (but not limited to): supply voltage (V_{DD} = 375 mV to 500 mV), sub-threshold slope (*SS*) degradation (from 0% to 25%), and accounting for CNFET-level parasitics using a commercially-available 3D field solver [TCAD Sentaurus] and interconnect simulator [Raphael] to model extrinsic elements based on the CNFET geometry and material properties (*e.g.*, on the dimensions and resistivity of the source/drain metal contact plugs). For each combination of parameters (*e.g.*, for each V_{DD}, *SS*, top-gate vs. bottom-gate), we perform the following design flow to quantify relative EDP (*e.g.*, as in Fig. 7) for all VLSI circuit modules:

1. *Standard cell library characterization*: using standard cell layouts (derived from the 15 nm node Nangate Open Cell Library [Nangate]) are used to extract standard cell parasitics, and then the extracted netlists are used in conjunction with the experimentally calibrated compact transistor models [Lee 2015] to characterize power and timing (using Cadence Spectre [Spectre]) for each standard library cell

2. *Synthesis*: using Synopsys Design Compiler [Design Compiler], synthesize each circuit module over a range of target clock frequencies (from 1 GHz to 10 GHz), since operating clock frequency after optimizing circuit EDP can vary depending on the device-level parameters (*e.g.*, V_{DD}).

3. *Placement & routing*: using Synopsys IC Compiler [IC Compiler], perform placement & routing for each synthesized netlist (for each target frequency), allowing for physical circuit optimization such as buffer insertion to meet circuit timing constraints.

4. *Power/timing analysis*: perform power and timing analysis for each physical design (using Synopsys PrimeTime [PrimeTime]) placed & routed above, over several *retargeted* clock frequencies spanning the range from 0.1 GHz up to 10 GHz in 0.1 GHz increments (*i.e.*, readjust the timing constraints in steps 2 and 3 targeting a different clock frequency), since it is potentially more energy efficient to operate at a separate clock frequency than that was specified during synthesis and place & route.

A.4: Non-self-aligned back-gate CNFET

The back-gate structure is not a self-aligned structure. Therefore, the back-gate may be misaligned to the source and drain contacts. This misalignment can lead to increased parasitic capacitances. To analyze the effect of the overlay misalignment, we extract the capacitance of a CNFET with a 30 nm CGP, assuming different overlay misalignment (Figure A3.1a). Given a 6 nm overlay inaccuracy between the gate and source and drain contacts, the input capacitance of the CNFET changes by only <12% (Figure A3.1b).

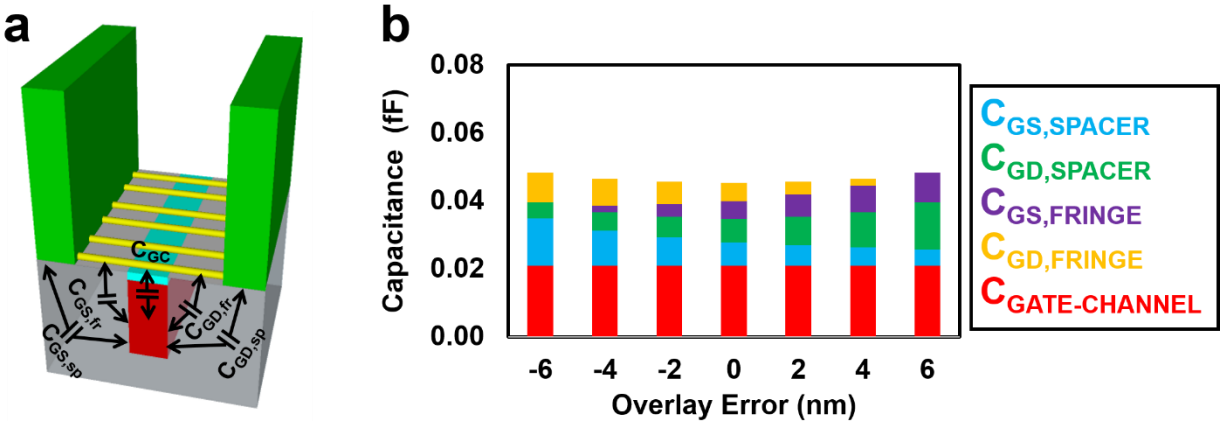


Fig. A4.1: (a) Schematic of back-gate CNFET, with labelled input capacitances. (b) The input capacitance of a CNFET changes by <12% given a 6 nm mis-alignment inaccuracy in either direction (for a highly-scaled 30 nm CGP CNFET).

A.5: Additional considerations for designing asymmetric back-gate CNFETs

Figure A4.1 shows the average reduction in I_{OFF} across multiple CNFETs, for a given L_{SP} (sample size: 30 CNFETs). All CNFETs have 180 nm channel length.

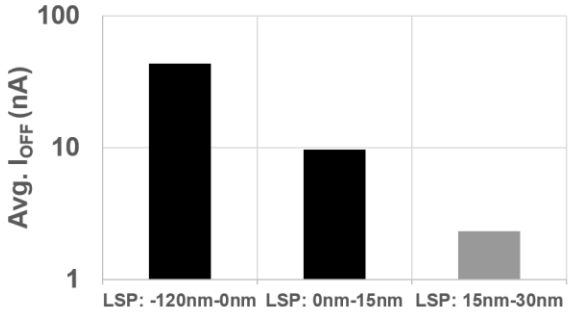


Fig. A5.1. Averaged I_{OFF} with varying L_{SP} (defined in Figure 1a), sample size = 30 CNFETs.

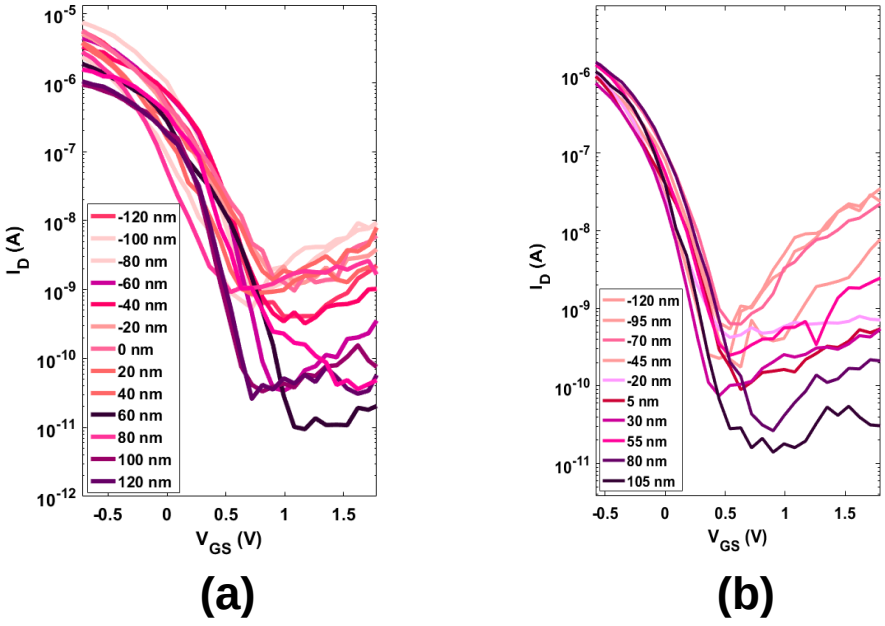


Fig. A5.2. Experimental I_D-V_{GS} characteristics for CNFETs with L_{CH} of 500nm (a) and 1µm (b), sweeping over more detailed L_{SP}.

To solve for the electrical transport in CNFETs and intrinsic parasitic capacitances, simulations are performed with TCAD Sentaurus. Devices parameters used for these simulations are listed in Table 3.2 For I-V transport simulation, CNFET is approximated as a 2D MOSFET with an extremely thin semiconductor (t = 2 nm) defining the CNT channel (with CNT material properties as reported in virtual-source CNFET compact model [Lee 2015]). Platinum is used to define the source, drain and gate electrode and HfO_2 is used to define the gate dielectric. For the sentaurus device model defining the device transport physics we use simple Hurkx tunneling model which calculates tunneling current using WKB approximation. For the capacitance simulation, quasistationary coupled poisson electron and hole equations are solved for a small applied ac voltage and lumped capacitances C_G and C_D (defined in Figure 3.5b, equations 1-2) is extracted as dQ_G/dV_G and dQ_D/dV_G respectively.

A.6: Gate-Induced Drain Leakage (GIDL)

In MOSFETs, gate-induced drain leakage mainly originates from band-to-band tunneling (BTBT) near the gate-drain overlap region, at large gate-to-drain bias. When high voltage is applied even when the transistor is off (V_{GS}<0 for a NMOSFET & V_{GS} >0 for a PMOSFET), a deep-depletion region is formed in the gate/drain overlap region (Fig. A5.1a). Thus valence band electrons tunnel to the conduction band through BTBT (for NMOS, Fig. A5.1b, for PMOS electrons tunnel from conduction band to valence band, Fig. A6.1c). Thus, electron-hole pairs generated through BTBT are collected by the drain and substrate separately, increasing the leakage current. From tunneling current models [Chan 1987], GIDL-induced current can be represented as:

$$I_{D,GIDL} = AE_S e^{\frac{B}{E_S}} \quad \text{.....} \textit{(eq. A6.1)}$$

A and *B* are constants, E_S is vertical electric field at the channel surface (in the overlap region), $E_S = \frac{V_{DG}-C}{3T_{OX}}$, *C* is a constant., T_{OX} is the oxide thickness, V_{DG} is the gate-to-drain bias voltage

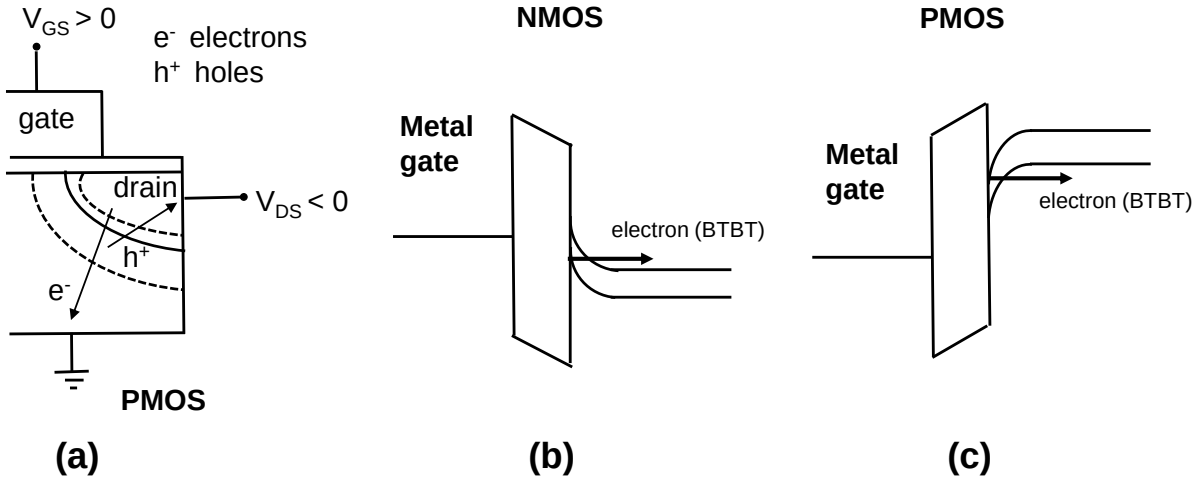


Fig. A6.1: a. formation of deep-depletion region in PMOSFET at off-state (V_{GS} > 0), showing tunneling of electrons to the substrate, increasing the leakage current. b-c. band diagrams of NMOS and PMOS at off-state showing band-to-band tunneling of electrons causing GIDL.

Possible means to reduce this GIDL-induced current relies on reduction of E_S (evident from equation A6.1). MOSFETs with relaxed access regions or undoped spacer regions can limit this electric-field near the gate-drain overlap region, suppressing excess GIDL-induced current (Fig. A6.2).

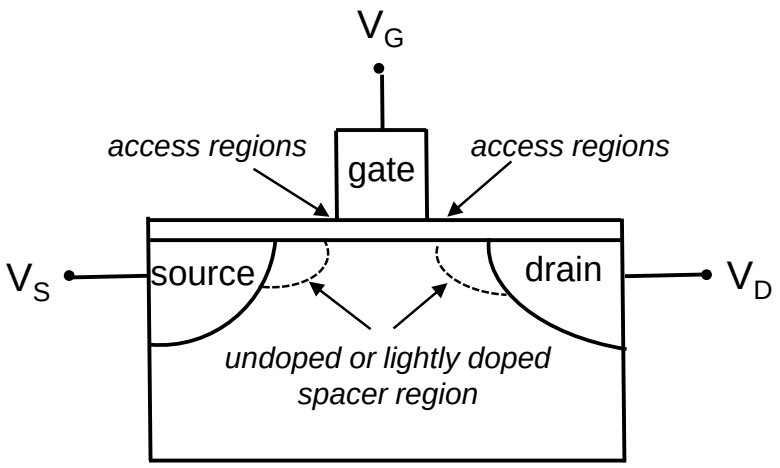


Fig. A6.2: FETs with long access regions (or, extension regions) or undoped/lightly doped spacer regions limit the high electric field near the gate/drain overlap region and are used to overcome GIDL-induced leakage current.

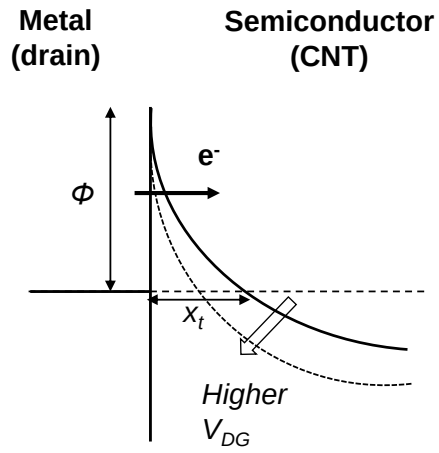


Fig. A6.3: Band diagram of the Schottky barrier near the gate/drain overlap region. Increasing gate-to-drain bias (V_{DG}) decreases schottky barrier tunneling width (x_t) increasing tunneling of electrons across the schottky barrier, causing excess off-state leakage current.

In a schottky-barrier FETs, high gate-to-drain bias induces band bending (Fig. A6.3 , equation A6.2) in the drain metal-semiconductor schottky barrier near the gate/drain overlap region, causing electrons to tunnel from the metal contact to the semiconducting channel leading to excess off-state leakage current.

Tunneling probability across a schottky barrier [Calvet 2001] can be mathematically expressed as (equation A6.2):

$$P = \exp\left(-\frac{4\sqrt{2m^{*}q}\,(\Phi)^{3/2}}{3hE}\right)$$ .....(equation A6.2)

where,

E = vertical electric field across the schottky barrier E is proportional to gate-drain bias voltage near the gate/drain overlap region (thus, higher V_{DG} exponentially increases the tunneling probability of electrons across the schottky barrier causing excess off-state leakage current),

h = reduced Planck's constant,

m* = electron effective mass,

q = charge of electron,

Φ= schottky barrier height

A.7: CNFET leakage temperature dependence

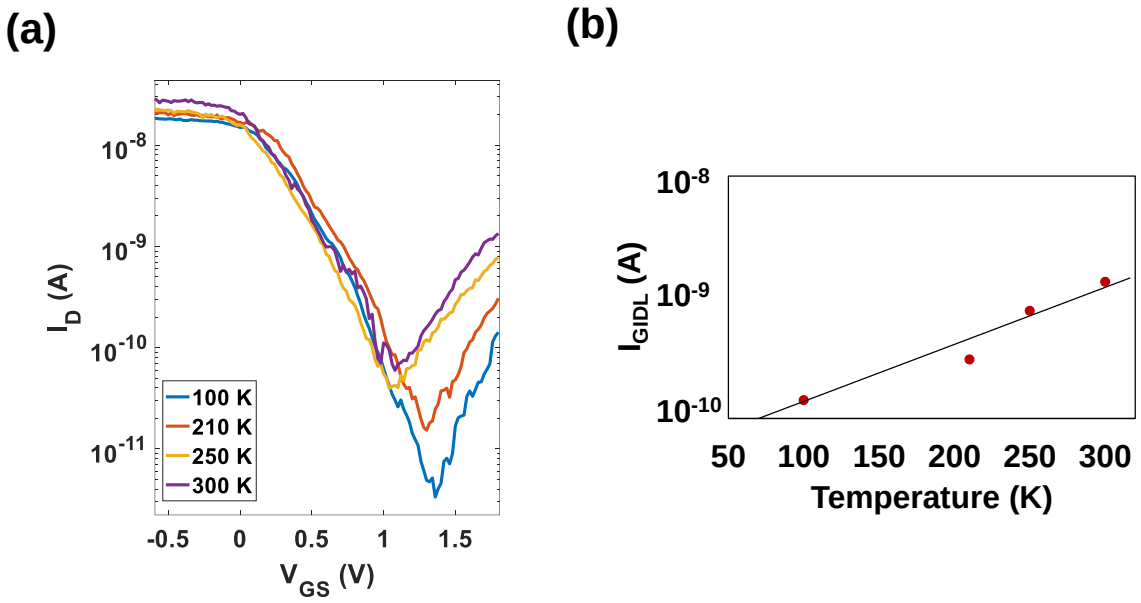


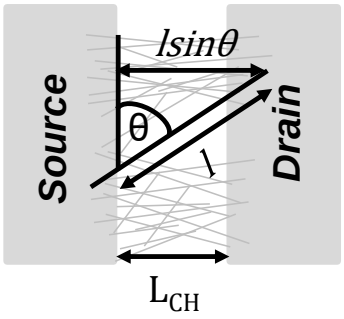
Fig. A7.4: (a) Temperature dependence of transfer characteristics of a CNFET (L_{CH} =500 nm) at V_{DS} = -1.45 V (b) Exponential dependence of I_D (GIDL current at V_{DS} = -1.45 V and V_{GS} = 1.8 V) with temperature.

We perform temperature-dependent transfer characteristics of a CNFET, from 100 °K to 300 °K. The measured results are shown in Figure A7.4. With lower temperatures, there is exponentially lower off-state leakage current. This further supports evidence of GIDL, as the tunneling nature of the off-state leakage current should exhibit exponential dependence as well.

A.8: Semiconducting CNT purity estimate

Assumptions:

- For each solution, we target a linear CNT density of ~ 50 CNTs/ μm with 2 μg ml^{-1} s-CNT concentration for incubation (CNT deposition) for a time of 48 hours or 1.728 x 10^4 s. This incubation time to density relationship was obtained from[31] and was further verified using random SEMs across different dies. Thus, we assume an average of 1000 CNTs per device (of width 20 μm).
- Since all the solutions prepared demonstrated an optical purity >99.9% from UV-Vis-NIR absorption spectra using method described in prior work[30], we assume CNFETs showing $I_{ON}/I_{OFF} < 50$ (characteristic of m-CNT) have at most 1 m-CNT per FET (since each device has <1000 CNTs on average). Here instead of defining a m-CNFET as one having low I_{ON}/I_{OFF} under low V_{DS}, we intentionally choose a high V_{DS} for our measurement, since noise margin of logic depends on I_{ON}/I_{OFF} at high drain bias (V_{DS})[33-35].
- We assume the CNTs are deposited at any random angle θ (Figure S1) with a uniform prior distribution ($0° < \theta < 180°$).
- We further assume the length of CNT (L_{CNT}) to be constant and use the expected value of length for each solution as measured from AFM characterization.
- Additionally, if a CNT crosses the source, we assume the length of the CNT under the channel region from the source towards the drain can be of length l with a uniform prior i.e ($0 < l < L_{CNT}$).



Typical incubated CNT parameters:

Number of CNTs per µm = N (~50)
Mean length = L_{CNT}
Deposition angle = θ *(relative to source)*
Channel length = L_{CH}

Fig. A8.1: Typical incubated CNT parameters. We assume uniform prior distributions of deposition angle *θ* and the length of CNT under the channel region *l*. A CNT is considered to bridge the channel if $lsin\theta > L_{CH}$.

Model:

We consider a CNT to bridge the channel if $lsin\theta > L_{CH}$.

Thus P_{bridge}, or probability of CNT bridging the channel is defined as:

$$P_{bridge} = P\ (l \sin\theta >\ L_{CH}) = P\ (\sin\theta\ >\ \frac{L_{CH}}{l})$$

If we consider l to be random variable U and $\sin\theta$ to be random variable V,

$$P\ (l \sin\theta >\ L_{CH}) =\ P(UV > L_{CH}) = \int p(V > \frac{L_{CH}}{U}) p(U) dU$$

So, with a uniform prior for θ,

$$P\ \left(\sin\theta\ >\ \frac{L_{CH}}{l}\right) = \int_{L_{CH}}^{L_{CNT}} \frac{2}{\pi} \left(\frac{\pi}{2} - \sin^{-1}\frac{L_{CH}}{l}\right) p(l) dl$$

or,

$$P\ \left(\sin\theta\ >\ \frac{L_{CH}}{l}\right) = \frac{2}{\pi L_{CNT}} \int_{L_{CH}}^{L_{CNT}} \left(\frac{\pi}{2} - \sin^{-1}\frac{L_{CH}}{l}\right) dl$$

As an example, if L_{CNT} = 1.5 µm and L_{CNT} = 1 µm, P_{bridge} ~ 0.13.

For different solutions listed in Table 1, P_{bridge} is computed and listed in Table 3 with length distribution data taken from Figure S5-S6. Please note L_{CNT} is modelled as a gaussian distribution with mean and standard deviation computed from AFM study as shown in Figure S5-S6. So P_{bridge} is computed as the expected value of $P\left(\sin\theta > \frac{L_{CH}}{l}\right)$

$$P_{bridge} = E\left[P\left(\sin\theta > \frac{L_{CH}}{l}\right)\right]$$

$$P_{bridge} = \int \left(\frac{2}{\pi L_{CNT}} \int_{L_{CH}}^{L_{CNT}} \left(\frac{\pi}{2} - \sin^{-1}\frac{L_{CH}}{l}\right) dl\right) p(L_{CNT}) dL_{CNT}$$

for given length distribution for a CNT sample.

Thus P_{s-CNT} can be computed simply as

$$P_{s-CNT} = 1 - \frac{N_{mCNFETs}}{W * N * P_{bridge} * N_{CNFETs}}$$

$N_{mCNFETs}$ = total number of CNFETs with $\frac{I_{ON}}{I_{OFF}} < 50$ at V_{DS} = 1.8 V,

N_{CNFETs} = total number of CNFETs,

W = width of the transistor

and N = CNTs per µm.

s-CNT estimate (as %) is listed in Table 3 following the above methodology.

Table A8.1: Estimated CNT purity

Sample	CNT source	Polymer	P_{bridge}	$N_{mCNFETs}$ $\left(\frac{I_{ON}}{I_{OFF}} < 50\right)$	s-CNT purity estimate (%)
LDD	Laser Ablation	PFDD	0.0971	46	99.9953
LPy	Laser Ablation	PFPy	0.0325	62	99.9809
LCz	Laser Ablation	polycarbazole	0.0770	260	99.9662
LBPy	Laser Ablation	PFBPy	0.0548	188	99.9656
ArcDD	Arc Discharge	PFDD	0.0495	172	99.9652
ArcPy	Arc Discharge	PFPy	0.0582	28	99.9952
ArcDDCz	Arc Discharge	PFDD and polycarbazole	0.0579	5000	99.9*
ArcCz	Arc Discharge	PFDD	0.0778	360	99.9532
PlaDD	Plasma	PFDD	0.0414	99	99.976

*solution-based purity estimate for ArcDDCz sample can't be calculated from electrical data since most CNFETs have a very low $\frac{I_{ON}}{I_{OFF}}$ at V_{DS} = 1.8 V so optical purity is reported.

A.9: Hybrid Conjugate Polymer Extraction (h-CPE)

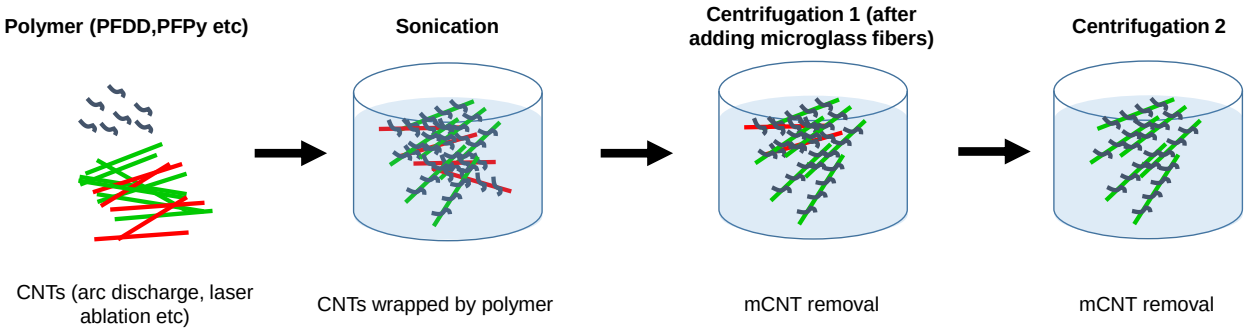


Fig. A9.1: Enhanced hybrid conjugated polymer extraction process. (a-b) Polymer and CNTs were added with toluene and tip sonicated in an ice bath for 30 min to thoroughly dispersed the solid. (c) The dispersion was centrifuged to obtain supernatant, which was combined with silica gel, sonicated at 30 oC for 30 min, and centrifuged again to collect the supernatant. (d) The solid obtained by filtering the supernatant was re-dispersed in toluene to undergo a conditioning step to yield final solution for device fabrication.

The sc-SWCNTs solutions of laser (L), plasma (Pla) and arc-discharge (Arc) tubes were prepared using an enhanced h-CPE (eh-CPE) process which include a traditional hybrid conjugated polymer extraction (h-CPE) [30], and then a final conditioning treatment. The eh-CPE process was started by mixing 160 mg of acid treated raw SWCNTs sample with 128 mg of PFDD (or, PCz) in 200 ml toluene. The mixture was sonicated for 30 min in an ice bath using a tip sonicator (Branson sonifier 250, 200 W maximum power) with a 10 mm tip operated at 60% duty cycle and 70% output. This process was repeated once again to the sediment. The supernatant of the second extraction was mixed with 200 mg of silica gel, sonicated in a bath sonicator (Branson 2510 sonicator) at ~30 °C for 40 min, stored overnight, and then centrifuged at 12,500 rpm (SLA1500 rotor, RCF:23700g) for 30 min. Afterwards, the extracted solution was filtered using a 200 nm PTFE membrane to collect PFDD/CNTs as a black film with a polymer to CNT weight ratio (P/CNT ratio) of ~1/1. For the samples with the wrapping polymer other than PFDD (or, PCz), a polymer exchange step was added. As an example, for a PFPy/CNT sample it was done by mixing

6 mg of a PFDD/CNT film with 30 mg of PFPy in 100 mL of toluene. This solution was then bath sonicated for 2 h and filtered to collect a PFPy/CNT film. This process was repeated once again to complete the polymer replacement. At last, 4~6 mg of each polymer wrapped CNT film (either obtained through direct extraction, or through polymer exchange) was dissolved in 100 mL toluene, and then underwent a conditioning to obtain the final solution with an enhanced s-CNT purity and solution stability. It was done by mixing each polymer wrapped CNT sample with more of the same polymer to adjust the P/CNT ratio in between 3/1 to 5/1 (initially, P/CNT ratio was 1/1) and then bath sonicating the solutions for 3 h at 30 °C. Then the solution was underwent a hybrid process again with a final centrifugation to complete the conditioning treatment. These pure s-CNT solutions were purged and sealed under nitrogen before deposition on high-k/metal gate stacks for CNFET fabrication.

A.10: High Purity s-CNT Extraction Additional Characterization

AFMs:

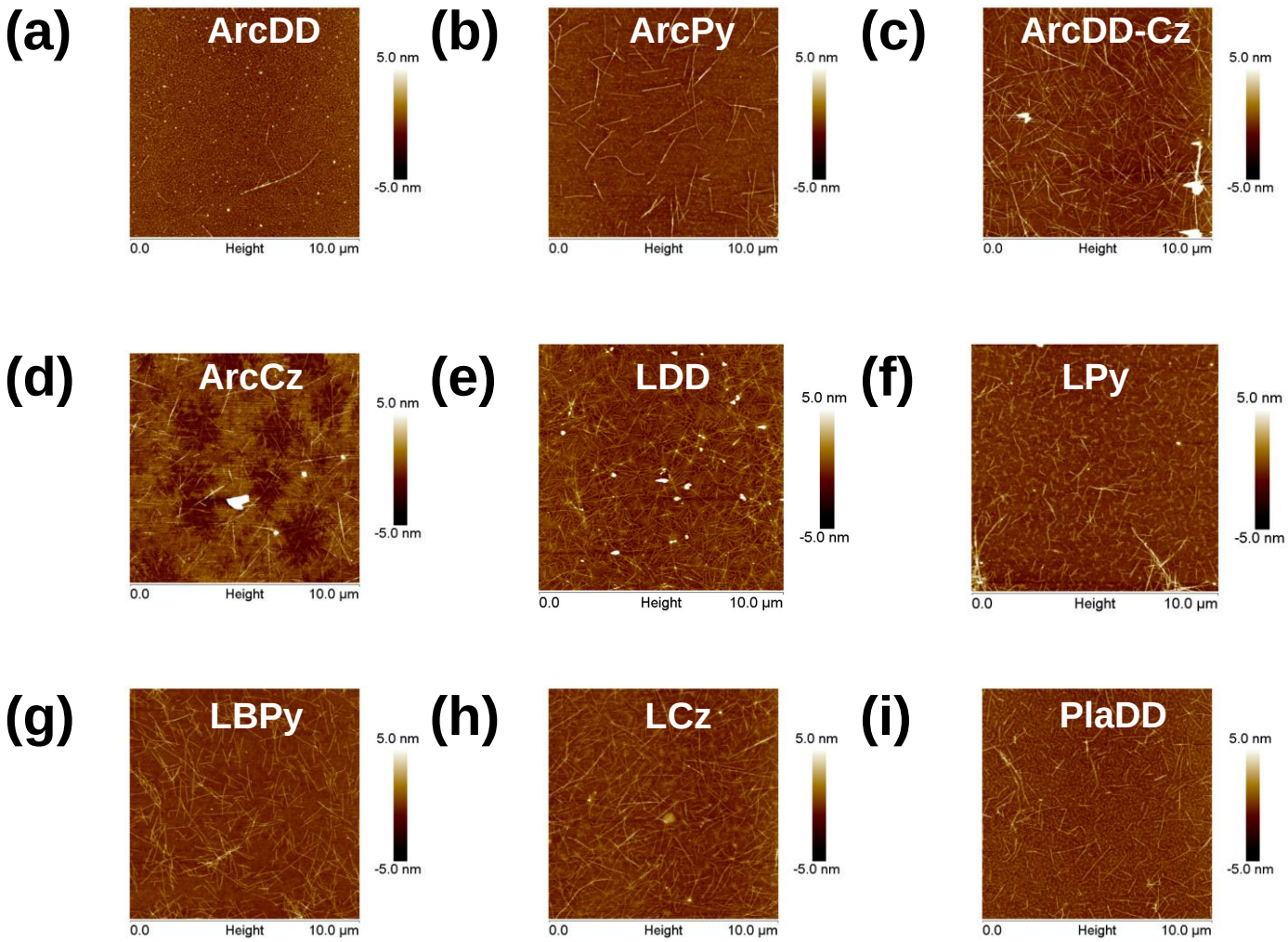


Fig. A10.1: AFMs of different CNT solutions for characterizing length of CNTs using semiconducting CNT (sCNT) solutions extracted from different CNT sources and polymers - (a-d) arc discharge CNTs (e-h) laser ablation CNTs (i) plasma CNTs. Table 1 lists all the different CNT sources and polymer types. (Length data provided in Fig S6.)

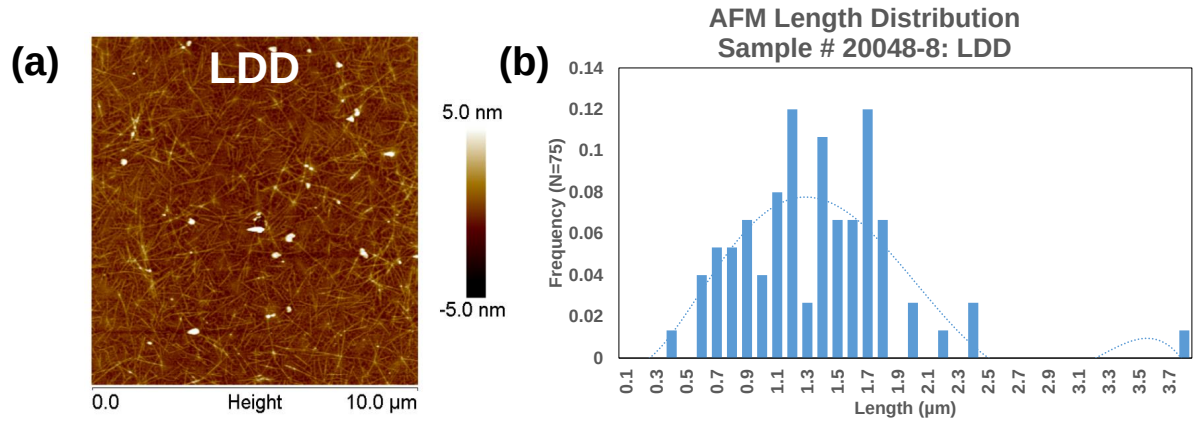


Fig. A10.2: Length distributions of sample LDD (laser ablated tubes wrapped in PFDD) using AFM analysis (Figure S5).

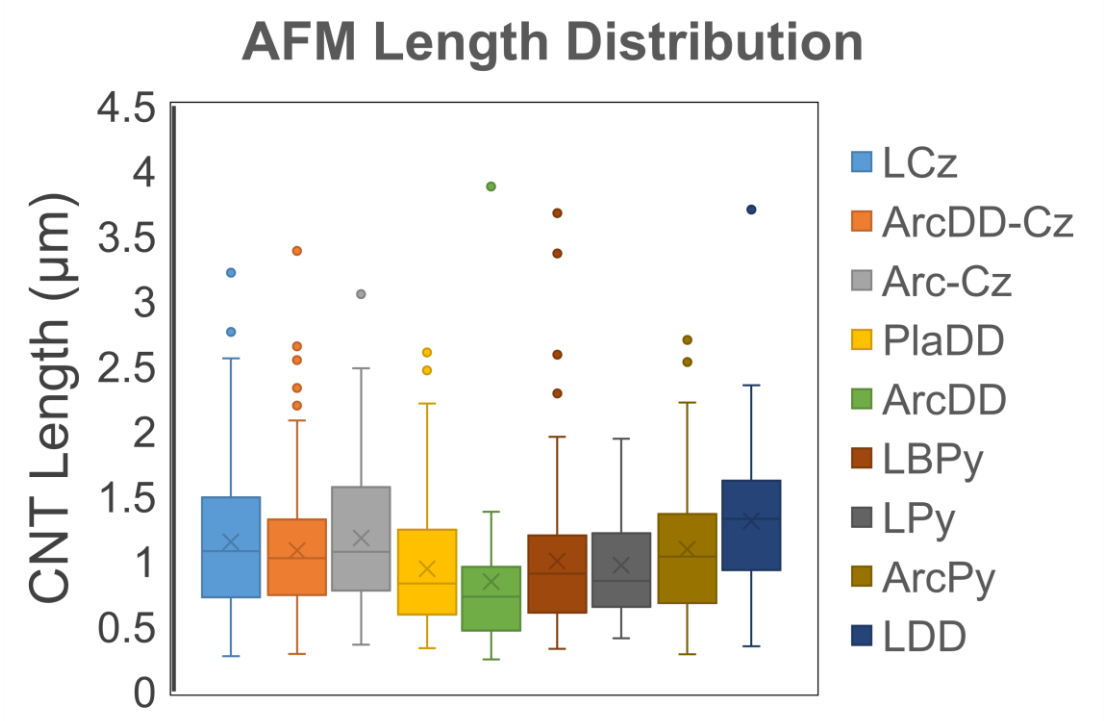


Fig. A10.3: Length distributions of all CNT solutions using similar method as shown in Figure S5-6. Table 1 lists all the different CNT sources and polymer types.

Additional Electrical Measurements:

Figure A10.4 shows I_D-V_{GS} characteristics of 500 CNFETs for V_{DS} = -0.3 V

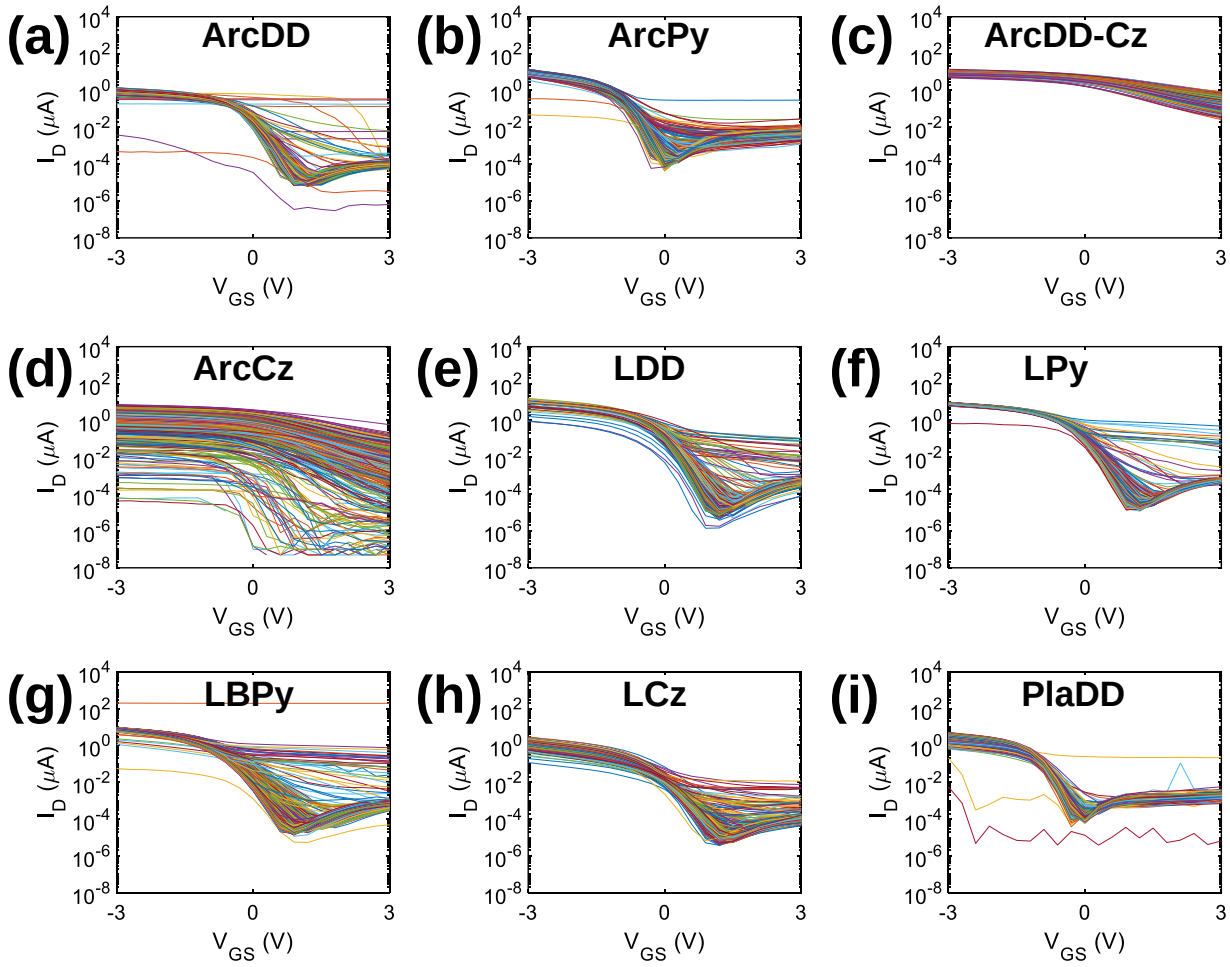


Fig. A10.4: Typical I_D-V_{GS} characteristics of 500 CNFETs at V_{DS} = -0.3 V, fabricated using semiconducting CNT (sCNT) solutions extracted from different CNT sources and polymers - (a-d) arc discharge CNTs (e-h) laser ablation CNTs (i) plasma CNTs. Table 1 lists all the different CNT sources and polymer types.

A.11: Monolithic 3D Imager Demo

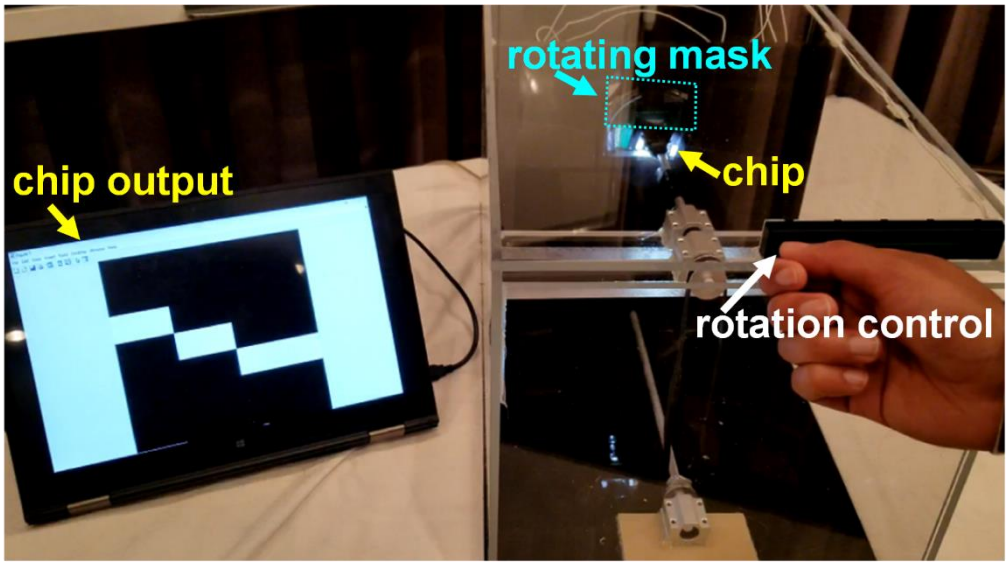


Fig. A11.1: Monolithic 3D imager demo setup in VLSI 2019. The imager chip is partially covered using a rotating mask which is controlled by a slider (labeled as rotation control). As a the mask rotates, the imager detects the edge in real-time without sending data to memory which is displayed in the monitor.

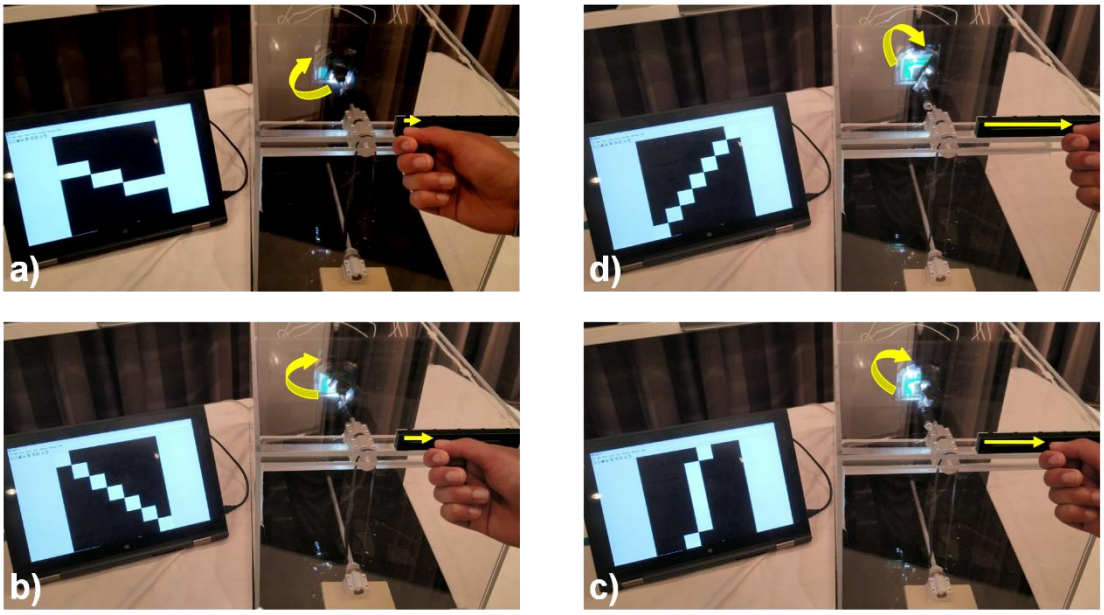


Fig. A11.2: Edge detection using monolithic 3D imager. (a-d) Sliding the rotation control (annotated in Figure A10.1) manually rotates the covering mask in front of the imager resulting in edge detection as observed in the monitor.

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- **Srimani, T.**, G. Hills, M.D. Bishop et. al. "Negative capacitance carbon nanotube FETs." *IEEE EDL* 39, no. 2 (2017): 304-307.
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