THE ARRAY E(APOLLO 17) COMMAND DECODER TEST SET

by

Paul M. Grahek

SUBMITTED IN PARTIAL FULFILLMENT OF THE

REQUIREMENTS FOR THE DEGREE OF

BACHELOR OF SCIENCE

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June, 1971

Signature redacted

Signature of Author _____
Department of Electrical Engineering

Signature redacted

Certified by _____
Thesis Supervisor

Signature redacted

Accepted by _____
Chairman, Departmental Undergraduate Thesis Committee

ABSTRACT

This thesis describes the digital hardware of an automatic test set which was designed by the author and built at the Aerospace Systems Division of the Bendix Corporation, under contract to the National Aeronautics and Space Administration. The test set described here will be used to check out and qualify for flight a component of the Apollo Lunar Surface Experiment package, which is the package of experiments set up and left behind on the Lunar Surface by two Apollo Astronauts.

Specifically, the test set will test the component known as the Command Decoder. The function of the Command Decoder, briefly, is to decode the output of the receiver in the package and route the commands to the proper part of the package. The test will be performed by feeding all possible combinations of inputs into the Command Decoder and examining the outputs for errors.

ACKNOWLEDGEMENTS

I would like to thank the Aerospace Systems Division of the Bendix Corporation for allowing me to do this thesis with the facilities in their plant at Ann Arbor, Michigan, and to Mr. George Cripps, who supervised the project.

I also would like to express my appreciation to the National Aeronautics and Space Administration for giving permission to use the photographs included here.

Last of all, of course, I am deeply indepted to Mr. Hoo-Min Toong for his tireless efforts which helped me to complete this project.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF FIGURES (Continued)

CHAPTER I

INTRODUCTION

The Apollo mission is a NASA project designed to soft-land astronauts on the surface of the Moon for exploration and the deployment of scientific experiments. Originally, ten such missions were planned, but that number has since been reduced to seven. To date, four of those missions have been flown, three of which were successful. The fourth was aborted when an oxygen tank exploded.

One of the objectives of these lunar landings is to set up a radio-controlled scientific data collection station, called the Apollo Lunar Surface Experiment Package, or Alsep. This package is designed to be set up by the two astronauts and left behind on the surface to operate for at least one year. Two such packages are presently operating on the lunar surface. The smaller package taken up on Apollo 11 has since terminated operation. The Alsep package contains a Central Station which controls and collects data from the individual experiments. Within this Central Station, as part of the uplink, is a module called the Command Decoder, whose function is to interface between the receiver and the rest of the system.

For Apollo 17, which is the last planned lunar landing in July, 1972, the Central Station is being completely redesigned for an expected life of at least two years. Before that flight it is desired to completely test each of the components of the Central Station, including the Command Decoder. This is to be performed by a digital test set which will automatically and exhaustively test the Command Decoder. The

primary concern of this report will deal with the design and implementation of the test system.

The Command Decoder, being basically a digital system, can be tested best by supplying signals at its inputs from another digital system, i.e., the test set, and examining the outputs for the proper response. The test set will do this automatically or manually, will be able to supply the Command Decoder with all necessary inputs, and will display all of its outputs.

There are three stages of testing before the actual flight. First, there is a design verification test. For this test, hardware similar to that which will actually go to the Moon is built and tested under worst case conditions. It is first tested at ambient conditions, then at hot and cold limits, and then in a thermal vacuum chamber under conditions it will experience on the Moon. This test also helps to iron out test procedures and test set-flight hardware interface problems.

The second test, on the qualifying model, is the most stringent. In this test, hardware that is exactly the same as the flight hardware is tested exhaustively to prove that the unit will live up to its claimed specifications. If the test is successful, the unit is qualified and the flight model is built. The flight model is then tested prior to integration into the system.

The Design Verification Test was started on April 20, 1971, and will continue until approximately the middle of June, 1971.

To provide a sufficient background for the interested reader, a brief description of Alsep will first be presented.

CHAPTER II

DESCRIPTION OF ALSEP

The Apollo Lunar Surface Experiment Package, or Alsep, is a package of remote controlled scientific experiments designed to be deployed on the lunar surface by two Apollo astronauts. Its function is to gather and transmit to Earth data about the lunar environment.

The package consists of three subsystems: the power subsystem, the data subsystem, and the experiments themselves. In the power supply subsystem, electrical power is generated by a Radio-Isotope Thermal generator, or RTG, which is a hot core of nuclear material which heats thermocouples to supply electrical power. The average power output of the RTG is about 70 watts. The power is conditioned by the Power Conditioning unit which converts and regulates the output of the RTG to voltages needed by the rest of the system. These voltages are then distributed by the Power Distribution Unit.

The Data Subsystem consists of the components of the uplink and downlink. The uplink consists of a receiver, which receives and demodulates a 2119 MHz signal from Earth, upon which commands are modulated; and the Command Decoder, which further demodulates the uplink signal to digital 1's and 0's and decodes the received commands.

The downlink components are the Data Processor, which collects data from the experiments, and formats it into a form suitable for transmission to Earth, and the transmitter, which actually transmits that data. Shared by the uplink and downlink are the antenna, and the

diplexer filter, which allows the same antenna to be used by both the transmitter and receiver. With the exception of the RTG, the components of the power and Data subsystems form the Central Station Electronics, which is shown deployed on the Moon in Figure 1. The modules that make up the Central Station are mounted on the base plate, and covered by a thermal bag. They are screened from direct sunlight by the sides and top of the Central Station. Figure 2 shows the modules mounted on the base plate and the thermal bag which closes over them.

The third part of the system, the actual experiments, varies. Up to five experiments are carried on each flight, but different flights take different experiments. For example, Apollo 12 Alsep contained a Passive Seismic Experiment, a Lunar Surface Magnetometer, a Charged Particle Detector, a Suprathermal Ion Detector, and a Lunar Mass Spectrometer. Apollo 17, on the other hand, will contain a Lunar Surface Profiling Experiment, a Heat Flow Experiment, a Lunar Surface Gravimeter, a detector for Lunar ejecta and Micrometorites, and a Lunar Mass Spectrometer. Figure 3 shows the CPLEE and SIDE in the foreground, with the Central Station and RTG in the background. A block diagram of the basic Alsep System is presented in Figure 3A.

For all flights except Apollo 17, the Alsep is designed to turn itself off after one year of operation. However, since Apollo 17 is the last lunar flight, the system is being redesigned to last two or more years on the lunar surface.

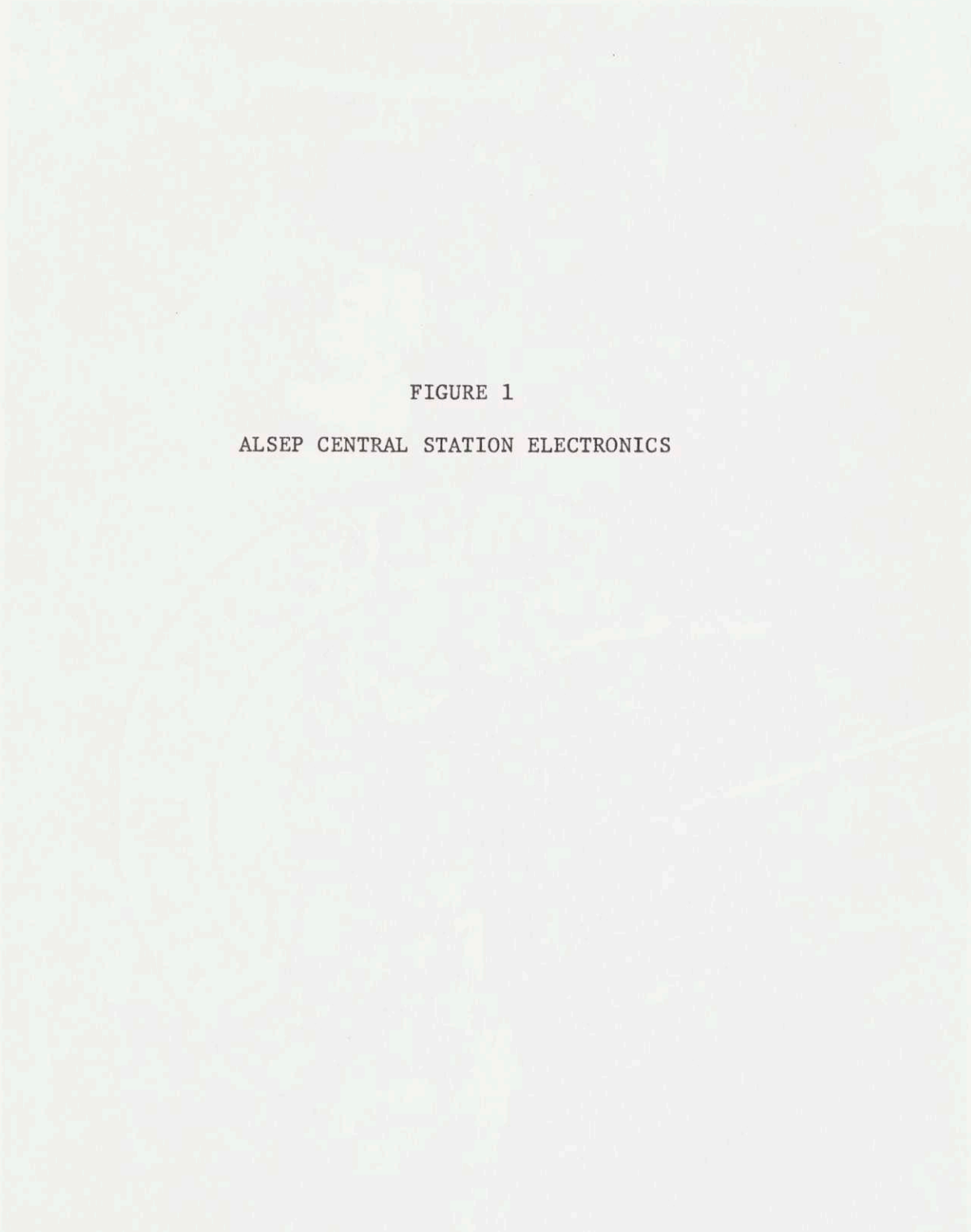


FIGURE 1

ALSEP CENTRAL STATION ELECTRONICS

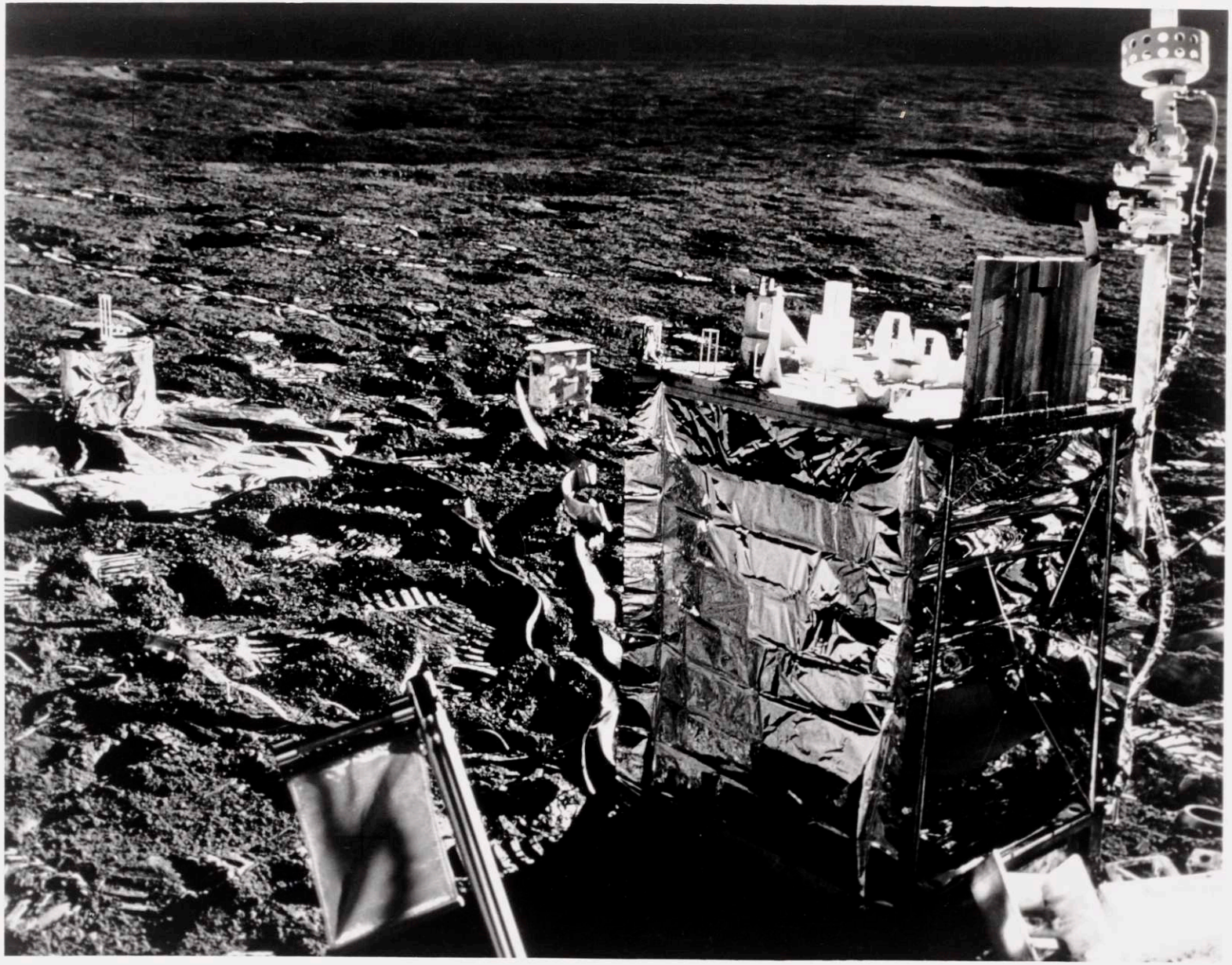


FIGURE 2

ALSEP MODULES

2330333 K
CENTRAL STATION ELECTRONICS, PSS
COMMAND DECODER
DIGITAL DATA PROCESSOR
POWER DISTRIBUTION UNIT

FIGURE 3

ALSEP EXPERIMENTAL PACKAGES

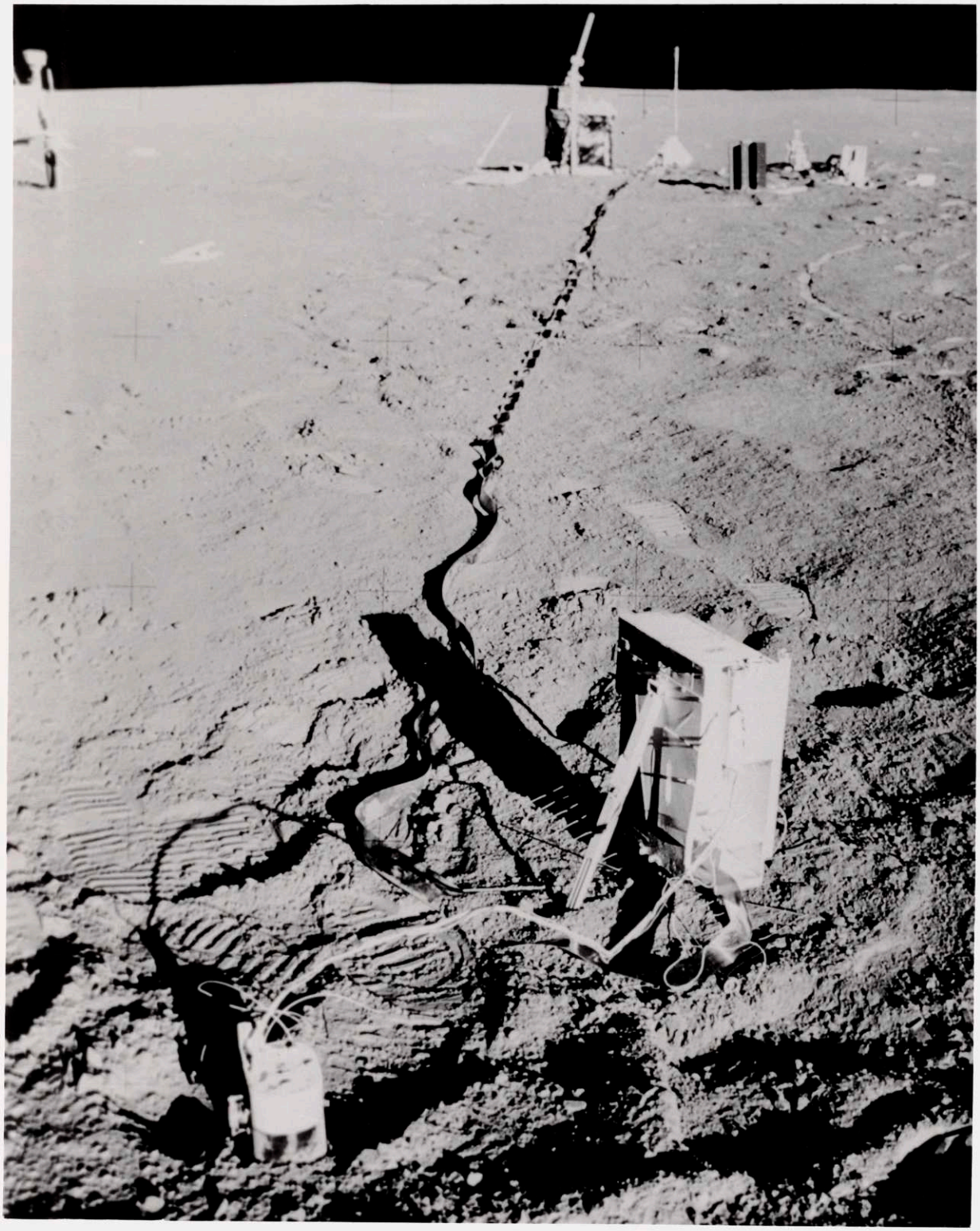
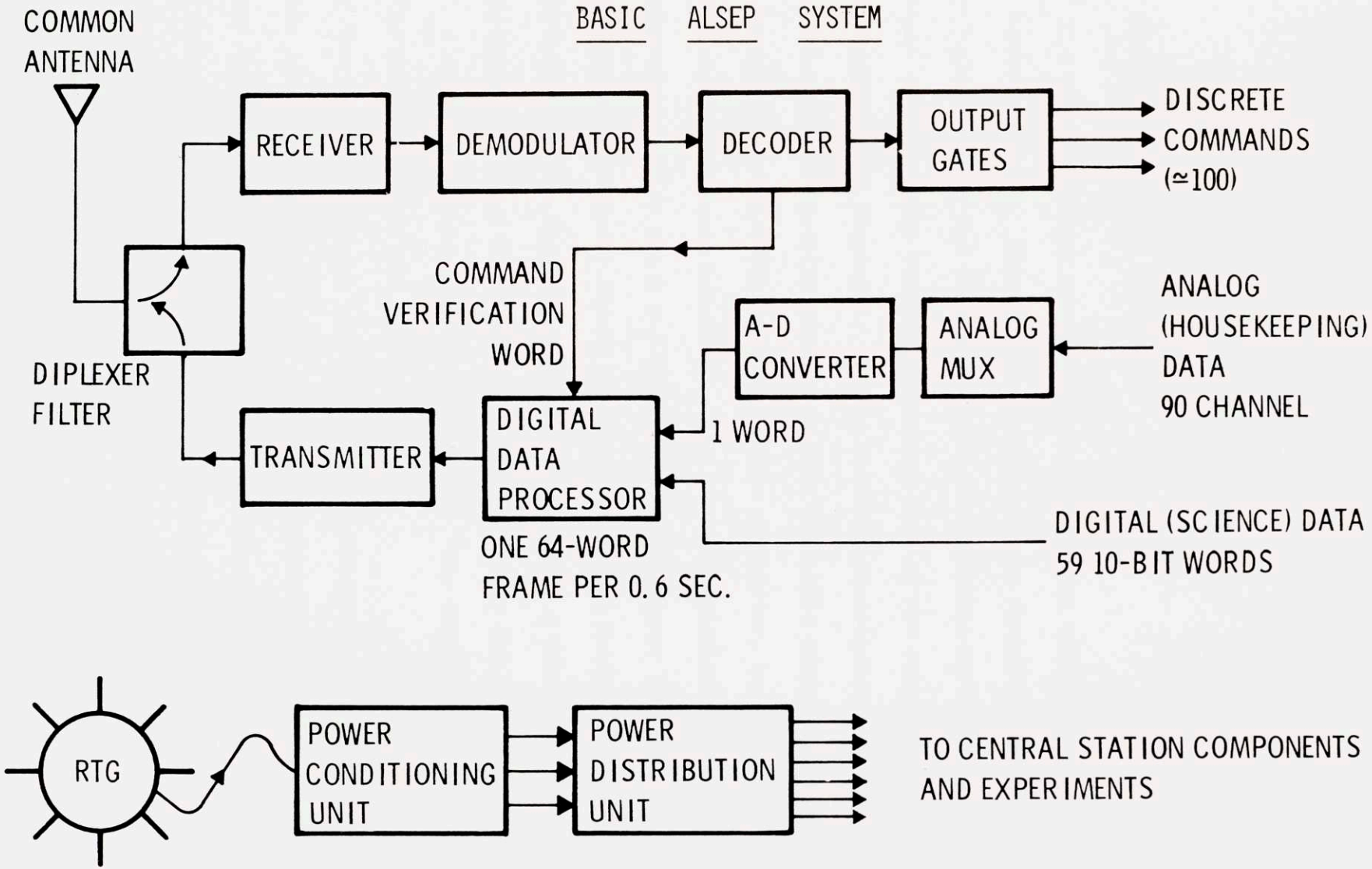


FIGURE 3A

BLOCK DIAGRAM OF BASIC ALSEP SYSTEM


BASIC ALSEP SYSTEM
COMMON ANTENNA
RECEIVER
DEMODULATOR
DECODER
OUTPUT GATES
DISCRETE COMMANDS (≃100)
COMMAND VERIFICATION WORD
DIPLEXER FILTER
A-D CONVERTER
ANALOG MUX
ANALOG (HOUSEKEEPING) DATA 90 CHANNEL
TRANSMITTER
DIGITAL DATA PROCESSOR
1 WORD
ONE 64-WORD FRAME PER 0.6 SEC.
DIGITAL (SCIENCE) DATA 59 10-BIT WORDS
RTG
POWER CONDITIONING UNIT
POWER DISTRIBUTION UNIT
TO CENTRAL STATION COMPONENTS AND EXPERIMENTS

CHAPTER III

THE COMMAND DECODER TEST SET

Description of the Unit Tested

The piece of flight hardware that the test set will test is called the Command Decoder. Briefly, its function is to interface between the flight receiver and the rest of the Alsep package by decoding commands sent from the Earth, and routing them to the proper experiment or Central Station component. A more detailed description follows.

The receiver receives signals on 2119 MHz. The signal is phase-modulated with a 1 & 2 KHz modulated audio subcarrier, on which the logical 1's and 0's are modulated. The receiver demodulates the 2119 carrier and supplies the 1 & 2 KHz audio to the Command Decoder.

The Command Decoder itself is in two parts: an analog section and a digital section. The analog section consists of a demodulator which demodulates the 1 & 2 KHz composite audio and feeds the digital section with a serial stream of logical 1's and 0's. The digital section does the actual decoding of the bit stream.

The commands are sent via the uplink as twenty-one bit words, the format of which is as follows: the first seven bits are an address, the second seven are the complement of the command, and the last seven are the actual command. The address serves two purposes: first, it permits the use of a single uplink frequency for several Alseps, and, second, it decreases the possibility of a spurious command execution by increasing the number of bits that must be decoded.

The complement of the command is sent in the middle seven bits. Its purpose is to provide a means to determine that the command was received correctly, which is accomplished by comparing the command with the command complement.

All this decoding is done as follows. The bit stream is shifted through an eight bit shift register. When the address is in the leftmost seven bits (assuming that data is shifted from left to right) it is detected, and the Command Decoder leaves the scan mode and enters the command mode. Eight bits after the address is detected, the command complement is sitting in the right most seven bits, and the first bit of the command is in the left most bit. For the next seven bits the Command Decoder serially compares the command with the command complement to ascertain that the command was properly transmitted and received. When this comparison is complete, and the command is in the right most seven bits, one of two things happens. If the command checked valid, the seven bits are decoded into one of 104 possible commands, and the line which is being commanded goes from a logical "1" to a logical "0" for 21 msec. At the same time, a "1" is placed in the left most bit to "remember" that the command checked good.

If the check detected an error, the command is considered to be invalid and is not executed. Also, a "0" is placed in the left most bit to indicate that the command checked bad.

Incidentally, the shift register was stopped when the command was in the right most seven bits.

After the command is executed (or not executed if the check was bad)

the Command Decoder is locked out, and does nothing until it sends back a "Command Verification Word" or "CVW" via the downlink. To explain the CVW, a brief discussion of the downlink is necessary.

The data collected on the Moon is transmitted as digital data in a 64-word frame, with each word containing ten bits. Thus, a frame consists of 640 bits. The 64 words of the frame contain data from the science experiments with the following exceptions. Words one, two, and three are called the control words, and contain such data as a 22-bit sync pattern, the frame number, and Alsep identification data. Word 7 contains the CVW, word 33 contains "housekeeping data", and word 63 contains data indicating how much power is being drawn from the power supply. Word 33 is different than the rest in that it is sub-commutated over ninety frames, permitting 90 channels of housekeeping data. Housekeeping data consists of various temperatures, status of the Central Station components, and the like. The sub-commutated housekeeping channels are the reason why the frame number is transmitted.

The Command Decoder then has an opportunity to transmit a CVW back to Earth during word seven of every downlink frame. Obviously, since the time needed to send a complete frame is approximately .6 second, there is not going to be a CVW for transmission every frame. Therefore, when a command has been received and the Command Decoder is ready to send a CVW, it tells the Data Processor (which does the downlink formatting) that it has a CVW to send, and when word 7 next comes around it shifts the CVW out of the Command Decoder and down to

Earth via the downlink. The CVW contains, by the way, the 7 bits of the command received, the bit that was a "1" or "0" indicating whether or not the command was valid, and two filler bits. This makes a total of ten bits, or one complete downlink word. After transmission of the CVW, the Command Decoder clears itself and returns to the scan mode. There are other subsidiary functions of the Command Decoder; however, they are beyond the scope of this paper.

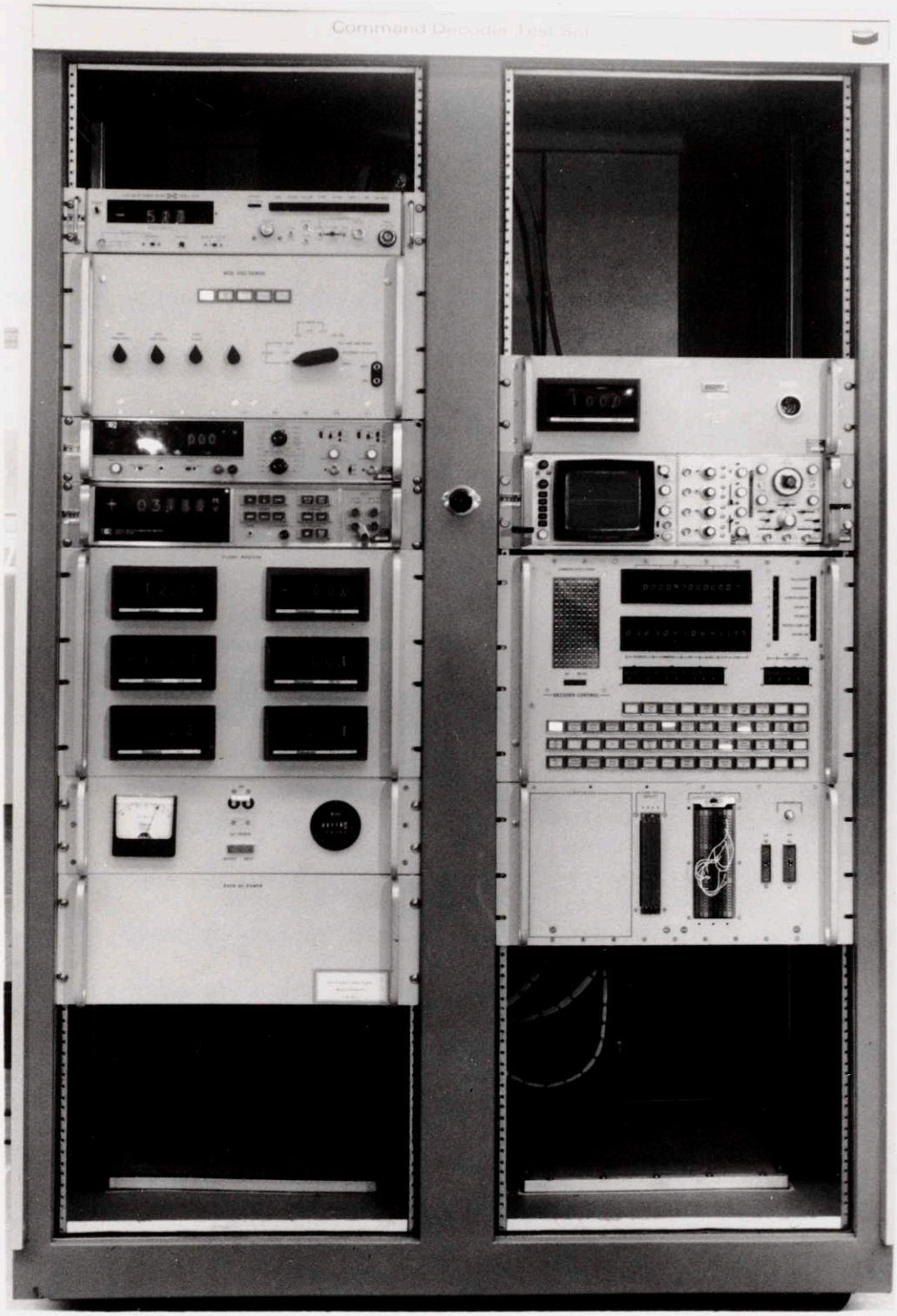
Description of the Test Set

The test set (Figure 4) is to provide a means of testing the Command Decoder completely automatically. The test is accomplished by sending a command to the unit, waiting for a response, and evaluating whether or not the response was correct. The underlying philosophy behind the design of the test set is to provide the Command Decoder with inputs and outputs exactly like those it will see when integrated into the complete system. The test set, then, needs circuitry to generate commands, a modulator, a shift register to receive the CVW, and error detectors on the 104 discrete command lines. In addition, it must have some sort of control circuit to run the test automatically.

The test set is capable of testing the Command Decoder in two ways. The first test is called a Bit Error Test, in which 1 & 2 KHz modulated data is fed into the demodulator. The digital output of the demodulator is then compared with what went in. The operator has four choices of the data that is fed into the demodulator. The choices are all 1's and 0's, 101010..., or a psuedo-random sequence. The serial comparator that

FIGURE 4

COMMAND DECODER TEST SET


Command Decoder Test Set

looks at the demodulator output is simply an equivalence function, sampled at the end of a bit period and fed to an error counter. This test is not shown on the block diagram.

The most complex, and main, purpose of the test set is the Word test, described by the block diagram in Figure 5. In this test, actual 21 bit command words are sent to the Command Decoder.

The Command and Address that are sent to the Command Decoder are selectable from two sources. The operator can manually select the desired Command and Address, on front panel thumbwheels, or, if automatic operation is desired, internal cycle counters will automatically select the next Command and Address.

In addition to sending commands to the Command Decoder, the test set also has the capability of sending the desired command at a selected time slot of the downlink frame. The reason for this is as follows. The Command Decoder runs at a bit rate of 1 KHz, while the Data Processor runs at a bit rate of 1060 BPS. This asynchronous operation has caused problems with earlier Alseps, in that sometimes the Command Decoder would not clear itself after sending a CVW. The Command Decoder for Apollo 17 has, hopefully, designed out this problem, and the test set must make sure it has. Therefore, the test set will initiate a transmission of a command only during the bit and word of the downlink frame selected by the operator.

The procedure for manually testing the Command Decoder will be as follows. First, the operator must select the command and address desired, and the bit and word during which he desires them to be sent.

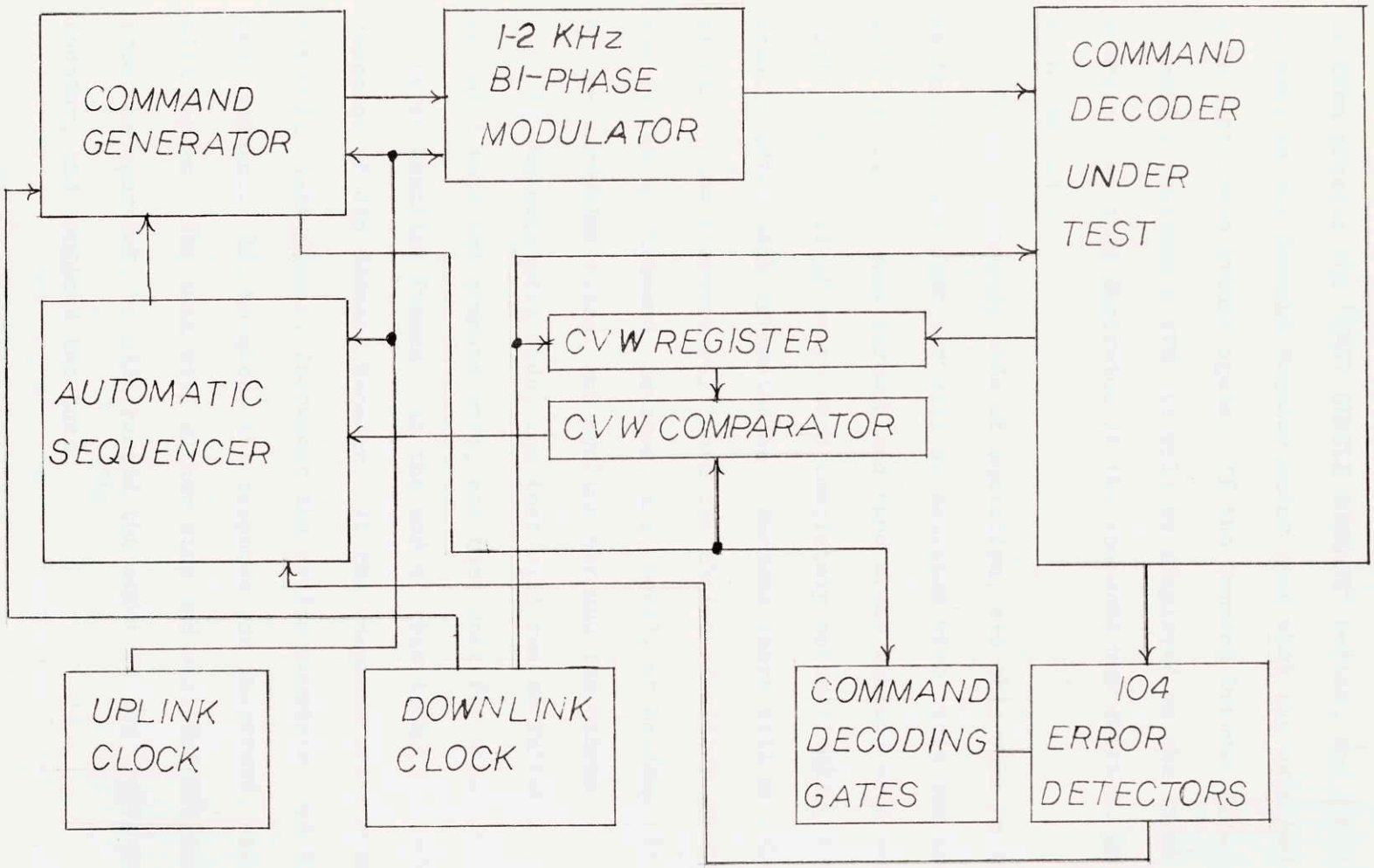


FIG. 5 SIMPLIFIED BLOCK DIAGRAM OF TEST SET

He then presses the "XMIT SINGLE COMMAND" button, and the command will be sent to the Command Decoder under test when the selected downlink time slot comes around again. If the Command Decoder then executes a command or outputs a CVW, it will be displayed on the front panel. The operator can then determine if the response was correct, and continue with the test.

In the automatic mode of operation, all this will be done automatically. The test set will be equipped with cycle counters, so it will be able to step through and send every command with every address during every bit of every word completely automatically, evaluating the results after each transmission. Because there will be different types of tests, the operator will have the choice of either cycling through the variables (Command, Address, Bit, Word), or holding any combination of the variables fixed, and cycling through the others.

In the automatic mode, the test will run as follows. The test set will send the command word, and then wait for a period of time equal to three downlink frames. At the end of this time, it evaluates the response of the Command Decoder. If the response was correct, the test set will clear itself, increment the cycles counters, and transmit the next command. If, however, the response was incorrect, one of two things will happen. The test will either stop and wait for further instructions from the operator, or will record the error on the appropriate error counter, and continue the test.

CHAPTER IV

FUNCTIONAL DESCRIPTION

As mentioned previously, the test set is capable of performing two types of tests: a bit error test and a word error test. An overview of the functional block diagram is presented in foldout Figure 6. Which of these modes the test set is in is determined by the block on the block diagram (Figure 6) titled Mode Select. In the bit error mode this block presents at the input of the Command Register data that will produce the desired bit pattern. The patterns available are all 1's, all 0's, alternating 1's and 0's, and a psuedo-random pattern. This data is clocked by the Uplink clock to the 1 & 2 KHz Modulator, which feeds the input of the Command Decoder under test. The Serial Comparator then compares the digital output of the Command Decoder Demodulator with what was fed in, and for every error that occurs, a pulse is sent to a counter. That error count can then be used to determine the bit error rate of the demodulator. The block called Error Generator is used as a self-check of the comparator. During the self-check, an error is generated every other bit, and the counter is set to read frequency. Proper operation of the comparator will then be verified by an error rate of half the clock frequency.

In the Word Error test, the Mode Select simply feeds the data at the output of the Command Register back into the input, turning the Command Register into a re-circulating shift register, which does the actual command generation. The 21-bit commands are loaded in parallel

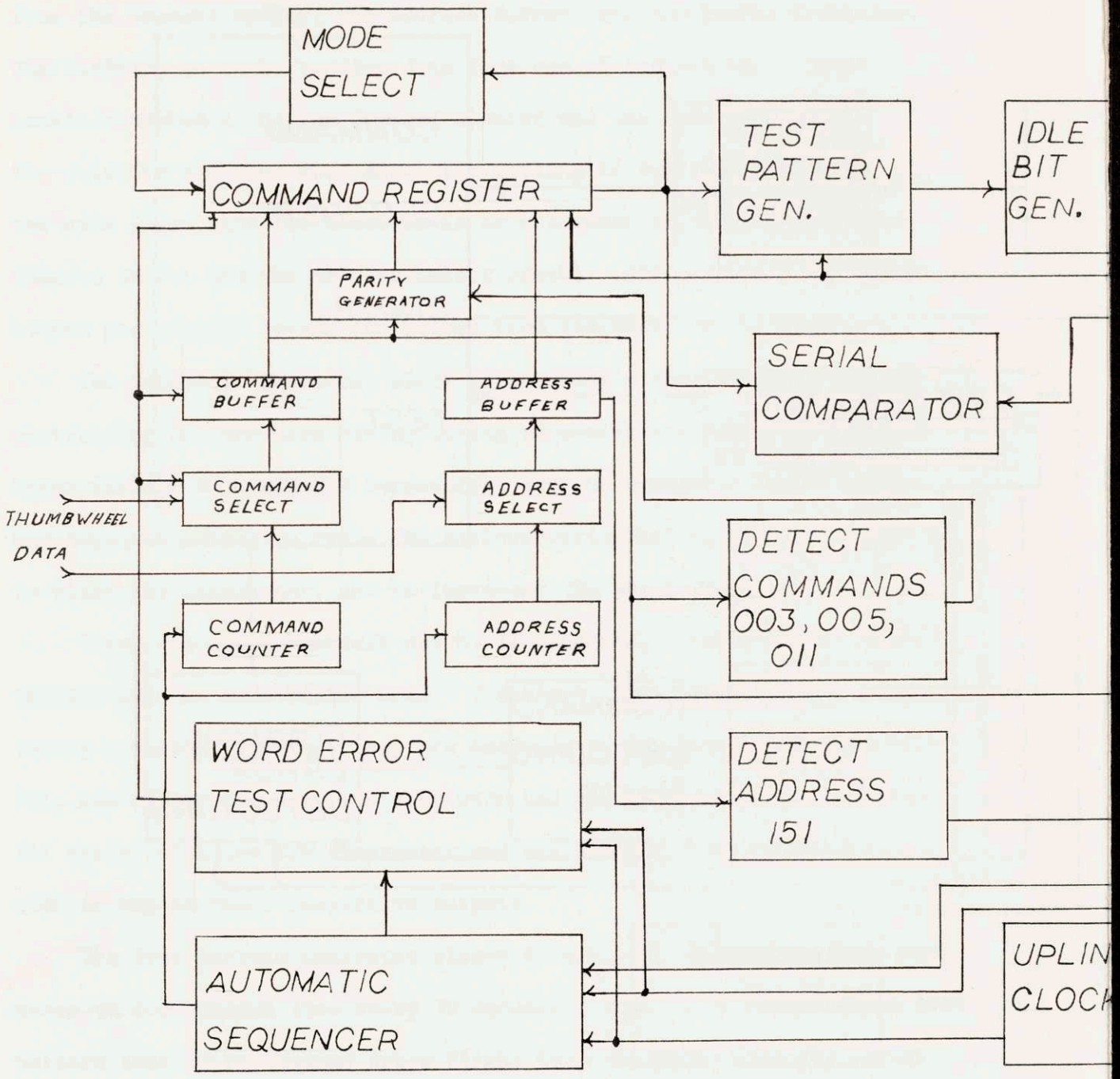
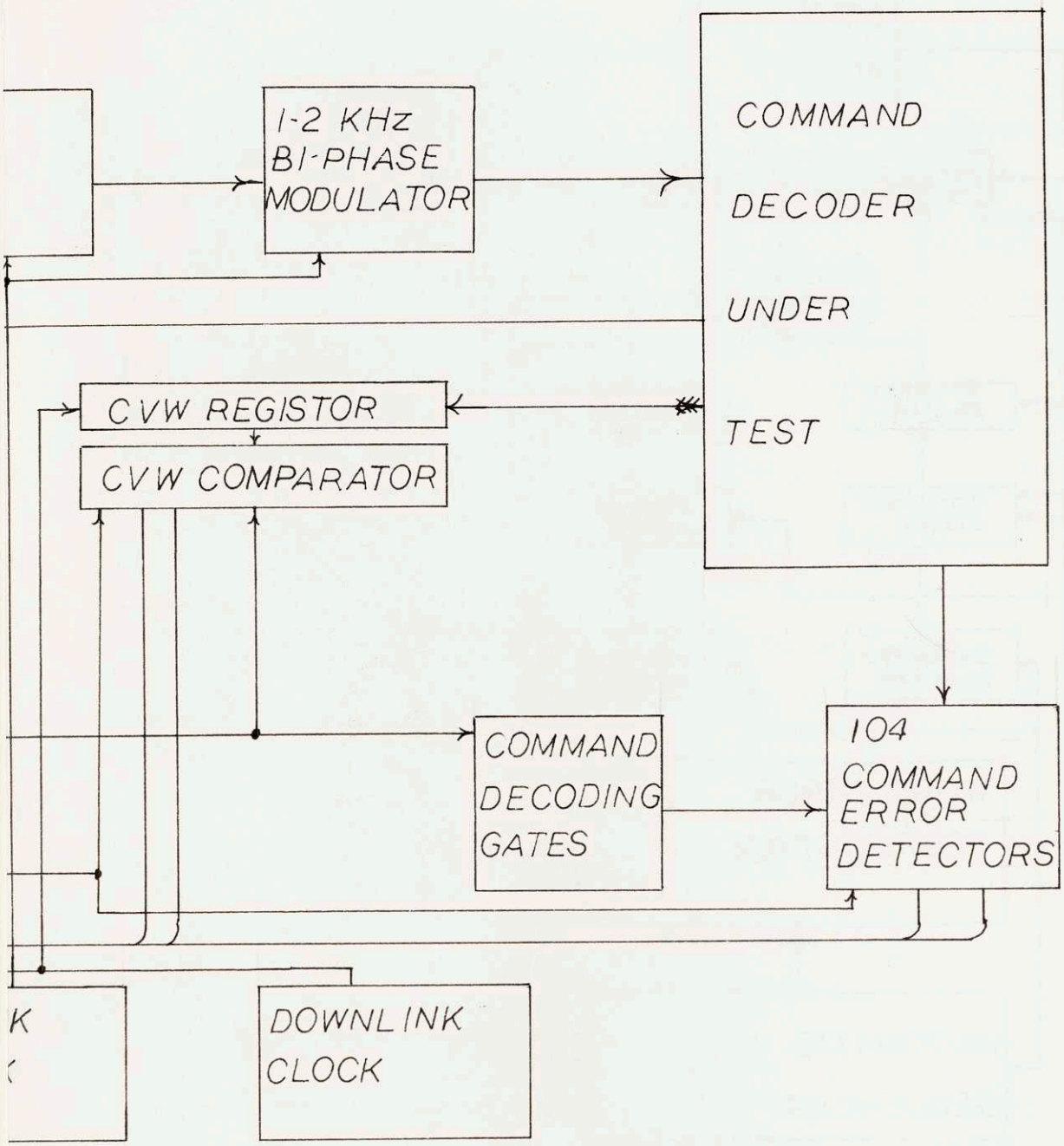


FIGURE 6 DETAILED BLO


1-2 KHz
BI-PHASE
MODULATOR
COMMAND
DECODER
UNDER
TEST
CVW REGISTOR
CVW COMPARATOR
COMMAND
DECODING
GATES
104
COMMAND
ERROR
DETECTORS
DOWNLINK
CLOCK

CK DIAGRAM

from the Command Buffer, the Address Buffer, and the Parity Generator. The Buffers, in turn, receive data from one of two places -- front panel thumbwheels, or the Command Counter and the Address Counter. The counters are used when automatic cycling is desired. Whether the data comes from the thumbwheels or a counter is determined by the Command Select and the Address Select blocks. All the above mentioned blocks get control levels and pulses from the Test Control block.

The Automatic Sequencer Block is the module that does the controlling and decision making during automatic cycling. It receives Error Signals from the CVW Comparator, and the Command Error Detectors, and supplies pulses to cycle the various variables, to transmit commands, to clear the comparator, and to increment the error counters.

There are three commands which, if executed, would lock the Command Decoder into an undesirable mode. Therefore, when these commands occur during automatic cycling, they are detected by the Detect Commands 003, 005, and 011 block, and then sent with bad parity. The Detect Address 151 block tells the CVW comparator and the Command Error Detectors when to expect their respective outputs.

The Test Pattern Generator places 40 msec. of alternating ones and zeros on the command line every 30 seconds. This is to simulate the test pattern sent by the Manned Space Flight Network, which does the actual transmission of Commands. The Idle Bit Generator sets the Command Line to a one or a zero whenever a command or the test pattern is not being sent.

The Uplink Clock supplies 1 KHz clock pulses to those blocks which

are used for command transmission. In addition, it supplies timing waveforms to the 1 & 2 KHz modulator for use in generating a signal usable by the Command Decoder.

There are two outputs from the Command Decoder: the Command Verification Word and the actual discrete commands. These are checked for correctness by the CVW Comparator and the Command Error Detectors. The CVW Comparator compares the contents of the command buffer with the contents of the CVW Register. With the information from the Detect Address 151 block, it can then determine if a Hit or Miss error has occurred. The Command Error Detectors serve the functions of storing and displaying a received command, and comparing received commands with the output of the Command Decoding gates. This information, along with the information about which address was sent, is used to generate Command Hit and/or Miss errors.

The Downlink Clock serves two functions. First, it provides the Command Decoder and the CVW Register with signals needed to obtain a CVW and, second, it provides information as to when a command may be transmitted.

The Transmit Request Timing block compares the contents of the panel thumbwheel, or, if the variables are being cycled, cycle counters, with the state of the downlink clock and outputs a transmit pulse at the proper time.

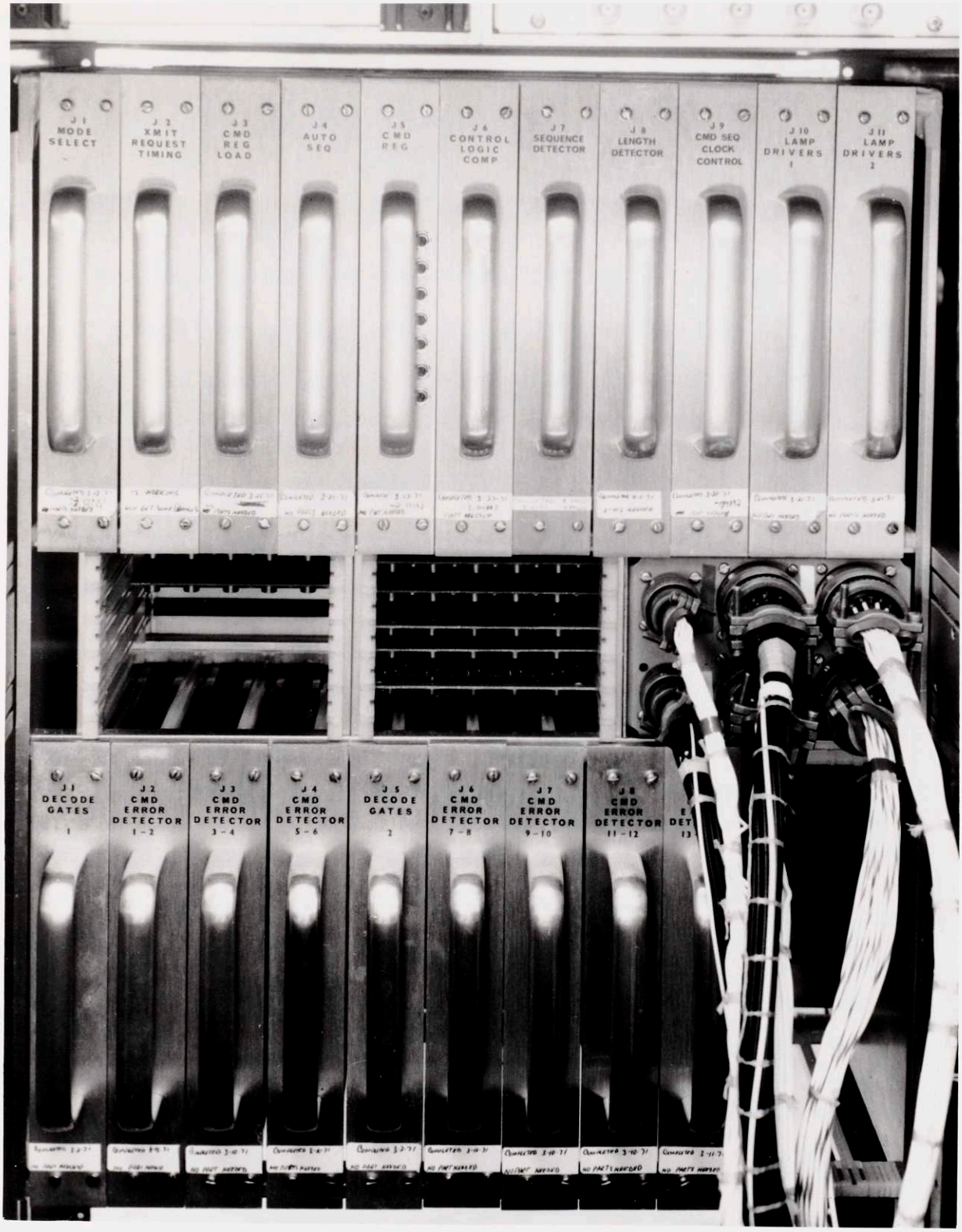
The test set logic is mounted on Scambe Dip-carrier boards, which hold a maximum of 60 I.C.'s apiece. Figure 7 shows a representative card, and Figure 8 shows the cards mounted in the rack.

FIGURE 7

REPRESENTATIVE IC BOARD CONSTRUCTION

FIGURE 8

PHYSICAL ORGANIZATION OF TEST SET


J1 MODE SELECT
J2 XMIT REQUEST TIMING
J3 CMD REG LOAD
J4 AUTO SEQ
J5 CMD REG
J6 CONTROL LOGIC COMP
J7 SEQUENCE DETECTOR
J8 LENGTH DETECTOR
J9 CMD SEQ CLOCK CONTROL
J10 LAMP DRIVERS 1
J11 LAMP DRIVERS 2
J1 DECODE GATES 1
J2 CMD ERROR DETECTOR 1-2
J3 CMD ERROR DETECTOR 3-4
J4 CMD ERROR DETECTOR 5-6
J5 DECODE GATES 2
J6 CMD ERROR DETECTOR 7-8
J7 CMD ERROR DETECTOR 9-10
J8 CMD ERROR DETECTOR 11-12

CHAPTER V

DETAILED LOGIC DESCRIPTION

Mode Select

This block contains combinational logic set by operator switches which in turn sets up the inputs of the Command Register for the various modes. For a list of symbol definitions and a description of MSI packages, refer to Appendix A. In the Word Error test, the output of the Command Register is simply fed back in to the input. For the bit error mode, the four bit patterns are generated as follows. All ones and all zeros are generated by setting the Command Register J and $\overline{K}$ inputs to a one or a zero. For alternating ones and zeros, J is set high and $\overline{K}$ is set low. For the psuedo-random sequence, the "exclusive or"function of the last two bits of the Command Register is fed into the J and $\overline{K}$ inputs. This generates $(2^{24} - 1)$ 24 bit words of psuedo-random data.

Command Register

The Command Register is a 24-bit shift register used for transmitting the 21 bit commands, and generating the bit patterns for the bit error test. The register is made up of six T.I. type 74L99 four bit MSI shift registers.

Command and Address Selectors and Buffers

The selectors and buffers are actually two functions of one kind

of MSI chip. Four T.I. type 74L98's are used here, each I.C. performing the dual function of selecting and storing four bits apiece.

Command and Address Counters

These are counters used for automatic cycling. They receive increment signals from the Automatic Sequencer, and their outputs go to the Command and Address Selectors. The Command Counter is a straight seven bit binary counter using two SN74193's, but the address counter is not quite so straightforward. If all possible 128 addresses were cycled through, the test would be prohibitively long. For this reason, only ten selected addresses are cycled through. Two approaches were tried to generated these ten addresses. First, a specialized seven bit, ten state counter was designed. However, the drawback to this plan was that the counter wouldn't know what to do if an address other than those selected ten was loaded into it. For this reason, a plain BCD counter was used with decoding for the seven bit addresses. The presetting could then be accomplished by decoding seven bits of address thumbwheel data into a four bit code.

Test Control

As its name implies, this block of logic controls the word error test. Its functions include: loading the buffers, loading the Command Register, controlling the Automatic Sequencer, and synchronizing the test pattern with the bit stream.

When a "Transmit Single Command" or Transmit pulse from the Automatic Sequencer is received, the buffers are loaded, and a command is sent, provided that the test set is not in the process of sending a test pattern. If a test pattern is in progress, the buffer is still loaded, but the transmit pulse is stored until the test pattern is over. When the test pattern is over, three kinds of pulses must be sent to the 74L99's in the Command Register to generate a command. First, a one must be placed on the mode control input to set up the shift register to load in parallel. Second, a load pulse must be sent to the input called Clock #2 to load data in parallel. After that load pulse occurs, the mode control goes back to a zero, and twenty-four pulses are sent to send a command, and re-circulate the data. See Figure 9 for timing relationships of these signals.

Automatic Sequencer

This block is the heart of the test. It is the circuit that, when commands are being automatically cycled, tells the rest of the test set what to do. The format of this circuit is a Moore-type sequential machine, described in Figure 10. The state diagram fairly well describes the circuit, but there are a few functions that are not covered. The Automatic Sequencer is turned on and off with a synchronized level from the test control. Once turned on, the test is started and stopped by again "anding" the clock with a synchronized level. In the Totalize Errors mode, the sequential machine works normally. However, in the Stop

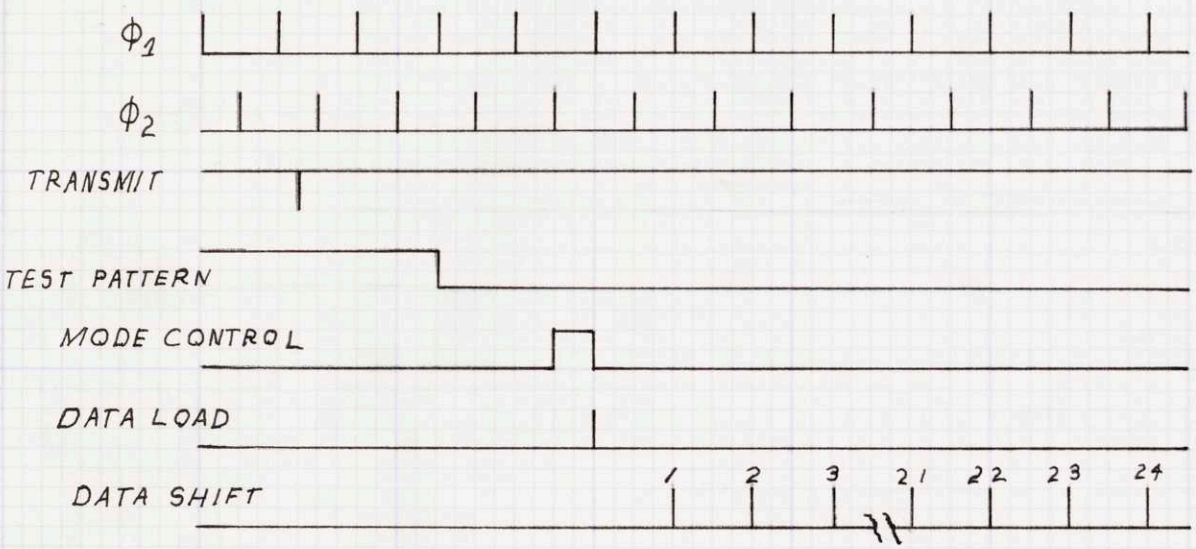
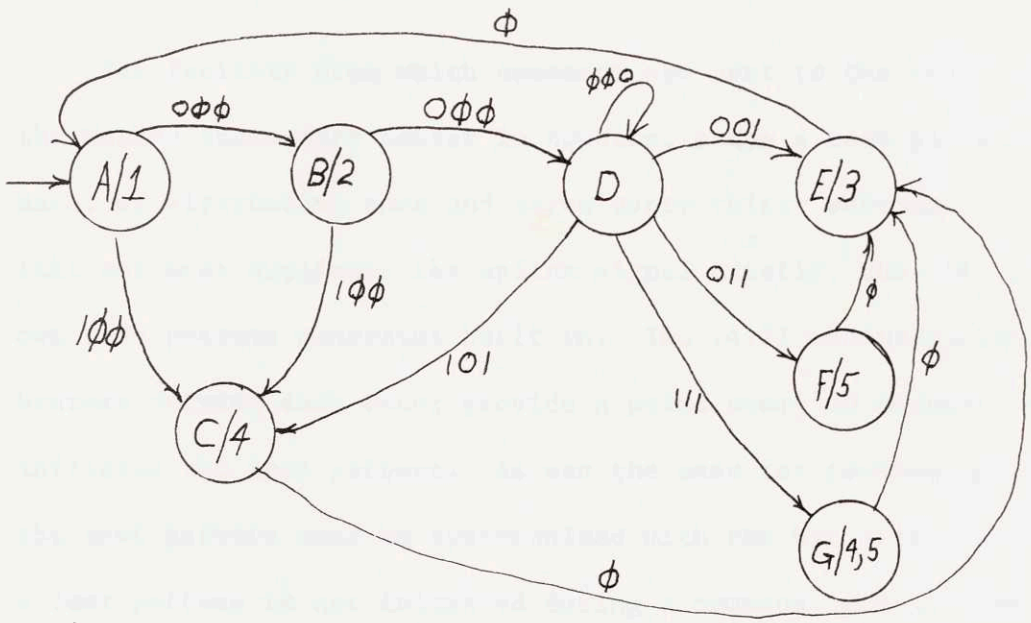


FIGURE 9 COMMAND TRANSMISSION TIMING

INPUTS: A = HIT ERROR
B = MISS ERROR
C = WAIT PERIOD COMPLETE

OUTPUTS: 1 = INCREMENT CYCLE COUNTERS
2 = TRANSMIT COMMAND
3 = CLEAR COMPARATORS
4 = HIT ERROR
5 = MISS ERROR



STATE	$Q_1\ Q_2\ Q_3$
A	0 0 0
B	0 0 1
C	0 1 0
D	0 1 1
E	1 0 0
F	1 0 1
G	1 1 0

$$J_1 = Q_2\,\bar{Q}_3 + \bar{A}\,C\,Q_2 + B\,C\,Q_2$$
$$K_1 = \bar{Q}_2\,\bar{Q}_3 + A\,\bar{B}\,\bar{C}\,\bar{Q}_2$$

$$J_2 = A\,\bar{Q}_1 + \bar{Q}_1\,Q_3 + Q_2$$
$$K_2 = Q_2\,\bar{Q}_3 + \bar{A}\,C$$

$$J_3 = \bar{A}\,\bar{Q}_1\,\bar{Q}_2$$
$$K_3 = Q_1 + A\,\bar{Q}_2 + \bar{A}\,\bar{B}\,C\,Q_2 + A\,C$$

FIG. 10 - AUTOMATIC SEQUENCER STATE DIAGRAM

on Error mode, the clock to the machine is turned off when the machine reaches a state which indicates that an error has been received. In this case, the machine continues when the flip-flops are directly set to the "Clear Comparators" state by the "Automatic Continue" front panel pushbutton.

Test Pattern Generator

The facility from which commands are sent to the lunar surface, the Manned Spacecraft Center in Houston, sends a test pattern of 40 msec. of alternating ones and zeros every thirty seconds. Since the test set must duplicate the uplink signal exactly, the test set has its own test pattern generator built in. Two 74121 monostable multivibrators driving each other provide a pulse every 30 seconds that initiates the test pattern. As was the case for command generation, the test pattern must be synchronized with the bit stream such that 1) a test pattern is not initiated during a command, and 2) every bit lasts a full millisecond. The first is accomplished by storing the 30 sec. pulse if it comes while a command is in progress. The second is accomplished by synchronizing the 30 second pulse with the main clock. The generator itself is a mod-forty counter which produces a synchronized level that goes high for forty milliseconds and gates the test pattern on the line.

Idle Bit Generator

This block is combinational logic which gates a one or a zero on the line whenever a command or a test pattern is not being sent.

Parity Generator

In the Command Decoder, parity has nothing to do with an odd or even number of ones. Good parity means that the seven parity bits are the exact complement of the seven command bits just received. In addition to simply generating the command complement, the test set must know when to send bad parity. There are two reasons for this. First, commands with bad parity must be sent to ensure that they will not be executed. Second, there are three commands, octal 003, 005, and 011, which, if executed during automatic cycling, will put the Command Decoder into an undesirable mode. In this mode the Command Decoder is inactive and no tests can be performed. During automatic cycling, then, these commands are detected and bad parity is generated.

In terms of hardware, parity is generated by exclusive or'ing the seven command bits with parity control lines. Six of these lines are controlled with internal toggle switches. The remaining line is controlled by the front panel "Set Parity Error" pushbutton, or the gates which detect the undesirable commands.

Downlink Clock

The downlink clock serves two purposes. First it supplies the timing signals that the Command Decoder would normally receive from the Data Processor, and second, it furnishes the transmit timing to the Command Generator.

The Command Decoder needs five timing signals from the Data Processor; a square wave clock at 1060 BPS, called SLIZN, used to shift out the Command Verification Word, a line that is a logical one during word seven of the downlink frame to tell the Command Decoder when to send the CVW, called DDIZP, another phase of the 1060 clock at 1/8 duty cycle, called CWEZP, a pulse during bit one of word one of every ninetieth frame mark, and a level that is a zero during word three of every frame, called THRZN. In addition to these, the test set itself uses a pulse during bit one of word eight, and a pulse during bit one of word nine. Refer to Figure 11 for the timing of these signals.

These signals are generated as follows. The timing signals are derived from a basic 8.480 KHz oscillator, which is divided down to the various phases of 1060 BPS by a 4-bit twisted ring counter. The twisted ring counter was chosen because of its ease of decoding and "glitch" free operation. From this twisted ring counter, SLIZN and CWEZP can be decoded directly. The rest of the needed signals need further division of the 1060 BPS clock. For reasons that will become clear later, the bit and word counters used here are BCD, counting bits one through ten,

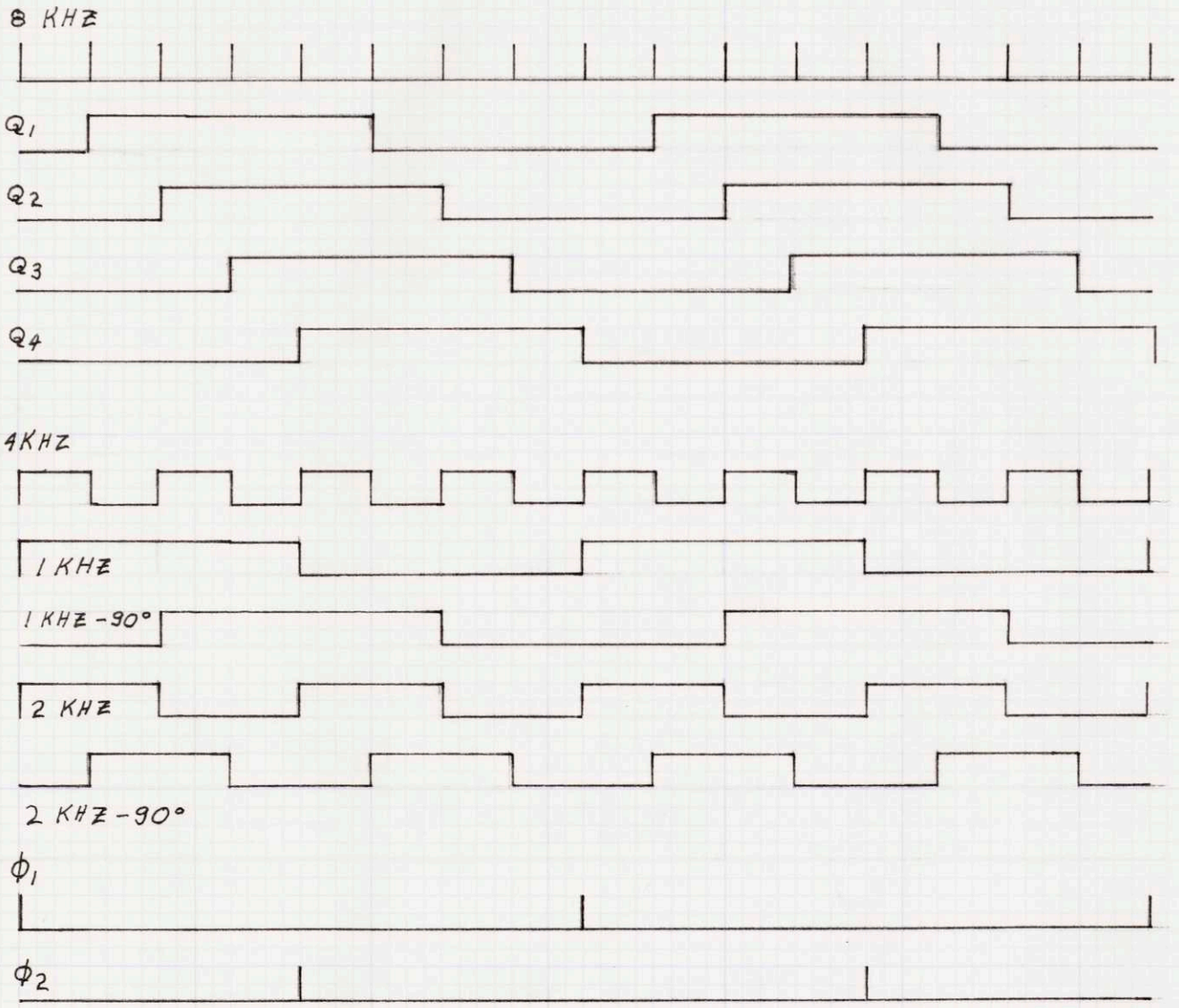


FIG. 11 UPLINK CLOCK SIGNALS

and words one through sixty-four in BCD. These counters are run off still another phase of the 1060 clock called BCP, or "Bit Counter Pulses." The bit counter is a T.I. type SN74192 synchronous decade counter. However, since the bits count one through ten instead of zero through nine, external decoding is necessary to generate a carry pulse in the all zero state rather than in state nine.

These carry pulses are fed to the BCD one through sixty-four word counter. This counter uses two T.I. type SN74192's with external logic to produce a count of one through sixty-four. See Figure 16 in Appendix B.

Five words are decoded off the word counter; words one, three, seven, eight, and nine. Word one is decoded to produce the ninetieth frame mark, word seven is decoded to produce the Data Demand (DDI) for the Command Decoder, word eight is used to load the Command Verification Word Register, and word nine is used by the Automatic Sequencer to determine the wait period.

The Command Decoder gives the Data Processor, or the test set's downlink Clock a one on a line called VWEZP to request a DDI to send a CVW. This one is combined with word seven and a pulse during bit one and sets an S-R flip-flop to form the Data Demand. This flip-flop is reset during bit one of word eight, forming a demand signal with the right timing relative to SLIZN and CWEZP.

The final timing signal needed by the Command Decoder, the ninetieth frame mark, is generated by dividing pulses occurring during bit one of word one by ninety using two 74192's in Mod-90.

Transmit Timing

The transmit timing pulses are generated by comparing a standard with the BCD bit and word counters. That standard comes from one of two sources; either front panel thumbwheels, or cycle counters. A parallel comparison of the eleven bits is done by 'exclusive or'ing' the complement of the standard with the eleven bits of the Bit and Word counters, and "anding" the "exclusive or" outputs with CWEZP. The resulting output is a pulse which occurs during the bit and word contained in the standard being used. The thumbwheels are self-explanatory, and the bit and word cycle counters are identical to the bit and word counters, except that the word cycle counter is driven by the increment cycle counters signal from the Automatic Sequencer. The Bit Cycle Counter is also driven by the increment cycle counters pulse, except when both bit and word are being cycled. In that case, the bit counter is incremented when the word cycle counter changes from 64 to 01. At this point the reason for using BCD Bit and Word counters should be clear; BCD is used so that the desired Bit and Word can be set up on the front panel in decimal rather than binary or octal, and the state of the cycle counters can be displayed directly in decimal, without conversion.

CVW Register

The CVW register is actually two registers; a ten bit Shift Register which receives the CVW serially from the Command Decoder, and a register of latches which stores that CVW. Those latches are loaded

by the word eight pulse from the downlink clock when a CVW has been received. Reception of a CVW is indicated by a one anywhere in the CVW shift register.

A few comments on the CVW register are needed. With the present design of the Command Decoder being what it is, two registers, a shift Register, and a Buffer, are not necessary. One register would have done as well. There are two registers because the design of the test set was done at a time when the Command Decoder sent a Command Verification Word every frame, whether a command had been received or not. In that case a CVW of all zeros was sent when a command had not been received. The design of the CVW Register reflects that fact, in that it distinguished between a real CVW, and a meaningless one (all zeros).

CVW Comparator

The CVW comparator is seven exclusive-or gates whose inputs are the complement of the CVW Received, and the command, as sent by the Command Register. The outputs of these exclusive-or gates are combined with the Address 151 information to generate CVW Hit and Miss error signals. A Hit error is generated when a wrong CVW is received, and a Miss error is generated when an expected CVW is not received.

Command Decoding Gates

This block is an array of combinational logic used to decode the seven bits of command into 104 discrete command lines. These discrete command lines are then compared with the command lines out of the Command Decoder in the Command Error Detectors.

The decoding is done in two levels. The first level consists of 24 four input gates which decode four bits apiece. These drive 104 two-input gates which decode the discrete commands.

Command Error Detectors

This block contains 104 identical circuits which perform the functions of storing a received command, and comparing that received command with the output of the test set decoding gates. Like the CVW Comparator, these error detectors generate Hit or Miss errors. These Hit or Miss signals are "or'ed" iteratively by each detector, so the error detector for the last command indicates a Hit or Miss error on any command line. The error detectors also display on the front panel which command was received.

The detailed logic implementation of each of the blocks discussed above are presented for completeness in Appendix B. They are arranged in order of discussion and are labelled appropriately.

CHAPTER VI

OPERATOR INTERFACE

The design of the front panel (Figure 12) was done with the desire to make the operation of the test set as easy and straightforward as possible. With this in mind, illuminated legend push-button switches were chosen for control switches, and Mini-Lever thumbwheels were chosen for Address, Command, Bit, and Word selection. These eliminate row upon row of hard to comprehend toggle or rotary switches. Also, digital numeric readouts were chosen for displays to eliminate long rows of single light bulbs. The exception to this is the Command Execution display, which would be impractical to display numerically.

The push-buttons were grouped carefully so that switches pertaining to each mode of operation were grouped together. Specifically, push-buttons which are common to both modes are in the top row, push-buttons for the Word Error Test are in the next row, and push-buttons for the Bit Error Test are in the third row down. The bottom row of switches are used when single cards from the Command Decoder are tested separately, and are not used when it is being tested as an assembled unit.

There are two advantages to using illuminated push-button switches. First, they save panel space by performing the dual function of controlling and displaying the status of the logic, and, second, since the lights are controlled by the logic, and not by the switch contacts directly, they provide feedback to the operator, showing him that the logic did in fact respond to the control.

For a listing of the functions of the controls, see Table 1.

FIGURE 12

OPERATOR CONTROL INTERFACE

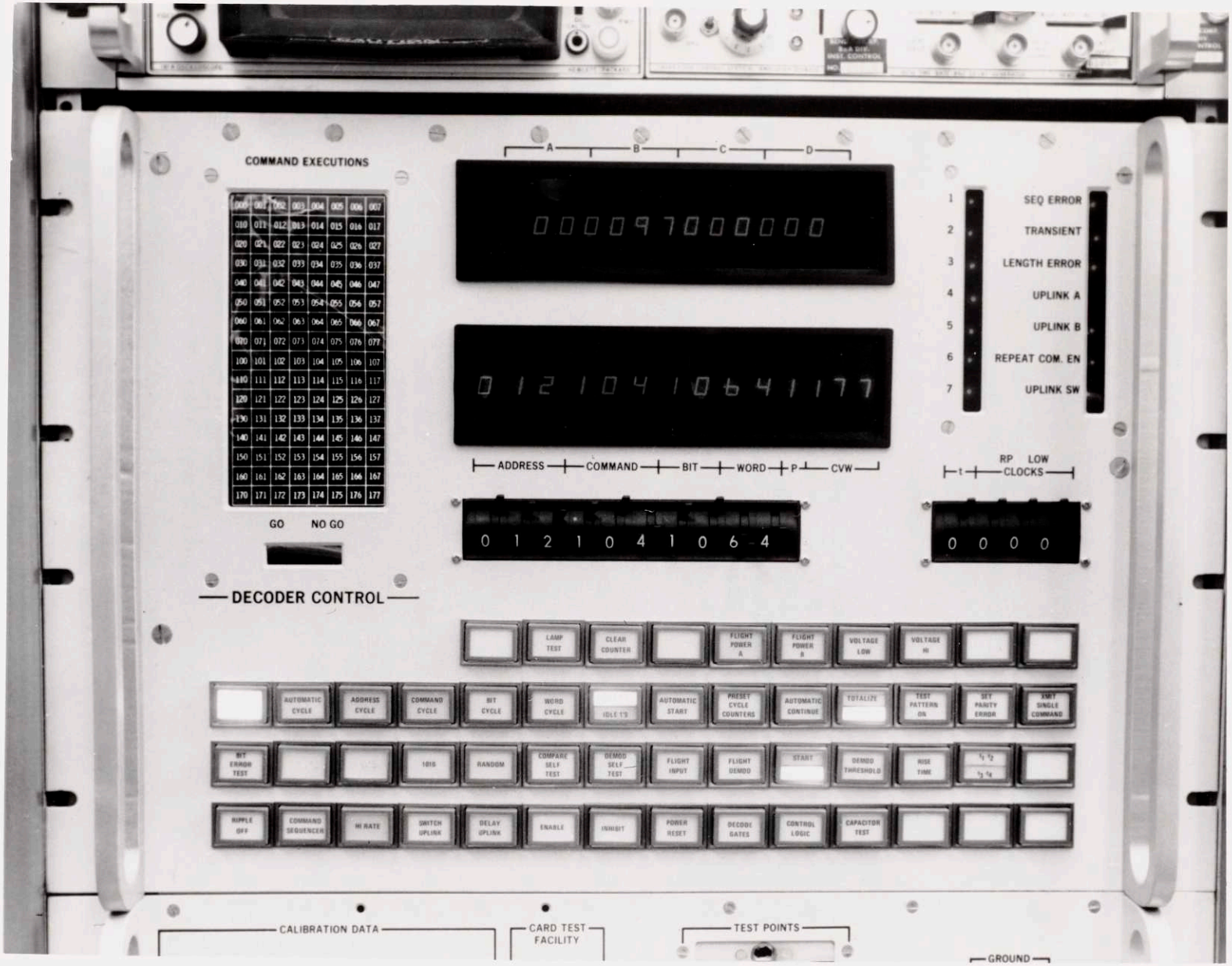

COMMAND EXECUTIONS
GO
NO GO
DECODER CONTROL
A
B
C
D
ADDRESS
COMMAND
BIT
WORD
P
CVW
0 1 2 1 0 4 1 0 6 4
RP LOW
CLOCKS
0 0 0 0
1 SEQ ERROR
2 TRANSIENT
3 LENGTH ERROR
4 UPLINK A
5 UPLINK B
6 REPEAT COM. EN
7 UPLINK SW
LAMP TEST
CLEAR COUNTER
FLIGHT POWER A
FLIGHT POWER B
VOLTAGE LOW
VOLTAGE HI
AUTOMATIC CYCLE
ADDRESS CYCLE
COMMAND CYCLE
BIT CYCLE
WORD CYCLE
IDLE '0'
AUTOMATIC START
PRESET CYCLE COUNTERS
AUTOMATIC CONTINUE
TOTALIZE
TEST PATTERN ON
SET PARITY ERROR
XMIT SINGLE COMMAND
BIT ERROR TEST
1010
RANDOM
COMPARE SELF TEST
DEMOD SELF TEST
FLIGHT INPUT
FLIGHT DEMOD
START
DEMOD THRESHOLD
RISE TIME
RIPPLE OFF
COMMAND SEQUENCER
HI RATE
SWITCH UPLINK
DELAY UPLINK
ENABLE
INHIBIT
POWER RESET
DECODE GATES
CONTROL LOGIC
CAPACITOR TEST
CALIBRATION DATA
CARD TEST FACILITY
TEST POINTS
GROUND

TABLE 1

Operator Control Functions

Control	Function
LAMP TEST	Momentary action -- Illuminates all light bulbs and all segments of the readouts
CLEAR COUNTER	Resets counters A, B, C, and D to Zero
FLIGHT POWER A FLIGHT POWER B	These two controls control power to redundant sides of the V.V.T. They are wired such that pushing one will light the one pushed, and, if the other is lighted, it will be extinguished. If the illuminated one is pushed, it will go out. In any case, it is impossible to turn both on.
VOLTAGE HI VOLTAGE LO	These operate similar to the flight power switches.
WORD ERROR TEST	Puts T.S. into the W.E.M.
AUTOMATIC CYCLE	Puts the T.S. into the A.C. mode.
ADR CMD BIT WRD	These switches select which variables will be cycled.
IDLE 1's IDLE 0's	Selects the idling state of the CMD OPT Line.
AUTO START	Starts automatic cycling.

TABLE 1 (Continued)

Control	Function
CONTINUE	When the Automatic Sequence is in the "Stop on Error" mode, this button will light when the A.S. has stopped on an error. Depressing this switch, then, will restore cycling from where it stopped.
STOP TOTALIZE	This switch selects the mode that the A.S. is in.
TEST PATTERN ON	Enables or inhibits the test pattern generator.
SET PARITY ERROR	Causes one parity bit in the command word to be wrong.
TRANSMIT SINGLE CMD.	One command will be sent each time this button is pressed.
BIT ERROR TEST	Selects the bit error mode.
ONES ZEROS 1010... RANDOM	These interlocked switches select the bit pattern to be sent.
COMPARE SELF TEST	Enables the Error Generator, so the comparator can be checked.
DEMOD SELF CHECK	Checks the demodulator interval to this test set by looking at its output and enabling the error generator.

TABLE 1 (Continued)

Control	Function
FLIGHT INPUT	Switches the internal demod to look at the flight demods input to verify a good data at the input.
FLIGHT DEMOD	Switches the comparator to the output of the flight demod.
	NOTE: D.S.C., F.I. and F.D. are interlocked so that only one is on at a time. C.S.T. is not and overrides the others.
	The rest of the switches are not relevant to the Unit test.

CHAPTER VII

CONCLUSION

The Apollo Mission is a NASA project designed to soft-land astronauts on the Moon for exploration and the deployment of scientific instruments. The first of seven such missions landed in July, 1969, and the last is scheduled to land in July, 1972.

The scientific instruments that the astronauts deploy are contained in a package called the Apollo Lunar Surface Experiment Package, or Alsep. These experiments are controlled by radio from Earth, and are designed to collect and transmit to Earth scientific data about the lunar environment. Commands to the package are transmitted from Earth, and, after being received by the package, are decoded and executed by a Command Decoder.

For all landings except the last, Apollo 17, the Alsep is designed to last one year on the lunar surface. For the last flight, though, the package is being completely redesigned for a life of two or more years on the Moon.

To meet this requirement, the package must be completely tested on all levels. The testing at the module level is done by automatic test sets for each module. The Command Decoder Test Set described here is one of those automatic test sets.

The design of the test set began in October, 1970, and actual construction began in January, 1971. Construction is now complete, and the test set is presently being used for design verification testing.

The test set is housed in a two-bay shielded enclosure and stands approximately six feet tall. In addition to the control logic described here, the test set contains power supplies necessary to power the flight hardware and test set logic, a modulator and demodulator to interface with the Command Decoder, and commercial test equipment for trouble-shooting.

During trouble-shooting of the test set logic, no major electrical problems were encountered. However, construction of the display portion of the front panel presented a mechanical problem. Because of the constraint on the number of I/O connections available on a logic card, the decoder/drivers for the numeric readouts were mounted behind the front panel, saving three connections/digit. This presented problems, though, since that meant that the current limiting-resistors had to be there also. This meant that 310 resistors had to be mounted behind the front panel, as the drivers for the Execution Display were mounted there, too. The problem was solved by using a larger piece of perforated board to accommodate the resistors. A better solution would have been to use readouts with the decoder/drivers built in.

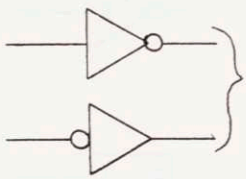
After the DVT, which is in progress at this time, there will then be a period of approximately four months for modifications to the Command Decoder, and to the test set. Qualification testing, then, is scheduled to begin in September, and will run until about December, 1971. The actual unit that will be flown will then be manufactured, and

testing on the flight model will begin in February, 1972. The test set described here will be used for all these tests. After this final component level test, the whole package is integrated into a complete system and tested. Upon completion of the system test, the Alsep package will be delivered to Cape Kennedy for launch in July, 1972.

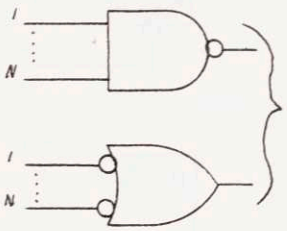
APPENDIX A

FIGURE 13: LOGIC SYMBOL DEFINITIONS

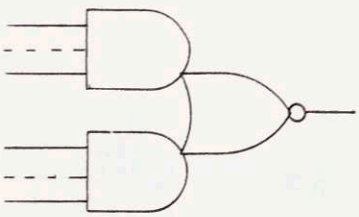
APPENDIX A



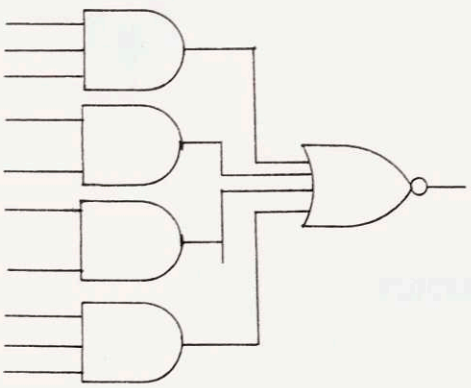
INVERTER; T.I. TYPE SN74L04



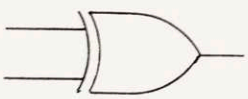
N INPUT NAND GATE; 2-INPUT - T.I. TYPE SN74L00
3-INPUT - T.I. TYPE SN74L10
4-INPUT - T.I. TYPE SN74L20
8 INPUT - T.I. TYPE SN74L30



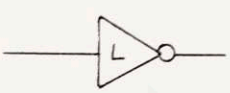
2-WIDE, 2 INPUT AND-OR-INVERT GATE;
T.I. TYPE SN74L51



4-WIDE, 3-2-2-3 INPUT AND-OR-INVERT
GATE; T.I. TYPE SN74L54

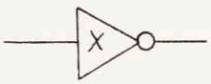


TWO INPUT EXCLUSIVE-OR GATE,
T.I. TYPE SN74L86

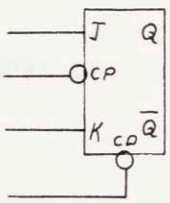


DRIVER FOR EXECUTION DISPLAY,
T.I. TYPE SN7416

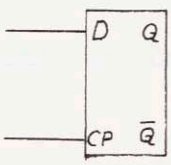
FIG. 13 LOGIC SYMBOL DEFINITIONS



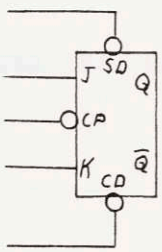
DRIVER FOR LAMPS IN PUSHBUTTONS;
NATIONAL SEMICONDUCTOR TYPE NH0017



J-K FLIP FLOP; T.I. TYPE SN74L73



D-TYPE FLIP FLOP; T.I. TYPE SN74L74



J-K FLIP FLOP; T.I. TYPE SN74L78

FIGURE 13 (Continued)

APPENDIX B

FIGURE 14: BIT ERROR TEST CONTROL, UPLINK CLOCK, TEST PATTERN & IDLE BIT GENERATOR, CVW REGISTER AND COMPARATOR

FIGURE 15: AUTOMATIC SEQUENCER

FIGURE 16: DOWNLINK CLOCK, BIT & WORD COUNTERS, BIT & WORD CYCLE COUNTERS

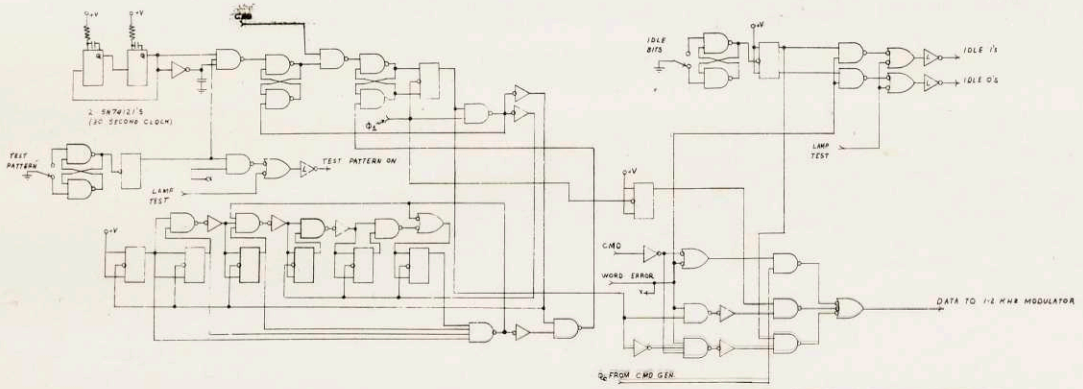
FIGURE 17: COMMAND DECODING GATES

FIGURE 18: COMMAND ERROR DETECTORS

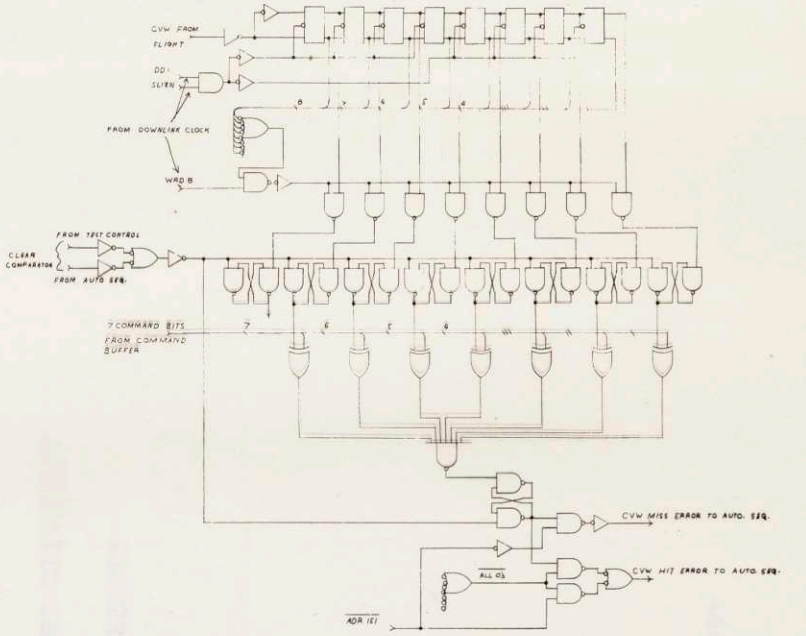
FIGURE 14

BIT ERROR TEST CONTROL, UPLINK CLOCK, TEST PATTERN

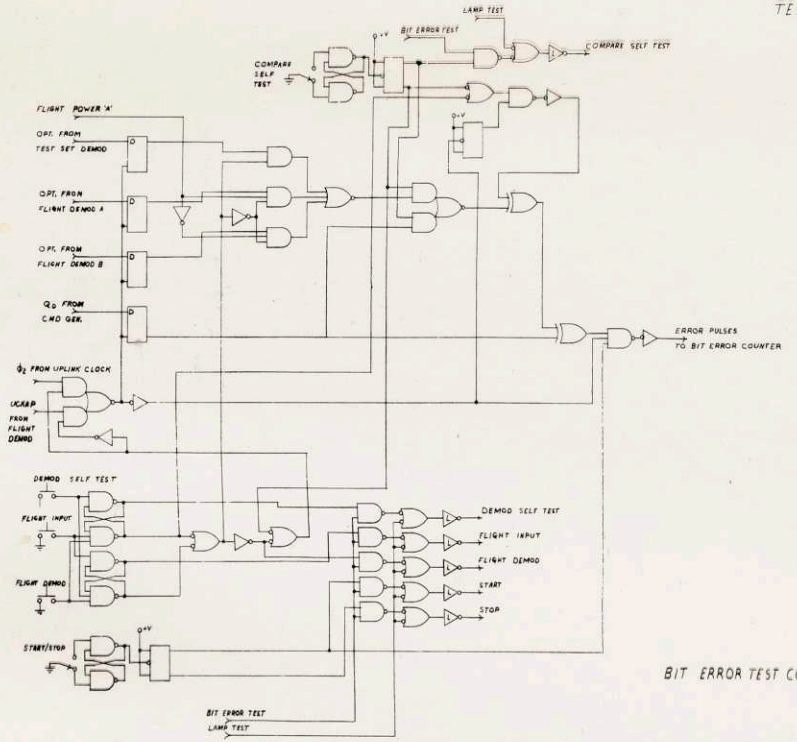
& IDLE BIT GENERATOR, CVW REGISTER AND COMPARATOR



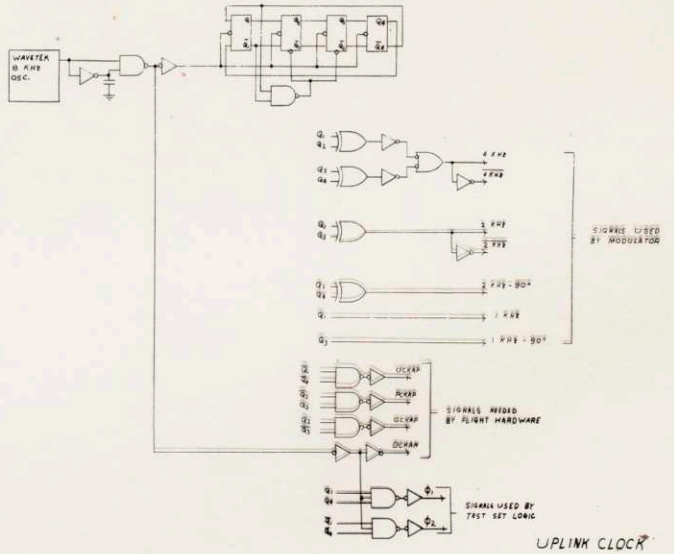
TEST PATTERN & IDLE BIT GENERATOR



CVW REGISTER & COMPARATOR



BIT ERROR TEST CONTROL



UPLINK CLOCK

FIGURE 14

FIGURE 15

AUTOMATIC SEQUENCER

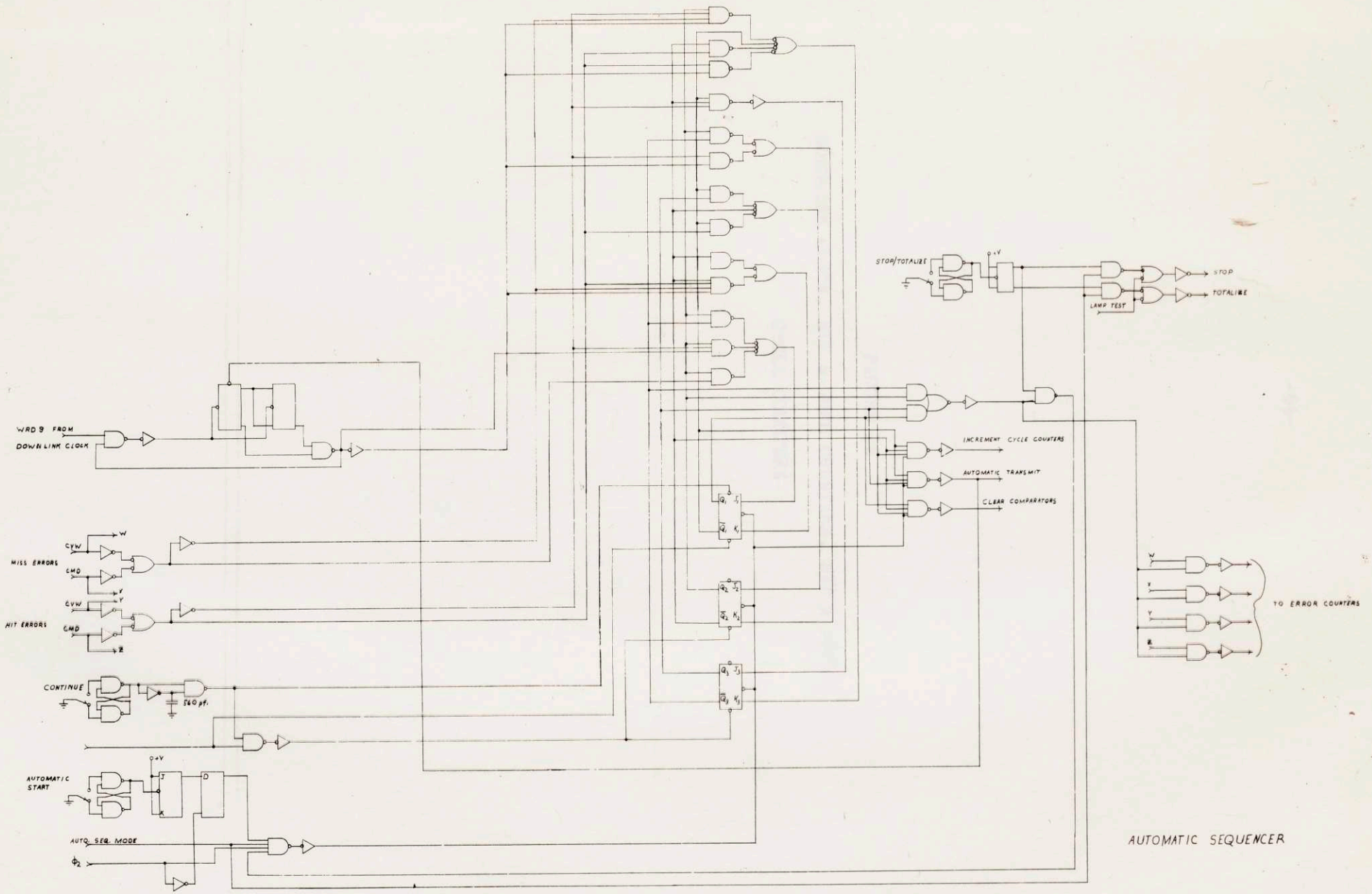

STOP/TOTALIZE
+V
STOP
TOTALIZE
LAMP TEST
WRD 9 FROM
DOWN LINK CLOCK
INCREMENT CYCLE COUNTERS
AUTOMATIC TRANSMIT
CLEAR COMPARATORS
MISS ERRORS
HIT ERRORS
CVW
CMD
W
Y
Z
TO ERROR COUNTERS
CONTINUE
560 pf.
AUTOMATIC START
AUTO. SEQ. MODE
AUTOMATIC SEQUENCER

FIGURE 15

FIGURE 16

DOWNLINK CLOCK, BIT & WORD COUNTERS, BIT & WORD CYCLE COUNTERS

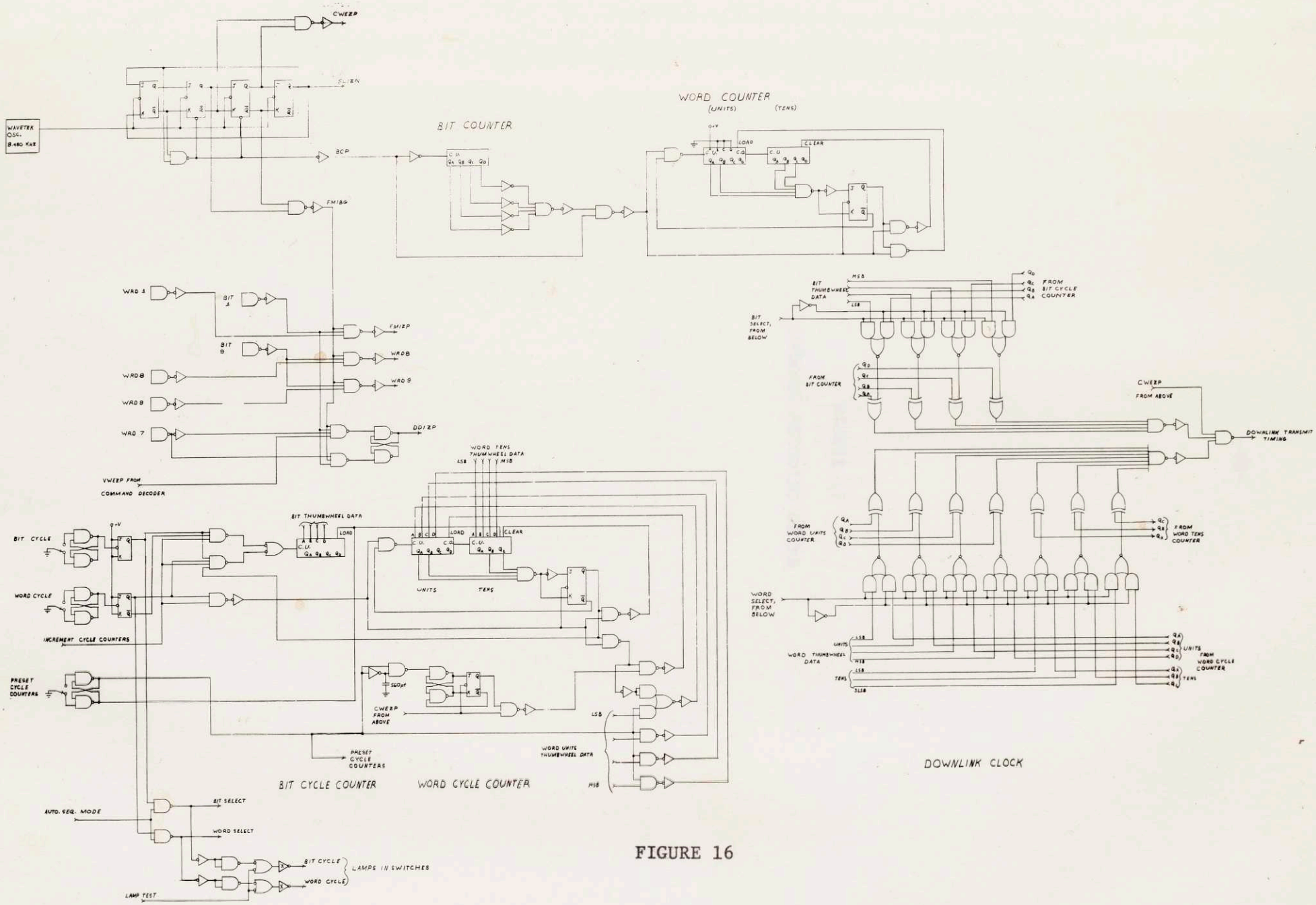

CWEEP
WAVETEK OSC. 8.480 KHz
BCP
FMIBG
BIT COUNTER
WORD COUNTER
(UNITS)
(TENS)
LOAD
CLEAR
WRD 1
BIT 1
BIT 0
WRD 0
WRD 8
WRD 9
WRD 7
FMIZP
DDIZP
VWEEP FROM COMMAND DECODER
BIT THUMBWHEEL DATA
WORD TENS THUMBWHEEL DATA
BIT CYCLE
WORD CYCLE
INCREMENT CYCLE COUNTERS
PRESET CYCLE COUNTERS
UNITS
TENS
CWEEP FROM ABOVE
WORD UNITS THUMBWHEEL DATA
BIT CYCLE COUNTER
WORD CYCLE COUNTER
AUTO. SEQ. MODE
BIT SELECT
WORD SELECT
LAMPS IN SWITCHES
LAMP TEST
FROM BIT CYCLE COUNTER
BIT SELECT, FROM BELOW
FROM BIT COUNTER
DOWNLINK TRANSMIT TIMING
FROM WORD UNITS COUNTER
FROM WORD TENS COUNTER
WORD SELECT, FROM BELOW
WORD THUMBWHEEL DATA
FROM WORD CYCLE COUNTER
DOWNLINK CLOCK

FIGURE 16

FIGURE 17

COMMAND DECODING GATES

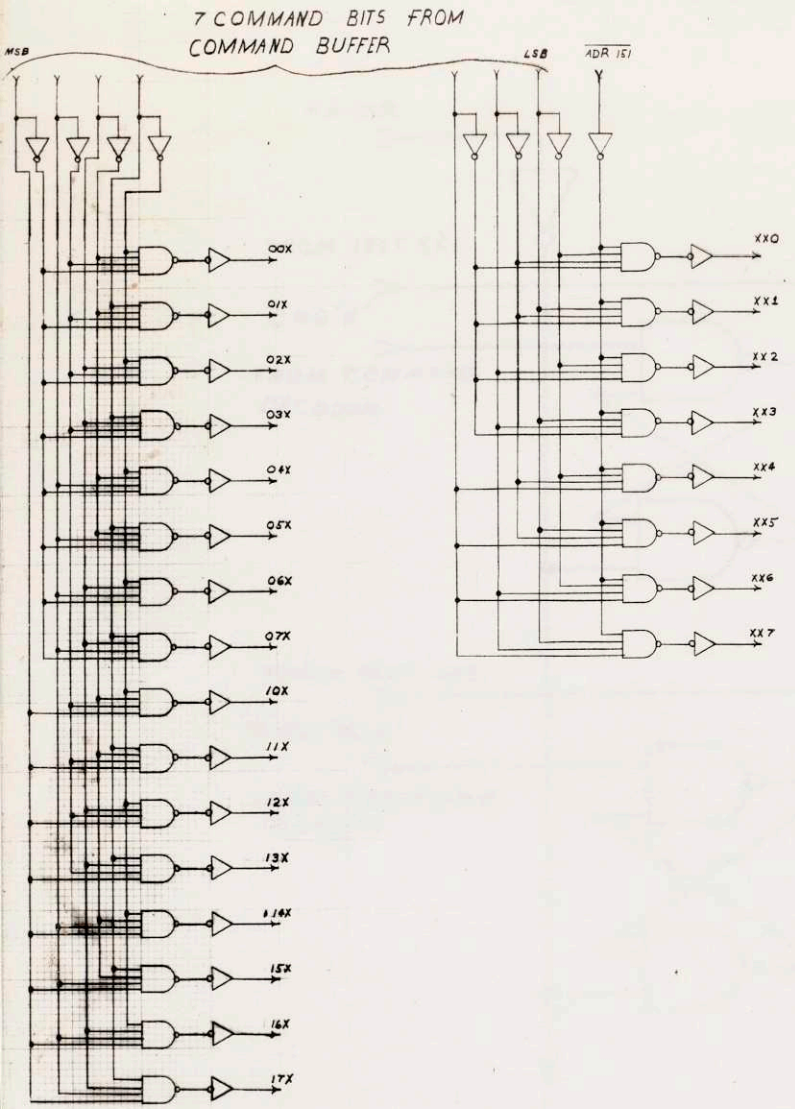
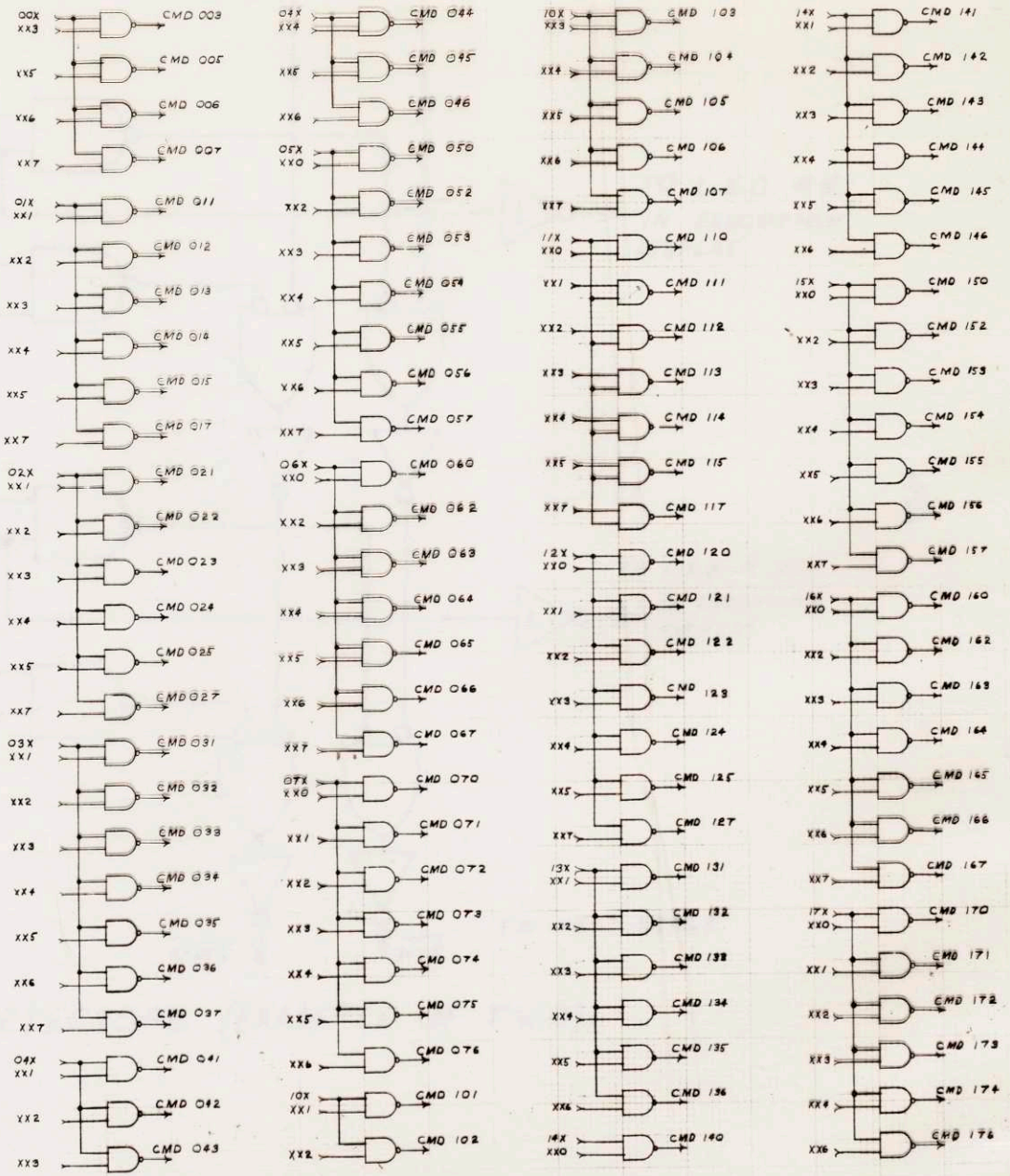


FIGURE 17



COMMAND DECODING GATES

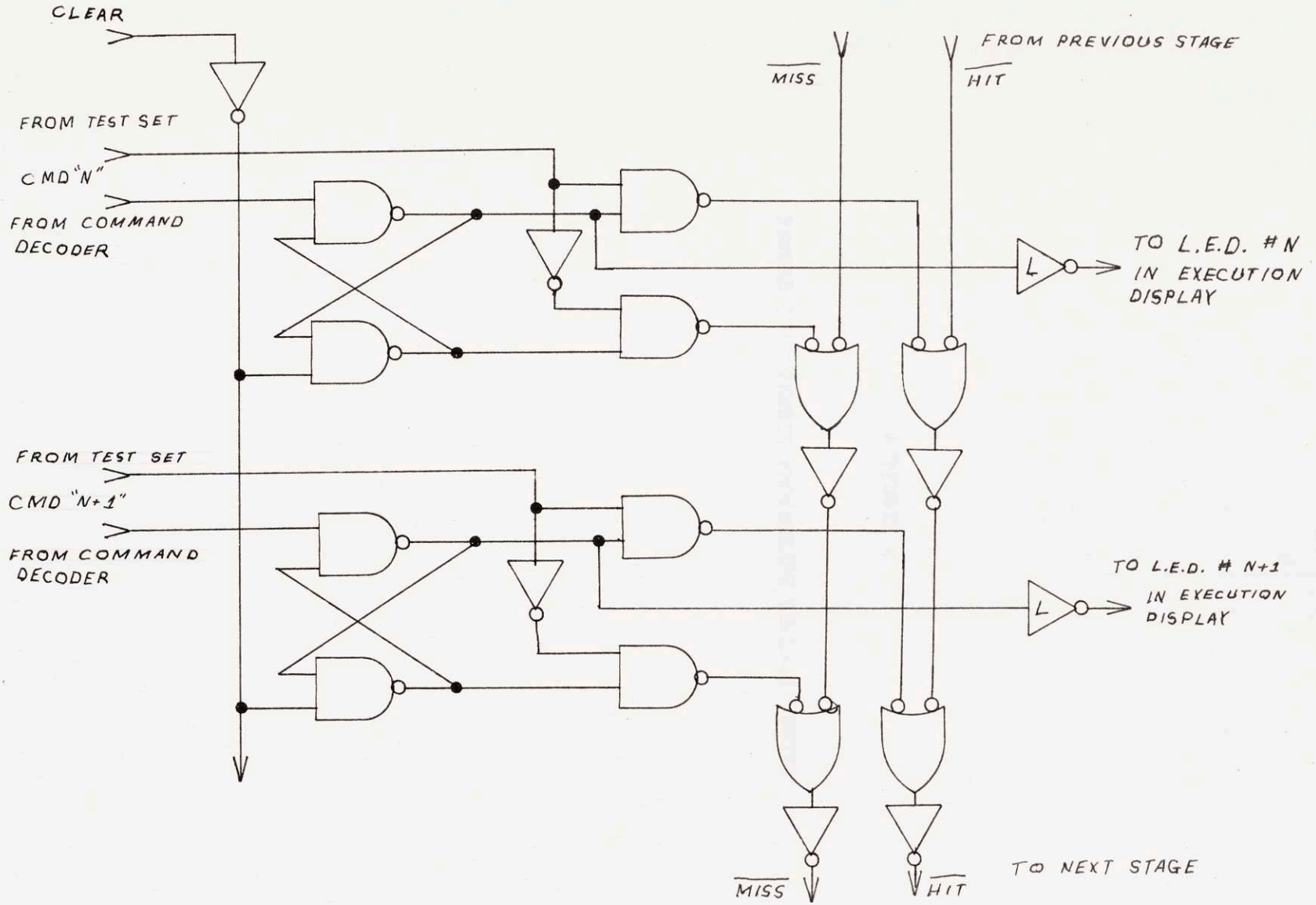


FIG. 18 COMMAND ERROR DETECTORS (EXAMPLE OF TWO)

APPENDIX C

FIGURE 19: BENDIX PHOTOGRAPH RELEASE LETTER

Bendix
Aerospace
Systems Division

3300 Plymouth Road
Ann Arbor, Michigan 48107
Tel (313) 665-7766
The Bendix Corporation

Mr. P. M. Grahek
1811 Village Green
Ann Arbor, Michigan

May 11, 1971

Dear Mr. Grahek:

The following ALSEP Program photographs are available to you for use in your thesis:

2887	22727
22170	22728
22171	22729
22134	

It is suggested that an acknowledgement for their use in respect to Bendix Aerospace Systems Division and NASA should be included in your thesis.

Sincerely,

G. A. Cripps
ALSEP Test Set Design Supervisor

GAC/as

FIGURE 19

BENDIX PHOTOGRAPH RELEASE LETTER

Bendix
Aerospace
Systems Division

3300 Plymouth Road
Ann Arbor, Michigan 48107
Tel (313) 665-7766
The Bendix Corporation

Mr. P. M. Grahek
1811 Village Green
Ann Arbor, Michigan

May 11, 1971

Dear Mr. Grahek:

The following ALSEP Program photographs are available to you for use in your thesis:

2887	22727
22170	22728
22171	22729
22134	

It is suggested that an acknowledgement for their use in respect to Bendix Aerospace Systems Division and NASA should be included in your thesis.

Sincerely,

Signature redacted

G. A. Cripps
ALSEP Test Set Design Supervisor

GAC/as

FIGURE 19

BENDIX PHOTOGRAPH RELEASE LETTER