Ultra-Miniaturized, Secure Wake-Up Receiver Based on THz Carrier Wave

by

Eunseok Lee

B.S., Korea Advanced Institute of Science and Technology (2020)

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Master of Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

February 2023

Author .....
Department of Electrical Engineering and Computer Science
January 25, 2023

Certified by .....
Anantha P. Chandrakasan
Vannevar Bush Professor of Electrical Engineering and Computer Science
Thesis Supervisor

Certified by .....
Ruonan Han
Associate Professor of Electrical Engineering and Computer Science
Thesis Supervisor

Accepted by .....
Leslie A. Kolodziejski
Professor of Electrical Engineering and Computer Science
Chair, Department Committee on Graduate Students

Ultra-Miniaturized, Secure Wake-Up Receiver Based on THz Carrier Wave

by

Eunseok Lee

Submitted to the Department of Electrical Engineering and Computer Science
on January 25, 2023, in partial fulfillment of the
requirements for the degree of
Master of Science

Abstract

Devices have become smaller over the last few decades, and billions of devices are estimated to be connected in the 2030s. Researchers are developing small-scale, massively deployable wireless nodes for various applications that can work together to collect information and build large networks. These miniaturized wireless nodes require various functionalities, including communication, sensing, actuation, and energy harvesting. There is a growing need for the development of mm^2 sized wake-up receivers to prolong the battery life on these devices. The mm-wave/THz spectrum is a promising candidate for millimeter-scale wake-up receiver designs as it is compatible with on-chip antenna integration.

A prototype wake-up receiver using THz carrier wave was fabricated using TSMC 65nm technology. The wake-up receiver, which includes on-chip integrated patch antennas, captures the THz signal, which is then rectified and passed through amplifier-filter stages and digitized by a comparator. It authenticates wake-up patterns, generates wake-up signals, and updates the cryptographically randomized tokens. The system operates at 0.8 V and consumes 2.88 μW, with a sensitivity of -48 dBm at a data rate of 1.02 kbps. Power consumption can be reduced to 750 nW with within-bit duty cycling. The WuRx has been tested at a distance of several meters and paired with a beam-steerable THz reflectarray, demonstrating its potential for real-world applicability.

Thesis Supervisor: Anantha P. Chandrakasan
Title: Vannevar Bush Professor of Electrical Engineering and Computer Science

Thesis Supervisor: Ruonan Han
Title: Associate Professor of Electrical Engineering and Computer Science

Acknowledgments

First and foremost, I would like to express my gratitude to my advisors, Professor Anantha Chandraksan and Professor Ruonan Han, for allowing me to work with their team and consistently supporting my research. Being able to work with both of my advisors was indeed a great honor. Their guidance was invaluable throughout my research.

Besides my advisors, I would like to thank Muhammad Ibrahim Khan for helping me learn simulation tools and setups, brainstorm research directions, and share experiences and tips for the tapeout. Also, thank you for your advice and help even after graduation. I also want to thank Xibi Chen for the research discussions and for sharing electromagnetic intuitions with me. Also, for helps during the measurements. I would like to thank Deniz Umut Yildirim for all our chats and challenges in our unexpected first year due to COVID. In addition, I would like to thank Jinchen Wang for sharing his positive energy with me. I enjoyed our casual research talks in the office. Also, special thanks to Utsav and Professor Rabia Yazicigil for sharing their intuitions on protocol and measurements.

I thank all the members of the Anantha group for sharing their knowledge and experiences. I loved the conversation about our daily lives and research at the office. I also have to thank my labmates in the Ruonan group. Thinking back, spending sleepless nights together before deadlines is a valuable experience. I look forward to our adventures for the remaining study.

I have to thank Irwin Mark Jacobs and Joan Klein Jacobs MIT Presidential Fellowship, and Korea Foundation for Advanced Studies Doctoral Study Abroad Scholarship for financial support during my study.

Last but not least, all of this must be dedicated to my family. My parents have always loved and encouraged my dreams and decisions throughout my life. Thank you for being my family.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Background and Motivation

Over the last few decades, smaller devices, such as smartphones, wearables, and Internet-of-Things (IoT) devices, have become increasingly popular. As a result, researchers have recently been working on developing small-scale, widely deployable wireless sensor nodes for various applications such as agriculture, healthcare, and military purposes. These nodes, in particular, can collaborate to collect information from their environments and build large-scale collaborative networks with minimal intrusion. To achieve this, these miniaturized wireless nodes need diverse functional capabilities, including communication [13], sensing, and energy harvesting [22].

This vision is enabled by devices with low power, miniaturization, and low-cost fabrication. While these nodes have several functional requirements, communication is necessary in most cases. However, communication is typically the most power-hungry part of these wireless nodes [11]. Thus, there has been a growing demand to develop mm^2-sized wake-up receivers (WuRxs) to help conserve the limited battery life of these devices. For instance, these mm^2-sized WuRxs can be incorporated into microbots [6, 5], or nano radios [13] without significant increase of overall device size, reducing total power by allowing the device to sleep in the idle state until activated.

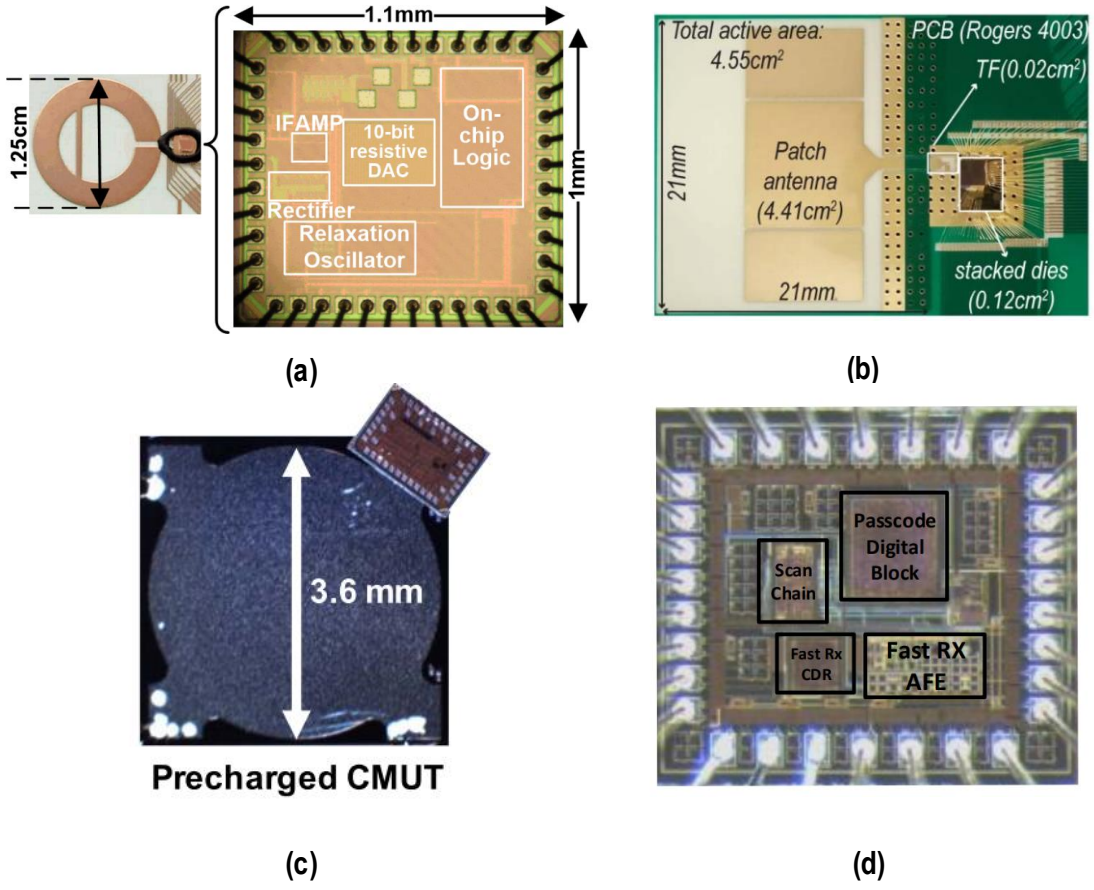


Figure 1-1: Examples of small-scale WuRxs : (a) 1.875 cm^2 2.4GHz WuRx [33], (b) 4.55 cm^2 9 GHZ WuRx [18], (c) 14.5 mm^2 ultrasound WuRx, (d) 0.85 mm^2 optical WuRx

1.1.1 Previous works on WuRx miniaturization

The dimensions of the RF WuRxs are determined by the antenna, which is fundamentally proportionate to the square of the carrier wavelength. Typically, the antenna size of a GHz range WuRx is at cm^2 level [33, 18]. [18] presents a WuRx with a 4.55 cm^2 antenna with a sensitivity of -69.5 dBm at 9 GHz. [33] presents a WuRx with a 1.875 cm^2 antenna that operates at 2.4 GHz and has a sensitivity of -61.5 dBm. In both cases, most of the system area is occupied by the off-chip antenna size. [9] pushes the carrier frequency to 78 GHz and achieves the reduced receiver size of 49 mm^2 with the off-chip antenna, but it requires a high DC power consumption of 25 mW. If the size of the antenna does not comply with the relationship between its size and the wavelength, the antenna gain is drastically reduced and the antenna cannot capture signals anymore.

Other modalities have been investigated to miniaturize the size of WuRxs by reducing the radiator size. [31] presents an ultrasonic WuRx with a size of 14.5 mm^2. This utilizes a precharged capacitive micromachined ultrasonic transducer (CMUT) to capture the ultrasound signal, which relaxes the high DC voltage requirements to drive the transducer. However, this approach still requires an off-chip transducer, limiting the further size reduction and adding the extra packaging cost. [24] introduces the optical WuRx by utilizing integrated photodiodes. This significantly reduces the WuRx size to 0.85 mm^2; however, optical receiver operation is typically susceptible to ambient light interference and has a sensitivity of -30 dBm in low-power mode. The examples of the miniaturized WuRxs are shown in Figure 1-1.

1.1.2 Previous works on mm-Wave/THz systems for miniaturization

The mm-wave/THz spectrum is a potentially good candidate for millimeter-scale WuRx designs due to their compatibility with on-chip antenna integration. Several studies have used mm-wave/THz systems to develop miniaturized IoT devices or wireless tags with on-chip antenna integration [36, 17, 22, 13]. For example, a pad-

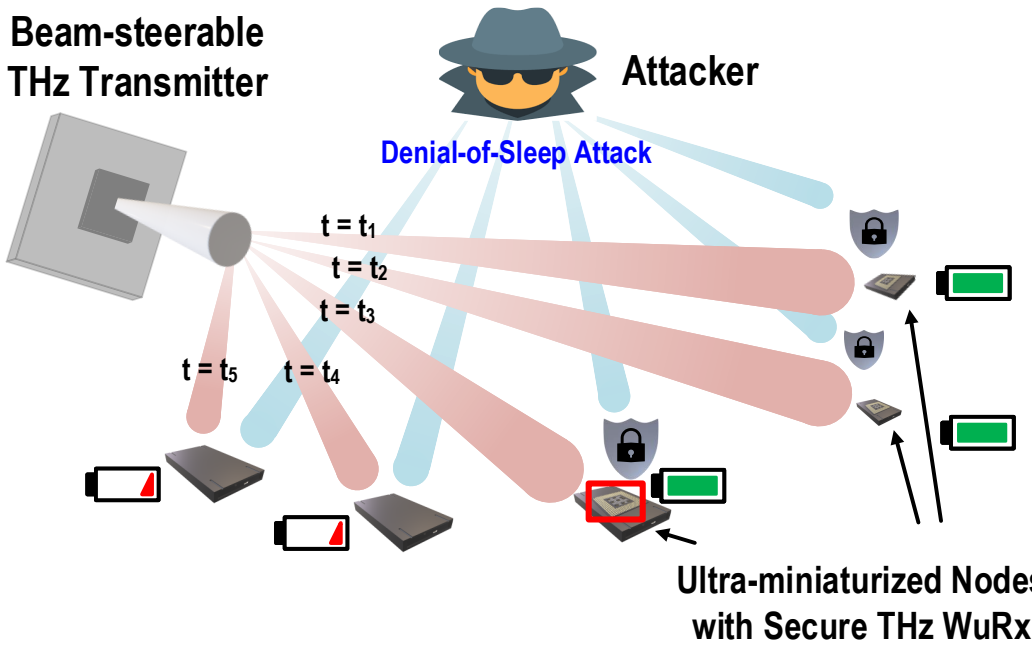


Figure 1-2: Application scenario of the mm^2-sized nodes with secure THz WuRx

less millimeter-sized radio is proposed as a miniaturized self-powered radio for IoT, and wireless tags applications [36] using frequencies at 24 GHz and 60 GHz. [17] demonstrated 1.6 mm^2 size, package-less wireless tags using a 260 GHz carrier wave and photovoltaic harvesting and THz detector/backscattering techniques with integrated authentication. In [22], a 263 GHz CMOS energy harvester is presented for the far-field wireless powering of ultra-miniaturized platforms. This energy harvester could potentially replace photovoltaic harvesting in [17]. In addition, a 150 GHz 2x2 transceiver array is presented [13] for stealth and widely deployable wireless nodes with the Tx DC power consumption of 11.6 mW and the Rx DC power consumption of 10 mW. Hence, exploration of the high mm-Wave/THz spectrum for miniaturized WuRx design should be carried out. However, utilizing a high-frequency spectrum can decrease the sensitivity of the WuRx due to the limited performance of high-frequency signals in transistors, reducing the communication distance. Therefore, evaluation of the real-world applicability of the THz WuRx is essential. The additional factors for THz wake-up design are discussed in Chapter 2.

1.2 Security threat for the ultra-miniaturized platform

Resource-constrained wireless nodes adopt WuRxs to control their sleep and active states to save limited battery energy. The WuRx monitors a communication channel for wake-up tokens sent by the base station and compares the incoming token to a reference token. When the two tokens match, the node activates. This wake-up token is typically predefined and fixed to specific codes in many cases [29].

However, such WuRx systems are susceptible to Denial-of-Sleep (DoSL) attacks. DoSL attack is one of the denial-of-service attacks that prevents wireless nodes from entering low-power idle states. A DoSL attacker can obtain the predefined wake-up message by listening to the communication channel and repeatedly replaying it to the target node. This cause the node to wake up continuously, rapidly draining the battery of the node and shortening its lifetime. This is especially critical for ultra-miniaturized nodes, which only have a small battery size. DoSL attacks can pose a severe threat to the reliability of WuRx-based systems.

The general countermeasure for DoSL attacks is dynamic wake-up tokens that are different and unpredictable for every wake-up [29, 20]. This can be achieved through randomized and unique token generation by cryptographic algorithms. By doing this, wake-up tokens become more challenging for an attacker to obtain or guess, and thus this attack can be effectively prevented. However, currently, there are no WuRx ICs with integrated cryptographic authentication. [16] utilizes cryptographic checksums to improve security, but it can still be monitored easily without dynamic wake-up tokens and are vulnerable to DoSL attacks. To improve the security and reliability of these systems, new circuit techniques and system-level developments need to be explored.

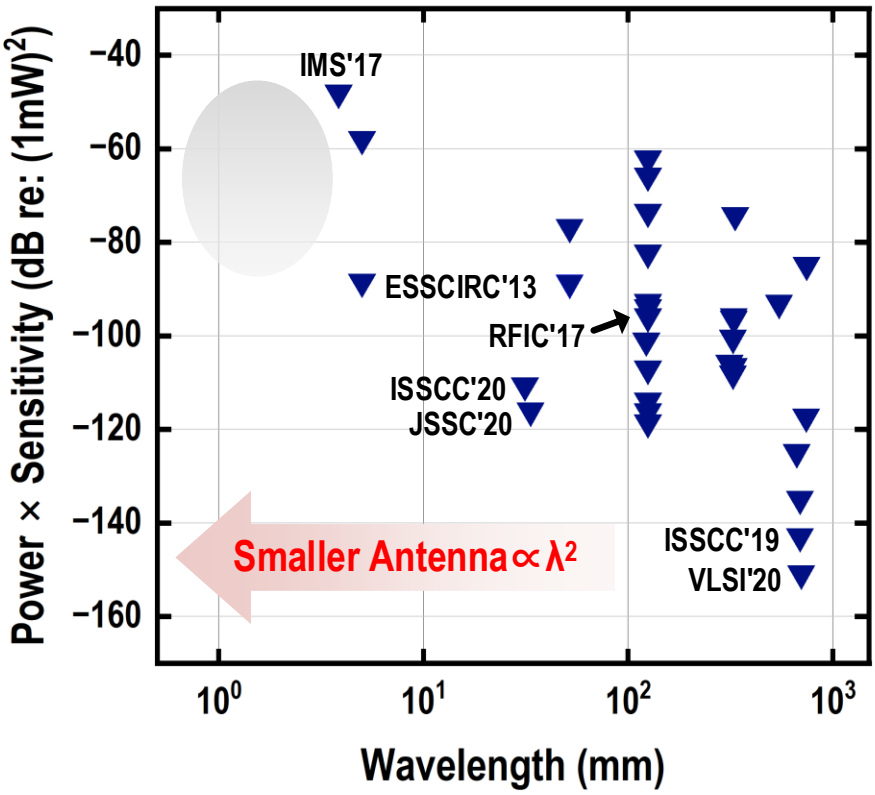


Figure 1-3: Survey of WuRxs in the literature from 2009-2021: Wavelength versus power-sensitivity product of the state-of-the-art WuRxs across frequencies in the RF-to-THz spectrum.

1.3 Thesis goal and contribution

This thesis introduces an mm^2-sized THz WuRx with integrated cryptographic authentication to protect against DOSL attacks for ultra-miniaturized platforms. The application scenario of this WuRx is illustrated in Figure 1-2. A highly directive beam-steerable THz interrogator can send the signals to each node. With the integrated authentication, the node can prevent replay attacks from malicious attackers, saving the battery energy.

Figure 1-3 presents the wavelength versus power-sensitivity product of the state-of-the-art WuRxs across frequencies in the RF-to-THz spectrum based on the literature from 2009-2021. As directly indicated in the graph, a trade-off exists between wavelength and power-sensitivity products. This work explores the trade-off space near the gray region (marked in Figure 1-3) to develop a miniaturized WuRx.

This thesis presents a secure mm^2-sized THz WuRx design for ultra-miniaturized platforms, pushing the boundary of the design trade space and offering a low-cost, fully-integrated solution for WuRx miniaturization. This thesis provides requirements for THz WuRxs, analyzes design considerations, and proposes circuit design techniques for the application scenario depicted in Figure 1-2 with practical demonstrations.

The thesis contributions can be summarized as followings:

1. This thesis presents the first THz WuRx architecture based on pseudo-differential THz detectors with a sensitivity of -48 dBm and power consumption of 2.88 μW.

2. A novel THz detector optimization technique using dual-antenna feeding is presented.

3. To counteract the Denial-of-Sleep attack, dynamic wake-up token generation using lightweight cryptography is implemented.

4. Wireless communication tests at several meters and pairing with beam-steerable THz reflectarray are performed to propose the real user scenario.

This work in the thesis will be published in the future:

- **E. Lee**, M. I. W. Khan, X. Chen, U. Banerjee, N. Monroe, R. Yazicigil, R. Han and A. Chandrakasan, "A 1.54 mm^2 Wake-Up Receiver Based on THz Carrier Wave and Integrated Cryptographic Authentication", IEEE Custom Integrated Circuit Conf. (CICC), San Antonio, TX, April. 2023 (Accepted)

1.4 Thesis outline

Chapter 2 introduces the properties of THz signals, along with how they affect THz WuRx design. Chapter 3 focuses on optimizing and implementing the THz detector for use in the WuRx using a dual-antenna and detector technique. Chapter 4 explores the baseband circuits for the WuRx that are integrated with the THz detectors and presents simulation results. Chapter 5 covers the THz WuRx system-level operation, mainly focused on the ultra-miniaturized platform's security considerations. Chapter 6 analyzes experimental results and analyzes the performance of the THz detector and WuRx. Finally, Chapter 7 summarizes the thesis and discusses potential areas for future research.

Chapter 2

THz for wake-up

This chapter introduces the characteristics of THz signals and their impacts on THz WuRx design and discusses the potential THz WuRx architectures.

2.1 THz consideration

2.1.1 Signal propagation

One of the main challenges in realizing THz wireless communication is the high free space path loss of THz signals, which can significantly limit their communication range.

The received power P_R can be calculated using the Friss transmission equation [12]:

$$P_R = P_T G_T (\frac{\lambda}{4\pi d})^2 G_R, \tag{2.1}$$

where P_T is the Tx output power, G_T is Tx antenna gain in the direction of the receiver, λ is the carrier wavelength, d is the distance between Tx and Rx. The distance versus received power is shown in Figure 2-1, assuming $P_T = 19$ dBm, $G_T = 25$ dBi, $\lambda = 1.132$ mm (corresponding carrier frequency at air = 264 GHz), $G_R = 0$ dBi. To be effective for indoor communication, a THz system should be able to support distances of several meters. For example, at a distance of 5 meters, the required

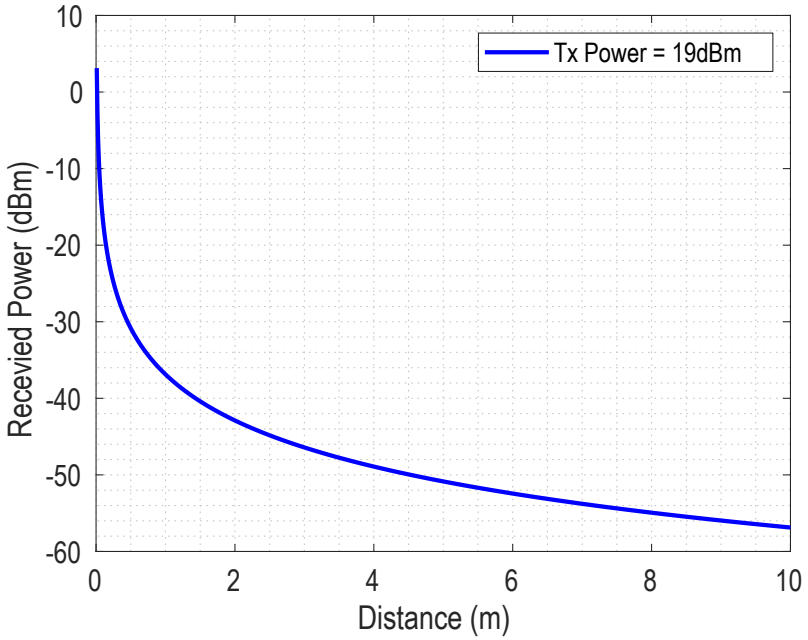


Figure 2-1: THz communication link budget

receiver power is around -50 dBm. This demonstrates that the target sensitivity should be near -50 dBm in order to achieve practical communication distances. An on-chip antenna array at the receiver can potentially increase the received power, but it comes with the trade-off of increased silicon area and manufacturing costs due to the need for additional antennas.

2.1.2 Highly directive THz beam

THz link utilizes highly directional beams from high-gain antennas for transmission in order to compensate for large free-space path loss. The narrow beam width of THz links can lead to alignment issues, resulting in link failures [7]. This problem can become more severe if there is a restriction in the communication range.

The diameter of the beam received area d_{beam} and beam received area A_{beam} can be approximated as $d_{beam} \approx 2\pi d(\theta/360^\circ)$, and $A_{beam} = \pi d_{beam}^2/4$, where θ is the beamwidth, and d is the distance between Tx and Rx as described in Figure 2-2. If we assume a beamwidth θ of 5°, a distance d of 5 m, the resulting d_{beam} and A_{beam} are approimately 0.44 m and 0.15 m^2, respectively. This suggests that the

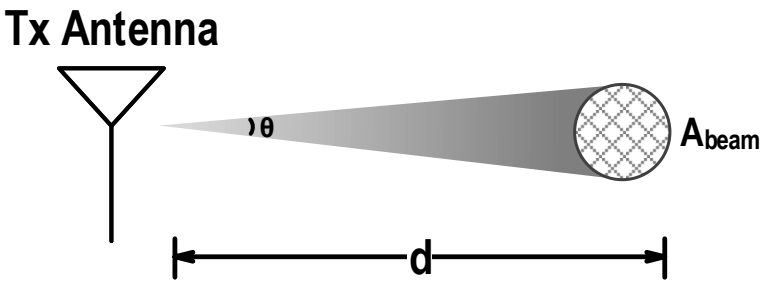


Figure 2-2: Beam received area approximation model

receiver does not need to be precisely positioned in order to receive the transmitted beam. However, as the distance between the transmitter and receiver decreases, the beam's received area becomes smaller. Thus, it is necessary to increase the transmit power and improve the sensitivity of the receiver to alleviate misalignment issues. In addition, using steerable THz beams allows for control over the larger coverage area, enabling targeting specific locations or devices.

Highly directive THz beam also can make THz communication links more secure, making it harder for eavesdroppers to intercept THz signals [35]. This can be helpful in situations where it is important to keep communication private and secure, particularly on ultra-miniaturized platforms that are vulnerable to DoS attacks, as previously mentioned in Chapter 1.2.

2.2 THz WuRx architecture

This section provides an overview of the various THz receiver architectures proposed in the literature and to develop a low-power THz WuRx architecture suitable for ultra-miniaturized platforms.

2.2.1 Existing THz receivers

f_{max} limitation

According to a recent report on CMOS technologies, the highest maximum oscillation frequency (f_{max}) has been observed to be near 280-320 GHz, including parasitic

interconnects such as vias and metal [40]. This limits the high-frequency operations of fundamental circuits, such as low-noise amplifiers (LNA) and local oscillators (LO) near carrier frequency, constraining how THz receivers can be implemented. For example, LNA first architecture cannot be used for THz receivers, which typically provides better sensitivity compared to other architectures in RF domain [39]. In addition, LNA also burns a significant amount of power, even with the recently developed high-speed transistors.

THz receivers with more than mW of power

Mixer-first architecture using a LO with fundamental frequency is also challenging due to the LO driver; An alternative is to use a mixer-first architecture with an LO that has a harmonic frequency, which leads to lower sensitivity due to high conversion loss. [8, 40]. However, these works still require relatively high power consumption (a few 10s of mW), which is not suitable for always turned-on WuRxs. [13] presents a 150 GHz regenerative receiver that uses harmonic frequencies but still requires 10 mW Rx power.

2.2.2 Energy detection architecture

Energy detection architectures, which do not require an LNA, LO, or mixer, can achieve significantly lower power consumption through direct demodulation to the baseband and are adopted to ultra-low power WuRxs in the RF domain. [38] presents a WuRx consuming DC power of 4.5 nW while achieving the sensitivity of -69 dBm at 113.5 MHz. Another example is the WuRx presented in [18], which has a sensitivity of -69.5 dBm at 9 GHz and consumes 22.3 nW of power.

CMOS terahertz incoherent receivers can be built through energy detection architecture. These receivers use the non-linearity of CMOS devices at the THz spectrum to detect the energy of the incoming electromagnetic waves. For example, CMOS Schottky barrier diodes [15] and NMOS transistors [34] have been used for THz signal detection. However, most incoherent receivers are designed for imaging applications,

not low-power THz communication applications.

2.3 Proposed architecture

We explored design perspectives for building THz WuRx systems and various approaches for RF/THz receiver architectures in the literature, each of which is suited to a particular application, such as high-data-rate communication or THz imaging. After considering available options, we have chosen an energy detection architecture for the THz WuRx system in order to reduce power consumption to the microwatt level.

The design of the WuRx system is depicted in Figure 2-3. It features a THz frontend consisting of a pair of pseudo-differential CMOS terahertz detectors with dual-antenna feeds, and an amplifier-filter-comparator chain, followed by a wake-up authentication engine. The THz frontend demodulates THz signals into baseband signals, which are then amplified, filtered, and digitized by an offset-controllable comparator. The wake-up authentication engine compares the incoming bits to a stored token and generates a wake-up signal if there is a match. The design and implementation of the entire system are discussed in more detail in later chapters.

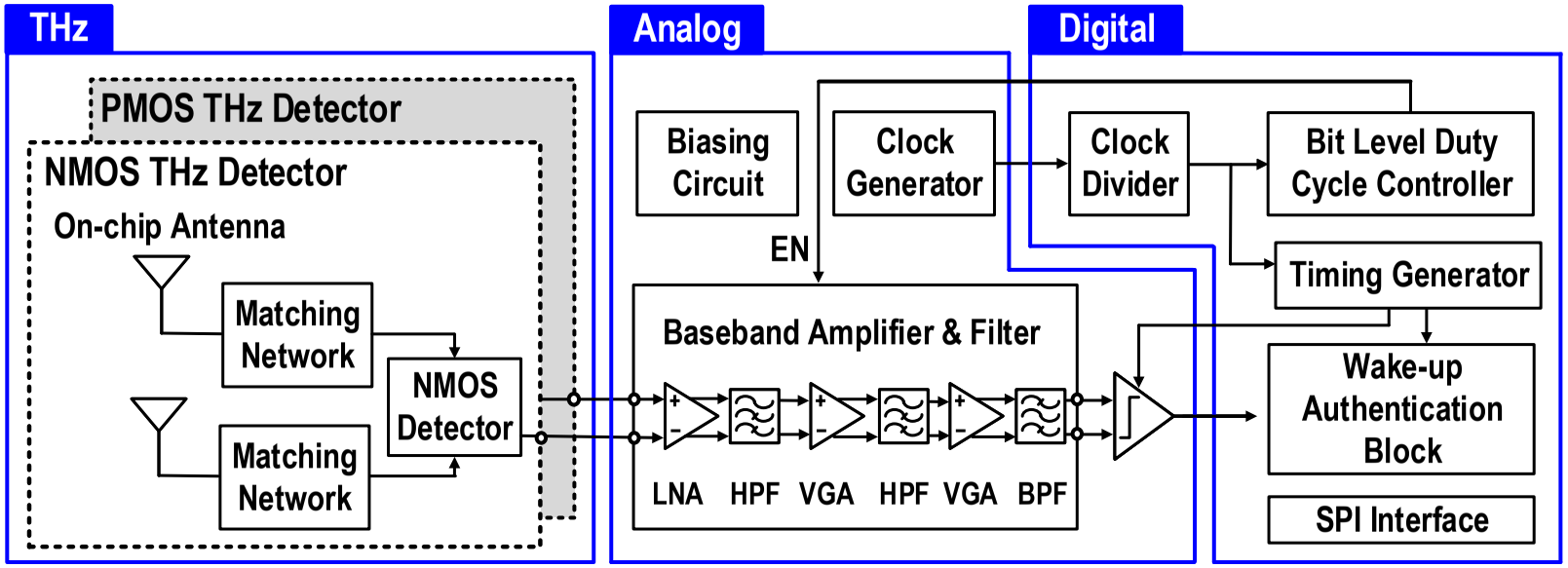


Figure 2-3: Block diagram of the THz WuRx system

Chapter 3

THz frontend design

In the previous chapter, the energy-detection first architecture is chosen for the THz WuRx design to achieve low-power consumption. This chapter discusses the schematic of the THz front end and its design methodology.

3.1 THz frontend and detector topology

The CMOS THz receiver front end, as shown in Figure 3-1, is of a pseudo-differential and consists of an NMOS detector and a PMOS detector with opposite responsivity polarities. Specifically, the NMOS detector offers positive responsivity, while the PMOS detector offers negative responsivity. In order to eliminate DC power consumption and avoid flicker noise, the MOSFETS are biased with zero drain-source voltage (also known as Cold-FET) [17]. The on-chip antennas capture THz signals, which are then rectified and demodulated at the drain node of NMOS and PMOS detectors. Demodulate signals are amplified by the subsequent baseband amplifier stages and digitized by a dynamic comparator, which will be described in Chapter 4.1.

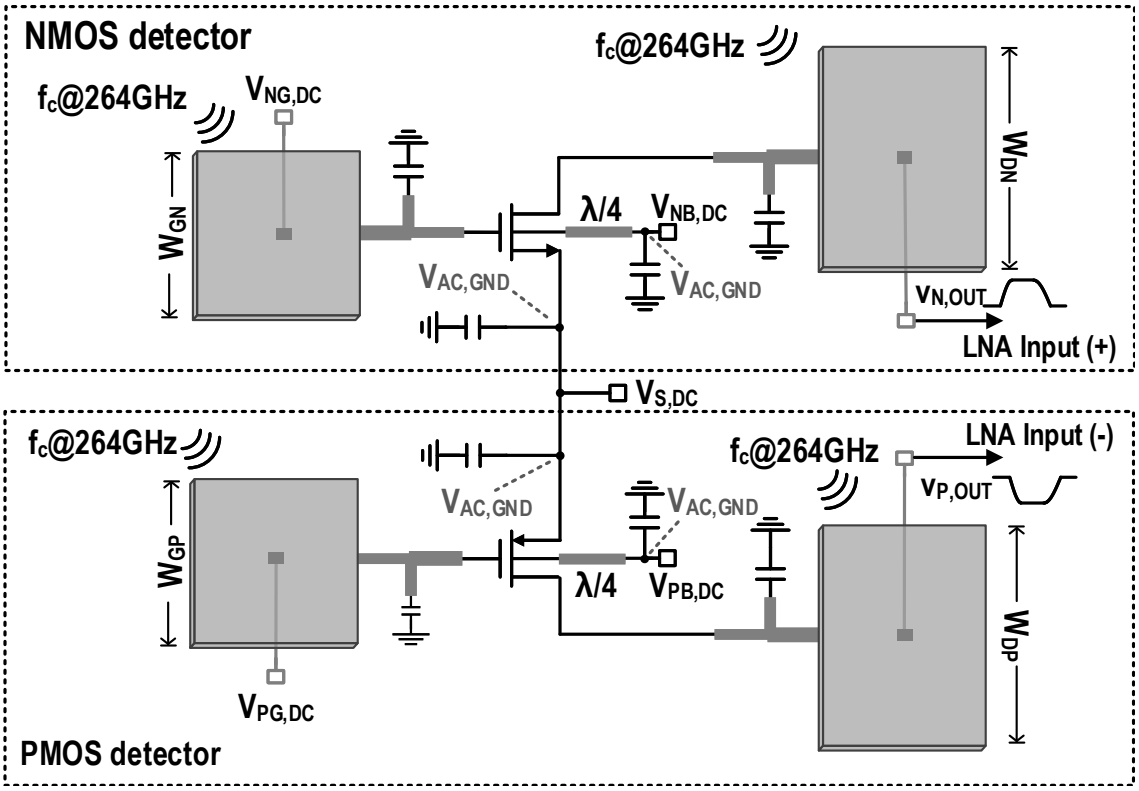


Figure 3-1: Schematic of the THz frontend

3.2 Optimum responsivity condition

Two important metrics for the THz detectors are responsivity and noise-equivalent power (NEP). NEP is typically regarded as the most important metric because it determines the sensitivity of the detecting system. NEP is the input THz power when the detector output SNR equals unity for 1 Hz bandwidth [14], and can be obtained by dividing the output voltage noise spectral density by the detector voltage responsivity. Similarly, for the receiver, lower NEP provides a better theoretical sensitivity limit. To enhance the sensitivity limit, NEP should be minimized. For Cold-FET detectors, the main noise source is channel thermal noise, which is determined by the gate bias voltage and transistor size. The optimization goal shifts from minimizing NEP to maximizing responsivity under the fixed DC bias condition.

Now, the goal is to determine the optimal condition for responsivity. THz power rectification behavior varies depending on the device driving conditions, as previously reported in [22]. Figure 3-2 shows a test bench for the detector responsivity test. The

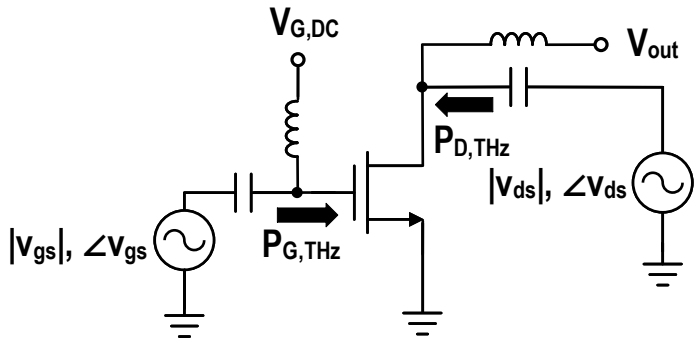


Figure 3-2: A testbench for detector responsivity test.

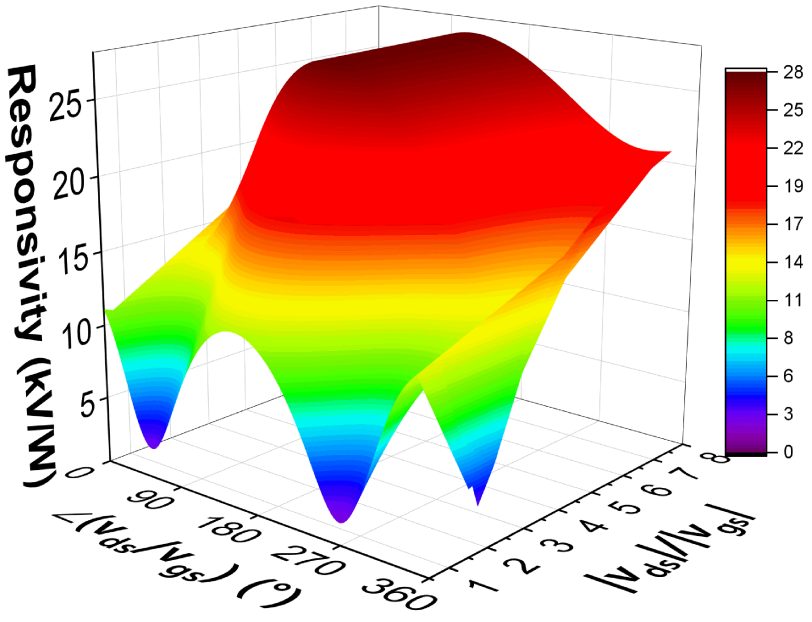


Figure 3-3: Simulated responsivity of an NMOS transistor at various v_{gs} and v_{ds} amplitude ratio and phase difference when the transistor gate is biased at 0.35 V.

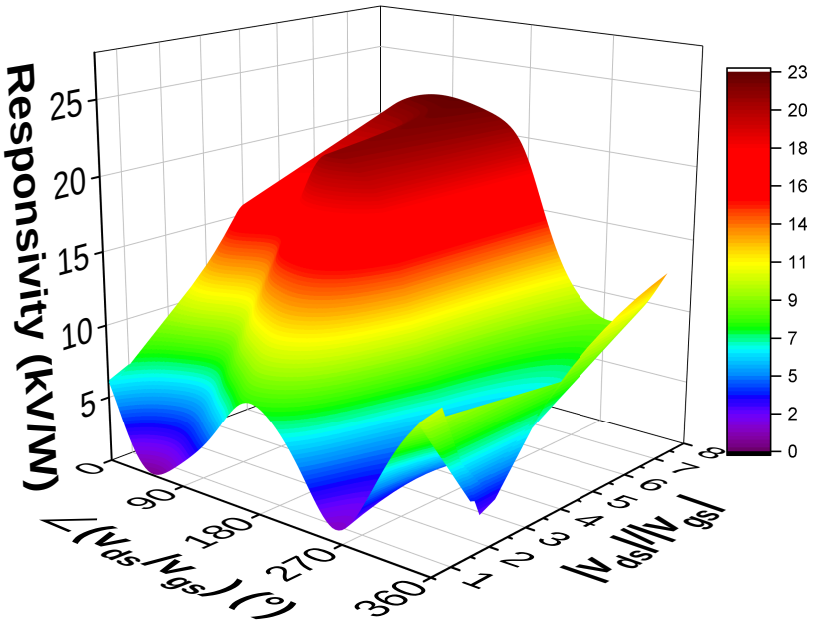


Figure 3-4: Simulated responsivity of a PMOS transistor at various v_{gs} and v_{ds} amplitude ratio and phase difference when the transistor gate is biased at 0.45 V.

transistor gate is DC biased to $V_{G,DC}$ through an RF choke while the drain is at the floating node. The MOSFET is driven by two ideal ac voltage sources, one applied to the gain side (v_{gs}) and the other to the drain side (v_{ds}).

The total THz input power, $P_{in,THz}$, can be calculated using the following equation:

$$P_{in,THz} = P_{G,THz} + P_{D,THz} = Re(v_{gs}i_{gs}^{*}) + Re(v_{ds}i_{ds}^{*}) \tag{3.1}$$

where $P_{G,THz}$ is the THz input power at the gate side, $P_{D,THz}$ is the THz input power at the drain side, v_{gs} is the THz voltage at the gate side, i_{gs} is the THz current at the gate side, v_{ds} is the THz voltage at the drain side, and i_{ds} is the THz current at the drain side.

Then, the responsivity R_v of the detector is obtained as:

$$R_v = \frac{V_{out}}{P_{in,THz}}, \tag{3.2}$$

where V_{out} is the rectified DC value that can be extracted through the RF choke.

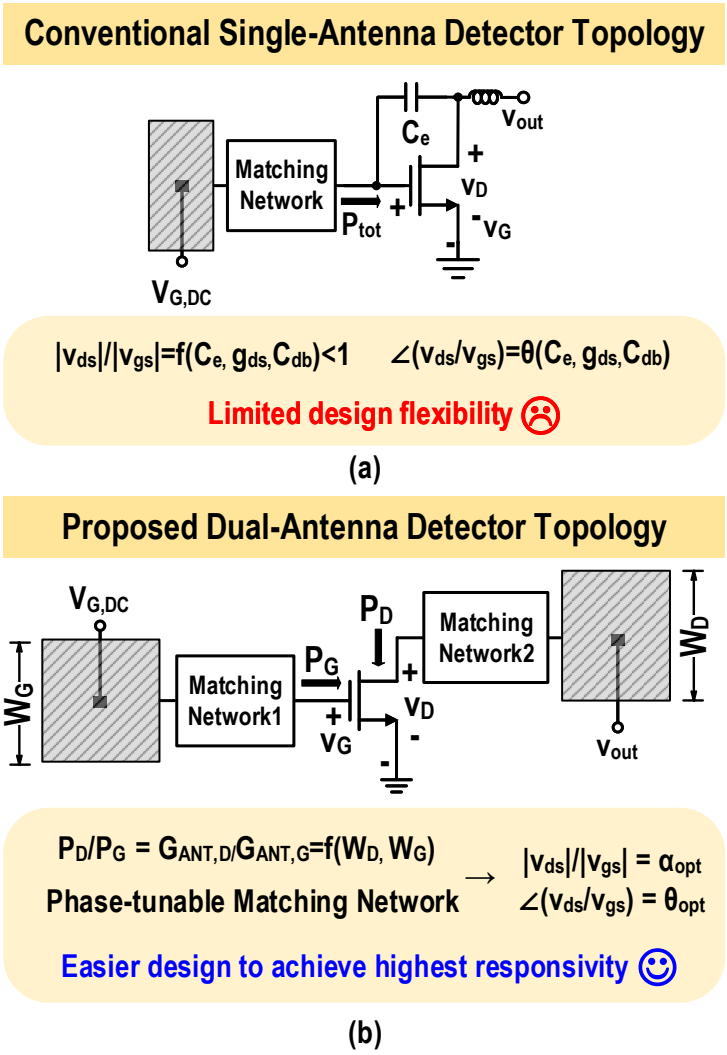


Figure 3-5: Comparison between (a) conventional single antenna detector topology and (b) proposed dual-antenna detector topology.

Figure 3-3 presents the simulated responsivity of an NMOS transistor at various $|v_{ds}/v_{gs}|$, $\angle(v_{ds}/v_{gs})$ pairs when the transistor gate is biased at 0.35 V. The peak responsivity of 26.8 kV/W is obtained, which is nearly 2 times higher than that at $v_{ds}/v_{gs} = 1$. The maximum responsivity can be achieved under the following optimal conditions,

$$|v_{ds}/v_{gs}| = 4.5 \text{ and } \angle(v_{ds}/v_{gs}) = 170^{\circ} \tag{3.3}$$

The responsivity of the device is obtained from the ADS harmonic balance simulation. During the simulation, parasitic interconnections from lower metal layers to higher metal layers, including vias, are extracted from the HFSS simulation and included in the harmonic balance simulation. The gain side transistor impedance (Z_{GN}) and the drain side transistor impedance (Z_{DN}) are obtained as,

$$Z_{GN} = 18 - 84.1j\,\Omega \text{ and } Z_{DN} = 10 - 180.3j\,\Omega \tag{3.4}$$

Similarly, the optimum responsivity condition is obtained as shown in Figure 3-4 when the PMOS gate is biased at 0.45 V. The peak responsivity of 23 kV/W is obtained under the following optimum conditions,

$$|v_{ds}/v_{gs}| = 5.5 \text{ and } \angle(v_{ds}/v_{gs}) = 170^{\circ} \tag{3.5}$$

The gain side PMOS transistor impedance (Z_{GP}) and the drain side PMOS transistor impedance (Z_{DP}) is :

$$Z_{GP} = 21 - j76\,\Omega \text{ and } Z_{DP} = 10 - j179\,\Omega \tag{3.6}$$

.

3.3 Dual-antenna topology to achieve optimal condition

A dual-antenna topology, previously applied for energy harvesting [22], is adopted for low NEP and high responsivity. The comparison between conventional single-antenna detector topology and proposed dual-antenna detector topology is summarized in Figure 3-5. The topology of a conventional MOSFET THz detector is shown in Figure 3-5 (a), where the drain and gate are coupled through an explicit or parasitic capacitor (C_e). Hence, the voltages of the gate nodes and drain nodes have a fixed amplitude ratio and phase difference [21], which is a function of the explicit capacitor (C_e), parasitic capacitor (C_{db}), and transistor output conductance (g_{ds}), and they are almost identical ($v_{ds} \approx v_{gs}$). Achieving the two optimal conditions in equation 3.3 simultaneously, along with antenna-to-device power matching, is very challenging because a single antenna feeds power both to the gate and drain sides. This may be possible with the complex matching network, but it often comes at the expense of a higher loss.

Under the optimum condition presented in equation 3.3, the ratio of THz power at the drain, $P_{D,THz}$, to THz power at the gate, $P_{G,THz}$, can be determined by the equation:

$$\frac{P_{D,THz}}{P_{G,THz}} = \frac{G_{DN}|v_{ds}|^2}{G_{GN}|v_{gs}|^2} = 2.5, \tag{3.7}$$

where G_{DN} and G_{GN} represent the conductance at the drain and the gate side of the NMOS device, respectively; however, achieving the desired power ratio is difficult in the conventional single-antenna topology due to the coupling between drain and gate. Such a problem is addressed in the dual-antenna topology, as shown in Figure 3-5 (b) by breaking the power feeding and impedance matching between the gate and drain. The design flow can be simplified into two steps.

1. Changing the widths of the patches (W_D and W_G) hence the corresponding antenna gains (Figure 3-6) allows for independent adjustment of the ratio between THz power (P_D/P_G) injected into the drain and gate. With W_G= 200 μm and

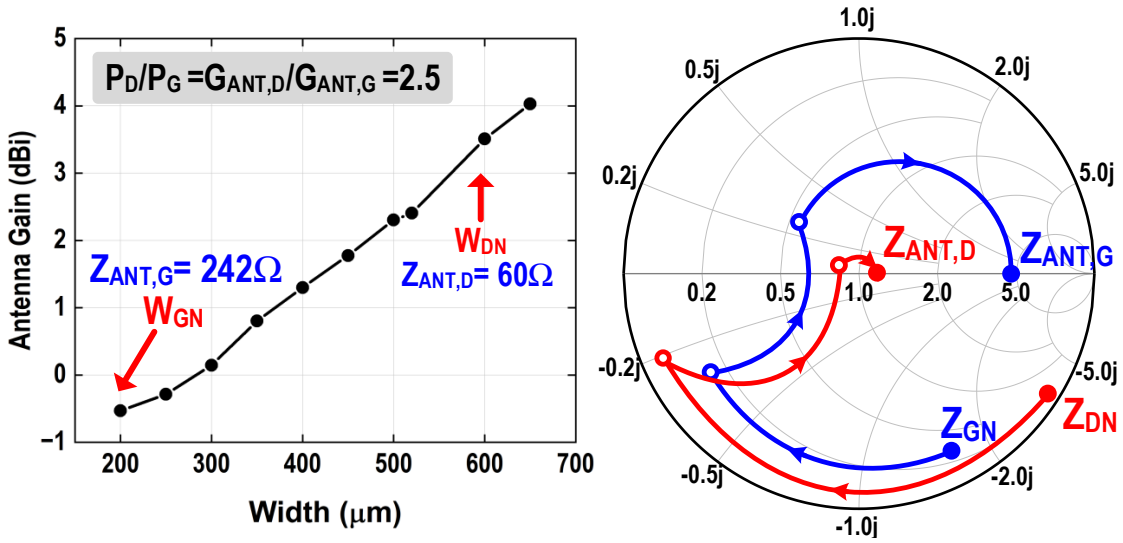


Figure 3-6: Antenna widths versus antenna gain curve from HFSS simulation (left), impedance matching networks for NMOS gate and drain on a Smith chart (right)

W_D = 600 μm, the resultant P_D/P_G is 2.54, and $|v_{ds}/v_{gs}|$ reaches the desired value of 4.5.

2. The two patch antennas placed back-to-back directly provide near-180° phase difference between v_{ds} and v_{gs}, as shown in Figure 3-1. Fine-tuning of phase can be easily achieved by slightly adjusting the characteristic impedance of the matching network.

The simulated NMOS detector responsivity is 13.3 kV/W, including matching networks losses, and is 4.4 kV/W with 34% effective antenna efficiency and overall NEP of 8.2 pW/Hz$^{1/2}$. Similarly, the PMOS detector achieves a simulated responsivity of 3.4 kV/W and NEP of 8.6 pW/Hz$^{1/2}$.

3.4 DC biasing and amplifier connection

As shown in the test bench setup in Figure 3-2, it is crucial to bias the gate and extracts the demodulated signal without interfering with THz operation. This is achieved by using the central AC grounds of the patch antennas for DC gate biasing and extracting the demodulated signals from the drain nodes with no disturbance to

THz operation. In this design, the top metal layer (aluminum) is used as the patch antenna. The center of the patch antenna is connected directly to the metal 1 layer, and the metal 1 layer is connected to the DC biasing point. Since metal 1 and metal 2 are used as ground and metal 2 still covers above the metal 1 DC path, the DC path does not greatly affect the antenna performance.

Chapter 4

Baseband circuit-level implementation

This chapter describes the baseband circuits for building the wake-up receiver integrated with the THz detectors from the previous chapter.

4.1 Baseband amplifier

Each detector receives the OOK-modulated radiated THz signals and demodulates them to the baseband signals. Figure 4-1 shows the architecture of the baseband amplifier. It consists of three amplifier stages followed by a buffer stage that provides additional noise filtering before the comparator input. The entire bandwidth of the baseband amplifier is around 10 kHz.

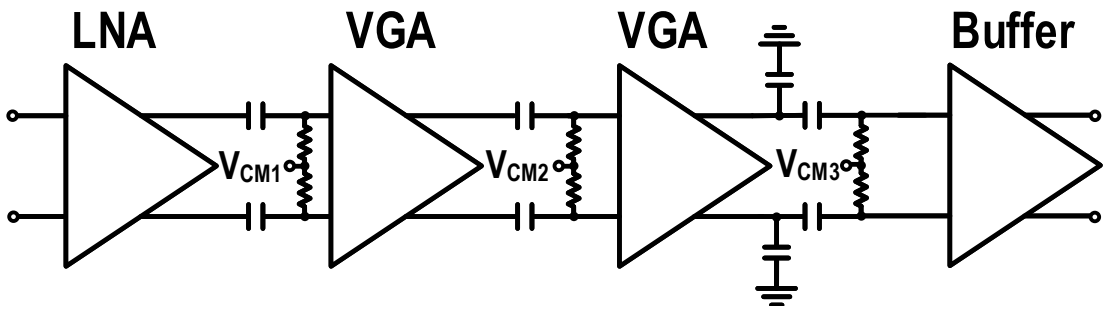


Figure 4-1: Block diagram of the baseband amplifier-filter chain

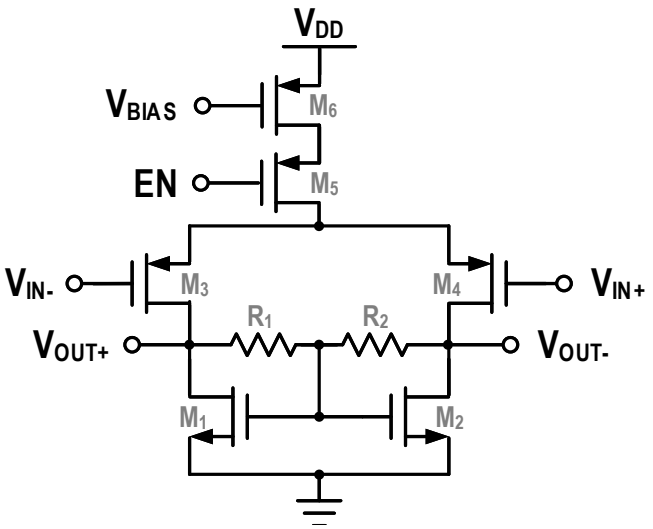


Figure 4-2: Schematic of the first stage LNA

The first stage LNA is a common-source differential amplifier, as shown in Figure 4-2. The LNA consumes 3.05 μA at the 0.8 V voltage supply and has a voltage gain of 29 dB. The PMOS pair (M_3, M_4) is used for input of the amplifier and is sized largely (W/L = 800 μm/4μm) to reduce the flicker noise. Resistors R_1 and R_2 are used for common-mode feedback.

One simple way VGA design topology is shown in Figure 4-3 (a), with a voltage gain of $-g_{mN}R_{1,2}$. Voltage gain can be adjusted by simply changing the load resistance. Assuming a bias current of 10 nA and $g_m/I_D = 20$ for the transistor operating in a sub-threshold region, the obtained g_m is 200 nS. To achieve a voltage gain of 20 dB, the required load resistance is 50 MΩ, which requires a large chip area and suffers from process variation.

To avoid this problem, common-source differential pair with current bleeding transconductance loading has been adopted for VGA topology, as shown in Figure 4-3 (b). The passband voltage gain A_v of this VGA topology can be approximated as follows:

$$A_v \approx -\frac{g_{mN}}{g_{mL}} \tag{4.1}$$

where g_{mN} and g_{mL} are transconductances of an input NMOS transistor and

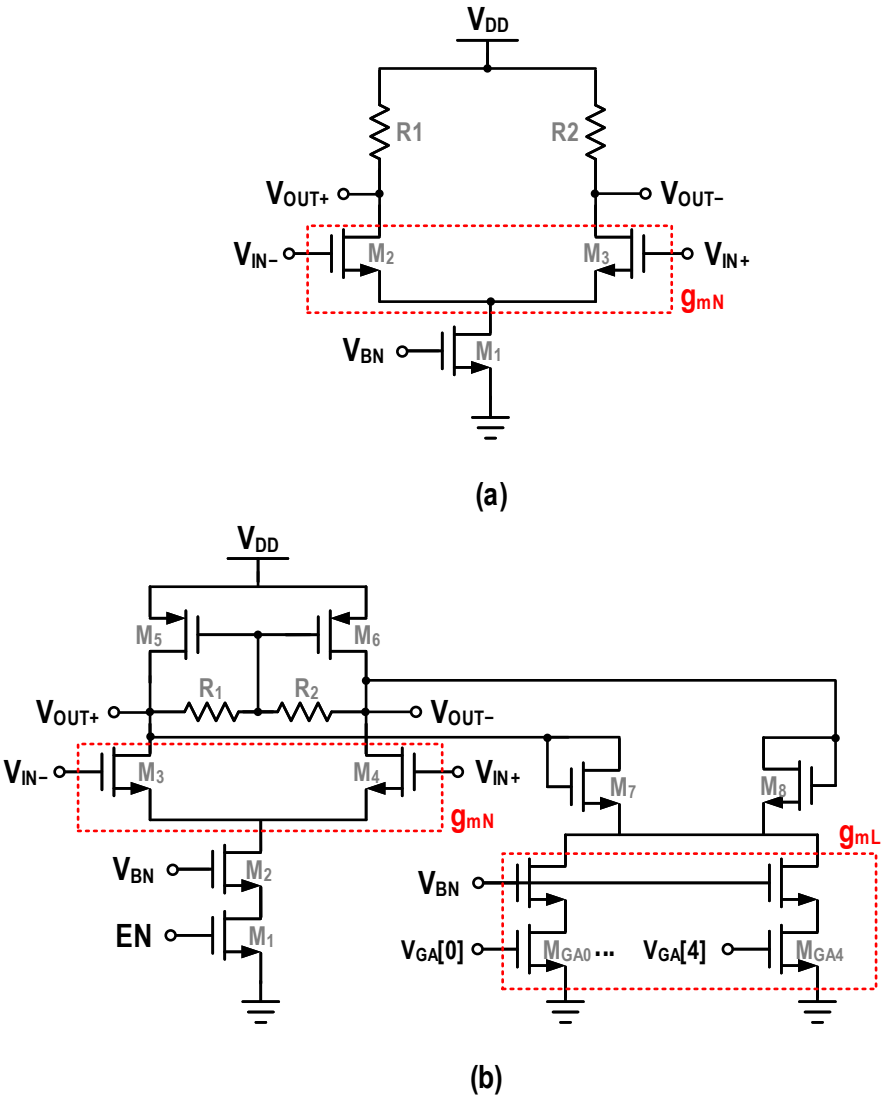


Figure 4-3: Schematic of the variable gain amplifier (a) Conventional VGA topology, (b) VGA with current bleeding transconductance load

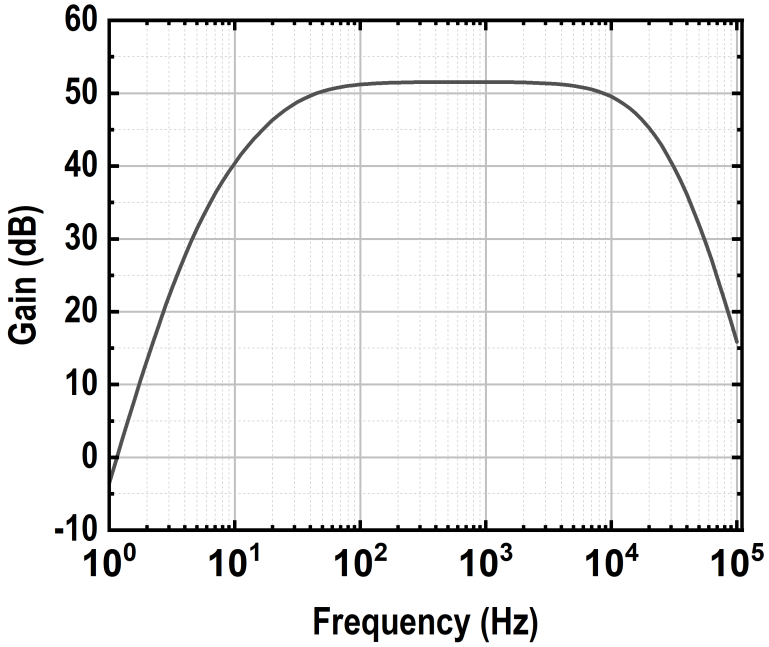


Figure 4-4: Simulated gain transfer function of baseband amplifier stage

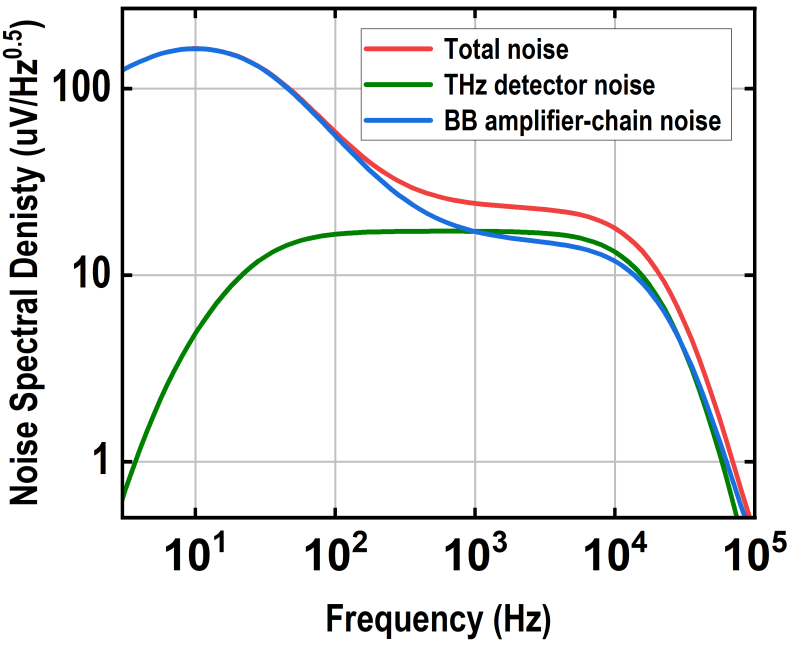


Figure 4-5: Simulated output noise spectral density of the THz detector, baseband chain, and their sum

NMOS load transistor, neglecting the effect of common-mode resistors. Similar to the LNA case, resistors R_1 and R_2 are for common-mode feedback and are large resistors to avoid gain degradation. This topology provides lower process variation because the gain is expressed as the ratio between transconductances. The output of three amplifier stages drives the buffer, providing additional noise filtering before the comparator input. The last stage buffer uses the same topology as Figure 4-3 (b), but without reconfigurability. The entire stage can provide a variable gain from 40-60 dB. The DC offsets from the amplifier mismatches and non-linearity should be canceled because a high-gain amplifier chain can saturate the subsequent amplifier stages. Thus, high pass poles are inserted after the amplifier stage to reduce DC offsets, which also reduce the flicker noise. Figure 4-4 provides the simulated gain transfer function of the entire amplifier stage.

Figure 4-5 shows the simulated output noise spectrum of the entire baseband chain, the THz frontend, and their sum at the passband gain of 51 dB while consuming 2.64 μW of DC power consumption. The LNA is biased in the sub-threshold region to save power consumption while maintaining its input-referred thermal noise is comparable to or less than the thermal noise of the detector. The baseband amplifier-chain noise contribution can be reduced at the expense of the higher DC power consumption.

V_{BIAS} in Figure 4-2 and V_{BN} in Figure 4-3 (b) are generated by cascode constant g_m circuits, modified from [17]. To avoid the meta-stable state, this circuit requires a reset signal generated by the enable signal (EN).

4.2 Comparator

Figure 4-7 shows the schematic of a dynamic latched comparator topology [26, 27]. It consists of a double latch type comparator and switching transistors with zero-bias transistors for capacitive balance control. When CLK is low, the M3 and M4 precharge the DI+ and DI- nodes to supply voltage while discharging the CMP+ and CMP- nodes to the ground (Reset phase). When CLK goes high, M5 turns on, and the DI+ and DI- nodes are pulled down. The falling edge difference between the

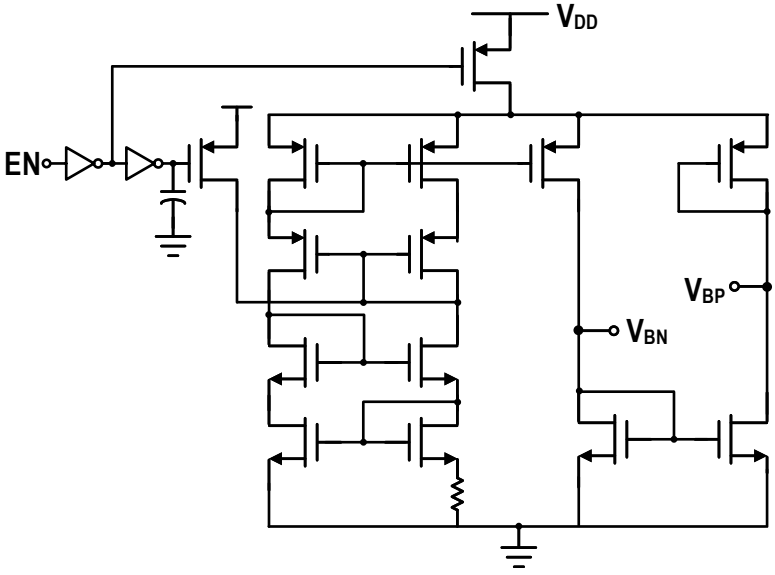


Figure 4-6: Cascode constant g_m circuits for amplifier current biasing

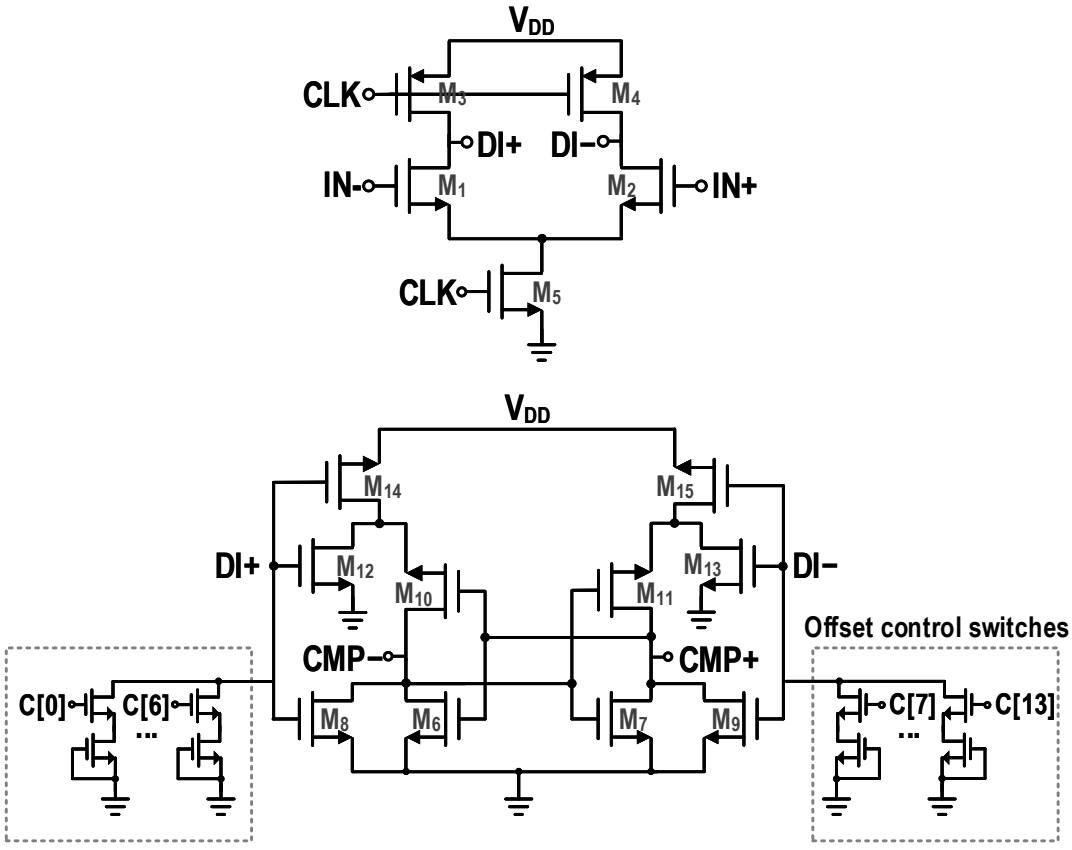


Figure 4-7: Schematic of the offset-controllable comparator

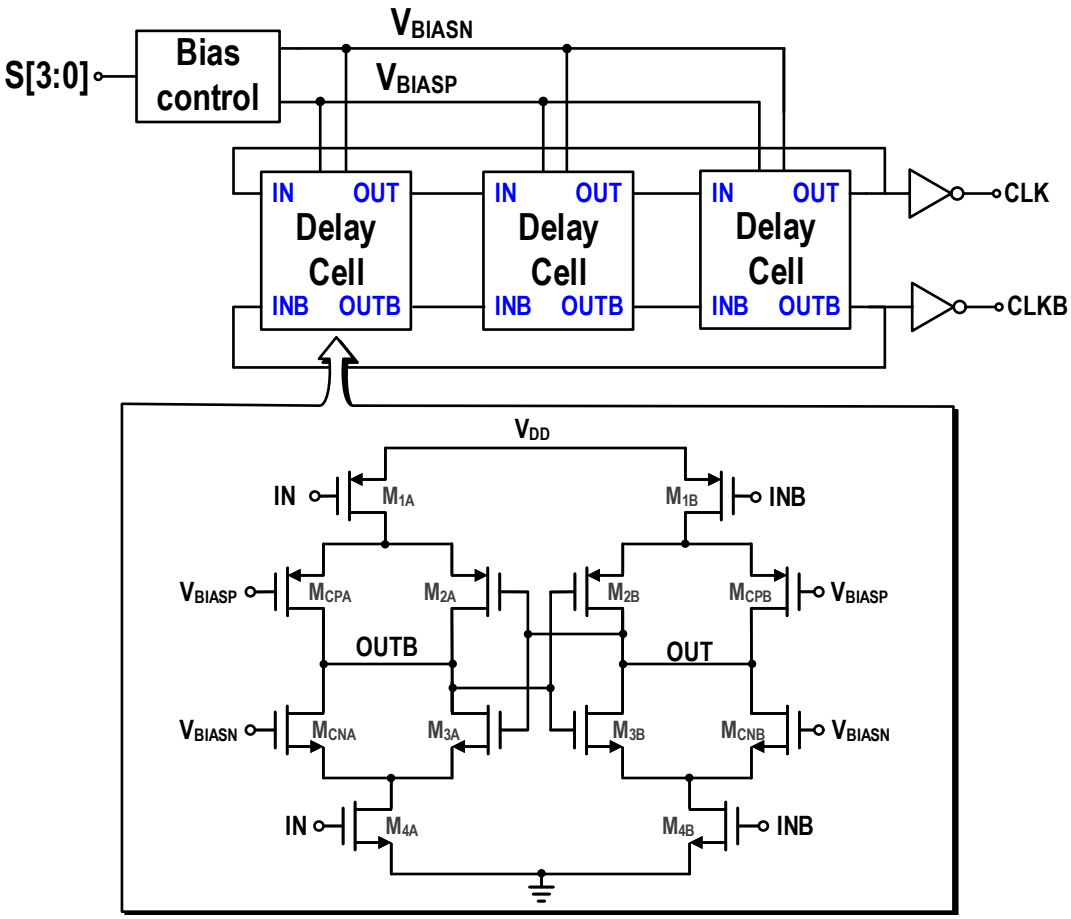


Figure 4-8: Schematic of the leakage-based cell oscillator

Di+ and DI- generates latch transistors work (Comparison phase). Switch transistors (C[13:0]) provide additional load capacitance to both nodes, enabling offset control from -30 mV to 30 mV.

4.3 Oscillator

Figure 4-8 shows the schematic of the delay-cell-based oscillator (or-leakage-based oscillator) [23]. This oscillator topology utilizes the transistor leakage current to charge/discharge capacitances the nodes, resulting in positive feedback that fully switches the output nodes with a prolonged delay. This topology has been adopted for wireless sensor nodes due to its low power consumption with a wide frequency tuning range [19, 23].

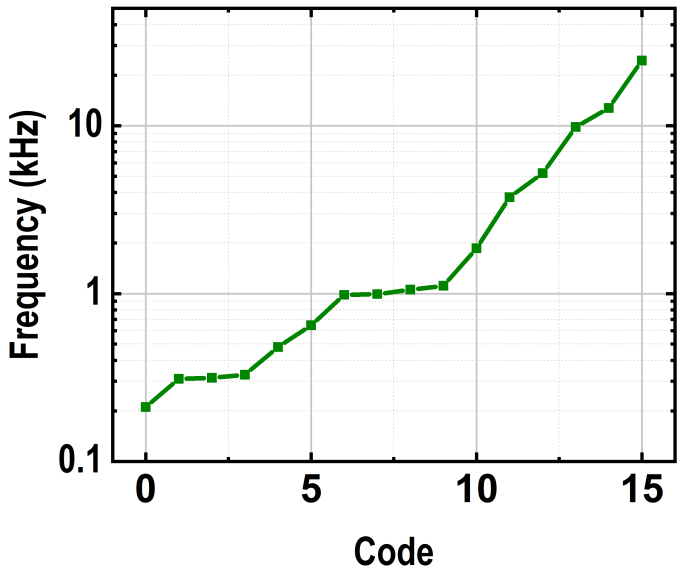


Figure 4-9: Measured oscillator frequency across 16 different code words

The oscillator is composed of three-stage delay cells and a 4-bit controllable bias control circuit. Two inverters are included to provide a balanced output load. Each delay cell consists of input transistors (M_{1A}, M_{1B}, M_{4A}, M_{4B}), back-to-back inverters (M_{2A}, M_{2B}, M_{3A}, M_{3B}), and voltage control transistor (M_{CPA}, M_{CPB}, M_{CNA}, M_{CNB}). The delay is controlled by the analog voltage generated by a digitally controllable voltage divider-based biasing circuit. Higher V_{BIASN} (Lower V_{BIASP}) induces larger charging/discharging leakage current, reducing the delay and increasing the oscillation frequency. The measured clock frequency across 16 different code words is shown in Figure 4-9, ranging from 210 Hz to 24.4 kHz. The oscillator consumes a maximum DC power of 18.56 nW at 24.4 kHz under a 0.8 V voltage supply.

Chapter 5

System-level optimization

This chapter illustrates system-level optimization for low-power, secure wake-up receiver design.

5.1 Wake-up authentication

As mentioned in Chapter 1.2, a DoSL attacker can easily obtain the wake-up token by intercepting the communication channel. If the wake-up token is a fixed pattern, the attacker can replay the target nodes and keep the nodes awake. To prevent this attack, the wake-up token should be changed after each use and be unpredictable.

The wake-up packet consists of an 8-bit preamble, a 20-bit counter value, and a 64-bit encrypted counter value, as shown in Figure 5-1. The high-gain amplifier stage can amplify noise, causing the system to respond to false signals to the authentication processor. The preamble verifies that the subsequent bits are valid signals for the wake-up authentication and rejects noise-induced signals. The counter value shared between the base station and the WuRx is encrypted by a pre-shared symmetric key. The encrypted counter serves as a wake-up token which is compared with the stored token to determine its validity. The counter values are also included in the packet to address potential desynchronization between the sender and receiver.

The authentication flow is shown in Figure 5-1. The WuRx waits for the preamble to be detected and stores the subsequent bits in 84-bit shift registers once the preamble

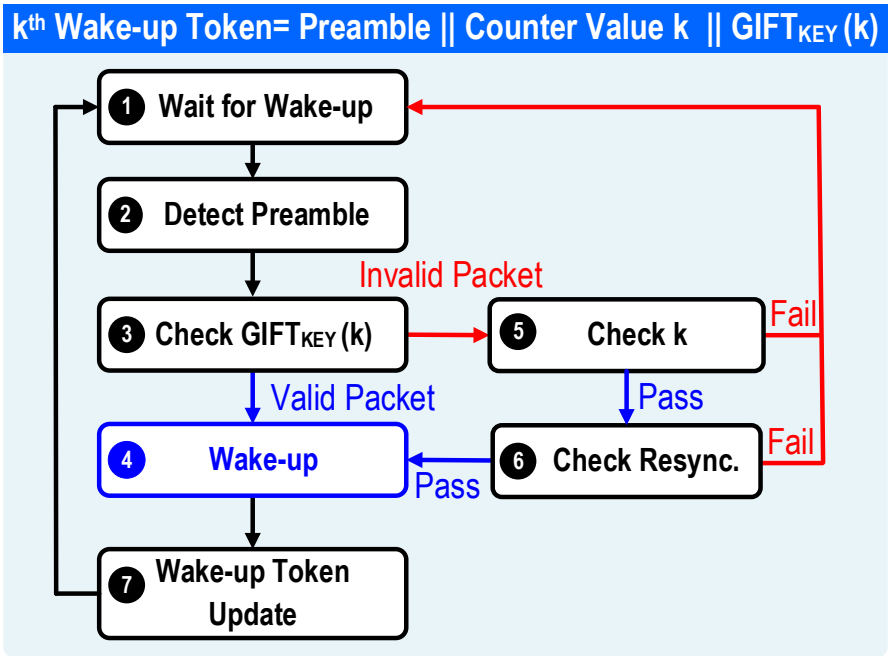


Figure 5-1: Block diagram for authentication flow

is detected. Once the entire packet is received, the correlator compares the received token and stores the token. Upon successful authentication, the WuRx generates a wake-up signal and updates the token using symmetric encryption using a pre-shared key and incremented counter value. If counter desynchronization between sender and receiver occurs due to the noise or blocked signal, packet control logic resynchronizes the counter using the received token.

The counter is encrypted by the lightweight symmetric block cipher called GIFT [1], which is specifically proposed for resource-constrained devices. While Advanced Encryption Standard (AES) is considered the standard for symmetric block ciphers, it may not be appropriate for resource-constrained systems due to the area and energy requirement of the AES [10], particularly for ultra-miniaturized nodes. Several lightweight ciphers have been proposed over the last few decades, such as PRESENT [4], SKINNY [3], and SIMON [2]. When choosing a lightweight cipher, the following criteria are considered:

- A key length of equal or greater than 128 bits, which is regarded sufficient for long-term protection [30].

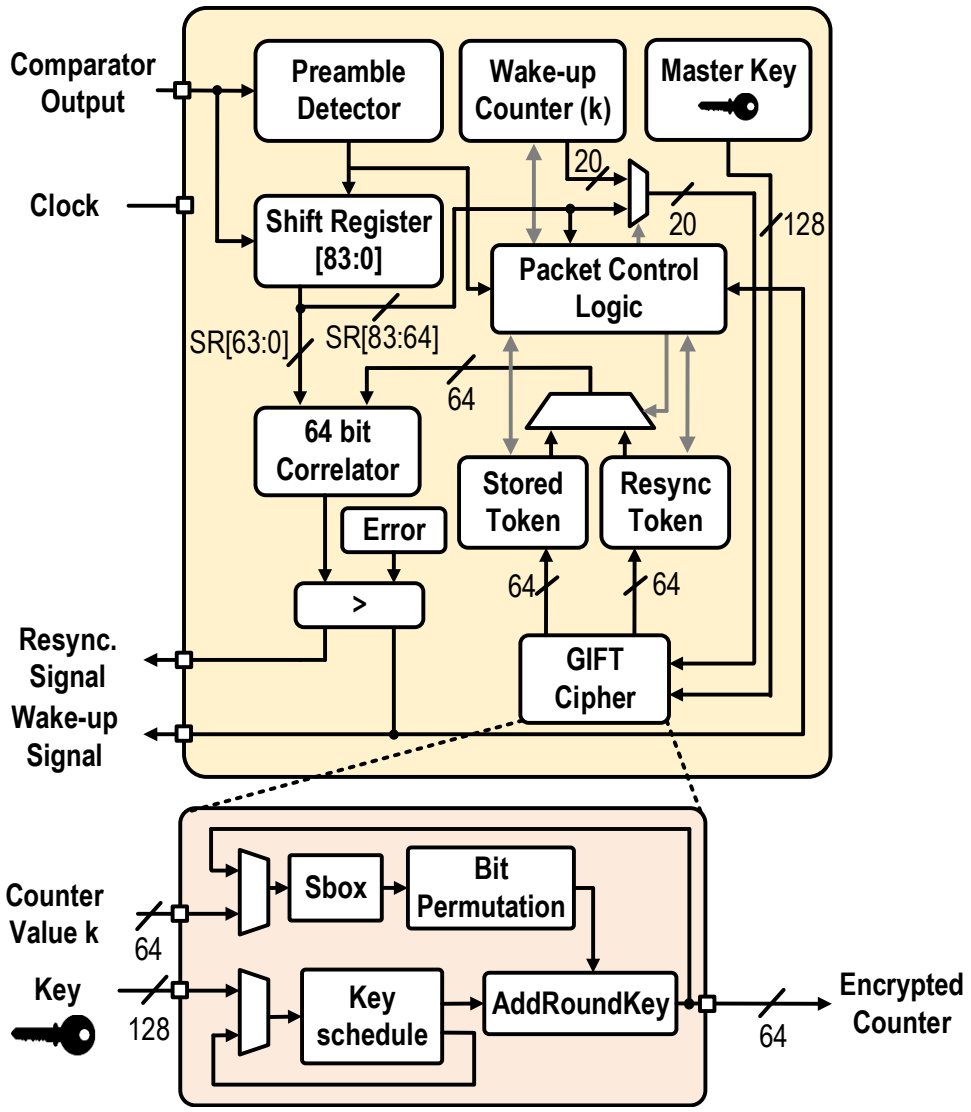


Figure 5-2: Schematic of the wake-up authentication block

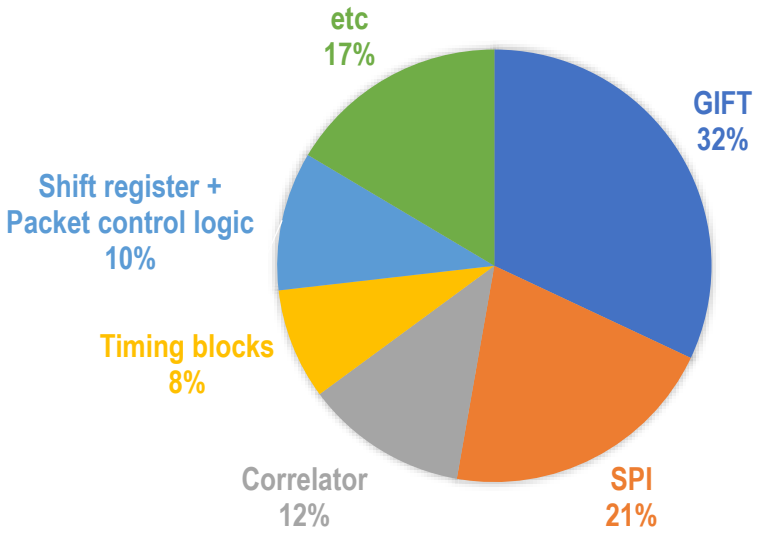


Figure 5-3: Area breakdown of entire digital circuits

- The block length of at least 32-bit. According to [29], a wake-up token length of 32-bit wake-up token takes 2.6 months for a brute-force attack at a data rate of 10 kbps, and 1.9×10^9 years to break a 64-bit wake-up token.
- A cipher with a smaller silicon area.
- A cipher that is the finalist in the currently ongoing NIST lightweight cryptography standardization process.

GIFT is chosen based on the following reasons. First, GIFT can support a cipher with a block length of 64 bits and a key length of 128 bits. Second, GIFT occupies less gate area compared to PRESENT, SIMON, and SKINNY using round-based implementations. Third, GIFT is a sub-block of GIFT-COFB, one of the finalists in NIST lightweight cryptography standardization.

The schematic of the authentication block is shown in Figure 5-2. The implemented GIFT-64-128 occupies 3.7 kGE, which occupies 32% of the entire digital circuits. Figure 5-3 shows the area breakdown of the entire digital circuits. The entire digital circuit occupies 11.6 kGE and is synthesized using HVT devices to minimize leakage power, consuming 33.6 nW measured leakage power and 65 nW measured total power at 10 kHz clock and a 0.8 V power supply.

Chapter 6

Experimental Results

6.1 Measurement setup

The chip is fabricated in TSMC 65nm CMOS technology and occupies an area of 1.54 mm^2 as shown in Figure 6-1. Unlike previous WuRx designs, no external antenna or transducer is needed in this work. The test setup in Figure 6-2 shows the measurement setup for the THz detector performance test. A Vector Network Analyzer (VNA) extender VDI-WR3.4-VNAX radiates a -6.2 dBm 264.3 GHz signal by inputting a 14.683 GHz signal via a 25 dBi horn antenna. The radiated power is measured from the VDI Erikson power meter PM5. The lock-in amplifier SR865A measures the THz detector output response. The signal generator and lock-in amplifier share the same 50% duty-cycled modulation signal, which is fed by a function generator. The lock-in amplifier aligns the modulation signal and detector output and measures the detector response. The responsivity is measured at a far-field distance of 25 cm. For the NEP measurement, the output noise of the detector needs to be measured. Output noise of the THz detector, which has low noise density, is amplified by 60 dB using an external ultra-low-noise amplifier (EG&G 5184, 0.8 nV/Hz input-referred noise) and measured by vector signal analyzer 89440A.

To measure the sensitivity of the WuRx, the setup shown in Figure 6-3 is used. Instead of using a function generator and lock-in amplifier, the input signal to the VDI-WR3.4-VNAX is OOK-modulated by an FPGA board (XEM7001). The bit er-

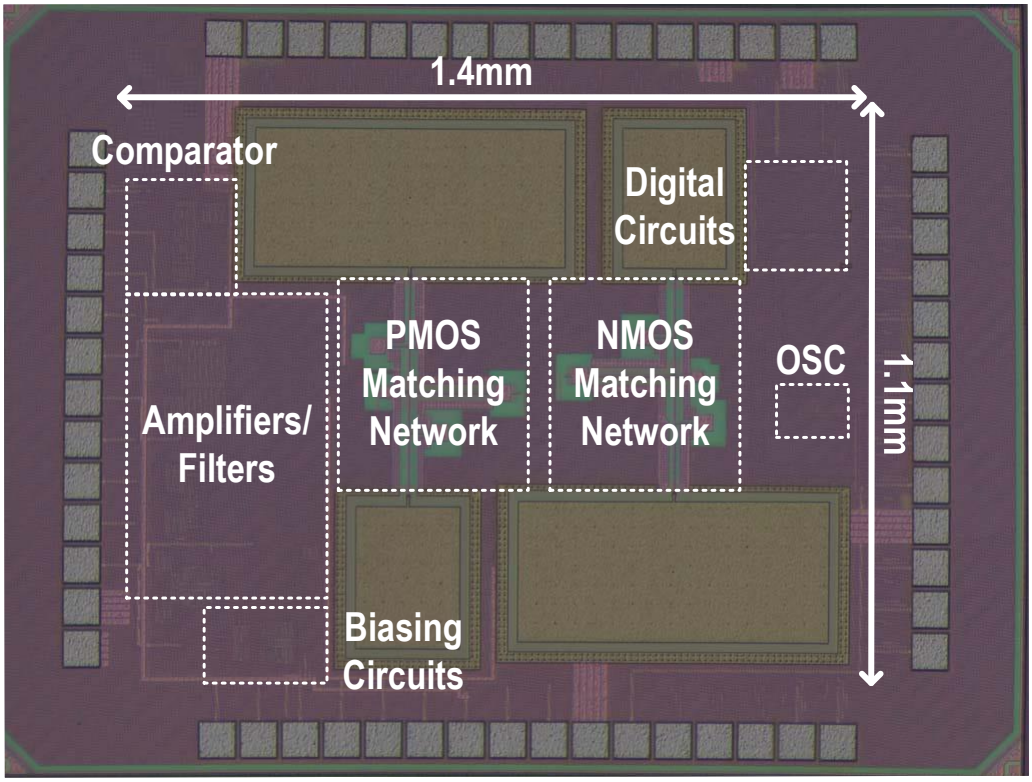


Figure 6-1: Die photograph

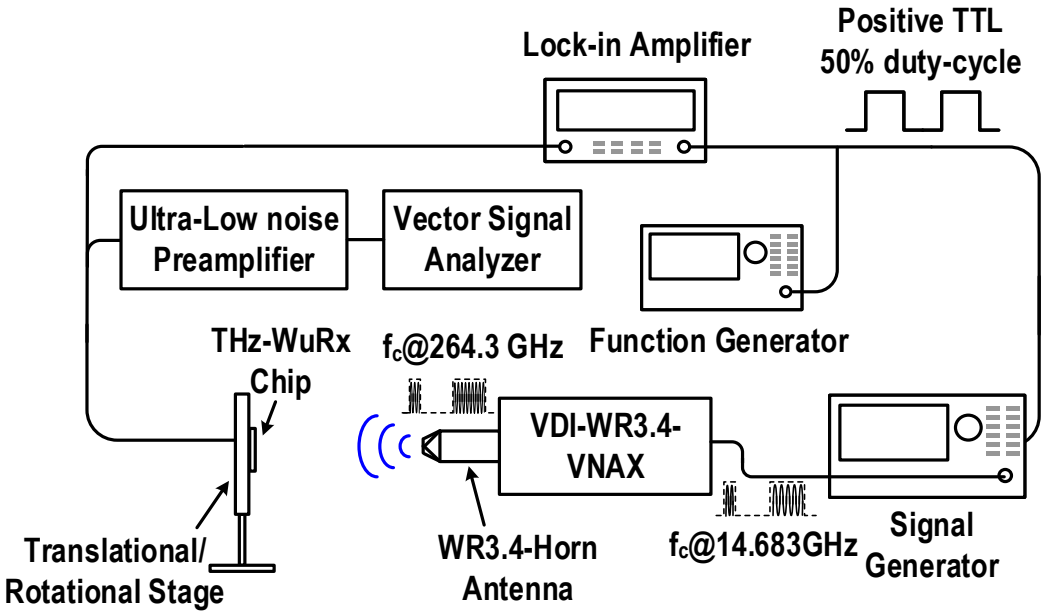


Figure 6-2: Setup for THz detector responsivity and NEP measurement

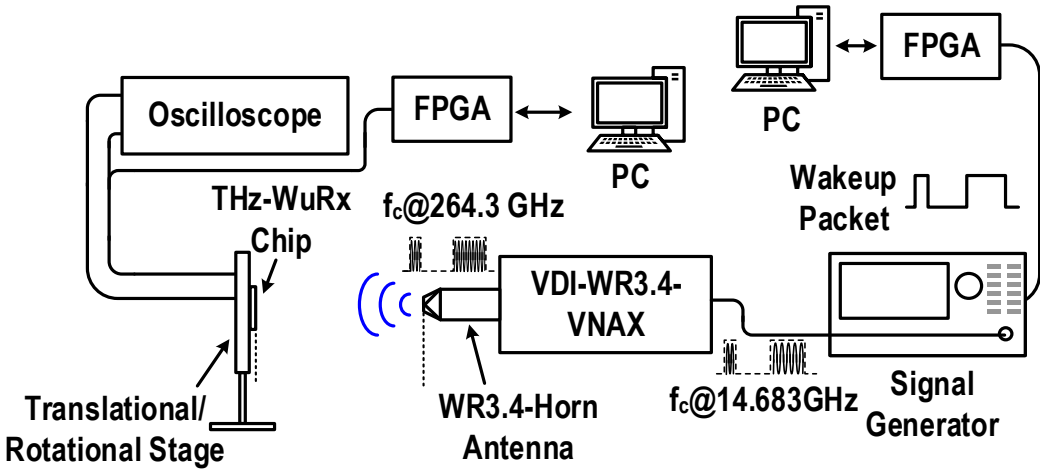


Figure 6-3: Setup for THz WuRx measurement

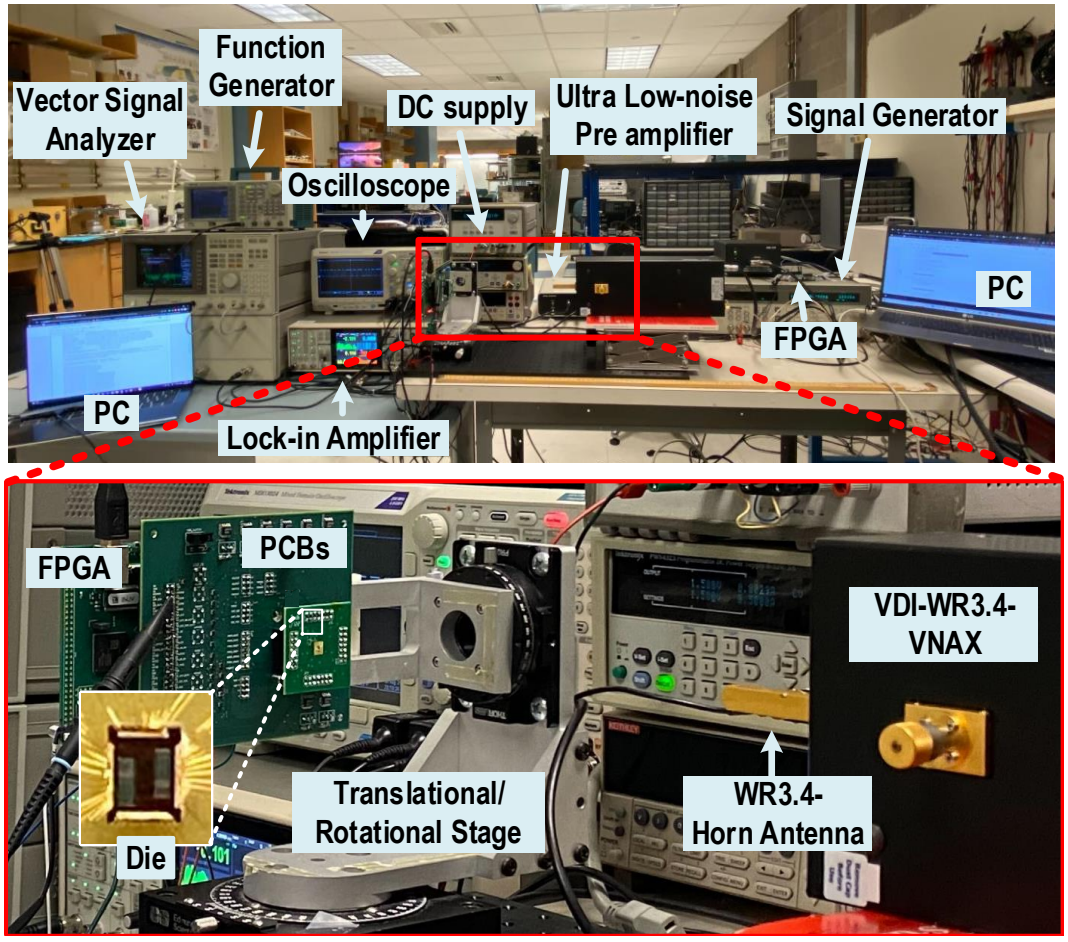


Figure 6-4: Photos of measurement setup for THz detector responsivity and NEP measurement

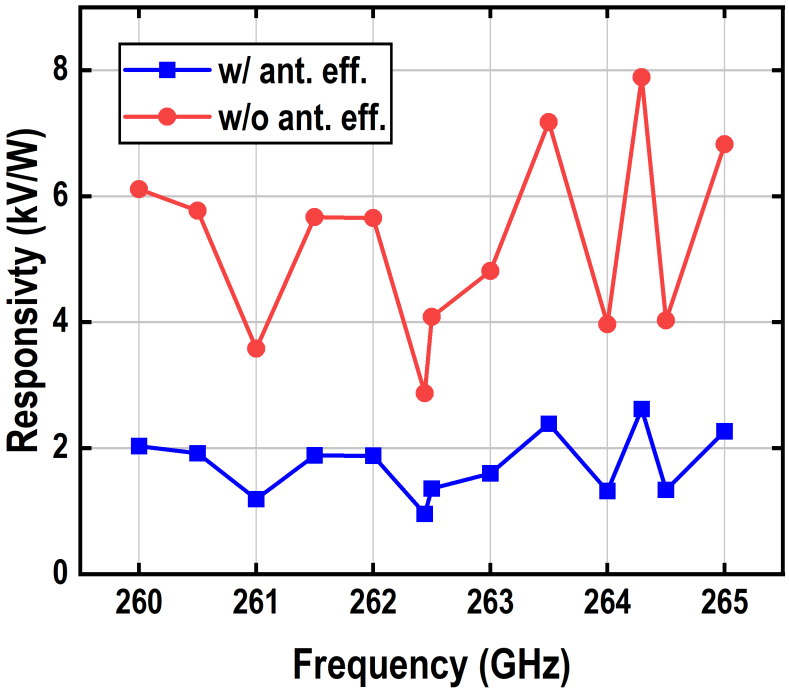


Figure 6-5: Measured pseudo-differential THz detector responsivity

ror rate is calculated by comparing the PRBS7 pattern that was transmitted with the comparator output on the chip. The PCBs are mounted on a translational/rotational stage for angle sensitivity measurement. The motherboard PCB only contains ultra-low noise voltage regulators, decoupling capacitors, and level shifters, and the daughter PCB only holds the chip.

6.2 Characterization of circuits

From the Friis Transmission Equation, the voltage responsivity R_v of the detector can be calculated as [14]:

$$R_v = \frac{v_{out}}{P_{in}} = \frac{\frac{\pi}{2} \times V_{rms}}{P_{cw} G_T (D_{G,R} + D_{D,R}) (\frac{\lambda}{4\pi d})^2}, \tag{6.1}$$

where V_{rms} is the detector output voltage from the lock-in amplifier, P_{cw} is the transmitted continuous wave signal power from the source without any modulation,

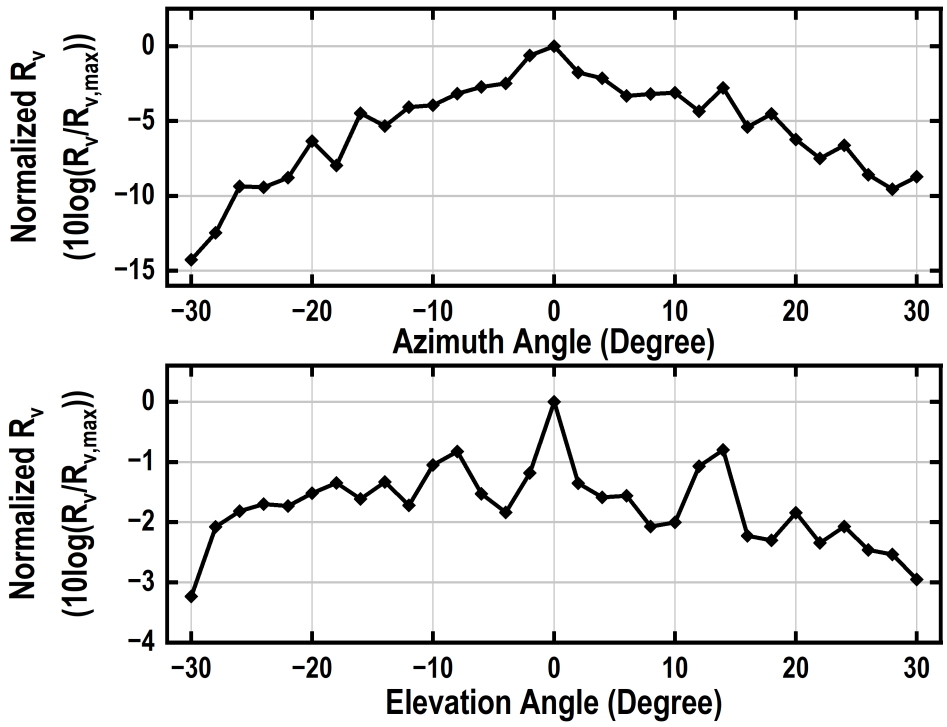


Figure 6-6: Measured angle sensitivity in E- and H- Planes

G_T is the transmitter antenna gain, λ is the carrier wavelength, and d is the distance between the source and the chip. $D_{G,R}$ and $D_{D,R}$ are the directivity of the patch antenna at the gain side and the drain side, respectively.

The measured frequency selectivity of responsivity is presented in Figure 6-5, and Figure 6-6 shows the incident angle sensitivity. The E-plane (or azimuth angle) is more sensitive to the H-plane (or elevation angle) because the non-zero Azimuth angle provides an additional phase difference between two antenna outputs, disrupting the optimal condition. It is important to note that angle sensitivity is not the same as antenna radiation patterns.

The noise spectral density of the THz NMOS detector is shown in Figure 6-7. Based on the measured responsivity and noise data, the NEP value is calculated and plotted in Figure 6-8. The minimum NEP is measured to be 10.5 pW/Hz$^{1/2}$ at $V_{GS} = 0.35$ V with effective antenna efficiency ($e_{eff} = 0.332$) taken into account, and 3.49 pW/Hz$^{1/2}$ without considering antenna efficiency.

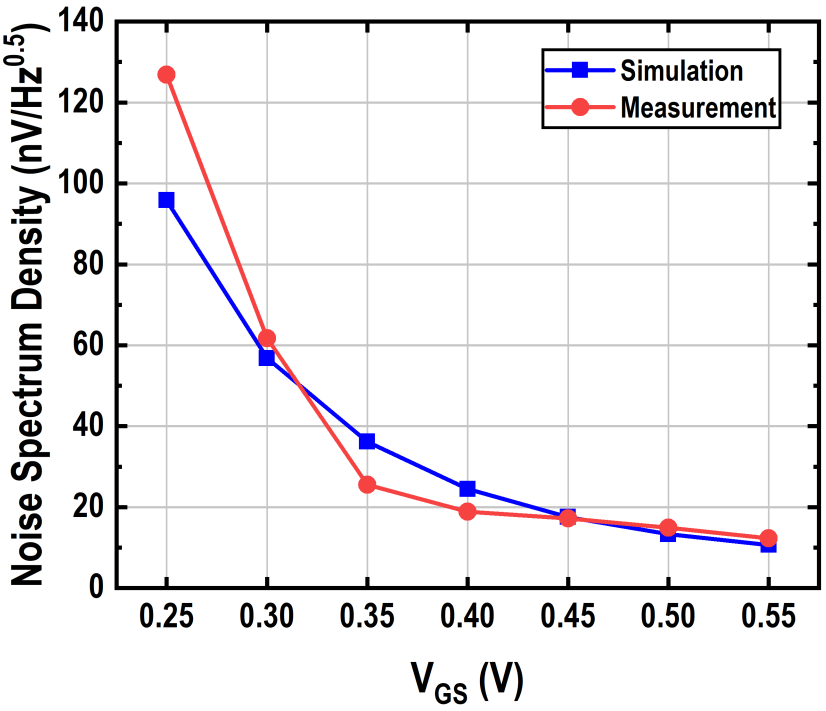


Figure 6-7: THz NMOS detector noise spectral density

Unfortunately, it is not possible to measure the noise spectral density of the THz PMOS detector because the PMOS drain node is a DC floating node. The PMOS drain is biased to a specific DC voltage when the PMOS source and drain are connected to an ultra-low-noise amplifier, disrupting the noise measurement.

The bit error rate test result of the THz WuRx is shown in Figure 6-9. As the output power of the VDI-WR3.4-VNAX is nearly constant at around -6 dBm, the received power at the WuRx can only be varied by adjusting the distance between the transmitter and WuRx. The received power is estimated based on the Friss transmission equation [12]. A sensitivity of -48 dBm with 10^{-3} bit error rate is obtained while consuming a measured power of 2.88 μW at the data rate of 1.02 kbps. With a 20% within-bit-level duty-cycling of the baseband amplifiers, the sensitivity of -47.8 dBm and data rate of 86.6 bps is obtained while reducing the average power to 748 nW. The power breakdown of the WuRx without duty-cycling is presented in Figure 6-10. The amplifier, filter, and biasing circuits consume 95.8 % of the power

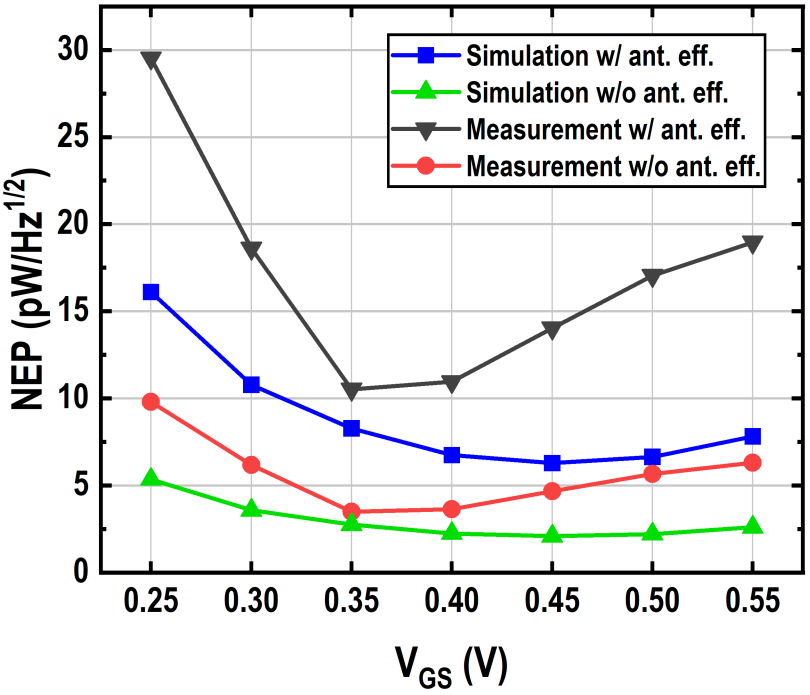


Figure 6-8: Measured NEP of NMOS THz detector

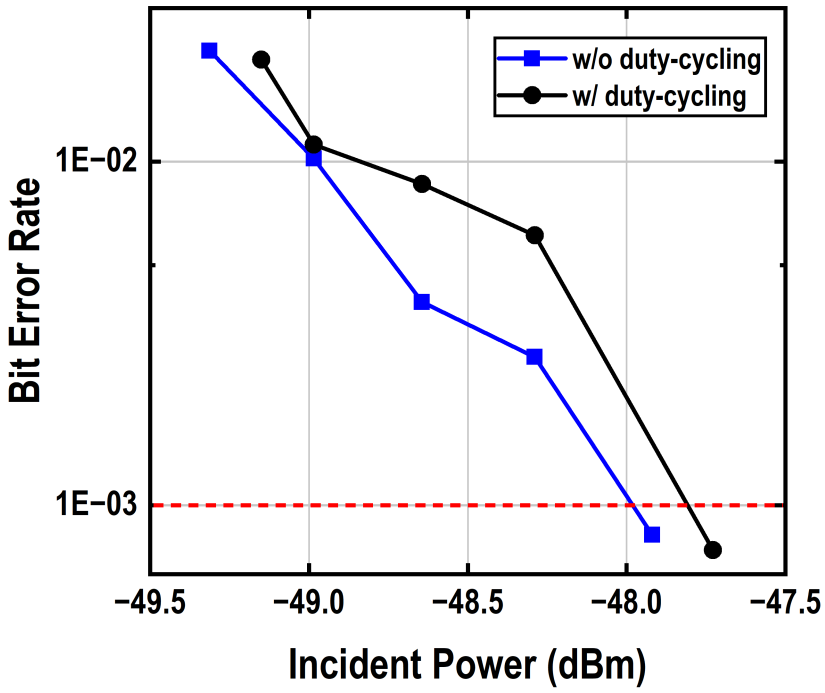


Figure 6-9: Received power versus bit error rate

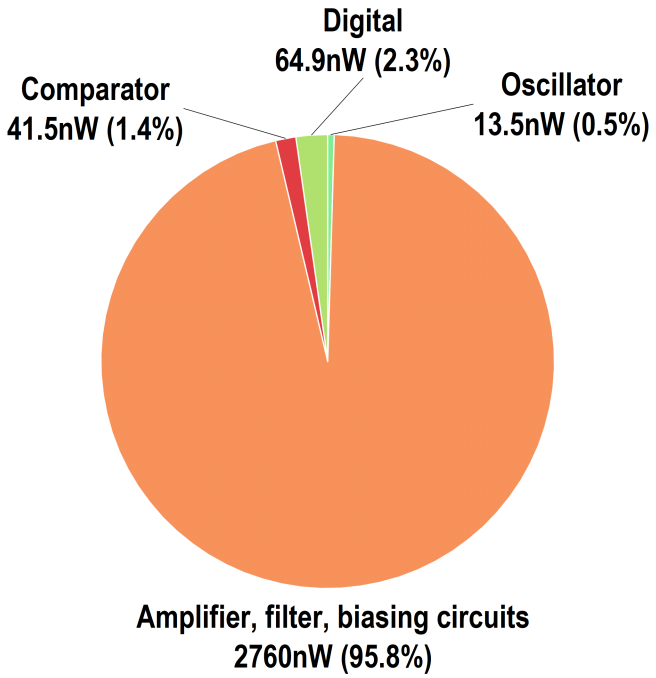


Figure 6-10: Power breakdown

consumption, mainly from the first stage LNA. As previously discussed in Chapter 4.1, entire power consumption can be reduced by lowering LNA current, but at the cost of sensitivity loss.

Figure 6-11 illustrates the various authenticated wake-up protocol scenarios. When a valid wake-up packet is successfully received (1, 7), the wake-up sign is generated, and the token is updated with the pre-shared key and incremented counter value (2, 8). In contrast, failed requests (3) or invalid requests (10) are ignored (4, 10). Failed requests can cause counter-desynchronization between the base node and WuRx (4), but subsequent valid packets resynchronize the two nodes (5, 6). The measured detailed time-domain waveform is shown in Figure 6-12. When a pre-shared 128-bit key is 128'h5e06d211e0842454d22391bd29022aa4, and a counter value is 3, the corresponding 92-bit wake-up packet is 92'hb6000036ff6294a9afcf94. When this wake-up packet is transmitted to the WuRx, both wake-up and resynchronization signals rise, which aligns with the authentication scenario in Figure 6-11. This verifies the proper

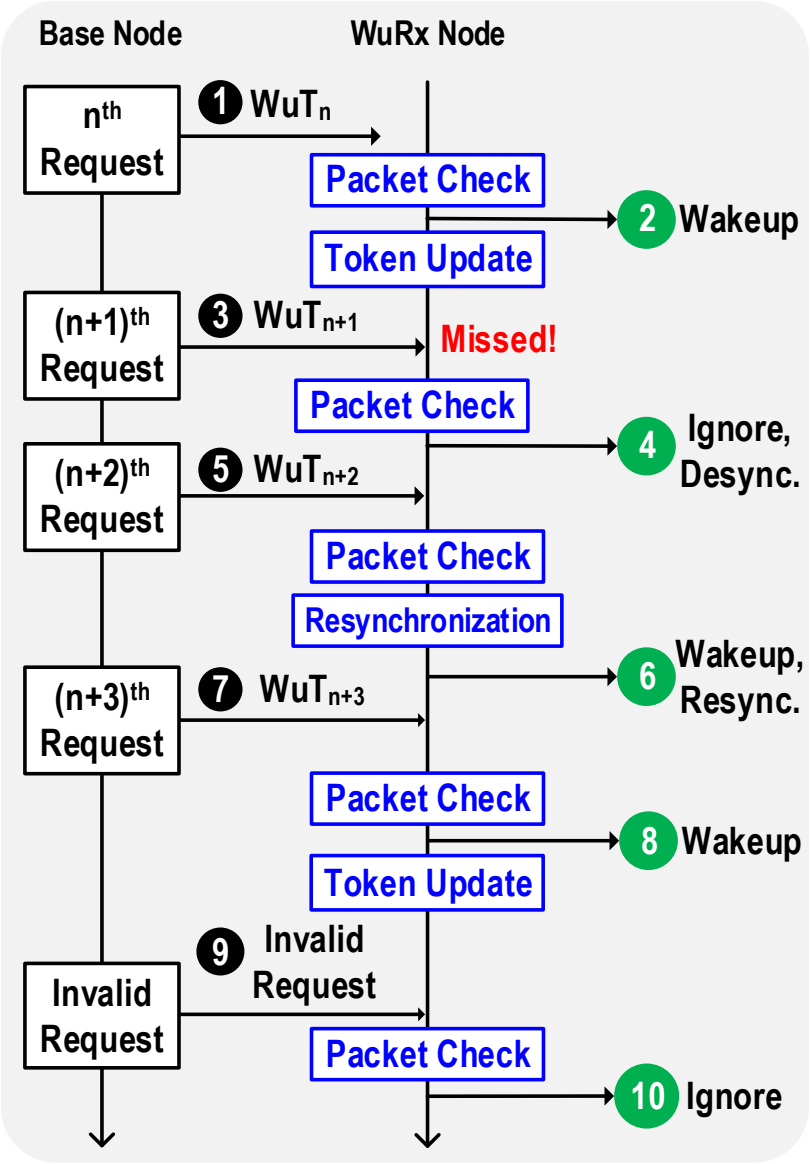


Figure 6-11: User scenario of the wake-up authentication protocol

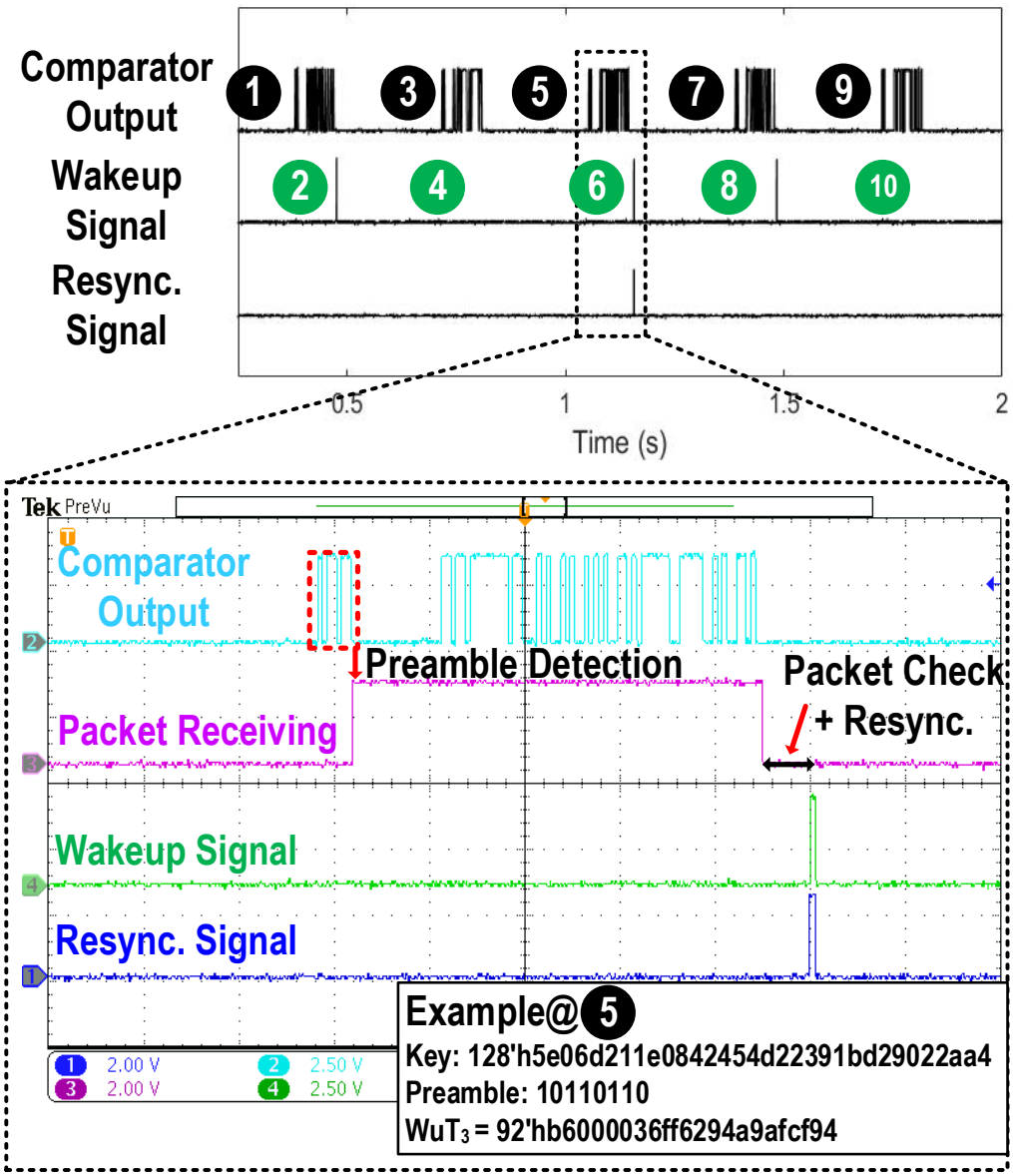
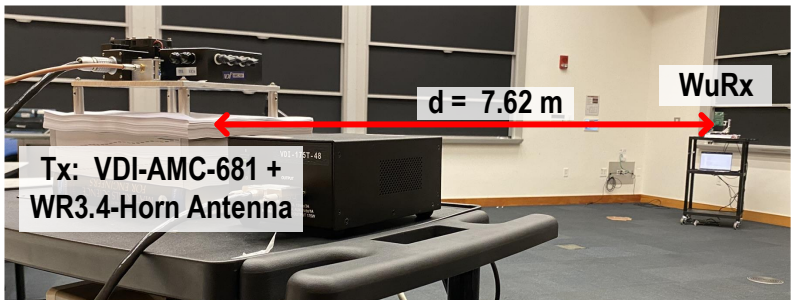


Figure 6-12: Measured time-domain waveform of the user scenario presented in Figure 6-11



Tx - WuRx Distance	Bit Error Rate (BER)
5.1 m	5.7×10^{-3}
7.6 m	1.7×10^{-2}

Figure 6-13: Wireless test setup at distances of several meters and results

functioning of the authentication process.

6.3 Demonstration

As discussed in Chapter 1.3, this thesis explores the potential WuRx application for large-scale deployment of miniaturized wireless nodes distributed over a wide area. To demonstrate the practical application of the THz WuRx, this section presents two examples: wireless test at distances of several meters and pairing with the THz reflectarray.

6.3.1 Wireless test at distances of several meters

The wireless communication distance at several meters tests is conducted to show communication distances of several meters. The measurement setup and the results are shown in Figure 6-13. The setup is similar to that in Figure 6-3, but with the exception of the VDI-WR3.4-VNAX being replaced by VDI amplifier-multiplier chain (VDI-AMC-681), which can provide a higher output power of 90 mW. The signal generator inputs an 11.0125 GHz, which is then multiplied 24 times by VDI-AMC-681. At the distance of 5.1 m and 7.6 m, the measured BERs are 5.7×10^{-3} and 1.7×10^{-2}, respectively.

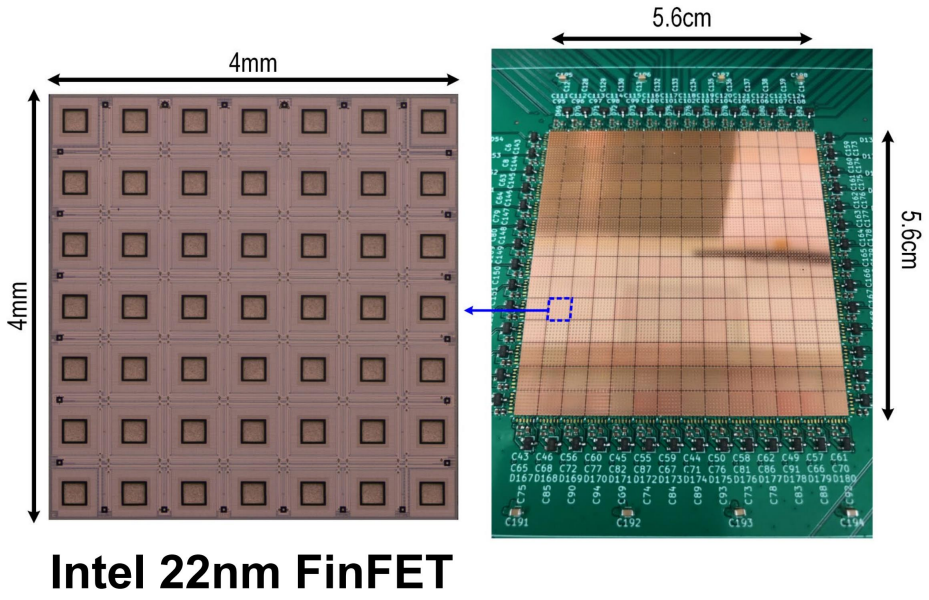


Figure 6-14: Photos of the CMOS beam-steerable THz reflectarray chip and the 14 × 14 array assembly, presented in [28]

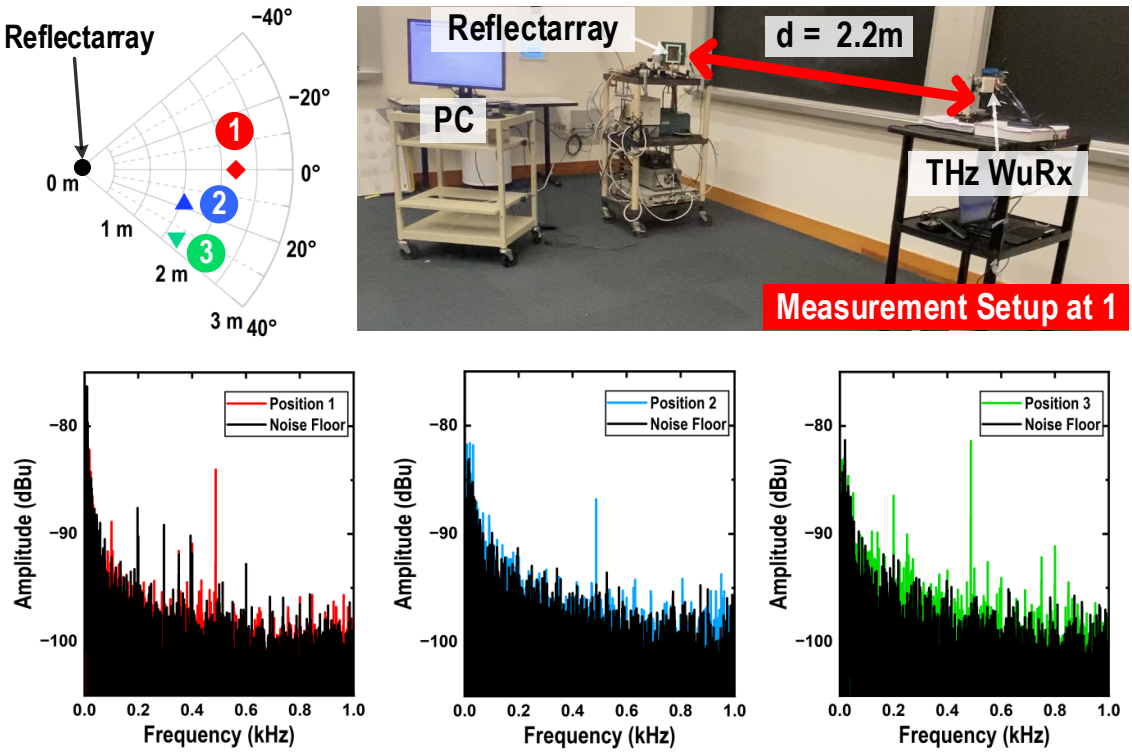


Figure 6-15: The measurement setup for wireless pairing test with THz reflectarray and obtained FFT results

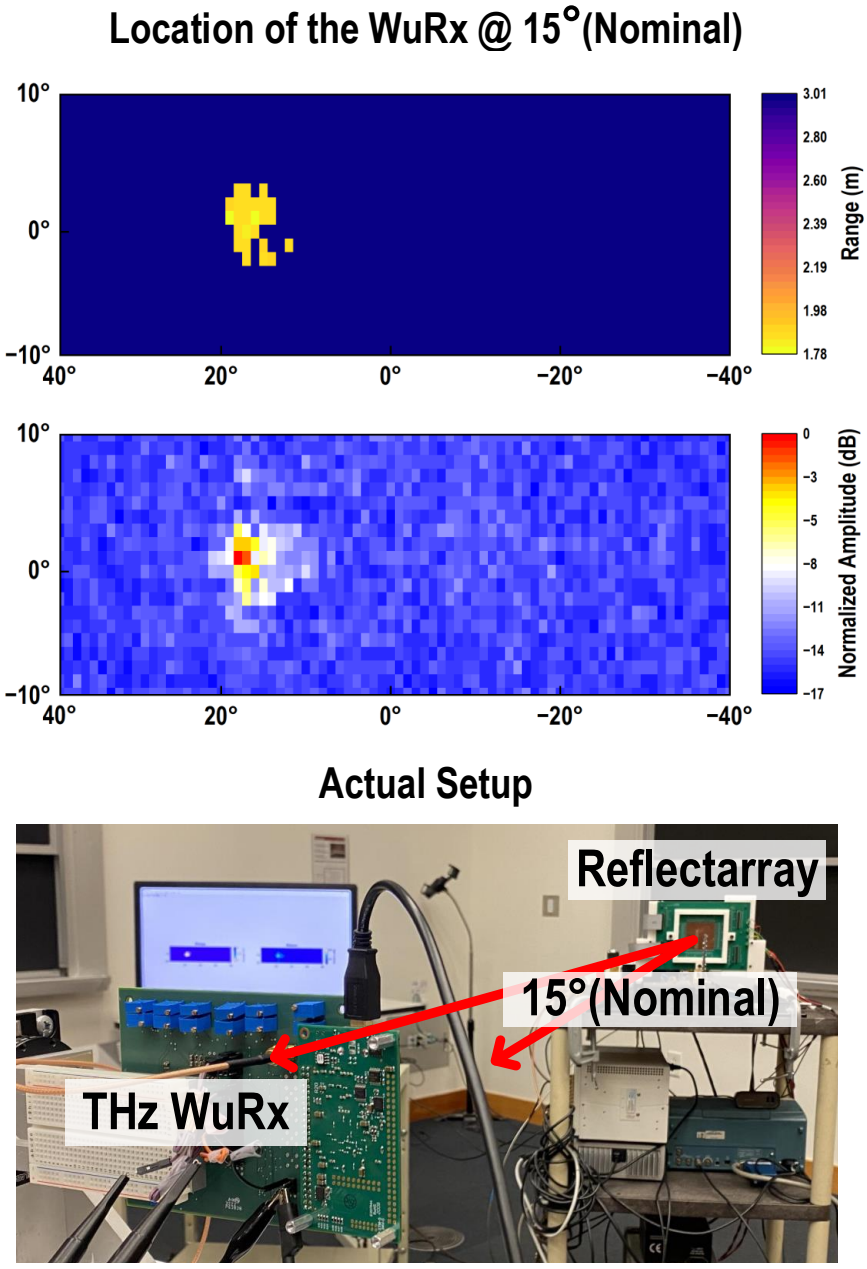


Figure 6-16: Radar image obtained from the THz reflectarray at 15 degrees (nominal) offset

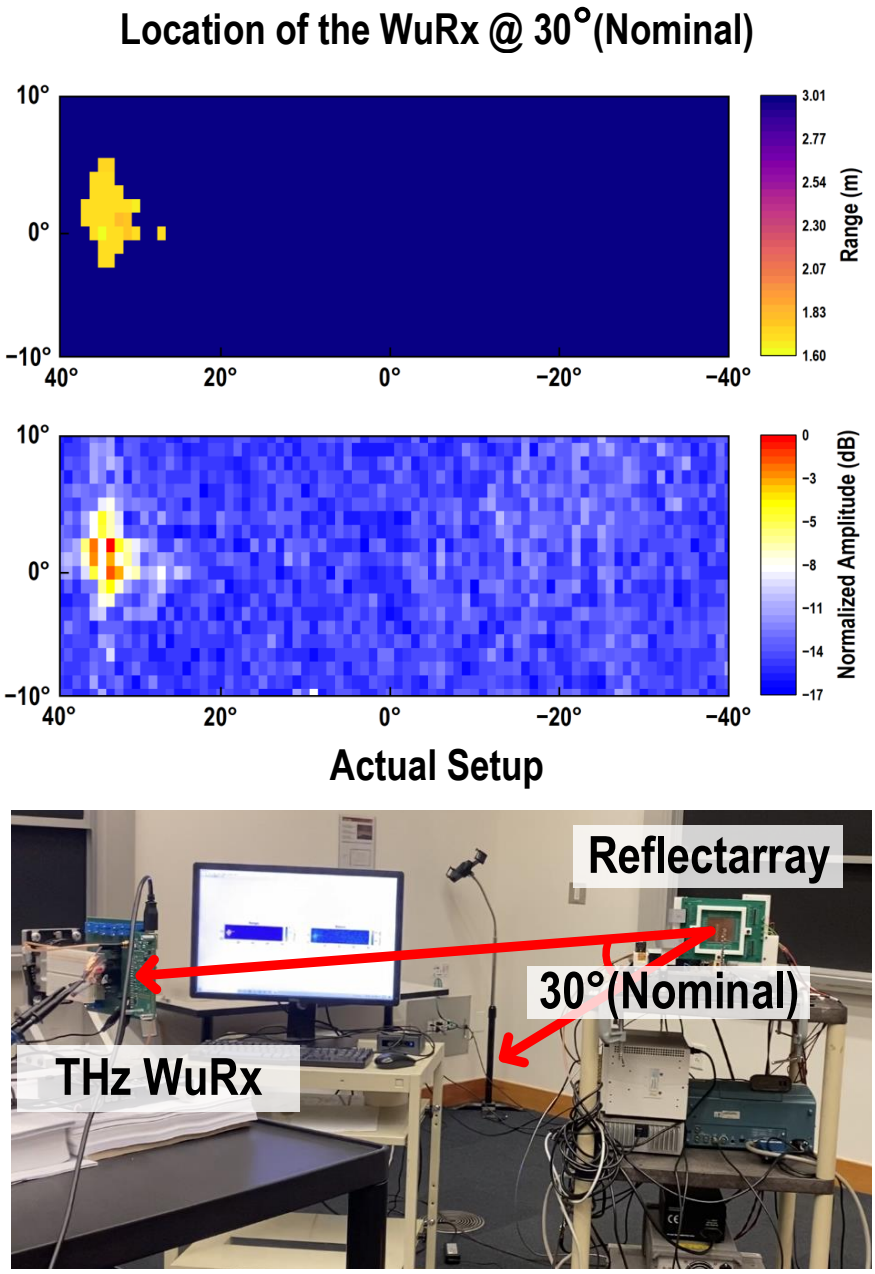


Figure 6-17: Radar image obtained from the THz reflectarray at 30 degrees (nominal) offset

Metric	Han, JSSC'13 [15]	Uzunkol, IMS'14 [37]	Ryu, T-ED'16 [32]	Shaulov, TSTT'21 [34]	This Work
Process Node	130nm CMOS	45nm CMOS SOI	65nm CMOS SOI	65nm CMOS	**65nm CMOS**
Frequency (GHz)	280	290-310	200	290-340	**264**
Responsivity (kV/W)	0.336	1.8	1.5	2	**2.6**
NEP (pW/Hz$^{\frac{1}{2}}$)	29	100	15	3.5	**10.5**

Table 6.1: Comparison table with THz detectors

6.3.2 Pairing with the THz reflectarray

A demonstration using a beam-steerable THz reflectarray [28], as shown in Figure 6-14, at the interrogator side is performed to address the limitation of fixed alignment between the interrogator and WuRx for real-world applicability. Figure 6-15 shows the measurement setup for pairing WuRx with the THz reflectarray. Upon the backscattering at the reflectarray, the 264.3 GHz beam is directed towards different directions and is OOK-modulated at 487.5 Hz. The WuRx is positioned at three different angles (nominal zero, 15, and 30 degrees), as shown in Figure 6-15. At each angle, the on-chip amplifier output is recorded by a portable oscilloscope and the resulting FFT spectra at different angles are shown in Figure 6-15. The location of WuRx is identified using radar imaging of the THz reflectarray. The resulting radar images, along with the corresponding actual setup at angles of 15 and 30 degrees (nominal), are presented in Figure 6-16 and Figure 6-17, respectively. The physical setup, FFT spectra, and radar images all indicate that the pairing of the THz reflectarray and WuRx is achieved. SNR limitations related to the reflectarray losses impede the fully recovering of the OOK-modulated signal through the on-chip comparator in the time domain; however, this demo showcases how large-scale distributed wireless nodes can be connected through a central THz hub. This is the first demonstration of pairing a CMOS beam-steerable THz reflectarray with a CMOS THz WuRx.

6.4 Comparison with the state of the arts

The comparison table with state-of-the-art THz detectors is shown in Table 6.1, and the comparison table with state-of-the-art radiator-integrated WuRxs is presented in Table 6.2. This work presents the WuRx with the smallest system area of 1.54 mm^2,

Metric	Lim, VLSI'16 [24]	Dadash, IMS'17 [9]	Sadagopan, RFIC'17 [33]	Rekhi, ISSCC'18 [31]	Jiang, JSSC'20 [18]	This Work
Transmit medium	Optical	mmWave	RF	Acoustic	RF	**THz**
Carrier frequency	352.9THz	78GHz	2.4GHz	∼57kHz	9GHz	**264GHz**
Die active area	0.85mm^2	0.44mm^2	1.1mm^2	1.5mm^2	4/12mm^2	**1.54mm^2**
System area/ Aperture	0.85mm^2	49mm^2	187.5mm^2	14.5mm^2	450mm^2	**1.54mm^2**
Process Node	180nm CMOS	55nm SiGe BiCMOS	65nm CMOS	65nm CMOS	65/180nm CMOS	**65nm CMOS**
Data Rate	5bps	Not shown	2.5kbps	336bps	33.3bps	**1.02kbps/ 86.6bps**^{a}
Sensitivity	-30.5dBm	-62dBm	-61.5dBm	-59.7dBm	-69.5dBm	**-48dBm/ -47.8dBm**^{a}
Power	380pW	25mW	365nW	8nW	22.3nW	**2.88μW/ 750nW**^{a}
External off-chip components	No	Antenna	Antenna	Transducer	Antenna	**No**
Beam-steering test?	No	No	No	No	No	**Yes**
Security	No	No	No	No	No	**Yes**

Table 6.2: Comparison table with the state-of-the-art radiator-integrated mm^2/cm^2-sized WuRxs

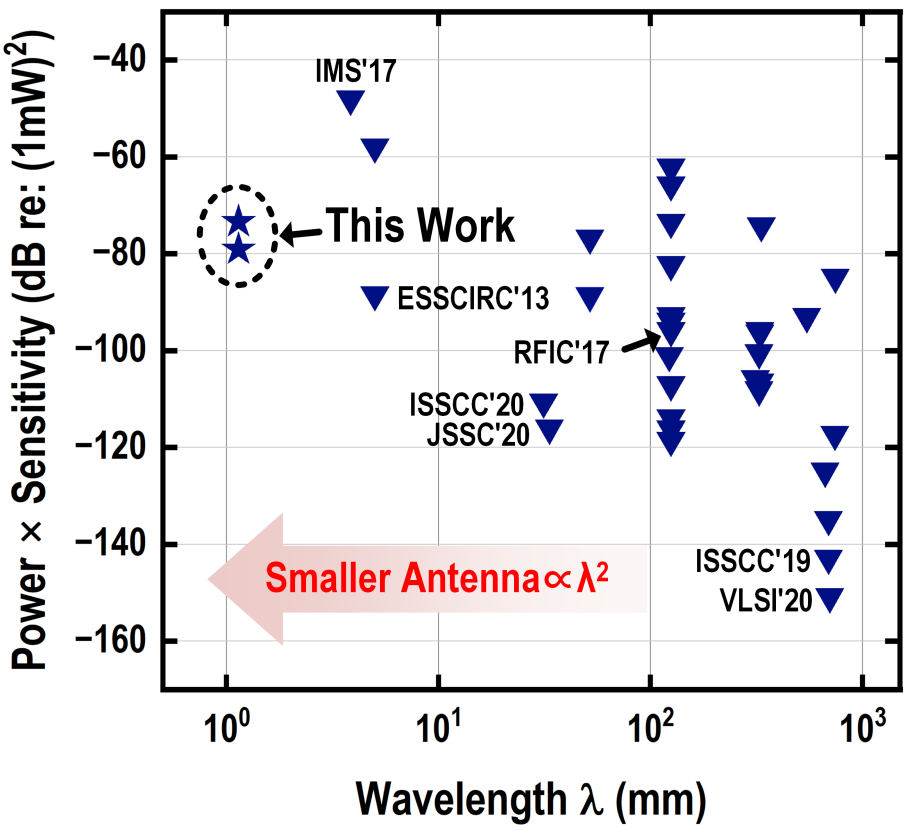


Figure 6-18: Comparison with State-of-the-art WuRxs Using RF-to-THz Spectrum

excluding the optical WuRx, which is susceptible to ambient light. Additionally, no other external off-chip components are required for matching network or radiator. Furthermore, this work also includes a beam-steering communication demo and security functionality.

Figure 6-18 presents the wavelength versus the power-sensitivity product among WuRxs using the RF-to-THz spectrum, which is regarded as an FoM for WuRxs for latency non-critical applications [38]. The graph clearly shows that this work pushes the design space boundary using THz frequencies, offering a low-cost, fully integrated solution for WuRx miniaturization.

Chapter 7

Conclusion

This chapter summarizes the work presented in this thesis and provides potential future research directions in the field of low-power, secure WuRx-miniaturization.

7.1 Summary

In this thesis, the motivation for the mm^2-sized WuRx system is presented with an overview of existing solutions. It then delves into requirements for THz wake-up and considerations for real-world applicability. Next, a novel THz receiver architecture with an on-chip antenna integrated THz detector pair and wake-up authentication engine is presented. Additionally, a new THz detector design based on dual-antenna is proposed to lower the noise-equivalent power, thereby providing a theoretical lower boundary for THz WuRx sensitivity. The thesis then advances to the baseband circuit design that develops from the detector to the low-power THz WuRx. A wake-up authentication is then developed to countermeasure the denial-of-sleep attack, which can drastically drain the battery power. A symmetric key encryption is used for the wake-up token generation, and a lightweight cryptographic algorithm GIFT-64 further provides a small area, low-power security solution. A prototype THz WuRx is fabricated in TSMC 65nm CMOS technology and achieved -48 dBm sensitivity at a DC power consumption of 2.88 μW. The system functionality of the WuRx is verified through the time-domain measurement. Also, wireless tests at distances of

several meters and with beam-steerable THz interrogator are introduced to showcase the practical application of THz WuRx. This thesis demonstrates the feasibility of a low-power secure wake-up receiver with on-chip integration and ultra-miniaturized size, which is expected to be used in a variety of applications, such as microbots and nano radios.

7.2 Future work

Several directions might be explored to enhance the system performance and broaden its potential applications. The following are some suggestions for future research directions:

- Fast, precise THz beam scanning and wake-up receiver wireless localization: The THz interrogator needs to scan a wide coverage area using radar or rely on information to find the location of the wireless nodes. To further expand the real-world applicability, precise and fast THz beam scanning protocol and circuits should be investigated.

- Physical layer security for wake-up receiver: there has been an increasing interest in physical layer security to secure the information based on information theory and signal processing [25]. This can relax the computation requirements of complicated cryptographic algorithms. However, applying this technique to a wake-up receiver needs to be investigated, which uses energy-constrained devices. As the number of wireless nodes increases, this way of communication can relax the requirements for key sharing between a base station and the wireless nodes.

Bibliography

[1] Subhadeep Banik, Sumit Kumar Pandey, Thomas Peyrin, Yu Sasaki, Siang Meng Sim, and Yosuke Todo. GIFT: A Small Present. In Wieland Fischer and Naofumi Homma, editors, *Cryptographic Hardware and Embedded Systems – CHES 2017*, pages 321–345, Cham, 2017. Springer International Publishing.

[2] Ray Beaulieu, Douglas Shors, Jason Smith, Stefan Treatman-Clark, Bryan Weeks, and Louis Wingers. The SIMON and SPECK Families of Lightweight Block Ciphers. Cryptology ePrint Archive, Paper 2013/404, 2013.

[3] Christof Beierle, Jérémy Jean, Stefan Kölbl, Gregor Leander, Amir Moradi, Thomas Peyrin, Yu Sasaki, Pascal Sasdrich, and Siang Meng Sim. The SKINNY Family of Block Ciphers and Its Low-Latency Variant MANTIS. In Matthew Robshaw and Jonathan Katz, editors, *Advances in Cryptology – CRYPTO 2016*, pages 123–153, Berlin, Heidelberg, 2016. Springer Berlin Heidelberg.

[4] A. Bogdanov, L. R. Knudsen, G. Leander, C. Paar, A. Poschmann, M. J. B. Robshaw, Y. Seurin, and C. Vikkelsoe. PRESENT: An Ultra-Lightweight Block Cipher. In Pascal Paillier and Ingrid Verbauwhede, editors, *Cryptographic Hardware and Embedded Systems - CHES 2007*, pages 450–466, Berlin, Heidelberg, 2007. Springer Berlin Heidelberg.

[5] R. Casanova, A. Dieguez, A. Arbat, O. Alonso, A. Sanuy, J. Canals, and J. Samitier. An Optically Programmable SoC for an Autonomous mm^3-sized Microrobot. In *2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, pages 302–303, 2009.

[6] R. Casanova, A. Dieguez, A. Sanuy, A. Arbat, O. Alonso, J. Canals, and J. Samitier. An ultra low power IC for an autonomous mm^3-sized microrobot. In *2007 IEEE Asian Solid-State Circuits Conference*, pages 55–58, 2007.

[7] Wenrong Chen, Lingxiang Li, Zhi Chen, Tony Quek, and Shaoqian Li. Enhancing THz/mmWave Network Beam Alignment With Integrated Sensing and Communication. *IEEE Communications Letters*, 26(7):1698–1702, 2022.

[8] Kyung-Sik Choi, Dzuhri Radityo Utomo, Keun-Mok Kim, Byeong-Hun Yun, Sang-Gug Lee, and In-Young Lee. 29.7 a 490ghz 32mw fully integrated cmos receiver adopting dual-locking fll. In *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, pages 452–454, 2020.

[9] M. Sadegh Dadash, Juergen Hasch, Pascal Chevalier, Andreia Cathelin, and Sorin P. Voinigescu. A W-band Active Millimeter-wave Tag IC with Wake-up Function. In *2017 IEEE MTT-S International Microwave Symposium (IMS)*, pages 1531–1534, 2017.

[10] Loïc Dalmasso, Florent Bruguier, Pascal Benoit, and Lionel Torres. Evaluation of SPN-Based Lightweight Crypto-Ciphers. *IEEE Access*, 7:10559–10567, 2019.

[11] Ilker Demirkol, Cem Ersoy, and Ertan Onur. Wake-up receivers for wireless sensor networks: benefits and challenges. *IEEE Wireless Communications*, 16(4):88–96, 2009.

[12] H.T. Friis. A note on a simple transmission formula. *Proceedings of the IRE*, 34(5):254–256, 1946.

[13] Edgar Felipe Garay, David Joseph Munzer, and Hua Wang. A 150 GHz Lens-Free Large FoV Regenerative 2 × 2 Transceiver Array With 31% DC-to-EIRP Efficiency and -70 dBm Sensitivity for a 70 cm Bidirectional Peer-to-Peer Link. *IEEE Journal of Solid-State Circuits*, 57(7):2102–2113, 2022.

[14] Ruonan Han, Yaming Zhang, Dominique Coquillat, Hadley Videlier, Wojciech Knap, Elliott Brown, and Kenneth K. O. A 280-GHz Schottky Diode Detector in 130-nm Digital CMOS. *IEEE Journal of Solid-State Circuits*, 46(11):2602–2612, 2011.

[15] Ruonan Han, Yaming Zhang, Youngwan Kim, Dae Yeon Kim, Hisashi Shichijo, Ehsan Afshari, and Kenneth K. O. Active Terahertz Imaging Using Schottky Diodes in CMOS: Array and 860-GHz Pixel. *IEEE Journal of Solid-State Circuits*, 48(10):2296–2308, 2013.

[16] Kuo-Ken Huang, Jonathan K. Brown, Nicholas Collins, Richard K. Sawyer, Farah B. Yahya, Alice Wang, Nathan E. Roberts, Benton H. Calhoun, and David D. Wentzloff. A Fully Integrated 2.7µW -70.2dBm-Sensitivity Wake-Up Receiver with Charge-Domain Analog Front-End, -16.5dB-SIR, FEC and Cryptographic Checksum. In *2021 IEEE International Solid- State Circuits Conference (ISSCC)*, volume 64, pages 306–308, 2021.

[17] Mohamed I. Ibrahim, Muhammad Ibrahim Wasiq Khan, Chiraag S. Juvekar, Wanyeong Jung, Rabia Tugce Yazicigil, Anantha P. Chandrakasan, and Ruonan Han. THzID: A 1.6mm^2 Package-Less Cryptographic Identification Tag with Backscattering and Beam-Steering at 260GHz. In *2020 IEEE International Solid-State Circuits Conference - (ISSCC)*, pages 454–456, 2020.

[18] Haowei Jiang, Po-Han Peter Wang, Li Gao, Corentin Pochet, Gabriel M. Rebeiz, Drew A. Hall, and Patrick P. Mercier. A 22.3-nW, 4.55 cm^2 Temperature-Robust Wake-Up Receiver Achieving a Sensitivity of -69.5 dBm at 9 GHz. *IEEE Journal of Solid-State Circuits*, 55(6):1530–1541, 2020.

[19] Wanyeong Jung, Sechang Oh, Suyoung Bang, Yoonmyung Lee, Zhiyoong Foo, Gyouho Kim, Yiqun Zhang, Dennis Sylvester, and David Blaauw. An Ultra-Low Power Fully Integrated Energy Harvester Based on Self-Oscillating Switched-Capacitor Voltage Doubler. *IEEE Journal of Solid-State Circuits*, 49(12):2800–2811, 2014.

[20] Anastasios Kavoukis and Salem Aljareh. Efficient time synchronized one-time password scheme to provide secure wake-up authentication on wireless sensor networks. *International Journal of Advanced Smart Sensor Network Systems*, 3, 02 2013.

[21] Muhammad Ibrahim Wasiq Khan, Suna Kim, Dae-Woong Park, Hyoung-Jun Kim, Seok-Kyun Han, and Sang-Gug Lee. Nonlinear Analysis of Nonresonant THz Response of MOSFET and Implementation of a High-Responsivity Cross-Coupled THz Detector. *IEEE Transactions on Terahertz Science and Technology*, 8(1):108–120, 2018.

[22] Muhammad Ibrahim Wasiq Khan, Eunseok Lee, Nathan M. Monroe, Anantha P. Chandrakasan, and Ruonan Han. A Dual-Antenna, 263-GHz Energy Harvester in CMOS for Ultra-Miniaturized Platforms with 13.6% RF-to-DC Conversion Efficiency at -8 dBm Input Power. In *2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 291–294, 2022.

[23] Inhee Lee, Dennis Sylvester, and David Blaauw. A Constant Energy-Per-Cycle Ring Oscillator Over a Wide Frequency Range for Wireless Sensor Nodes. *IEEE Journal of Solid-State Circuits*, 51(3):697–711, 2016.

[24] Wootaek Lim, Taekwang Jang, Inhee Lee, Hun-Seok Kim, Dennis Sylvester, and David Blaauw. A 380pW Dual Mode Optical Wake-up Receiver with Ambient Noise Cancellation. In *2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits)*, pages 1–2, 2016.

[25] Xuyang Lu, Suresh Venkatesh, Bingjun Tang, and Kaushik Sengupta. [4.6 space-time modulated 71-to-76ghz mm-wave transmitter array for physically secure directional wireless links. In *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*.

[26] Masaya Miyahara, Yusuke Asada, Daehwa Paik, and Akira Matsuzawa. A low-noise self-calibrating dynamic comparator for high-speed ADCs. In *2008 IEEE Asian Solid-State Circuits Conference*, pages 269–272, 2008.

[27] Masaya Miyahara and Akira Matsuzawa. A low-offset latched comparator using zero-static power dynamic offset cancellation technique. In *2009 IEEE Asian Solid-State Circuits Conference*, pages 233–236, 2009.

[28] Nathan M. Monroe, Georgios C. Dogiamis, Robert Stingel, Preston Myers, Xibi Chen, and Ruonan Han. Electronic THz Pencil Beam Forming and 2D Steering

for High Angular-Resolution Operation: A 98 × 98-Unit 265GHz CMOS Reflectarray with In-Unit Digital Beam Shaping and Squint Correction. In *2022 IEEE International Solid- State Circuits Conference (ISSCC)*, volume 65, pages 1–3, 2022.

[29] Maxime Montoya, Simone Bacles-Min, Anca Molnos, and Jacques J.A. Fournier. SWARD: A Secure WAke-up RaDio against Denial-of-Service on IoT Devices. In *Proceedings of the 11th ACM Conference on Security .. Privacy in Wireless and Mobile Networks*, WiSec '18, page 190–195, New York, NY, USA, 2018. Association for Computing Machinery.

[30] Muhammad Naveed Aman, Sachin Taneja, Biplab Sikdar, Kee Chaing Chua, and Massimo Alioto. Token-based security for the internet of things with dynamic energy-quality tradeoff. *IEEE Internet of Things Journal*, 6(2):2843–2859, 2019.

[31] Angad Singh Rekhi and Amin Arbabian. A 14.5mm^2 8nW -59.7dBm-Sensitivity Ultrasonic Wake-up Receiver for Power-, Area-, and Interference-constrained Applications. In *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, pages 454–456, 2018.

[32] Min Woo Ryu, Jeong Seop Lee, Kwan Sung Kim, Kibog Park, Jong-Ryul Yang, Seong-Tae Han, and Kyung Rok Kim. High-Performance Plasmonic THz Detector Based on Asymmetric FET With Vertically Integrated Antenna in CMOS Technology. *IEEE Transactions on Electron Devices*, 63(4):1742–1748, 2016.

[33] Kamala Raghavan Sadagopan, Jian Kang, Sanket Jain, Yogesh K. Ramadass, and Arun S. Natarajan. A 365nW -61.5 dBm Sensitivity, 1.875 cm^2 2.4 GHz Wake-up Receiver with Rectifier-Antenna Co-design for Passive Gain. *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 180–183, 2017.

[34] Edoh Shaulov, Samuel Jameson, and Eran Socher. A Zero Bias J-Band Antenna-Coupled Detector in 65-nm CMOS. *IEEE Transactions on Terahertz Science and Technology*, 11(1):62–69, 2021.

[35] Rabi Shrestha, Hichem Guerboukha, Zhaoji Fang, Edward Knightly, and Daniel M. Mittleman. Jamming a terahertz wireless link. *Nature Communications*, 13(1):3045, Jun 2022.

[36] Maryam Tabesh, Nemat Dolatsha, Amin Arbabian, and Ali M. Niknejad. A Power-Harvesting Pad-Less Millimeter-Sized Radio. *IEEE Journal of Solid-State Circuits*, 50(4):962–977, 2015.

[37] Mehmet Uzunkol, Jennifer M. Edwards, and Gabriel M. Rebeiz. A 0.3 THz 4 × 4 Cold-FET Imaging Array in 45 nm CMOS SOI. In *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*, pages 1–4, 2014.

[38] Po-Han Peter Wang, Haowei Jiang, Li Gao, Pinar Sen, Young-Han Kim, Gabriel M. Rebeiz, Patrick P. Mercier, and Drew A. Hall. A Near-Zero-Power

Wake-Up Receiver Achieving -69-dBm Sensitivity. *IEEE Journal of Solid-State Circuits*, 53(6):1640–1652, 2018.

[39] Mohamed Zgaren and Mohamad Sawan. A Low-Power Dual-Injection-Locked RF Receiver With FSK-to-OOK Conversion for Biomedical Implants. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 62(11):2748–2758, 2015.

[40] Q. Zhong, W.-Y. Choi, D.-Y. Kim, Z. Ahmad, R. Xu, Y. Zhang, R. Han, S. Kshattry, N. Sharma, Z.-Y. Chen, D. Shim, S. Sankaran, E.-Y. Seok, C. Mao, F. C. De Lucia, J. P. McMillan, C. F. Neese, I. Kim, I. Momson, P. Yelleswarapu, S. Dong, B. Pouya, P. Byreddy, Z. Chen, Y. Zhu, S. Ghosh, T. Dinh, F. Jalalibidgoli, J. Newman, and K. O. Kenneth. CMOS terahertz receivers. In *2018 IEEE Custom Integrated Circuits Conference (CICC)*, pages 1–8, 2018.