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GaN Memory Operational at 300 ℃

Mengyang Yuan, Qingyun Xie, John Niroula, Nadim Chowdhury, Tomás Palacios, *Fellow, IEEE*

***Abstract*— The most commonly used memory cells, namely a 32-bit × 10-bit read-only memory, a 1-bit 4-transistor static random-access memory, D latch, and D flip-flop (DFF), were demonstrated using high temperature (HT) GaN technology on a monolithically integrated GaN-on-Si platform and n-FET-only E/D-mode logic (E: enhancement, D: depletion). The memory cells exhibit stable operation at 300 ℃. A maximum clock frequency of 36 MHz at 300 ℃ was estimated for the DFF using the measured setup time. To the best of the authors' knowledge, the operational temperature of the reported prototypes represents the highest value for GaN memory, paving the way for the realization of robust mixed-signal systems operating at HT.**

***Index Terms*— GaN, transistor, high temperature, E/D-mode, memory, SRAM, ROM, D latch, D flip-flop**

I. Introduction

The rapid growth of high temperature (HT, ≥ 300 °C) electronic applications in the fields of aerospace, automotive, oil and gas exploration and more, requires fundamental advancements in semiconductor technology [1]. Considering their wide band gap, high chemical stability, very low intrinsic carrier concentration and excellent transport properties, gallium nitride (GaN) and other III-N materials stand out, alongside silicon carbide, as leading candidates. High performance (room temperature) transistors for RF, power, and increasingly, mixed-signal applications have been demonstrated [2]–[6]. Moreover, early studies on the HT characterization of III-N transistors [7]–[11] and MEMS sensors [12], [13] have been reported.

The focus of HT GaN electronics has thus far been basic *combinational logic* building blocks [14]–[17]. While these studies offer strong indication of the potential of GaN transistor technology for HT applications, the development of HT GaN ICs is still at its infancy due to the low level of complexity and integration demonstrated so far. Significant research is required for the next big leap of HT GaN mixed-signal ICs. Memory, which is the storage of state information, is a fundamental requirement of any complex digital system, and is realized using *sequential logic* circuits. There are very few reports of GaN sequential logic circuits [18]–[20], and only one experiment which demonstrates operation of such circuits at 160 °C [21] with little indication of their suitability for higher temperature (≥ 300 °C) operation.

Sequential logic requires a high level of uniformity and high operating frequency. Among the various GaN logic implementations and E-mode GaN transistor designs, the n-FET-only E/D-mode (E: enhancement, D: depletion) based on the p-GaN/AlGaN/GaN platform is preferentially considered for HT technology, thanks to its absence of gate dielectrics and its process simplicity. Unfortunately, previous experiments on GaN HT circuits [22] were based on relatively immature HT technologies with a low level of complexity.

This work demonstrates progress towards the integration of GaN HT electronics through an optimized process flow, in order to study the different trade-offs involved in HT memory cells. The proposed memory cells, namely (1) read-only memory (ROM), (2) static random-access memory (SRAM), (3) D latch, and (4) D flip-flop (DFF), show stable operation at 300 °C. The key performance metrics of the fabricated DFF, the most challenging implementation among all, were evaluated across temperature.

II. High Temperature GaN Platform

The GaN platform used in this work is based on epitaxial p-GaN/AlGaN/GaN on 150 mm Si wafer (Fig. 1(a)) which offers the scalable monolithic integration of E- and D-mode transistors [22]. The E-mode p-GaN-gate high electron mobility transistors (HEMTs) are fabricated with a self-aligned gate-first technology and tungsten gate (Schottky to p-GaN [23]). The back-end-of-line (BEOL) started with the deposition of Ni (30 nm)/Au (80 nm) to act as both D-mode Schottky gate and the first layer of interconnect. A SiO_2 interlayer dielectric was formed and opened through a via mask over the transistor electrodes. Ti (20 nm)/Au (200 nm) was deposited to serve as the contact pads and the second layer of interconnect.

In the E/D-mode logic implementation, the E-mode transistor serves as the driver and is therefore critical to the performance of the circuits. The E-mode transistor technology of this work was optimized for HT applications through features including, (1) a refractory metal (W) gate, and (2) self-alignment of p-GaN and metal through the gate-first process, which ensures a high metal/p-GaN interface quality and reduces gate leakage which would become significant problems at HT [24]. Early studies indicate HT (500 °C) robustness of the transistors through long-term survival tests [25]. The sheet resistances of the AlGaN/GaN channel, 1st-, and 2nd-interconnects are 460 Ω/□, 0.59 Ω/□, and 0.21 Ω/□, respectively. The E- and D-mode transistors share the same $L_G = L_{GS} = L_{GD} = 2$ μm.

In order to achieve high uniformity, a BCl_3/SF_6-based etch stop process was optimized for the selective removal of p-GaN over AlGaN. Good uniformity was observed at 25 °C across

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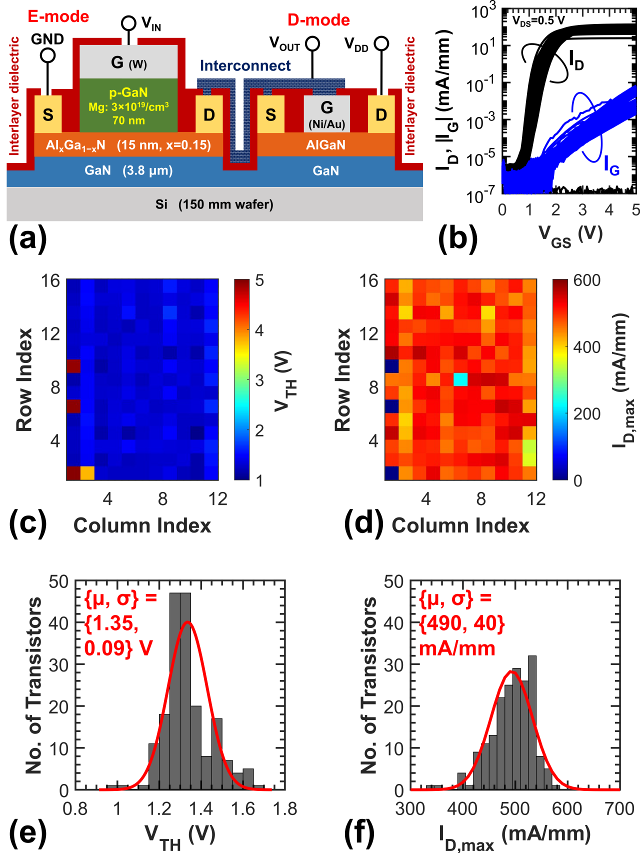

Fig. 1. Optimized GaN HT transistor technology used in this work. (a) Illustration of the E-mode transistor (p-GaN-gate AlGaN/GaN HEMT) and D-mode transistor (AlGaN/GaN HEMT) connected as an E/D-mode inverter. (b) Transfer characteristics with V_{DS} = 0.5 V, (c) distribution and (e) histogram of V_{TH}, and (d) distribution and (f) histogram of $I_{D,max}$ of a total of 192 E-mode transistors across a 1.2 cm × 1.2 cm sample with excellent average ON/OFF ratio $> 3 \times 10^7$. V_{TH} is measured at V_{DS} = 0.5 V. $I_{D,max}$ is measured at V_{GS} = 5 V. Measurements were conducted at 25 °C.

192 E-mode transistors ($W_G = 6$ μm) on a 1.2 cm × 1.2 cm sample with $V_{TH} = 1.35 \pm 0.09$ V, $I_{D,max} = 490 \pm 40$ mA/mm (Fig. 1(b)–(f)). As a reference, V_{TH} of D-mode transistors is -1 V.

While the results indicate the maturity of the proposed platform for higher integration in HT circuits, there are some outliers ($> 3\sigma$) in the transistor characteristics (5% for V_{th} and 3% for $I_{D,max}$) at room temperature. The circuits which incorporate transistors with significant outlying characteristics would likely not work as expected. The corresponding distributions were unable to be measured at HT due to the limitation of the measurement equipment. To mitigate the non-uniformity, in particular outlying characteristics, redundancy may be introduced to the circuit design, though this is beyond the scope of a proof-of-concept demonstration which is the focus of this work. Instead, the circuits in this work were designed with large tolerances to account for the majority of the measured distribution in transistor characteristics, therefore ensuring functionality.

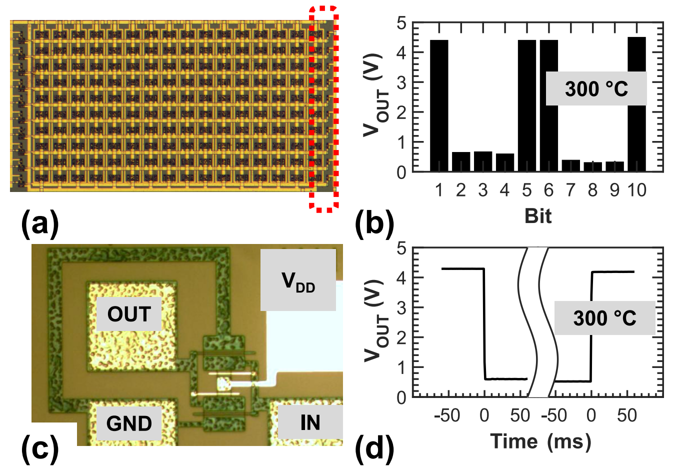

Fig. 2. GaN ROM and 4T-SRAM. (a) Micrograph of a 32-bit × 10-bit NOR-based ROM array. (b) The measured output of the 1st instruction stored in the ROM. (c) Micrograph of a 4T-SRAM. (d) Waveform of the SRAM operating at 300 °C with input transition from logic state '1' to '0' (left) and '0' to '1' (right).

III. Memory Characteristics

Several memory cells were implemented based on the GaN-on-Si platform reported in Section II. Monolithically integrated n-FET-only E/D-mode logic was used with $(W_G/L_G)_{\{E,D\}} = \{36/2, 12/2\}$ μm/μm. These devices yielded a drive/load ratio $\beta = (W/L)_E/(W/L)_D = 3$. V_{DD} was chosen to be 5 V to achieve a balance among speed, noise margin and power consumption. Future studies on the impact of V_{DD} scaling would allow for temperature-adaptive voltage techniques for operation over a wide temperature range [26]. The measurements were conducted in a probe station where the chip was placed on a thermal chuck up to 300 °C (rating of the chuck) in atmosphere. Each measurement was conducted 30 min. after the chuck reached the temperature set point.

As shown in Fig. 2(a), a 32 bit × 10 bit NOR-based ROM array was constructed with the 1st 10-bit instruction being enabled. The measured output matched the expected instruction with $BL[0:9] = [1000110001]$ at 300 °C (Fig. 2(b)). The maximum voltage of the output is limited to 4.5 V due to the voltage drop induced by the static current (IR drop) through the interconnect, which could be improved with an optimized interconnect metal stack. The minimum voltage is above 0 V due to the nature of n-FET-only logic. It should be noted that, due to the nature of the NOR-based implementation of ROM, the measurement of each word line is independent of the other lines. Therefore, the measurement of one line proves the feasibility of this implementation.

A four-transistor SRAM (4T-SRAM) was constructed from a pair of cross-coupled E/D-mode inverters as shown in Fig. 2(c). The input is first connected to ground ($V_{IN} = 0$ V) at $t = -50$ ms, driving V_{OUT} to logic state '1' (≈ 4.2 V) as shown in Fig. 2(d). At $t = 0$, V_{in} = 5 V is applied to the input to write a logic state '0' (≈ 0.5 V) into V_{OUT}. The above results demonstrate that the proposed 4T-SRAM cell functions as a stable memory cell at 300 °C.

A multiplexer-based negative D latch was constructed with input and output buffers using 13 transistors (Fig. 3(a)). As shown in Fig. 3(c), the latch becomes transparent while *CLK*

TABLE I. A summary of the published GaN- and SiC-based FFs.

Ref.	Semiconductor	Driver (Transistor)	Logic Family	L_G (μm)	V_{DD}/V_{SS} (V/V)	Temp. (°C)	f_{CLK} (MHz)*
[27]	SiC	MESFET	D-mode, RTL	2	$+5/-12$	300	–
[28]	SiC	JFET	D-mode, RTL	6	$+25/-25$	500	–
[29]	SiC	MOSFET	E/D-mode, DCFL	–	+20/GND	300	–
[18]	GaN	F implanted HEMT	E/D-mode, DCFL	0.8	+2/GND	25	–
[19]	GaN	–	E/D-mode, DCFL	1.2	+12/GND	25	10
[21]	GaN	Conventional HEMT	D-mode, RTL	0.5	$+14/-14$	25 160	2.5 1.6
This Work	GaN	p-GaN-gate	E/D-mode, DCFL	2	+5/GND	25 300	55 36

DCFL: direct coupled FET logic; RTL: resistor-transistor logic. * Estimated lower bound value.

is LOW, and holds its value while CLK is HIGH with $f_{CLK} = 1$ kHz and $f_{DATA} = 1.5$ kHz.

Lastly, a positive DFF was constructed using a *primary-secondary* (*master-slave*) configuration with a total of 20 transistors. For the fabricated positive flip-flop, the value of output (Q) is the value of input (D) sampled at the rising edge of CLK as shown in Fig. 3(c). A large voltage swing over 4 V could still be achieved for both the D latch and the DFF at 300 °C due to the matched temperature behavior of the ON-resistance for both the E- and D-mode transistors.

To evaluate the performance of the DFF across temperature, the setup time (t_{su}), an important metric to estimate maximum clock frequency ($f_{CLK} \approx 1/(t_{cq}+t_{su})$), was characterized up to 300 °C. t_{su} is the time that the data input (D) must be valid before the rising edge of CLK. Fig. 3(d) illustrates the determination of t_{su} at 300 °C, where D must be valid for a minimum of 14 ns before the rising edge of CLK ($t = 0$) to allow Q to reach state '1'. The measurement of CLK to Q time (t_{cq}) is limited due to the large load capacitance (350 pF) introduced by the measurement setup [14]. Therefore, $f_{CLK} = 1/(2 \times t_{su})$ is used to estimate the maximum clock frequency, because the estimated value of t_{cq} should be similar to the value of t_{su} based on the schematic of the fabricated DFF.

As presented in Fig. 3(e), when the operating temperature increased from 25 °C to 300 °C, the t_{su} increased from 9 ns to 14 ns, leading to a decrease of f_{CLK} from 55 MHz to 36 MHz. The decrease in performance is mainly due to the decreased ON-current of both E- and D-mode transistors resulting from the reduction of channel mobility at higher temperatures. Due to the distributions in V_{TH} and $I_{D,max}$ in the process reported in Section II, performance metrics such as t_{su} would be affected. Nevertheless, the circuits detailed here are representative circuits on the sample as a whole.

A summary of the GaN- and SiC-based FFs reported in the literature is presented in Table I. The reported DFF prototype based on the proposed GaN HT-robust technology features a simple voltage bias approach and competitive performance at room temperature. Furthermore, to the best of the authors' knowledge, the operational temperature of the reported DFF prototype is the highest among GaN-based FFs.

Several areas of improvement are identified to push the performance of GaN-based memory cells (including f_{CLK}) at HT: (1) aggressive transistor scaling, especially for the driver (E-mode transistor), to achieve higher current density with lower gate capacitance [30]; (2) reduced gate leakage at HT; (3) optimized layout for reduced parasitics and chip area; (4) HT-robust BEOL and advanced packaging [25], [31], [32]; (5) use of monolithically integrated GaN complementary technology based on a p-GaN/AlGaN/GaN-on-Si platform for higher power efficiency [14], [17], [30], [33].

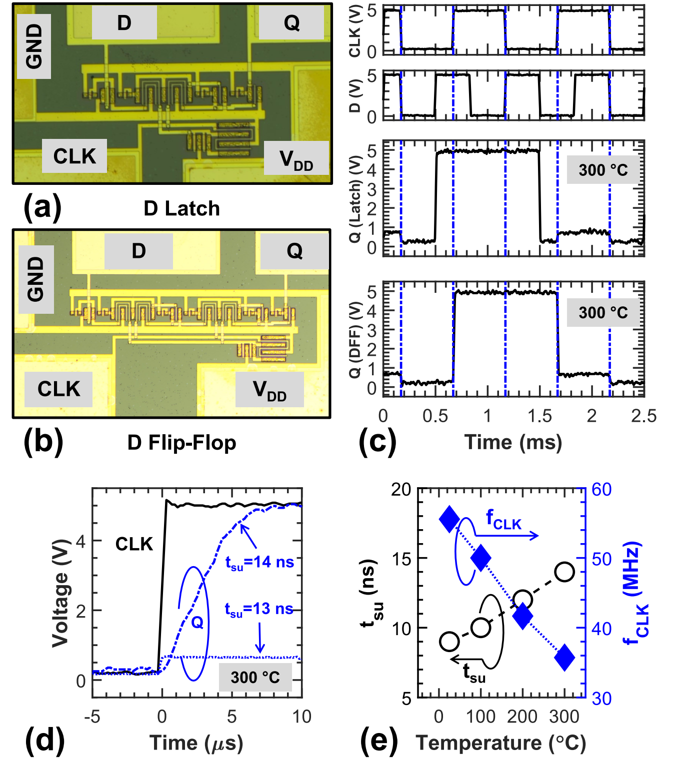

Fig. 3. GaN negative D latch and positive DFF. (a) Micrograph of a negative multiplexer-based latch. (b) Micrograph of a positive DFF using a *primary-secondary* configuration. (c) Waveforms of CLK at 1 kHz, D at 1.5 kHz, and outputs (Q) of both the D latch and the DFF. (d) Determination of t_{su}, using the output waveform of DFF at 300 °C as an example. (e) Trend of t_{su} and the estimated f_{CLK} *vs.* temperature.

IV. CONCLUSION

This letter reports the comprehensive demonstration of four different GaN memory cells, namely ROM, SRAM, D latch, and DFF, implemented by an optimized HT-robust GaN-on-Si technology. The memory cell prototypes were operational at 300 °C. By validating the potential of GaN memory cells, this work paves the way for the realization of robust mixed-signal circuits operating at HT.

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References

[1] P. Neudeck, R. Okojie, and L.-Y. Chen, "High-temperature electronics - a role for wide bandgap semiconductors?" *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1065–1076, June 2002. doi: 10.1109/JPROC.2002.1021571

[2] L. Li, K. Nomoto, M. Pan, W. Li, A. Hickman, J. Miller, K. Lee, Z. Hu, S. J. Bader, S. M. Lee, J. C. M. Hwang, D. Jena, and H. G. Xing, "GaN HEMTs on Si with regrown contacts and cutoff/maximum oscillation frequencies of 250/204 GHz," *IEEE Electron Device Letters*, vol. 41, no. 5, pp. 689–692, May 2020. doi: 10.1109/LED.2020.2984727

[3] K. H. Teo, Y. Zhang, N. Chowdhury, S. Rakheja, R. Ma, Q. Xie, E. Yagyu, K. Yamanaka, K. Li, and T. Palacios, "Emerging GaN technologies for power, RF, digital, and quantum computing applications: Recent advances and prospects," *Journal of Applied Physics*, vol. 130, no. 16, p. 160902, October 2021. doi: 10.1063/5.0061555

[4] H. Xie, Z. Liu, W. Hu, Y. Gao, H. T. Tan, K. E. Lee, Y.-X. Guo, J. Zhang, Y. Hao, and G. I. Ng, "AlN/GaN MISHEMTs on Si with in-situ SiN as a gate dielectric for power amplifiers in mobile SoCs," *Applied Physics Express*, vol. 15, no. 1, p. 016503, Jan 2022. doi: 10.35848/1882-0786/ac428b

[5] N. Chowdhury, Q. Xie, and T. Palacios, "Self-Aligned E-Mode GaN p-Channel FinFET With $I_{ON} > 100$ mA/mm and $I_{ON}/I_{OFF} > 10^7$," *IEEE Electron Device Letters*, vol. 43, no. 3, pp. 358–361, March 2022. doi: 10.1109/LED.2022.3140281

[6] G. Lyu, S. Feng, L. Zhang, T. Chen, J. Wei, and K. J. Chen, "GaN on engineered bulk silicon power integration platform with avalanche capability enabled by built-in Si PN junctions," *IEEE Electron Device Letters*, vol. 43, no. 11, pp. 1826–1829, Nov 2022. doi: 10.1109/LED.2022.3208909

[7] D. Maier, M. Alomari, N. Grandjean, J.-F. Carlin, M.-A. Diforte-Poisson, C. Dua, S. Delage, and E. Kohn, "InAlN/GaN HEMTs for operation in the 1000 °C regime: A first experiment," *IEEE Electron Device Letters*, vol. 33, no. 7, pp. 985–987, July 2012. doi: 10.1109/LED.2012.2196972

[8] A. Hassan, Y. Savaria, and M. Sawan, "GaN integration technology, an ideal candidate for high-temperature applications: A review," *IEEE Access*, vol. 6, pp. 78 790–78 802, Dec 2018. doi: 10.1109/ACCESS.2018.2885285

[9] S. R. Eisner, H. S. Alpert, C. A. Chapin, A. S. Yalamarthy, P. F. Satterthwaite, A. Nasiri, S. Port, S. Ang, and D. G. Senesky, "Extended exposure of gallium nitride heterostructure devices to a simulated venus environment," in *2021 IEEE Aerospace Conference (50100)*, March 2021. doi: 10.1109/AERO50100.2021.9438131 pp. 1–12.

[10] J. Liu, M. Xiao, R. Zhang, S. Pidaparthi, H. Cui, A. Edwards, M. Craven, L. Baubutr, C. Drowley, and Y. Zhang, "1.2-kV vertical GaN Fin-JFETs: High-temperature characteristics and avalanche capability," *IEEE Transactions on Electron Devices*, vol. 68, no. 4, pp. 2025–2032, April 2021. doi: 10.1109/TED.2021.3059192

[11] A. Li, M. Cui, Y. Shen, Z. Li, W. Liu, I. Z. Mitrovic, H. Wen, and C. Zhao, "Monolithic comparator and sawtooth generator of AlGaN/GaN MIS-HEMTs with threshold voltage modulation for high-temperature applications," *IEEE Transactions on Electron Devices*, vol. 68, no. 6, pp. 2673–2679, June 2021. doi: 10.1109/TED.2021.3075425

[12] Q. Xie, N. Wang, C. Sun, A. B. Randles, P. Singh, X. Zhang, and Y. Gu, "A passively temperature-compensated dual-frequency AlN-on-silicon resonator for accurate pressure sensing," in *2017 IEEE 30th International Conference on Micro Electro Mechanical Systems (MEMS)*, 2017. doi: 10.1109/MEMSYS.2017.7863574 pp. 977–980.

[13] G. Boldeiu, G. E. Ponchak, A. Nicoloiu, C. Nastase, I. Zdru, A. Dinescu, and A. Müller, "Investigation of temperature sensing capabilities of GaN/SiC and GaN/Sapphire surface acoustic wave devices," *IEEE Access*, vol. 10, pp. 741–752, Jan 2022. doi: 10.1109/ACCESS.2021.3137908

[14] N. Chowdhury, Q. Xie, M. Yuan, K. Cheng, H. W. Then, and T. Palacios, "Regrowth-free GaN-based complementary logic on a Si substrate," *IEEE Electron Device Letters*, vol. 41, no. 6, pp. 820–823, June 2020. doi: 10.1109/LED.2020.2987003

[15] P. Palacios, T. Zweipfennig, A. Ottaviani, M. Saeed, C. Beckmann, M. Alomari, G. Lukens, H. Kalisch, J. Burghartz, A. Vescan, and R. Negra, "3D integrated 300°C tunable RF oscillator exploiting AlGaN/GaN HEMT for high temperature applications," in *2021 IEEE MTT-S International Microwave Symposium (IMS)*, June 2021. doi: 10.1109/IMS19712.2021.9574881 pp. 519–522.

[16] R. Hao, C. Sun, B. Fang, N. Xu, Z. Tao, H. Zhang, X. Wei, W. Lin, X. Zhang, G. Yu, Z. Zeng, Y. Cai, X. Zhang, and B. Zhang, "Monolithic integration of enhancement/depletion-mode high electron mobility transistors using hydrogen plasma treatment," *Applied Physics Express*, vol. 12, no. 3, p. 036502, Feb 2019. doi: 10.7567/1882-0786/aafcd5

[17] L. Zhang, Z. Zheng, Y. Cheng, Y. H. Ng, S. Feng, W. Song, T. Chen, and K. J. Chen, "SiN/in-situ-GaON staggered gate stack on p-GaN for enhanced stability in buried-channel GaN p-FETs," in *2021 IEEE International Electron Devices Meeting (IEDM)*, Dec 2021. doi: 10.1109/IEDM19574.2021.9720653 pp. 5.3.1–5.3.4.

[18] Y. Xie, S. Quan, X. Ma, J. Zhang, Q. Li, and Y. Hao, "Monolithically integrated enhancement/depletion-mode AlGaN/GaN HEMT D flip-flop using fluorine plasma treatment," *Journal of Semiconductors*, vol. 32, no. 6, p. 065001, Jun 2011. doi: 10.1088/1674-4926/32/6/065001

[19] W. Jiang, M. Zaman, S. Murray, H. De Vleeschouwer, J. Roig, P. Moens, and O. Trescases, "GaN PMIC opportunities: Characterization of analog and digital building blocks in a 650V GaN-on-Si platform," in *2020 IEEE Symposium on VLSI Technology*, June 2020. doi: 10.1109/VLSITechnology18217.2020.9265112 pp. 1–2.

[20] Y. Zhu, M. Cui, A. Li, F. Li, H. Wen, and W. Liu, "Monolithic DFF-NAND and DFF-NOR logic circuits based on GaN MIS-HEMT," in *2021 International Conference on IC Design and Technology (ICICDT)*, Sep. 2021. doi: 10.1109/ICICDT51558.2021.9626401 pp. 1–4.

[21] A. Hassan, J.-P. Noël, Y. Savaria, and M. Sawan, "Circuit techniques in GaN technology for high-temperature environments," *Electronics*, vol. 11, no. 1, Jan 2022. doi: 10.3390/electronics11010042

[22] M. Yuan, Q. Xie, K. Fu, T. Hossain, J. Niroula, J. A. Greer, N. Chowdhury, Y. Zhao, and T. Palacios, "GaN ring oscillators operational at 500 °C based on a GaN-on-Si platform," *IEEE Electron Device Letters*, vol. 43, no. 11, pp. 1842–1845, Nov 2022. doi: 10.1109/LED.2022.3204566

[23] N. Chowdhury, Q. Xie, and T. Palacios, "Tungsten-gated GaN/AlGaN p-FET with $I_{max} > 120$ mA/mm on GaN-on-Si," *IEEE Electron Device Letters*, vol. 43, no. 4, pp. 545–548, April 2022. doi: 10.1109/LED.2022.3149659

[24] A. Stockman, E. Canato, A. Tajalli, M. Meneghini, G. Meneghesso, E. Zanoni, P. Moens, and B. Bakeroot, "On the origin of the leakage current in p-gate AlGaN/GaN HEMTs," in *2018 IEEE International Reliability Physics Symposium (IRPS)*, Mar 2018. doi: 10.1109/IRPS.2018.8353582 pp. 4B.5–1–4B.5–4.

[25] M. Yuan, Q. Xie, J. Niroula, M. F. Isamotu, N. S. Rajput, N. Chowdhury, and T. Palacios, "High temperature robustness of enhancement-mode p-GaN-Gated AlGaN/GaN HEMT technology," in *2022 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Nov 2022.

[26] J. W. Poulton, J. M. Wilson, W. J. Turner, B. Zimmer, X. Chen, S. S. Kudva, S. Song, S. G. Tell, N. Nedovic, W. Zhao, S. R. Sudhakaran, C. T. Gray, and W. J. Dally, "A 1.17-pJ/b, 25-Gb/s/pin ground-referenced single-ended serial link for off- and on-package communication using a process- and temperature-adaptive voltage regulator," *IEEE J. Solid-State Circuits*, vol. 54, no. 1, pp. 43–54, Jan 2019. doi: 10.1109/JSSC.2018.2875092

[27] M. Alexandru, V. Banu, X. Jordà, J. Montserrat, M. Vellvehi, D. Tournier, J. Millán, and P. Godignon, "SiC integrated circuit control electronics for high-temperature operation," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 5, pp. 3182–3191, May 2015. doi: 10.1109/TIE.2014.2379212

[28] P. G. Neudeck, D. J. Spry, M. J. Krasowski, N. F. Prokop, G. M. Beheim, L.-Y. Chen, and C. W. Chang, "Year-long 500°C operational demonstration of up-scaled 4H-SiC JFET integrated circuits," *Journal of Microelectronics and Electronic Packaging*, vol. 15, no. 4, pp. 163–170, Oct 2018. doi: 10.4071/imaps.729648

[29] A. Patil, N. Rao, and V. Tilak, "300C capable digital integrated circuits in SiC technology," *Materials Science Forum*, vol. 717, pp. 1261–1264, Jun 2012. doi: 10.4028/www.scientific.net/MSF.717-720.1261

[30] Q. Xie, M. Yuan, J. Niroula, J. A. Greer, N. S. Rajput, N. Chowdhury, and T. Palacios, "Highly-scaled self-aligned GaN complementary technology based on a GaN-on-Si platform," in *2022 IEEE International Electron Devices Meeting (IEDM)*, Dec 2022.

[31] A. A. Bajwa, Y. Qin, R. Reiner, R. Quay, and J. Wilde, "Assembly and packaging technologies for high-temperature and high-power GaN devices," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 5, no. 10, pp. 1402–1416, Oct 2015. doi: 10.1109/TCPMT.2015.2468595

[32] F. Li, "3D stacking of SiC integrated circuit chips with gold wire bonded interconnects for long-duration high-temperature applications," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 2022. doi: 10.1109/TCPMT.2022.3210477

[33] J. Chen, Z. Liu, H. Wang, Y. He, X. Zhu, J. Ning, J. Zhang, and Y. Hao, "A GaN complementary FET inverter with excellent noise

margins monolithically integrated with power gate-injection HEMTs," *IEEE Transactions on Electron Devices*, vol. 69, no. 1, pp. 51–56, Jan 2022. doi: 10.1109/TED.2021.3126267