Highly-Scaled Self-Aligned GaN Complementary Technology on a GaN-on-Si Platform

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***Abstract*—** This paper reports on the scaling of self-aligned GaN complementary technology on a GaN-on-Si platform to push its performance limits for circuit-level applications. The highly scaled self-aligned p-channel FinFET (fin width=20 nm) achieved $I_{D,max}$ of −300 mA/mm and R_{ON} of 27 Ω·mm, a record for metal organic chemical vapor deposition (MOCVD)-grown III-N p-FETs. A systematic study on impact of fin width scaling and recess depth in these transistors was conducted. A new self-aligned scaled n-channel p-GaN-gate FET process (n-FET), compatible with the p-FinFET, demonstrated enhancement-mode (E-mode) n-FETs (L_G=200 nm, $I_{D,max}$=525 mA/mm, R_{ON}=2.9 Ω·mm) on the same platform. The p-FETs and n-FETs feature competitive performance in their respective categories, and when taken together, offer a leading solution for GaN complementary technology on a GaN-on-Si platform.

I. Introduction

The rising performance of GaN power ICs has offered compactness, and record levels of efficiency and power for data centers, power adapters, electric vehicles (EVs), and 5G telecommunication systems [1]-[2]. However, the lack of a practical GaN p-FET introduces major limitations: (1) significant static power dissipation (resulting from the use of n-type enhancement-mode/depletion-mode logic); (2) a roadblock towards all-GaN integration (e.g. control loops, analog mixed-signal blocks) [3]. Furthermore, the availability of high-side switching GaN p-FETs would circumvent the switching speed bottleneck (limited common-mode transient immunity (CMTI) in the level shifter), therefore enabling more efficient power converters [4].

Several recent works have studied the feasibility of a GaN complementary technology (CT), realized using, (1) epitaxy regrowth to optimize n- and p-channels separately, by Chu *et al.*, offering great flexibility in epitaxy and transistor design [5]; (2) co-existence of n- and p-channels on p-GaN/GaN/AlGaN/GaN (or slight variations), by Hahn, Nakajima, Chowdhury *et al.*, offering ease of integration [6]-[11]. While each approach has its own merits, the next chapter of GaN CT research should adopt an application-driven perspective, where stringent requirements should be placed on, (1) easy integration of p-FETs and n-FETs on the same platform, ideally, without the need of regrowth steps that increase cost; (2) scalable platform for eventual commercialization; (3) ability to withstand the large heat generation in EVs, data centers, and base stations; (4) most importantly, high p-FET and n-FET performance. Thus far, discrete GaN p-FETs have received significant attention [12]–[17], but equal attention should be paid to their monolithic integration with n-FETs.

In view of the above application requirements and among the various options, the GaN CT platform in [9] based on p-GaN/AlGaN/GaN heterostructures stands out as a promising candidate. To this end, this work further develops this platform by studying the advanced scaling of self-aligned (SA) GaN CT based on a III-N heterostructure grown by MOCVD on 150 mm (6 in.) Si wafers (Fig. 1(a)). The epitaxial structure ("GaN-on-Si platform", Fig. 1(a)) is modified from earlier work by inserting a 1.5 nm AlN (in actual implementation, high Al composition AlGaN) layer, to achieve a p-GaN/UID-GaN/AlN/AlGaN/GaN (UID: unintentionally doped) heterostructure. The use of an AlN layer allows for polarization enhancement of the p-channel charge density [17] and a better etch stop during the selective etch of p-GaN/UID-GaN over AlGaN (a key process step for the n-FET). In addition, a conventional p-GaN/AlGaN/GaN epitaxial structure ("Epi-2"), which has been used in the past for p-FETs [16], was investigated for SA p-GaN-gate n-FETs to explore the epitaxial design space.

II. GaN SA P-FET: Design and Characterization

Channel length scaling of p-FETs realized by SA technology is critical to overcome the low hole mobility and to take advantage of field-induced acceptor ionization [18]-[19]. The SA FinFET architecture [15] offers new opportunities for p-FET design. This work studies the impact of fin width scaling and recess depth on these transistors.

The baseline process flow for p-FET fabrication is shown in Fig. 1(b)–(h), with key improvements with respect to [15] as follows. (1) Aggressive scaling of the fins was achieved using an optimized hydrogen silsesquioxane (HSQ)-based SA fin process, which reduces the fin widths to 20 nm while maintaining scaled L_{SD} of <200 nm (Fig. 1(c)); (2) Fins were aligned to the *m*-plane to achieve optimal sidewall smoothening by hot (75 °C) tetramethylammonium hydroxide (TMAH), which was reduced to 5 min. (from 15 min. in [15]) to prevent etching of the entire highly-scaled fins (Fig. 1(d)); (3) When compared to the planar channel, the fin channel has more surface area exposed to RIE plasma, therefore healing etch-induced damage by N_2 treatment [20] becomes critical. This treatment resulted in a 15% improvement in channel resistance (hence current level) (Fig. 1(e)); (4) Ti/Au sputtering was used for gate metallization to ensure conformality and good adhesion on the gate dielectric (Fig. 1(h)). An optimized SA p-FinFET is presented in Fig. 1(i).

The p-FET with the best overall characteristics (L_{SD}=175 nm, L_G self-aligned, fin width=20 nm) is presented in Fig. 2. $I_{D,max}$ of –300 mA/mm, R_{ON} of 27 Ω·mm, and current saturation at high gate overdrive were achieved. V_{th} of 3 V and a peak transconductance, g_m, of 13 mS/mm were found. A second g_m peak at large gate overdrive and highly negative V_{DS} likely indicates a second channel being activated. The current ON/OFF ratio is 200, limited by the leakage current through the gate dielectric. The hysteresis in the transistor transfer characteristics (~1 V) resembles the hysteresis in metal-

SiO_2-metal capacitors (Fig. 1(g)), which indicates the significant contribution of the gate dielectric quality (and p-GaN/dielectric interface) and need for further optimization [21].

The impact of two key device design parameters (fin width, gate recess depth) on DC output characteristics ($I_{D,max}$, R_{ON}) was systematically studied for GaN p-FinFETs for the first time, to better understand their design space. As the fin width is reduced below 50 nm, the current density and R_{ON} improves. However, this trend was not observed above 50 nm, possibly due to the significant reduction in the field-induced acceptor ionization effect [19]. A deeper gate recess was found to reduce current density, primarily due to reduction of carrier density in the p-channel, but is expected to significantly improve ON-OFF ratio and sub-threshold swing, as is the case for p-FETs based on similar epitaxial structures. Unfortunately, in this batch of fabricated transistors, the gate oxide quality was found to be the limiting factor for ON-OFF ratio. It follows that, the OFF-state characteristics were limited by gate control and drain-induced barrier lowering (DIBL), before a destructive breakdown at ~20 V.

Fig. 4 summarizes the performance of GaN p-FETs. To the best of the authors' knowledge, the best transistor in this work feature record current density for a MOCVD III-N p-FET (>2× the previous record, –140 mA/mm [15]), and competitive performance compared with GaN/AlN molecular beam epitaxy (MBE) counterparts [12]. The proposed p-FET technology is compatible with n-FETs fabricated on the same platform (discussed in Section III).

III. GaN SA N-FET: Design and Characterization

This work also seeks to improve the performance of GaN n-FETs based on the GaN CT platform through the development of a self-aligned (SA) gate technology. Approaches to the realization of GaN E-mode n-FETs include, F-plasma treatment of gate region [22], MIS-recessed gate [23], and p-GaN-gate [9]. The p-GaN-gated n-FET is chosen in this work because (1) easy integration with p-FET (Fig. 5(a)) and other power IC components [5]; (2) minimum degradation of as-grown gate surface (i.e. no photo-resist or etching), which reduces hysteresis and trapping issues. SA technology between the gate metal and the p-GaN gate would help to reduce gate capacitance, which is key for high-speed low/medium-voltage power ICs and analog mixed-signal applications. A self-aligned p-GaN-gate technique was previously explored [24]. This work proposes a simple gate-first process flow, which incorporates novel (1) metallization scheme with lower sheet resistance, (2) GaN/AlGaN selective etch recipe, (3) etch hard mask to improve gate length scalability.

The SA gate process begins with the blank sputtering of W (100 nm). Ni/Au/Ni (30/120/80 nm) was then patterned by electron beam lithography and lift-off (Fig. 5(b)). W was etched using the Ni/Au/Ni as a hard mask. Selective etching of p-GaN over AlGaN was achieved using SF_6/BCl_3 plasma (Fig. 5(c)). W was chosen because of its high melting point (necessary for a gate-first process) and Schottky behavior with p-GaN gates [20]. The use of Ni/Au/Ni on top allows for, (1) the top Ni to serve as the hard mask for gate definition; (2) the reduction of gate sheet resistance from 10 Ω/□ (W only) to <0.5 Ω/□ (this work). Ohmic contacts were formed by Ti/Al/Ni/Au alloyed at 800 °C (Fig. 5(d)). The typical contact resistance is ~0.75 Ω·mm (Fig. 5(e)). A scaled SA p-GaN-gated n-FET is presented in Fig. 5(f).

Scaled n-FETs with L_G=200 nm, L_{SD}=1.1 µm show good current saturation with $I_{D,max}$=525 mA/mm, R_{ON}=2.9 Ω·mm (Fig. 6(a)). The maximum achievable I_D is typically limited by (1) gate leakage which becomes significant at high gate overdrive; (2) carrier velocity in scaled transistors. E-mode operation (V_{th}≈1.6 V) was achieved (Fig. 6(b)). Peak g_m of 265 mS/mm reflects the good gate control.

The impact of gate length scaling on the SA p-GaN-gate n-FETs was studied (Fig. 7). In terms of ON-state characteristics, gate length scaling improves $I_{D,max}$. Furthermore, it is observed that V_{th} becomes more positive (E-mode) for scaled L_G<250 nm. In terms of OFF-state characteristics, a slightly longer L_G improves gate control and reduces leakage current before destructive breakdown (at ~50 V). It should be noted that, none of the transistors in this work feature any electric field management structure.

Although the scaled SA p-GaN-gate n-FET technology was originally developed for integration with p-FETs, it could also be useful in its own in GaN n-FET-only logic. To evaluate the robustness of this technology for such a possibility, the process flow was applied on a conventional p-GaN-gate epitaxial structure made of p-GaN (70 nm)/AlGaN (15 nm)/GaN ("Epi-2"). In the n-FETs based on Epi-2, better performance ($I_{D,max}$=750 mA/mm, R_{ON}=1.3 Ω·mm, higher current ON-OFF ratio, sharper ON-OFF transition, and negligible hysteresis (<0.1 V)) was observed (Fig. 8). The above improvements are attributed to the location of the gate metal closer (by ~25 nm) to the n-channel at the AlGaN/GaN interface, and better gate electrostatic control due to a simpler epitaxial structure (absence of UID-GaN and AlN) above the thinner AlGaN layer.

IV. Benchmarking and Conclusion

A summary of GaN CT based on the same platform is presented in Table I [5]-[11]. Two key DC parameters in power IC and VLSI are chosen, namely $|I_{D,max}|$ (ratio of n-FET/p-FET) and R_{ON} (ratio of p-FET/n-FET). In each case, on the basis of ensuring individual transistor performance, a ratio approaching unity (=1) is desired to achieve reasonable transistor sizing. To the best of the authors' knowledge, the scaled SA CT on GaN-on-Si platform feature the best ratios. The current density of the reported GaN CT is comparable with that of 5 V-rated Si CMOS in an industry 0.13 µm BCD process published in 2016 ($I_{D,max}${n, p}={520, −323} mA/mm) [25]. The results are attributed to innovation in device architecture (self-alignment), aggressive scaling, and advancement in processing technology. Furthermore, the results were achieved despite relatively high channel resistances (p=60 kΩ/□, n=800 Ω/□), which could be improved with epitaxial design optimization. It should be acknowledged, however, that significant research remains to be done in the co-optimization of this emerging GaN CT, in (1) device and process engineering to achieve a good balance of performance specifications (DC and switching); (2) epitaxial structure, to achieve lower channel resistances while ensuring carrier confinement.

In conclusion, advanced scaling based on self-aligned features, as proposed in this work, offers a viable technology path for future high performance GaN complementary technology based on a MOCVD GaN-on-Si platform. The scaled p-FETs and n-FETs achieve competitive performance in their respective categories, and when taken together, deliver a leading GaN CT solution. Further design innovation and engineering of the proposed technology would greatly benefit the eventual heterogeneous integration of GaN CT with Si CMOS to achieve multi-functional chips [26].

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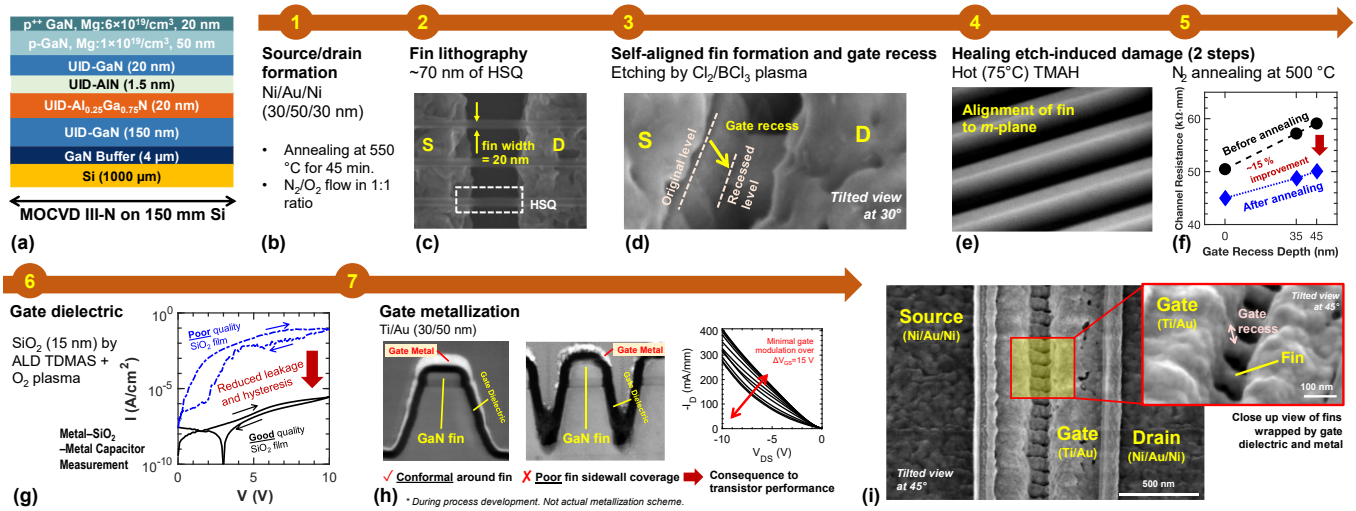

Fig. 1. Device structure of GaN p-FET. (a) Starting material, epitaxial III-N grown by metal organic chemical vapor deposition (MOCVD) on 150 mm (6 in.) Silicon wafer. Process flow of the self-aligned (SA) FinFET: (b) source/drain (S/D) formation using Ni/Au/Ni. (c) Fin lithography. An improved fin lithography process using thinner HSQ (70 nm) has allowed for aggressive scaling of the fins down to 20 nm fin width. The HSQ thickness was carefully calibrated to achieve a balance between fine lithography and subsequent etch resistance. Fins were aligned to the *m*-plane. (d) SA gate region. Two etches were conducted using medium-power Cl_2/BCl_3 plasma, (1) fin etch, using SiO_2 (formerly HSQ) as mask, which ensures self-alignment to S/D contacts, (2) after removal of SiO_2, SA gate recess using S/D contacts as mask. (e) Healing etch-induced damage (step 1), tetramethylammonium hydroxide (TMAH) treatment at 75 °C for 5 min. (f) Healing etch-induced damage (step 2), N_2 annealing at 500 °C for 1 hour. ~15 % improvement in the channel resistance for various recess depths is observed. (g) Atomic layer deposition (ALD) of gate dielectric (SiO_2). Typical characteristics of metal-insulator-metal (MIM) capacitors (with variation in quality of SiO_2 films) is presented. (h) Gate metallization. Conformal gate metallization is extremely important for gate control, especially for closely packed fins. (i) Image of the completed SA FinFET. The process flow images in (b)–(h) are for illustrative purposes only. Thanks to the aggressive scaling in both the lateral (L_{SD}) and fin dimensions, shortest L_{SD} of 120 nm and narrowest fin width of 20 nm were achieved.

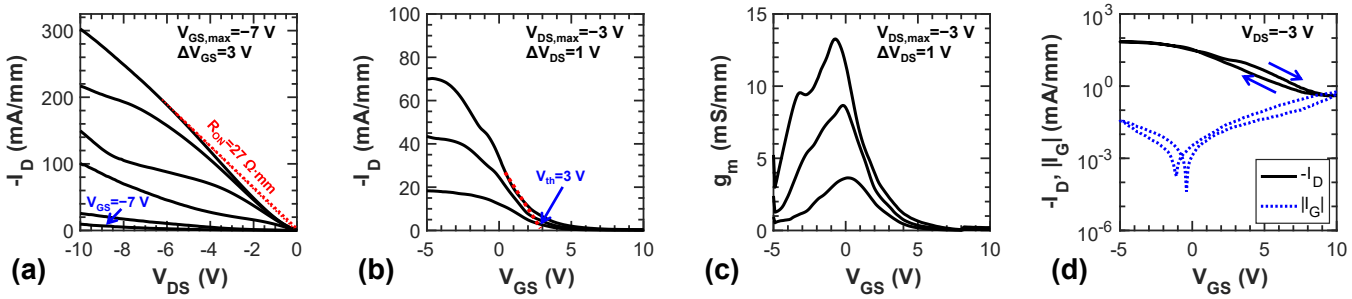

Fig. 2. Performance of p-FET with L_{SD}=175 nm (L_G self-aligned), fin width=20 nm. (a) Output characteristics, showing $I_{D,max}$=−300 mA/mm, R_{ON}=27 Ω·mm. Current saturation at higher gate overdrive was observed. Transfer characteristics: (b) Linear I_D *vs.* V_{GS}, showing V_{th}=3 V. (c) Transconductance vs. V_{GS}, showing peak g_m=13 mS/mm (V_{DS}=−3 V). The presence of a more pronounced second g_m peak at high gate overdrive and highly negative V_{DS} likely indicates the presence of a second channel being accumulated. Further physics studies would be required to understand the mechanism. (d) Logarithmic I_D *vs.* V_{GS}. Current ON/OFF ratio is 200, limited by the gate leakage. The hysteresis is typically attributed to the interface traps at the gate oxide [21]. These transistor characteristics resemble typical characteristics of metal-SiO_2-metal capacitors (Fig. 1(g)), which indicates the significant contribution of the gate dielectric quality and the need for its further optimization.

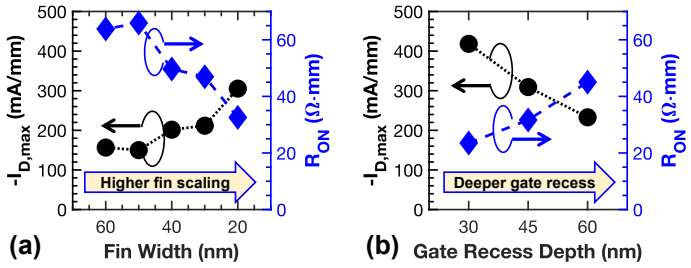

Fig. 3. Systematic study of the impact of (a) fin width and (b) gate recess depth on the performance ($-I_{D,max}$ and R_{ON}) of GaN p-FinFETs. SA p-FinFETs (~40 in total) fabricated in the same batch. Starting from larger fin widths at 50 nm, fin width scaling delivers benefits in terms of current density and R_{ON}. However, such a trend was not observed from larger fins, possibly due to the significant reduction in the field-induced acceptor ionization effect [19]. A deeper gate recess was found to reduce current density due to reduction of p-channel charge density and sidewall damage, but is expected to significantly improve ON-OFF ratio, as is the case for other p-FETs based on similar epitaxial structures. Unfortunately, in this batch of transistors, the gate oxide quality was found to be the limiting factor for ON-OFF ratio. $-I_{D,max}$ and R_{ON} were measured at V_{GS}=−7 V.

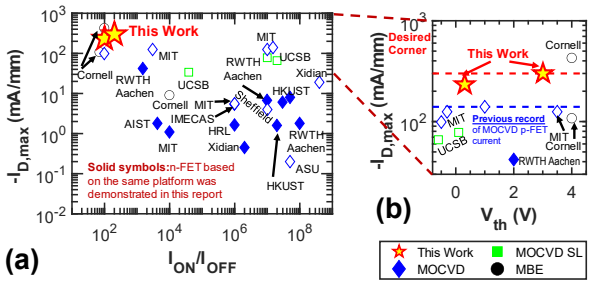

Fig. 4. Benchmarking of GaN p-FET. (a) ON-current and ON-OFF ratio. The two best p-FETs in this work show competitive performance compared with the existing MBE p-FET. (b) A zoom-in of the p-FETs with higher ON-current and a comparison of V_{th}. The reported p-FETs break the MOCVD III-N p-FET current density record (1.6~2.1× the previous record), and are located close to the desired corner. These results are achieved with a technology that is compatible with on-chip n-FET integration without any regrowth. Reports of n-FETs and p-FETs based on the same platform are highlighted using solid symbols, given that such experimental work would be valuable for the eventual realization of GaN complementary technology.

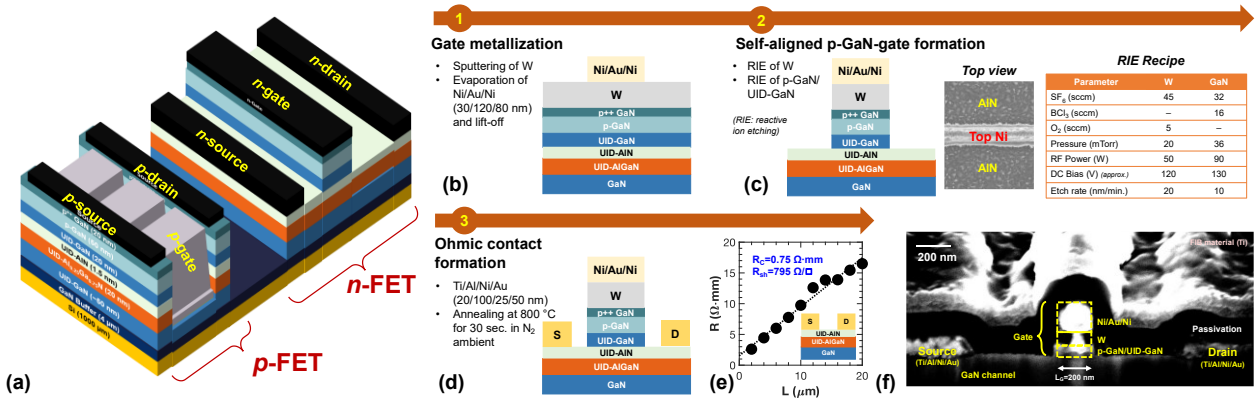

Fig. 5. Device structure of n-FET. (a) Illustration of monolithic integration of n-FET and p-FET on the same platform (Fig. 1(a)) without the need of any regrowth. Process flow: (b) Conformal deposition of W, then patterning of Ni/Au/Ni (30/120/80 nm) using electron beam lithography and lift-off. (c) Self-aligned (SA) p-GaN gate formation is achieved using reactive ion etching (RIE) of W and GaN (recipes are included). AlN layer aids the etch stop to minimize damage to the n-channel. (d) Formation of ohmic contacts using alloyed Ti/Al/Ni/Au. (e) TLM measurement of ohmic contacts. Contact resistance of 0.75 Ω·mm was obtained, which could be further optimized for contact formation through the AlN/AlGaN barrier. (f) Cross-sectional image of the schematic shown in (d). In the SA p-GaN-gate, the extent of the p-GaN region is defined by the top Ni/Au/Ni. The undercut in W could be significantly reduced by using inductively coupled plasma (ICP) RIE and/or sidewall spacers [24].

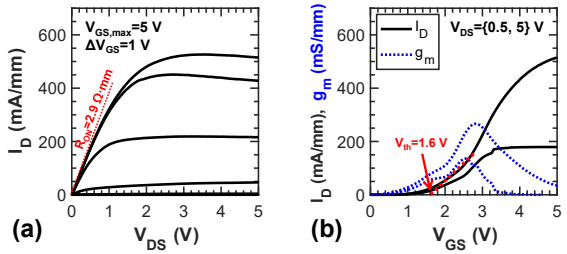

Fig. 6. Performance of n-FET with L_G=200 nm, L_{SD}=1.1 μm. (a) Output characteristics, showing R_{ON}=2.9 Ω·mm and good current saturation with $I_{D,max}$=525 mA/mm (calculated at V_{GS}=5 V). (b) Transfer characteristics, showing V_{th}≈1.6 V and peak g_m=265 mS/mm.

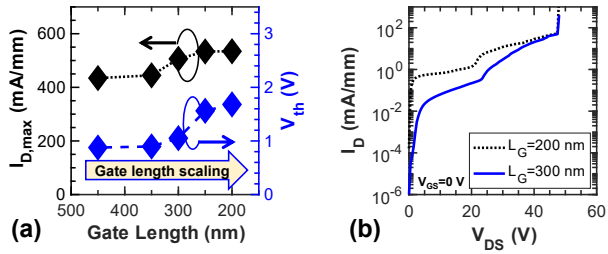

Fig. 7. Gate length scaling of SA p-GaN-gate n-FETs. (a) ON-state characteristics. ~40 transistors fabricated in the same batch were studied. Gate length scaling would deliver benefits in $I_{D,max}$ (extracted at V_{GS}=5 V). Furthermore, it is observed that, V_{th} becomes more positive (E-mode) for scaled L_G<250 nm, therefore limiting the maximum achievable $I_{D,max}$. Further studies would be desired to understand this phenomenon. (b) OFF-state characteristics, without any electric field management structures (e.g. field plate). A slightly longer gate length would improve the gate control and therefore reduce the leakage current before destructive breakdown (both at ~50 V due to destruction of probe pad). In these transistors, L_{GS}=L_{GD}=450 nm.

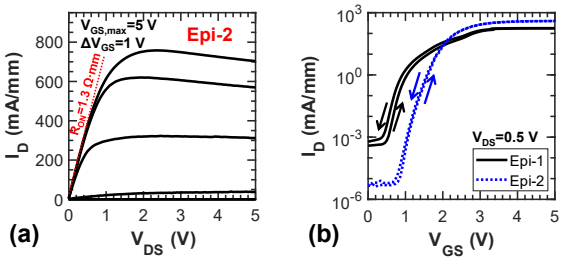

Fig. 8. n-FETs (L_G=200 nm, L_{SD}=1.1 μm) were fabricated on a conventional p-GaN (70 nm)/AlGaN (18 nm)/GaN epitaxial structure (Epi-2) used for E-mode n-FETs. (a) Output characteristics, showing R_{ON}=1.3 Ω·mm and good current saturation with $I_{D,max}$=750 mA/mm (calculated at V_{GS}=5 V). (b) Comparison of the performance n-FETs based on Epi-1 (Fig. 1(a), the GaN CT platform)) and Epi-2. By using Epi-2, a more positive V_{th} (E-mode), an improvement in current ON-OFF ratio (by more than two orders of magnitude) and a sharper ON/OFF transition was achieved. This is attributed to the location of the gate metal closer to the channel at the AlGaN/GaN interface, as well as better gate electrostatic control due to a simpler epitaxial structure above the AlGaN barrier.

Table I. Benchmarking of GaN CT demonstrations. Two parameters, $|I_{D,max}|$ (ratio of n-FET/p-FET) and R_{ON} (ratio of p-FET/n-FET), are chosen because of their significance in power IC and VLSI design. In each case, on the basis of ensuring individual transistor performance, a ratio approaching unity (=1) is desired to achieve reasonable transistor sizing. To the best of the authors' knowledge, among recent demonstrations, the proposed n-FET and p-FET on the GaN-on-Si platform feature the best $I_{D,max}$ and R_{ON} combination in the respective categories. When combined, the proposed GaN CT features the best ratios among recent demonstrations. It should be acknowledged that, co-design of the n-FET and p-FET would be required to allow for simultaneous E-mode operation.

Affiliation	Year	Epitaxial Structure	$\|I_{D,max}\|$ [mA/mm] (n/p-FET)	R_{ON} [Ω·mm] (p/n-FET)	V_{th} [V] (n/p-FET)
RWTH Aachen [6]	2014	p-GaN/GaN/AlInGaN/GaN	10/0.2=**500**	-	0.5/−0.5
			800/15=**53**	-	−11/2
AIST [7], [8]	2015	p-GaN/GaN/AlGaN/GaN	16/1.8=**8.8**	30000/660=**45**	−2/4
	2018	p-GaN/GaN/AlGaN/GaN	0.14/0.01=**14**	20000/6000=**3.3**	4/−2.7
HRL [5]	2016	(1) AlGaN/GaN (2) p-GaN/ GaN/AlGaN *(regrowth)*	230/1.65=**140**	1314/10=**131**	0/0
MIT [9]	2020	p-GaN/GaN/AlGaN/GaN	310/1.2=**258**	2300/6=**383**	0.2/−1
HKUST [10]	2021	p-GaN/AlGaN/GaN	170/1.65=**103**	4500/12.7=**354**	2.5/−2
Xidian U. [11]	2022	p-GaN/AlGaN/GaN	275/0.45=**611**	8900/9.1=**978**	2.3/−2
This Work	2022	p-GaN/GaN/AlN/AlGaN/GaN	525/300=**1.75**	27/2.9=**9.3**	1.6/3

Values are based on best estimates. Epitaxial structure is unintentionally doped (UID) unless otherwise stated.

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