The Connection Machine CM-5, Moore's Law, and the Future of Computational Performance

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Bradley C. Kuszmaul
kuszmaul@gmail.com
Independent Consultant
Lexington, Massachusetts, USA

Charles E. Leiserson
cel@mit.edu
Massachusetts Institute of Technology
Cambridge, Massachusetts, USA

ABSTRACT

In June 1993, the Connection Machine Model CM-5 Supercomputer [6] manufactured by Thinking Machines Corporation was the most powerful computer in the world [10]. At the time, Moore's Law [8, 9] was about halfway through its roughly 60-year reign, and indeed, your smartphone today is likely more powerful than the CM-5, no matter how you want to measure it: FLOPS, bisection bandwidth, storage, etc. As one of the earliest commercially successful parallel supercomputers, the CM-5 network architecture introduced many innovations: a user-level network interface, a fat-tree [5] data network, a global synchronization network, and a system-wide parallel diagnostic network. The CM-5 architecture delivered unprecedented computing power for its day while also simplifying the process of coding for parallel performance.

The CM-5 inspired the development of significant software and algorithmic technology still in use today, including work/span analysis [2, Chapter 26], the LogP performance model [3], data-parallel computing [4], task-parallel computing [2, Chapter 26], and work-stealing algorithms [1]. Indeed, although the focus at the time was on the CM-5's hardware innovations, its legacy in the areas of programming models, algorithms, and software performance engineering may be the CM-5's greater contribution. The recent end of Moore's Law [7]—and with it, the attenuation of exponential gains in hardware performance—portends increased relevance of research in these areas, especially in software performance engineering.

CCS CONCEPTS

• **Computer systems organization → Interconnection architectures**; **Parallel architectures**.

KEYWORDS

Supercomputers, Moore's Law

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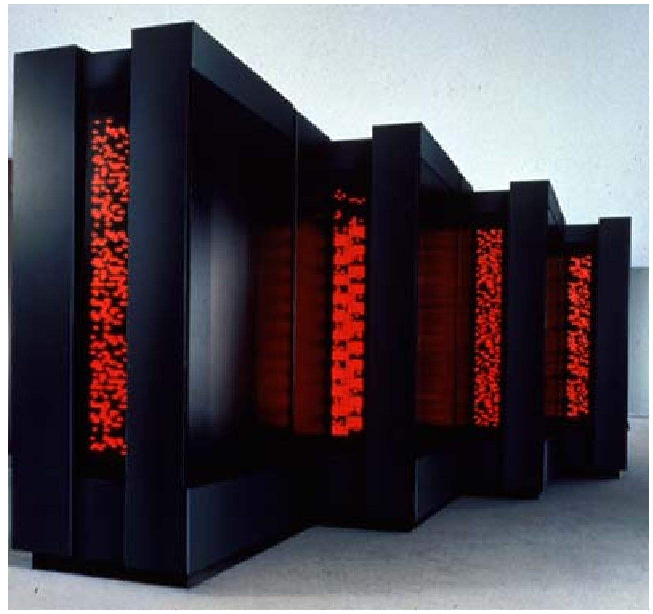

BIOGRAPHY

Bradley C. Kuszmaul's research focuses on developing computer systems that behave well both in practice and in theory. He received a Ph.D. in computer science and engineering from MIT in 1994. He has served as Assistant Professor of Computer Science at Yale, Architect of Akamai's distributed data-collection system, Research Scientist at MIT, Founder and Chief Architect at Tokutek, Architect of Oracle's File Storage Service cloud offering, and Senior Software Engineer at Google.

Charles E. Leiserson is Edwin Sibley Webster Professor of Computer Science and Engineering in MIT's Department of Electrical Engineering and Computer Science (EECS) and a member and former Associate Director of MIT's Computer Science and Artificial Intelligence Laboratory (CSAIL). He received a B.S. in computer science and mathematics from Yale University in 1975 and a Ph.D. in computer science from Carnegie Mellon University in 1981. He currently serves as the MIT Faculty Director of the USAF-MIT AI Accelerator and leads its Fast AI project. His award-winning research on algorithms, parallel computing, and software performance engineering has been widely deployed in industry. He held the position of Director of System Architecture for the MIT spin-off Akamai Technologies, and he founded Cilk Arts, Inc., a multicore-software start-up acquired by Intel. He coauthored the influential textbook *Introduction to Algorithms*, which has sold over one million copies. Leiserson is a Fellow of four professional societies—ACM, AAAS, SIAM, and IEEE—and he is a member of the National Academy of Engineering.

The authors were the network architects of the Connection Machine Model CM-5 Supercomputer manufactured by Thinking Machines Corporation.

Bradley C. Kuszmaul

Charles E. Leiserson

CONTEXT

Abstract for talk given for the SPAA 2023 Test-of-Time Award.

REFERENCES

[1] Robert D. Blumofe and Charles E. Leiserson. 1999. Scheduling Multithreaded Computations by Work Stealing. *J. ACM* 46, 5 (Sept. 1999), 720–748.

[2] Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest, and Clifford Stein. 2022. *Introduction to Algorithms* (fourth ed.). The MIT Press.

[3] David Culler, Richard Karp, David Patterson, Abhijit Sahay, Klaus Erik Schauser, Eunice Santos, Ramesh Subramonian, and Thorsten von Eicken. 1993. LogP: Towards a Realistic Model of Parallel Computation. In *Fourth ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming* (San Diego, California) *(PPOPP '93)*. ACM, New York, NY, 1–12.

[4] W. Hillis and G. Steele. 1986. Data Parallel Algorithms. *Commun. ACM* 29, 12 (Dec. 1986), 1170–1183.

[5] Charles E. Leiserson. 1985. Fat-trees: universal networks for hardware-efficient supercomputing. *IEEE Trans. Comput.* C-34, 10 (October 1985), 892–901.

[6] Charles E. Leiserson, Zahi S. Abuhamdeh, David C. Douglas, Carl R. Feynman, Mahesh N. Ganmukhi, Jeffrey V. Hill, W. Daniel Hillis, Bradley C. Kuszmaul, Margaret A. St. Pierre, David S. Wells, Monica C. Wong, Shaw-Wen Yang, and Robert Zak. 1992. The Network Architecture of the Connection Machine CM-5. In *Fourth Annual ACM Symposium on Parallel Algorithms and Architectures*. Association for Computing Machinery, San Diego, California, 272–285. A later version was published in *Journal of Parallel and Distributed Computing*, 33, 2 (1996), 145–158.

[7] Charles E. Leiserson, Neil C. Thompson, Joel S. Emer, Bradley C. Kuszmaul, Butler W. Lampson, Daniel Sanchez, and Tao B. Schardl. 2020. There's plenty of room at the Top: What will drive computer performance after Moore's law? *Science* 368, 6495 (2020).

[8] Gordon E. Moore. 1965. Cramming more components onto integrated circuits. *Electronics* 38, 8 (1965).

[9] Gordon E. Moore. 1975. Progress in digital integrated electronics. In *International Electron Devices Meeting Technical Digest*. IEEE, 11–13.

[10] TOP500.org. 2023. TOP500 List: Top 10 Sites for June 1993. Available at https://www.top500.org/lists/top500/1993/06/.