A DIGITAL PHASE-LOCKED ULTRASTABLE WIDEBAND FM OSCILLATOR

by

IVAN RAYMOND BURNS

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Signature of Author _____ Signature redacted _____
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Certified by _____ Signature redacted _____
Thesis Supervisor (Academic)

Certified by _____ Signature redacted _____
Thesis Supervisor (VIA Cooperating Company)

Accepted by _____ Signature redacted _____
Chairman, Departmental Committee on Graduate Students

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Submitted to the Department of Electrical Engineering on July 10, 1970 in partial fulfillment of the requirements for the Degrees of Bachelor of Science and Master of Science.

ABSTRACT

A digital phase-locked automatic frequency control (AFC) loop has been successfully used to achieve extreme temperature stability in a wideband 68 MHz voltage-controlled oscillator (VCO). The initial open loop wide deviation and high frequency modulation capabilities of the VCO have been retained. The stabilization technique used is unique in that it overcomes the deviation limitations of conventional techniques by greatly reducing the modulation index of the FM signal at the input of the phase detector.

Two similar versions of the modulator and AFC loop have been designed and breadboarded. The carrier stability of both is precisely locked to a crystal reference frequency over a temperature range of -32°C to more than 85°C. Measured results have shown that the 3 db baseband response ranges from 11 Hz to 11 MHz, and the feasibility of extending the upper response limit to 30 MHz has been indicated. When translated to S-Band (2.1 GHz) the modulator is capable of ±9 MHz deviation with 1 percent linearity and ±13.5 MHz deviation with 2 percent linearity. The modulator sensitivity at S-Band is 6.4 MHz/volt. Techniques of achieving DC baseband response and a technique for automatic quick pull-in are also described.

THESIS SUPERVISOR: James K. Roberge
TITLE: Assistant Professor of Electrical Engineering

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I. Summary

A digital phase-locked automatic frequency control (AFC) loop has been successfully used to achieve extreme temperature stability in a wideband 68 MHz voltage-controlled oscillator (VCO). The initial open-loop wideband deviation and high frequency modulation capabilities of the VCO have been retained. Two similar versions of the modulator and AFC loop have been designed and breadboarded. The carrier stability of both is precisely locked to a crystal reference over a temperature range of -32°C to more than 85°C. Measured results have shown that the 3dB baseband response ranges from approximately 11 Hz to 11 MHz, and the modulation sensitivity is 213 kHz per volt rms. Techniques of extending the baseband response to dc are described in this report. A modulation linearity of ±1 percent is maintained for deviations up to 300 kHz. For deviations up to approximately 450 kHz, the linearity is ±2 percent. These deviation and sensitivity results are given for an output carrier frequency of 68 MHz.

The importance of these results is more obvious when expressed in terms of the resulting deviations and linearity obtainable at S-Band frequencies.

For a given degree of linearity or amount of distortion the peak deviation capabilities of a modulator is directly proportional to its center or carrier frequency. The above results indicate that if the modulator output is directly multiplied to S-Band, deviations of ±9 MHz are obtainable with 1 percent linearity, and 2 percent linearity can be achieved for deviations up to ±13.5 MHz. The initial crystal stability and baseband response are not changed.

The technique described in this report can easily be extended to achieve a baseband response of better than 30 MHz. The carrier stability will still be equivalent to that obtainable with a temperature compensated fixed crystal oscillator, and the 1 percent deviation capability will remain at ±9 MHz at S-Band.

II. Introduction

The impending 1970 change-over of RF telemetry links from VHF to UHF and S-Band requires a significant improvement over the present state-of-the-art in solid-state transmitters. Future space applications require that UHF and S-Band transmitters be very small and lightweight, and capable of very high dc to RF efficiency. Advanced missions and increased data transmission requirements call for greater technical sophistication. Design requirements for such transmitter systems include wideband frequency response and wide carrier deviation capabilities so that the transmitter can handle real-time video signals for use with television, radar, and infra-red transmission systems. Good linearity and low intermodulation distortion are essential requirements in all multiplexed applications. Sensitive receivers require a very high carrier stability.

In view of such requirements, the Astro-Electronics Division of RCA is conducting an investigation of communication link microcircuit modules. The critical circuits in this project include a wideband frequency modulator, integrated circuit multipliers, and high-power solid-state amplifiers. The final circuits will be converted to high-dielectric and microelectronic form.

As an integral part of this effort, this report discusses the design and development of the wideband FM modulator. The specifications for the modulator, after multiplication into S-Band, are as follows:

Operating Frequency	S-Band (2100 MHz)
Deviation Rate	100 Hz to 20 MHz
Temperature Stability	±0.002% (-10° to +40°C)
Linearity @ Deviation	±1% @ ±4.5 MHz
	±4% @ ±20 MHz

A frequency modulated oscillator (FMO) which meets these specifications will likely be the most sophisticated yet designed. With conventional techniques, the requirements of extreme stability and wide deviation are seemingly contradictory. The digital phase-locked AFC loop detailed in this report has been successfully used to achieve both state-of-the-art requirements simultaneously.

A qualitative comparative analysis of conventional modulation and stabilization schemes versus the digital phase-locked loop technique immediately follows this section. After the reader has compared the various schemes and has a basic understanding of the physical operation of the digital phase-locked AFC loop the advantages and capabilities of the latter technique should be evident.

This report contains a thorough mathematical description of the modified version of the phase-locked loop used, followed by a description of the design of the VCO. Distortion and preliminary temperature compensation are discussed. The digital divider and phase detector design is considered next, and the loop filter, varactor bias scheme, and crystal oscillator, which complete the feedback loop, are also described. Two different techniques of obtaining dc response from the modulator

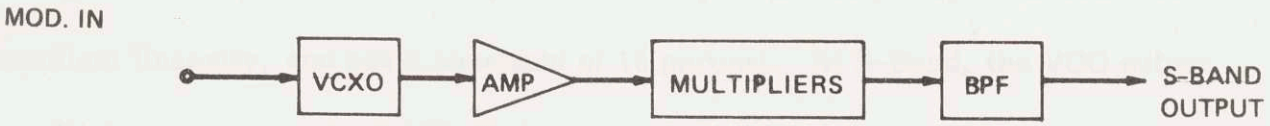
and AFC loop are disclosed. In an effort to avoid an unnecesssarily lengthy report, the author must assume that the reader has a moderate technical understanding of RF techniques, phase-locked loop analysis, and digital systems design.

III. Comparison of Design Approaches

This section discusses the advantages, disadvantages, and limitations of various typical S-Band transmitter design approaches. There are several minor variations of the schemes presented here, but the basic capabilities do not change significantly.

A. The VCXO

The simplest and least expensive approach to the design of an S-Band transmitter uses only a voltage-controlled crystal oscillator followed by an amplifier-multiplier chain. This basic scheme is shown in Figure III-1.



ADVANTAGES	DISADVANTAGES
1. SIMPLEST DESIGN.	1. MODULATION BANDWIDTH LIMITED TO 0.1%.
2. CRYSTAL STABILITY.	2. DEVIATION LIMITED TO 0.1%.
3. ALLOWS DC MODULATION.	3. POOR SPECTRAL PURITY.

Figure III-1. VCXO Transmitter

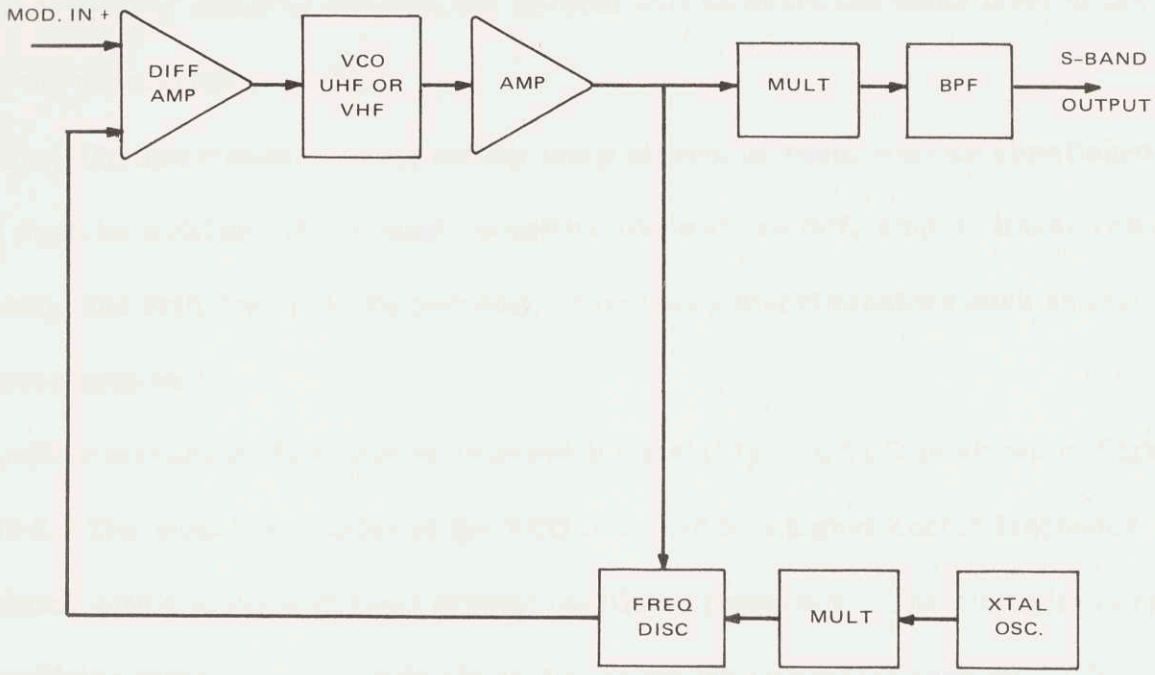
This approach, in addition to being simple and inexpensive, offers crystal controlled frequency stability. However, this system has serious modulation limitations. The modulation bandwidth is limited to approximately 0.1 percent of the VCXO frequency, and the peak deviation is limited to 0.1 percent of the S-Band output frequency. In addition, VCXO's generally have poor spectral purity characteristics, and the modulation response can be non-linear. The VCXO scheme fails to meet the IR&D baseband and deviation response specifications by more than two orders of magnitude, and thus is not worth further consideration.

B. The VCO and Conventional Techniques

The Voltage Controlled Oscillator provides a simple and efficient means of obtaining a relatively wide baseband and wide deviation capability. A well designed voltage controlled oscillator is capable of ±1.5 percent frequency deviation with excellent linearity, and has a baseband of 15 percent. At S-Band, the VCO output sensitivity can approach 15 MHz/Volt.

It is this inherent sensitivity that discourages the use of an unmodified VCO. Since a wideband VCO is necessarily a low-Q device, its long and short term frequency stability is relatively poor. It is extremely difficult to repeatedly compensate a wideband VCO to a frequency stability much better than 1 part in 10^3. This is an unacceptable stability figure for most applications.

Two techniques are generally proposed to improve the stability of a VCO. One such AFC loop is shown in Figure III-2. This approach allows dc modulation, and the RF circuitry is relatively simple. However, the discriminator and the differential



ADVANTAGES

1. ALLOWS DC MODULATION. (WITH SIMPLE MODIFICATION)
2. GOOD SPECTRAL PURITY.

DISADVANTAGES

1. DISCRIMINATOR STABILITY CRITICAL.
2. AMPLIFIER OFFSET CRITICAL.
3. LINEARITY DETERMINED BY DISCRIMINATOR.
4. DEVIATION LIMITED BY DISCRIMINATOR BANDWIDTH.

Figure III-2. Transmitter with Frequency Discriminator AFC Loop

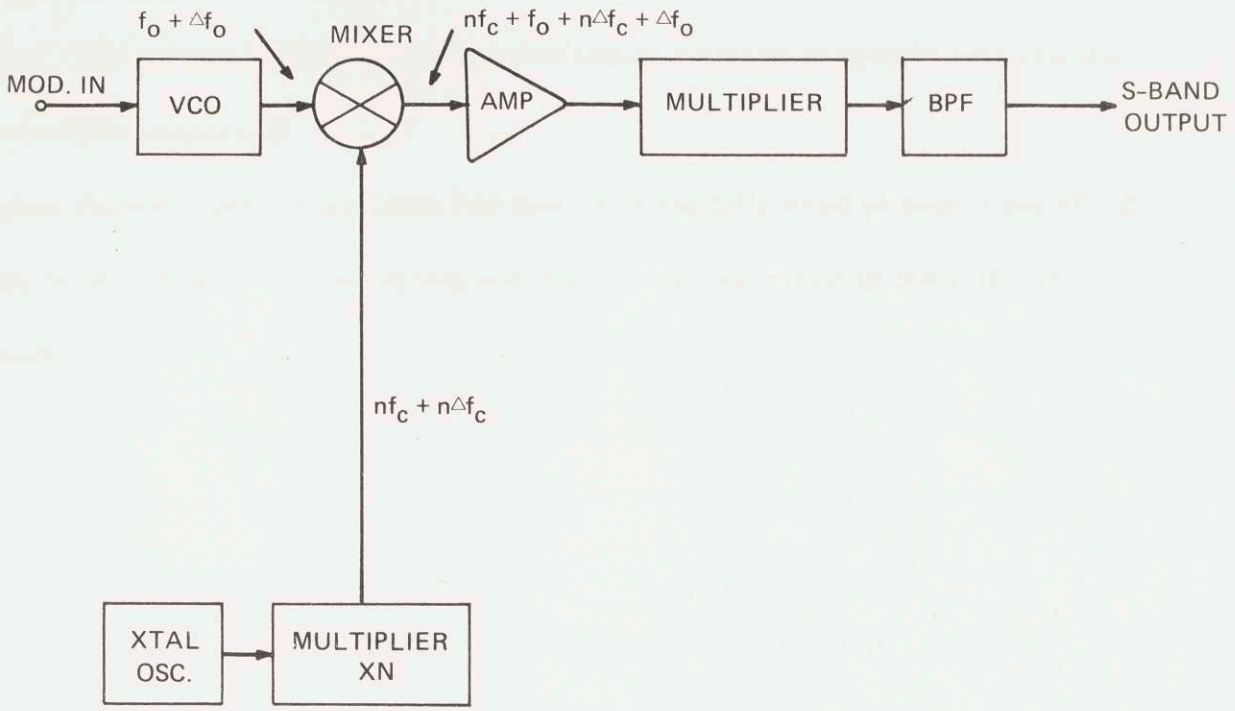
amplifier are very critical parts of this design. Drifts of the discriminator center frequency or the differential amplifier offset voltage have first order effects on the overall frequency stability. Also, the modulation linearity is critically determined by the discriminator linearity. In addition, the discriminator must be at least as

wideband as the VCO if the circuit is to operate properly. The discriminator must also be very sensitive because if it isn't, the correction signal produced to maintain the frequency stability within 0.001 percent will be below the noise level of the input of the differential amplifier.

Thus, the discriminator must satisfy many strenuous requirements simultaneously: it must be wideband (40 percent, sensitive (depends on diff. amp.), linear (±2 percent), and drift free (<0.001 percent). Frequency discriminators such as this have never been built.

Another technique often used to improve the stability of a VCO is shown in Figure III-3. The modulated output of the VCO is mixed to a higher center frequency by mixing with a multiplied fixed crystal oscillator frequency. The multiplied crystal oscillator frequency is usually about five or ten times greater than the VCO frequency.

It is this high ratio of multiplied crystal frequency to VCO frequency that gives an improved frequency stability. By letting f_o and Δf_o represent the absolute center frequency and drift component respectively of the VCO and letting f_c and Δf_c represent the same for the crystal oscillator, one can see that the multiplier-mixer combination gives an overall stability of $\frac{n\Delta f_c + \Delta f_o}{nf_c + f_o} \approx \frac{\Delta f_c}{f_c} + \frac{\Delta f_o}{nf_c}$ for $nf_c > f_o$. In an approximate sense, the modulator stability is thus improved by a factor of $\frac{nf_c}{f_o}$. However, the relative deviation of the VCO is also reduced by this same ratio, and that is a major drawback of this technique. The wide deviation capability of the VCO



ADVANTAGES

1. IMPROVES STABILITY OF VCO.
2. GOOD MODULATION LINEARITY.
3. ALLOWS DC MODULATION.
4. WIDE MODULATION BANDWIDTH.

DISADVANTAGES

1. DEVIATION CAPABILITY OF VCO IS REDUCED.
2. POOR SPECTRAL PURITY.

Figure III-3. Transmitter Using Mixer Technique

is destroyed for the sake of stability. This technique cannot be used if wide deviation is a major design objective.

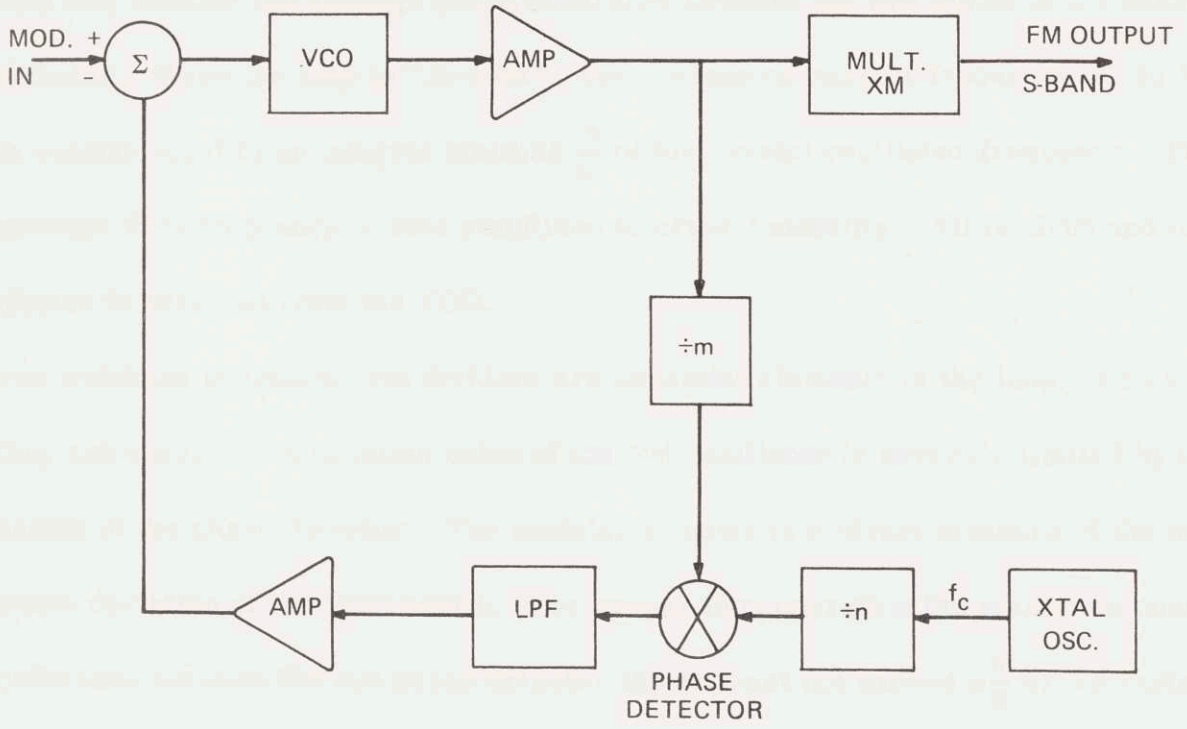
In conclusion, none of the three standard transmitter techniques are satisfactory. They cannot meet the stringent IR&D requirements of wide baseband and deviation, high stability, and good linearity. A single VCXO does not allow sufficient peak

deviation or base modulation bandwidth. The use of a frequency discriminator is not possible because the requirements placed on the discriminator itself are overly severe. The mixing technique is not satisfactory because it greatly reduces the VCO deviation capability.

A digital phase-locked loop circuit has been successfully used to overcome all of the above difficulties. Its operation and design are described in the following sections.

IV. The Digital Phase-Locked Loop

The basic digital phase-locked scheme is shown in Figure IV-1. The loop consists of two high frequency digital counters (dividers), a crystal reference oscillator, a phase detector, a low-pass filter, and a loop amplifier. For certain applications, one or both of the dividers and/or the loop amplifier can be omitted.



ADVANTAGES

1. CRYSTAL STABILITY.
2. WIDE DEVIATION.
3. WIDE MODULATION BANDWIDTH.
4. GOOD MODULATION LINEARITY.
5. GOOD SPECTRAL PURITY.

DISADVANTAGES

1. DOES NOT ALLOW DC MODULATION.
2. COMPLEX DESIGN.

Figure IV-1. Simplified Block Diagram of Digital AFC Loop for an Ultrastable Wideband FMO

A simplified explanation of the phase-locked loop operation is as follows. The phase detector compares the phase of the modulated VCO signal divided by m with the phase of a fixed crystal oscillator divided by n. The phase detector output is a measure of the phase difference between these two signals. This difference voltage is then filtered by the loop filter and is applied as a correction voltage to the VCO. The control voltage on the VCO corrects the average frequency of VCO in a direction that reduces the average phase difference between the two inputs of the phase detector. When the loop is "in-lock", the average or carrier frequency of the VCO is exactly equal to an integral multiple $\frac{m}{n}$ of the crystal oscillator frequency. The average VCO frequency is thus stabilized to crystal stability. All dc drift and modulation is removed from the VCO.

For wideband operation, the dividers are essential elements of the loop. Unless they are used, the modulation index of the FM oscillator is severely limited by the nature of the phase detector. The modulation index is a direct measure of the peak phase deviation of the VCO output. For proper loop operation the maximum phase difference between the two phase detector inputs must not exceed $\pm\frac{\pi}{2}$ or $\pm\pi$ radians, depending on the type of phase detector circuit used. A digital phase detector provides an unambiguous range of $\pm\pi$ radians. The frequency division scheme shown in Figure IV-1 circumvents this basic limitation, since the modulation index is reduced by a factor of m, as is the oscillator center frequency.

The scheme as shown in Figure IV-1 does not allow dc modulation of the VCO. The modulation index is inversively proportional to the modulation frequency, and is

thus infinite for dc modulation. Trying to reduce the modulation index by further division is futile.

The advantages of the resulting circuit are numerous. The excellent modulation characteristics of the VCO, which includes its linearity, wide baseband, and wide deviation, are maintained. The carrier frequency has crystal stability. In addition, the digital loop components require no tuning, and they are not temperature sensitive. Also a digital loop is much more easily adaptable than its equivalent analog version to a lower frequency VCO. A detailed analysis of the operation and properties of the digital phase-locked loop is now given in the following section.

V. Loop Analysis

A. Frequency Modulation

An understanding of the mathematics of frequency modulation is a necessary preclude to understanding the operation of a phase-locked FM loop. The basic equations of frequency modulation are presented here. For a more complete background, the reader is referred to Black[1]. A fairly complete bibliography of all aspects of phase-lock techniques can be found in Gardner[2].

Frequency modulation cannot be discussed until the concept of instantaneous frequency is defined. In the general expression for a constant amplitude modulated waveform $M(t) = A \cos \theta(t)$ the instantaneous frequency of M(t) is defined as the derivative of the phase angle $\theta(t)$, that is,

$$\omega_i = 2\pi f_i = \frac{d}{dt}\theta(t) \tag{1}$$

where ω_i is the instantaneous angular frequency in $\frac{\text{radians}}{\text{sec}}$.

Frequency modulation is by definition that type of modulation in which the instantaneous frequency of M(t) is equal to the constant frequency of the carrier plus a time-varying component that is proportional to the time dependent magnitude of the modulating waveform. That is, if V(t) is the modulating wave and β is the constant of proportionality then the instantaneous radian frequency ω_i is given by

$$\omega_i(t) = \omega_c + \beta V(t) = \frac{d}{dt}\theta(t) \tag{2}$$

For the case of a sinusoidal modulating wave

$$V(t) = -A_m \sin \omega_m t \tag{3}$$

it is easily shown that

$$M(t) = A \cos \left(\omega_i t + \frac{\Delta\omega}{\omega_m} \cos \omega_m t \right) \tag{4}$$
$$= A \cos \theta(t)$$

where

$$\Delta\omega = K_o A_m; \tag{5}$$

A_m = input amplitude (volts)

K_o = VCO gain (radians/volt)

The term $\frac{\Delta\omega}{\omega_m}$ is an important parameter in the discussion of FM, and is usually called the modulation index or β. As equation (4) shows, the modulation index represents the peak phase deviation of the modulated wave M(t).

It is sometimes very useful to express waveform M(t) as a sum of cosines of a constant frequency. The reader is referred to H.S. Black[1] for a derivation of the result that

$$M(t) = A \sum_{n=\infty}^{\infty} J_n(\beta) \cos \left((\omega_i + n\omega_m) t + \frac{n\pi}{2} \right) \tag{6}$$

Thus the frequency spectrum of the frequency modulated wave M(t) includes sidebands around the carrier which extend indefinitely. In reality, however, the magnitude of the higher - order Bessel functions eventually diminish, and it is a well known result that the actual bandwidth of an FM spectrum is approximately twice the sum of the modulation rate and the peak frequency deviation that is,

$$BW_{FM} \approx 2(2\pi\omega_m + 2\pi\Delta\omega) = 2(f_m + \Delta f) \tag{7}$$

B. Loop Transfer Functions

A block diagram of the basic phase-locked FM loop is shown in Figure V-1. The phase-locked loop consists of a phase detector, a low-pass loop filter, a voltage-controlled oscillator, a summing network to combine the modulation and feedback control, a crystal oscillator that provides the reference frequency and phase, and two divider chains. The VCO is a frequency modulator which produces an output frequency with an instantaneous component that is proportional to the amplitude of its input voltage. The size of the divide-by-m network is a function of the bandwidth requirements of the transmitter, the modulation index, and the nature of the

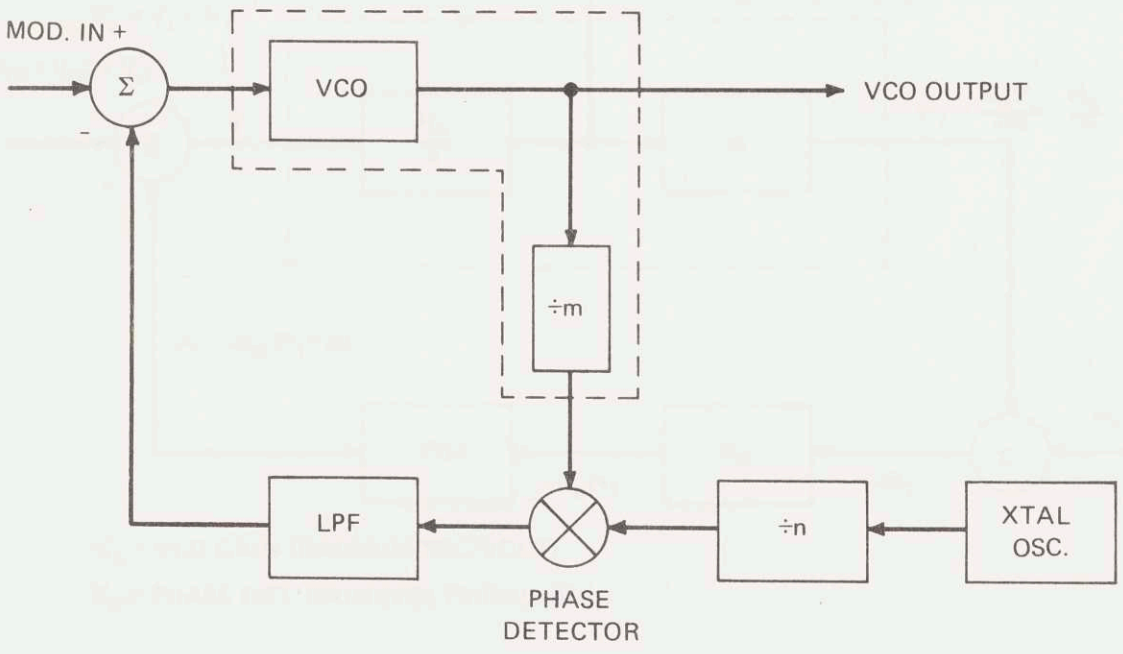


Figure V-1. Basic Block Diagram of the Phase-Locked FM Loop

phase detector. This will be explained fully later in this section. The crystal oscillator frequency f_c and the division ratio n are then chosen such that $\frac{m}{n} f_c$ is equal to the desired transmitter frequency. The division ratio m is usually but not necessarily greater than n.

The linearized equivalent block diagram of the phase-locked FM loop (Figure V-1) is shown in Figure V-2. It is a valid representation of the system when the loop is locked i.e., when θ_1 is within the unambiguous range of the phase detector, $|\theta_1| \leq \pi$. The phase detector produces a voltage output which is proportional to the phase difference between its two inputs and thus it can be replaced by a summing network

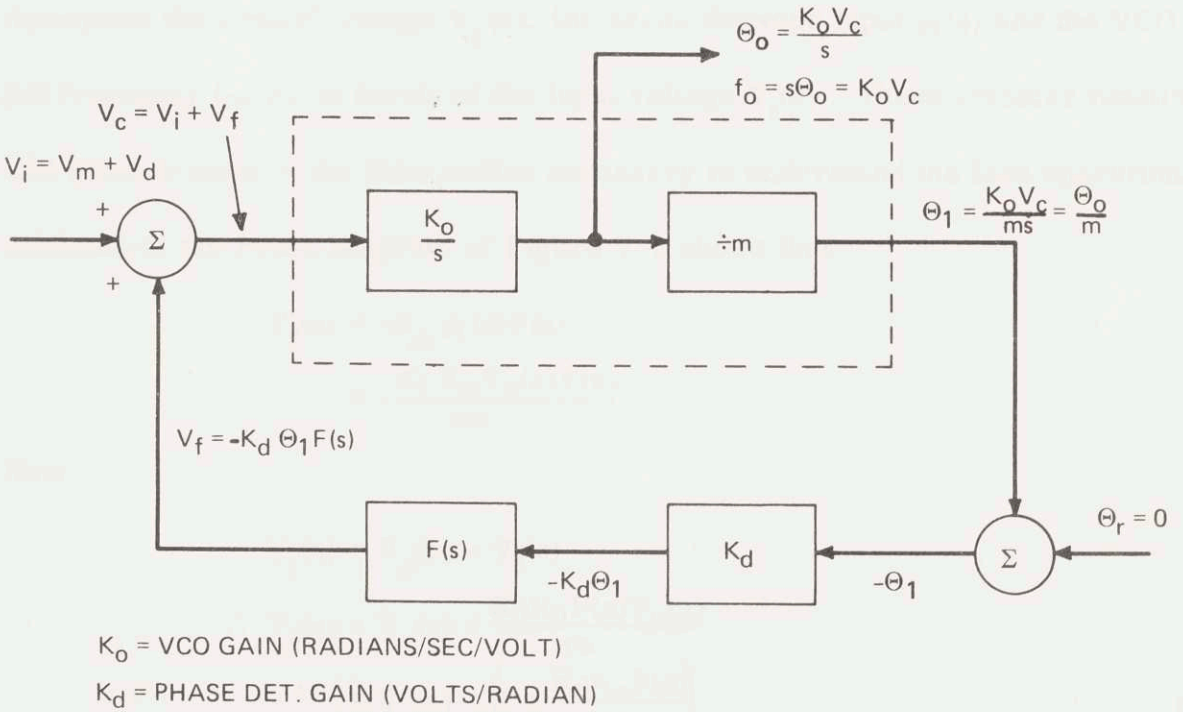


Figure V-2. Linearized Equivalent Block Diagram of Figure V-1

followed by a proportionality amplifier. The output phase of a VCO is proportional to the integral of its input voltage and thus its transfer function is represented as $\frac{K_o}{s}$. For convenience, the reference phase θ_1 is set to zero. The low-pass loop filter can be active or passive. It's transfer function is denoted as F(s).

The input voltage V_i is represented as a sum of the modulation voltage V_m and an equivalent drift on instability voltage V_d. The drift voltage is the equivalent voltage that would be required to simulate the open loop VCO drift caused by such physical factors as temperature variation or component aging. As such, V_d is a dc or very low frequency voltage.

The loop can now be analyzed by standard control systems techniques. We can now determine the control voltage $V_c(s)$, the phase detector input $\theta_1(s)$ and the VCO output frequency f_o, all in terms of the input voltage $V_i(s)$. These transfer functions will provide most of the information necessary to understand the loop operation.

Analysis of the Block Diagram of Figure V-2 shows that

$$\begin{aligned} V_f(s) &= -K_d\, \theta_1(s) F(s) \\ &= -\frac{K_d\, K_o V_c(s) F(s)}{ms} \end{aligned} \tag{8}$$

Now

$$V_i(s) = V_c(s) - V_f(s) \tag{9}$$

$$\begin{aligned} \therefore\ V_i(s) &= V_c(s) + \frac{K_d K_o F(s) V_c(s)}{ms} \\ &= V_c(s) \left(1 + \frac{K_d K_o F(s)}{ms}\right) \end{aligned} \tag{10}$$

Which reduces to

$$\frac{V_c(s)}{V_i(s)} = \frac{s}{s + \frac{K_o K_d}{m} F(s)} \tag{11}$$

Now we proceed to find the transfer function

$$\frac{\theta_1(s)}{V_i(s)}$$

$$\theta_1(s) = \frac{K_o V_i(s)}{ms} = \frac{K_o}{ms} \left(V_i + V_f \right)$$

$$= \frac{K_o}{ms} \left(V_i(s) - K_d \, \theta_1(s) F(s) \right) \tag{12}$$

which reduces to

$$\frac{\theta_1(s)}{V_i(s)} = \frac{K_o}{m \left(s + \frac{K_o K_d}{m} F(s) \right)} \tag{13}$$

The time varying component of the VCO output frequency, f_o, is the derivative of the output phase. Thus

$$\frac{f_o(s)}{V_i(s)} = \frac{s\theta_0(s)}{V_i(s)} = \frac{sm\theta_1(s)}{V_i(s)} \tag{14}$$

therefore

$$\frac{f_o(s)}{V_i(s)} = \frac{s \, K_o}{s + \frac{K_o K_d}{m} F(s)} \tag{15}$$

These results cannot be carried further until F(s) is specified. Both the active and passive version of the most widely used type of loop filter are shown in Figure 7.

Use of these filters yields a second-order system which is amenable to analysis and is always stable. The transfer function F(s) for the filters of Figure V-3 is of the form

$$F(s) = K_f \frac{(\tau_2 s+1)}{(\tau_1 s+1)} \tag{16}$$

Where K_f is the dc gain of the filter and τ_1 and τ_2 are the filter time constants and $\tau_1 > \tau_2$ always. A Bode Plot of the filter transfer function F(s) given by eq. 16 is shown in Figure V-4.

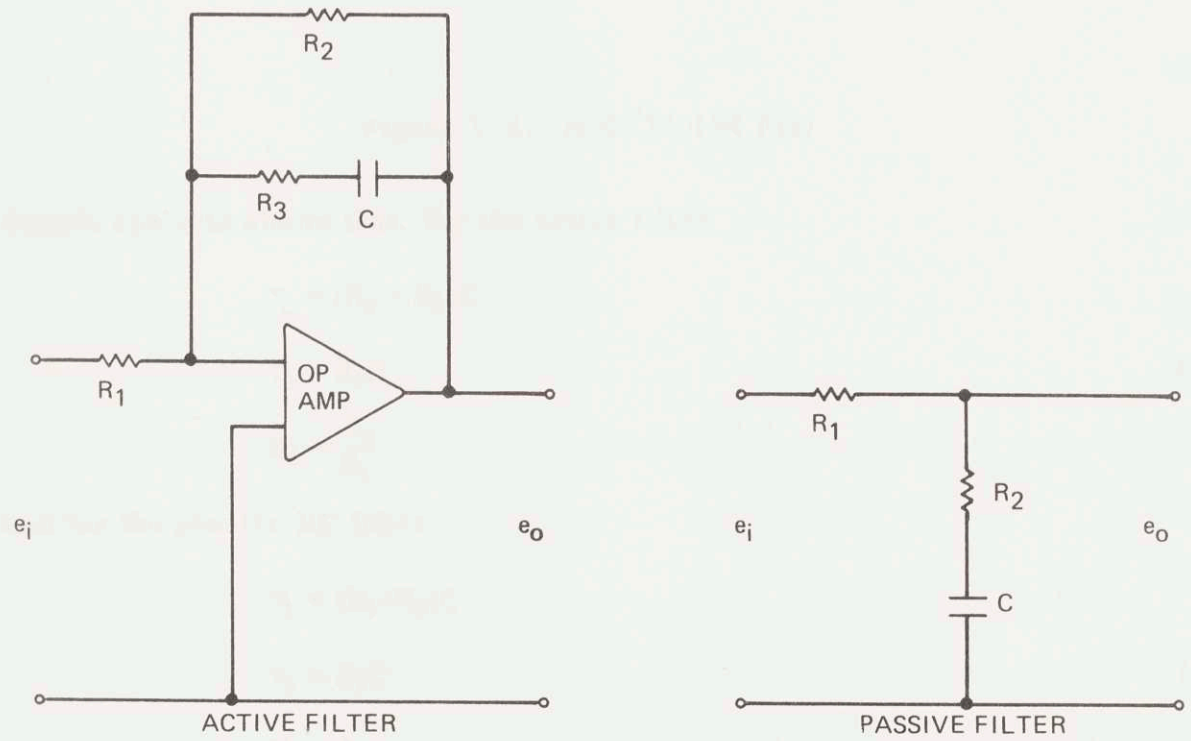


Figure V-3. Active and Passive Loop Filters

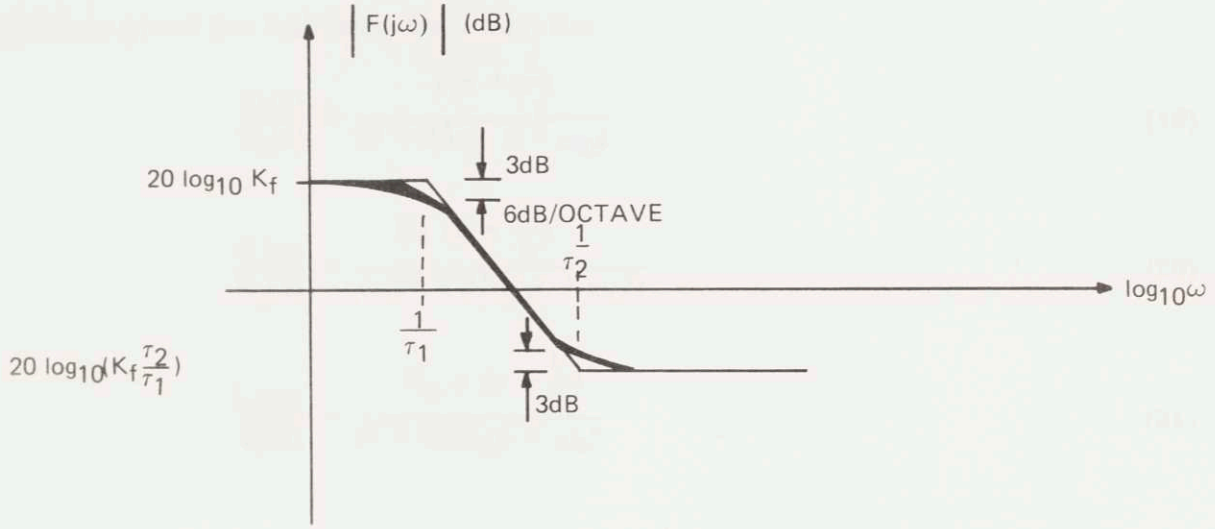


Figure V-4. Bode Plot of F(s)

Simple analysis shows that, for the active filter

$$\tau_1 = (R_2 + R_3)C$$

$$\tau_2 = R_3C \qquad (17)$$

$$K_f = \frac{R_2}{R_1}$$

and for the passive RC filter,

$$\tau_1 = (R_1+R_2)C$$

$$\tau_2 = R_2C \qquad (18)$$

$$K_f = 1$$

Substituting the general form of F(s) (eq. 16) into Equations 11, 13, and 15, and rearranging the terms to get expressions analogous to standard control systems equations gives the following final results:

$$\frac{V_i(s)}{V_i(s)} = \frac{s(s + \frac{1}{\tau_1})}{s^2 + 2\delta\omega_n s + \omega_n^2} \tag{19}$$

$$\frac{\theta_1(s)}{V_i(s)} = \frac{K_o (s + \frac{1}{\tau_1})}{m(s^2 + 2\delta\omega_n s + \omega_n^2)} \tag{20}$$

$$\frac{f_o(s)}{V_i(s)} = \frac{K_o s (s + \frac{1}{\tau_1})}{s^2 + 2\delta\omega_n s + \omega_n^2} \tag{21}$$

where

$$\omega_n = \left(\frac{K_o K_d K_f}{m\tau_1}\right)^{1/2} \tag{22}$$

and

$$\delta = \frac{\omega_n}{2}\left(\frac{1}{K} + \tau_2\right) \tag{23}$$

$$K = \frac{K_o K_d K_f}{m} \tag{24}$$

In this standard notation, ω_n is the closed-loop natural frequency, δ is the damping ratio, and K is the open loop dc gain.

C. Tracking Behavior

The tracking behavior or frequency modulation characteristics of the loop during locked operation can be easily examined with the help of Bode plots of Equations 19 through 21. Normally δ is optimized for $\delta = 0.707$. In the following Bode Plots, for convenience $\delta = 1$. This does not change the results significantly.

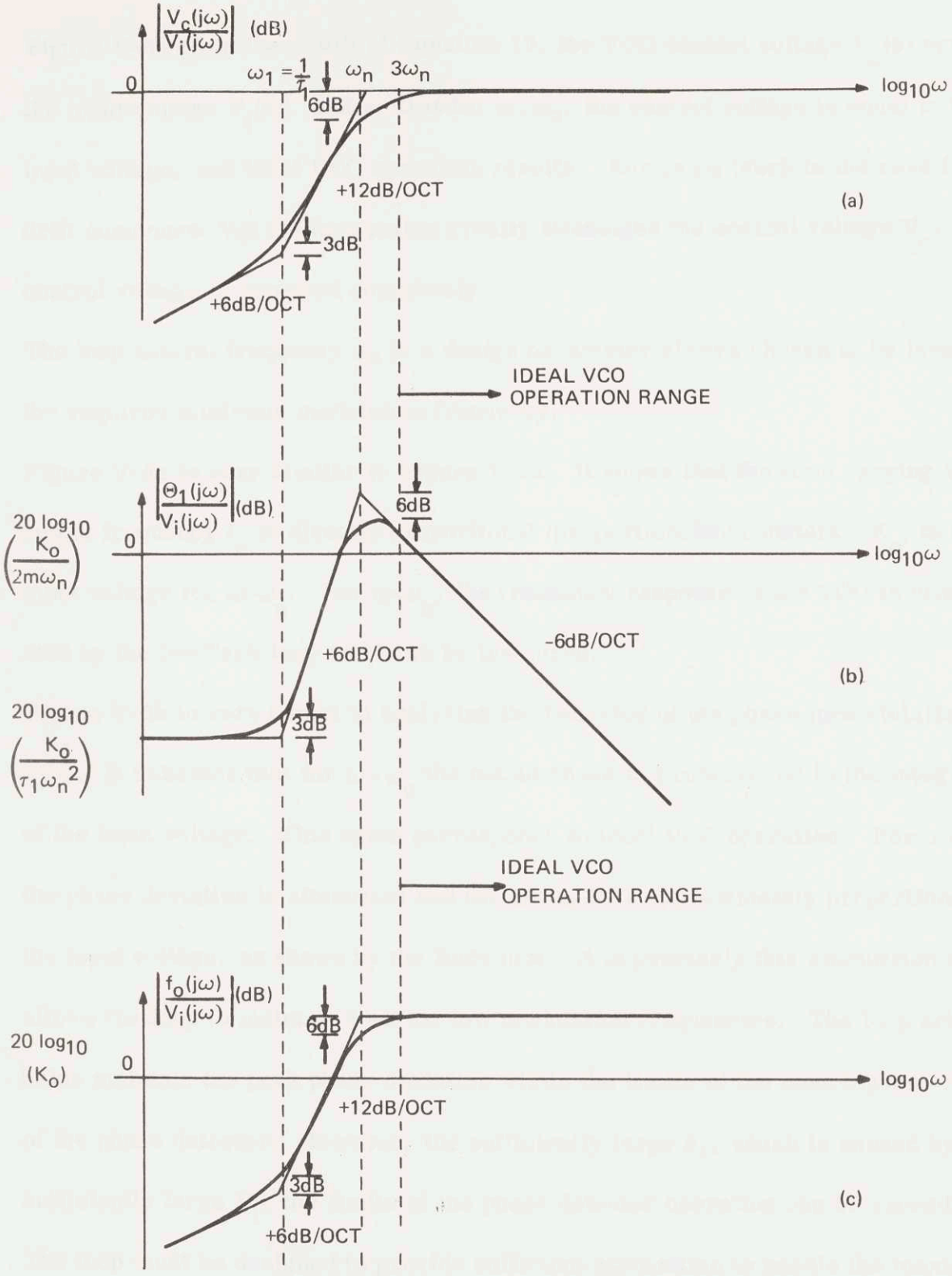


Figure V-5. Bode Plots of the Transfer Equations of a Phase-Locked FM Loop

Figure V-5a plots the result of Equation 19, the VCO control voltage $V_c(s)$ versus the input voltage $V_i(s)$. Notice that for $\omega > \omega_n$, the control voltage is equal to the input voltage, and ideal VCO operation results. For $\omega < \omega_n$ (such is the case for the drift component V_d) the loop action greatly attenuates the control voltage V_c. Dc control voltage is removed completely.

The loop natural frequency ω_n is a design parameter always chosen to be less than the required minimum modulation frequency.

Figure V-5c is very similar to Figure V-5a. It shows that the time varying VCO output frequency f_o is directly proportional (proportionality constant = K_o) to the input voltage for $\omega > \omega_n$. For $\omega < \omega_n$, the frequency response of the VCO is attenuated by the feedback loop as shown by the curve.

Figure V-5b is very useful in analyzing the behavior of the phase lock stabilized VCO. It indicates that for $\omega > \omega_n$ the output phase is proportional to the integral of the input voltage. This again corresponds to ideal VCO operation. For $\omega < \omega_n$ the phase deviation is attenuated and for $\omega < \omega_1$ it is approximately proportional to the input voltage, as shown by the Bode plot. It is precisely this attenuation that allows the loop to maintain lock for low modulation frequencies. The loop action helps maintain the peak phase deviation within the limits of the unambiguous range of the phase detector. However, for sufficiently large θ_1, which is caused by sufficiently large V_i, the limits of the phase detector operation can be exceeded. The loop must be designed to provide sufficient attenuation to handle the maximum

expected input voltage $V_{i(max)}$. The loop will then maintain lock under worst-case conditions. Loop limitations will be discussed further in a following section.

D. Hold-In and Acquisition With a Sawtooth Phase Comparator

The above discussion of tracking behavior or modulation responses assumes that the loop is "in lock". This section defines what is meant by "in lock". An expression describing the limits of locked operation is given. Acquisition of lock is also discussed.

Several typical phase detector characteristics are shown in Figure V-6. The characteristics shown are sinusoidal, triangular, and sawtooth, in that order. A phase-controlled loop is said to be "in lock" if the phase difference $\Delta\theta$ between its two inputs θ_1 and θ_2 is maintained within the unambiguous range of the phase detector. For the sinusoidal phase detector this requires that

$$\left|\Delta\theta \text{ max}\right| \leq \frac{\pi}{2} \tag{25}$$

and for a typical triangular or sawtooth phase comparator

$$\left|\Delta\theta \text{ max}\right| \leq \pi \tag{26}$$

Referring to the expression for a frequency modulated waveform, Equation 4, it becomes clear that the peak phase deviation at the output of the VCO is given by the modulation index $\frac{\Delta\omega}{\omega_m}$. This phase deviation is divided by m before it reaches the input of the loop phase detector. Expressed in terms of the modulation index and the division ratio Equation 26 thus becomes

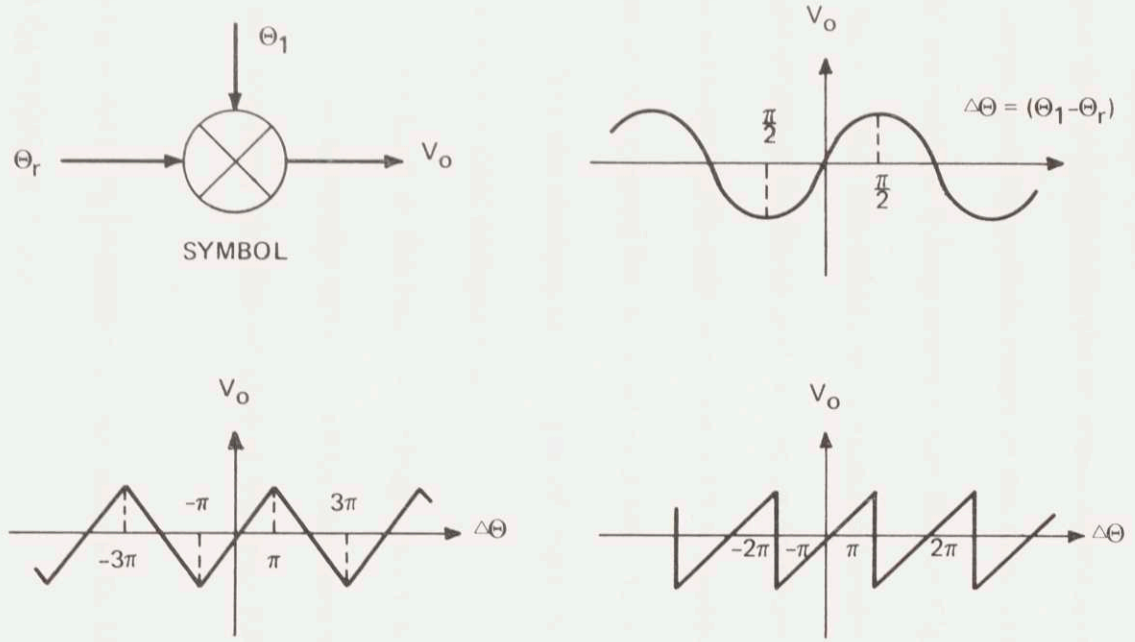


Figure V-6. Common Phase Detector Characteristics

$$\left|\frac{\Delta\omega_{(max)}}{m\omega_{m(min)}}\right| \leq \pi \qquad (27)$$

for $\omega_{m(min)} > \omega_n$

Many authors [2-5] have derived approximate or exact expression for the hold-in range, the lock-in range, and the pull-in range of the standard phase-locked loop. Even though they did not analyze a loop exactly like that of Figure V-1, their results are still applicable here. The non-linear mathematics involved is most effectively solved by using phase-plane techniques and an analog computer[3-5].

The expressions given below apply only to a loop with a sawtooth phase comparator A sawtooth comparator was chosen for several reasons. It is easily realizable in a digital system. It also has the obvious advantages of improved linearity and a wider hold-in range over the sinusoidal comparator.

The first topic of consideration is the input dc voltage range over which the loop will maintain lock. This is naturally determined by the maximum output voltage capability of the phase detector, and the dc gain of the loop filter. It should be obvious that

$$\Delta V_H = \max\left|V_i\right| = (\text{Filter Gain})\ (\text{max P.D. Output})$$

$$\therefore\ \Delta V_H = K_f K_d\, \pi \qquad (28)$$

for the sawtooth phase comparator. This can be converted to an equivalent hold-in frequency $\Delta\omega_H$ which is given by the hold-in voltage times the VCO gain:

$$\Delta\omega_H = K_o \Delta V_H = K_o K_d K_f\, \pi \qquad (29)$$

This is equivalent to the lock-in frequency as defined by Goldstein[4] and Protonotarios[5].

$$\Delta\omega_L = K_o K_d K_f \pi \tag{30}$$

Suppose that the loop of the phase-lock system were initially open. Then the pull-in frequency $\Delta\omega_p$ is defined as the maximum frequency difference from which the loop will eventually lock in (after the loop is closed) after slipping through one or more cycles. Goldstein derived the pull-in frequency $\Delta\omega_p$ in terms of γ_p, which is the ratio of the pull-in frequency to the lock-in frequency.

$$\gamma_p = \frac{\Delta\omega_p}{\Delta\omega_L} \tag{31}$$

For the case of a simple RC filter ($R_2 = 0$ in the passive filter of Figure V-3) Goldstein and Protonotarios agree that

$$\gamma_p = \begin{cases} \tanh \frac{\pi}{4} \left(K_o R_1 C - \frac{1}{4}\right)^{\frac{1}{2}} & \text{for } K_o R_1 C \geq \frac{1}{4} \\ 1 & \text{for } K_o R_1 C \leq \frac{1}{4} \end{cases} \tag{32}$$

For the more general filter ($R_2 \neq 0$) a transcendental equation results which must be solved by numerical approximation methods. Goldstein plotted the contours of constant γ_p on the $\tau_1 - \tau_2$ plane and his results are reproduced in Figure V-7.

As yet, nobody has derived an accurate expression for the time required for the loop to pull into lock from some initial offset for a sawtooth comparator. Viterbi's[6] approximate expression for a loop with a sinusoidal comparator is

$$T_p \approx \frac{(\Delta\omega)^2}{2\delta\omega_n^3} \tag{33}$$

where $\Delta\omega$ is the initial offset frequency. This expression is not accurate if $\Delta\omega$ is either very large or very small.

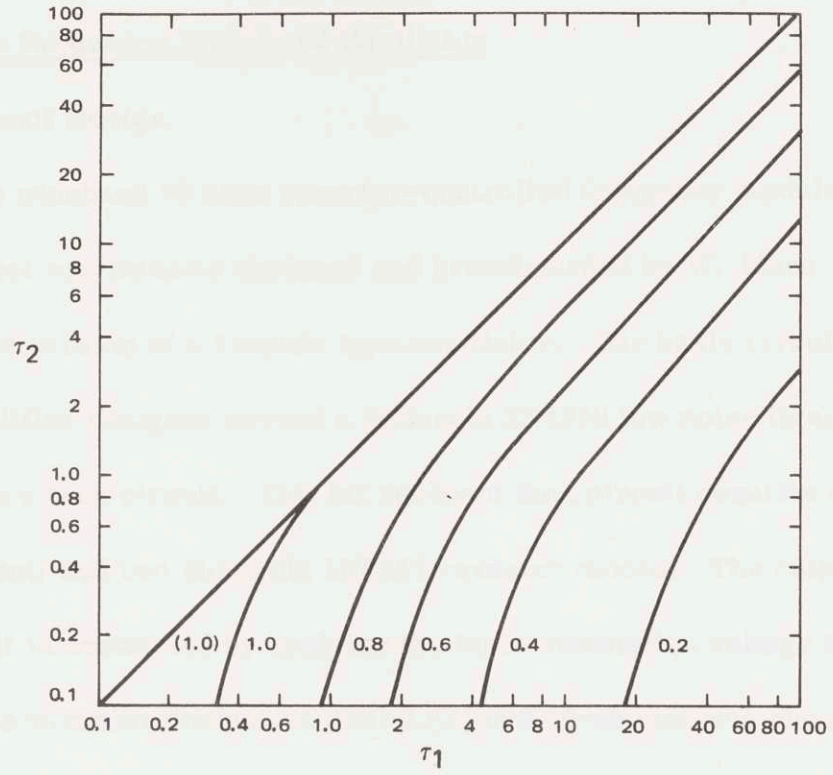


Figure V-7. Contours of Constant γ_p as a Function of τ_1 and τ_2

VI. CIRCUIT DESIGN AND CONSIDERATIONS

A. The Frequency Modulated Oscillator

1. Circuit Design

The wideband 70 MHz varactor-controlled frequency modulated oscillator for this project was initially designed and breadboarded by W. Maco. The oscillator is a modified version of a Colpitts type oscillator. The basic circuit consists of a 70 MHz amplifier designed around a Motorola 2N4959 low noise figure RF transistor, coupled to a tank circuit. The LC resonant tank circuit consists of a very stable inductor coil and two Motorola 1N5147 varactor diodes. The output frequency of the circuit is controlled by applying the input modulation voltage to vary the bias across the varactor diodes. A JFD LF3P008 80-nh coil was chosen for its good temperature characteristics. The oscillator circuit is followed by a common base amplifier stage to provide isolation and signal gain.

The Linvill Analysis design of the 70 MHz common base amplifier and the feedback calculations are not given here. The complete original FMO circuit diagram is given as a portion of Figure VI-13. The common base buffer amplifier has since been redesigned by S. Knight, to provide the necessary 20 dB of gain. The redesigned buffer amplifier is included in the circuit diagram of Figure VI-14. The 600K resistor across the varactors and the 5K thermistor are not a part of the original circuit. They were added as part of a temperature compensation technique to be described later.

2. Distortion and Linearity Analysis

The major cause of distortion in varactor controlled phase and frequency modulators is the nonlinearity of the varactor control elements. Harmonic and intermodulation distortion has been analyzed in phase and frequency modulated oscillators using both graded and abrupt junction varactors by W. Maco[7]. Another analysis with interesting but less useful results has been performed by Pelchat[8]. Maco's analysis and a brief description of his results will be presented here. The distortion was calculated by first selecting a particular circuit type and circuit element values, including varactor capacitance at center frequency and zero deviation. The phase or frequency transfer function of the circuit as a function of varactor capacitance was derived, and by substituting the varactor capacitance-voltage characteristic, the transfer function as a function of modulation voltage was obtained. The n^{th} order distortion was then calculated by computing the deviation at n+1 modulation voltage points and converting to a power series equation of deviation as a function of modulation voltage using Larange's Interpolation Formula[9]. The distortion as a function of deviation was then calculated from the power series coefficients. The deviation sensitivity and amplitude modulation as a function of deviation were also obtained. The above steps were carried out with the aid of a Telecomp time-shared computer.

The phase modulation circuit selected for analysis is shown in Figure VI-1. The basic modulator circuit is a symmetrical capacitive-coupled two-section bandpass

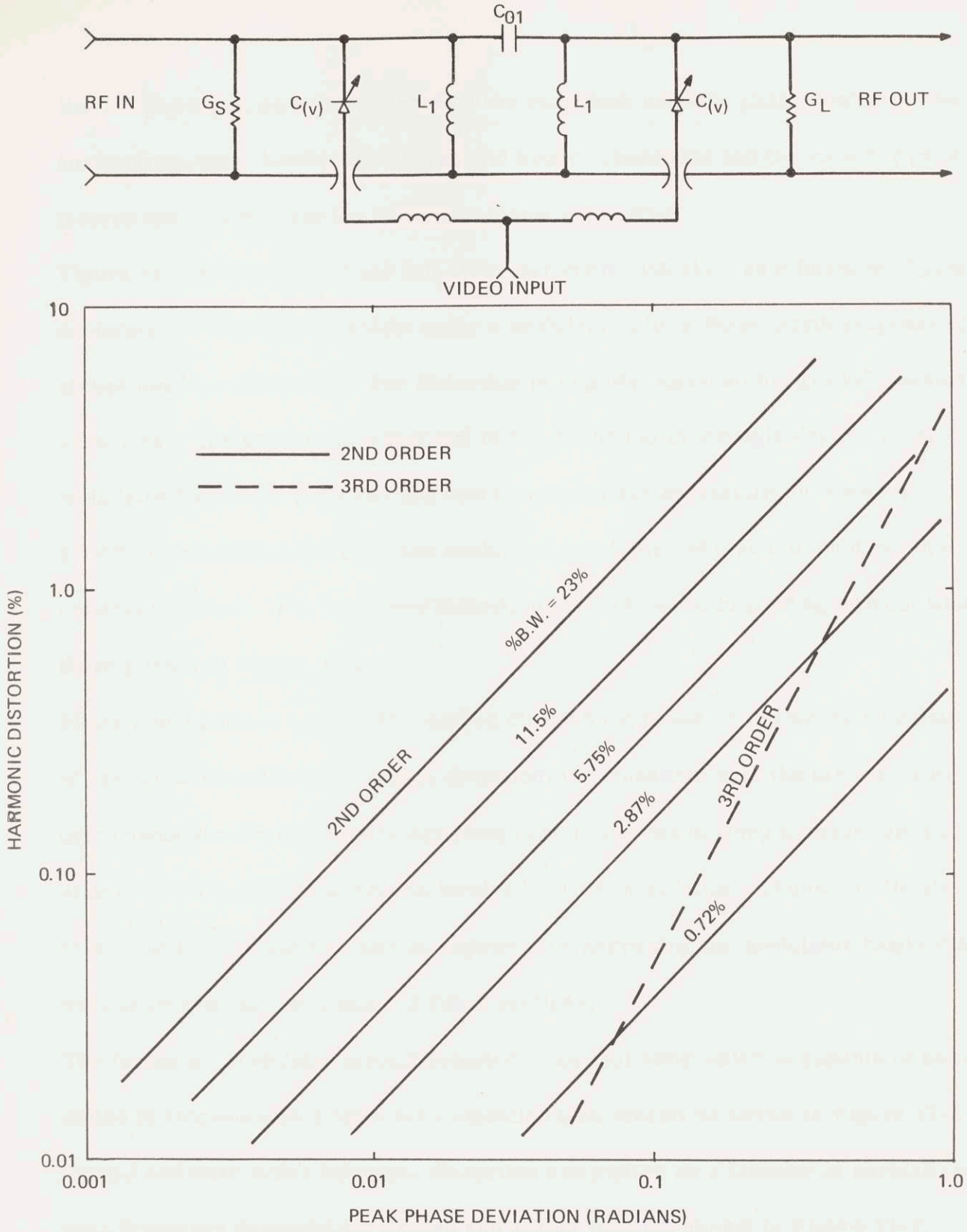


Figure VI-1. Phase Distortion in 2-Section Butterworth Phase Modulator

filter. The shunt capacitive elements are varactors used for phase control. The center frequency, bandwidth, source and load conductances and the varactor parameters are selected and the distortion terms calculated.

Figure VI-1 shows the 2nd and 3rd order harmonic distortion as a function of phase deviation for various bandwidths using a modulator with a Butterworth response and abrupt junction varactors. The distortion is slightly degraded for graded junction varactors. The curves show that 2nd order distortion in strongly dependent on modulator bandwidth while the 3rd order products are essentially independent. A 47 MHz 6 percent bandwidth phase modulator was built and tested to confirm the computed curves. The measured distortion products were in good agreement with those plotted in Figure VI-1.

Phase modulation is a desirable method of obtaining phase or frequency modulation where the modulation index (phase deviation) is compatible with the distortion requirements since a fixed frequency stable oscillator can be used to drive the modulator and no frequency pulling is involved. This modulation technique is flexible in that deviation capability can be improved by narrowing the modulator bandwidth and/or increasing the number of filter sections.

The frequency modulator circuit selected is an oscillator which is capable of being pulled in frequency by a varactor-controlled tank circuit as shown in Figure VI-2. Second and third order harmonic distortion are plotted as a function of normalized peak frequency deviation for graded and abrupt junction diodes in Figure VI-2, clearly showing the advantage of abrupt junctions.

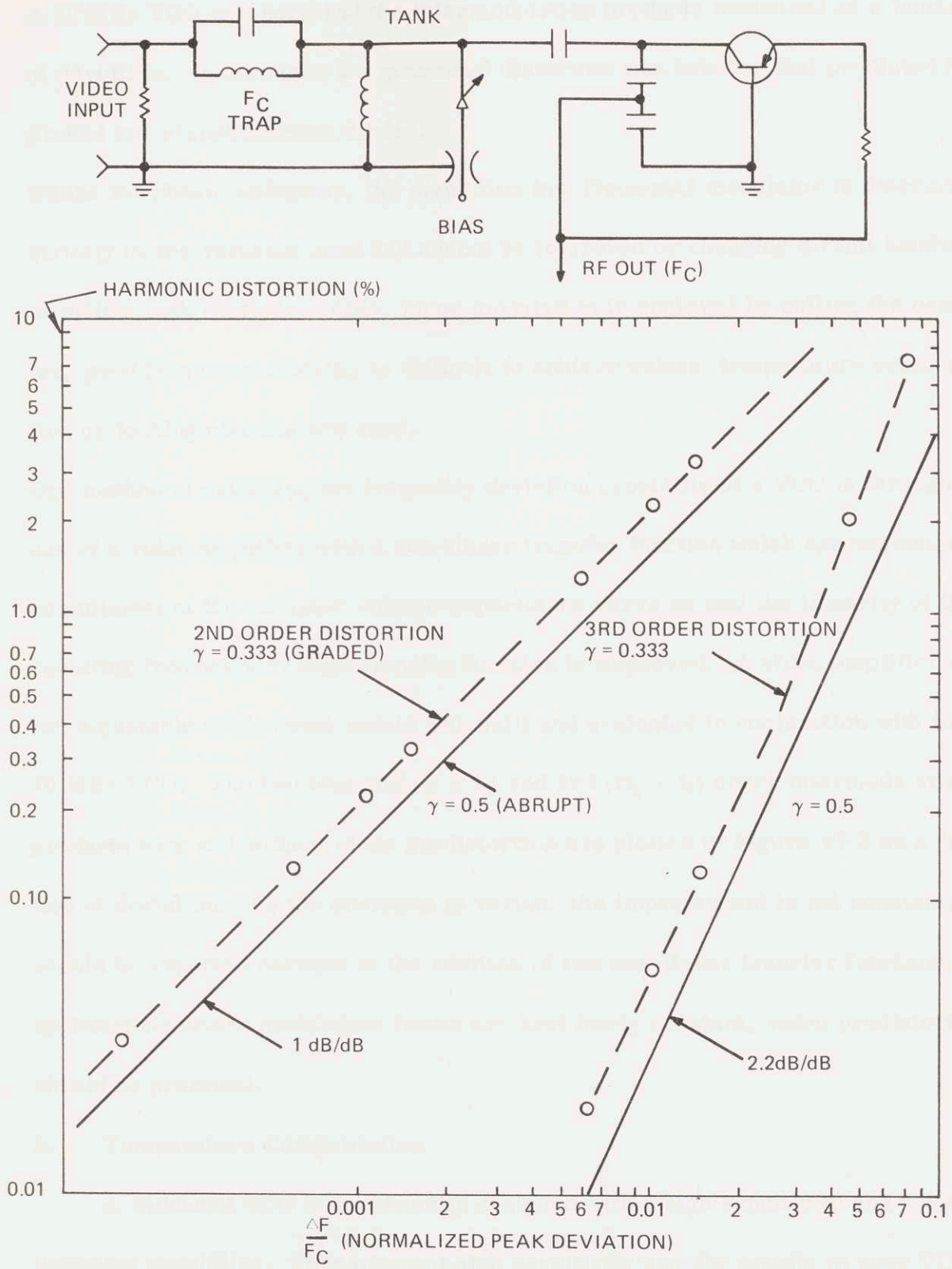


Figure VI-2. FM Distortion for Graded and Abrupt Junction Varactors

A 70 MHz VCO was built and the intermodulation products measured as a function of deviation. In all cases the measured distortion was between that predicted for graded and abrupt junction diodes.

Unlike the phase modulator, the distortion in a frequency modulator is determined strictly by the varactor used and cannot be improved by changing circuit bandwidth or adding tank sections. Also, since modulation is achieved by pulling the oscillator, good frequency stability is difficult to achieve unless temperature compensation or locking circuits are used.

One method of extending the frequency deviation capability of a VCO is through the use of a video amplifier with a non-linear transfer function which approximates the compliment of the varactor voltage-capacitance curve so that the linearity of the resulting frequency-voltage transfer function is improved. A video amplifier with two adjustable diode break points was built and evaluated in conjunction with the 70 MHz VCO. The two tone 2nd ($f_1 \pm f_2$) and 3rd ($2f_1 \pm f_2$) order intermodulation products with and without video predistortion are plotted in Figure VI-3 as a function of deviation. As the deviation is varied, the improvement is not constant, as should be expected because of the addition of two non-linear transfer functions. In applications where modulation levels are kept fairly constant, video predistortion should be practical.

3. Temperature Compensation

A wideband VCO is necessarily designed with a high sensitivity and a wide deviation capability. This inherent high sensitivity usually results in poor VCO

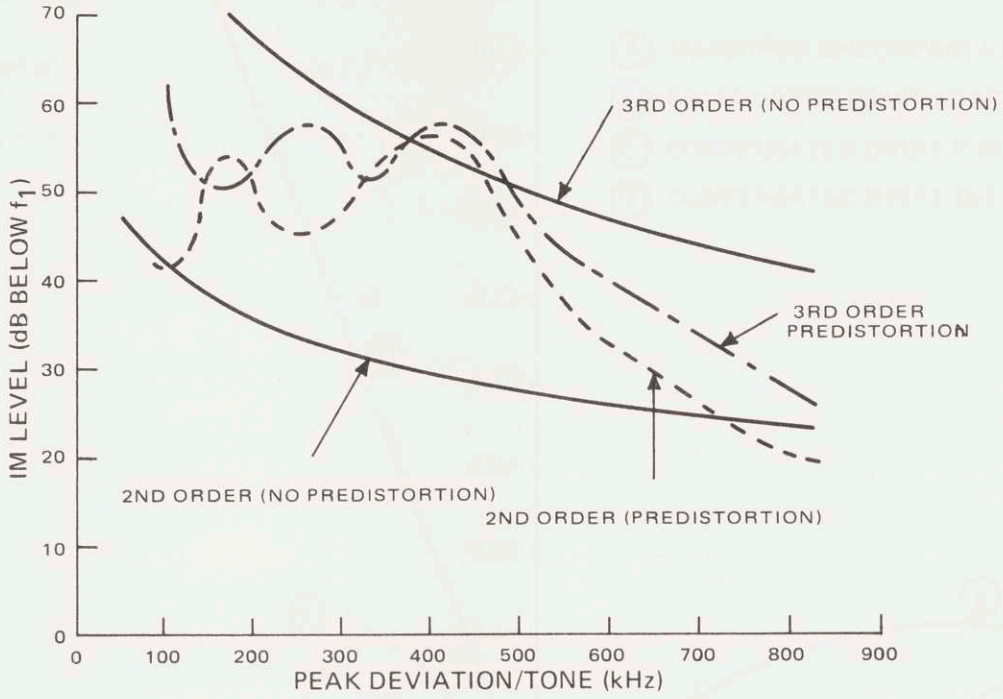


Figure VI-3. IM Improvement With Predistortion for 70-MHz VCO (Two Equal Tones)

temperature characteristics. It is extremely difficult and time consuming to repeatedly and reliably compensate a wideband VCO to an absolute stability of 0.002 percent or 0.001 percent over the flight temperature range of -20° to +40°C. Some type of AFC technique such as those mentioned in Section III or IV must ultimately be used to achieve high stability.

However, moderate or improved open loop VCO stability can be easily obtained by relatively simple temperature compensation techniques. These techniques involve the use or matching of temperature sensitive circuit components. Preliminary temperature compensation by these techniques is desirable because it reduces the stress placed on the feedback control loop.

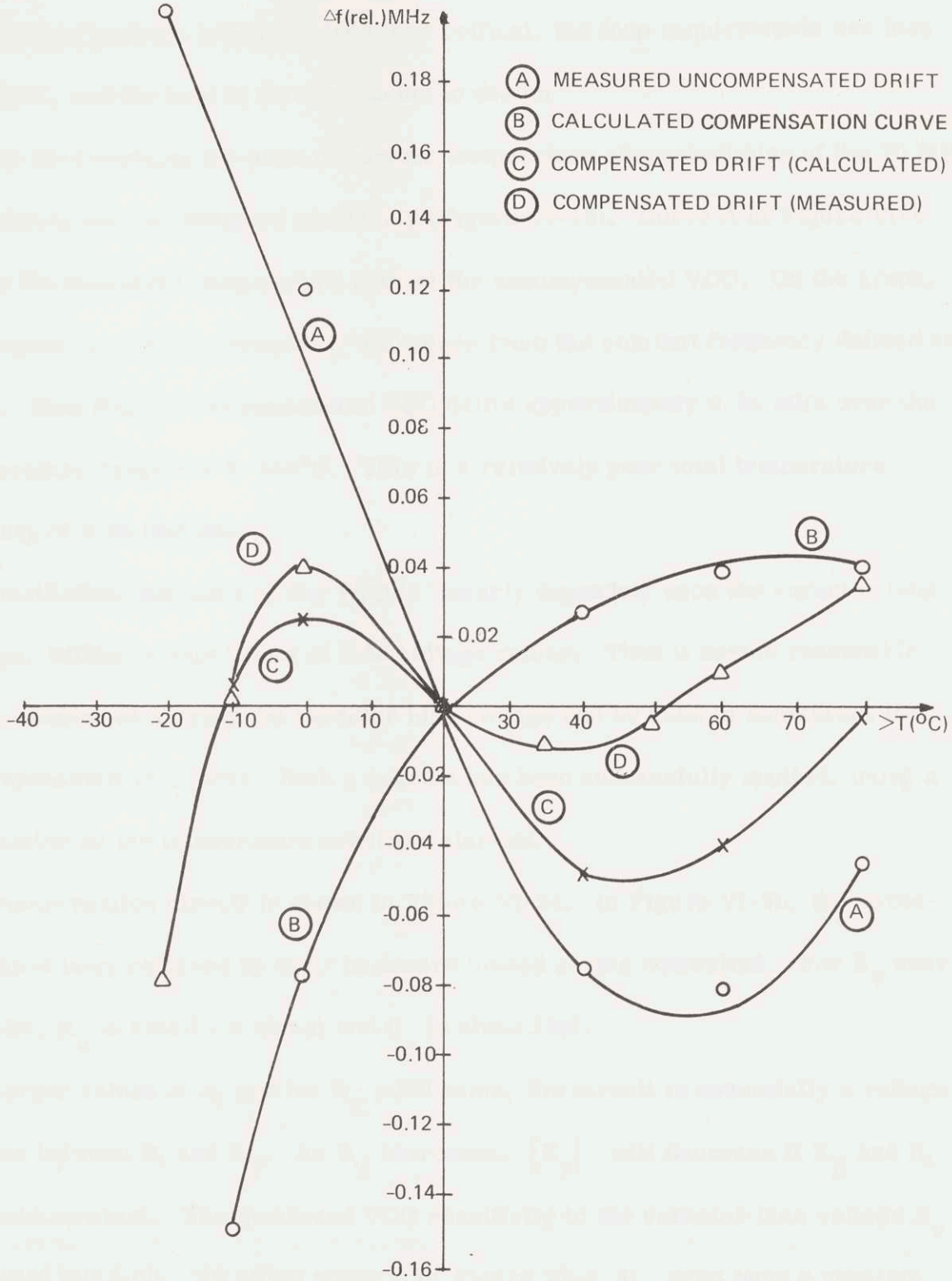


Figure VI-4. VCO Temperature Curves, Compensated and Uncompensated. $f_o = f\ (20°C) = 67.579$ MHz

Worst-case analysis becomes much less critical, the loop requirements are less stringent, and the loop is thereby easier to design.

Figure VI-4 contains the plots of various temperature characteristics of the 70 MHz VCO discussed and designed previously (Figure VI-13). Curve A of Figure VI-4 shows the measured temperature drift of the uncompensated VCO. On the graph, $\triangle f$ denotes the relative frequency difference from the nominal frequency defined at 20°C. Note that the uncompensated VCO drifts approximately 0.24 MHz over the temperature range -10 to +40°C. This is a relatively poor total temperature stability of 0.34 percent.

The oscillation frequency of the VCO is linearly dependent upon the varactor bias voltage, within certain limits of bias voltage values. Thus it seems reasonable that a scheme of varying the varactor bias voltage can be used to counteract the uncompensated VCO drift. Such a scheme has been successfully applied, using a thermistor as the temperature sensitive element.

The compensation circuit is shown in Figure VI-5a. In Figure VI-5b, the varactors have been replaced by their backward biased series equivalent. For E_v near 14 volts, R_v is small (<5 ohms) and C_v is about 20pf.

For larger values of R_1 and for R_T >300 ohms, the circuit is essentially a voltage divider between R_1 and R_T. As R_T increases, $|E_v|$ will decrease if E_B and R_1 are held constant. The measured VCO sensitivity to the varactor bias voltage E_v was +340 kHz/volt. To offset curve A of Figure VI-4, R_T must have a negative temperature coefficient. By choosing R_1 = 600K and selecting R_T with a -4.4%/°C

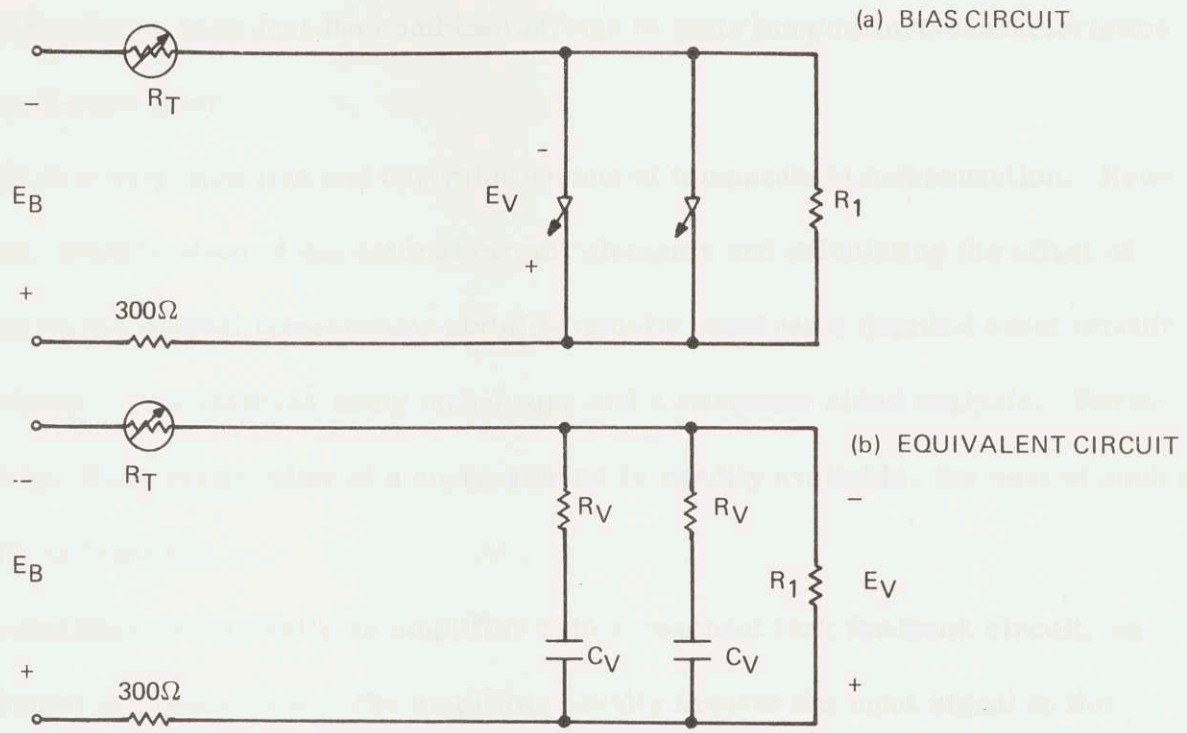


Figure VI-5. Thermistor Temperature Compensation Circuit

temperature coefficient and a nominal 5K resistance value at 25°C, the calculated compensation cure, curve B in Figure VI-4, results.

The effects of the two curves A and B add linearly, and the resulting calculated net drift is shown as Curve C. The actual measured compensated drift is plotted as Curve D. The resulting stability is now 0.07 percent or ±0.035 percent. This is a significant improvement, although a much better compensation could have been achieved with unavailable thermistors.

The VCO can also be temperature compensated by careful selection of all critical temperature sensitive circuit components. Critical components, after they are identified, can be chosen to be as stable as possible, and/or pairs of components

can be chosen such that the combined effects of their temperature characteristics cancel each other.

This is a very effective and desirable means of temperature compensation. However, identification of the critical circuit elements and calculating the effect of each on the overall temperature stability usually requires a detailed exact circuit analysis. This involves many man-hours and a computer aided analysis. Fortunately, if the cheap labor of a co-op student is readily available, the cost of such a task is feasible.

An oscillator is basically an amplifier with a resonant tank feedback circuit, as depicted in Figure VI-6. The amplifier usually inverts the input signal in the process of amplification. If the feedback loop gain is greater than unity when the tank circuit provides exactly 180° of phase shift oscillation will result.

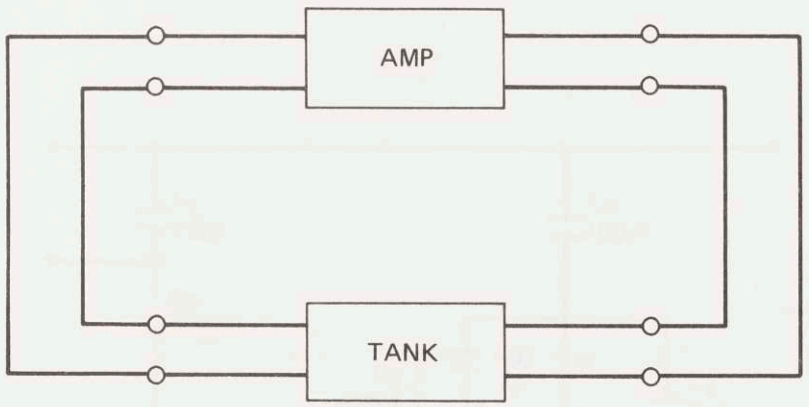


Figure VI-6. Basic Oscillator Representation

A detailed incremental analysis of the complete oscillator circuit, calculating the temperature effect of every component in the circuit, is both cost prohibitive and unnecessary. Rather, it is sufficient to isolate the most critical circuit components by using the computer to carefully find the tank circuit. The tank circuit is found by intelligent guessing and using the computer to verify the guess: if the proper tank circuit is "guessed" the computer's network analysis program will indicate that the tank has a very sharp phase slope passing through 180° at exactly the resonant frequency, and the tank's input admittance is zero at the resonant frequency.

The NATS (Network Analysis Time-Shared) program was used to analyze the circuit. The resulting tank circuit, consisting of the appropriate circuit components of Figure VI-13 is shown in Figure VI-7. The resistor R represents the equivalent series resistance of the coil at 70 MHz.

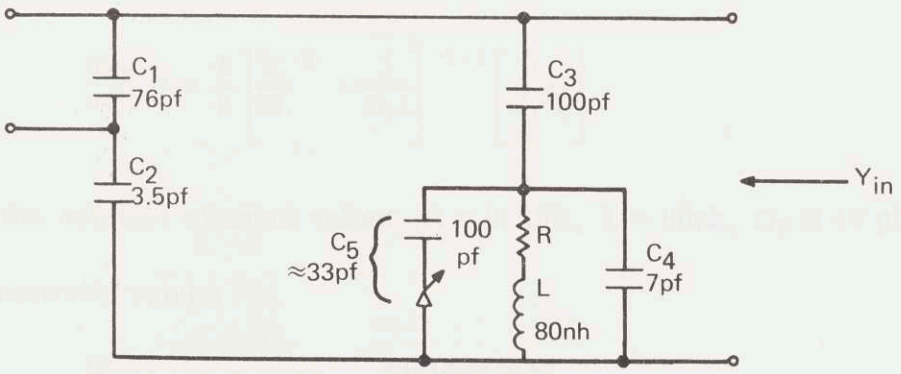


Figure VI-7. Resonant Tank Circuit of 70 MHz VCO of Figure VI-12

At resonance, $Y_{in} = 0$. Solving the circuit of Figure VI-7 for the zeros of it's admittance results in the quadratic equation

$$s^2 + \frac{R}{L} s + \frac{1}{C_7 L} = 0 \tag{34}$$

where

$$C_7 = \frac{(C_1 C_3 + C_2 C_3)(C_4 + C_5) + C_1 C_2 (C_3 + C_4 + C_5)}{C_1 C_3 + C_2 C_3 + C_1 C_2} \tag{35}$$

Solution of equation 34 for the zeros of Y_{in} gives

$$s = \tau + j\omega = -\frac{R}{22} \pm \left[\frac{R}{22}^2 - \frac{1}{C_7 L}\right]^{1/2} \tag{36}$$

The above equation directly indicates the effect of a low Q coil ($R \neq 0$). The tank resonant frequency is given by

$$\omega_r = \pm \left[\frac{R}{2L}^2 - \frac{1}{C_7 L}\right]^{1/2}$$

This result can now be used to calculate the effect of varying values of L and C_1 through C_5 and C_7. By taking the partial derivative of the resonant frequency expression (eq 37) one obtains

$$\frac{\partial \omega_r}{\partial L} = \pm \frac{1}{2} \left[\frac{R}{2L}^2 - \frac{1}{C_7 L}\right]^{-1/2} \left[\frac{-R^2}{2L^3} + \frac{1}{C_7 L^2}\right] \tag{38}$$

$$\frac{\partial \omega_r}{\partial C_7} = \pm \frac{1}{2} \left[\frac{R}{2L}^2 - \frac{1}{C_7 L}\right]^{-1/2} \left[\frac{1}{C_7^2 L}\right] \tag{39}$$

Substituting the nominal element values ($R = 0.35\Omega$, $L = 80$nh, $C_7 \cong 40$ pf) gives the following sensitivity values

$$\frac{\partial \omega_r}{\partial L} = (3.5 \times 10^6) \quad \frac{\text{radians/sec}}{\text{nh}} \tag{40}$$

$$\frac{\partial \omega_r}{\partial C_7} = (6.95 \times 10^6) \quad \frac{\text{radians/sec}}{\text{pf}} \tag{41}$$

Since C_7 analytic function of the circuit capacitors C_1 through C_5, the sensitivity of the resonant frequency to each of these capacitors can be calculated by applying the chain-rule of differentiation. That is,

$$\frac{\partial \omega_r}{\partial C_n} = \frac{\partial \omega_r}{\partial C_7} \cdot \frac{\partial C_7}{\partial C_n}$$

$$= (6.95 \times 10^6) \cdot \frac{\partial C_7}{\partial C_n} \qquad \frac{\text{rad/sec}}{\text{pf}} \tag{42}$$

$$\text{for } n = 1,\ 2,\ 3,\ 4,\ 5$$

The partial derivatives of C_7 are dimensionless constants (very nearly constants) calculated by computer to be

$$\frac{\partial C_7}{\partial C_1} = 0.0046 \qquad \frac{\partial C_7}{\partial C_4} = 1.0$$

$$\frac{\partial C_7}{\partial C_2} = 0.74 \qquad \frac{\partial C_7}{\partial C_5} = 1.0 \tag{43}$$

$$\frac{\partial C_7}{\partial C_3} = 0.037$$

Thus the final sensitivity results are:

$$\frac{\partial \omega_r}{\partial L} = 3.5 \times 10^6 \quad \frac{\text{rad/sec}}{\text{nh}}$$

$$\frac{\partial \omega_r}{\partial C_1} = 3.2 \times 10^4 \quad \frac{\text{rad/sec}}{\text{pf}}$$

$$\frac{\partial \omega_r}{\partial C_2} = 5.15 \times 10^6 \quad \frac{\text{rad/sec}}{\text{pf}} \tag{44}$$

$$\frac{\partial \omega_r}{\partial C_3} = 2.6 \times 10^5 \quad \frac{\text{rad/sec}}{\text{pf}}$$

$$\frac{\partial \omega_r}{\partial C_4} = 6.95 \times 10^6 \quad \frac{\text{rad/sec}}{\text{pf}}$$

$$\frac{\partial \omega_r}{\partial C_5} = 6.95 \times 10^6 \quad \frac{\text{rad/sec}}{\text{pf}}$$

These sensitivity constants can be applied to the manufacturer's component temperature data to calculate the temperature drift effect of each critical component.

B. Digital Design

1. High Frequency Techniques

High frequency division at toggle frequencies of 30 to 400 MHz has recently been made feasible through the use of non-saturating emitter-coupled logic (ECL) elements. Preliminary investigation of techniques led to the choice of the Motorola MECL family of ECL to accomplish the high frequency division. MECL is the only currently available commercial IC family capable of toggling at sufficiently high frequencies. Low power dissipation and minimum size are major requirements of the divider chain. The circuit must also be guaranteed to operate over the required temperature range. A high speed digital circuit generally requires considerably more power than a slower rated circuit. It is thus desirable to use high-speed circuitry only where absolutely necessary. Thus, to minimize power consumption, the divider chain has been designed as in the general scheme shown in Figure VI-8. High-frequency MECL flip-flops are used to reduce the input frequency until it is slow enough to be handled by conventional TTL. After the signal has been reduced to about 3 MHz, low-power TTL IC's can be used to complete the divider chain. The actual IC circuitry used will be detailed in the next section.

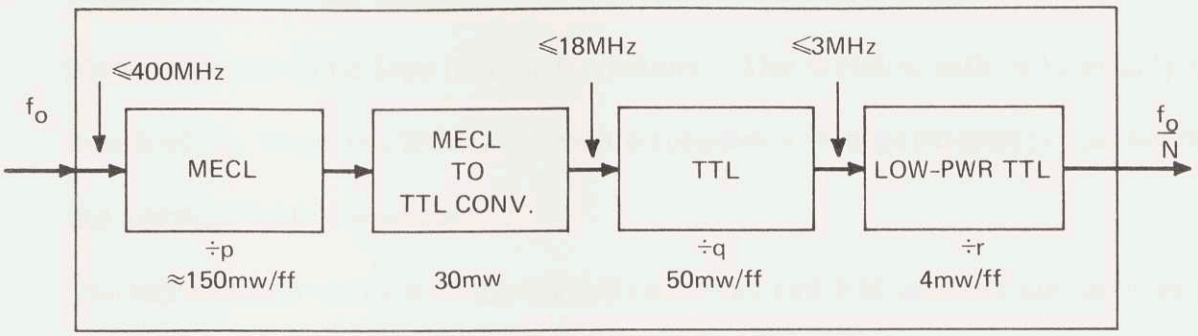


Figure VI-8. Optimum Power Configuration of High Frequency Divider

Several discrete-component high-frequency division techniques were also considered, but recent investigations performed in IR&D programs at Camden on digital frequency synthesizer techniques[10-12] have shown the use of MECL integrated circuits to be far superior. Among the techniques investigated by the engineers at CSD Camden include a tunnel diode circuit and a combination transistor and zener diode circuit. Use of these techniques has since been abandoned since MECL is much more compact, consumes less power (transistor high-speed ÷ 3 required 2.1 watts!), is much less sensitive to bias voltage and temperature drifts, and offers greater versatility.

2. Logic Design and Implementation

Three separate divider chains were designed and implemented in the course of this project. The IR&D version of the digital phase-locked FM loop required a 70 MHz divided-by-m (m = 10, 240) and a 17 MHz divide-by-n (n = 2, 560). These

two divider circuits are included in Figure VI-13. The division ratio m was calculated by requiring the maximum effective modulation index at the input to the phase detector to be less than $\pm\pi/2$ radians. The division ratio n is simply one-fourth of m, since the XTAL reference frequency is approximately one-fourth of the average VCO frequency.

The narrowband version of the digital phase-locked FM loop did not have as strenuous deviation and modulation index requirements as the IR&D specifications called for, and thus required relatively small dividers. A 70 MHz divide-by-8 and a 17 MHz divide-by-2 were designed and used for the narrowband breadboard. The 70 MHz divide-by-8 circuit used is shown in Figure VI-14.

The phase detector circuits, although they can be incorporated into the divider circuits, are not shown in the divider diagrams. The phase detectors are discussed below.

3. The $\pm\pi$ Digital Phase Detectors

There are three widely used types of phase detectors. The common output characteristics of the three phase detectors are sinusoidal, triangular, and sawtooth. The usual unambiguous range of a sinusoidal phase detector is $\pm\pi/2$ radians, but this range can readily be extended to multiples of $\pm n\pi/2$ for certain kinds of triangular and sawtooth phase detectors.

In addition to a wide unambiguous range and excellent linearity, the sawtooth phase detector will also yield improved tracking, hold-in, and pull-in characteristics when used in a phase-locked loop.

Such phase comparators are also extremely convenient to incorporate into the loop circuit if square wave inputs are already available, as they are when dividers are used. A sawtooth phase-detector can thus simply be a set-reset flip-flop followed by an integrator. For such a detector the XTAL reference signal sets the flip-flop once in each cycle, and the VCO signal resets (or changes) the flip-flop once in each cycle. The phase difference between the two signals is the average of the flip-flop output. This operation is shown in Figure VI-9.

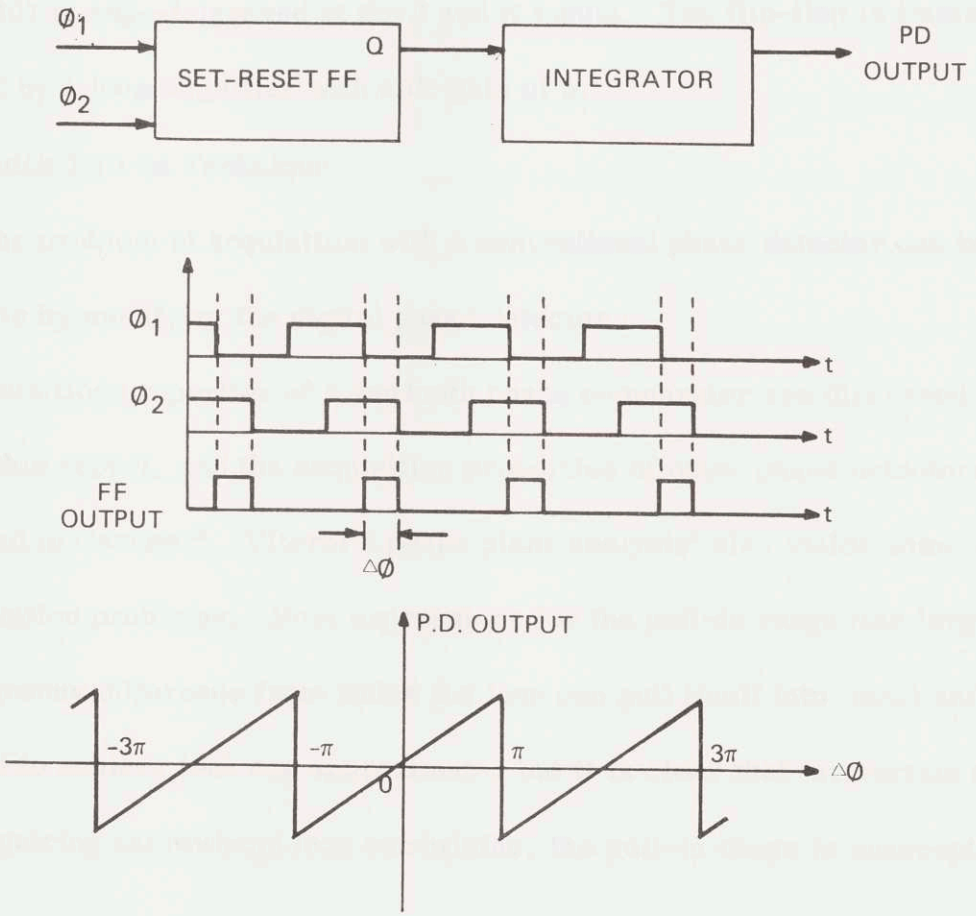


Figure VI-9. Ideal Sawtooth Phase Detector Operation

Since TTL input levels were readily available in the IR&D loop version, a TTL realization of a sawtooth phase detector shown in Figure VI-13 was used in the circuit. This phase detector was designed around available components, but other designs using other flip-flops could be much simpler. The zener diode is used to achieve a constant bias level shift. This phase detector has a unambiguous range of $\pm\pi$ radians.

The phase detector circuit used in the narrowband breadboard is shown in Figure VI-14. The inputs do not have to be sent through pulse generators, since MECL the MC307 is edge-triggered at the J and K inputs. The flip-flop is immediately followed by a loop amplifier with a dc gain of 5.

4. Quick Pull-In Technique

The problem of acquisition with a conventional phase detector can be easily overcome by modifying the digital phase detector.

The acquisition properties of a sawtooth phase comparator are discussed in Section V-D of this report, and the acquisition properties of other phase detectors are discussed in Gardner[2]. Viterbi's phase plane analysis[6] also yields some insight to acquisition problems. Most expressions for the pull-in range (the largest initial frequency difference from which the loop can pull itself into lock) and the time required to achieve lock are approximate, but it is clear that for certain applications requiring narrowband loop bandwidths, the pull-in range is unacceptably

small and the lock-in range is unacceptably long. In extreme cases where the initial frequency offset is near the limit of the pull-in range, the pull-in time required to lock can be on the order of hours.

The state diagram of a four-state digital machine which eliminates the problem of acquisition is shown in Figure VI-10, where A denotes a pulse from the VCO and B denotes a pulse from the crystal reference oscillator, both pulses being taken at the output of the divider chains. The digital phase detector discussed in the previous section is simply the averaged output of a set-reset flip-flop that is set by A and reset by B. The acquisition technique shown in Figure VI-10 operates on the basis that if A is faster than B, or vice-versa, there will initially be at least two consecutive A pulses or B pulses. A circuit designed from the stage diagram of Figure VI-10 detects an out-of-lock condition and immediately sets its output voltage to a dc value of the correct polarity, and the output can then be integrated and applied as a ramp correction voltage to pull the VCO into lock. The pull-in range of this scheme is limited only by the saturation voltage of the integrator or loop amplifier. After the VCO has been pulled into lock, the four state machine starts oscillating between its two middle states, and effectively serves as a conventional set-reset flip-flop phase detector. There are many equivalent implementations of the state diagram of Figure VI-10, and it is left to the reader to design the machine using available digital logic.

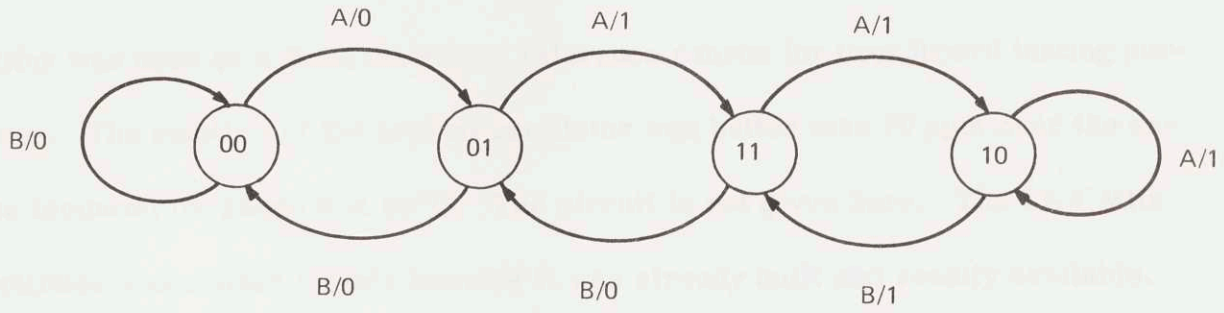


Figure VI-10. State Diagram of Quick Acquisition Scheme

C. Loop Filter and Bias Schemes

The loop filters were designed using the equations of Section V-B, and the values given in Table VI-1 to calculate τ_1 and τ_2. The resulting filters, loop amplifiers and bias networks are indicated in the circuit diagrams of Figures VI-13 and VI-14.

TABLE VI-1. PARAMETER VALUES USED IN DESIGN CALCULATIONS

Parameter	Wideband IR&D	Narrowband 70p	Units
ω_n	$2\pi\times10^2$	$2\pi\times2\times10^3$	rad/sec
K_o	$2\pi\times250\times10^3$	$2\pi\times250\times10^3$	$\frac{\text{rad/sec}}{\text{volt}}$
K_d	0.48	0.127	$\frac{\text{volts}}{\text{rad}}$
K_f	1.0	5.0	—
m	10,240	8	—

D. The Crystal Reference Oscillator

A 17.1 MHz crystal oscillator originally designed for the TIROS APT Transmitter was used as a fixed frequency reference source for breadboard testing purposes. The stability of the crystal oscillator was better than 20 ppm over the entire temperature range 0 to 60°C. The circuit is not given here. The 17.1 MHz oscillator was chosen merely because it was already built and readily available. Future modulator systems will be controlled by a crystal source custom designed to meet the specific frequency requirements of the system.

If MECL logic is used in the divider chain or loop phase detector it is convenient to use a MECL Integrated Circuit crystal controlled oscillator, using a MECL II MC1023 OR/NOR logic gate. An IC crystal oscillator offers the advantages of simplicity and small size. It also has several other advantages over conventional circuitry. When a second gate is used as a buffer for the oscillator, frequency does not change with loading. The high input impedance and 0.9 volt logic swing prevents the possibility of overdrawing the crystal. Results have shown the circuits to be frequency insensitive to ±20 percent power supply variations, and that the frequency versus temperature characteristics closely follow the crystal characteristics.

Figure VI-11 shows the basic MECL oscillator circuit for fundamental frequency crystals. This circuit has a maximum operating frequency of 20 MHz and a minimum frequency of approximately 1 MHz. Higher frequency operation at a desired crystal overtone can be achieved with the circuit of Figure VI-12. C_1 and L_1 form

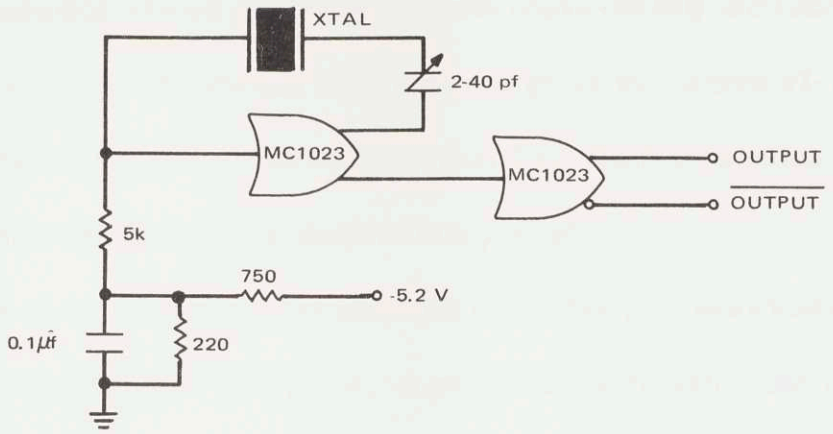


Figure VI-11. MECL Crystal Oscillator 1 MHz to 20 MHz Fundamental Frequency

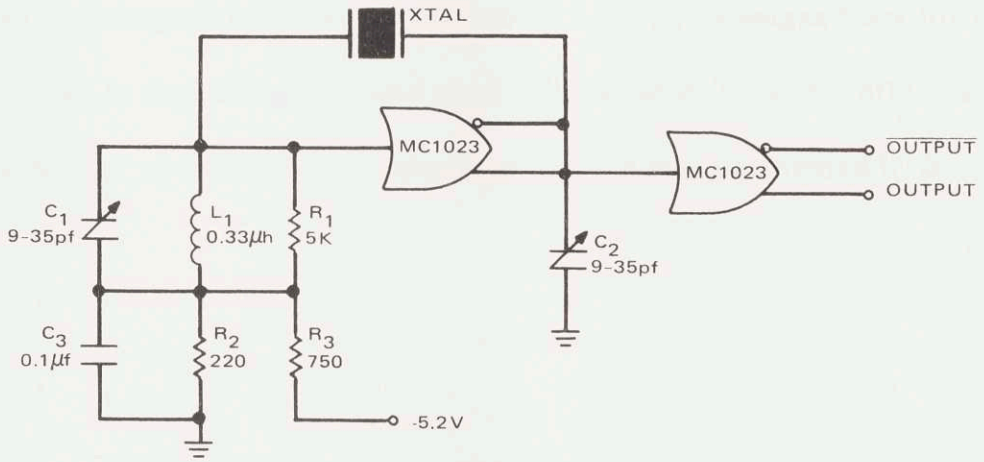


Figure VI-12. MECL Crystal Oscillator 50 MHz to 100 MHz Overtone Operation

the resonant tank circuit, which with the values specified has a resonant frequency adjustable from approximately 50 MHz to 100 MHz. Overtone operation is obtained by adjusting the tank circuit frequency at or near the desired circuit frequency. A complete description of the operation of these IC crystal controlled oscillators can be obtained from the Motorola Application Note AN-417.

E. Complete Phase-Locked Oscillator Circuit Diagrams

The complete circuit diagrams for both phase-locked oscillators are included here for reference. The circuit diagrams are given in Figures VI-13 and VI-14, and are reasonably detailed and self-explanatory. Each subsection of the circuits has been discussed in other sections of this report.

Photographs of the laboratory breadboards of the two phase-locked oscillators are included in Figures VI-15 and VI-16. A preliminary miniaturized version of the narrowband modulator circuit using miniature components mounted on thin ceramic substrates is photographed in Figure VI-17. Notice that the circuit could be much more densly packaged if desired by machining a custom-designed box for the circuit. The box shown in the photograph was used only because it was readily available. All layout design work for the miniaturized version was performed by S. Knight.

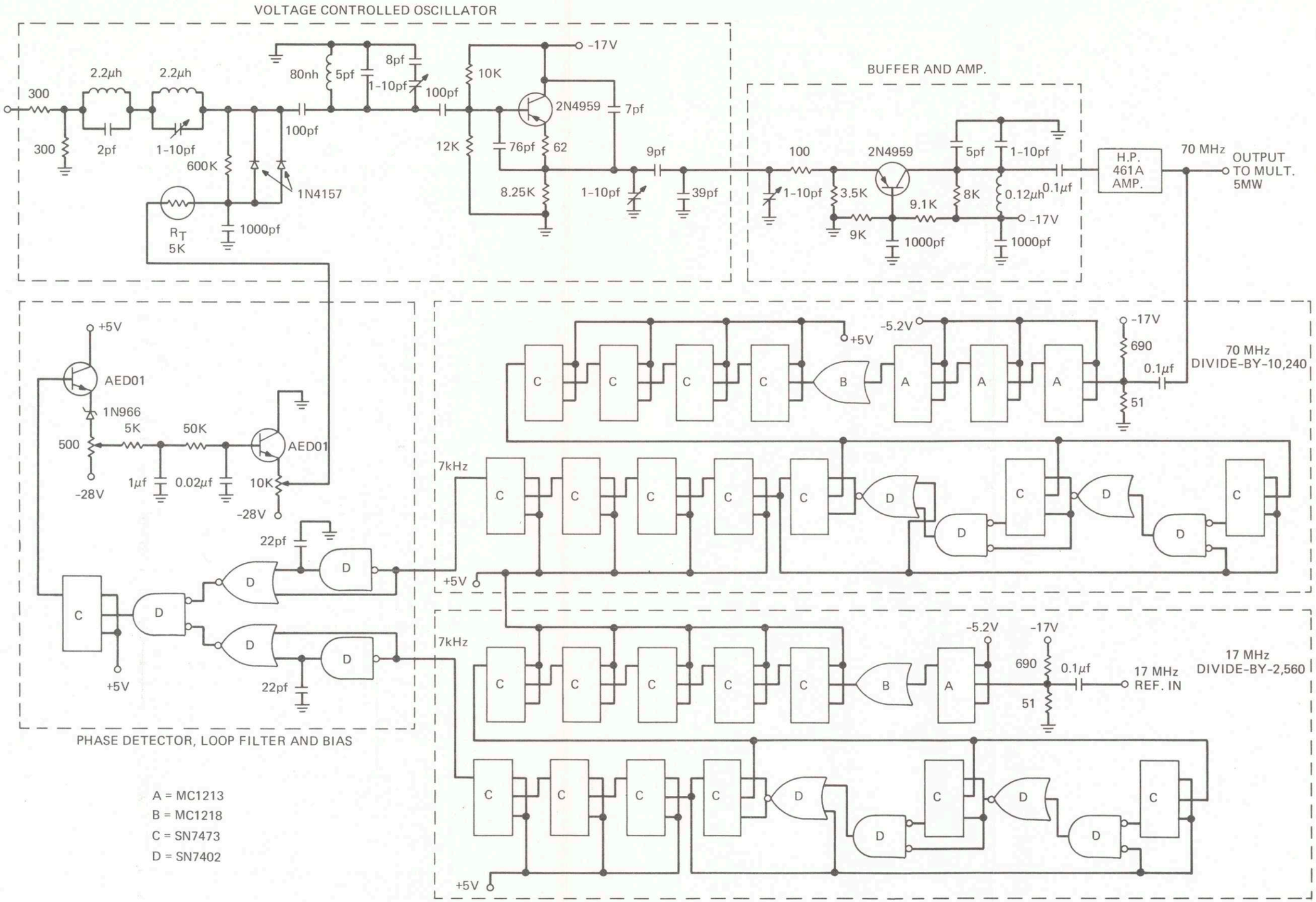


Figure VI-13. IR&D Wideband Modulator Circuit Diagram

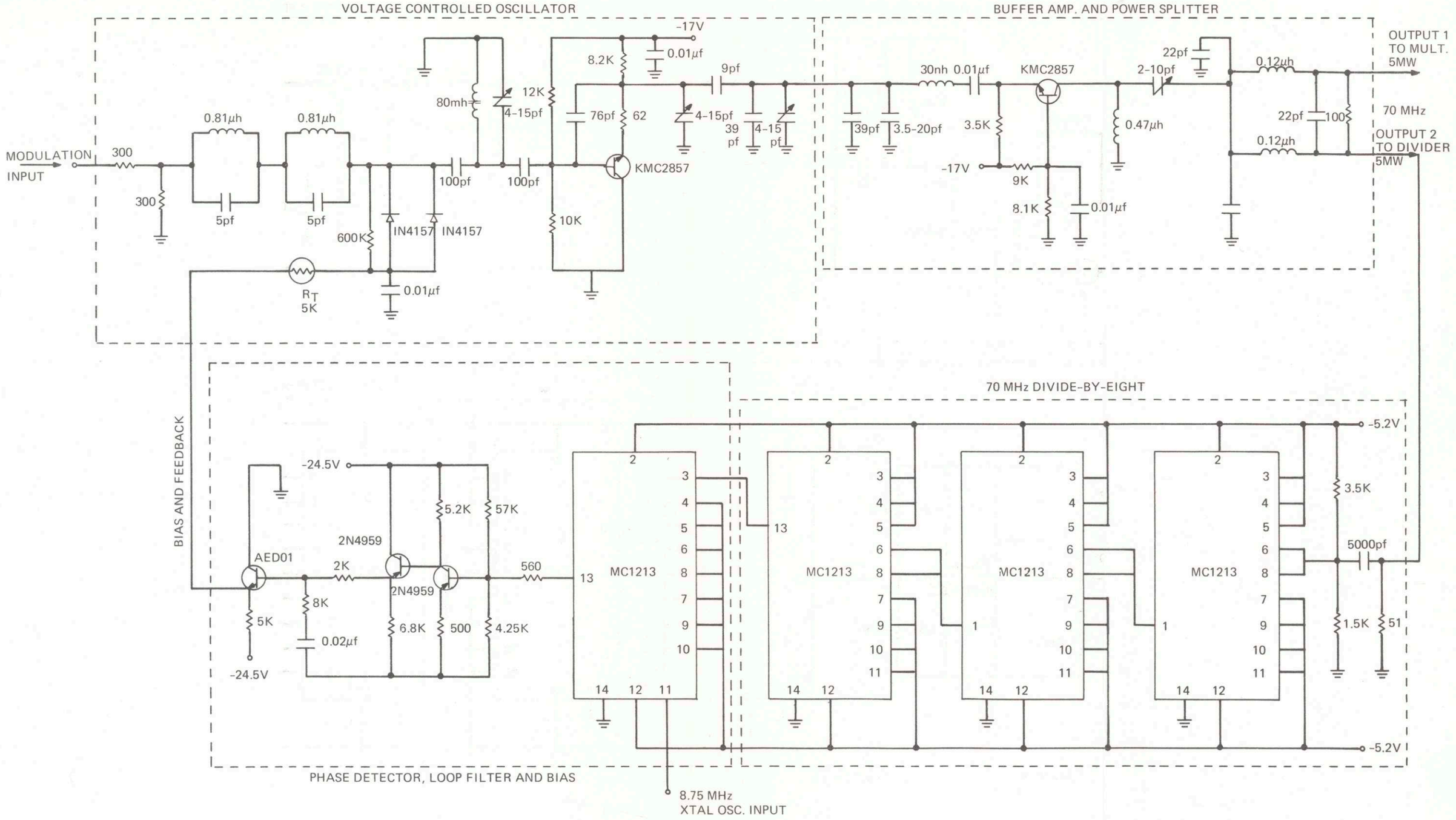


Figure VI-14. Narrowband Modulator Circuit Diagram

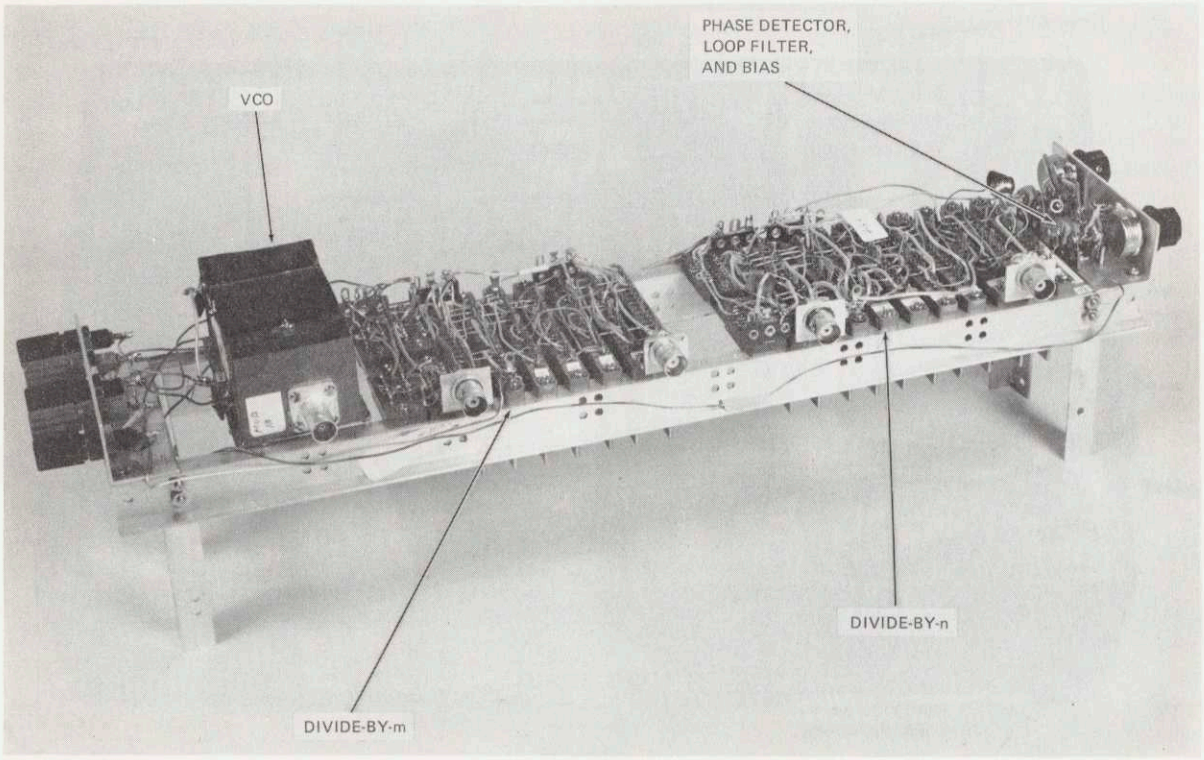


Figure VI-15. IR&D Wideband Modulator Breadboard

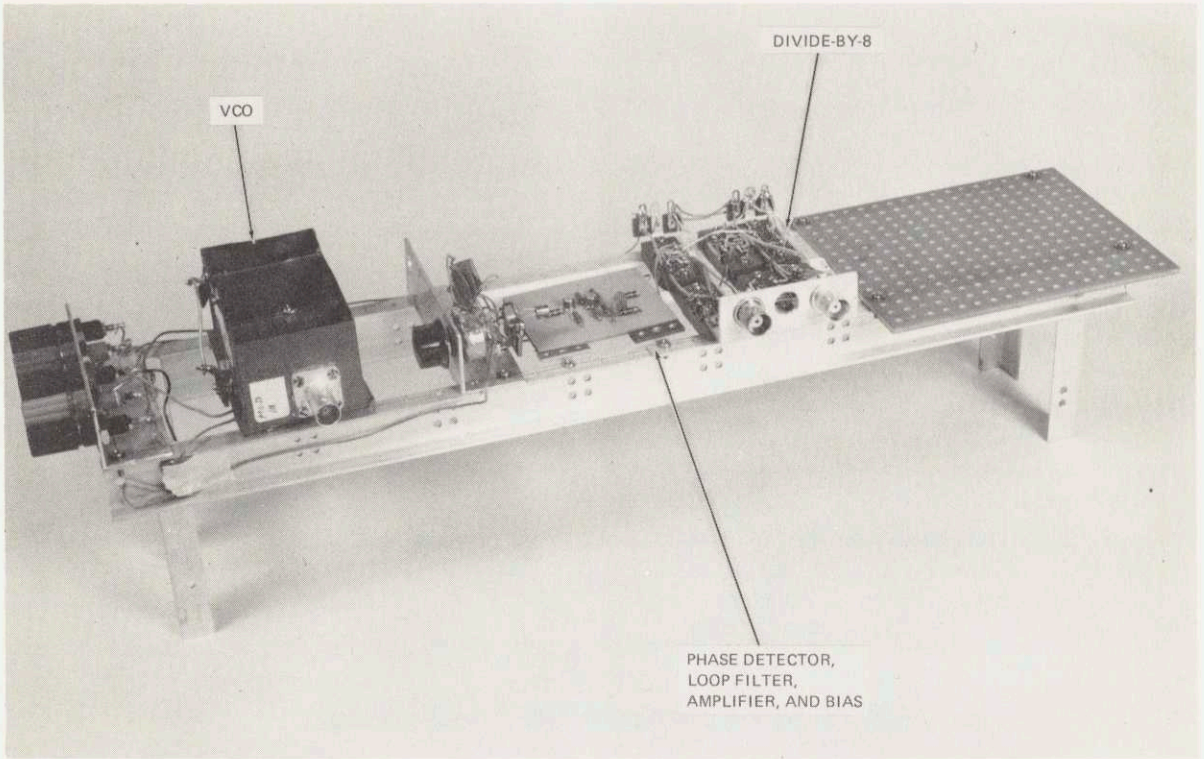


Figure VI-16. Narrowband Modulator Breadboard

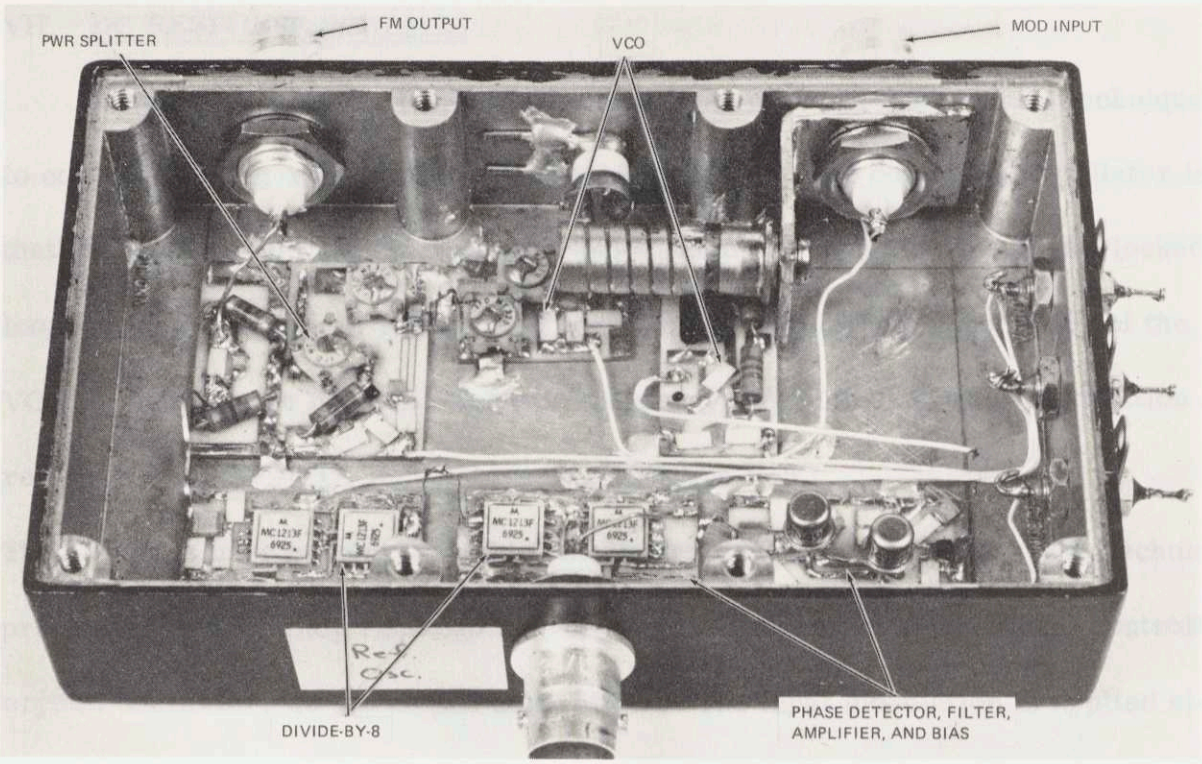


Figure VI-17. Miniaturized Version of Narrowband Modulator (Box Dimensions 4 inches × 2-1/2 inches)

VII. DC RESPONSE SCHEMES

A major problem or disadvantage of the use of phase-locked AFC techniques to control the long-range and overall stability of a voltage controlled oscillator is that the AFC system does not allow dc modulation of the VCO. The phase-locked loop shown previously in Figure IV-1 locks the average carrier frequency of the VCO to $\frac{m}{n}$ times the crystal reference frequency. All low frequency modulation is removed from the VCO, as can be seen in Figure V-5.

Two schemes have been proposed to obtain dc modulation capability. The technique proposed by Don Shipley replaces the fixed crystal reference by a voltage controlled crystal oscillator, as shown in Figure VII-1. The input modulation is applied si-

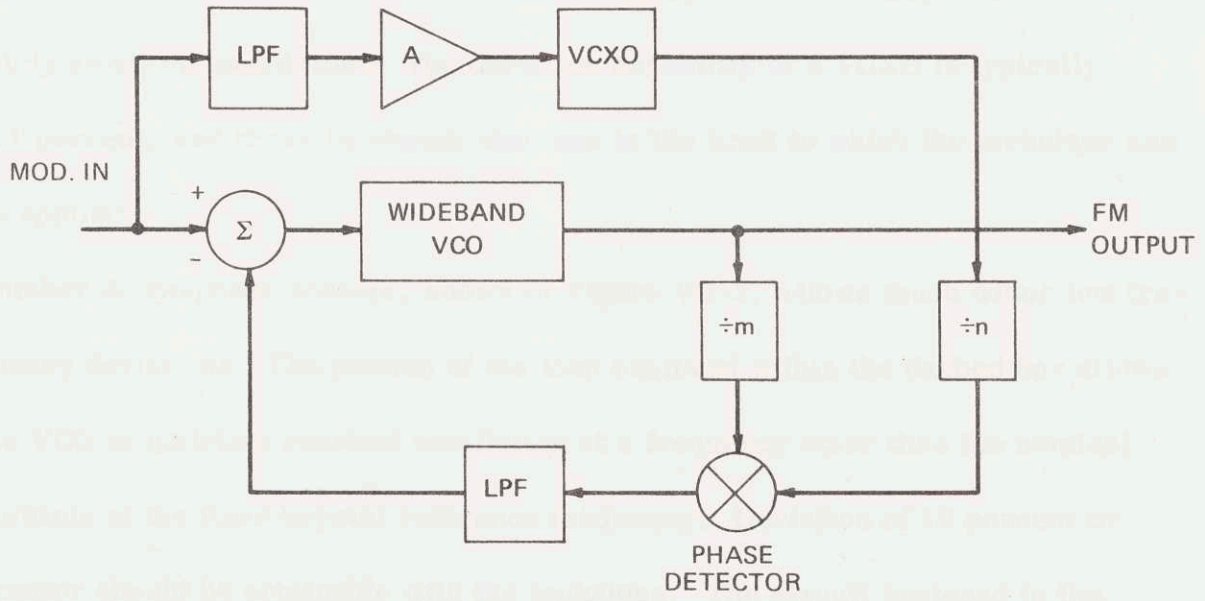


Figure VII-1. DC Response Using VCXO

multaneously to both the VCO and the VCXO. If the deviation sensitivities of the two oscillators are suitably matched, the two inputs to the phase detector are exactly equal for low modulation frequencies, and thus no unwanted correction voltage is produced. DC modulation thus passes unremoved.

There are several difficulties encountered with this technique. The deviation sensitivities of the two oscillators must be precisely matched to an exact ratio, and this becomes a critical design and adjustment task. Also, perfect crossover between the low frequency VCXO response and the high frequency phase-locked loop response is most critical and perhaps difficult to achieve. Phase differences might also pose a problem in the crossover region.

The overall stability of the phase-locked loop is now as good as that obtainable from a VCXO, not a fixed reference crystal. This slight decrease in stability is usually acceptable. The major limitation of this technique is that it only works for fairly small dc modulation. The deviation capability of a VCXO is typically 0.1 percent, and it can be shown that this is the limit to which the technique can be applied.

Another dc response scheme, shown in Figure VII-2, allows much wider low frequency deviations. The portion of the loop enclosed within the dashed box allows the VCO to maintain constant oscillation at a frequency other than the nominal multiple of the fixed crystal reference frequency. Deviation of 10 percent or greater should be obtainable with the technique. The circuit enclosed in the

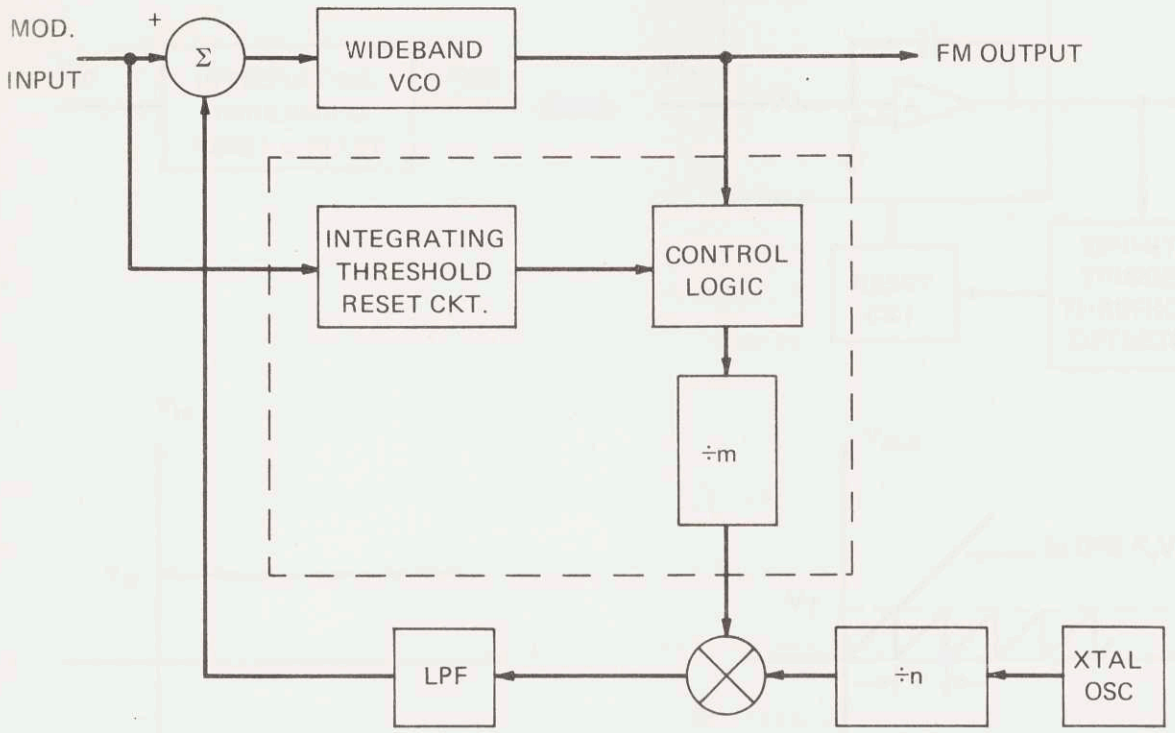


Figure VII-2. DC Response Using Variable Division Scheme

dashed box effectively eliminates the effect of a continuous offset of the VCO output frequency at the top input to the phase detector. This is done by inhibiting or adding pulses at the input of the divider at a rate proportional to the dc or low frequency modulation input. DC modulation does not pass through the variable divider and thus is not subtracted or removed by the feedback loop.

The integrating threshold reset circuit (ITRC) denoted in Figure VII-2 simply integrates the dc input voltage and resets itself when its output reaches a fixed predetermined threshold voltage V_T. This input-output relation is shown in Figure VII-3. K_i is the integrator gain, the reset rate f_r is given by

$$f_r = \frac{1}{\tau} = \frac{K_i V_o}{V_T}$$

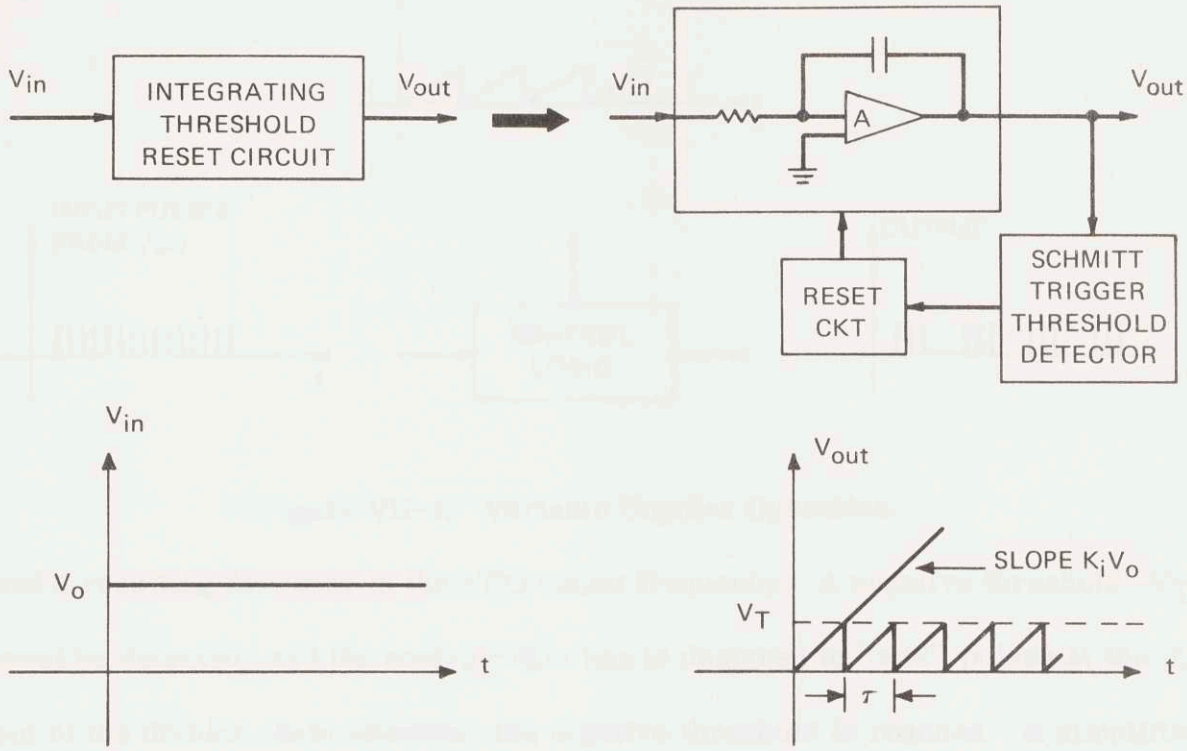


Figure VII-3. ITRC Operation

which is directly proportional to the input voltage level V_o.

For a large division ratio m, there are many (exactly m) input cycles or pulses during the interval of one output cycle. A logic control box can be inserted near the input of the divider chain to inhibit or speed up the counting process. The falling edge of the sawtooth output of the ITRC can be used to inhibit one (or more) of the input pulses. This operation is displayed in Figure VII-4.

By proper selection of the threshold voltage V_T and the integration gain K_i it should be possible to counteract an increase Δf in the VCO frequency by periodically inhibiting the correct number of input pulses. The output of the divider chain should remain fixed at $\frac{f_o}{m}$. An analogous technique is used to allow negative input voltages

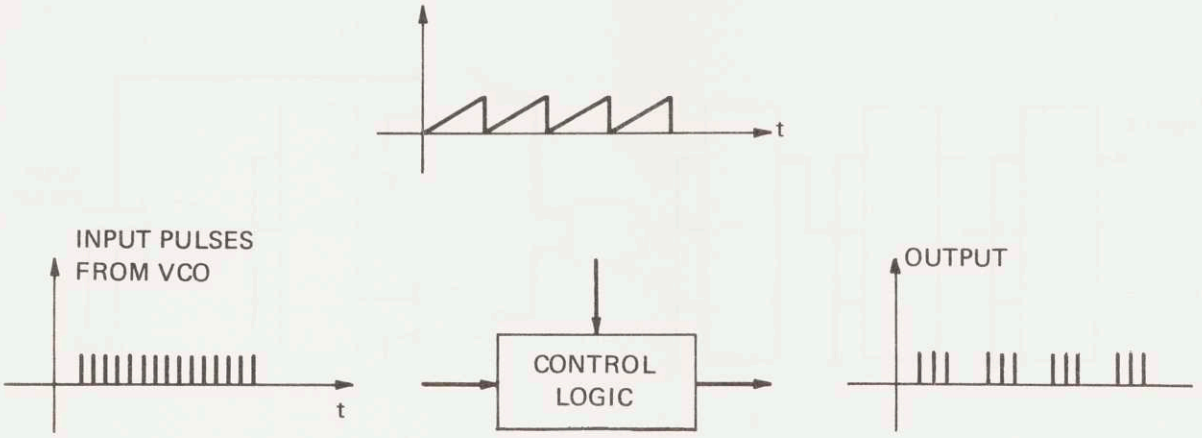


Figure VII-4. Variable Counter Operation

and a resulting decrease in the VCO output frequency. A negative threshold $-V_T$ must be detected, and the control logic box is designed to "add" pulses at the input of the divider chain whenever the negative threshold is reached. A simplified logic control design is given in Figure VII-5, using NOR gates and JK flip-flops. Assume that the reset circuit of the ITRC can be used to generate two control levels C_1 and C_2, corresponding to the occurrence of positive or a negative threshold level from the integrator. $C_1 = 1$ will inhibit the input pulse, and $C_2 = 1$ will effectively add a pulse to the count. $C_1 = C_2 = 0$ will allow each input pulse to clock the divider once.

There are three apparent problems with the variable counter dc response technique: the discreteness of the variable division, problems in the crossover region, and phase delay in the divider. The first two of these problems are easily overcome.

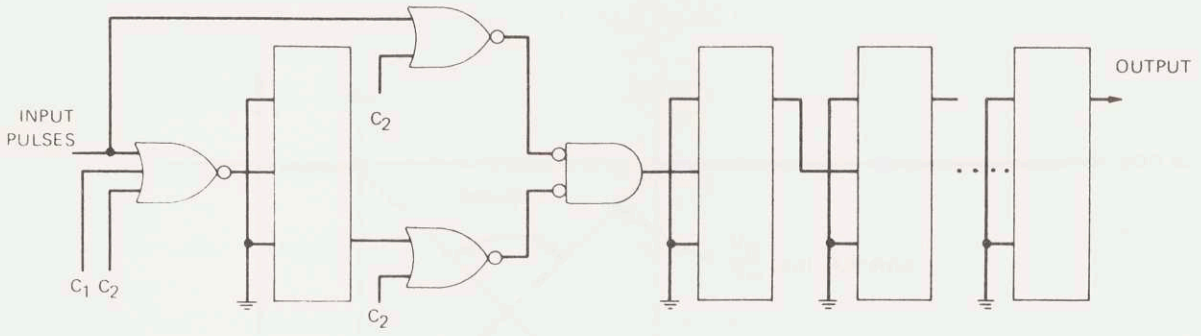


Figure VII-5. Control Circuit Example Design

Since only discrete integer division can be obtained with the variable counter, it would appear that only discrete levels of modulation will result, or that the feedback loop will cause significant modulation jitter in the VCO output. In actuality, neither of the above fears is true, because the output of the variable divider is smoothed or averaged twice by the feedback loop; once by the phase detector integrator and once by the loop low pass filter. Jitter will occur at the phase detector comparison frequency, which is doubly attenuated before being fed back to the VCO. The smoothing effect of the integrator and loop filter allows smooth continuous modulation of the VCO, within the limits of the VCO deviation capability. Problems in the crossover region between the low frequency response of the variable divider and the high frequency response of the feedback loop can easily be avoided by choosing the loop natural frequency to be significantly lower than the variable divider cutoff. An approximate Bode plot of the correction voltage relative to the modulation voltage is given in Figure VII-6. V_c' is the correction

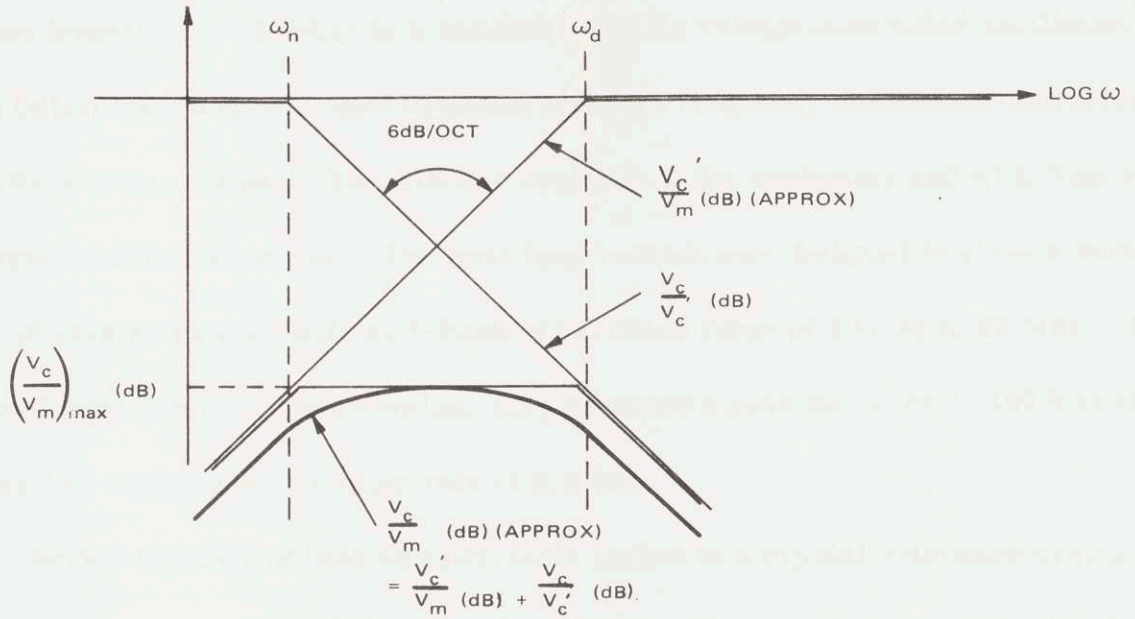


Figure VII-6. Correction Voltage Versus Modulation Voltage in the Crossover Region

voltage at the phase detector output, V_c is the correction voltage applied to the input of the VCO, V_m is the input modulation, ω_n is the loop natural frequency and ω_d is the cutoff of operation of the variable divider and ITRC. If ω_n is two orders of magnitude smaller than ω_d (easy to achieve) then the peak value of $\frac{V_c}{V_m}$ is about -40 dB.

Phase delay due to propagation delay in the divider chain is unavoidable, but is usually small. It is only of concern for modulation frequencies near or less than the loop natural frequency. The phase delay is a function of the divider length m, the average VCO frequency ω_o, and the modulation frequency ω_m, and is given by

$$\Delta\phi = \frac{2\pi m\omega_m}{\omega_o} \text{ radians.}$$

VIII. RESULTS

A digital phase-locked AFC loop has been successfully used to achieve extreme temperature stability in a wideband 68 MHz voltage-controlled oscillator. The initial open loop wideband deviation and high frequency modulation characteristics have been retained. Two similar versions of the modulator and AFC loop were designed and breadboarded. The first loop version was designed to allow a deviation of greater than 20 MHz at S-Band at deviation rates of 100 Hz to 20 MHz. The second loop, a narrowband version, only required a peak deviation of 100 kHz at S-Band at a minimum deviation rate of 5.5 kHz.

The carrier stability of both was precisely locked to a crystal reference over a temperature range of -32°C to more than +85°C. The modulation sensitivity of the VCO was measured to be 213 kHz per volt rms. Measured results of the wideband loop have shown that the 3 dB baseband response ranges from approximately 11 Hz to 11 MHz.

Excellent modulation linearity and intermodulation distortion results were obtained. Some of the measured characteristics and results are presented in tabular form. Table VII-1 lists the characteristics of the wideband modulator developed for the IR&D program, while Table VIII-2 gives the same data for the narrowband modulator. Table VIII-3 shows some typical two tone intermodulation distortion measurements for the modulator. As expected, the loop did not adversively affect the modulation characteristics of the open loop VCO. Figure VII-1 shows the measured baseband response of the wideband modulator. The response peak at the low end is due to an underdamped loop filter design.

TABLE VIII-1. WIDEBAND IR&D MODULATOR CHARACTERISTICS

Parameter	At f_o = 70 MHz	At f_o = 2.1 gHz
Modulation Sensitivity K_o	213 kHz/vrms	6.4 MHz/vrms
Max. Deviation Δf_{max} at $(f_m)_{min}$	667 kHz	20 MHz
Min. Mod. Freq. $(f_m)_{min}$	100 Hz	100 Hz
Max. Mod Index $\beta = \left(\frac{\Delta f}{f_m}\right)_{max}$	0.67×10^3	2×10^5
Temperature Stability[1]	±0.001%	±0.001%
Temperature Range[2]	-32 to +85°C	-32 to +85°C
Modulation Linearity	1% @ Δf = 250 kHz	1% @Δf = 7.5 MHz
Modulation Baseband	11 Hz to 11 MHz	11 Hz to 11 MHz
Intermodulation Distortion	See Table VIII-3	

[1] Crystal oscillator located outside of the temperature chamber.

[2] Temperature range over which loop remained in phase lock.

TABLE VIII-2. NARROWBAND MODULATOR CHARACTERISTICS

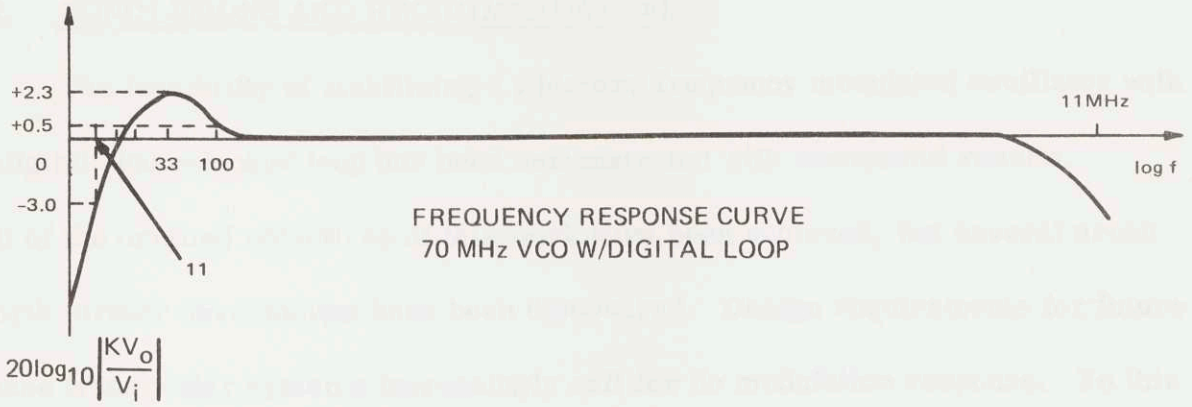
Parameter	At f_o = 70 MHz	At f_o = 2.1 gHz
Modulation Sensitivity K_o	213 kHz/vrms	6.4 MHz/vrms
Max. Deviation Δf_{max} at $(f_m)_{min}$	3.3 kHz	100 kHz
Min. Deviation Rate $(f_m)_{min}$	5.5 kHz	5.5 kHz
Max. Mod. Index $\beta = \left(\frac{\Delta f}{f_m}\right)_{max}$	0.6	18
Temperature Stability[1]	±0.001%	±0.001%
Temperature Range[2]	-30 to +80°C	-30 to +80°C
Modulation Linearity	1%@Δf = 250kHz	1%@Δf = 7.5MHz
Modulation Baseband	2kHz to 11 MHz	2kHz to 11MHz

[1] Crystal oscillator located outside of temperature chamber.

[2] Temperature range over which loop remained in phase lock.

TABLE VIII-3. TWO-TONE INTERMODULATION PRODUCTS

Tone	f(kHz)	Δf = 250 kHz Level (dB)	Δf = 400 kHz Level (dB)
f_1	500	0	0
f_2	200	0	0
$2f_1$	1000	-39	-35
$2f_2$	400	-37	-33
$f_1 + f_2$	700	-31.5	-28
$f_1 - f_2$	300	-32	-28
$2f_1 + f_2$	1200	-65	-58
$2f_1 - f_2$	800	-66	-58
$2f_2 + f_1$	900	-63	-56
$2f_2 - f_1$	100	-63	-55
$3f_1$	1500	-51	-50
$3f_2$	600	-59	-62



V_{in} = 1.18 V_{RMS} $\triangle f$ = 250 kHz

f	dB Out
5.0Hz	-10
7.6	-6.0
8.5	-5.0
9.5	-4.0
11	-3.0
12	-2.0
14	-1.0
15	-0.5
16	0
19	+1.0
25	+2.0
33	+2.3 (PEAK)
40	+2.0
70	+1.0
100	+0.5
600	0
—	—
—	—
—	—
—	—
—	—
—	—
—	—
8 MHz	—
10.0	-2.0
12.5	-3.5
16.7	-3.5

Figure VIII-1. Baseband Response of Wideband Modulator

IX. CONCLUSIONS AND RECOMMENDATIONS

The feasibility of stabilizing a wideband frequency modulated oscillator with a digital phase-locked loop has been demonstrated with successful results. All of the original objectives of this work have been achieved, but several areas worth further development have been discovered. Design requirements for future space transmitter systems increasingly call for dc modulation response. To this end, the dc response scheme described previously should be further analyzed, designed and tested for feasibility and performance. Incorporation of the quick pull-in technique described in Section VI-B.4 could prove useful in some applications. Finally, if a higher baseband response is required, the FMO should be redesigned with a center frequency of 350 or 400 MHz.

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