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Abstract: This article reports advances in high temperature (HT) GaN-on-Si technology by taking pioneering steps towards design technology co-optimization (DTCO). A computer-aided design (CAD) framework was established and experimentally validated up to 500 °C, the highest temperature achieved by such a framework for GaN technology. This framework was made possible thanks to (1) demonstration of multiple key functional building blocks (e.g. arithmetic logic unit (ALU)) by the proposed technology at HT; (2) experimentally calibrated transistor compact models up to 500 °C (highest temperature modeled for an Enhancement-mode GaN transistor). Excellent agreement was achieved between experimental and simulated circuits in the static characteristics (<0.1 V difference in voltage swing) and trends of dynamic characteristics (timing) were accurately captured. By adopting complementary approaches in experiment and simulation, this work lays the foundation for the scaling-up of HT GaN-on-Si technology for mixed-signal applications of HT (>300 °C) electronics.

Keywords: GaN, arithmetic logic unit, VLSI, high temperature, compact modeling, MVSG, computer-aided design (CAD).

Introduction

High temperature (HT) electronics is critical for emerging applications in automotive (electric vehicles), renewable energy (geothermal), oil and gas exploration (deep drilling), and aerospace (hypersonic aircraft) [1]. Such harsh environments (> 250 °C) exceed the typical rating of Silicon-on-Insulator (SOI) technology. These applications call for the deployment of wide band gap (WBG) semiconductors, where GaN, alongside SiC, stands out as a promising candidate [2].

Experimental research thus far has focused on proof-of-concept HT GaN transistors and circuits, based on a variety of logic families (Enhancement/Depletion-mode n-FET, complementary n-/p-FETs etc. [3]–[5]), transistor technologies (*p*-GaN-gate, fluorine-plasma etc. [3]–[4]), and integration (monolithic or heterogeneous [6]). However, more research effort is required on: (1) improving the performance of HT circuits; (2) accessing the long-term robustness of the transistors; (3) monolithic integration on a scalable platform to accelerate commercialization; and (4) leveraging computer-aided design (CAD) framework to achieve rapid scaling-up and reduce time-to-market.

Technology Foundation and Roadmap

The HT GaN technology used in this work (Fig. 1) stands out thanks to (1) state-of-the-art propagation delay $t_p \propto L_G^2$ at 25 °C and operational at 500 °C (highest temperature of GaN ring oscillators (ROs)) [7]; (2) long-term robustness in harsh environment (Table I and [8]); (3) monolithically integrated on 150 mm GaN-on-Si platform [7]. The technology is based on E/D-mode *n*-FETs, where the E-mode driver is the *p*-GaN-gate AlGaN/GaN high electron mobility transistor (HEMT) and the D-mode load (gate-source tied) is the AlGaN/GaN HEMT. A refractory metal (tungsten) self-aligned gate process is used to achieve high uniformity and eventual scaling for HT, high-speed applications [9].

Using complementary approaches of experiment and simulation, this work advances a roadmap for the proposed technology (Fig. 2). At its core is a novel computer-aided design (CAD) framework that is then calibrated with experimental data at both the device-level (HT transistors) and circuit-level (more complex circuits, e.g. arithmetic logic unit (ALU)). The differences between the simulation and experimental circuits are used to provide feedback on future improvements to the proposed technology.

Demonstration of Arithmetic Logic Unit (ALU)

An important milestone for the development of HT electronics would be the demonstration of a microprocessor unit (MPU). Using the proposed technology, a variety of building blocks were fabricated. NAND and NOR gates were operational at 300 °C (Fig. 3(a)–(b)). The ALU, which consists of the control bit (*A*>*B*) and an output bit (XOR), exhibits correct operation at 300 °C (Fig. 3(c)–(d)). The results are achieved at V_{DD}=5 V (a low bias for WBG circuits [10]) and without a negative bias (V_{SS}) terminal (commonly needed in SiC-based circuits [10]). The ALU maintains a voltage swing of ~4.7 V (V_{DD}=5 V) at 300 °C which indicates high noise margin at HT, and will serve as a key component of the future HT one-instruction set computer (OISC) [11].

Experimentally Verified CAD Framework for HT GaN-on-Si Technology

A CAD framework of the proposed technology would serve as a first step towards the scaling up and eventual design technology co-optimization (DTCO) [12]. A unique challenge in this framework is the need for modeling and validation over a wide temperature range. To this end, a HT-enhanced version of the industry-standard MIT Virtual Source GaN Transistor Model (MVSG) [13] was adopted to achieve excellent fit up to 500 °C (Fig. 4). Table II presents 6 key MVSG parameters with up to second-order temperature dependencies. The E-mode transistor features a unique trend in V_{TH} due to its *p*-GaN-gate. A slightly increasing V_{TH} was found up to 300 °C, which could be attributed to the increasing ionization ratio of Mg (dopant) in *p*-GaN. A decrease in V_{TH} above 300 °C is due to a lower turn-on voltage of the *p*-*i*-*n* junction (in *p*-GaN-gate) and a reduced Schottky barrier (gate metal/*p*-GaN) height [14]. A two-part equation (Eq. (1)) for V_{TH} was inserted in the enhanced MVSG.

Besides the conventional "CAD simulation path" (Fig. 2), this work also pursues the "experimental circuit validation path," which takes advantage of the experimental results to benchmark the accuracy of the proposed CAD framework. Excellent agreement is obtained in the static characteristics of the inverter and ALU at HT, as shown in the <0.1 V difference in the voltage swing (Fig. 5(a)–(b)). In terms of the dynamic (transient) characteristics, excellent fit between the experimental and simulated t_p of the RO was achieved up to 500 °C (Fig. 5(c)). A constant ~10 % deviation was found, which could be improved by using future experimental data of higher-stage ROs. For the D flip-flop (DFF), the simulation underestimates the setup time (t_{su}). However, a similar temperature-dependent trend (increase of ~8 ns) in t_{su} was found from 25 ºC to 500 ºC (Fig. 5(d)). This is the first study of GaN-based DFF up to 500 ºC. A major reason for the difference in deviations (absolute values) of t_p and t_{su} is layout parasitics, given that the fabricated RO has a significantly more compact layout than that of the DFF (Fig. 5(e)–(f)). The simulation study confirms that, at HT, the increase in t_p and t_{su} is attributed to the lower $I_{D,max}$ and higher R_{ON} in the E-mode transistor.

Benchmarking and Conclusion

To the best of the authors' knowledge, the proposed technology advances the frontier of HT electronics through the following aspects, for the first time: (1) demonstration of an ALU at 300 °C; and (2) E-mode GaN transistors were systematically characterized and modeled up to 500 °C (benchmarking in Table III). These experimental advances are supported by, and have strengthened the CAD framework for HT technology (benchmarking in Table IV): (1) the highest temperature (and widest temperature range) achieved by an experimentally verified CAD framework for GaN technology; (2) simultaneous verification and tuning of the models of two types of transistors (E-mode and D-mode) using >6 temperature-dependent parameters in the HT-enhanced MVSG; and (3) verification of CAD framework by multi-transistor (>10) ICs.

This work lays the technology roadmap of the proposed HT GaN technology and takes concrete steps towards the realization of a HT MPU and its DTCO. As part of future research, the proposed roadmap will be extended to HT (>300 °C) analog mixed-signal and power ICs. In the broader context, this work offers insights for the scaling-up of nascent semiconductor technologies (as exemplified by the proposed technology) to deliver practical microsystems.

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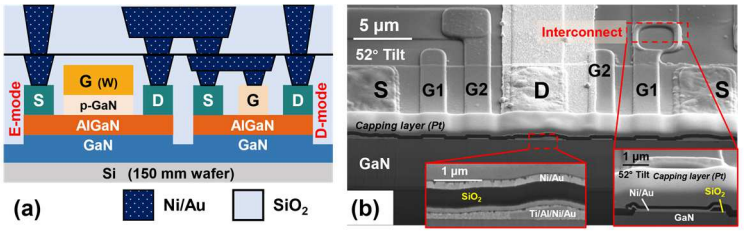

Fig. 1. (a) Proposed GaN high temperature (HT) technology based on an E/D-mode GaN-on-Si platform. (b) Tilted view shows the device structure and the cross-section (focused ion beam cut) of the fabricated circuit. Double-gate transistors are presented. The metal stack and interconnect are presented in the insets.

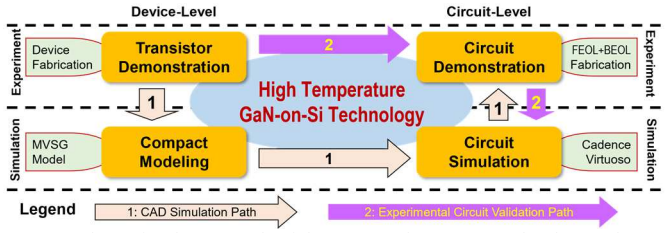

Fig. 2. Roadmap for the research of the proposed GaN HT technology. The green shapes indicate the key task or tool necessary for the accomplishment of each module. The numbered arrows indicate the two complementary pathways adopted in this work to scale up the proposed technology.

TABLE I. ROBUSTNESS OF THE PROPOSED TECHNOLOGY IN HARSH ENVIRONMENT

Specification	Change over 6 days
V_{th}	− 5 %
$I_{D,max}$	− 20 %
$\log(I_{ON}/I_{OFF})$	− 7 %
R_{ON}	+ 3 %

The E-mode transistor was tested in a simulated harsh environment (465 °C, 90 atm., corrosive gases) over 6 days. Excellent robustness was achieved, therefore serving as the technology foundation for the HT circuits of this work.

INPUT		NAND	NOR	ALU	
A	B	$\overline{AB}$	$\overline{A+B}$	$A \oplus B$	$A > B$
0	0	1	1	0	0
0	1	1	0	1	0
1	0	1	0	1	1
1	1	0	0	0	0

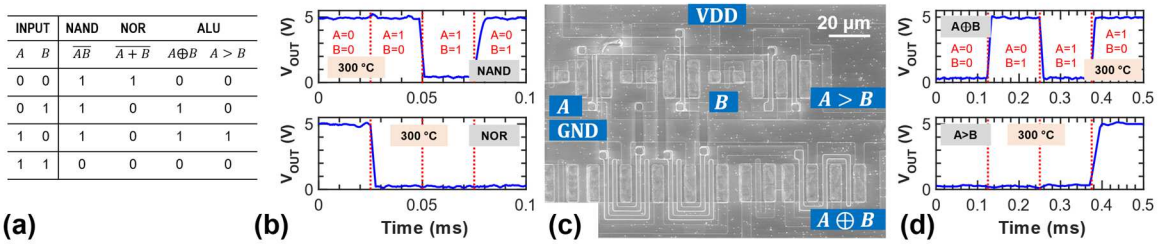

Fig. 3. Experimental demonstrations of logic gates and the arithmetic logic unit (ALU) at HT. (a) Logic table of NAND, NOR, and the ALU including their Boolean expressions. (b) Measured waveforms of NAND and NOR. (c) Micrograph of ALU after HT measurement. (d) Measured waveforms of the ALU outputs. These circuits are connected to V_{DD}=5 V and GND without the need of a negative bias (V_{SS}) terminal. The circuits are measured in a probe station with a thermal chuck whose rating is 300 °C.

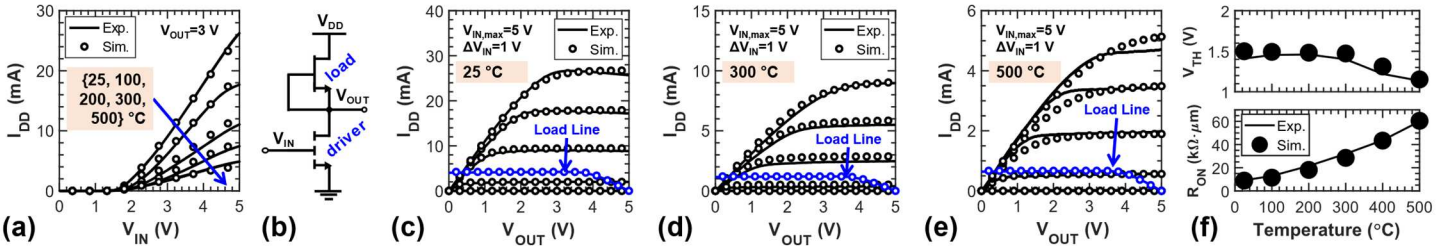

Fig. 4. Characterization and compact modeling of the transistors up to 500 °C. Industry-standard MIT Virtual Source GaN Transistor Model (MVSG) was used. (a) Transfer characteristics of the E-mode transistor (driver, W/L=36/2 μm/μm). (b) E/D-mode inverter. (c)–(e) Output characteristics of the driver with the load line (D-mode transistor, W/L=12/2 μm/μm), at {25, 300, 500} °C, respectively. (f) Summary of the key parameters of the driver transistor, V_{TH} (calculated by linear extrapolation at V_{DS}=3 V) and R_{ON} (calculated at V_{GS}=5 V, V_{DS}=0.1 V). Excellent fit was achieved using a single model for each type of transistor across a wide temperature range.

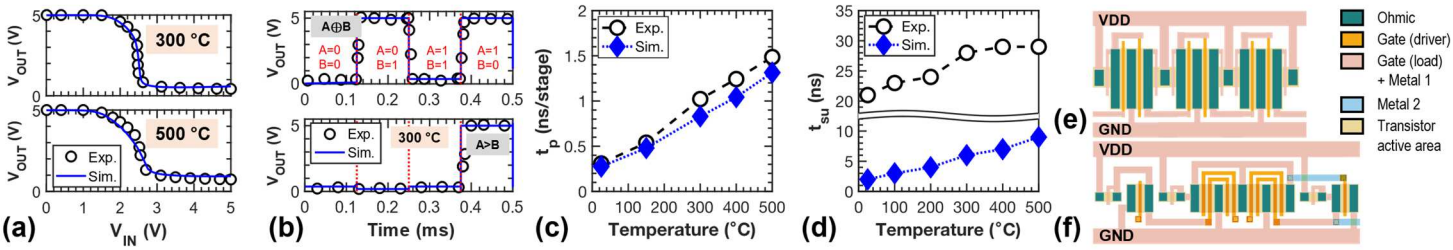

Fig. 5. Convergence of "CAD simulation path" and "experimental circuit validation path": Experimental results of the circuit proof-of-concept demonstrations are used to compare against the simulations. (a) Inverter voltage transfer curves at 300 and 500 °C. (b) Waveform of the ALU at 300 °C. (c) Ring oscillator (RO) (7-stage) propagation delay *vs.* temperature up to 500 °C. (d) D flip-flop (DFF) setup time *vs.* temperature. This is the first study of GaN-based DFF up to 500 ºC. (e)–(f) Layouts of the RO and DFF, respectively. This comparison illustrates the importance of a compact layout and the need for accurate parasitic extraction in the proposed technology. The fabricated circuits are measured up to the rating of the thermal chuck in the particular probe station (two different probe stations with ratings of 300 °C and 500 °C were used). In all circuits, V_{DD}=5 V and no V_{SS}.

TABLE II. KEY PARAMETERS OF THE MVSG MODELS

Parameter	E-mode	D-mode	Parameter	E-mode	D-mode
C_g (nF/cm²)	2.75	3.50	R_1 (10^{-3}/K)	1	6
$v(T_0)$ (10^6 cm/s)	6.5	10	R_2 (10^{-6}/K²)	22	3.6
v_ζ (10^3 /K)	1	1	$SS(T_0)$ (mV/dec)	110	110
$\mu(T_0)$ (cm²/V·s)	220	550	$V_{TH}(T_0)$ (V)	1.5	−1.6
$R_{sh}(T_0)$ (Ω/□)	1050	920	$V_{TH\zeta}$ (10^{-4} V/K)	1	−2
$R_c(T_0)$ (kΩ·μm)	1.1	1.1	$V_{TH\zeta 2}$ (10^{-3} V/K)	−1.6	0

Eq. (1): Modified equation for $V_{TH}(T)$ of the E-mode transistor

$$V_{TH}(T) = V_{TH}(T_0) + V_{TH\zeta} \times (T - T_0) + V_{TH\zeta 2}(T) \times (T - T_1)$$

$$V_{TH\zeta 2}(T) = \{0 \text{ if } T < 300, \quad V_{TH\zeta 2} \text{ if } T > 300\}, \ \{T_0, T_1\} = \{25, 300\}\,°C \quad -(1)$$

TABLE III. BENCHMARKING OF HT E-MODE GAN HEMTS

Feature \ Publication	[3] (2007)	[16] (2022)	[14] (2015)	[17] (2020)	This Work (2023)
Transistor type	F-plasma	MIS	*p*-GaN gate	*p*-GaN gate	*p*-GaN gate
Highest temp. (°C)	375	250	420	175	500
Compact modeling	–	–	–	✓	✓

This work features the highest temperature at which an E-mode GaN transistor is systematically characterized and then modeled.

TABLE IV. BENCHMARKING OF RECENTLY PUBLISHED HT GAN CIRCUIT SIMULATIONS

Feature \ Publication	[18] (2021)	[19] (2021)	[20] (2022)	[15] (2022)	This Work (2023)
Wafer	GaN-on-Sapphire	GaN-on-Si	GaN-on-SiC	GaN-on-SiC	GaN-on-Si
Technology	D-mode (HEMT)	Complementary (p-GaN-gate HEMT + *p*-FET)	D-mode (HEMT)	D-mode (HEMT)	E/D-mode (*p*-GaN-gate HEMT + HEMT)
Integration	3D Bonding	Monolithic	Monolithic	PCB	Monolithic
Highest temperature (°C)	300	300	160, 400, 550	220	500
V_{DD} (V)	0	5	14	20	5
V_{SS} (V)	−12	No V_{SS}	−14	N.A.	No V_{SS}
Circuit experiment	Oscillator at 1 GHz	–	NAND/NOR, DFF, Voltage ref.	Transmitter at 2 GHz	ALU
Circuit simulation	(same as above)	RO, SRAM	Passive components	(same as above)	ALU, RO, DFF
Circuit sim. verified by exp.	✓	–	–	✓	✓

Highlights of the proposed CAD framework include: (1) the highest temperature (and widest temperature range) achieved by an experimentally verified CAD framework for GaN technology; (2) simultaneous verification and tuning of the models of two types of transistors (E-mode and D-mode); (3) verification of CAD framework by multi-transistor (>10) ICs.

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