Superconducting Nanowire Technology for Microwave and Photonics Applications

by

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Abstract

Quantum computing and quantum communication are innovative technologies promising to revolutionize several aspects of our societal landscape. However, early cutting-edge experiments are rapidly approaching significant scalability roadblocks. As the qubit count increases, superconducting quantum processors require an increasing number of control and readout electronic devices, which are incompatible at scale with the performance of dilution refrigerators. Photonic-based platforms struggle with integration issues due to operational, design, and heterogeneous material compatibility.

In this thesis, we demonstrate that superconducting nanowires have the potential to drive a major leap in the scalability of these and other architectures. We show that the exotic microwave properties of superconducting nanowires enable cryogenic devices at microwave frequencies with an ultra-compact footprint. We introduce microwave directional couplers and resonators featuring a footprint reduction of up to 200 times, making them suitable for on-chip integration with superconducting quantum processors and in any application needing cryogenic microwave signal processing.

Furthermore, we engineer the nanowire properties to overcome the metrics trade-offs of single-photon detectors. We demonstrate an all-in-one nanowire detector with record performances, imaging capabilities, and photon-number resolution capabilities, all in the same design. Our device can be used to scale experiments needing many high-performance detectors.

Finally, we demonstrate single-photon detectors integrated on lithium-niobate-on-insulator with state-of-the-art performance. We also introduce integrated array technology on silicon-on-insulator. Our nanowire technology can be on-chip heterogeneously integrated with current quantum photonic platforms, removing the need for out-coupling to fiber-coupled detectors.

In conclusion, superconducting nanowires have the potential to become a comprehensive solution for scaling classical and quantum architectures.

Thesis Supervisor: Karl K. Berggren
Title: Professor of Electrical Engineering and Computer Science

To Sara

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Chapter 1

Introduction

Quantum computing is an innovative technology that utilizes the concepts of quantum mechanics, including superposition, entanglement, and interference, to address computational challenges that are beyond the capabilities of traditional computing systems [1, 2, 3, 4]. Quantum computers promise to revolutionize computational biology and chemistry [5], medicine [6, 7], weather prediction [8, 9], and financial optimization [10], and offer significant speed-up for complex, time-consuming computational tasks [11]. However, while the excitement about the prospect of this technology is palpable, the actual route to scalability and commercialization is still arduous and uncertain.

Superconducting quantum computing, one of the most promising architectures relies on dilution refrigeration technology to cool down the quantum processors to milli-Kelvin temperatures [12, 13]. As the number of qubits increases, a more complex control and readout electronics is required. With that, more physical cables, more internal wiring, more discrete microwave components, and more challenging interconnects [14, 15, 16]. Unfortunately, due to the limited cooling capacity of dilution refrigerations and hard physical design constraints (i.e., it is unrealistic to scale the dimension of cryostats even more), the current infrastructure paradigm is unlikely to support increasingly demanding requirements and the scalability of this technology is at stake [17, 18].

Quantum technology using photons (e.g., photonic quantum computing and information processing [19, 20, 21, 22, 23], boson sampling [24, 25, 26], etc.) hold the promise of operation at room temperature and a straightforward interface to telecom fibers, with a prospect for an extensive network of interconnected systems [27]. However, their scalability relies on

the heterogeneous integration of several technologies, including photon sources, memories, photonic circuits, and detectors. Specifically, the technology of choice for single photon detectors is often cryogenic [28] (e.g., superconducting nanowire single-photon detectors (SNSPDs) or transition edge sensors (TESs)). Integrating, controlling, and reading out a large number of single-photon detectors will result in similar scalability issues as the superconducting quantum computing hardware. Ultimately, quantum architectures will not scale effectively without a major technological revolution.

Development and integration of cryogenic microwave circuitry and photonic devices represent the first step toward solving these scalability bottlenecks. For superconducting quantum computing, we need integrated cryogenic microwave devices to replace the bulky components and perform on-chip data processing and reduction. For scaling superconducting detectors for applications in photonics, we need a reliable integration technology with photonic platforms, multiplexing, microwave signal routing, and processing strategies.

In this thesis, we demonstrate the potential of superconducting nanowires in addressing and solving the scalability challenges of these quantum and other classical applications. We engineer the exotic properties of superconducting nanowires to develop ultra-compact cryogenic microwave devices that could be integrated with current superconducting quantum computing hardware. We use these properties to improve the performance of superconducting single-photon detectors. Finally, we develop processes to integrate and multiplex a large number of detector elements on quantum photonic platforms.

In the next section, we briefly introduce superconducting nanowires, their main applications, and their challenges.

1.1 Superconducting nanowires

Superconducting nanowires (SNs) are quasi-one-dimensional nanofabricated structures made of thin film superconductors. Their usual width is of the order of $w \approx 100\,\text{nm}$, and their thickness d ranges between 5 nm and 15 nm, depending on the application. They are generally fabricated out of type-II superconductors —the most popular are niobium nitride (NbN), niobium titanium nitride (NbTiN), tungsten silicide (WSi), and molybdenum silicide (MoSi). These materials are generally deposited with sputtering and their critical temperature and sheet resistance vary according to the thickness and stoichiometry. Unless specific applica-

tions are pursued, devices are normally designed to have a critical temperature above 4 K, to be easily tested in state-of-the-art $1\,\mathrm{K} - 2\,\mathrm{K}$ refrigeration systems. The room-temperature sheet resistance of nanowires $R_\mathrm{s} = \rho/d$ is about $100\,\Omega$ to $1\,\mathrm{k}\Omega$ per square, where ρ is the room-temperature resistivity. Superconducting nanowires can support currents without resistance up to (or slightly below) the corresponding theoretical, critical current density. We call this threshold the *critical* or *switching* current, of the order of μA. Above this threshold, the nanowire is approximately a resistor with a value $R_\mathrm{s}L/w$, where L is the length of the wire.

Single-photon detectors (SPDs) are undoubtedly the most popular application of this technology. In the SNSPDs, a single photon can break the superconducting state of the nanowire, leading to a measurable output response. These detectors have outstanding performances in most relevant detection metrics, from visible to mid-infrared wavelength. In Section 1.1.1, we briefly introduce this popular technology.

SNs have also been used as a platform for cryogenic nanoelectronics. In these devices, superconducting nanowires of different widths are combined with constricted sections (e.g., notches [29], sharp corners [30]) to manipulate the supercurrent and obtain electronic functionality. The n-Tron [29], for example, is a three-terminal device where the current flowing in the *channel*, source to drain, is controlled with the current injected through a narrower *gate*. By sizing the device accordingly, and combining several elements, one can obtain amplification and switching behaviors and one can realize logic gates [31] and memory cells [32, 33]. The application of superconducting nanowires as nanoelectronics elements will not be part of this thesis. For more details on the topic, we direct the reader to the works at Refs. [34, 35, 36, 37, 38].

Lastly, superconducting nanowires have unusual and unique microwave properties. Due to their extremely reduced size compared to the vacuum wavelength of microwave signals, SNs were always treated as lumped elements in applications (i.e., an inductor in series with a time- and event-dependent resistor). However, a few seminal studies showed that long superconducting nanowires were characterized by distributed behaviors (self-resonance) at modest GHz frequencies [39, 40]. Thin film superconducting nanowires behave as transmission lines with two main exotic properties: (a) a characteristic impedance much higher than the $50\,\Omega$ standard —generally in the kΩ range; (b) a velocity factor (v/c) much lower than the coaxial standards $0.6 - 0.8$ —and equivalently, an effective index ($n = c/v$) much

higher, about 50 times, than what could be achieved in traditional printed circuit boards (PCB) devices. These properties were first deemed deleterious for conventional applications: the insertion loss of nanowire devices is very high when combined with normal electronics due to the high impedance, and the compressed microwave signal leads to time delays and uncertainties. However, engineering the microwave dynamics of superconducting nanowires resulted in novel detector architectures [41, 32] and improved performances [42, 43]. More details on these points are available throughout this thesis: these properties are at the base of the technologies presented in this work. In Sec. 1.1.2, we provide more details on nanowire microwave devices.

1.1.1 Superconducting nanowire single-photon detectors

Introduced in 2001 [44], SNSPDs are currently the highest-performing and most popular single-photon counting technology at near-infrared wavelengths. Unlike the other technology used in this space, photomultiplier tubes (PMT) and single photon avalanche photodiodes (SPADs), SNSPDs can combine high detection efficiency, high timing resolution, and low noise [28] in the same detector design, at the expense of lower operating temperatures. Here, we provide a summary of the main characteristics of superconducting nanowire detectors to help the understanding sections following in this thesis. For more details, we refer the readers to specialized reviews on the topic [45, 46].

Working principle

The SNSPD consists of a current-biased closely-packed superconducting nanowire, with the same physical characteristics described above. A single photon of energy $E_{\mathrm{ph}} \approx 1\,\mathrm{eV}$, incident on the wire, can break a cooper pair ($E_{\mathrm{ph}} \gg \Delta$, with Δ the superconducting gap), creating an excited electron, which we call *quasiparticle*. The hot electron will relax, creating a cascading process that mostly converts into energetic phonons over a timescale of few tens of femtoseconds. This initial-state energetic *phonon bubble* will further down covert into a state where many electrons and phonons are thermalized at a certain temperature. This cascading process takes about half a picosecond. These energetic clouds will diffuse and convert into a dissipative stage, generating a normal, resistive region called a *hotspot*. The hotspot will rapidly expand ($\sim$ ps) under electrothermal feedback and divert the bias current to the load in the readout circuit, creating a detectable voltage pulse. As the current leaves

the nanowire, the hotspot will cool down, and the detector will reset with an exponential dynamic with a time constant ($\tau \sim 10\,\text{ns}$) [46, 47].

Main detection metrics

There are several performance metrics for SNSPDs. The most relevant for applications are:

- **Dark count rate (DCR)**: false counts from SNSPD, with no illumination. Unit: count per second (cps). Typical: 1-100 cps. Trend: best if low. Record: 1.6×10^{-7} cps [48].

- **System detection efficiency (SDE)**: effective count rate (count rate - dark count rate) normalized by the number of photons sent to the detector. Includes all the system and detector losses. Unit: a.u. Typical: 50% - 80%. Trend: best if approaching unity. Record: $> 98\%$ [49, 50].

- **System jitter**: uncertainty on the arrival time of the electrical pulse on the readout —timing resolution. Includes other system contributions and it is dependent on photon wavelength and bias level. Unit: ps. Typical: 20 ps. Trend: best if low. Record: 4.6 ps (at 1550 nm) [42].

Other relevant metrics include maximum count rate, wavelength range, photon number resolution, pixel number, and operating temperature. Developing an all-in-one architecture, capable of achieving record performance in several metrics is necessary to enable the scalability of modern demanding quantum experiments. We will show our advancements in this area in Chapter IV.

Waveguide integrated SNSPDs

The SNSPD was developed at first as a free-space/fiber-coupled element. Namely, the nanowire is illuminated by projecting light onto its active area. With the advent of photonic integrated circuits (PIC), to avoid the lossy out-coupling to optical fibers and minimize the overall footprint and circuit complexity, waveguide integrated SNSPDs (WGSNSPDs) were developed [51]. In these structures, the nanowire is directly in contact with the waveguide, coupled with the evanescent field of the guided mode. WGSNSPDs generally consist of a single hairpin detector, and the reduced area leads to a higher time resolution and faster reset

dynamics [51]. However, the fabrication technology is overall more challenging because the superconducting processing must be compatible and integrable with PIC technology. These emerging detectors have been integrated on several traditional waveguide platforms (e.g., SiN, silicon-on-insulator (SOI), GaAs). However, integration with popular novel quantum optics platforms (e.g., thin-film lithium niobate-on-insulator (LNOI) [52]) is slower due to technological compatibility issues.

Arraying strategies

Several strategies are being developed to increase the number of active pixels N^2 in a sensor while reducing and limiting the number of input/output electrical lines. Thermal row-column arrays exploit the thermal coupling between two orthogonal photosensitive layers to achieve spatial resolution with $2N$ readout lines [53]. Time-domain multiplexed arrays [54, 41] exploit the slow propagation speed in superconducting nanowires to interleave pixels with delay lines and read them with a differential readout with just 2 readout outputs. More advanced architectures combine several methods to achieve complex functionalities and a higher pixel count [55].

Developing fabrication technology for integrated high-performance detectors, and novel multiplexing strategies for larger arrays are fundamental stepping stones to guarantee the advancement and scalability of quantum photonic integrated circuits [56]. We will show our advancement in these areas in Chapter V.

1.1.2 Cryogenic microwave circuitry with superconducting nanowires

Cryogenic microwave circuitry has collected renewed interest in recent years thanks to the emergence and development of quantum computing based on superconducting qubits [57, 58]. In these architectures, various microwave devices —such as filters, resonators, couplers, circulators, and traveling-wave parametric amplifiers —are required to drive and perform operations [59]. With the number of qubits increasing, these components are also expected to significantly increase. However, if this happens linearly, the external electronics will constitute the main bottleneck in creating large-scale quantum technology [18]. Integrated circuitry must be therefore pursued. Unfortunately, the size of distributed components is

limited by the wavelength of the signal, which is in the $\sim$ cm for $\sim$ GHz frequency, making integration extremely challenging.

As mentioned in the Introduction, superconducting nanowires exhibit peculiar distributed microwave properties. One of the first studies of microwave dynamics in long nanowires was performed by Santavicca et al. [40]. They observed that a 0.5 mm-long 100 nm-wide wire exhibited a self half-wave resonance at $f_{\mathrm{res}} = 12\,\mathrm{GHz}$. This result broke the lumped-element model of nanowires devices but, most importantly, showed that the light in the nanowire propagated at speed $c/(2lf_{\mathrm{res}}) = 25$ times slower than in vacuum, or equivalently the microwave wavelength was compressed by the same amount. As a matter of fact, nanowires made of disordered thin films behave as slow-speed transmission lines thanks to their strong kinetic inductive behavior. By engineering the microwave properties of nanowires to compress the microwave wavelengths even more, we can create ultra-compact cryogenic integrated microwave electronic devices. This technology could constitute the foundation for on-chip integrated microwave electronics and solve the scalability bottlenecks of quantum hardware and several other applications requiring low-temperature signal handling and processing (e.g., superconducting quantum interference device (SQUID) magnetometry [60, 61], radio astronomy [62, 63]). We will discuss our advancement in these directions in Chapter III.

1.2 This thesis

In this thesis, we will first describe how to engineer the properties of superconducting nanowires to demonstrate ultra-compact cryogenic microwave devices. The objective is to provide a path toward the solution of the hardware scalability challenges of superconducting quantum computing and applications requiring low-temperature signal processing. We will then leverage the microwave properties of nanowires to address performance trade-offs in SNSPDs. We will introduce an improved detector design that combines high SDE with record low timing jitter and previously-unavailable properties, such as imaging capabilities and photon number resolution. Finally, we will introduce integrated detector technology on lithium-niobate on-insulator waveguides, achieving state-of-the-art SDE. We will also show preliminary work on integrated waveguide detector arraying and multiplexing. These technologies can be adopted to address the scalability of detectors on quantum photonic

platforms.

The thesis is structured as follows. Chapter II will briefly introduce the exotic microwave properties of superconducting nanowires. We will show how the kinetic inductance is responsible for the high impedance and slow propagation velocity in superconducting nanowire transmission lines, and we will introduce a few engineered architectures. We will use these structures in Chapter III to demonstrate an ultra-compact high-impedance microwave directional coupler and ultra-compact resonators. These devices are the basis of the envisioned integrated microwave electronics. In Chapter IV, we will show that by engineering the structures of SNSPDs according to their microwave characteristics, one can solve the trade-offs between performance metrics and combine advanced properties. In Chapter V, we will introduce waveguide-integrated detectors on lithium niobate and show an integrated 65-channel detector on silicon-on-insulator waveguides. Appendix A will include a collection of fabrication processes and tips useful for readers and fellow students to reproduce the results of this thesis.

Chapter 2

Superconducting nanowire microwave properties and engineered transmission lines

In this chapter, we provide a brief introduction to the exotic microwave properties of superconducting nanowires. We show how the kinetic inductance is responsible for the high impedance and slow propagation velocity in superconducting nanowire transmission lines. We also provide an analytical framework for designing these structures.

2.1 Kinetic inductance

The kinetic inductance is the equivalent series inductance of a material caused by the inertia of the mobile charge carriers in an alternating electric field [64]. Its contribution is present in any conductor but becomes particularly relevant in superconductors or at high frequencies [65]. It is at the base of the operation of many superconducting devices, including detectors (e.g., MKIDs, SNSPDs) and microwave devices (e.g., resonators, KPUPs). This section briefly introduces the theoretical foundation of kinetic inductance and provides useful relations for device design. We will start with the application of the Drude model.

Drude model

In the Drude model, the dynamics of electrons of charge $-e$ and mass m in the presence of an electric field E is described by a global equation of motion [66]:

$$\frac{dv}{dt} = -e\frac{E}{m} - \frac{v}{\tau}, \tag{2.1}$$

where v is the velocity, and τ is the characteristic collision time. By introducing the notion of current density in a conductor $j = -nev$, with n the density of electrons, we can rewrite the equation for the electric field:

$$E = \rho j + \mathcal{L}_{\text{kin}}\frac{dJ}{dt}, \tag{2.2a}$$

$$\rho = \frac{m}{ne^2\tau}, \tag{2.2b}$$

$$\mathcal{L}_{\text{kin}} = \frac{m}{ne^2}. \tag{2.2c}$$

The first term ρ represents the usual microscopic Ohm's law, while the second term $\mathcal{L}_{\text{kin}}$ is the *kinetic inductivity*. $\mathcal{L}_{\text{kin}}$ has unit $\left[\frac{\text{kg}\cdot\text{m}^3}{\text{C}^2}\right] = [\text{H}\cdot\text{m}]$ and, for a normal metal, it is $\approx 10^{-20}\,\text{H}\cdot\text{m}$, hence it is relevant only at $\frac{R}{L} = \frac{\rho}{\mathcal{L}_{\text{kin}}} = \frac{1}{\tau} \sim$ THz frequency, and for this reason, generally neglected. In superconductors, $\tau \to \infty$, and the kinetic inductive term becomes relevant down to DC [67]. Note that if we assume that the carriers of the superconducting state are coupled electrons with density $n_{\text{s}} = \frac{1}{2}n$, mass $m^* = 2m$, and charge $q = -2e$, the inductive term is ultimately invariant $\mathcal{L}_{\text{kin}} = m^*/(n_{\text{s}}q^2)$. The application of the Drude model shows that in superconductors, a kinetic inductive component must be considered in addition to the standard magnetic inductance.

London Description

The same result of Eq. 2.2c is obtained by considering the London's equations in the two-fluid model picture, i.e., the carriers in a superconductor consist of ground-state frictionless coupled electrons (superelectrons) and excited normal electrons (quasiparticles). We consider the first London's equation:

$$\frac{\partial j_{\text{s}}}{\partial t} = \frac{n_{\text{s}}e^2}{m}E, \tag{2.3}$$

where we dropped the vector notation, and with j_s the current density given by the superelectrons. We assume the current density is homogeneous in the superconductor. Assuming an oscillatory behavior of the electric field $E = E_0 \exp(\,\mathbb{j}\omega t)$ we have:

$$j_\mathrm{s} = -\mathbb{j}\frac{n_\mathrm{s}e^2}{m\omega}E = \sigma_\mathrm{im,s}E, \tag{2.4}$$

where $\sigma_\mathrm{im,s}$ is the imaginary component of the complex conductivity, given by the superelectrons. If we were to take into account the quasiparticles, the overall complex conductivity would read:

$$\sigma_\mathrm{total} = \sigma_\mathrm{real} - \mathbb{j}\sigma_\mathrm{im} = \sigma_\mathrm{real} - \mathbb{j}(\sigma_\mathrm{im,n} + \sigma_\mathrm{im,s}), \tag{2.5}$$

with

$$\sigma_\mathrm{real} = \frac{ne^2\tau}{m(1+\omega^2\tau^2)}, \tag{2.6a}$$

$$\sigma_\mathrm{im,n} = \frac{n(e\tau\omega)^2}{m\omega(1+\omega^2\tau^2)}. \tag{2.6b}$$

Assuming $\omega^2\tau^2 \gg 1$ and a temperature $T \ll T_\mathrm{C}$, such that the density of quasiparticles is negligible, thus $\sigma_\mathrm{real}, \sigma_\mathrm{im,n} \ll \sigma_\mathrm{im,s}$, the complex conductivity is:

$$\sigma_\mathrm{total} = -\mathbb{j}\frac{n_\mathrm{s}e^2}{m\omega} = -\mathbb{j}\frac{1}{\omega\mathcal{L}_\mathrm{kin}}. \tag{2.7}$$

This expression resembles the one of the admittance for an inductive component, with $\mathcal{L}_\mathrm{kin} = m/(n_s e^2)$, the same conclusion of the Drude model (Eq. 2.2c). However, with the London model, we can go a little further into the derivation. Let's consider the second London's equation and manipulate it with Ampere's law:

$$\nabla \times \nabla \times \mathbf{B} = -\frac{n_\mathrm{s}e^2}{\mu_0 m}\mathbf{B} \quad \rightarrow \quad \nabla^2\mathbf{B} = \frac{1}{\lambda_\mathrm{L}^2}\mathbf{B}. \tag{2.8}$$

We obtain the Helmholtz's equation for the magnetic field, where $\lambda_\mathrm{L} = \sqrt{\frac{m}{\mu_0 n_\mathrm{s}e^2}}$ is the London penetration depth, the characteristic length over which external magnetic fields decay into a superconductor. With a final manipulation, we obtain:

$$\mathcal{L}_\mathrm{kin} = \frac{m}{n_\mathrm{s}e^2} = \mu_0\lambda_\mathrm{L}^2, \tag{2.9}$$

connecting the concept of kinetic inductance with the magnetic field penetration in a superconductor.

Surface Impedance

While the complex conductivity concept we introduced above is not directly experimentally accessible, we can generally resort to the complex surface impedance Z_s[1] [Ω per square]. For a good conductor, taking the standard form of the skin depth [65]:

$$Z_s = \left(\frac{\jmath\omega\mu_0}{\sigma} \right)^{1/2}. \tag{2.10}$$

We can replace the complex conductivity with the result from the London's model (Eq. 2.7), in the case of a superconductor at $T \ll T_C$, and obtain:

$$Z_s \approx j\omega\mu_0\lambda_L. \tag{2.11}$$

In thin films (thickness $d \ll \lambda_L$), the penetration depth is replaced by an effective thickness-dependent thin-film penetration depth introduced in the classic 1964 paper by Pearl [68]:

$$\lambda_{eff} = \frac{\lambda_L^2}{d} = \frac{\Lambda_p}{2}, \tag{2.12}$$

where Λ_p is the Pearl length. In this situation, the surface impedance is enhanced by a factor λ_L/d, becoming much greater and thickness dependent:

$$Z_s \approx \jmath\omega\mu_0\frac{\lambda_L^2}{d} = \jmath\omega L_{kin,s} \tag{2.13}$$

where $L_{kin,s} = \mathcal{L}_{kin}/d$ is the sheet kinetic inductance[1]. It can be shown that in the case of thin films, the surface impedance is given by $Z_s = (\sigma d)^{-1}$ [69, 62]. We have now connected the concept of kinetic inductance with materials and physical properties. Unfortunately, these are somewhat hard to measure and make this expression less useful from a design perspective.

[1]Note that here the subscript s stands for *sheet* or *surface*. Quantity X_s are function of the geometric *number of squares*. Calligraphic fonts indicate *per unit length* quantity.

Mattis-Bardeen Description

We can resort to the Mattis-Bardeen (MB) theory, describing the microscopic electrodynamics of superconductors, based on applying the Bardeen–Cooper–Schrieffer (BCS) theory framework. In MB, the complex conductivity is given by $\sigma(\omega) = \sigma_1(\omega) - \jmath\sigma_2(\omega)$, with:

$$\frac{\sigma_1(\omega)}{\sigma_0} = \frac{2}{\hbar\omega}\int_{\Delta}^{\infty} dE \frac{E^2 + \Delta^2 + \hbar\omega E}{\sqrt{E^2 - \Delta^2}\sqrt{(E+\hbar\omega)^2 - \Delta^2}}\,[f(E) - f(E+\hbar\omega)], \tag{2.14a}$$

$$\frac{\sigma_2(\omega)}{\sigma_0} = \frac{1}{\hbar\omega}\int_{\Delta}^{\Delta+\hbar\omega} dE \frac{E^2 + \Delta^2 - \hbar\omega E}{\sqrt{E^2 - \Delta^2}\sqrt{\Delta^2 - (E-\hbar\omega)^2}}\,[1 - 2f(E)], \tag{2.14b}$$

where σ_0 is the DC conductivity, Δ the superconducting gap, and $f(E) = \left[\exp\frac{E}{k_B T} + 1\right]^{-1}$ the Fermi-Dirac distribution, applied to quasiparticles. The complex conductivity is a valid concept provided that the electron mean free path is short compared to the depth to which the field penetrates below the surface of the superconductor. When $T \to 0$, $f(E)$ decreases exponentially and σ_1 can be arbitrarily small at sufficiently low temperatures. On the other hand, when $T \ll T_C$ and for $\hbar\omega \ll \Delta_0$ ($\omega \ll 462\,[\text{rad/s}] \cdot T_C/1\,[\text{K}]$) [62, 69]:

$$\frac{\sigma_2(\omega)}{\sigma_0} \approx \frac{\pi\Delta_0}{\hbar\omega}. \tag{2.15}$$

Replacing the complex conductivity in the surface impedance with this final expression from MB, assuming a low temperature, and at frequencies below the gap frequency:

$$Z_s = \frac{1}{\sigma d} = \jmath\omega\frac{\hbar\rho_0}{\pi\Delta_0 d} = \jmath\omega L_{\text{kin,s}}. \tag{2.16}$$

Sheet kinetic inductance

We can finally summarize the expressions for the sheet kinetic inductance:

$$L_{\text{kin,s}} = \frac{m}{n_s e^2 d} = \mu_0\frac{\lambda_L^2}{d} = \frac{\hbar R_s}{\pi\Delta_0}, \tag{2.17}$$

with $R_s = \rho/d$ the sheet resistance of the material. From a design perspective, this is the *most useful* expression. If we expand Δ_0 with the BCS theory ($\Delta_0 = 1.76 k_B T_C$, with k_B the

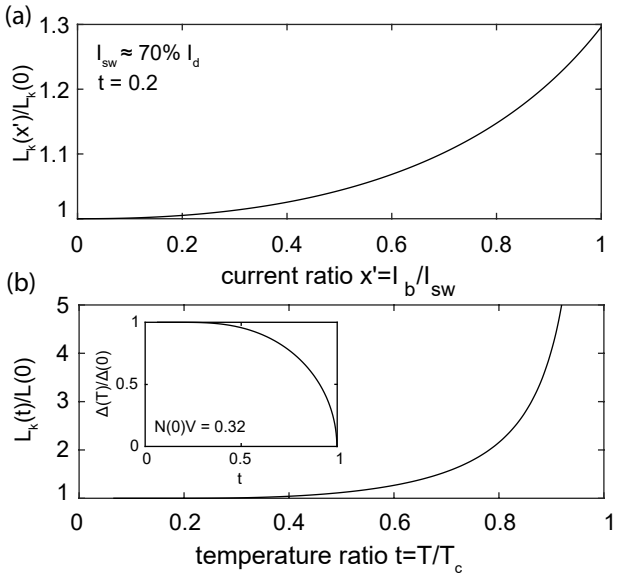

Figure 2-1: Non-linear dependence of the kinetic inductance. (a) Kinetic inductance versus applied bias current, normalized by the switching current of the nanowire $I_{\rm sw}$ (about $0.7I_{\rm d}$). (b) Kinetic inductance versus operational temperature. We solved the gap dependence (inset) using N(0)V for bulk niobium nitride.

Boltzmann constant), we obtain:

$$L_{\rm kin,s} = 1.38\,\frac{R_{\rm s}}{T_{\rm C}} \quad [{\rm pH}/\square]. \tag{2.18}$$

Equation 2.18 is extremely useful in practical applications as it connects the inductance to measurable parameters of the superconducting film. If we assume a thin-film slab of material with length L and width w, the number of squares is $\square = L/W$, and the total kinetic inductance is $L_{\rm kin} = 1.38\,\frac{R_{\rm s}}{T_{\rm C}}\frac{L}{W}$.

Non-linearities and tunability

To conclude the section on kinetic inductance, we would like to briefly mention its non-linear properties with operational parameters, namely current and temperature. We will use the notation by Clem and Kogan [70]. In the fast-relaxation/slow-experiment regime[2], the kinetic inductance has the following dependence as a function of the density of bias

[2]Fast relaxation regime: this is the most common regime of nanowire operation in our experiments. Note that the time scale of our experiments is on the order of 100 ps - 1 ns. In comparison, the order parameter relaxation is ≈ 1 ps.

current applied to the superconductor j_s:

$$\frac{\mathcal{L}_{\rm kin}(0,t)}{\mathcal{L}_{\rm kin}(x,t)} = (1-x^n)^{1/n}, \tag{2.19}$$

where $t = T/T_C$, $x = j_s/j_d(T)$, and $j_d(T)$ is the temperature dependent depairing current. The couples (t,n) are available in Ref. [70]. In Fig.2-1(a), we show the kinetic inductance as a function of the bias current, for $(t,n) = (0.2, 2.27)$[3]. Note that, here, we are plotting the curve as a function of x', normalizing the bias current with the switching current $I_{\rm sw}$. In our devices, due to defects in the nanowire or vortex dynamics, the maximum operational current, i.e., $I_{\rm sw}$, is limited to a fraction of the true departing current, I_d. This fraction depends on the width of the wire, the operation temperature, and the thickness of the film. For the devices shown here, we assume $I_{\rm sw} \approx 70\%\, I_d$ and $x' \approx x/0.7$ [71, 72]. This constraint limits the non-linear inductance increase to about 20% to 30% compared to the unbiased case.

In the presence of zero bias, we can express the dependence of the kinetic inductance with temperature [73]:

$$\frac{\mathcal{L}_{\rm kin}(0,t)}{\mathcal{L}_{\rm kin}(0,0)} = \left(\frac{\Delta(T)}{\Delta(0)}\tanh\frac{\Delta(T)}{2k_BT}\right)^{-1}. \tag{2.20}$$

This expression requires the calculation of the superconducting gap temperature dependence. This is provided by BCS theory:

$$\frac{1}{N(0)V} = \int_0^{\hbar\omega_c} d\xi \frac{\tanh\left[\frac{1}{2k_BT_C}(\xi^2+\Delta^2)^{1/2}\right]}{(\xi^2+\Delta^2)^{1/2}}, \tag{2.21}$$

where we used the notation of the BCS pairing Hamiltonian [73]. Here ξ is the energy, $N(0)$ is the density of states at the Fermi surface, V is the BCS interaction potential and ω_c is the Debye frequency. The integral can be solved self-consistently. We performed this calculation for $N(0)V = 0.32$, valid for bulk niobium nitride [74, 75]. Thin-film niobium nitride will experience slight variations. The temperature dependence of the gap is shown in the inset of Fig. 2-1(b). In Fig. 2-1(b), we show the kinetic inductance as a function of the temperature fraction $t = T/T_C$. Note that the tunability/non-linearity of the kinetic inductance is particularly pronounced as a function of temperature, with values up to five times higher

[3]This specific value of t is selected as representative of our experimental conditions. Our thin films are generally deposited to a thickness determining a critical temperature of about 6 K to 7 K, and are tested at 1.5 K, giving $t \approx 0.2$

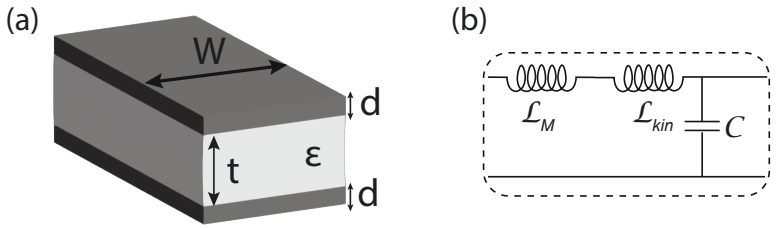

Figure 2-2: Parallel plate thin-film superconducting transmission line: (a) stack and (b) model

close to the critical temperature, compared to 0 K. If we could bias our nanowire close to the true depairing current, we would also expect a similarly large increase as a function of injected current.

2.2 Superconducting nanowire transmission lines

We now introduce the concept of superconducting transmission lines. We start from the simplest case of a dielectric slab (with thickness t and permittivity ϵ) sandwiched between two superconducting thin films (with thickness d). This is a parallel-plate transmission line, and it is shown in Fig. 2-2(a). We now proceed to the analysis of this structure. We can write the capacitance per unit length and the magnetic inductance per unit length for this parallel plate geometry:

$$\mathcal{C} = \epsilon \frac{w}{t}, \tag{2.22a}$$

$$\mathcal{L}_{\mathrm{M}} = \mu_0 \frac{t}{w}. \tag{2.22b}$$

The contribution of the kinetic inductance per unit length, in the presence of two thin films of thickness d, assuming homogeneous current distribution and with $d \ll \lambda_{\mathrm{L}}$ (Eq. 2.17) is:

$$\mathcal{L}_{\mathrm{kin}} = 2\mu_0 \frac{\lambda_{\mathrm{L}}^2}{dw}. \tag{2.23}$$

The model is shown in Fig. 2-2(b). We can now calculate the characteristic impedance and effective refractive index of the transmission line, including the kinetic inductance:

$$Z_0 = \sqrt{\frac{\mathcal{L}_{\mathrm{M}} + \mathcal{L}_{\mathrm{kin}}}{\mathcal{C}}} = \eta_0 \frac{t}{w} \sqrt{1 + \frac{2\lambda_{\mathrm{L}}^2}{dt}}, \tag{2.24a}$$

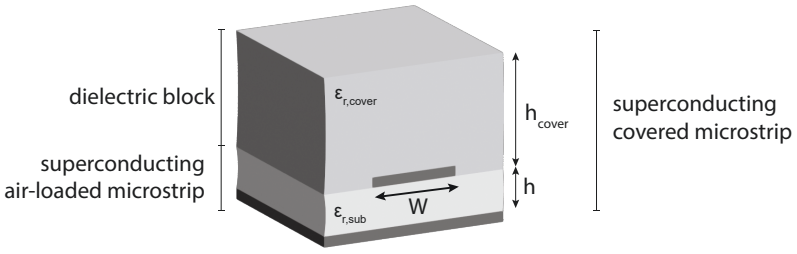

Figure 2-3: Sketch of a superconducting nanowire covered microstrip architecture.

$$n_{\text{eff}} = \frac{c}{v_{\text{ph}}} = \frac{\sqrt{(\mathcal{L}_{\text{kin}} + \mathcal{L}_{\text{M}})\,\mathcal{C}}}{\sqrt{\mu_0 \epsilon_0}} = \sqrt{1 + \frac{2\lambda_{\text{L}}^2}{d}}. \tag{2.24b}$$

Eqs. 2.24a and 2.24b show that, due to the penetration of the field in the superconductor or, equivalently, the presence of the kinetic inductance term, the effective index and impedance are higher than that of a parallel-plate transmission line with standard/normal metallic conductors. The mode supported by the structure is referred to as Swihart wave [76, 77], compared to a simple TEM wave.

This simple example shows that the impedance and effective index can be made larger by integrating superconducting thin films in transmission line architectures, leading to low phase velocity and high compression of the wavelength. These characteristics have one important direct implication: we can use superconducting transmission lines to fabricate ultra-compact devices operating at microwave frequency.

In the following sections, we will analyze two superconducting transmission line architectures we used extensively in this thesis. This analytical treatment was used for preliminary device design sizing before full simulation. Treatment of simpler structures can be found in Ref. [43].

2.2.1 Superconducting nanowire covered microstrip

In this section, we introduce the superconducting nanowire covered microstrip. The structure, shown in Fig. 2-3, consists of a traditional superconducting air-loaded microstrip modified with the addition of a dielectric cover block. In particular, the superconducting line has a width w and it is referenced to ground through a dielectric of thickness h and permittivity $\epsilon_{\text{r,sub}}$. The dielectric block has a thickness h_{cover} and permittivity $\epsilon_{\text{r,cover}}$. The analytical treatment starts with the air-loaded microstrip.

Airloaded Microstrip

We use some known microstrip design formulas [78], first introduced by Wheeler [79], Schneider [80], and Hammerstad [81] to calculate the characteristic impedance of an airloaded microstrip with a substrate relative dielectric constant $\epsilon_{\mathrm{r,sub}}$. In our case, we assume $w/h < 2$ (generally valid for nanowires)[4], and the equation reads as:

$$Z_{0,\mathrm{airloaded}} = \frac{377[\Omega]}{2\pi[(\epsilon_{\mathrm{r,sub}}+1)/2]^{1/2}}\left[\log\left(\frac{8h}{w}\right)+\frac{1}{8}\left(\frac{w}{2h}\right)^2-\frac{1}{2}\frac{\epsilon_{\mathrm{r,sub}}-1}{\epsilon_{\mathrm{r,sub}}+1}\left(\log\frac{\pi}{2}+\frac{1}{\epsilon_{\mathrm{r,sub}}}\log\frac{4}{\pi}\right)\right]. \tag{2.25}$$

We use the formula introduced by Hammerstad [81] and Bekkadal [82] to calculate the effective index of the airloaded microstrip. In our case, $w/h < 2$ [4]:

$$\epsilon_{\mathrm{eff,airloaded}} = \frac{\epsilon_{\mathrm{r,sub}}+1}{2}+\frac{\epsilon_{\mathrm{r,sub}}-1}{2}\left[\left(1+\frac{12h}{w}\right)^{-1/2}+0.04\left(1-\frac{w}{h}\right)^2\right]. \tag{2.26}$$

Covered Microstrip

We now introduce a dielectric cover on the airloaded microstrip. This modification requires a different formula for the effective index. We use the formalism by Gouker and Kushner[4] [83]:

$$F(w/h) = \left(1+\frac{12h}{w}\right)^{-1/2}+0.04\left(1-\frac{w}{h}\right)^2, \tag{2.27a}$$

$$A = -\left(\frac{\epsilon_{\mathrm{over}}}{\epsilon_{\mathrm{sub}}}-1\right)\log\frac{w}{h}, \tag{2.27b}$$

$$B = 2-\sqrt{\left|\log\frac{w}{h}\right|}, \tag{2.27c}$$

$$\begin{aligned}\epsilon_{\mathrm{eff,covered}} = {} & \frac{\epsilon_{\mathrm{r,sub}}+\exp\left(-1.4\sqrt{\frac{h_{\mathrm{over}}}{h}}\right)+\left(\frac{\epsilon_{\mathrm{r,sub}}}{\epsilon_{\mathrm{r,over}}}\right)^{0.1}\epsilon_{\mathrm{r,over}}\left[1-\exp\left(-1.4\sqrt{\frac{h_{\mathrm{over}}}{h}}\right)\right]}{2} \\ & + \frac{\epsilon_{\mathrm{r,sub}}-\exp\left(-1.4\sqrt{\frac{h_{\mathrm{over}}}{h}}\right)-\left(\frac{\epsilon_{\mathrm{r,sub}}}{\epsilon_{\mathrm{r,over}}}\right)^{0.1}\epsilon_{\mathrm{r,over}}\left[1-\exp\left(-1.4\sqrt{\frac{h_{\mathrm{over}}}{h}}\right)\right]}{2}F(w/h) \\ & + A\exp\left(-B\frac{h_{\mathrm{over}}}{h}\right)\left[1-\exp\left(-B\frac{h_{\mathrm{over}}}{h}\right)\right].\end{aligned} \tag{2.28}$$

[4]Here we only consider the analytical model at the nanowire section, for brevity. However, the $w/h > 2$ was considered to construct the plots shown below, and in the analysis of impedance matching tapers

When $h_{\text{over}}/h \to \infty$ (often the case in our devices)[5] the equation converges to:

$$\epsilon_{\text{eff,covered}} = \frac{\epsilon_{\text{r,sub}} + \left(\frac{\epsilon_{\text{r,sub}}}{\epsilon_{\text{r,over}}}\right)^{0.1} \epsilon_{\text{r,over}}}{2} + \frac{\epsilon_{\text{r,sub}} - \left(\frac{\epsilon_{\text{r,sub}}}{\epsilon_{\text{r,over}}}\right)^{0.1} \epsilon_{\text{r,over}}}{2} F(w/h). \tag{2.29}$$

The impedance for the covered microstrip is obtained starting from the airloaded formula:

$$Z_{0,\text{covered}} = Z_{0,\text{airloaded}} \sqrt{\frac{\epsilon_{\text{eff,airloaded}}}{\epsilon_{\text{eff,covered}}}}. \tag{2.30}$$

Introducing the kinetic inductance

When treating the simple parallel plate structure, we assumed that the current was uniformly distributed across the width w of the superconductor. This assumption holds when $w < \lambda_{\text{L}}$. When $w > \lambda_{\text{L}}$ and approaching Λ_{p}, the current distribution is not constant and peaks sharply at the edges of the film, where the magnetic field is perpendicular to the film and large [84]. One can obtain the current distribution in the wire by solving the Helmholtz equation for the magnetic field in the London gauge [43]. An example is given in Figure 2-4 where we show the superconducting current distribution in a wire of thickness $d = 10\,\text{nm}$ with $\lambda_{\text{L}} = 892\,\text{nm}$, for several wire widths. Note that in the presence of a uniform current distribution ($w < \lambda_{\text{L}}$), the kinetic inductance is $L_{\text{kin,s}} = \frac{\mu_0 \lambda_{\text{L}}^2}{d} = 100\,\text{pH}$ per square. When the distribution is non-uniform, the kinetic inductance is calculated by integrating the supercurrent distribution over the width of the wire. In Fig.2-4, we provide the screening *s-factor* [43, 85], which accounts for the difference in the kinetic inductance due to the non-uniform current distributions versus $L_{\text{kin,s}}$. We note that $s = 1.02$ for $w = 100\,\mu\text{m}$, which we will neglect in the following calculations for simplicity.

To introduce the kinetic inductance in the formula, we consider a simple trick. By manipulating the known formula listed above, we can extract the magnetic inductance and capacitance as:

$$\mathcal{L}_{\text{M}} = \frac{Z_{0,\text{covered}} \sqrt{\epsilon_{\text{eff,covered}}}}{c}, \tag{2.31a}$$

$$C_0 = \frac{\sqrt{\epsilon_{\text{eff,covered}}}}{c Z_{0,\text{covered}}}. \tag{2.31b}$$

[5]Here, we are assuming that the microstrip cover is the handle wafer. From a fabrication perspective, it is convenient to fabricate the microstrip *upside-down*: we deposit the conductor on the cover. For this reason, the thickness of the cover is generally larger than all the other thicknesses involved in the architecture.

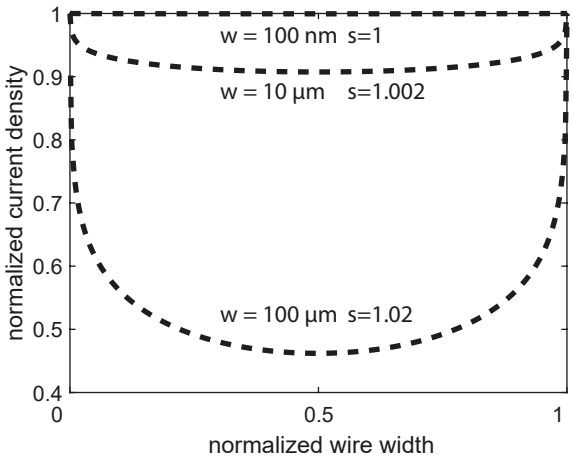

Figure 2-4: Current density distribution in a superconducting nanowire of $d = 10\,\mathrm{nm}$ with $\lambda_\mathrm{L} = 892\,\mathrm{nm}$, for several widths. The current density is approximately uniform when the width is much smaller than $\Lambda_\mathrm{P} = 2\Lambda_\mathrm{L}^2/d$. Conversely, when $w \approx \Lambda_\mathrm{P}$, the current density sharply peaks at the edge of the wire. We provide the s-factors describing the ratio between the kinetic inductance calculated integrating the non-uniform current density vs. the one assuming a constant distribution, i.e., $L_{\mathrm{kin,s}}$.

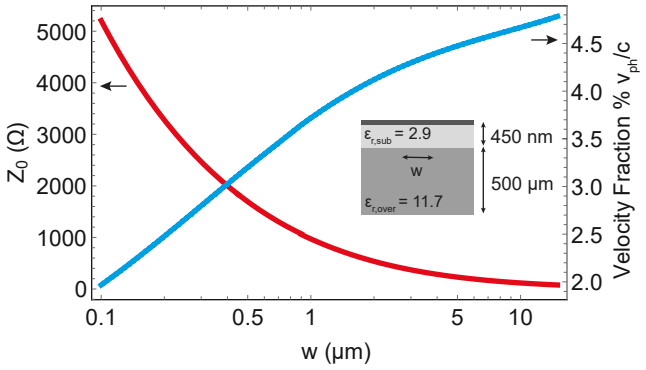

Figure 2-5: Characteristic impedance and velocity fraction for a superconducting nanowire covered microstrip. The inset shows the sketch of the stack.

We then recombine the formula by adding the kinetic inductance term:

$$Z_{0,\text{covered,kin}} = \sqrt{\frac{\mathcal{L}_\text{M} + \mathcal{L}_\text{kin}}{\mathcal{C}_0}}, \tag{2.32a}$$

$$n_{\text{eff,covered,kin}} = c\sqrt{(\mathcal{L}_\text{M} + \mathcal{L}_\text{kin})\mathcal{C}_0}. \tag{2.32b}$$

In Fig. 2-5, we show an example of covered microstrip which we will extensively use in the next sections: an NbN nanowire with a $L_{\text{kin,s}} = 80\,\text{pH}$ per square, deposited on a silicon substrate ($\epsilon_{\text{r,cover}} = 11.7$), and referenced to a top ground through a soft oxide layer ($\epsilon_{\text{r,sub}} = 2.9$). We can see that with a conductor width of $w = 100\,\text{nm}$, the characteristic impedance is about $5\,\text{k}\Omega$, and the velocity fraction ($100\%/n_\text{eff}$) is about 2%, corresponding to a wavelength compression factor of about 50. As we mentioned in the introduction, the high-inductivity behavior of the nanowires results in a high-impedance slow-speed microstrip line.

2.2.2 Multilayer superconducting nanowire coplanar waveguides

This section introduces another type of transmission line architecture we routinely use to design our devices: the superconducting nanowire coplanar waveguide (SCPW). SCPWs offer the simplicity of single-layer fabrication and are often preferred to other structures. Here we focus on the case of coplanar waveguides fabricated on multilayer dielectrics. These structures offer additional design knobs (layer thickness and dielectric constants), allowing more flexible line capacitances than an SCPW on a single-layer substrate. In the following, we summarize the analytical treatment for the reader's convenience.

We show our base multilayer coplanar waveguide structure in Fig. 2-6. Here the nanowire has a width S, and it is separated from the ground plane by a gap W. The substrate bottom layer is assumed semi-infinite with a dielectric constant $\epsilon_{\text{r,sub}}$. The substrate top layer, in contact with the conductors, has a thickness h and a dielectric constant $\epsilon_{\text{r,layer}}$. The top layer is a semi-infinite block of air. We assume zero-thickness conductors and magnetic walls along all the dielectric boundaries. To calculate the microwave properties, we split the CPW into several regions and assume the electric field only exists in those regions, one at a time. We can calculate the total capacitance of the SCPW (C_CPW) as the sum of the capacitance of each partial region. This approach is referred to as *partial capacitance method* (PC) [86].

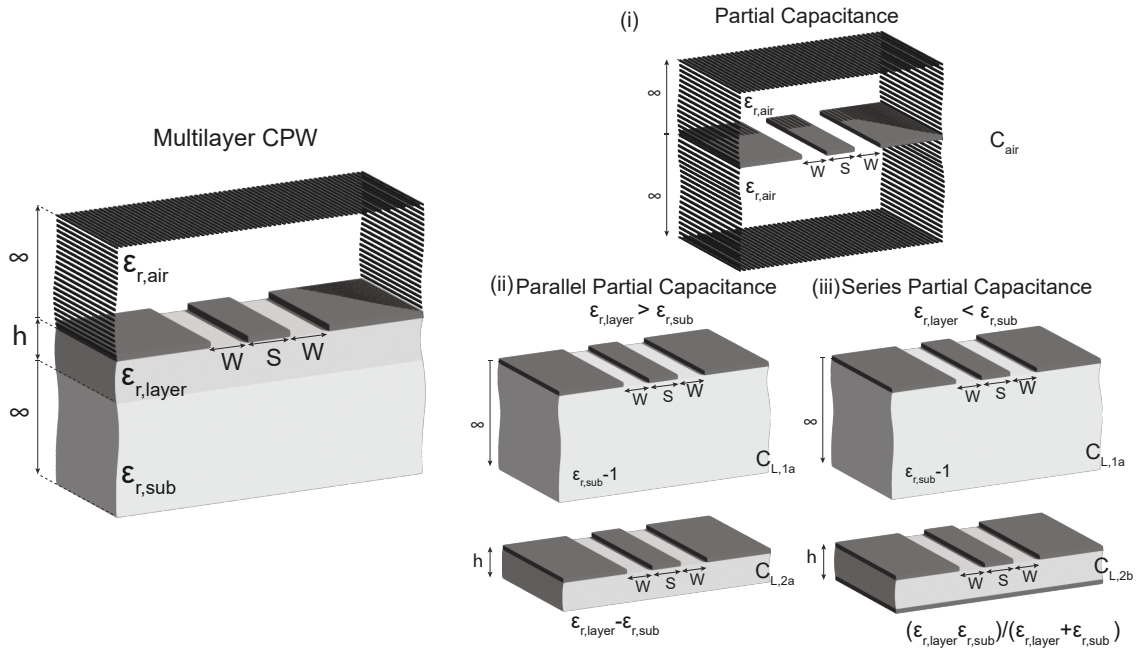

Figure 2-6: Analytical modeling of SCPW. Multilayer SCPW base structure. (i) Partial capacitance method: air-filled SCPW. (ii) Substrate capacitance: parallel method. (iii) Substrate capacitance: serial method.

For our structures:

$$C_{\mathrm{CPW}} = C_{\mathrm{air}} + C_{\mathrm{L}}, \tag{2.33}$$

where C_{air} is the capacitance of the structure with air as dielectric, and C_{L} is the partial capacitance of the bottom dielectrics block. The effective dielectric constant is derived as:

$$\epsilon_{\mathrm{eff}} = \frac{C_{\mathrm{CPW}}}{C_{\mathrm{air}}}. \tag{2.34}$$

Partial capacitance C_{air}

We assume our CPW is surrounded by two semi-infinite air volumes, Fig. 2-6(i). We use the conformal mapping technique (Schwarz-Christoffel transformations [86]) to calculate the analytical form of this partial capacitance:

$$C_{\mathrm{air}} = 4\epsilon_0 \frac{K(k_0)}{K(k_0')}, \tag{2.35}$$

where $K(k)$ is the complete elliptic integral of the first kind, $k_0 = S/(S+2W)$, and $k_0' = \sqrt{1-k_0^2}$

The partial capacitance of the lower substrates (C_{L}) is dependent on the relative value of the dielectric constants. If $\epsilon_{\mathrm{r,layer}} > \epsilon_{\mathrm{r,sub}}$ we will use Parallel Partial Capacitance PPC [86]. Conversely, if $\epsilon_{\mathrm{r,layer}} < \epsilon_{\mathrm{r,sub}}$, we will use Serial Partial Capacitance SPC [87].

Lower partial capacitance: parallel $\epsilon_{\mathrm{r,layer}} > \epsilon_{\mathrm{r,sub}}$

In this case, the capacitance of the lower layer is obtained as a sum of the partial capacitances (parallel capacitors):

$$C_{\mathrm{L}} = C_{\mathrm{L,1a}} + C_{\mathrm{L,2a}}, \tag{2.36}$$

where $C_{\mathrm{L,1a}}$ is the capacitance of a semi-infinite half space with permittivity $\epsilon_{\mathrm{r,sub}}$ topped by a magnetic wall, and $C_{\mathrm{L,2a}}$ is the capacitance of a layer of thickness h and effective permittivity $\epsilon_{\mathrm{r,layer}} - \epsilon_{\mathrm{r,sub}}$ topped by a magnetic wall (Fig. 2-6(ii)). With conformal mapping techniques [86]:

$$C_{\mathrm{L,1a}} = 2\epsilon_0(\epsilon_{\mathrm{r,sub}} - 1)\frac{K(k_0)}{K(k_0')}, \tag{2.37a}$$

$$C_{\mathrm{L,2a}} = 2\epsilon_0(\epsilon_{\mathrm{r,layer}} - \epsilon_{\mathrm{r,sub}})\frac{K(k_2)}{K(k_2')}, \tag{2.37b}$$

with $k_0 = S/(S+2W)$, $k_0' = \sqrt{1-k_0^2}$, $k_2 = \sinh[\pi S/4h]/\sinh[\pi(S+2W)/4h]$, and $k_2' = \sqrt{1-k_2^2}$

Lower partial capacitance: serial $\epsilon_{\mathrm{r,layer}} < \epsilon_{\mathrm{r,sub}}$

In this case, the capacitance of the lower layer is obtained as the parallel of the partial capacitances (series capacitors):

$$C_{\mathrm{L}}^{-1} = C_{\mathrm{L,2a}}^{-1} + C_{\mathrm{L,2b}}^{-1}, \tag{2.38}$$

where $C_{\mathrm{L,2a}}$ is the capacitance of a semi-infinite half space with permittivity $\epsilon_{\mathrm{r,sub}}$ topped by a magnetic wall, and $C_{\mathrm{L,2b}}$ is the capacitance of a layer of thickness h and effective permittivity $\epsilon_{\mathrm{series}} = \epsilon_{\mathrm{r,layer}}\epsilon_{\mathrm{r,sub}}/(\epsilon_{\mathrm{r,sub}} - \epsilon_{\mathrm{r,layer}})$ topped by an electric wall (Fig. 2-6(iii)). With conformal mapping techniques [87]:

$$C_{\mathrm{L,1a}} = 2\epsilon_0(\epsilon_{\mathrm{r,sub}} - 1)\frac{K(k_0)}{K(k_0')}, \tag{2.39a}$$

$$C_{\mathrm{L,2b}} = 2\epsilon_{\mathrm{series}}\epsilon_0 \frac{K(k_1)}{K(k_1')}, \tag{2.39b}$$

with $k_0 = S/(S+2W)$, $k_0' = \sqrt{1-k_0^2}$, $k_1 = \tanh[\pi S/4h]/\tanh[\pi(S+2W)/4h]$, and $k_1' = \sqrt{1-k_2^2}$

Effective dielectric constant

We now calculate the effective dielectric constants using Eq. 2.34. For PPC ($\epsilon_{\mathrm{r,layer}} > \epsilon_{\mathrm{r,sub}}$) the effective dielectric constant is:

$$\epsilon_{\mathrm{eff,PPC}} = \frac{\epsilon_{\mathrm{r,sub}}+1}{2} + \frac{\epsilon_{\mathrm{r,layer}}-\epsilon_{\mathrm{r,sub}}}{2}\frac{K(k_2)}{K(k_2')}\frac{K(k_0')}{K(k_0)}. \tag{2.40}$$

For SPC ($\epsilon_{\mathrm{r,layer}} < \epsilon_{\mathrm{r,sub}}$) we have:

$$\epsilon_{\mathrm{eff,SPC}} = \frac{\epsilon_{\mathrm{r,sub}}+1}{2} + \frac{\epsilon_{\mathrm{series}}}{2}\frac{K(k_1)}{K(k_1')}\frac{K(k_0')}{K(k_0)}. \tag{2.41}$$

Characteristic impedance

Using conformal mapping techniques we calculate the expression for the magnetic inductance of the structure:

$$\mathcal{L}_{\mathrm{M}} = \frac{\mu_0}{4}\frac{K(k_0')}{K(k_0)}. \tag{2.42}$$

The characteristic impedance of a CPW in presence of an effective dielectric constant ϵ_{eff}, with normal conductor is:

$$Z_0 = \sqrt{\frac{\mathcal{L}_{\mathrm{M}}}{C_{\mathrm{CPW}}}} = \sqrt{\frac{\mathcal{L}_{\mathrm{M}}}{C_{\mathrm{air}}\epsilon_{\mathrm{eff}}}} = \frac{30\pi}{\sqrt{\epsilon_{\mathrm{eff}}}}\frac{K(k_0')}{K(k_0)}. \tag{2.43}$$

Introduction of the kinetic inductance

Using the same method shown in the previous section, we include the kinetic inductance of the center superconductor. In this setting, to calculate the kinetic inductivity $\mathcal{L}_{\mathrm{kin}}$, we will use the formalism developed by Clem [88] and already implemented by Zhu et al.[43] and Santavicca et al.[58].

As we mentioned above, our superconducting thin film has a thickness $d \ll \lambda_{\mathrm{L}}$ and the current distribution is governed by the Pearl length $\Lambda_{\mathrm{p}} = 2\lambda_{\mathrm{L}}^2/d$. When the width of the conductor approaches the Pearl length, the current distribution diverges from constant.

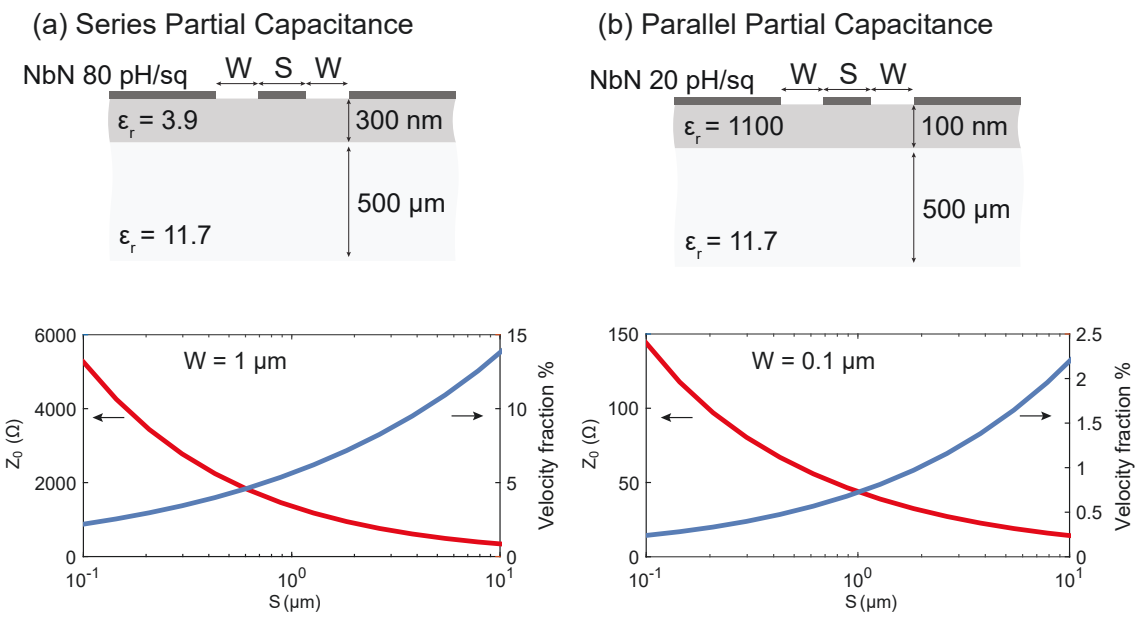

Figure 2-7: Application of the analytical model to two SCPWs of interest. (a) Application of SPC method to NbN CPW on thermal oxide on silicon. (b) Application of PPC method to NbN CPW on thin-film strontium titanate on silicon

Clem [88] introduced a procedure for calculating the kinetic inductivity for all the center conductor widths. In particular:

$$\mathcal{L}_{\text{kin}} = \frac{\mu_0 \Lambda_{\text{p}}}{2S} f(k,p) \tag{2.44}$$

with

$$f(k,p) = \frac{(k+p^2)\,\text{arctanh}\,(p) - (1+kp^2)\,\text{arctanh}\,(kp)}{p(1-k^2)\,[\text{arctanh}\,(p)]^2} \tag{2.45a}$$

$$k = \frac{S}{S+2W} \tag{2.45b}$$

$$p \approx 0.63/\sqrt{2\Lambda_{\text{p}}/S} \quad \text{for} \quad \Lambda_{\text{p}} \gg S/2 \tag{2.45ca}$$

$$p \approx 1 - 1.34\Lambda_{\text{p}}/S \quad \text{for} \quad \Lambda_{\text{p}} \ll S/2 \tag{2.45cb}$$

We calculated the properties of two SCPWs of interest using this analytical formalism. In Fig. 2-7(a), we show the structure and the simulation of an SCPW having NbN with $L_{\text{kin,s}} = 80\,\text{pH}$ per square, patterned on a 300 nm-thick thermal oxide ($\epsilon_{\text{r}} = 3.9$) on a silicon substrate ($\epsilon_{\text{r}} = 11.7$). The gap was fixed to 1 μm. This SCPW structure requires the SPC

method. We note that when the conductor has a width of 100 nm, the impedance is about 5 kΩ, and the phase velocity is about 2% of the speed of light in vacuum. This shows that the superconducting nanowire coplanar waveguide structures achieve high-impedance and slow-speed operation. We will not make explicit use of this structure in this thesis. However, this architecture is the simplest to fabricate and at the base of several seminal devices and demonstrations [54, 43, 89]. In Fig. 2-7(b), we show the structure and the simulation of an SCPW having NbN with $L_{\mathrm{kin,s}} = 20\,\mathrm{pH}$ per square, patterned on a 100 nm-thick strontium titanate layer ($\epsilon_{\mathrm{r}} = 1100$) on silicon substrate ($\epsilon_{\mathrm{r}} = 11.7$). The gap is fixed to 100 nm. This SCPW requires the PPC method. In this case, we can observe that the presence of the high dielectric constant substrate, together with the narrow gap, balances the superconductor's kinetic inductance, leading to a lower impedance while preserving a high compression of the microwave wavelength. At 1 μm, the structure has 50 Ω impedance while the speed of light is kept below 1% c. This architecture is particularly useful for interfacing nanowire devices with normal electronics without the need for impedance matching. We will show a direct application of these concepts in Chapter III.

2.2.3 Design space

In modern design processes, simulation tools often replace the models for the superconducting nanowires transmission lines introduced above (e.g., Sonnet). However, analytic formalism is still particularly useful in guiding the preliminary selection of parameters (e.g., thickness, widths), with the possibility of running fast calculations and optimization before fine-tuning through simulations. In Fig. 2-8, we show an example of applying the covered nanowire microstrip model to study its entire design space. We calculated constant impedance and effective index sectors to bound main design parameters such as the kinetic inductance (i.e., the film's thickness) and the line's width.

2.3 Impedance matching tapers

As observed in the previous section, thin-film superconducting transmission lines achieve a very high-characteristic impedance. This property has several advantages in specific contexts (e.g., interfacing with high-impedance environments). However, when we design devices to be interfaced and used with 50 Ω *normal* electronics, this represents a clear downside, with

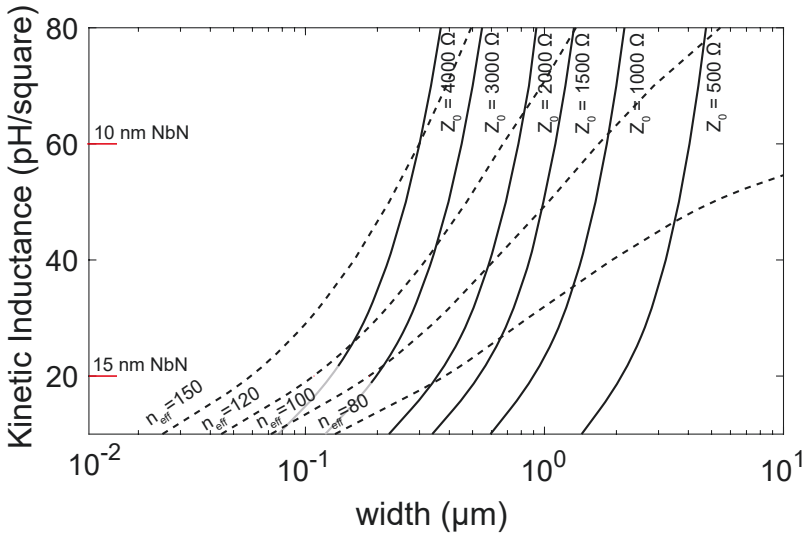

Figure 2-8: Design parameter space for a covered microstrip transmission line, with a silicon oxide ($\epsilon_r = 2.9$) 450 nm-thick dielectric layer and with a 500 μm-thick silicon ($\epsilon_r = 11.7$) cover layer.

high device return loss expected. In this case, we must introduce impedance transformers. Impedance-matching tapers represent an attractive solution from an integration and fabrication perspective. One can tune the impedance by changing the geometry of the transmission line without major discontinuity from the high-impedance side to 50 Ω. This section provides a quick summary of the theory of impedance-matching tapers.

The design of an impedance-matching taper is structured around the solution of the linearized form of the Riccati equation [90]:

$$\frac{d\rho(x)}{dx} - 2\gamma(x)\rho(x) + \frac{1}{2}\frac{d\log Z(x)}{dx} = 0 \tag{2.4}$$

where we assumed $\rho(x)^2 \ll 1$. Here, $\rho(x)$ is the reflection coefficient, $\gamma(x)$ is the imaginary propagation constant, and $Z(x)$ is the characteristic impedance at any point along the line.

Klopfenstein taper

A taper structure that we will extensively use in this thesis is the Klopfenstein taper [91]. The following relations give the characteristic impedance profile for this structure:

$$Z(x) = \sqrt{Z_1 Z_2}\exp\left[\Gamma_m A \int_0^{2x/l-1} dy \frac{I_1(A\sqrt{1-y^2})}{\sqrt{1-y^2}}\right], \tag{2.5a}$$

$$\Gamma_0 = \frac{1}{2}\log Z_2/Z_1, \tag{2.5b}$$

$$\cosh A = \frac{\Gamma_0}{\Gamma_\mathrm{m}}, \tag{2.5c}$$

where l is the length of the taper, $Z_1 = Z(0)$ and $Z_2 = Z(l)$ are the impedances to be matched, I_1 is the Bessel function of the first kind, Γ_m is the maximum reflection ripple in the passband, and Γ_0 is the unmatched reflection coefficient. The direct design parameters are the cutoff frequency $f_\mathrm{co} = c/\lambda_\mathrm{co}$, and the passband ripple A, which determine the electrical length of the taper $l = \lambda_\mathrm{co}A/2\pi$. For additional details on the design, we direct the readers to Refs. [43, 91]. The Klopfenstein taper is generally considered the *optimal* taper: it provides the minimum length, given the desired cutoff frequency and maximum reflection. However, Klopfenstein geometry is not the best solution for applications susceptible to in-band ripple due to the relatively large non-rolling-off reflection ripples [92]. Moreover, the inherent discontinuities at the taper ends, i.e., small geometrical line discontinuities, limit its practical applicability due to the excitation of unwanted spurious modes. We generally neglect these secondary effects in our applications and use the Klopfenstein geometry anyway. However, Hecken tapers provide a simple solution to this issue.

Hecken Taper

Another taper structure we will use in this thesis is the Hecken taper [93]. The following relations give the characteristic impedance profile for this structure:

$$Z(\xi) = \frac{1}{2}\log Z_1 Z_2 + \frac{1}{2}G(B,\xi)\log\frac{Z_2}{Z_1}, \tag{2.6a}$$

$$\xi = \frac{2x}{l}, \tag{2.6b}$$

$$G(B,\xi) = \frac{B}{\sinh B}\int_0^\xi d\xi' I_0(B\sqrt{1-\xi'^2}), \tag{2.6c}$$

where l is the length of the taper, $Z_1 = Z(0)$ and $Z_2 = Z(l)$ are the impedance to be matched, and I_0 is the modified Bessel function of the first kind. One can specify the desired return loss r_max and extract the parameter B with the following relation:

$$\frac{B}{\sinh B} = \frac{\operatorname{arctanh} r_\mathrm{max}}{\log\frac{Z_2}{Z_1}}. \tag{2.7}$$

B will set a relationship between the propagation constant at the lowest band frequency $\beta_{co} = 2\pi/\lambda_{co}$, and the minimum length $\beta_{co}l = \sqrt{B^2 + 6.523}$. Hecken tapers remove the discontinuity in the geometry by trading it off with the βl product [93]; compared to the Klopfenstein design, Hecken tapers are longer for the same bandwidth or a little narrower in-band for the same electrical length.

As for the analytic model of the nanowire transmission lines, these formalisms are extremely useful for calculating and designing impedance-matching structures without (or before) using simulation software. This is particularly important to limit the simulation space. Note that the simulation of tapers can be computationally expensive due to the large size difference involved in the structure.

2.4 Conclusion

In this chapter, we introduced the concept of kinetic inductance following several theoretical approaches. We showed that integrating high inductivity nanowires in transmission line architectures results in high characteristic impedance, slow phase velocity, and high compression of the microwave wavelengths. We provided analytical tools to design such structures and discussed strategies to perform impedance matching. In Chapter III, we engineer these transmission lines to design ultra-compact devices for cryogenic microwave signal processing.

Chapter 3

Superconducting nanowire ultra-compact microwave devices

This chapter presents the applications of the concepts and methods introduced in Chapter II. We use superconducting nanowire transmission line architectures to design devices operating at microwave frequencies. These devices are characterized by extreme compression of the microwave wavelength, hence a highly reduced footprint compared to their standard counterparts.

3.1 Superconducting nanowire directional forward coupler

In Chapter II, we discussed the properties of superconducting nanowire transmission lines with a single conductor. This section introduces a device based on coupled nanowire transmission lines, shown in Fig.3-1(a). This device is designed for balanced forward coupling at microwave frequencies. We refer to it as the *nanowire coupler*. After a summary of the analytical model, we show in detail the design of its architecture, the fabrication process, and the experimental results. Part of the material presented in this chapter has been published and is reproduced from Physical Review Applied 15.2 (2021): 024064 [57]. I want to acknowledge Dr. Di Zhu for developing the initial model of the nanowire coupler, Dr. Brenden Butters for assistance with the experimental design, and Prof Daniel F. Santavicca and Dr. Joshua Bienfang for helpful scientific discussion on the device and experimental design.

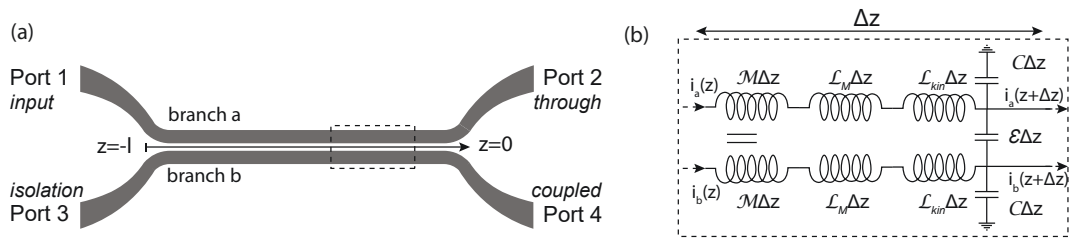

Figure 3-1: Geometry, model, and implementation of a nanowire parallel line coupler. (a) Two nanowire transmission lines are brought together for a coupling length l. (b) Analytical model as a coupled LC ladder, including the kinetic inductance contributions.

3.1.1 Analytical model

The initial analytical model of a nanowire coupler was presented by Dr. Zhu in their doctoral dissertation [43]. Here, after a summary of the analysis, following [43, 57], we include an extension of the theory to model the coupler in the presence of inductance asymmetries and non-linearities [57].

The analytical treatment is based on a coupled-mode formalism [78, 94] adapted to explicitly include the kinetic contribution to the total line inductance. We consider here the schematic shown in Fig. 3-1(a). Our coupler consists of two nanowire transmission lines laid down parallel. We model these as a coupled LC-ladder, Fig. 3-1(b). The inductance per unit length of each line has been separated into two components $\mathcal{L}_{a;b} = \mathcal{L}_{\mathrm{M,a;M,b}} + \mathcal{L}_{\mathrm{kin,a;kin,b}}$, which are the magnetic and kinetic inductance contributions, respectively. $\mathcal{M}$ and $\mathcal{E}$ are the mutual inductance and coupling capacitance between the two lines. $\mathcal{C}_{a;b}$ are the self-capacitances, corrected for the fringing field component [95].

Starting from this model, we can write the coupled telegrapher's equations:

$$-\partial_z \begin{bmatrix} i_a \\ i_b \end{bmatrix} = \begin{bmatrix} \mathcal{C}_a + \mathcal{E} & -\mathcal{E} \\ -\mathcal{E} & \mathcal{C}_b + \mathcal{E} \end{bmatrix} \partial_t \begin{bmatrix} v_a \\ v_b \end{bmatrix}, \tag{3.1a}$$

$$-\partial_z \begin{bmatrix} v_a \\ v_b \end{bmatrix} = \begin{bmatrix} \mathcal{L}_a + \mathcal{M} & -\mathcal{M} \\ -\mathcal{M} & \mathcal{L}_b + \mathcal{M} \end{bmatrix} \partial_t \begin{bmatrix} i_a \\ i_b \end{bmatrix}. \tag{3.1b}$$

Taking the partial derivative with respect to z of Eq. (3.1b) and substituting in Eq. (3.1a)

we have:

$$\partial_z^2 \begin{bmatrix} v_a \\ v_b \end{bmatrix} = \begin{bmatrix} \alpha_a & \gamma_a \\ \gamma_b & \alpha_b \end{bmatrix} \partial_t^2 \begin{bmatrix} v_a \\ v_b \end{bmatrix} \tag{3.2}$$

with

$$\alpha_a = (\mathcal{L}_a + \mathcal{M})(\mathcal{C}_a + \mathcal{E}) + \mathcal{M}\mathcal{E}, \tag{3.3}$$

$$\gamma_a = -\mathcal{E}(\mathcal{L}_a + \mathcal{M}) - \mathcal{M}(\mathcal{C}_b + \mathcal{E}), \tag{3.4}$$

$$\alpha_b = (\mathcal{L}_b + \mathcal{M})(\mathcal{C}_b + \mathcal{E}) + \mathcal{E}\mathcal{M}, \tag{3.5}$$

$$\gamma_b = -\mathcal{M}(\mathcal{C}_a + \mathcal{E}) - \mathcal{E}(\mathcal{L}_b + \mathcal{M}). \tag{3.6}$$

When two transmission lines are brought in close proximity, their coupling produces mode splitting into common (c) and differential (π) modes, having different effective indices and propagation constants. Assuming the voltages in the two lines $v_{a,b}(z,t)$ propagate in the form of $v_{a,b} = V_{a,b}e^{j\omega t - j\beta z}$ for the eigenmodes, we can solve the dispersion relation:

$$\frac{\beta_{c,\pi}^2}{\omega^2} = \frac{(\alpha_a + \alpha_b) \pm \sqrt{(\alpha_a - \alpha_b)^2 + 4\gamma_a\gamma_b}}{2}, \tag{3.7}$$

and for the two eigenmodes, the voltage ratios on the two lines are

$$R_{c,\pi} = \frac{v_b}{v_a} = \frac{\alpha_b - \alpha_a \pm \sqrt{(\alpha_a - \alpha_b)^2 + 4\gamma_a\gamma_b}}{2\gamma_a}. \tag{3.8}$$

The general solution for the voltages on the lines in terms of forward and backward propagating waves for the c and π modes:

$$\begin{aligned} V_a(z) =& A_1 e^{-j\beta_c z} + A_2 e^{j\beta_c z} + \\ & A_3 e^{-j\beta_\pi z} + A_4 e^{j\beta_\pi z}, \end{aligned} \tag{3.9a}$$

$$\begin{aligned} V_b(z) =& A_1 R_c e^{-j\beta_c z} + A_2 R_c e^{j\beta_c z} + \\ & A_3 R_\pi e^{-j\beta_\pi z} + A_4 R_\pi e^{j\beta_\pi z}. \end{aligned} \tag{3.9b}$$

The currents on the line can be obtained by substituting Eq.3.9a and Eq.3.9b in Eq.3.1b:

$$\begin{aligned} I_a(z) =& \frac{A_1}{Z_{c,a}} e^{-j\beta_c z} - \frac{A_2}{Z_{c,a}} e^{j\beta_c z} + \\ & \frac{A_3}{Z_{\pi,a}} e^{-j\beta_\pi z} - \frac{A_4}{Z_{\pi,a}} e^{j\beta_\pi z}, \end{aligned} \tag{3.10a}$$

$$\begin{aligned} I_b(z) =& \frac{R_c A_1}{Z_{c,b}} e^{-j\beta_c z} - \frac{R_c A_2}{Z_{c,b}} e^{j\beta_c z} + \\ & \frac{R_\pi A_3}{Z_{\pi,b}} e^{-j\beta_\pi z} - \frac{R_\pi A_4}{Z_{\pi,b}} e^{j\beta_\pi z}, \end{aligned} \tag{3.10b}$$

where $Z_{c,a;b}$ and $Z_{\pi,a;b}$ denotes the common and differential mode impedances [94]. Differently from [43], the equations for $Z_{c,a;b}$ and $Z_{\pi,a;b}$ below do not assume any particular geometric configuration. Therefore, this formalism is valid for symmetric or asymmetric coupler geometries without loss of generality.

$$Z_{c,a} = \frac{\omega}{\beta_c} \frac{(\mathcal{L}_a + \mathcal{M})(\mathcal{L}_b + \mathcal{M}) - \mathcal{M}^2}{\mathcal{L}_b + \mathcal{M} + \mathcal{M} R_c}, \tag{3.11}$$

$$Z_{c,b} = \frac{R_c \omega}{\beta_c} \frac{(\mathcal{L}_a + \mathcal{M})(\mathcal{L}_b + \mathcal{M}) - \mathcal{M}^2}{(\mathcal{L}_a + \mathcal{M}) R_c + \mathcal{M}}, \tag{3.12}$$

$$Z_{\pi,a} = \frac{\omega}{\beta_\pi} \frac{(\mathcal{L}_a + \mathcal{M})(\mathcal{L}_b + \mathcal{M}) - \mathcal{M}^2}{\mathcal{L}_b + \mathcal{M} + \mathcal{M} R_\pi}, \tag{3.13}$$

$$Z_{\pi,b} = \frac{R_\pi \omega}{\beta_\pi} \frac{(\mathcal{L}_a + \mathcal{M})(\mathcal{L}_b + \mathcal{M}) - \mathcal{M}^2}{(\mathcal{L}_a + \mathcal{M}) R_\pi + \mathcal{M}}. \tag{3.14}$$

Finally, the port voltages can be evaluated by applying the following boundary conditions:

$$[V_{\mathrm{IN}} - V_a(z = -l)]/Z_{\mathrm{L}a} = I_a(z = -l), \tag{3.15}$$

$$-V_b(z = -l)/Z_{\mathrm{L}b} = I_b(z = -l), \tag{3.16}$$

$$V_a(z = 0)/Z_{\mathrm{L}a} = I_a(z = 0), \tag{3.17}$$

$$V_b(z = 0)]/Z_{\mathrm{L}b} = I_a(z = 0), \tag{3.18}$$

where V_{IN} is the input voltage at port 1 and $Z_{\mathrm{L}b}$ and $Z_{\mathrm{L}a}$ are the load impedances. We now consider a symmetric coupler, $\mathcal{L}_a = \mathcal{L}_b = \mathcal{L}$ and $\mathcal{C}_a = \mathcal{C}_b = \mathcal{C}$. We assume $\mathcal{M}/\mathcal{L} \ll 1$. In

this conditions, the propagation constants reduce to

$$\beta_c = \omega\sqrt{\mathcal{LC}} \tag{3.19}$$

$$\begin{aligned}\beta_\pi &= \omega\sqrt{\mathcal{LC}}\sqrt{1+\frac{2\mathcal{E}}{\mathcal{C}}+\frac{2\mathcal{M}}{\mathcal{L}}+\frac{4\mathcal{ME}}{\mathcal{LC}}}, \\ &\approx \omega\sqrt{\mathcal{LC}}\sqrt{1+2\mathcal{E}/\mathcal{C}}\end{aligned}, \tag{3.20}$$

and similarly, the impedances for the c and π modes

$$Z_\mathrm{c} = \sqrt{\frac{\mathcal{L}}{\mathcal{C}}}, \tag{3.21}$$

$$\begin{aligned}Z_\pi &= \sqrt{\frac{\mathcal{L}}{\mathcal{C}}}\frac{\sqrt{1+\frac{2\mathcal{E}}{\mathcal{C}}+\frac{2\mathcal{M}}{\mathcal{L}}+\frac{4\mathcal{ME}}{\mathcal{LC}}}}{1+2\mathcal{E}/\mathcal{C}} \\ &\approx \sqrt{\frac{\mathcal{L}}{\mathcal{C}}}\frac{1}{\sqrt{1+2\mathcal{E}/\mathcal{C}}}.\end{aligned} \tag{3.22}$$

A signal injected through the input port is a superposition of the two modes and the energy propagates through the coupled structures, shuttling between the two lines with a periodicity $l_\pi = \pi/\Delta\beta$. Here

$$\Delta\beta = \beta_\pi - \beta_c \approx \omega\sqrt{\mathcal{LC}}\left(\sqrt{1+\mathcal{E}/\mathcal{C}}-1\right). \tag{3.23}$$

From Eq. 3.23, the minimum length required for balanced forward coupling ($-3\,\mathrm{dB}$) is

$$l_{\pi/2,\mathrm{sc}} = \frac{\pi}{2}\frac{1}{\Delta\beta} \approx \frac{\lambda_c}{4}\frac{1}{\sqrt{1+\mathcal{E}/\mathcal{C}}-1}, \tag{3.24}$$

where λ_c is the guided wavelength for the common mode. Note that in the high-inductance regime, the coupling is mainly determined by the kinetic inductance and the capacitance terms.

The formalism presented above for symmetric couplers also allows the modeling of asymmetric couplers and situations of static non-linear effects. For example, to model temperature non-linearities, one could use the temperature dependence of the kinetic inductance presented in Section 2.1, and replace it in Eq. 3.1a and 3.1b.

3.1.2 Design and simulation

This section provides an overview of the microwave design and simulation of the microwave coupler.

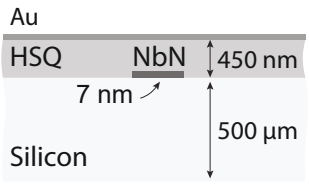

Figure 3-2: Architecture, material stack, and sizing of the transmission line.

Stack and materials

Fig. 3-2 shows the base microwave architecture and material stack selected for this device: a superconducting nanowire covered microstrip (Sec. 2.2.1). In this context, microstrips can produce more compact devices with respect to CPW, at the expense of a more complex/multilayer fabrication.

The materials of our base stack were chosen to facilitate the fabrication process while still trying to produce ultra-compact devices. As for the line inductance, we targeted $L_{\mathrm{kin,s}} = 80\,\mathrm{pH}$ per square. This value corresponds to about 7 nm-thick NbN, using our room-temperature reactive sputtering deposition process [96]. In our fabrication process, the superconducting film must be deposited on a substrate with minimal preliminary processing, ideally on a pristine silicon wafer, to minimize contamination (Appendix A). This constraint imposes a silicon substrate as the microstrip's cover layer. As for the substrate dielectric layer, we chose hydrogen silsesquioxane spun to 450 nm and patterned using a low-contrast electron beam lithography process (Appendix A). By using a spin-on dielectric, we ensure homogeneity of the layer, we can tune its thickness by adjusting the spin speed, and we avoid exposing the superconducting thin film to the chemistry and high temperatures required with other deposition processes (e.g., plasma-enhanced chemical vapor deposition (PECVD), atomic layer deposition (ALD)). The other conducting layers were fabricated with evaporated gold.

Transmission line microwave simulation

In Fig. 3-3, we show the simulation of the characteristic impedance, velocity fraction, and effective index for several combinations of conductor widths and sheet kinetic inductances. The simulations were run using Sonnet EM solver. The top ground was simulated as a perfect electric conductor (PEC). We also included an additional bottom ground layer, also

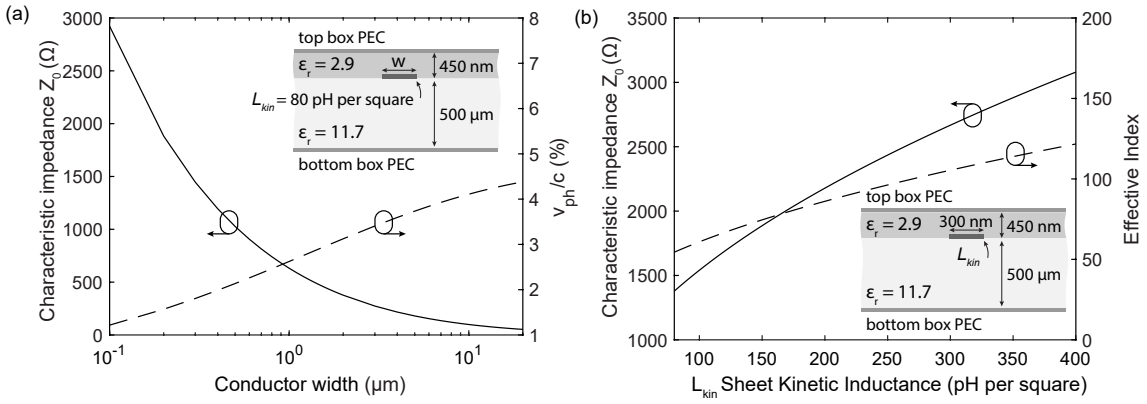

Figure 3-3: Microwave simulations of the base transmission line architecture. (a) Characteristic impedance and velocity fraction for a line with a $L_{\mathrm{kin,s}} = 80\,\mathrm{pH}$ per square, as a function of its width. (b) Characteristic impedance and effective index for a 300 nm-wide line as a function of its sheet kinetic inductance.

simulated as PEC, representing the contact to the testing enclosure. The relative dielectric constants of the materials were set to standard literature values [97, 98] ($\epsilon_{r,\mathrm{Si}} = 11.7$ and $\epsilon_{r,\mathrm{HSQ}} = 2.9$). In Fig. 3-3(a), we study the dependence of the microwave properties as a function of the conductor width. As expected, when the conductor width is in the hundreds of nanometers, the characteristic impedance is in the kΩ, and the phase velocity is limited to fractions of c. These results agree with the analytical model of Section 2.2.1, although the values from the simulation seem to highlight an underestimation of the capacitive components in the model. In particular, here, the characteristic impedance is lower, and the effective index/velocity fraction is higher/lower, indicating an overall higher capacitance.

We did not investigate the source of these inconsistencies. However, one immediate difference stands in the presence of a PEC ground plane on the bottom of the device in the simulation. We neglected this component in the analytical model due to the large differences in dielectric thicknesses. Another option is the limited accuracy of the analytical treatment. Recently, it was noted that the formula by Gouker [83], obtained with a fitting extension, produces non-physical results for some combination of parameters. A new formula based on conformal mapping for covered microstrip, solving these problems, is available at Ref. [99]. Implementation of this method might provide more accurate results. For this project, we decided to follow the indication from the simulation. We want to point out that the analytical model still provides valuable guidance at the initial stage of the design and for interpreting the results.

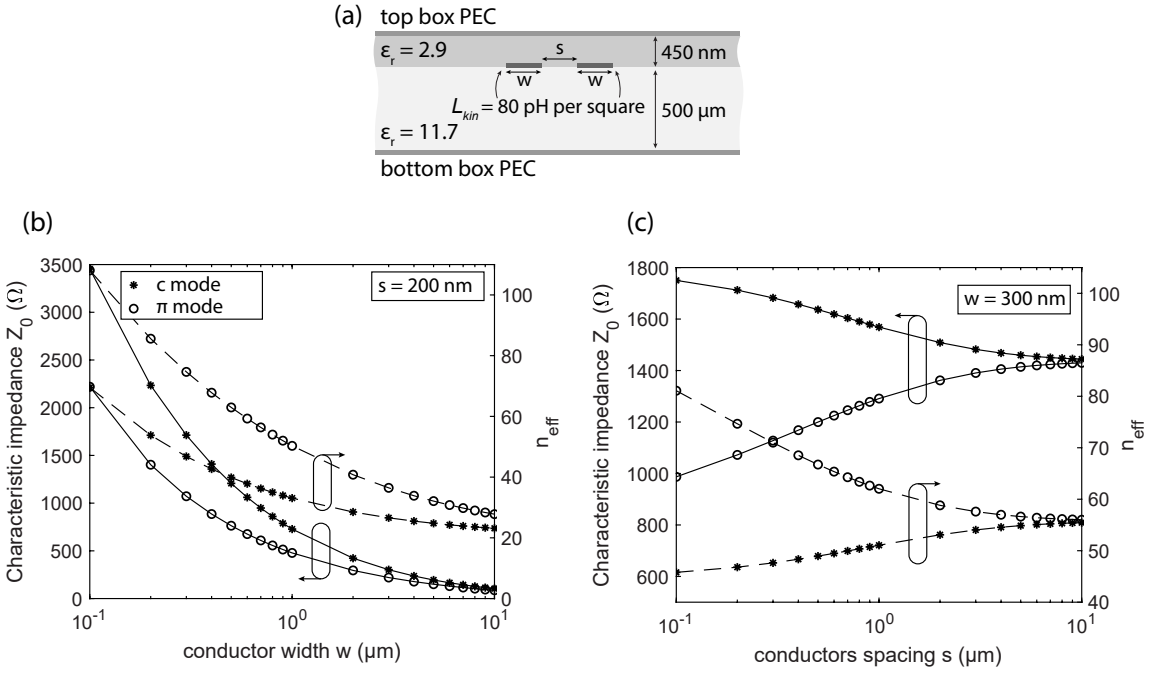

Figure 3-4: Microwave simulation of the coupler cross-section. (a) Material stack. (b) Even and odd modes impedances and indexes for several conductor widths and a fixed gap $s = 200\,\text{nm}$. (c) (b) Even and odd mode impedances and indexes for several gaps and fixed width $w = 300\,\text{nm}$

In Fig. 3-3(b), we study the variation of the microwave parameters as a function of the thin-film inductance. In particular, we study the effect of making the film thinner, i.e., increasing the inductance. Selecting a narrower width and/or a higher sheet inductance would lead to higher impedance and a larger effective index, hence a potentially more compact device. However, as we will show in the next section, an even greater characteristic impedance, compared to the standard $50\,\Omega$, requires a larger and more complex impedance matching taper, in contrast to the overall goal of achieving ultra-compact devices. For this reason, we set the conductor width at 300 nm-wide and targeted 80 pH per square. These physical parameters represent a comfortable target for our fabrication processes. From Fig. 3-3(a) the characteristic impedance is $Z_0 = 1443\,\Omega$, and the effective refractive index is $n_0 = 55.5$ or, equivalently, the velocity fraction is 1.8%.

Parallel coupler analysis and simulation

As shown in Fig. 3-1(a), our microwave coupler consists of two parallel transmission lines running together for a certain coupling length l. In Fig. 3-4, we study the coupler eigenmode

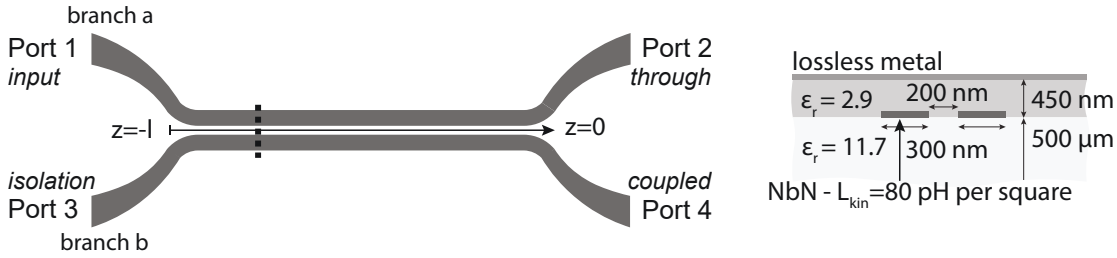

Figure 3-5: Geometry, model, and implementation of a nanowire parallel line coupler: two nanowire transmission lines brought together for a coupling length l. On the right, the coupler cross-section with the selected design values.

Analytical Distributed Parameters

n_0	n_c	n_π	Z_0	Z_c	Z_π
55.5	46.6	74.4	$1443\,\Omega$	$1720\,\Omega$	$1075\,\Omega$

$\mathcal{L}$	$\mathcal{M}$	$\mathcal{C}_0$	$\mathcal{C}_{\text{fringe}}$	$\mathcal{C}$	$\mathcal{E}$
$198.9\,\mu_0$	$-0.1\,\mu_0$	$10.4\,\epsilon_0$	$5.3\,\epsilon_0$	$14.9\,\epsilon_0$	$8.7\,\epsilon_0$

Table 3.1: Distributed parameters corresponding to the device cross-section of Fig. 3-5. The parameters are calculated using results from the analytical model.

impedances and indexes as a function of the conductors width (w) and their gap spacing (s). Fig. 3-4(a) shows the stack used in the simulations. Here we assume a symmetric coupler configuration. Fig. 3-4(b) shows that for a fixed gap spacing $s = 200\,\text{nm}$, a larger conductor width leads to lower modes impedances and, more importantly, lower modes indexes with closer values. This would result in a less compact device, as expected from Eqs. 3.23 and 3.24. In particular, the ratio $\mathcal{E}/\text{C}$ increases leading to a longer $l_{\pi/2,\text{sc}}$. Fig. 3-4(c) shows that fixing the line width to $w = 300\,\text{nm}$, a tight gap spacing s, increasing the coupling capacitance $\mathcal{E}$, would instead decrease the coupling length, leading to a more compact device. This is explained by the increase in the difference of the mode indexes, which in turn decreases the coupling length (Eq. 3.24). However, a large difference in the mode impedances might lead to higher back reflections and lower isolation performance. For these reasons, we set $s = 200\,\text{nm}$ as a trade-off between performance and size. Our final cross-section is shown in Fig. 3-5, accompanied by its analytical distributed parameters, in Table 3.1. These parameters are calculated using finite element modeling of the cross-section. Note that the propagation constant β is related to the effective refractive index n through the following relation: $\beta = n\frac{2\pi}{\lambda}$.

Using the model presented in Section 3.1.1, we calculated the coupling length $l_{\pi/2}$ re-

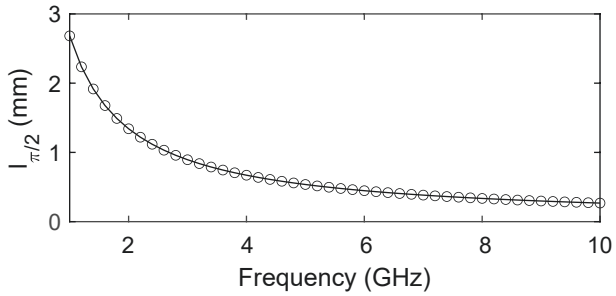

Figure 3-6: Coupling length $l_{\pi/2,\mathrm{sc}}$ required for balanced coupling at several target frequencies

quired for balanced coupling at several target frequencies, shown in Fig. 3-6. A balance coupling at 5 GHz can be obtained with a 520 µm-long coupled-line structure. In Fig. 3-7, we calculate the voltage at the coupler ports for several coupler lengths l, assuming a 5 GHz sinusoidal signal applied at Port 1. As expected, at $l = 520\,\mu\mathrm{m}$, we observe balanced forward coupling behavior, where half of the power is transmitted (Port 2) and half is coupled forward (Port 4). The figure also shows the calculation for an identical coupler fabricated with normal metal traces ($L_{\mathrm{kin,s}} = 0$). It is worth pointing out that forward coupling behavior is observed for the coupler made with normal metal. However for a 5 GHz signal, the required $l_{\pi/2}$ is about 40 mm. For this reason, and considering the strict fabrication requirements for the above-specified design, parallel line couplers are generally not used in standard RF circuitry[1].

This concludes the design of the coupling section. As a summary, our final coupler design consists of two 520 µm-long, 300 nm-wide, and 7 nm-thick NbN lines, separated by a 200 nm gap, deposited on a silicon substrate and referenced to ground through a 450 nm-thick HSQ layer. This device is expected to produce balanced forward coupling at 5 GHz.

Impedance matching taper design and simulation

To test our microwave coupler, we need to interface it with standard electrical characterization equipment. The vast majority of these tools operate at 50 Ω, while the characteristic impedance of our lines is 1443 Ω. To interface the high-impedance nanowire to the 50 Ω rf electronics, we designed a Klopfenstein impedance matching taper following the methods

[1]Note that 40 mm is still a reasonable coupling length for normal metal lines. However, this is possible thanks to the requirement of a 200 nm-wide gap, which would be challenging to fabricate and thus not be used in standard design.

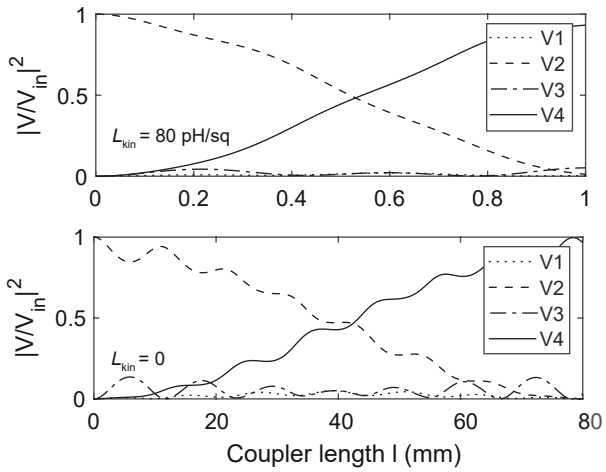

Figure 3-7: Simulation of the port voltages versus coupler length at 5 GHz for balanced forward coupling with (a) $L_{\mathrm{kin,s}} = 80\,\mathrm{pH}$ per square, and (b) $L_{\mathrm{kin,s}} = 0$

of Ref. [91], briefly described in Chapter II. One end of the taper has a width of 300 nm to match the nanowire transmission line at the coupler section ($Z_2 = 1443\,\Omega$). The other end of the taper is designed to provide a $Z_1 = 50\,\Omega$ characteristic impedance to match the room-temperature testing electronics. For our covered superconducting nanowire microstrip, $50\,\Omega$ is obtained with a width of approximately 15 µm. The designed taper has a total length of ≈ 1.97 mm, and is divided in 5214 sections, with ≈ 1178 squares in total and a kinetic inductance of ≈ 94 nH, assuming uniform superconducting current distribution and $L_{\mathrm{kin,s}} = 80\,\mathrm{pH}$ per square. The design return loss is -20 dB, and the cutoff frequency is $f_{\mathrm{co}} = 2.5\,\mathrm{GHz}$. Fig. 3-8(a) shows the layout of the impedance matching taper. The taper is packed in a meandering shape (a turn every 450 µm) for geometrical constraints in the chip design. Fig. 3-8(b) shows the taper's expected transmission and return loss characteristic calculated using the Klopfenstein analytical model and compared to simulation with Sonnet EM. The simulation includes geometric constraints and curvatures, while the analytical model assumes a straight geometry. The characteristics are in good agreement.

Layout design

In Fig.3-9(a), we show the final layout of the microwave coupler, including the impedance matching tapers and the additional gold microwave feedlines required for wire-bonding to the testing enclosure. The layout was programmed in Python using PHIDL CAD tool [100]. On the same fabrication run, we also fabricated calibration devices, consisting of just one

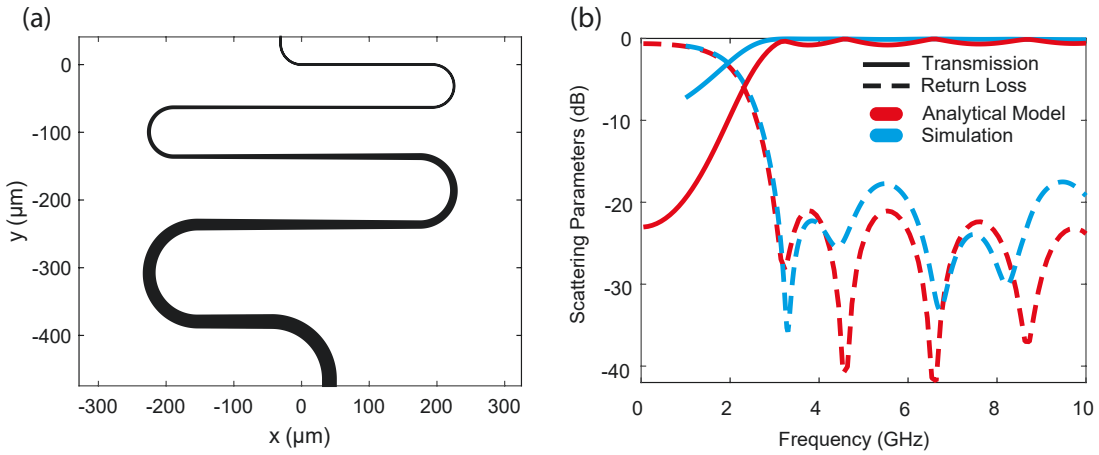

Figure 3-8: Impedance matching taper: (a) Klopfenstein geometry and layout, (b) Analytical and simulated characteristic.

arm of the coupler, i.e., feedline, taper, single wire, taper, feedline designed with the same geometry of the coupler (shown in Fig.3-9(b)).

Full device simulation

In Fig. 3-10, we present the microwave simulation of the full device layout. In particular, Fig. 3-10(a), compares the result from the analytical model of the coupling section with the simulation of the coupling section including impedance-matching taper. The $-3\,\mathrm{dB}$ coupling point is at $4.99\,\mathrm{GHz}$, as expected from the design. The isolation parameter is at $-21.9\,\mathrm{dB}$ (not shown in the plot). This comparison clearly shows that the coupling behavior is not affected by introducing the impedance-matching tapers, having a cutoff frequency at $2.5\,\mathrm{GHz}$, far from the $5\,\mathrm{GHz}$ point. In Fig. 3-10(b), we compare the simulation of the coupling section, including the impedance matching tapers and the coplanar wave feedlines, in the presence or absence of conductor losses. In one case, we assume lossless metals; in the other, we instead take into account the finite conductivity of gold $\sigma_{\mathrm{gold}} = 4.09 \times 10^7\,\mathrm{S/m}$. Using gold layers introduces an overall $\approx 3\,\mathrm{dB}$ loss, shifting the balanced coupling point to $\approx -6\,\mathrm{dB}$.

3.1.3 Device fabrication

Fig. 3-11 shows the fabrication flow of the microwave coupler device. A $\approx 7\,\mathrm{nm}$-thick NbN film was sputter deposited on a $2 \times 2\,\mathrm{cm}^2$ high-resistivity Si substrate (Fig. 3-11(a)).

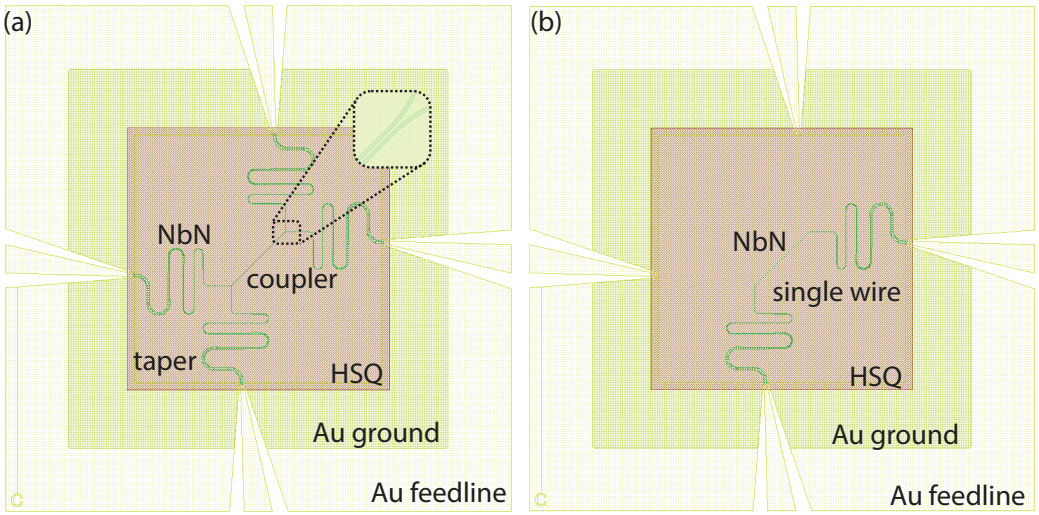

Figure 3-9: Layout designs. (a) Full microwave forward coupler. (b) Single arm calibration device.

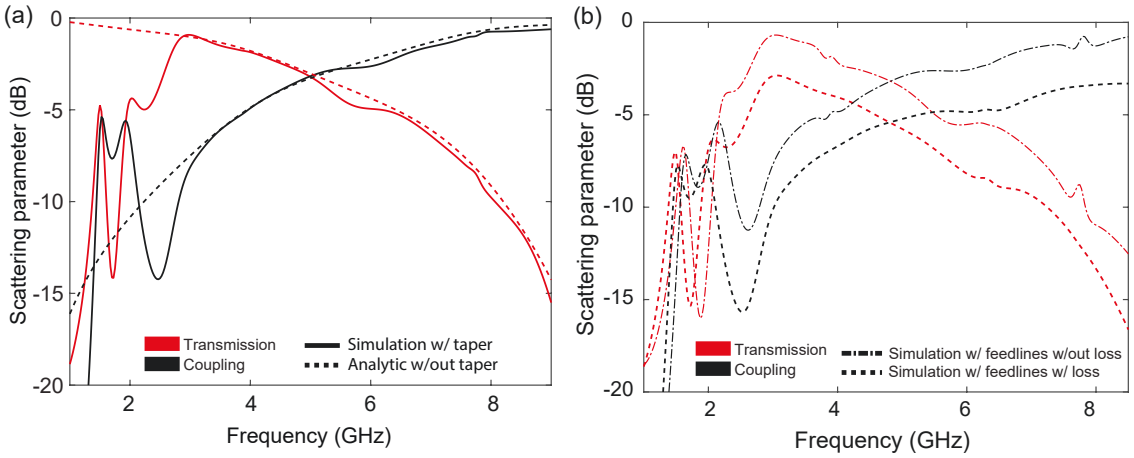

Figure 3-10: Microwave coupler simulation. (a) Results from the analytical model of the coupling section are compared with the simulation of the coupling structure, including the impedance-matching tapers. (b) Simulations of the coupling section, including impedance-matching taper and metallic feedlines, assuming lossless materials or including metals nominal losses.

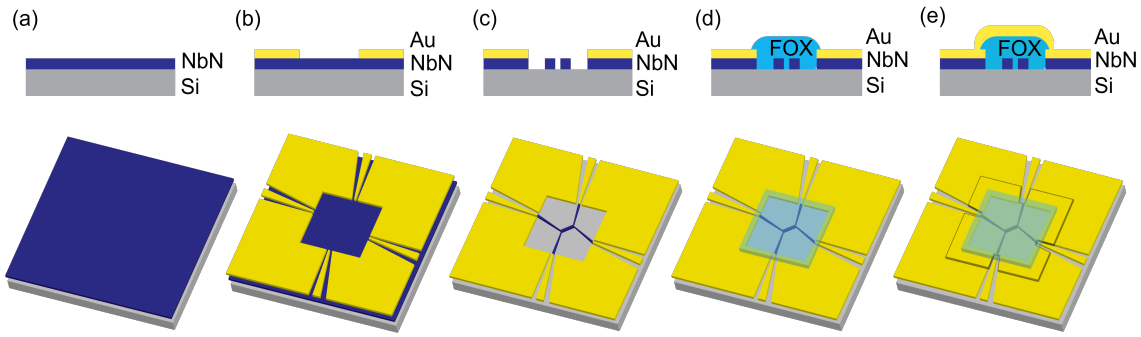

Figure 3-11: Fabrication flow of the microwave coupler.

following Ref. [96]. The high-resistivity silicon substrate ($\rho > 10000\,\Omega \cdot \mathrm{cm}$) was selected to minimize microwave losses [101]. We fabricated the coplanar waveguide feedlines using direct writing photolithography with a positive-tone resist followed by gold evaporation and liftoff (Fig. 3-11(b)). We patterned the nanowire transmission lines and Klopfenstein tapers by aligned negative-tone electron beam lithography using ma-N 2401, and we transferred the patterns into the NbN through reactive ion etching with CF4 plasma (Fig. 3-11(c)). To complete the microstrip structure we patterned a 450 nm hydrogen silsequioxane dielectric spacer, having $\epsilon_r = 2.9$, using a purposely designed low-contrast electron beam lithography process (Fig. 3-11(d)). Lastly, we fabricated the top ground, with aligned direct writing photolithography, followed by gold evaporation and liftoff (Fig. 3-11(e)). The operational details of these processes are reported in Appendix A. After fabrication, the width of the lines was 320 nm while physical separation was reduced to 180 nm, due to the proximity effect. The superconducting transition of the fabricated device was observed at $T_C = 8\,\mathrm{K}$, reflecting film degradation during fabrication.

An earlier version of the device, designed for coupling at 10 GHz and featuring a shorter impedance-matching taper, with a tighter bandwidth (cutoff at 5 GHz), was fabricated using the HSQ process. The device is shown in Fig. 3-12(a). This coupler was functional and showed intended behavior at the design frequency. However, due to limitations in the measurement setups, we decided to design a new device for lower-frequency operation (i.e., the one described above). Due to a lack of resist supply, the HSQ process was discontinued temporarily in favor of the ma-N process. Fig. 3-12(b) shows a scanning electron micrograph of the fabricated 5 GHz coupler device before the dielectric spacer and top-ground fabrication.

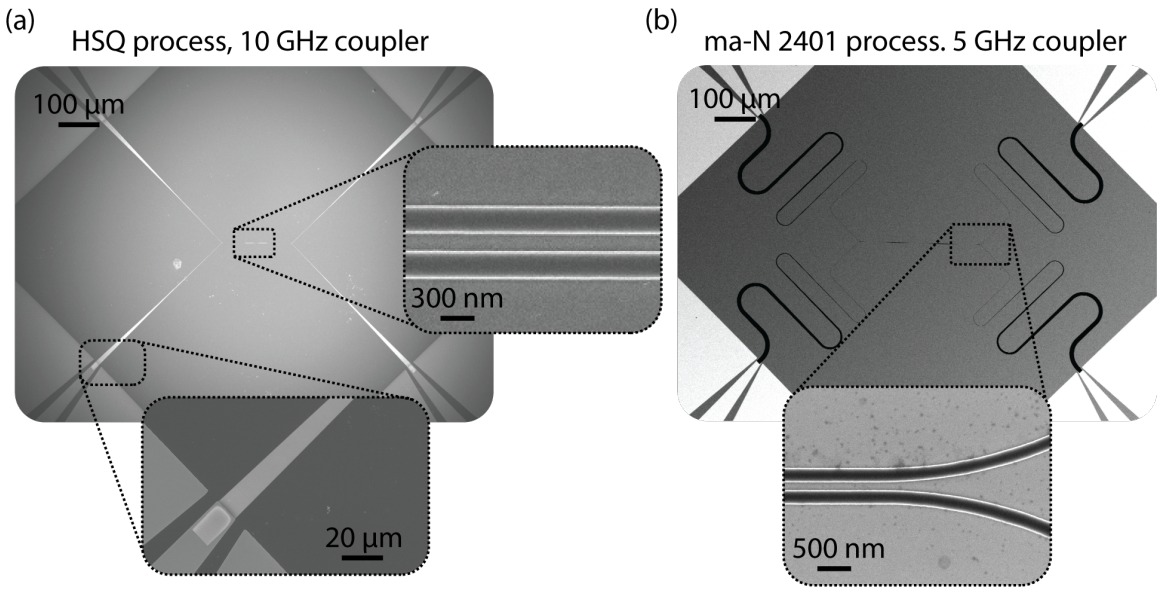

Figure 3-12: Microwave couplers. (a) Scanning electron micrograph of an earlier 10 GHz coupler fabricated with HSQ process. (b) Scanning electron micrograph of a 5 GHz coupler fabricated with the ma-N process. Both devices are shown before the dielectric spacer, and top-ground planes are fabricated.

3.1.4 Measurement setup

Fig. 3-13(a) shows a sketch of the measurement setup assembled to characterize the coupler S parameters and perform cable and connector loss measurements for the purpose of normalization (i.e. loss calibration). The packaged device was cooled down to 1.3 K in a closed-cycle cryostat. The input of the coupler was connected to the Port 1 of the vector network analyzer (VNA). The other three coupler ports (isolation, transmission, and coupling) were connected to an RF switch at room temperature. The common port of the switch was connected to the Port 2 of the VNA through a DC block and a room-temperature low-noise amplifier (LNA). The cables illustrated with the same colors are of the same length and from the same manufacturer. The loss calibration was performed at every cooldown. It consisted of a transmission measurement of the input and output cable assembly, connected with a female-to-female straight SMA connector, anchored to the 1.3 K stage of the cryostat.

Fig. 3-13(b) shows a modification to the measurement setup used to characterize the S-parameter tunability. At the input, the VNA was replaced by a signal generator (SG) and, at the output, by a spectrum analyzer (SA). A constant tuning current was supplied with a current source (CS) to the isolation port of the coupler through a bias tee (BT). The temperature of the 1.3 K stage was controlled by a heater. When measuring the coupling-point

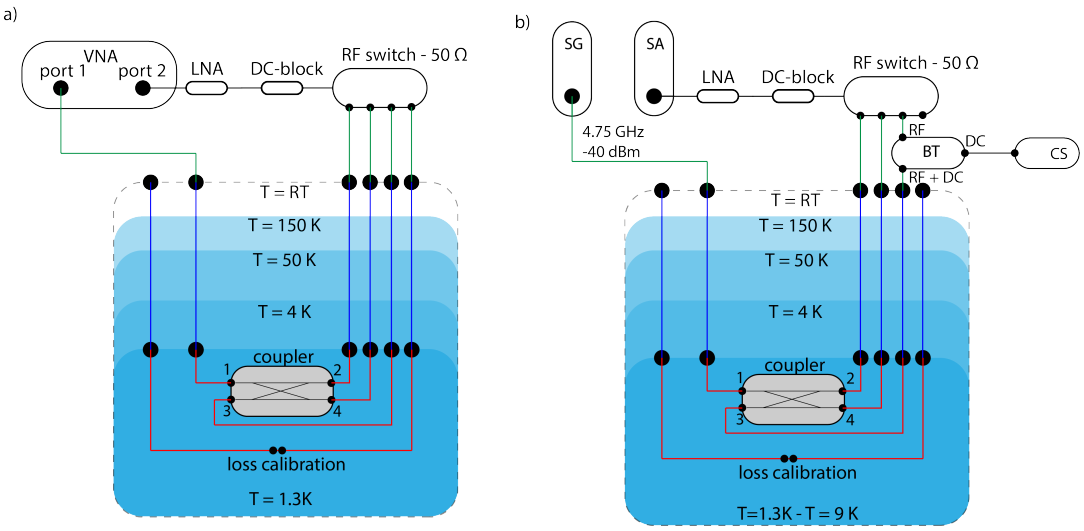

Figure 3-13: Measurement setups. (a) Setup for the characterization of the scattering parameters and cable calibration. (b) Setup for investigating coupler tunability.

Reference	Instrument
Room temperature LNA	RF Bay LNA 8G (1 GHz – 8 GHz)
VNA	N5242A (43 GHz)
RF switch	Mini Circuits MSP4TA-18-12+
Spectrum analyzer	Aglient N9030A
Signal generator	Windfreak SynthHD PRO
Bias tee	Mini Circuits ZFBT-6GW+
Cryostat	ICE Oxford DryIce 1K
Current source	SRS SIM800 + 100 kΩ resistor

Table 3.2: Overview of the instruments for the measurement setups shown in Fig. 3-13.

tunability with temperature, we allowed a 5-minute stabilization time to avoid temperature fluctuation during acquisition. Table 3.2 provides a list of the equipment.

3.1.5 Experimental results

Superconducting properties and DC characterization

We characterized the superconducting and DC electrical properties of the device. Fig. 3-14(a) shows the superconducting transition of the sputtered NbN thin-film. The characterization was performed in liquid He on a blanket film from the same wafer used to fabricate the device. The room-temperature sheet resistance was $R_s = 360\,\Omega$ per square, the residual resistance ratio RRR = 0.8, and the critical temperature $T_C = 8.8\,\mathrm{K}$, taken at 50% of the transition. The sheet kinetic inductance at $T = 0\,\mathrm{K}$ was $L_{\mathrm{kin,s}} = 70.5\,\mathrm{pH}$ per square

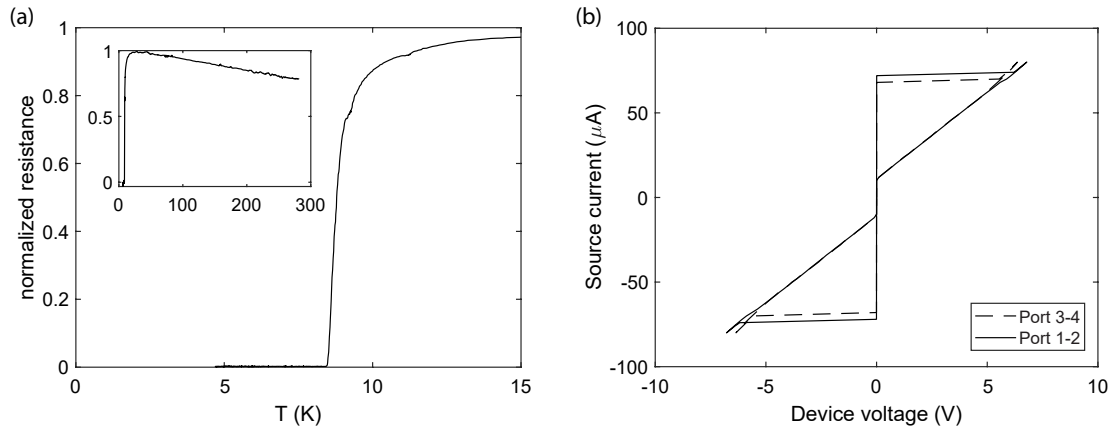

Figure 3-14: DC characteristic and superconducting properties. (a) Characterization of the critical temperature of a bare film from the same wafer used to fabricate the coupler. (b) Characterization of the switching currents of the coupler branches.

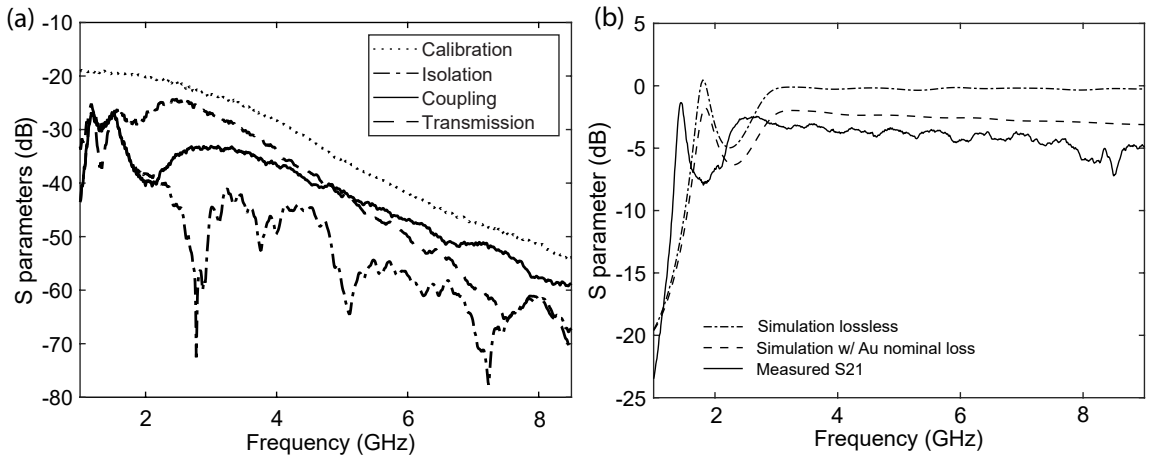

Figure 3-15: Loss calibration. (a) Characterization of loss in the measurement setup. (b) Characterization of additional loss contribution coming from the device.

(Eq. 2.18). After fabrication, we measured the switching current of the coupler arms at $T = 1.3\,\mathrm{K}$. For the input/transmission branch (Port 1-2), we found $I_{\mathrm{sw}} = 72\,\mu\mathrm{A}$. For the isolation/coupling branch (Port 3-4), $I_{\mathrm{sw}} = 68\,\mu\mathrm{A}$. The variation in switching current reflects a slight electrical imbalance that may be due to fabrication asymmetry or local imperfections of the film.

Loss characterization

We characterized the loss of our measurement setup to normalize the response of the coupler. Figure 3-15(a) shows the loss calibration curve and the measured coupler S parameters before

correction. The calibration curve accounts for the losses of room temperature and cold cables, intermediary connectors, RF switch, DC block and includes the amplification of the LNA. Note that the raw S parameters are characterized by the same frequency-dependent attenuation as in the calibration curves. Across the frequency range, the loss ranges from 20 dB to 55 dB. We also characterized the additional intrinsic losses in the coupler due to using normal metals in certain sections, e.g., the ground plane and the coplanar feedlines, for wire bonding. To do so, in Figure 3-15(b), we compare the measured transmission of the calibration device with its simulations, considering lossless conductors or including nominal conductor losses. While the curve shapes and dynamics agree, including nominal losses in the simulation produces a result closer to the measurement results. However, there are still unaccounted loss contributions, which we attribute to a possible underestimation of the conductor losses, connectors, wire bonds, and PCB insertion losses. We can see that at the target coupling frequency 5 GHz we should expect ≈ 3.5 dB additional loss.

Microwave response

In Fig. 3-16, we show the normalized S parameters of the coupler, and we compare it with the simulated response, including nominal conductor losses. The measurement was performed at $T = 1.3$ K with an effective signal power lower than -60 dBm, corresponding to a < 1.2 μA peak signal current [57]. The measurements show balanced forward coupling at 4.75 GHz, at a level of -6.7 dB, and with an isolation of -13.5 dB (not shown in the plot). The experimental data agree with the simulation overall. However, there are a few discrepancies we want to highlight:

- **Coupling frequency** The slight discrepancy in the balanced coupling frequency between measurement (4.75 GHz) and simulation (4.99 GHz) can be attributed to the uncertainties in the device parameters. The simulation does not capture post-fabrication size variations, and electrical asymmetry, which could explain these observations.

- **Coupling level** We attribute the inconsistency in the magnitude of the S parameters to device-level conductor losses contributing to most of the insertion loss of the coupler, as confirmed by the characterization of the calibration device in the previous section.

- **Isolation parameter** The isolation parameter significantly differs from the expected value. This discrepancy (approximately 8.5 dB) might be caused by several factors,

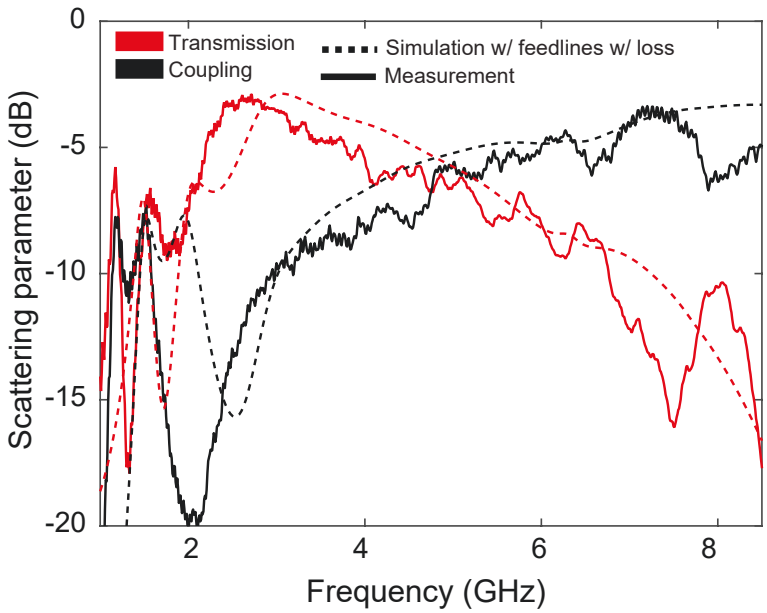

Figure 3-16: Normalized microwave response of the coupler

including impedance-matching taper deviation from the prescribed design, with suboptimal performance and higher backward reflections; full device simulation not including element-to-element transitions (e.g., the abrupt transition from microstrip to CPW in the design). The intrinsic isolation performance of the coupler can be improved by reducing the difference between the characteristic impedance of the modes. We will discuss this in a later section.

Coupler tunability

In Section 2.1, we briefly mentioned the dependence of the kinetic inductance on operating parameters such as the bias current and the temperature. Here we exploit these dependencies to explore the tunability of the coupling point. In Fig. 3-17, we show the tunability of the coupling point as a function of (a) injected bias current in the coupled arm, and (b) temperature. In both cases, we compare the experimental results with the analytical model. The measurements were performed with the setup in Fig. 3-13(b).

First, we consider the coupling tunability with bias current. In this case, we introduce an asymmetry in the device characteristic by injecting a bias current in the coupled arm (and only there). As we will see in a later section, asymmetric devices can achieve a larger

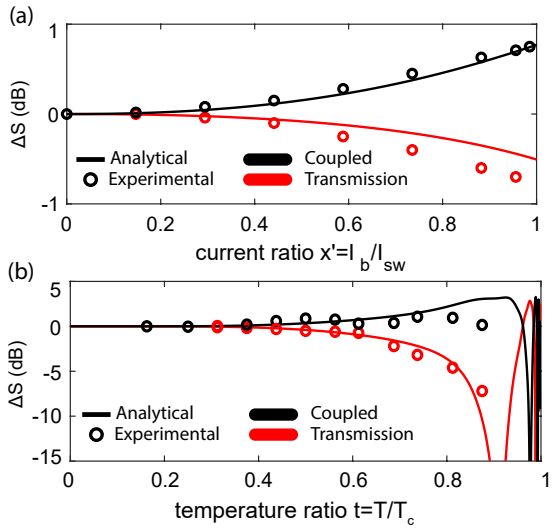

Figure 3-17: Coupling point tunability. (a) Scattering parameter tunability as a function of the injected bias current. (b) Scattering parameter tunability as a function of the device temperature.

bandwidth and, characteristically, have the first crossing/coupling point shifted to lower frequencies. Thanks to this effect, we observe an increase in the coupled power and a decrease in transmitted power, at the original coupling frequency, as a function of injected bias currents. Fig. 3-17(a) shows the coupling tunability at the original coupling point. Close to the switching current ($\approx 70\%$ of the depairing current), and with a $\approx 30\%$ higher kinetic inductance of the coupled arm, we obtain $\approx 1\,\mathrm{dB}$ tunability, in agreement with the analytical model. Note that the analytical curve was obtained from the original model by altering the inductance formula with the dependencies of Sec. 2.1.

We consider the tunability with temperature. By increasing the temperature, we are effectively increasing the inductance of both arms (the device is still symmetric) and increasing the mode impedances and effective indexes. Effectively, we are increasing the wavelength compression and reducing the coupling length. For this reason, as the geometry is fixed, we expect the nominal coupling frequency of the structure to shift to a lower frequency. Hence, we expect a larger coupled power and a smaller transmitted power at the original coupling frequency. Fig. 3-17(b) shows the coupling tunability at the original coupling point while increasing the temperature to 7 K. At $T = 0.9T_\mathrm{c}$, most of the input power is shuttled to the coupled arm.

These results demonstrate that the superconducting nanowire microwave coupler is tun-

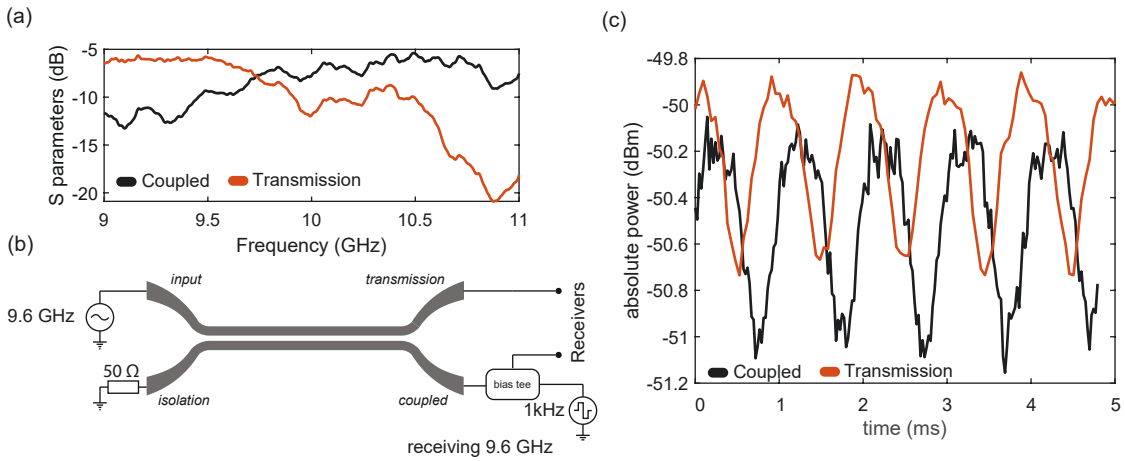

Figure 3-18: Modulation using kinetic inductance non-linearity as a function of injected current. (a) Scattering parameter at the balanced coupling point for a higher frequency coupler design. (b) Measurement setup for modulation. (c) Modulated 9.6 GHz signals at the coupler transmission and coupling port.

able with operating parameters. We exploited these properties to demonstrate the use of this device as a simple modulator. We used our earlier device designed for 10 GHz balanced coupling fabricated with the same process described above. Fig. 3-18(a) shows the S parameters at the coupling point. Due to a suboptimal calibration, the additional losses at the coupling point are higher than those with the 5 GHz coupler. The balanced coupling frequency is at 9.7 GHz. Fig. 3-18(b) shows the measurement configuration used for the modulation experiment. We supplied a 9.6 GHz signal at the input port and monitored the power at the transmission and the coupling port (we use the VNA in receiver mode). Using a bias tee, we also supply a 1.8 V_{pp} 1 kHz sinusoidal modulation signal from the coupling port. Fig. 3-18(c) shows the modulation results. Thanks to the nonlinearity of the kinetic inductance with a current, the 9.6 GHz signal is amplitude-modulated at both ports, even if the modulation signal is supplied to just the coupled port. Due to measurement imperfections and the absence of a calibration sample, these data cannot accurately measure the phase delay (expected to be π) or the real power level. This example serves as a demonstration of the possible applications enabled by the coupler tunability.

3.1.6 Extension of functionality

In this section, we introduce two coupler design tweaks to solve some flaws and shortcomings of the original design.

Bandwidth extension

Single-section symmetric parallel line couplers provide a relatively narrow bandwidth for 3 dB coupling [102]. When the uncoupled propagation constants are the same (symmetric coupler), the power traveling on one line can be fully transferred to the other line. This is clearly shown by the measurement of our device in Fig. 3-16. Effectively, this behavior allows arbitrary coupling ratios but limits the operation bandwidth to a fixed value, i.e., 3 dB coupling is at a single frequency only. A wideband operation can be obtained with asymmetric couplers where the two parallel lines have different widths and, therefore, different uncoupled propagation constants. The maximum power transfer will be limited to a certain fraction in this case. One could design the parameters to transfer precisely half the maximum power, effectively extending the operation bandwidth. To demonstrate this concept, we simulated an impedance-matched asymmetric parallel coupler. To do so, we kept all the parameters constant, but we reduced the width of the coupled line to 100 nm. Effectively, this increases the inductance in the coupled line by two times. Fig.3-19 compares the bandwidth of the original symmetric coupler with the new asymmetric coupler design. The bandwidth is where the coupling oscillates ±10%. The symmetric coupler 10% operation bandwidth is 4.4 GHz to 5.8 GHz. The asymmetric coupler operates between 4 GHz to 8.5 GHz. Note that two different taper designs are required to match the asymmetric coupling section.

Improved isolation

The expected isolation parameter of our symmetric coupler was −21.9 dB, which is worse than the typical −40 dB achieved with bulky cryogenic directional couplers. For parallel lines, backward coupling (determining the isolation parameter) is directly proportional to the difference between the reflection coefficients seen looking into a port of the structure under differential- and common-mode excitation conditions, respectively [102, 43]. This qualitatively implies that if the common- and differential-mode impedances are too different, there will always be a significant part of the signal that will be back-reflected. Equivalently, Z_c and Z_π must be close to minimize backward reflection. Considering the analytical model, we can act on the capacitive terms to reduce the backward reflection. We can reduce the capacitive coupling $\mathcal{E}$ by increasing the coupling gap, operating in a lower coupling regime.

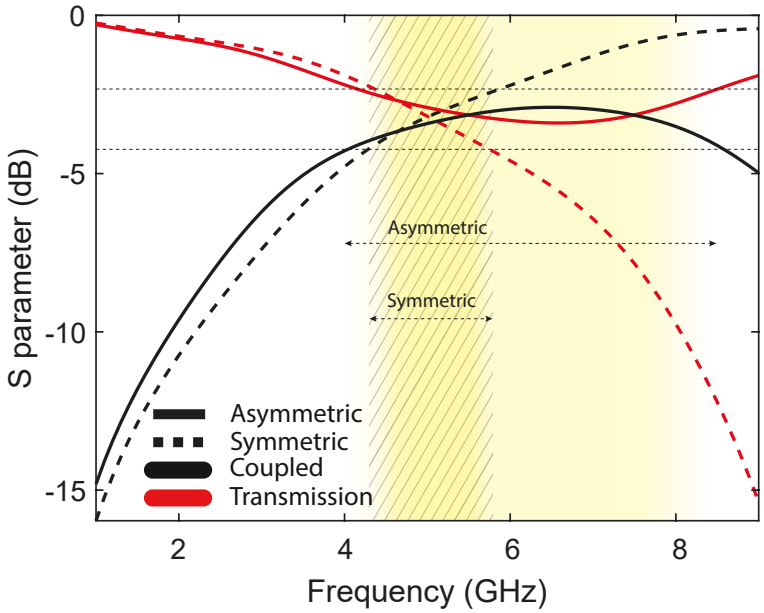

Figure 3-19: Comparison of the coupling bandwidth for the original symmetric coupler and the improved asymmetric coupler.

We can increase the self-capacitance term $\mathcal{C}$ by increasing the width of the line and decreasing the ground spacing. To keep the operation at the original design frequency (5 GHz), we must also increase the coupling length to compensate for the change in the capacitive terms.

We redesigned the 5 GHz coupler to demonstrate improved theoretical isolation, implementing the above corrections. We increased the coupling gap to 400 nm, increased the line width to 1 µm, and reduced the dielectric spacer to 100 nm. This changes extended the $l_{\pi/2}(5\,\text{GHz})$ to 2.9 mm. In Fig. 3-20(a), we show the analytical S parameters for the improved design. The isolation parameter is -35 dB at the balanced coupling frequency. As a comparison, Fig. 3-20(b) shows the analytical S parameters for the original coupler design. Note that to improve the isolation parameters, we have increased the footprint of the coupling section by about six times.

3.1.7 Footprint

As laid out in the design, our original symmetric coupling section (i.e., just the nanowires) had a footprint of about 500 μm^2, with an aspect ratio of 500:1. The aspect ratio can be reduced by meandering the coupling section, making the design overall more compact.

However, introducing large impedance matching tapers to interface the device to 50 Ω

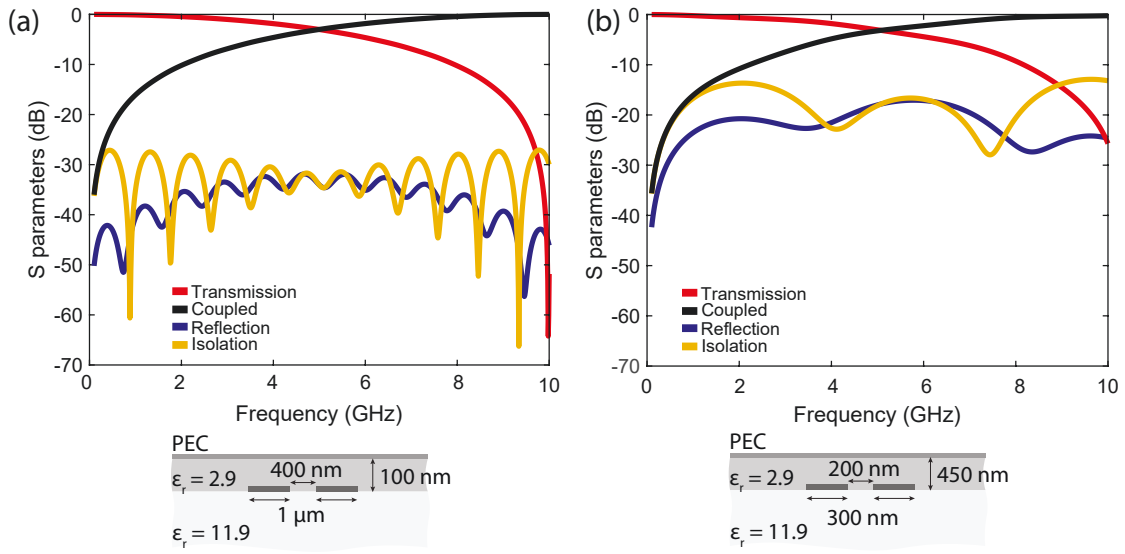

Figure 3-20: (a) Symmetric coupler design with improved isolation. (b) Original coupler design.

electronics increases the footprint to 1.75 mm^2. This seems a particularly critical issue when trying to realize nanowire devices, in contrast with the idea of ultra-compact integrated microwave electronics. However, there are a few points of discussion here:

- in designing a more complex circuit based on nanowires microwave devices, we can expect just a few inputs and outputs; hence, the number of impedance matching elements is not expected to grow linearly with the number of internal microwave devices, and the same applies to the total footprint;

- operating in a compatible high-impedance environment amends the necessity of impedance-matching structures;

- Increasing the target operation frequency decreases the footprint of both the nanowire devices and tapers;

- Resistive impedance matching could reduce the footprint at the expense of high attenuation and a mode matching problem - for example, a matching PI attenuator with an input shunt of 51 Ω, a series resistance of 1495 Ω and an output shunt of 28.4 kΩ will match the device to the external readout, but will induce a 20 dB attenuation [103].

3.1.8 Applications and perspectives

We demonstrated a microwave directional forward coupler by engineering superconducting nanowire transmission line architectures. This device is one of the fundamental components of microwave electronics. It is widely used in most experimental setups, including superconducting quantum computers. This demonstration paves the way to realize other devices using the same platform. Hybrids, interferometers, non-reciprocal devices, traveling-wave parametric amplifiers, bias tee, delay lines, and phase shifters can be implemented using the same technology. Our platform is already cryogenic, has virtually zero-power dissipation, can be operated at higher temperature refrigeration stages (1 K or 4 K), uses CMOS compatible materials (gold can be replaced with thicker superconducting layers, e.g., Nb), employs state-of-the-art fabrication techniques, and it is resilient to the magnetic field. The native high-impedance operation interfaces well with other high-impedance architecture. For example, this device could be used without impedance-matching tapers in combination with qubits shunted with superconductors (e.g., fluxonium) and to create electromagnetically protected environments. These characteristics make our platform particularly attractive for quantum-adjacent applications as scalable integrated cryogenic microwave electronics. Many alternative solutions face several challenges in satisfying the requirements for on-chip integrability. Devices based on semiconductors [104, 105, 15, 106, 107] either dissipate too much power to be operated at a few millikelvin [12] or are made from unconventional materials for which integration with superconductors has not yet been demonstrated. Among the superconducting solutions, 50 Ω transmission-line-based devices [108, 109, 110] require too large a footprint for large-scale integration. Josephson junction (JJ) electronics are a natural candidate for integration with JJ-based quantum processors [111, 112, 113, 114, 115, 116], but they can be challenging to manufacture and require magnetic shielding. Our superconducting nanowire platform does not experience any of these issues and can be directly integrated with the quantum processor at milliKelvin temperatures.

The microwave coupler presented here can be used as a base element to realize a simple ultra-compact Mach-Zehnder interferometer (MZI), with a design similar to the counterpart in integrated photonics [117]. The similarity can also be pushed further with other devices and architectures. An example stands in assembling meshes of these MZIs, including nanowire-based microwave phase-shifters (i.e., a single nanowire coupled to a heater [34]),

with the potential of realizing programmable processors capable of performing SU(N) operations in the microwave domain. Such architectures are generally realized with integrated photonics thanks to the speed, compactness, potential scaling, and low power afforded by using photons [118]. In deployed practical applications, microwave signals modulate light carriers, which are then processed and converted back. Here, thanks to the extreme compression of the microwave wavelength achieved by superconducting nanowires, it could be possible to design processing devices in the microwave regime using photonic-inspired architectures.

3.2 $50\,\Omega$ nanowire transmission lines and devices

In the previous section, we showed a nanowire microwave device with a footprint of about $2\,\mathrm{mm}^2$. However, most of the footprint was taken by the impedance-matching tapers. To avoid matching to $50\,\Omega$, a straightforward solution would be to design the nanowire device at $50\,\Omega$. This task is somewhat challenging.

We consider the general relations for the characteristic impedance $Z_0 = \sqrt{\mathcal{L}/\mathcal{C}}$ and effective index $n_{\mathrm{eff}} = \sqrt{\mathcal{L}\mathcal{C}}$. We note that in the presence of a high inductivity, the only way to reduce the impedance is to engineer the capacitance, and in particular, to increase its value to offset the large $\mathcal{L}$. An increased capacitance would also increase the index, giving the indirect benefit of stronger wavelength compression, and an even higher footprint reduction.

In this section, we present strategies to increase the capacitance, with the objective of compensating for the high kinetic inductance and achieving a $50\,\Omega$ architecture.

3.2.1 Ultra-thin dielectric superconducting microstrip

A straightforward way to increase the capacitance in a microstrip architecture while using conventional materials is to reduce the dielectric thickness or increase the conductor width. In Fig. 3-21, we show the simulation of the characteristic impedance as a function of both these parameters assuming a thin-film silicon dielectric layer ($\epsilon_{\mathrm{r}} = 11.7$). With a 10 nm-thick film, a 2.5 µm-wide NbN conductor results in a $Z_0 = 50\,\Omega$ impedance and $n_{\mathrm{eff}} = 190$. The extreme compression of the microwave wavelength, together with the few-micron line, allows a reduced footprint and does not require impedance matching. The structure can be

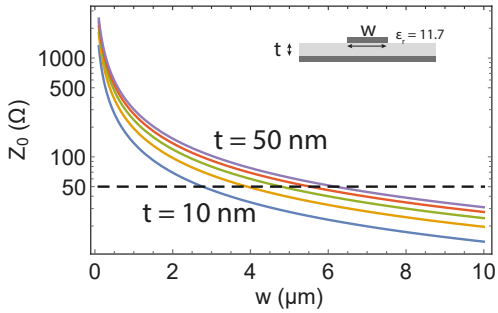

Figure 3-21: Low impedance nanowire transmission lines, obtained with a reduction of the dielectric thickness.

realized by engineering a thin-film dielectric deposition process using sputtering or atomic layer deposition. The dielectric quality, continuity, and conformality are the main challenge in this case.

Another method to increase capacitance consists of exploring high-dielectric constant materials. By increasing ϵ_r considerably, one could relax the requirement on the dielectric thickness while keeping $\approx$ µm wide conductors. The use of high-permittivity oxides, such as hafnium dioxide ($\epsilon_r = 25$) or titanium dioxide ($\epsilon_r = 80$), can get to 50 Ω with a thickness of 100 nm and microstrip width of about 3 µm.

3.2.2 Ultra-high dielectric constant bilayer SCPW

Using extremely thin layers or material with high-dielectric constants, or a combination of both, one could get to 50 Ω with µm-wide conductors. Unfortunately, the capacitance produced by a nano-sized microstrip cannot wholly offset the high-kinetic inductance, suggesting that it is impossible to decrease the line width below $\approx$ 1 µm.

Advances in materials science have allowed the synthesis of ceramic materials belonging to the class of perovskites with extremely high relative permittivities. One such material, strontium titanate ($SrTiO_3$, abbreviated as STO) [119], has been shown to have a relative permittivity exceeding 10^4 in a single crystal form at 4 K, a value that decreases upon the application of an external electric field. This permittivity would be sufficiently large to achieve a 50 Ω characteristic impedance with an NbN nanowire. However, to interface the nanowires to other circuits, a transition to micrometer width is still necessary for readout. As the wire width increases, the kinetic inductance decreases, and the extreme permittivity of STO results in transmission lines with characteristic impedances well below 50 Ω.

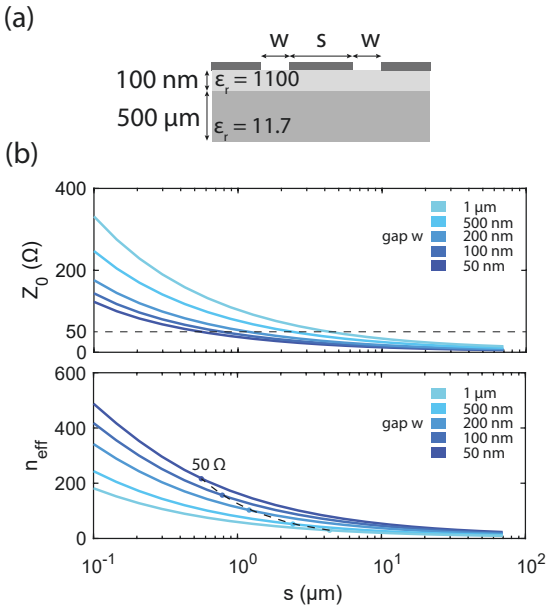

Figure 3-22: Superconducting coplanar waveguide fabricated on a multilayer dielectric, using an ultra-high dielectric constant material. (a) Cross-section sketch. (b) Characteristic impedance and effective index as a function of gap and width.

We can use the bilayer SCPW we introduced in the previous section to solve this challenge. In particular, we combine a thin film of ultra-high dielectric constant material (the STO) on a silicon substrate. At nanoscale dimensions, the STO dominates the effective permittivity, but as the transmission linewidth increases, the contribution of the STO to the total effective permittivity decreases [58]. By tuning the width and gaps of the CPW, one can get a constant $50\,\Omega$ while transitioning from nanowire to $\approx 100\,\mu$m bonding pad. In Fig. 3-22, we show the simulation of the characteristic impedance of a superconducting CPW on a 100 nm STO substrate ($\epsilon_r = 1100$) on the silicon substrate. The impedance is calculated as a function of the conductor width for several gaps.

3.2.3 $50\,\Omega$ nanowire SCPW resonators

In this section, we use the bilayer ultra-high dielectric constant SCPW architecture introduced above to realize nanowire resonators with a $50\,\Omega$ impedance and extreme compression of the microwave wavelength. Part of the material presented here has been published and is reproduced from Applied Physics Letters 119.25 (2021): 252601 [58]. This work was carried out in collaboration with Prof. Daniel F. Santavicca. Design and testing were performed at

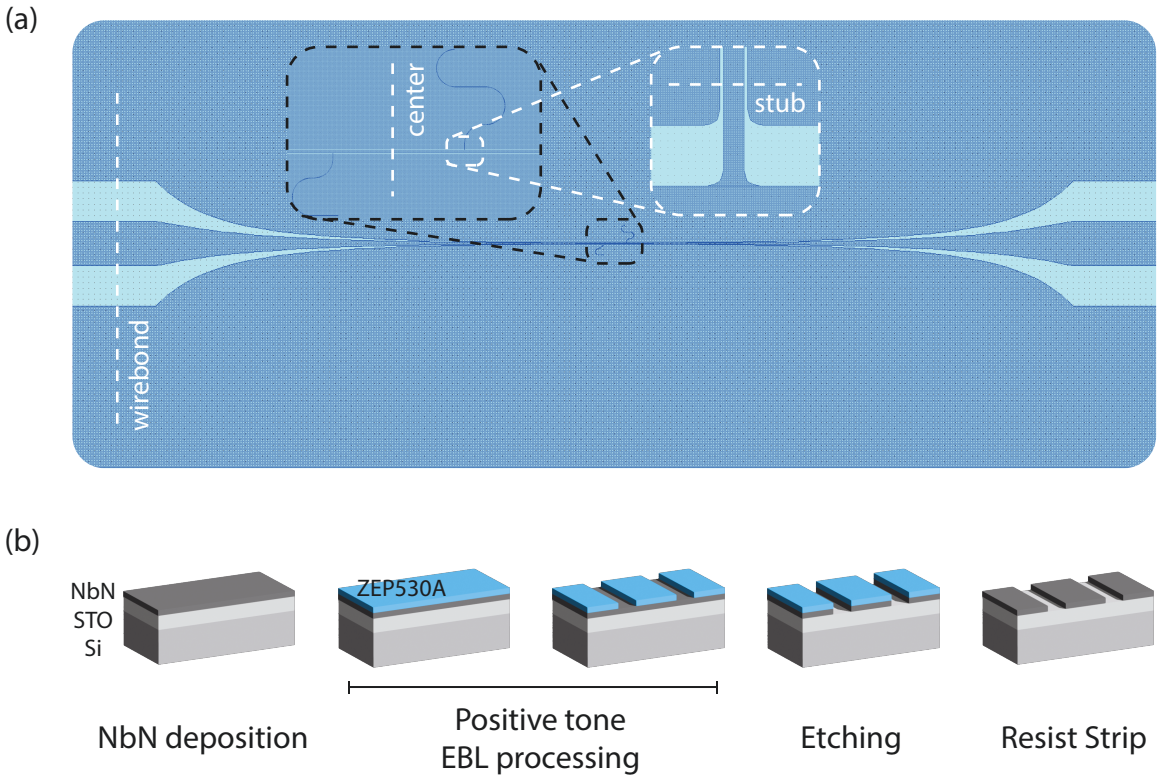

Figure 3-23: Nanowire stub resonators fabricated with ultra-high dielectric constant SCPW. (a) Design layout. (b) Fabrication process.

the University of North Florida (UNF) by Prof. Santavicca and collaborators. Fabrication and design verification were performed at MIT.

Material

The $SrTiO_3$ (STO) thin-film was grown by molecular-beam epitaxy (MBE) on an (001) oriented extremely low-doped silicon (Si) substrate. Ref. [58] reports the growth parameters and process. All the precautions were taken to enhance conformality and reduce oxygen vacancies, which could increase dielectric losses. X-Ray diffraction measurements confirmed the good quality of the grown crystal [58].

Design and fabrication

In Table 3.3, we summarize the parameters of the device assuming STO with a permittivity $\epsilon = 1100$, and using a 15 nm-thick NbN with a 21.5 pH per square sheet inductance. In the

section	width	gap	Z_0	n_{eff}	length	expected resonance
wirebond	400 µm	360 µm	43.1 Ω	3.1	-	-
center	5 µm	1.75 µm	62.2 Ω	23.7	-	-
stub 1	560 nm	120 nm	65.4 Ω	184.8	200 µm	4.06 GHz
stub 2	560 nm	120 nm	65.4 Ω	184.8	300 µm	2.70 GHz

Table 3.3: Design parameters and expected resonance frequencies for the 50 Ω bilayer superconducting nanowire coplanar waveguide.

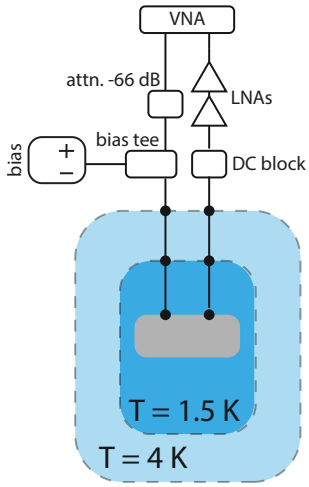

Figure 3-24: Measurement setups for SCPW stub resonators device.

initial design stage, the permittivity of STO thin film was unknown. The value used here was obtained by matching the simulation with the experimental data, shown in the next section. The impedance and effective indexes shown in the table are simulated using Sonnet EM. We note that the impedance values are slightly off the target of 50 Ω. We did not optimize the dimensions further to reach the exact value of 50 Ω as this minor discrepancy does not significantly affect the results or the demonstration.

We show the fabrication flow in Fig. 3-23(b). Thanks to the SPCW architecture, the fabrication is pretty straightforward. After the NbN deposition, we perform a single-layer electron beam lithography exposure with a positive tone resist, followed by reactive ion etching and cleaning. We discuss process details in Appendix A.

Reference	Instrument
Room temperature LNA	2× Minicircuits ZX60-V63+ (0.05 GHz − 6 GHz)
VNA	HP 8720D
Bias tee	Mini Circuits ZFBT-6GW+
Cryostat	4 K cryostat with 1 K pot
Current source	Yokogawa 7651 + 100 kΩ

Table 3.4: Overview of the instruments for the measurement setup shown in Fig. 3-24.

Measurement setup

In Fig. 3-24, we show a sketch of the characterization setup, accompanied by a list of the equipment in Table 3.4. The measurements were run at the University of North Florida by Prof. Daniel F. Santavicca. The device was mounted inside the vacuum can of a helium-4 cryostat with a base temperature of 1. K. One port of the device (input) was interfaced to the Port 1 of a VNA. On the same line we included a bias tee, which we use to perform DC tests. The VNA power (0 dBm) was attenuated at room temperature with a −66 dB attenuator. The output of the device was interfaced to Port 2 of the VNA through a chain of room-temperature LNAs and a DC block.

Results

We first characterized the superconducting and DC properties of the device. The critical temperature was 12.0 K. The switching current measured between the center conductor of the SCPW and the ground (measuring the two resonators in parallel) was 813 μA at 1.5 K. We measured the scattering parameters of the device at 1.5 K. The signal power at the device was < -70 dBm (< 1.4 μA), such as to avoid exciting non-linear effects. Fig. 3-25(a) shows the transmission of the SCPW resonators. We also measured a calibration device with the same CPW geometry but no resonators to normalize the data. The fundamental half-wave resonances occurred at 2.80 GHz and 4.20 GHz, for the 300 μm and 200 μm stubs, respectively. These resonances correspond to an effective index on the resonators $n_{\text{eff}} = 178$. The quality factor of the resonators was about $Q = 160$. By matching the simulation (AWR Microwave Office) to the experimental data, we were able to determine that our thin-film STO has a permittivity of $\epsilon_{\text{r}} = 1100$ and a loss tangent $\delta = 0.009$ (Fig. 3-25(b)). Note that the loss tangent represents an upper bound on the actual loss tangent of the STO as all the other materials were assumed lossless while matching the simulation.

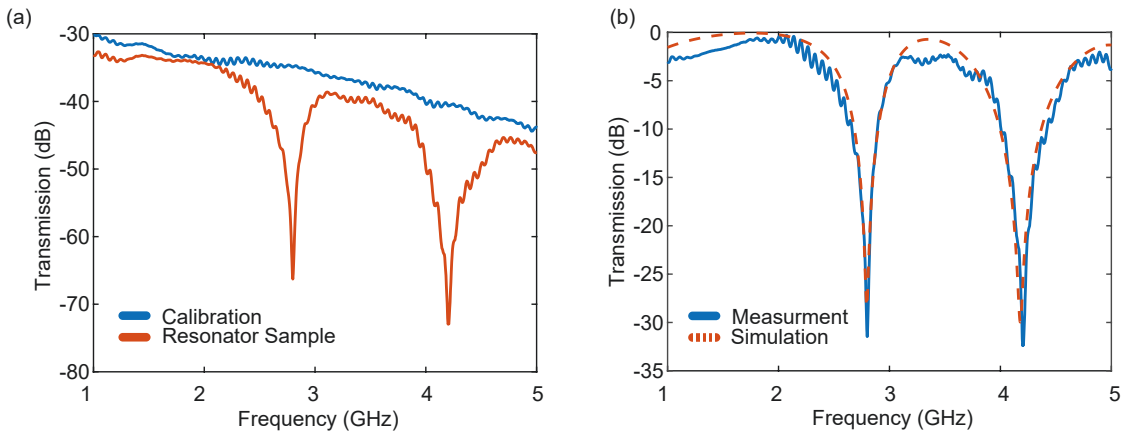

Figure 3-25: Device characterization. (a) Calibration and device raw transmission; (b) Normalized transmission compared with simulation.

Conclusion

We demonstrated ultra-compact nanowire stub resonators with GHz frequency operation. Thanks to the combination high-inductance nanowires and high-dielectric constant substrate, our SCPW transmission line design achieve a $\approx 50\,\Omega$ characteristic impedance and does not require impedance matching for seamless operation with normal electronics. Thanks to the extreme wavelength compression, our device is ≈ 178 times smaller than a counterpart realized on a traditional printed circuit board (e.g., copper on FR4). Our work demonstrates that with substrate engineering, it is possible to design ultra-compact nanowire devices operating at $50\,\Omega$. A promising future direction is combining superconducting nanowires with other dielectric substrates exhibiting non-linear properties, such as ferroelectrics, piezoelectrics, and electrooptics. Strontium titanate is ferroelectric. Coupling the properties of kinetic inductive nanowires with these types of substrates might lead to non-linear non-reciprocal devices with applications in quantum transduction and sensing. Traveling wave parametric amplifiers, circulators, and transducers could be realized towards a complete nanowire-based superconducting MMIC technology.

3.3 Summary and perspective

In this chapter, we showed two applications of superconducting nanowire transmission lines. In Sec. 3.1, we engineered a superconducting covered microstrip using conventional semi-

conductor materials and a thin-film niobium nitride. We used this structure to demonstrate a 3 dB microwave directional coupler operating at 5 GHz, whose coupling section footprint is just about 500 μm^2. The characteristic impedance of the structure is about 1.5 kΩ, and the effective index is about 55. To interface the device to 50 Ω electronics, impedance matching tapers are required, and the footprint increases to $\approx 2\,mm^2$. The dependence of the kinetic inductance on operational parameters, such as bias current and temperature, allows tuning the characteristic of the coupler. In particular, we demonstrated that both current injection and temperature increase leads to a change in the coupling ratio, explicitly increasing the coupled power. The injection of bias current makes the coupler asymmetric and allows minimal tuning of the coupling point. The temperature keeps the symmetry of the coupler and shifts the coupling point to lower frequencies, allowing the exploration of a larger tuning regime. We also provided design improvements to increase the bandwidth and improve the isolation figure. Overall, our 3 dB coupler is tunable and potentially has high bandwidth and isolation. We proposed its application as a base element for other nanowire-based microwave devices with application in scaling superconducting quantum computing hardware. We also proposed the combination of this coupler with phase shifters to design programmable processors and circuits based on networks of these components.

The naturally large impedances of our structures can create challenges for coupling to standard microwave circuitry design, mainly when it's impossible to afford impedance-matching structures. To address this challenge, in Sec. 3.2.3, we introduced methods to decrease the characteristic impedance while keeping the natural wavelength compression of our structure. To compensate for the high inductance of thin-film nanowires, we propose their use in combination with ultra-high dielectric constant materials. We proposed a SCPW on a bilayer dielectric consisting of strontium titanate on silicon. We demonstrated 100 μm-long half-wavelength stub resonators at GHz using 500 nm wide lines, while keeping an inductance of 50 Ω, and achieving a compression factor of about 200. This demonstrates that we can fabricate microwave devices operating at the standard 50 Ω, but with an extreme footprint reduction compared to normal microwave circuitry. A future direction is integrating nanowires on other substrates exhibiting non-linear behaviors to investigate combined functionality in quantum transduction.

Cryogenic microwave circuitry is receiving an increased interest driven by the field of quantum computing based on superconducting circuits. In these systems, several distributed

microwave components, such as filters, resonators, couplers, circulators, and traveling wave parametric amplifiers, are necessary for qubit measurements and readout. However, the size of these distributed components is limited by the signal wavelength $\approx$ cm for GHz signals in standard material systems. This large size makes on-chip integration difficult and represents one of the major bottlenecks in scaling up cryogenic microwave systems. Our platform solves these challenges, with the added benefit of being already cryogenic and CMOS-processing compatible.

Chapter 4

Impedance-matched differential readout SNSPDs

Superconducting nanowire single-photon detectors (SNSPDs) are the preferred photon-counting technology at near-infrared wavelength. Specialized designs can achieve 98% system detection efficiency [120], 4.6 ps system jitter [42], 10^{-7} cps dark count rate [48], 1.5 Gcps maximum count rate [121], as well as intrinsic photon number resolution [89]. These outstanding performances make them an attractive technology for many applications, including optical communication [121], single-photon LIDAR [122, 42], high-energy physics [123, 48], and biomedical imaging [124, 125].

Quantum information science applications need high-performance single-photon detectors, and SNSPDs shine in these contexts [126]. A couple of notable examples: SNSPDs were used to demonstrate a loophole-free violation of the Bell's inequality [127], they are routinely used for distance records experiments in QKD applications [128], and they are the photon detection technology in the recent 100-mode Gaussian boson sampling experiment [26], claiming quantum advantage.

While SNSPDs have demonstrated high performance, there is considerable room to improve this technology further [126]. In this thesis, we will focus on two main directions:

- **Performance improvement** Users and applications will always need SNSPDs with better performances. The requirements for an *all-rounder* SNSPD, where two or more metrics are simultaneously maxed out, are increasing. Special applications need unique properties such as detection at longer wavelengths or photon number resolution (PNR)

capabilities [56].

- **Array technology and integration** While single-pixel detectors are enough for limited-size experiments, multiplexed pixel designs will be necessary with the increase in experiment complexity and functionality. Similarly, direct integration on experimental platforms (e.g., with photonic integrated circuits) will be necessary to reduce the number of connections and coupling loss.

In this chapter, we focus on the first direction. One challenge currently faced with SNSPDs is integrating multiple of the aforementioned metrics into a single design. Commercially available SNSPDs can provide an efficiency of around 85% but have a limited timing resolution to about 40 ps [129]. Although these performances are often enough for current experiments, they are far from the academic records on single metrics. This is caused by necessary metrics trade-offs inherent to the traditional designs. In the following sections, we show that by engineering the architecture of the detector, conforming to the microwave properties of superconducting nanowires, one can overcome these performance compromises. Some materials presented in the chapter have been published and are reproduced from Physical Review Applied 19.4 (2023): 044093. I would like to acknowledge Dr. Boris Korzh for his priceless help and support during this project, Dr. Matthew Shaw and Prof. Maria Spiropulu for hosting me in their laboratory space at the California Institute of Technology (Caltech) for the experimental characterization of the devices, Dr. Andrew Beyer for carrying out part of the fabrication at the Microsystem Device Laboratory (MDL) at the Jet Propulsion Laboratory (JPL), Dr. Jason Allmaras for the design of the optical stack and for sharing preliminary codes for data processing, and Andrew Muller for his help with the characterization setup at Caltech.

4.1 Important metrics and trade-off

Here we specifically focus on one crucial trade-off: the one with detection efficiency and timing resolution. Before going into the details on the origin of this trade-off, we will spend a few paragraphs expanding on these two fundamental detection metrics.

Detection efficiency

We described the concept of detection efficiency (DE) in the introduction to the thesis. Here we highlight a few additional details. First, when discussing DE in applications, it is important to report the *system* detection efficiency (SDE). SDE includes all the coupling losses to the detectors and represents the effective efficiency the end user will experience in experiments. A detector designer must consider four main elements to achieve a high system detection efficiency:

- **Detector active area (A).** The detector active area must be large enough to collect the projected optical mode (free-space or fiber-coupled). A large active area will increase the efficiency, but it will make the detector slower and more prone to dark counts.

- **Meander fill factor (FF).** The SNSPD is generally meandered to realize a compact active area. Increasing the meander fill factor can increase the efficiency, but it might degrade the electrical performance with larger current crowding in the bends and fabrication defects [130, 131, 132]. Generally, FF = 25% to FF = 33% is recommended.

- **Optical stack and anti-reflection coating.** Superconducting nanowires are made of thin films, achieving limited optical absorption. An optical cavity and anti-reflection coatings are necessary to increase optical absorption. Single optical stacks ($\lambda/4$ cavity) with a metallic reflector are a popular simple option. More complex cavities made with distributed Bragg reflectors (DBR) are also used, but they increase the fabrication complexity significantly.

- **Coupling loss.** Coupling losses are the largest responsible for low system efficiency. It is important to design efficient coupling schemes to reduce losses. A popular solution to the problem is the *lollipop* coupling [133]. The detector die is designed and fabricated to be inserted in a fiber sleeve, self-aligned, and in contact with the fiber core. Other approaches using lensed fibers and active coupling (e.g., piezopositioners) are possible but increase the fabrication and setup complexity [89].

In summary, a necessary, yet not sufficient condition to achieve high system detection efficiency is to have a large enough active area.

Jitter

We described the concept of jitter (i.e., timing resolution) in the introduction to the thesis. Here we highlight a few additional details. The jitter is the uncertainty on the pulse arrival time at the readout. Like for the DE, it is crucial to report the *system* metric, in this case j_{system}. The system jitter includes the intrinsic detection jitter, but also other uncertainty components due to the readout electronics, optical pulse width, and detector geometry. Once again, the end user will experience the system jitter as the true device timing uncertainty. j_{system} can be found experimentally by measuring the time difference between each output pulse and an optical timing reference signal, and by taking the full-width-at-half-maximum (FWHM) of a Gaussian fit to a histogram of such differences. Here, to describe the several components in j_{system}, we take the approach of Santavicca et al. [134]. The system jitter can be decomposed as:

$$j_{\text{system}}^2 = j_{\text{amp}}^2 + j_{\text{geom}}^2 + j_{\text{hotspot}}^2 + j_{\text{timing}}^2 + j_{\text{opt}}^2 \tag{4.1}$$

where

- j_{amp} jitter from the noise of the readout amplifier - can be significant and typically accounts for several tens of ps;
- j_{geom} jitter from the geometric contribution due to the length of the nanowire and slow speed of propagation - can be significant and typically accounts for several tens of ps;
- j_{hotspot} jitter from the stochastic nature of the hotspot formation - on the order of $5\,\text{ps} - 10\,\text{ps}$;
- j_{timing} jitter from the noise on the timing reference - can be minimized making the optical reference with a fast photodiode;
- j_{opt} jitter form the finite optical pulse width - can be minimized using a femtosecond laser.

While it is possible to minimize the external jitter components (j_{amp}, j_{timing}, j_{opt}), the jitter related to the detector geometry j_{geom} and the intrinsic jitter j_{hotspot}, can only be improved by investigating novel design (e.g., differential readout [135]) or detector materials.

In particular, the intrinsic jitter can be further decomposed into the following elements following Kozorezov et al. [136]:

$$j^2_{\text{hotspot}} \propto j^2_{\text{geom},\perp} + j^2_{\text{nu}} + j^2_{\text{Fano}} \tag{4.2}$$

where

- $j_{\text{geom},\perp}$ represents the geometric jitter connected to the absorption site position along the perpendicular direction (y axis), including coordinate-dependent dynamics of normal domain initiation and growth;
- j_{nu} reflects contributions due to material-dependent spatial non-uniformities;
- j_{Fano} represents the jitter contribution due to Fano fluctuations in the detection process, specifically in the electron-phonon interactions during the energy downconversion process [136].

$j_{\text{geom},\perp}$ was estimated to be $< 1\,\text{ps}$ for detectors operating closer to the detector depairing current ($> 0.7 I_{\text{dep}}$) [137] and $j_{\text{j,nu}}$ can be minimized by selecting amorphous materials. Ultimately, j_{Fano} is considered the most plausible responsible for the remaining intrinsic jitter, affecting the uncertainty on the detector latency [136, 47].

The trade-off

In general, to obtain a high SDE at 1550 nm, an active area larger than $H \times W = 15\,\mu\text{m} \times 15\,\mu\text{m}$ is needed. This size ensures that the optical mode projected by the optical fiber is fully contained in the detector active area. Assuming a fill-factor of FF = 33% and a width of $w = 100\,\text{nm}$, the total length of the nanowire will be $L = WH\,\text{FF}/w \approx 740\,\mu\text{m}$. If the nanowire behaves like a slow-speed transmission line with a $v_{\text{ph}} = 3\,\mu\text{m/ps}$, the end-to-end propagation delay amounts to $\approx 250\,\text{ps}$. This implies that the uncertainty on the pulse arrival time at the output can be as large as 250 ps, assuming the photons can be detected over the whole active area. As a consequence, the geometric jitter component j_{geom} can be fairly significant, on the order of $\approx 100\,\text{ps}$.

This back-of-the-envelope calculation shows that in the effort to increase the active area to enhance the collection efficiency, hence the SDE, one negatively affects the system jitter. For this reason, a trade-off between the two metrics is unfortunately inevitable. Commercial

SNSPDs achieve about 85% SDE with 40 ps of jitter. The record jitter device [42] with $j_{\text{system}} = 4.6$ ps was just a single 5 µm-long straight wire, with an estimated efficiency of 0.01%. The record efficiency device with SDE = 98% [50] had a system jitter larger than 100 ps.

The dependence we just pointed out finds some exceptions. As a matter of fact, this trade-off is mainly determined by the superconducting nanowires behaving like a slow-speed transmission line. This behavior is particularly marked when nanowires are fabricated on optical cavities with metallic mirrors. The mirror acts as a ground plane, decreasing the velocity. In SNSPD with optimized superconducting films (lower inductance) and fabricated on DBRs, the speed of light is not as slow as in the other architectures, and the lumped-element approximation can still hold. In this case, it is possible to achieve high-efficiency ($> 85\%$) and low-jitter detectors (< 15 ps) [138, 49]. Although, as we will see later in this chapter, these detectors miss on some great additional features afforded by the slow-speed properties of nanowires.

To solve this inherent trade-off between SDE and jitter, in the next section we propose a new architecture.

4.2 Impedance-matched differential architecture

In this section, we describe the concepts and inspiration at the base of our improved detector architectures.

4.2.1 Overview and inspiration

To address the combination of a large active-area with the low-jitter operation, we engineer impedance-matched devices in a differential readout configuration. An artistic sketch of the architecture is shown in Fig. 4-1.

Differently from a traditional single-ended SNSPD, in our device both ends of the meander are interfaced to the readout electronics through impedance-matching tapers. This architecture tackles the trade-off between efficiency and timing jitter. However, it also increases the number of electrical components for its readout and control (2 × bias, amplifier,

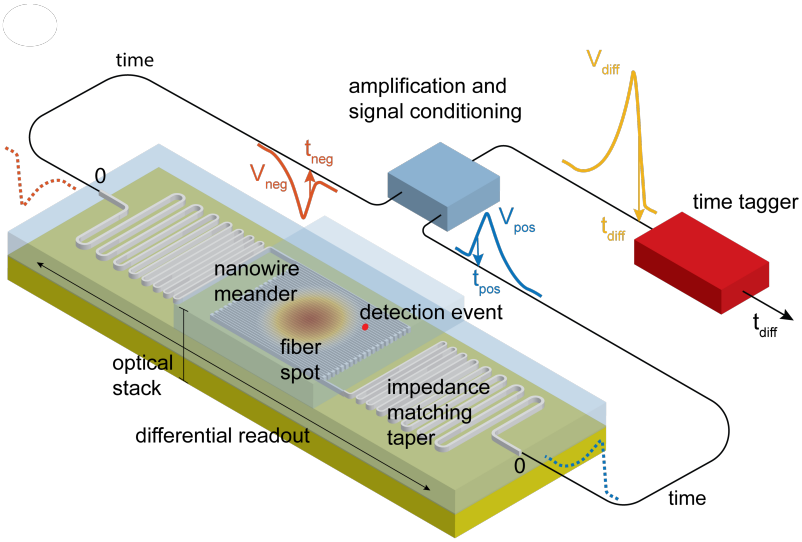

Figure 4-1: Artistic sketch of our improved single-photon detector architectures. A standard single-pixel SNSPD, embedded in an optical cavity, is read out deferentially through two impedance-matching tapers. In the final implementation, the signals are collected and post-processed using dedicated electronics.

cables) and, ultimately, the cost to the end-user. To address this second problem, we also design readout electronics to convert differential signals back to single-ended, such as to maintain the current detector operation methodology and compatibility with commercial refrigeration systems. This is shown in the sketch in Fig. 4-1 as the *amplification and signal conditioning* and *time tagger* blocks.

Our device inherits its base elements from the superconducting nanowire single-photon imager (SNSPI) [54]. The SNSPI was designed to provide micrometer-level spatial resolution based on the timing information from post-processed differential photon-detection pulses. The impedance-matching tapers were mainly used to preserve the fast-rising edges of the pulses. Here, we adopt the same two-ended impedance-matched readout scheme. However, we engineer the readout elements to improve the timing performances of a single-pixel SNSPD. Our impedance-matching tapers are designed to achieve a superior signal-to-noise ratio and minimize reflections and distortions at the device level [139]. The differential readout architecture is engineered to automatically cancel the geometric delay-line contributions to the timing jitter (j_{geom}).

Our optimized architecture provides a path to low-jitter large-area single-pixel designs, breaking the existing trade-off between these design variables. As we provide more details,

Parameter	Description
t_{pos}	time tag of the positive pulse V_{pos}
t_{neg}	time tag of the negative pulse V_{neg}
t_{Σ}	sum of the time tags $t_{\Sigma} = \frac{t_{\mathrm{pos}}+t_{\mathrm{neg}}}{2}$
j_{Σ}	jitter, associated to t_{Σ}
t_{Δ}	difference of the time tags $t_{\Delta} = t_{\mathrm{pos}} - t_{\mathrm{neg}}$
t_{diff}	time tag of the difference of the complementary pulses $V_{\mathrm{diff}} = V_{\mathrm{pos}} - V_{\mathrm{neg}}$
j_{diff}	system jitter, associated to t_{diff}

Table 4.1: Summary of the definition of relevant timing parameters.

we take the occasion to present Table 4.1 summarizing some of the terminology used in the following sections.

4.2.2 Differential readout

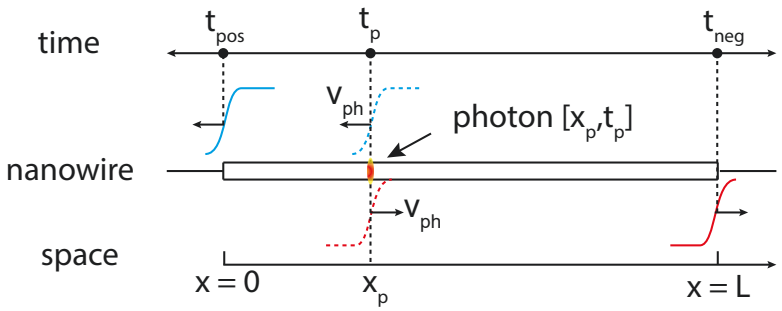

Figure 4-2: Sketch of differential readout method. A photon-generated hotspot launches two counter propagating rising edges, traveling to the ends of the nanowire. If the two rising edges are tagged at the readout, those time-tags can be processed to either distill a geometry-independent or a time-independent tag.

The concept of differential readout, applied to SNSPDs, was first introduced by Calandri et al. [135]. Referencing Fig. 4-2: we consider a nanowire of length L with a velocity v_{ph}. A photon-generated hotspot, at time t_{p} and coordinate x_{p}, launches two counter-propagating rising edges traveling towards the nanowire ends. The time tags at the readouts can be expressed with the parameters of the wire:

$$t_{\mathrm{pos}} = t_{\mathrm{p}} + \frac{x_{\mathrm{p}}}{v_{\mathrm{ph}}}, \tag{4.3a}$$

$$t_{\mathrm{neg}} = t_{\mathrm{p}} + \frac{L - x_{\mathrm{p}}}{v_{\mathrm{ph}}}. \tag{4.3b}$$

We can observe that by manipulating these expressions one can eliminate either the time or spatial coordinate:

$$t_{\Sigma} = \frac{t_{\mathrm{pos}} + t_{\mathrm{neg}}}{2} = t_{\mathrm{p}} + \frac{L}{2v_{\mathrm{ph}}}, \tag{4.4a}$$

$$t_{\Delta} = t_{\mathrm{pos}} - t_{\mathrm{neg}} = \frac{2x_{\mathrm{p}} - L}{v_{\mathrm{ph}}}. \tag{4.4b}$$

By using t_{Σ} to represent the timing information of a detection event, one can make this process independent from the geometry. It should also be clear that the jitter associated with t_{Σ}, j_{Σ}, will also be independent of the geometry of the detector. By using Santavicca's approach [134]:

$$j_{\Sigma}^2 = \frac{j_{\mathrm{amp,neg}}^2}{4} + \frac{j_{\mathrm{amp,pos}}^2}{4} + j_{\mathrm{hotspot}}^2 + j_{\mathrm{timing}}^2 + j_{\mathrm{opt}}^2. \tag{4.5}$$

We also observe that the jitter due to the amplifier noise is reduced by a factor of 2. By minimizing the external jitter components, one can observe the intrinsic jitter, j_{hotspot} in any SNSPD, independently from its area.

Conversely, by using t_{Δ}, one can reconstruct the location of the detection event on the detector and

$$j_{\Delta}^2 = 4j_{\mathrm{geom}}^2 + j_{\mathrm{amp,neg}}^2 + j_{\mathrm{amp,pos}}^2. \tag{4.6}$$

From this expression, one could retrieve j_{geom}.

In summary, when we design SNSPDs for differential readout, the system jitter j_{system} is independent from j_{geom} and $\equiv j_{\Sigma}$.

4.2.3 Impedance matching

In the previous chapter, we introduced the concept of impedance matching and used it to interface high-impedance transmission lines devices to normal $50\,\Omega$ electronics. Here we use the same concept applied to single-photon detectors. Assume a single photon detector made with a high impedance nanowire (Z_{H}) interfaced with a $Z_{\mathrm{L}} = 50\,\Omega$ readout. The output voltage on the load will be proportional to and cannot exceed:

$$V_{\mathrm{load}} \propto I_{\mathrm{bias}} \times 50\,\Omega, \tag{4.7}$$

where I_{bias} is the bias current. When using an impedance matching taper, assuming broadband lossless operation, one can establish the following identity:

$$I_{\text{L}}^2 Z_{\text{L}} = I_{\text{H}}^2 Z_{\text{H}} \tag{4.8}$$

where I_{L} (I_{H}) is the current injected in the low (high) impedance side of the taper, Z_{L} (Z_{H}). In presence of the taper, the output voltage will be proportional to and cannot exceed:

$$V_{\text{load}} \propto I_{\text{bias}} \sqrt{\frac{Z_{\text{H}}}{Z_{\text{L}}}} \times 50\,\Omega, \tag{4.9}$$

representing a passive amplification of about $\sqrt{\frac{Z_{\text{H}}}{Z_{\text{L}}}}$ compared to the unmatched detector. As a summary, using an impedance matching taper, one will observe a passive amplification leading to an improved slew rate and signal-to-noise ratio (SNR) [139]. Moreover, thanks to the impedance-matching, signal reflections and distortions will be minimized. The use of impedance matching taper can help reducing the electrical noise contribution to the timing jitter, j_{amp}

4.2.4 Specialized readout electronics

The introduction of low-jitter detectors in applications represents another outstanding challenge. To characterize and use fast detectors, one generally requires a real-time oscilloscope. Unfortunately, these are expensive, large, and have a limited number of channels. By introducing a differential readout detector, we are making this even more challenging.

Commercial SNSPDs are nowadays deployed with time-to-digital converters (TDC), realizing the popular technique called time correlated single-photon counting (TCSPC). This represents a cheaper and more scalable option compared to real-time oscilloscope readout.

To make sure our novel detector architecture can be deployed in current commercial systems, we also introduce electronics converting the differential readout scheme into a single-ended readout. To characterize the potential performance of our detector in an existing refrigeration system, we used a commercial TDC system in combination with our converters.

4.3 Simulation of SNSPDs readout architectures

In this section, we compare the output signals from three SNSPD designs, using SPICE simulations. We show the advantages of using a differential impedance-matched readout over traditional schemes.

4.3.1 SPICE simulation setup

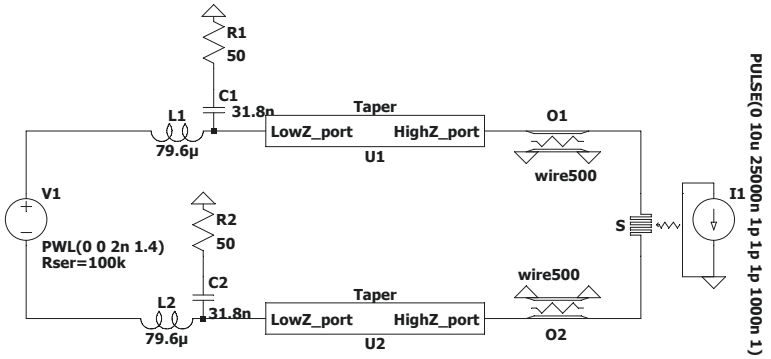

Figure 4-3: Schematics of the LTspice simulation for an impedance-matched differential detector. The taper is modeled as cascaded transmission lines (300 sections) with varying impedance and velocities. The nanowire is simulated as a lossy transmission line (LTRA) with $L = 800.6\,\mu$H/m and $C = 75.27\,$pF/m. In this specific scheme the length of the symmetric transmission line are set to $500\,\mu$m. Note that L1, C1, L2, and C2 constitute bias-tee elements. Their values were selected to match the specification of commercial bias-tees employed in measurement setups.

We set up a simulation environment using LTspice. Our single-pixel SNSPD was simulated as the combination of a photon-sensitive element, corresponding to the inductance of a single-wire, and two high-impedance slow-speed transmission lines with a length matching our designs. For the photon-sensitive element, we used the model by Berggren et al. [140] based on the phenomenological hotspot velocity model by Kerman et al. [141]. For the slow-speed nanowire transmission lines (Sec. 4.3.2), we used the LTspice-embedded lossy transmission line model (LTRA). We used a capacitance per unit length and an inductance per unit length values reproducing the impedance and velocity of the nanowire transmission line ($L = 800.6\,\mu$H/m and $C = 75.27\,$pF/m) as shown in Sec.4.5.2. The biasing circuits included a bias tee, with a 100 kHz cutoff frequency ($L = 79.6\,\mu$H and $C = 31.8\,$nF), and a current source realized with a voltage source with $100\,$kΩ series resistance. What we just described represents the simulation of a conventional single-ended SNSPD readout, discussed

in Sec. 4.3.2

For the simulation of a single-ended impedance-matched readout (Sec. 4.3.3), we included an impedance-matching taper, designed following the Klopfenstein taper theory. The taper was simulated as a cascade of 300 transmission line sections (LTRA) with varying impedances and velocities, designed for an overall cutoff frequency of 200 MHz and an in-band return loss of −20 dB.

For the simulation of differential impedance-matched readout (Sec. 4.3.4), we included a second impedance-matching taper and second bias tee on the other side of the SNSPD. Moreover, the biasing was converted to fully differential. Fig. 4-3 shows this final simulation setup. The other setups can be reconstructed by removing selected elements.

4.3.2 Conventional readout

In the conventional readout architecture, the SNSPD is configured for single-ended readout with a 50 Ω RF low-noise amplifier on one side and termination to the ground on the other side. This is shown in Figure 4-4(a). When a photon is absorbed and creates a hotspot, it generates two counter-propagating, opposite rising edges. One travels towards the 50 Ω output (LNA or readout) and gets reflected from the large impedance mismatch. The other travels towards the ground termination and gets reflected. The process continues till the hotspot heals. Figure 4-4(b) shows the simulation of the output detection pulses (probed on the 50 Ω load) for photons absorbed at three different locations on the detector's active area. The voltage pulses are characterized by several reflections and distortions caused by the impedance mismatch on both sides of the nanowire. These cause a reduced slew rate and lead to a higher impact of electrical noise on the timing jitter (j_{amp} [42, 134]). When photons are absorbed in different locations of the meander, the propagation delays in the nanowires due to low velocity will appear at the output as uncertainty on the pulse arrival time. This is called geometric jitter j_{geom} [135]. However, the partial reflection from the termination to the ground creates a local feature on the rising edge of the pulse (dashed circle), which acts as a partial compensation for the j_{geom}. The compensation feature on the rising edge was previously experimentally observed in Ref. [142], analyzed in Ref. [143], and described as a pulse-echoing effect due to impedance mismatch. This effect might explain the compensation of the geometric jitter in traditional detectors. Triggering at this optimal level produces a time tag with the geometric contribution partially compensated

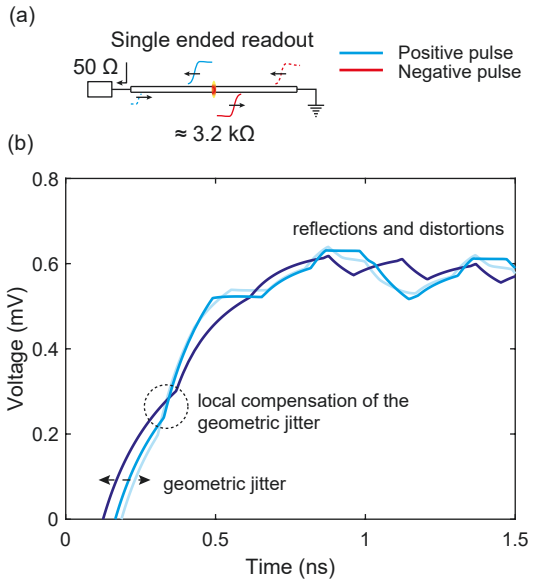

Figure 4-4: Simulation of detection pulses from an SNSPD in a conventional readout configuration. (a) Schematic of the pulse reflection dynamics. (b) Output pulses on the 50 Ω load. Light to dark color shading indicates the distance of the absorption location from the load port.

for. Nevertheless, this compensation feature strongly depends on other elements of the SNSPD design (e.g., pad layout, printed circuit board (PCB), ground termination) and does not always guarantee optimal timing resolution. Moreover, this treatment only applies to detectors in a distributed regime.

4.3.3 Single-ended impedance-matched readout

In the conventional readout, the high impedance nanowire is interfaced to 50 Ω electronics leading to pulse reflections and distortions, and limited SNR. These issues can be mitigated by integrating an impedance-matching structure at the readout port interfacing the high-impedance nanowire (in this case 3.2kΩ) to the 50 Ω. Thanks to the impedance transformation, the output pulse has a higher amplitude and a faster slew rate, allowing a reduction of the electrical noise contribution to the timing jitter through a higher SNR [139]. Fig. 4-4(a) shows the reflection dynamics of the impedance-matched readout. There are no reflections from the load thanks to the impedance-matching taper. The simulation result in Fig. 4-5(b) shows that the integration of a 200 MHz cutoff Klopfenstein taper increases the output amplitude by a factor of 3.3, compared to the unmatched version in Fig. 4-4. This

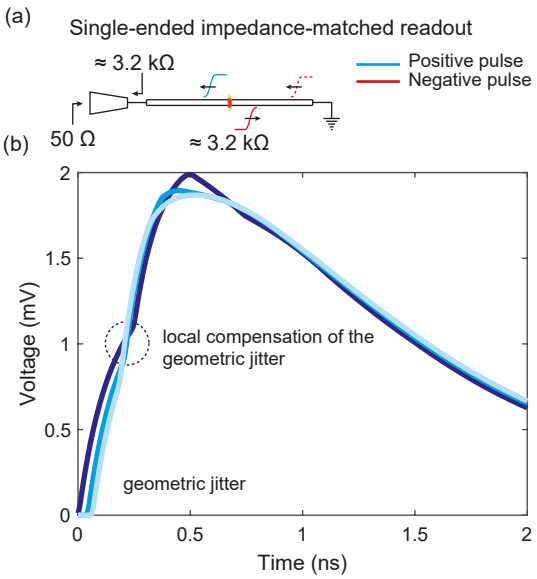

Figure 4-5: Simulation of detection pulses from an SNSPD in a single-ended impedance-matched readout configuration. (a) Schematic of the pulse reflection dynamics. (b) Output pulses on the 50 Ω load. Light to dark color shading indicates the distance of the absorption location from the load port.

intrinsic amplification is in agreement with previous experimental demonstration [139]. The pulse-rising edge is affected by just one reflection due to the ground terminal. The geometric effects of the transmission line for pulses generated by photons absorbed on different locations in the active area are still present. However, the ground reflection provides the local feature where j_{geom} is partially compensated.

4.3.4 Differential impedance-matched readout

The use of single-ended impedance-matched designs improves the SNR of the device but does not solve the impact of geometric effects on the timing jitter. We show here the results of using our proposed differential impedance-matched architecture.

Figure 4-6(a) shows the reflection dynamics of a detector in this configuration. Thanks to the differential impedance-matched readout, we have no reflections or distortions. However, we must process two complementary output pulses, V_{pos} and V_{neg}. Figure 4-6(b) shows the output pulses probed on the two 50 Ω readouts. These show no reflections and have a superior slew rate compared to the unmatched pulse. However, we can still see the geometric effects when photons are absorbed in different areas of the meander. As we described above, we can time-tag the pulses and compute t_{Σ} to make the detection process independent from

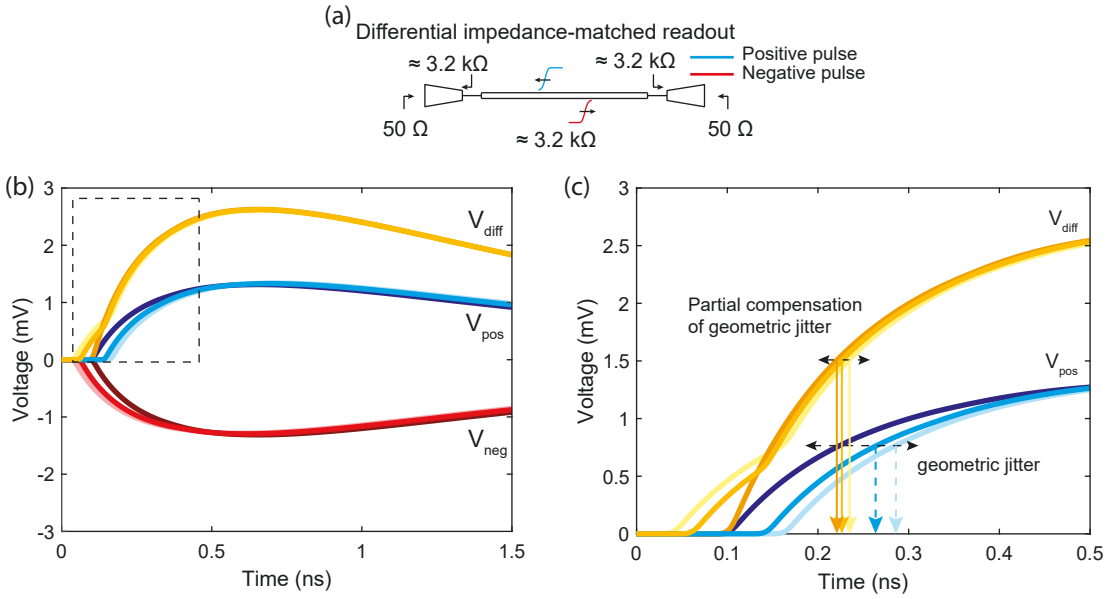

Figure 4-6: Simulation of detection pulses from a differential impedance-matched SNSPD. Here we interface both the detector ends to the 50 Ω readout through identical Klopfestein impedance matching tapers. (a) Pulse reflection dynamics. (b) Detection of photons on different sections on the meander. (c) Zoom in on the pulse traces in panel (b). We demonstrate that by processing the difference of the complementary pulses, one can partially compensate for the impact of geometric effects on the timing jitter.

the geometry. Equivalently, as shown in Fig. 4-6(c), partial cancellation of the geometric contribution can be achieved by processing the difference of the complementary pulses $V_{\text{diff}} = V_{\text{pos}} - V_{\text{neg}}$.

4.4 Electrical Readout

As we mentioned in the introduction, using a differential detector can increase the number of readout electrical components (e.g., amplifiers and cables), creating issues with the scalability of this technology. To solve this problem, we provide readout electronics to convert the differential architecture to a single-ended readout while preserving the advantages given by our design. In this section, we describe several readout methods for our detectors.

4.4.1 Direct two-channel readout

The simplest way to read out the differential impedance-matched detector involves using a high-resolution real-time oscilloscope. In this case, the two ends of the SNSPD are directly fed to the input of the oscilloscope after amplification (Fig. 4-7(a)). This direct readout

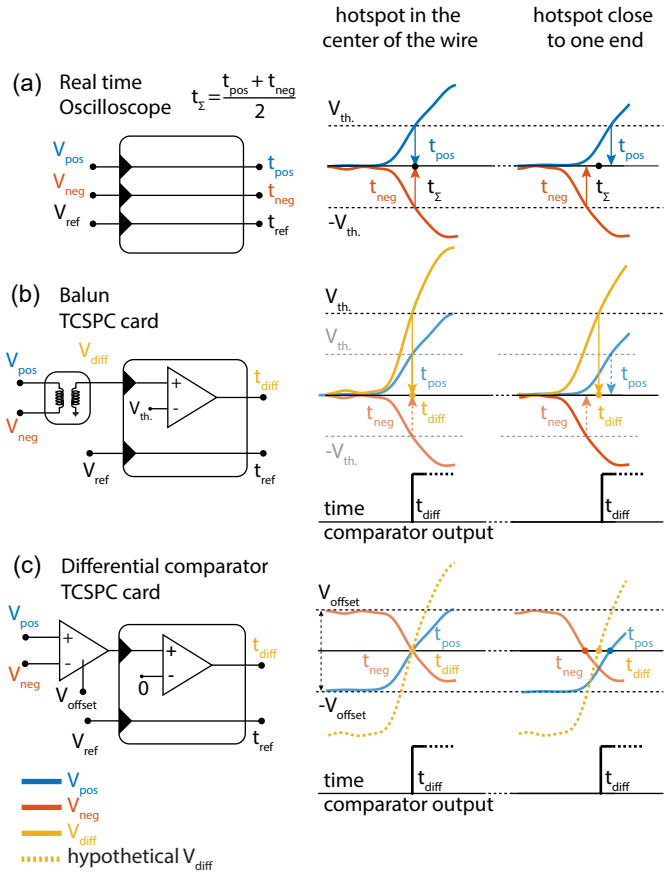

Figure 4-7: Sketch readout methods and pulse processing for our differential impedance-matched SNSPD. The pulses are shown for two arbitrary hotspot locations along the meander. (a) A high-resolution real-time oscilloscope is used to collect the complementary pulses. (b) After amplification, the complementary pulses are fed to the differential input of a balun that performs an analog difference of the pulses. The output is sent to the TCSPC module. (c) The complementary pulses are fed, after amplification, to the input of a differential comparator. The output is sent to the TCSPC module.

technique can provide the best timing resolution results. In particular, we can use cryogenic RF amplifiers at each end to minimize the electrical noise jitter. The oscilloscope trigger voltage V_{th} can be set to minimize the noise contribution by sampling the steepest point of the pulse [42]. Digitization noise can be reduced by maxing the sampling rate [42].

The direct readout provides access to the time tags of the complementary pulse, t_{pos} and t_{neg}. If the detection event happens at the exact center of the SNSPD (left side of sub-figure in Fig. 4-7(a)), and the system is perfectly balanced, there will be no geometric contribution and $t_{\text{pos}} = t_{\text{neg}} = t_{\Sigma}$. When the detection event happens elsewhere (right side of the sub-figure), the pulses arrive with a relative delay induced by the transmission line effect. In this case, t_{Σ} can be post-processed and used to compensate for the geometric jitter contribution as illustrated in Fig. 4-7(a).

4.4.2 Single-channel readout

For practical single-photon counting applications, an instantaneous measurement is required, and the use of two low-jitter time taggers for each differential detector becomes impractical in many situations. To overcome this limitation, we designed two readout schemes that make the differential detector compatible with a single-ended TCSPC module while maintaining the advantages of differential compensation of the geometric jitter. Fig. 4-7(b) and (c) show a comparison of the two approaches. Note that, due to additional electronic devices between the detector and the TDC, we expect the system jitter obtained with the single-channel readout to be slightly degraded compared to the direct two-channel readout, implemented with the real-time oscilloscope.

Balun + TCSPC

As previously shown in the simulation of Section 4.3, the geometric jitter can be compensated by processing the difference of the complementary pulses V_{diff}. In Fig. 4-7(b), we illustrate how a balun transformer can perform an equivalent analog difference of the complementary pulses. After amplification, the two sides of the detector are connected to the differential inputs of the balun, with the output being sent to a TCSPC module. The module will output a time tag t_{diff}. The threshold voltage of the module can be set to minimize the spread of time tag distribution, corresponding to the condition $t_{\text{diff}} \approx t_{\Sigma}$. The jitter extracted with this method, j_{diff}, represents the system jitter for this configuration.

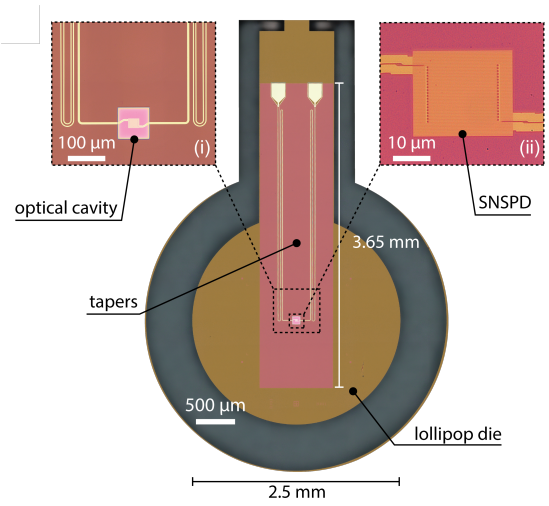

Figure 4-8: Differential impedance-matched superconducting nanowire single-photon detector. Optical micrograph of a representative device. The detector die (lollipop) is connected to the parent wafer before packaging. Inset (i): Optical micrograph of the detector embedded in an optical cavity. Inset (ii): Optical micrograph of the active area.

Comparator + TCSPC

Figure 4-7(c) illustrates the use of a differential comparator, or equivalently, a differential-input TCSPC module.[1] In this case, the differential comparator automatically cancels the geometric jitter, and no transformation of the pulses is required. To achieve optimum cancellation, a positive/negative offset is provided to the negative/positive pulse at the input of the differential comparator. When the difference between the two inputs becomes positive, the comparator generates a digital signal, with a rising edge slope limited by the slew rate of the comparator. This digital signal is time tagged by the TCSPC module producing the time tag t_{diff}. The offset voltage can be set to minimize the spread of the time tag distribution, matching the condition $t_{\text{diff}} \approx t_{\Sigma}$.

4.5 Device design and fabrication

This section shows the design and fabrication process of impedance-matched differential detectors. In particular, we describe several fundamental elements at the base of our architecture. Figure 4-8 shows an optical micrograph of one of the fabricated devices before packaging. Note that the detectors are designed for fiber-coupling through a self-aligned

[1] Some TCSPC modules allow feeding a differential input and include a comparator in the internal circuitry.

ID	type	width	pitch	active area/length	# squares	L-ratio
A	meander	100 nm	500 nm	$25 \times 20\,\mu m^2$	27545	37%
B	meander	100 nm	400 nm	$15 \times 10\,\mu m^2$	21295	18.4%
C	straight wire	120 nm	-	25 µm	17603	1.2%
D	meander	100 nm	500 nm	$22 \times 15\,\mu m^2$	24215	28%

Cavity λ	Cavity	NbN variant
1550 nm	Single	MIT
800 nm	Double	JPL
1550 nm	Single	MIT
1550 nm	Double	JPL

Table 4.2: Characteristics of a subset of devices representative of the design space. The device's size is also reported as the *number of squares*, useful to calculate the total inductance. Note that because most of the inductance is due to the impedance matching tapers, we also report the fraction of the inductance in the active area over the total inductance of the device (L-ratio).

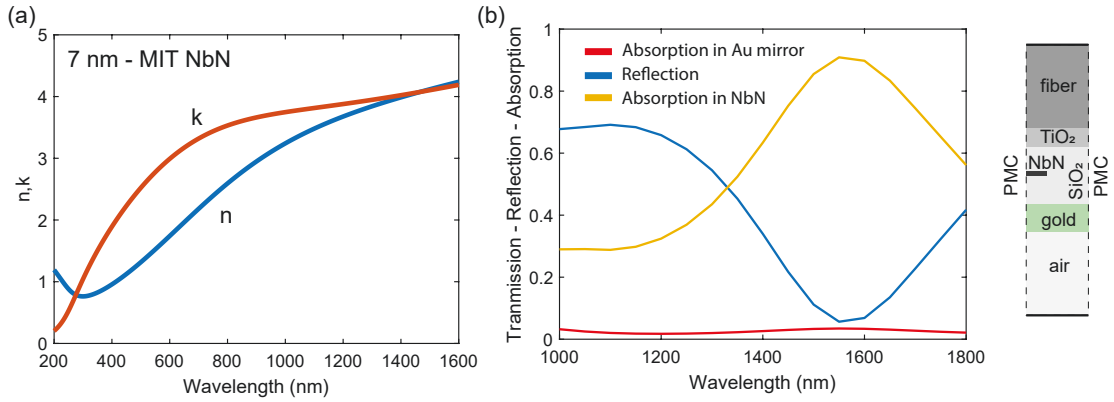

Figure 4-9: Design of optical stack for impedance-matched differential detector. (a) Refractive index of 7 nm-thick MIT NbN layer. (b) Characteristics of the single AR MIT optical stack: reflection, NbN and Au absorption. On the side is a sketch of the simulation setup.

packaging method using lollipop-shaped dies [133]. The active area consists of a standard meander embedded in an optical cavity to maximize photon absorption (inset (i) and (ii)). Both ends of the meander are interfaced with the readout through superconducting tapers extending along the die. We fabricated several devices using wafer-scale fabrication. In Table 4.2, we report the design details of a few samples whose characterization is reported in this thesis.

4.5.1 Optical stack design

As we mentioned in the introduction, the nanowire meander must be embedded in an optical cavity to maximize the SDE. The initial design of the optical stack for these devices was performed by Dr. Allmaras using the rigorous coupled wave analysis method (RCWA). Here, we verify the expected characteristics and absorption using COMSOL. The general structure of the optical stack consists of a bottom reflector mirror (gold), a first stack layer made with silicon dioxide ($n_{\mathrm{SiO_2}(1550\,\mathrm{nm})} = 1.44$, $t_{\mathrm{SiO_2}} = 243\,\mathrm{nm}$), the superconducting thin film, and finally, an antireflection (AR) coating. This project used two types of NbN superconducting films from two sources (MIT and JPL). We also experimented with single and double AR coatings designed for the two types of NbN (they have different refractive indexes). Here we report the simulation for the single AR coating designed for the MIT-type NbN. The AR coating consists of a silicon dioxide layer with $t_{\mathrm{SiO_2}} = 263\,\mathrm{nm}$ and a titanium dioxide layer with $t_{\mathrm{TiO_2}} = 187\,\mathrm{nm}$ and $n_{\mathrm{TiO_2}}(1550\,\mathrm{nm}) = 2.43$. In Fig.4-9(a) we show the refractive index (n,k) of our 7 nm-thick MIT NbN, measured with ellipsometry. In Fig.4-9(b), we show the simulation of the absorption in the NbN layer when embedded in the optical stack described above. The simulation assumes a normally incident TE wave launched from an optical fiber core ($n_{\mathrm{fiber}} = 1.47$). We used periodic boundary conditions and assumed a 100 nm-wide NbN nanowire with a 300 nm pitch. At 1550 nm, the cavity allows a maximum optical absorption in the NbN layer, of about 90%.

4.5.2 Microwave architecture and impedance-matching taper

The optical stack design also determines the properties of the transmission line architecture. The superconducting film is referenced to the ground (the gold mirror) through the 243 nm silicon dioxide layer.

Characteristics

In Fig. 4-10 we show the simulation of the characteristic impedance and velocity fraction as a function of the width of the nanowire. At 100 nm wide our nanowire has a characteristic impedance $Z_0 = 3.2\,\mathrm{k\Omega}$ and a velocity of $4.1\,\mu\mathrm{m/\,ps}$ (1.36% c) corresponding to an effective index $n_{\mathrm{eff}} = 74$.

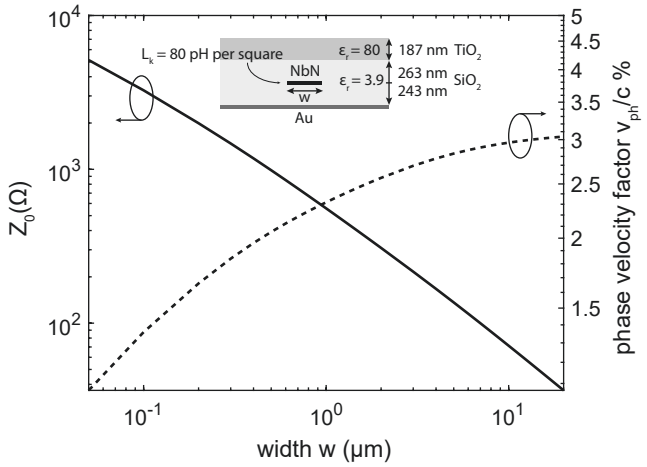

Figure 4-10: Simulation of the characteristic impedance and effective index/velocity for the nanowire transmission line architecture determined by the optical cavity design.

Impedance matching taper design

We designed an impedance-matching taper to interface the high-impedance nanowire transmission line to the 50 Ω readout. For convenience, we used the functions coded in the PHIDL CAD package [100]. We designed Hecken tapers with $B = 4.0091$ and a cutoff frequency of 536 MHz. The length of the taper was about 7.6 mm, and it meandered in 3 sections of about 2.5 mm each. To limit the size of the taper, we introduced an optimal curve transition section from 100 nm to 300 nm at both SNSPD ends. Effectively the tapers matched an impedance of about 1.795 kΩ. While this transition might introduce some reflections, it represents a necessary trade-off to limit the device's size.

4.5.3 Fabrication process

The fabrication process of our differential impedance-matched SNSPDs was performed in tandem at MIT and JPL. At MIT, we performed the superconducting layer deposition (MIT variant), all the electron beam lithography steps, and the etching for the MIT NbN variant. At JPL, we performed the superconducting deposition process (JPL variant), the optical lithography processes, the depositions of optical cavity layers, and the etching processes (JPL variant + release etch).

We fabricated our differential SNSPDs on 100 mm silicon wafers, to obtain about 200 devices per wafer. We first patterned the bottom reflector using a positive-tone photolithog-

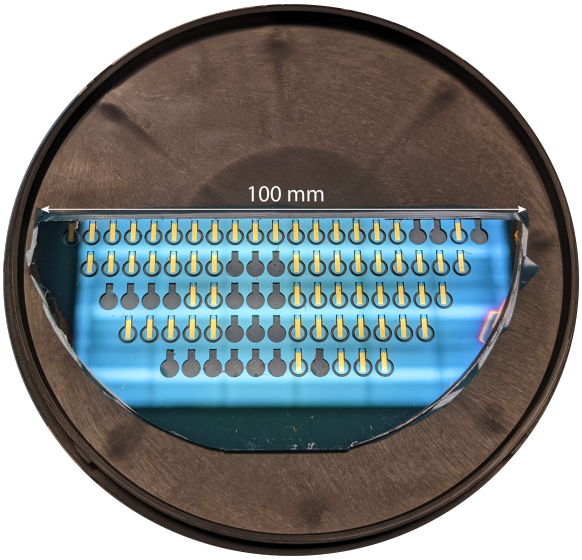

Figure 4-11: Lollipop devices wafer after fabrication.

raphy process on a Canon EX3 DUV stepper, followed by liftoff. The reflector consists of a Ti/Au/Ti stack, with 80 nm thick Au and 2 nm Ti for adhesion. Au was selected for the good mirror properties at 1550 nm. The first layer of the cavity (SiO_2) was blanket RF-bias sputtered on top of the mirrors. The JPL and MIT NbN superconducting layers were deposited at the two institutions by reactive-sputtering a Nb target in a N_2/Ar gas mixture, while applying RF-bias to the substrate to reduce the grain size in the films following Ref. [96]. Both processes were calibrated to obtain 7 nm-thick films. We next fabricated Ti/Au/Ti bond pads, using ion milling prior to Ti/Au/Ti e-beam evaporation to produce good contact with the NbN. We employed electron-beam lithography to write the nanowires and tapers simultaneously. The wafer with JPL NbN used a negative-tone resist, while the MIT wafer used a positive-tone resist. These electron beam lithography processes are available in Appendix A. The JPL NbN films were etched in a mixture of $CCl_2F_2/CF_4/O_2$ in an inductively coupled plasma reactive ion etcher (ICP-RIE), while MIT were etched in a CF_4 plasma in a RIE system. A blanket film of ≈ 100 nm of SiO_2 was deposited to protect the SNSPDs immediately after this etch and the removal of the e-beam photoresist in solvent baths. We then exposed a liftoff pattern in the stepper to define the remainder of the anti-reflection (AR) stack above the active area of the SNSPDs but away from the bond pads, to avoid wire bonding through thick dielectrics. The AR stacks on each of the three wafers were designed and simulated using refractive indices data of each layer and designed to maximize

Reference	Instrument
Cryogenic LNA	CMT LF1S (1 MHz – 2 GHz)
Real-time oscilloscope	Keysight DSOZ634A (63 GHz)
Differential Amplifier	Analog Devices LTC6432-15 (100 kHz – 1.4 GHz)
Balun board	Texas Instruments ADC-WB-BB/NOPB (4.5 MHz – 3 GHz)
Cryogenic Comparator	Analog Devices HMC675LP3E
Inductive shunts	Custom: 1.1 μH + 50 Ω
Room temperature amplifiers	Mini Circuits ZX60-P103LN+ (50 MHz – 3 GHz)
TCSPC module	Becker & Hickl SPC-150NXX
Photodiode	New Focus 1014 (45 GHz)
Pulsed Laser	Calmar Mendocino 1550 nm 10 MHz repetition rate
Universal Counter	Keysight 53220A
Amplitude Modulator	iXblue MXER-LN-20

Table 4.3: Overview of the instruments for the measurement setups shown in Fig. 4-12

efficiency at design wavelengths (1550 nm or 775 nm). For two of the wafers, we fabricated a one-layer AR stack of SiO_2/TiO_2. For the third wafer and fourth wafer considered here, we used a double-layer AR stack of SiO_2/TiO_2 to produce a narrower band around 1550 nm and 775 nm. The one-layer AR stack was 271 nm/167 nm (SiO_2/TiO_2) for one wafer with the JPL NbN film. Meanwhile, a wafer with MIT NbN had a stack of 263 nm/184 nm. The thicknesses differed due to the difference in refractive indices between the JPL and MIT NbN films. The two-layer AR stack on the other wafer with JPL NbN was approximately 150 nm/279 nm/157 nm/262 nm ($SiO_2/TiO_2/SiO_2/TiO_2$). Next, we wrote an etch-back pattern with the stepper and used the ICP-RIE with CHF_3 and O_2 to etch through the blanket SiO_2 and spacer SiO_2. Finally, we exposed an etch-back pattern and used deep reactive ion etching (DRIE) to define the lollipop pattern for self-alignment to single-mode optical fibers [144]. Figure 4-11 shows a piece of the wafer containing several lollipop dies before packaging.

4.6 Measurement Setup

This section describes the experimental setup used to characterize our differential detectors. Figure 4-12 shows the sketch of three different setups and Table 5.2 provides an overview of the instrumentation. In all the setups, the detectors were biased with a fully differential circuit. Moreover, to bias as close as possible to switching current and avoid latching at high photon fluxes, cryogenic inductive shunts were added at both ports.

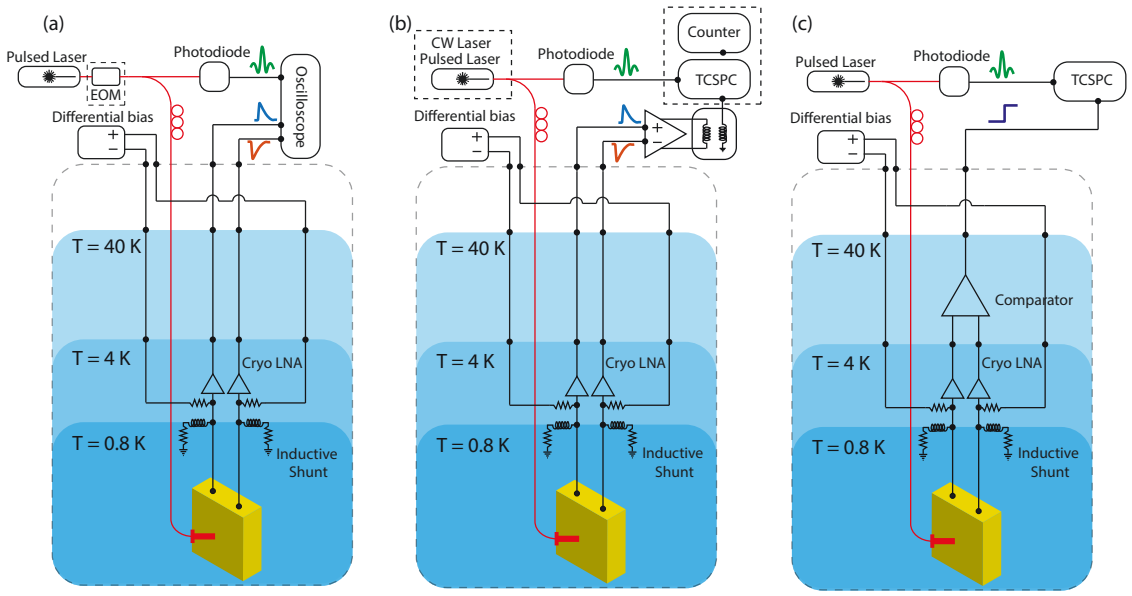

Figure 4-12: Measurement setups. (a) Measurement setup for the characterization of the detector pulses, detector jitter t_Σ, differential time t_Δ-histogram, and photon-number resolution. (b) Measurement setup for the characterization of the system detection efficiency and for the measurement of the system jitter j_{diff} using the balun in combination with the TCSPC module. (c) Measurement setup for the characterization of the system jitter j_{diff} using the cryogenic comparator in combination with the TCSPC module.

Figure 4-12(a) shows the experimental setup used for the characterization of the detector pulses, system jitter t_Σ, differential time t_Δ-histogram, and photon-number resolution capabilities. Thanks to the impedance-matched design of the detectors, the signal amplitude is significantly increased by as much as a factor of three compared to a regular SNSPD [139]. This produces a signal amplitude of a few millivolts for both positive and negative pulses. We used single-stage high-dynamic range cryogenic amplifiers developed for this device. After amplification, the detector outputs are directly interfaced with a real-time oscilloscope to acquire the pulse traces. The trigger was set on the steepest part of the pulse-rising edge to improve the SNR and reduce the impact of the electrical noise. The oscilloscope sampling rate was set to $80 \times 10^9\,\text{s}^{-1}$ to minimize quantization error. The analog bandwidth was set to 6 GHz [42]. For measuring the PNR capabilities, the pulsed laser repetition rate was reduced to 1 MHz using an intensity modulator.

The setup shown in Fig 4-12(b) was used for the characterization of the system detection efficiency and the measurement of the system jitter j_{diff} using the balun in combination with the TCSPC module. After amplification with the cryogenic low noise amplifier, the detec-

ID	T_c	I_{sw}
A	7.9 K	14.6 μA
B	6.8 K	22.0 μA
C	7.9 K	22 μA
D	6.4 K	20 μA

Table 4.4: Critical temperature and switching current for selected devices.

tor outputs undergo a further amplification stage through a low noise differential amplifier. This is necessary to improve the signal level before the balun, which has a 6 dB insertion loss. From the differential amplifier, the outputs are connected to the balun board, which performs the difference of the complementary pulses. For the characterization of the detection efficiency, the balun's output was connected to a universal counter. The detection efficiency was characterized after a calibration of the optical path losses. To measure the system jitter j_{diff}, the balun's output was connected to the TCSPC module together with a synchronization signal from the pulsed laser obtained with a fast photodiode.

The setup shown in Fig 4-12(c) was used for the characterization of the system jitter j_{diff} using the cryogenic comparator in combination with the TCSPC module. After amplification with the cryogenic low noise amplifiers, the detector outputs are fed to the differential comparator. The electronic circuit consists of a SiGe current-mode logic comparator thermalized at the 40 K stage of the cryostat. The offset of the input pulses is achieved with a pair of bias tees between the cryogenic amplifiers and the comparator. The output from the comparator is connected to the TCSPC module and the synchronization signal.

4.7 Main results

In this section, we show and discuss the results for the selected devices in Table 4.2.

4.7.1 DC properties

All the devices were tested for switching current I_{sw} and critical temperature T_{C}. The extracted data are reported in Table 4.4. Overall, all of our devices achieve a switching current approaching or higher than 15 µA and critical temperatures higher than 6 K, making them compatible with most state-of-the-art detector refrigeration systems (1 K to 3 K operation).

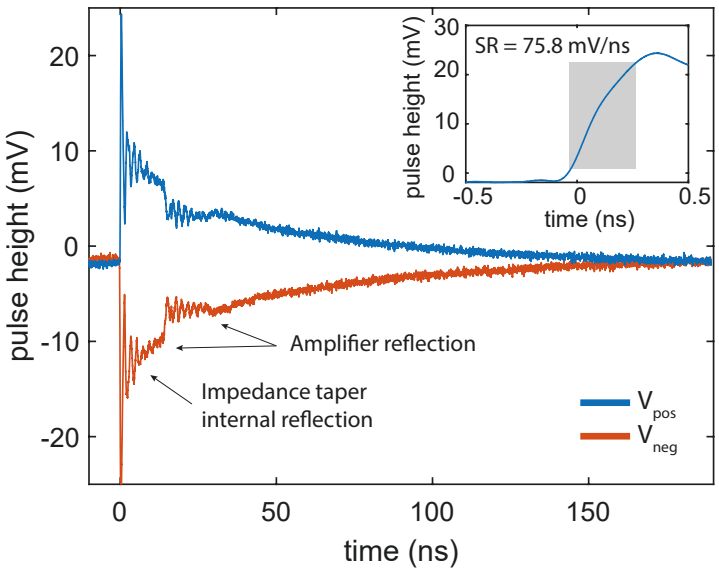

Figure 4-13: Differential pulses from impedance-matched detector A.

4.7.2 Characteristic pulses

Fig. 4-13 shows the output differential pulses from detector A. There are several features in the pulse worth discussing. First, the reset time is approximately $3\tau = 160\,\text{ns}$, consistent with the characteristic $\tau = L/R$ time constant for detector A. Second, the fast ripple on the exponential decay is due to the limited bandwidth of the impedance-matching tapers. Finally, the two primary reflections are due to the amplifier's impedance mismatch. In the inset of Fig. 4-13 we show the pulse slew rate SR $= 75.8\,\text{mV/ns}$, in agreement with our previous results with single-ended impedance-matched detectors [139].

4.7.3 System detection efficiency

We discuss the measurements and estimation of the system detection efficiency of our detectors.

Calibration routine and uncertainty

The system detection efficiency is estimated as

$$\text{SDE} = \frac{\text{count rate}}{\text{photon flux}}. \tag{4.10}$$

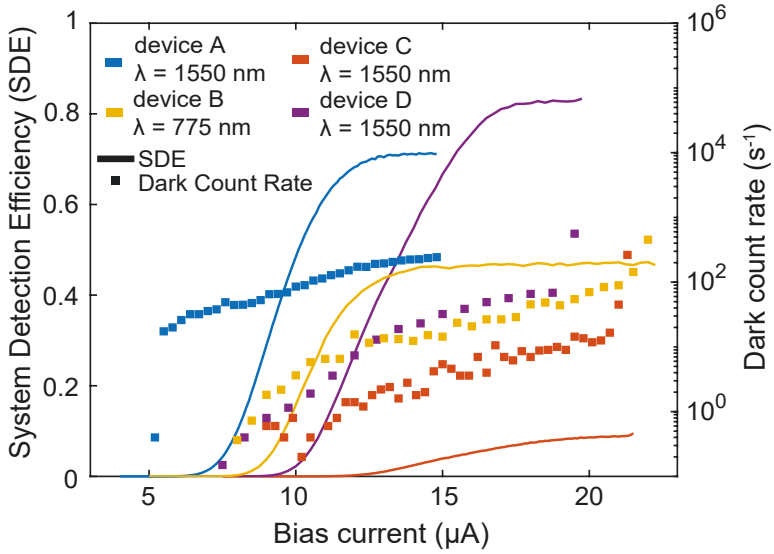

Figure 4-14: Differential pulses from our impedance-matched detector A

where the count rate is given by the measured light count minus the dark counts of the detectors. We assume the uncertainty on the count rate to be negligible. The photon flux is estimated as:

$$\text{photon flux} = \frac{P_0 A_1 A_2 A_3}{E_\lambda} \tag{4.11}$$

where P_0 is the input optical power, measured with a calibrated power meter, A_{1-3} are the values of three optical attenuators used to attenuate the optical power, and E_λ is the energy of the photon of wavelength λ. To measure the attenuation ratios A_{1-3}, the attenuators are connected in series and interfaced to the calibrated power meter through an optical switch. To measure the attenuation ratio, we set one of the attenuators to the desired values and the others to 0 dB. We measure the attenuated output power and repeat the procedure for the other attenuators. A_{1-3} results from a relative optical power measurement using the same power meter. Therefore, to estimate the uncertainty on A_{1-3} we only consider the relative uncertainty due to the non-linearity $\sigma_{\text{NL}}(P)/P = 0.5\%$, on each measurement. The total uncertainty on the SDE is dominated by the power meter uncertainty $\sigma(P)/P = 5\%$, and it is approximately $\sigma(\text{SDE})/\text{SDE} = 5.2\%$.

System detection efficiency

In Fig. 4-14, we show the measured SDE curves and the dark count rate. We want to explicitly highlight a few details on these results.

- **Large saturation plateaus** All our detectors achieve saturated detection efficiency with significant plateau width (about 25% of the current range). In the saturation region, the internal detection efficiency approaches unity, and the overall system efficiency is limited by coupling and absorption losses. We note that in this saturation region, the SNSPD will be insensitive to bias noise with high stability characteristics.

- **Dark count rate** In all our devices, the dark count rate is limited to about 100 counts per second. It is interesting to point out the direct proportionality between the active area and dark counts. Device A has the largest area, hence the largest dark count rate. Device D, is a single wire and has the lowest dark count rate. This linear dependence is expected from the dynamics of the dark count rate in superconducting nanowire single-photon detectors, indicating the absence of spurious counts or dynamics.

- **SDE results** Detectors A and D achieve $71.1\% \pm 3.7\%$ and $83.3\% \pm 4.3\%$ SDE, respectively. These two detectors have the largest area and can effectively collect most of the coupled light. The SDE results are in agreement with the optical stack design and represent state-of-the-art efficiency for SNSPDs. Detector D is just a single wire and achieves $8.8\% \pm 0.5\%$ efficiency, collecting just a small portion of the coupled light. Detector B, designed for 775 nm only achieves $47.6\% \pm 2.5\%$ even if embedded in a cavity with double AR coating. We would have expected a better SDE result from this detector. We investigate the origin of this result in the next sections.

4.7.4 System jitter

Here we report and discuss the measurement and results of the system jitter, characterized with the three setups described above.

Two-channel system jitter (j_Σ)

We first characterized the system jitter using the direct two-channel readout approach with the fast real-time oscilloscope. Each jitter value was obtained by processing about 120k

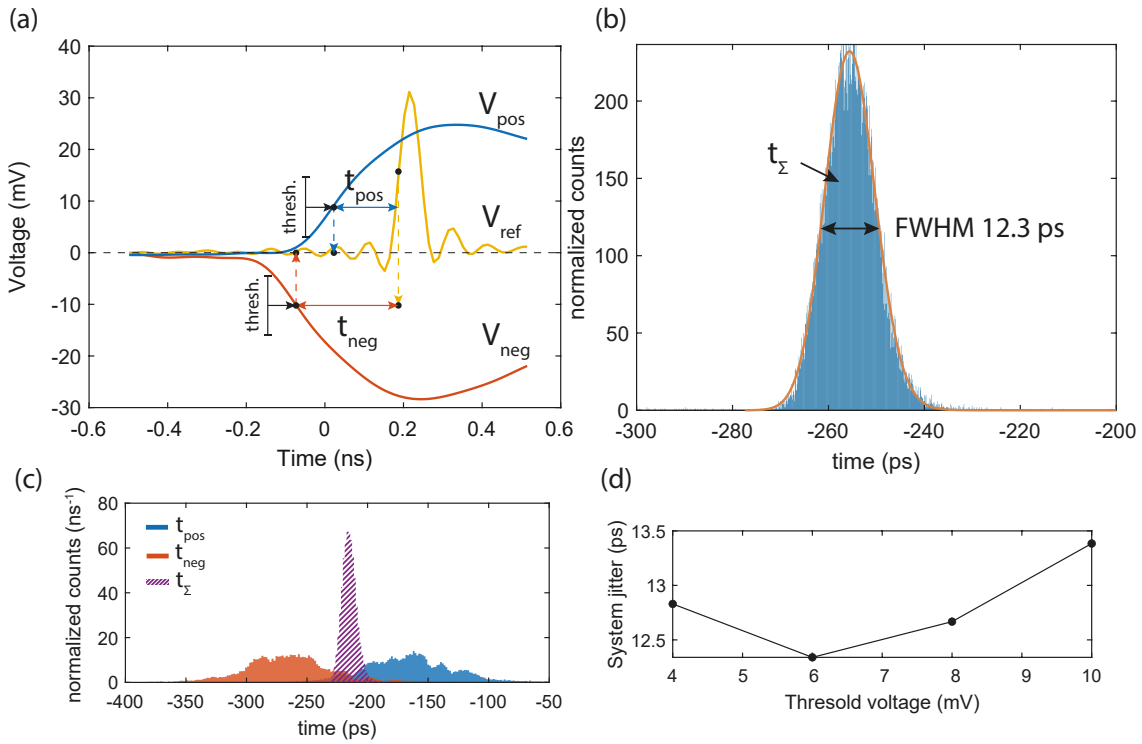

Figure 4-15: Calculation of system jitter. (a) Tagging procedure. (b) Estimation of jitter value from a Gaussian fitting of t_Σ distribution. (c) Visual comparison of tags distributions. (d) Study of jitter versus threshold value used to tag the complementary pulses.

detection event traces. Here we describe the tagging procedure for a single detection event. We acquire the rising edge portion of the differential pulse traces and the reference optical signal from the fast photodiode. We then extract the raw time tags from both detector pulses ($t_{\text{pos,raw}}$ and $t_{\text{neg,raw}}$) and the reference signal (t_{ref}). We reference the pulse time tags to the optical signal: $t_{\text{x}} = t_{\text{x,raw}} - t_{\text{ref}}$, where x labels the positive or negative pulse. The tagging procedure is visually shown in Fig.4-15(a). We use these normalized time tags to calculate t_Σ as described in Sec.4.2.2. To extract the system jitter, we fit the histogram of all the t_Σ using a Gaussian distribution, and we calculate the FWHM, as shown in Fig.4-15(b). The FWHM represents the system jitter, j_Σ. This procedure is repeated for several bias points. To visually show the impact of using t_Σ versus single-end time-tags, in Fig.4-15(c) we plot and compare the histrograms of t_{pos}, t_{neg}, and t_Σ. We note the width of the distribution of t_Σ is much narrower than the single time-tags. We also would like to mention an important detail. To extract the reference signal tag, we use a threshold voltage corresponding to the steepest point of the trace. In this way, we minimize the impact of the electrical noise (j_{amp}).

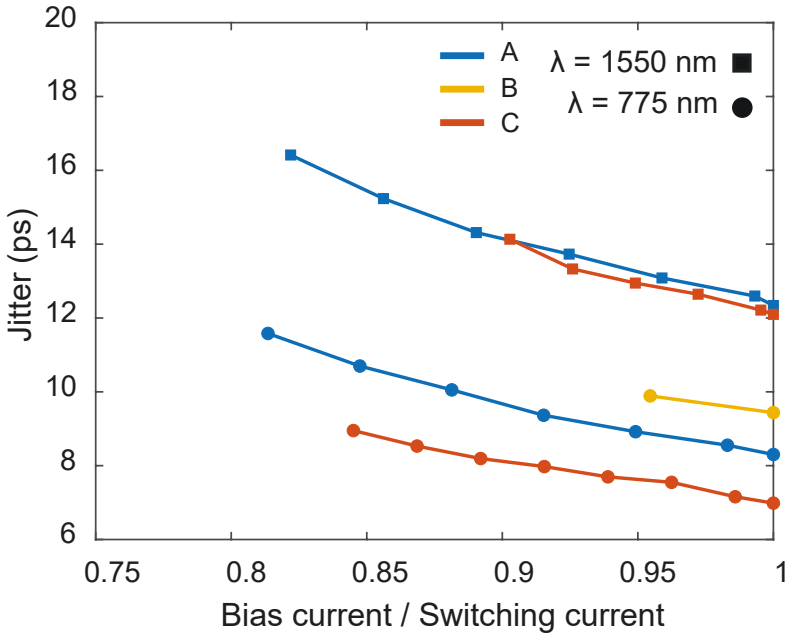

Figure 4-16: System jitter j_Σ with bias current, for different detectors and wavelengths.

We should use the same rationale for the detector pulse tagging. However, we decided to explicitly investigate the impact of the pulse threshold on the system jitter. Fig.4-15(d) shows the dependence of the system jitter on the threshold value for detector A. The values reported in this thesis are taken with the threshold value giving the lowest system jitter.

In Figure 4-16, we show the value of the system jitter calculated as described above for several detectors, wavelengths, and bias points. The bias current is normalized by the switching current reported in Table 4.2. We would like to discuss a few important highlights from these results:

- **System jitter at** $\lambda = 1550\,\text{nm}$. We tested the system jitter for detectors A and C at their cavity wavelength 1550 nm. It's interesting to note that while detectors A and C have very different geometric designs, they achieve similar system jitter values, about 12 ps. This result is remarkable as it shows the effectiveness of the differential readout in canceling the geometric jitter. This result also indicates that at 1550 nm, we are observing the intrisic contribution to teh timing jitter.

- **System jitter at** $\lambda = 775\,\text{nm}$. We measured detector B at its stack wavelength, 775 nm. The system jitter is 9.4 ps. We also measured detectors A and C at this

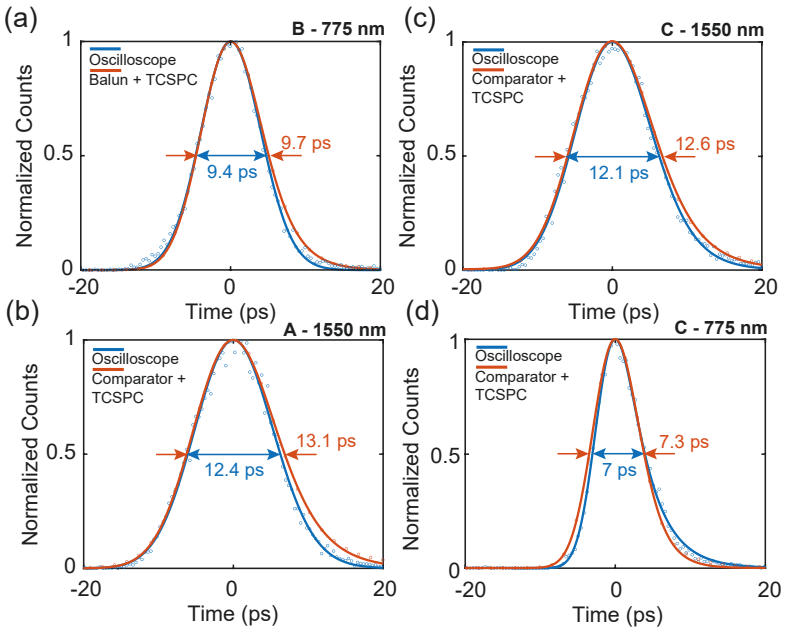

Figure 4-17: Comparison of system jitters acquired with different setups and methods. (a-d) Direct comparison of the system jitter acquired with a real-time oscilloscope, and with one of the cancellation methods described in previous sections.

wavelength obtaining 8.3 ps and 7.0 ps jitters, respectively. At 775 nm, our detectors all break the 10 ps barrier. This remarkable result shows that a large area detector can approach low jitters, breaking the traditional metric trade-off.

The lower jitter achieved with shorter wavelengths is expected, based on the latency dynamics in the detection process [136, 42].

One-channel system jitter

We used the setup described in Sec. 4.4.2 to characterize the system jitter j_{diff}, in case of single-ended configurations. As mentioned above, with optimized parameters j_{diff} is expected to converge to j_{Σ}.

Figure 4-17 compares the distribution of t_{Σ} with t_{diff} obtained with the methods described Sec.4.4.2. The proposed acquisition schemes achieve a j_{diff} only 3 % to 6 % higher than j_{Σ}, demonstrating that both methods achieve effective cancellation of the geometric jitter equivalent to the oscilloscope-based acquisition, while minimally affecting the overall timing resolution. The uncertainty on these values is estimated as two time-bins $\sigma_{\text{TCSPC}} = 0.4$ ps. This opens up the possibility of using the detection system for photon-counting applications

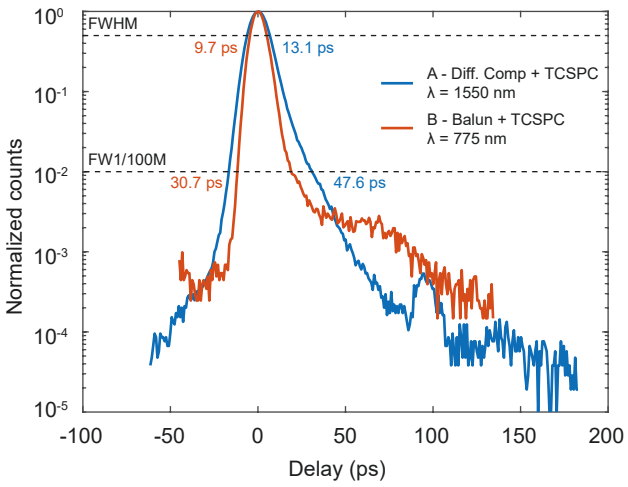

Figure 4-18: Characterization of the FW1/100M for detectors A and B.

with high detection efficiency and sub-10 ps system jitter while operating at count rates in the MHz range, something that is not possible with oscilloscope-based data acquisition and that has not been achieved previously for the wavelengths in question.

FW1/100M

In applications such as quantum key distribution or pulse-position modulated optical links, in order to achieve a low error rate and a high clock rate [145, 146, 147], an instrument response function with low spread over several orders of magnitudes (high dynamic range) is required. In addition to a low system jitter (FWHM of the timing response), this characteristic is quantified by the full width at one-tenth-of-maximum (FWTM) and one-hundredth-of-maximum (FW1/100M) of the instrument response function. These metrics measure the width of the distribution tails and represent *second-order* system jitters, extremely significant in certain applications. For example, in fluorescent lifetime imaging, a large FW1/100M can limit the contrast, while in time-resolved spectroscopy, it can affect the dynamic range [148, 149]. Figure 4-18 shows that our differential Detector A, in combination with the differential comparator and the TCSPC module, achieves 47.6 ps ± 0.4 ps FW1/100M at 1550 nm, which is a factor of four lower than what has been achieved with free-running InGaAs/InP single photon avalanche diodes (SPAD) operating at the same wavelength [147]. At 775 nm, Detector B combined with the balun and TCSPC module, achieves 30.7 ps ± 0.4 ps FW1/100M, which is a factor of seven lower than the best demonstration with red-enhanced silicon

ID	System Efficiency	System Jitter (osc)
A	71.1% ($\lambda = 1550\,\text{nm}$)	12.4 ps
B	47.6% ($\lambda = 775\,\text{nm}$)	9.4 ps
C	8.8% ($\lambda = 1550\,\text{nm}$)	12.1 ps
D	83.3% ($\lambda = 1550\,\text{nm}$)	-

Cancellation Method	System Jitter (method)	Difference
Diff. Comparator	13.1 ps	5.6%
Balun	9.7 ps	3.2%
Diff. Comparator	12.6 ps	4.1%
Balun	13.0 ps	-

Table 4.5: Summary of experimental results. Note that Device D was not measured with the real-time oscilloscope method.

SPADs [149]. These metrics position our differential detector for application in biomedical imaging [124, 125], quantum communication [28] and laser ranging [122], where the most stringent timing performance is required over an extensive dynamic range.

To conclude this section, in Table 4.5, we summarize the best result for the detectors studied here.

4.8 Additional capabilities

This section describes a secondary set of results from our detectors. Thanks to the differential impedance-matched architectures, our device demonstrates additional capabilities which are generally not available with standard SNSPDs.

4.8.1 Imaging capabilities

As mentioned in Sec.4.2.2, [135, 54], $t_\Delta = t_{\text{pos}} - t_{\text{neg}} = \frac{2x_\text{p} - L}{v_\text{ph}}$ encodes the spatial coordinate of the photon detection location x_p on the nanowire (Fig. 4-19(a)); L is the total length of the meander. Thanks to the covered microstrip design, the signal propagation velocity is low enough to use t_Δ to determine the photon absorption locations along the nanowire meander. With a velocity of about 4.1 µm/ ps, it takes approximately 6.1 ps for the signal to traverse a single meander. This delay can be resolved with high-resolution time taggers, and these detectors can achieve imaging capability by time-multiplexing adjacent locations on the meander.

To showcase this method, we first simulated the imaging capability of the detector for

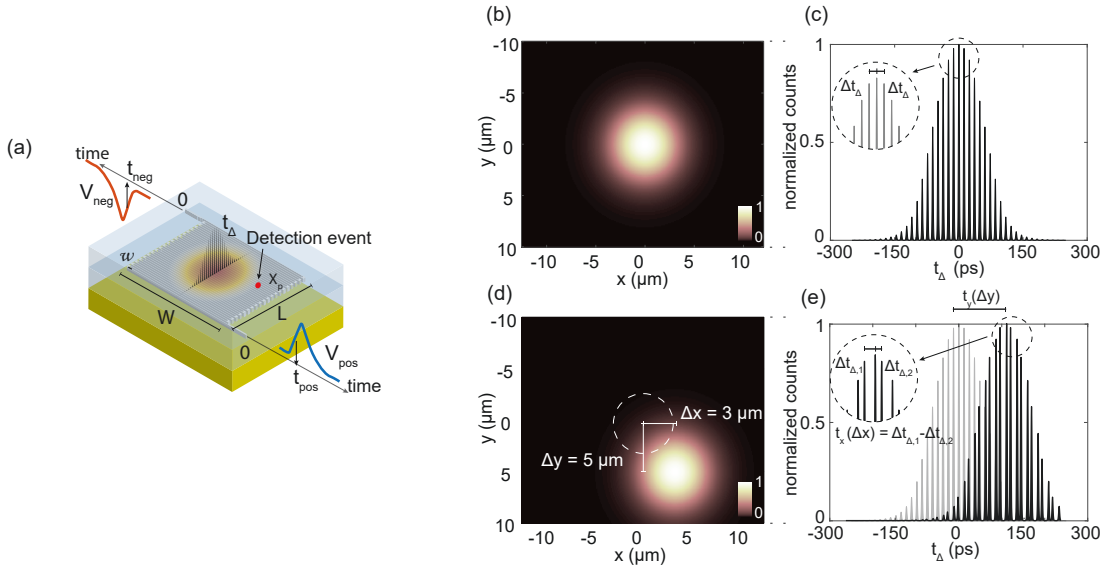

Figure 4-19: Detector imaging capabilities. (a) Detector model. (b-c) Simulation of a LP01 mode centered on the active area of the detector and the pulse distribution histogram expected from this illumination condition. (c-d) Simulation of a LP01 mode on the detector active area, with a certain shift $(\Delta x, \Delta y)$, and the pulse distribution histogram expected from this illumination condition.

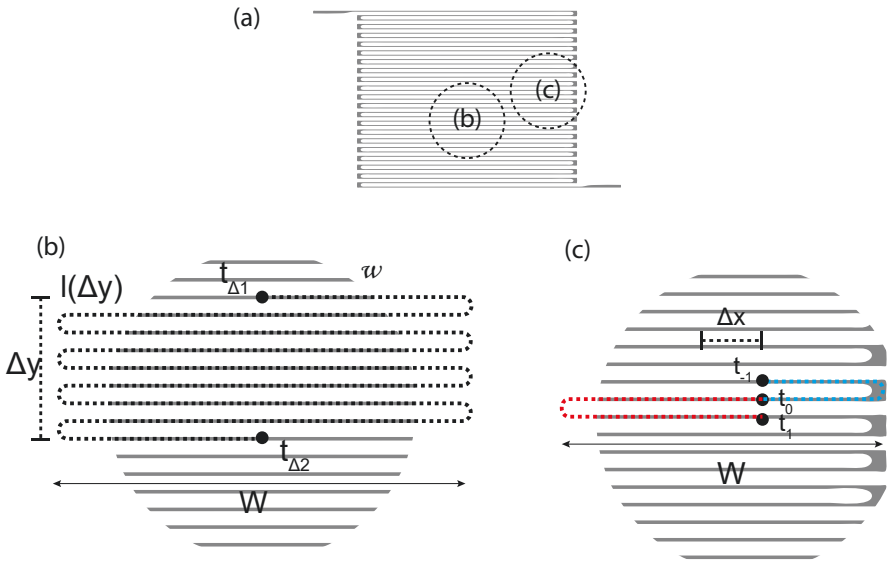

Figure 4-20: Illustration for the reconstruction of the illumination shift on the active area. (a) Example treated. (b) Case for vertical misalignment. (c) Case for horizontal misalignment.

the lowest-order mode LP01 of a single-mode fiber at 1550 nm. The mode is assumed to land on the SNSPD without spreading or distortions, maintaining the same size as at the end of the fiber. Figure 4-19(c) shows the simulated distribution of the differential time t_Δ when the center of the optical mode coincides with the center of the detector (Fig. 4-19(b)). Each sub-distribution of the histogram corresponds to detection events from consecutive wires in the meander. Because the mode is aligned with the center of the meander, the spacing between adjacent sub-distributions is constant, and the peak of the envelope of the t_Δ-distribution (t_y) is located at 0 ps.

When the mode and the detector centers are misaligned (e.g. $\Delta x = 3\,\mu\mathrm{m}$ and $\Delta y = 5\,\mu\mathrm{m}$ in Fig. 4-19(d)) the histogram shows two characteristic features (Fig. 4-19(e)). First, t_y does not coincide with $t_\Delta = 0$. Second, the relative spacings between adjacent peaks, $\Delta t_{\Delta,1}$ and $\Delta t_{\Delta,2}$, are not identical.

We show that by analyzing these features one can reconstruct the mode misalignment on the active area. In Fig. 4-20(b) we analyze the condition in which the mode is vertically misaligned. In general:

$$\begin{aligned} t_{\Delta,1} &= \frac{L_\mathrm{m} - 2x_\mathrm{p}}{v_\mathrm{ph}}, \\ t_{\Delta,2} &= \frac{L_\mathrm{m} - 2(x_\mathrm{p} + l(\Delta y))}{v_\mathrm{ph}}, \end{aligned} \tag{4.12}$$

where $l(\Delta y) = W\frac{w\Delta y}{\mathrm{FF}}$ is the linearized length on the meander corresponding to Δy, as shown in the Fig.4-19(a). Here, w is the width of the nanowire, W the width of the meander, and FF the meander fill-factor. The time-domain shift associated to $l(\Delta y)$ is

$$t_\mathrm{y} = t_{\Delta,2} - t_{\Delta,1} = \frac{2l(\Delta y)}{v_\mathrm{ph}} = \frac{2W}{v_\mathrm{ph}}\frac{w\Delta y}{\mathrm{FF}}. \tag{4.13}$$

When $\Delta y = 0$, the peak of the envelope of the t_Δ-histogram is at $t_{\Delta,1} = 0$. By rearranging Eq. 4.13 we obtain a first order formula to evaluate the vertical shift in function of the peak of the envelope of the t_Δ-distribution. Note that this derivation assumes $\Delta x = 0$, and it's therefore accurate within one meander pitch. In Fig. 4-20(c), we analyze the situation in

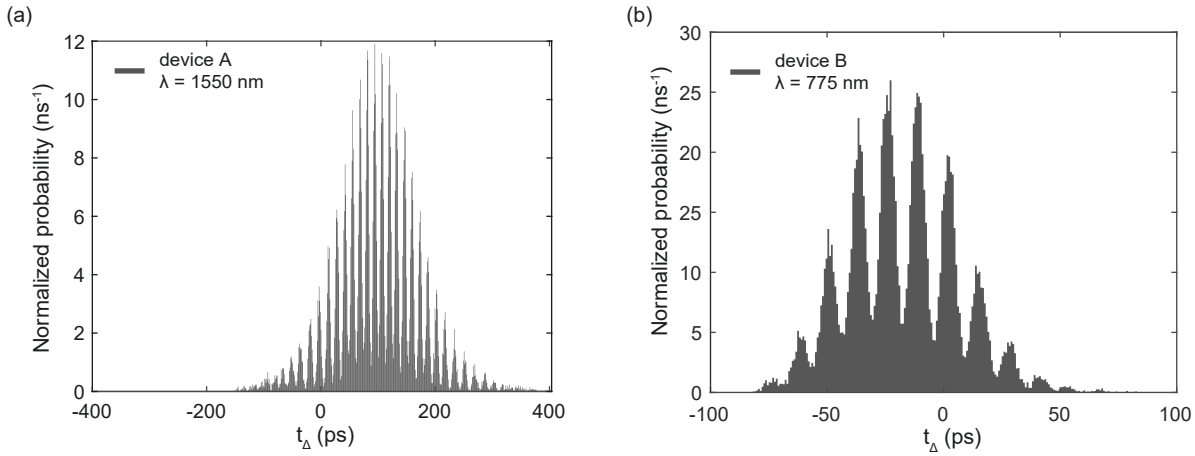

Figure 4-21: Analysis of the output histograms of detector A and B, exploiting the imaging capabilities of our architecture. (a) Detector A: small vertical shift. (b) Detector B: the mode is shifted toward the lower corner of the device and highly impacts the efficiency of the detector.

which the mode is horizontally misaligned. In general

$$\begin{aligned} t_{\Delta,0} &= \frac{L_\mathrm{m} - 2x_\mathrm{p}}{v_\mathrm{ph}}, \\ t_{\Delta,-1} &= \frac{L_\mathrm{m} - 2\left[x_\mathrm{p} - (W - 2\Delta x)\right]}{v_\mathrm{ph}}, \\ t_{\Delta,1} &= \frac{L_\mathrm{m} - 2\left[x_\mathrm{p} + (W + 2\Delta x)\right]}{v_\mathrm{ph}}. \end{aligned} \tag{4.14}$$

The relative difference between adjacent histogram sub-peaks is:

$$\begin{aligned} t_x &= \Delta t_{\Delta,1,0} - \Delta t_{\Delta,0,-1} \\ &= (t_{\Delta,1} - t_{\Delta,0}) - (t_{\Delta,0} - t_{\Delta,-1}) \\ &= t_{\Delta,1} - 2t_{\Delta,0} + t_{\Delta,-1} \\ &= \frac{8\Delta x}{v_\mathrm{ph}}. \end{aligned} \tag{4.15}$$

By rearranging Eq. 4.15 we obtain a first order formula to evaluate the horizontal shift in function of the relative difference between adjacent histogram sub-peaks.

Figure 4-21(a) shows the t_Δ-distribution for Detector A illuminated with the 1550 nm pulsed laser fiber coupled to the detector through a single-mode fiber. The misalignment is estimated from fitting the distribution with Gaussian functions: $\Delta x = -0.01\,\mu\mathrm{m}$ and $\Delta y = 3.74\,\mu\mathrm{m}$. The fraction of the mode collected by the active area was 99.7 %. This

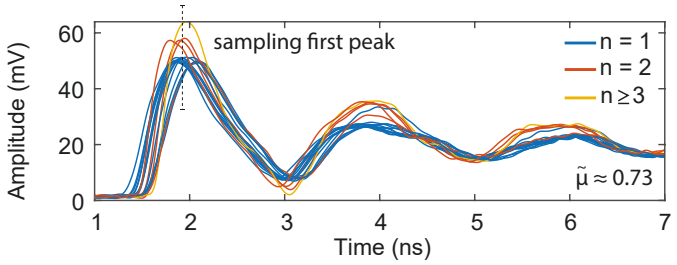

Figure 4-22: Photon number resolution. Representative V_{diff} traced for a mean photon number of 0.73.

analysis confirms that the SDE is limited to $\approx 70\%$ at 1550 nm by the meander fill-factor and cavity design.

Figure 4-21(b) shows the t_Δ-distribution for Detector B illuminated with the 775 nm pulsed laser fiber coupled to the detector through a single mode fiber. In this case, an inspection of the histogram reveals that the mode was strongly misaligned toward the lower corner of the meander. Combined with the smaller active area, the detector can only reach $\approx 47\%$ SDE. When aligned, the system detection efficiency should exceed 70 %, based on the Detector A characterization. We verified this by packaging a detector with a larger active area ($30 \times 10\,\mu\text{m}^2$) that relaxes the constraints on the fiber alignment. For this detector, the system detection efficiency was $78.0\,\% \pm 4.0\,\%$.

4.8.2 Photon number resolution

Recently, we demonstrated that an impedance-matched superconducting nanowire detector could reveal the number of photons detected simultaneously. This information was contained in the amplitude of the detection pulses [89].

The original demonstration was a single-ended SNSPD interfaced to the $Z_{\text{L}} = 50\,\Omega$ load through a 200 MHz Klopfenstein taper. When n photons are absorbed simultaneously a photon-number dependent hotspot resistance $R_{\text{hs}}(n)$ is generated. Thanks to the impedance matching structure, the output current to the load will be proportional to $\sqrt{\frac{Z_{\text{H}}}{Z_{\text{L}}}}\frac{R_{\text{hs}}(n)}{R_{\text{hs}}(n)+Z_H}$. Here Z_{H} has the same order-of-magnitude value as R_{hs}, and the current divider value is sensitive to n. For this reason, by processing the output amplitude, it is possible to reconstruct n value. Here, the same simple picture can be applied. Still, the differential character of the detector encodes the photon-number information in the amplitude of the difference of the pulses from the two ends, V_{diff}.

We characterized the photon-number resolution capability using an attenuated 1550 nm pulsed laser with a repetition rate of 1 MHz. We used an intensity modulator to reduce the repetition rate and allow our detector to fully reset. Figure 4-22 shows representative traces of the difference of the output pulses for an effective mean photon number $\tilde{\mu} = 0.73$. This number was estimated from the photon rate at the cryostat input port, scaled by the system efficiency

$$\tilde{\mu} = \frac{\text{photon rate}}{\text{rep. rate}} \text{ SDE} \tag{4.16}$$

The pulse amplitude distribution sampled on the first peak (dashed line in Fig. 4-22) is shown in Fig. 4-23. In the same figure, we also show the distribution for other mean photon numbers. Each distribution was fitted with up to four Gaussian functions. The fourth Gaussian was introduced to fit the distribution for $\tilde{\mu} = 3.7$. For every effective mean photon number, the left shoulder was excluded from the fit. Our detector can distinguish up to $n = 3$ photons. The separation between the one- and two-photon distributions is more than 9 standard deviations of the one-photon distribution width $\sigma_{n=1}$ ($9\sigma_{n=1}$), making this detector suitable for application in quantum optics experiments.

To verify the correct estimation of the photon number, in Fig. 4-24 we plot the counting probability $Q(n)$, extracted by integrating the area under each Gaussian distribution, together with the photon statistics of the coherent source $S(n) = e^{-\tilde{\mu}}\tilde{\mu}^n/n!$ (line). We grouped the probability for the events with $n \geq 3$, which are not clearly separated. Note that in the figure we normalized the theoretical $S(n)$ by the probability of zero photons $S(n)/(1-S(0))$ where $S(0) = e^{-\tilde{\mu}}$. Further details on the procedure are available in Ref. [89]. We can observe good agreement between our reconstructed statistics and the theoretical expectation, confirming that our detector achieves PNR capabilities.

4.9 Summary

In this chapter, we demonstrated that by redesigning the architecture of the SNSPD and with an appropriate readout scheme, the trade-off between detection efficiency and system jitter can be overcome. At 775 nm we achieved 9.7 ps±0.4 ps system jitter with 47.3 %±2.4 % system detection efficiency, limited by fiber alignment (Detector B). At 1550 nm we achieved 13.1 ps±0.4 ps FWHM with 71.1 %±3.7 % system detection efficiency (Detector A). Detector D, with a double cavity, achieved 83.3 % ± 4.3 % and a system jitter of 13.0 ps ± 0.4 ps.

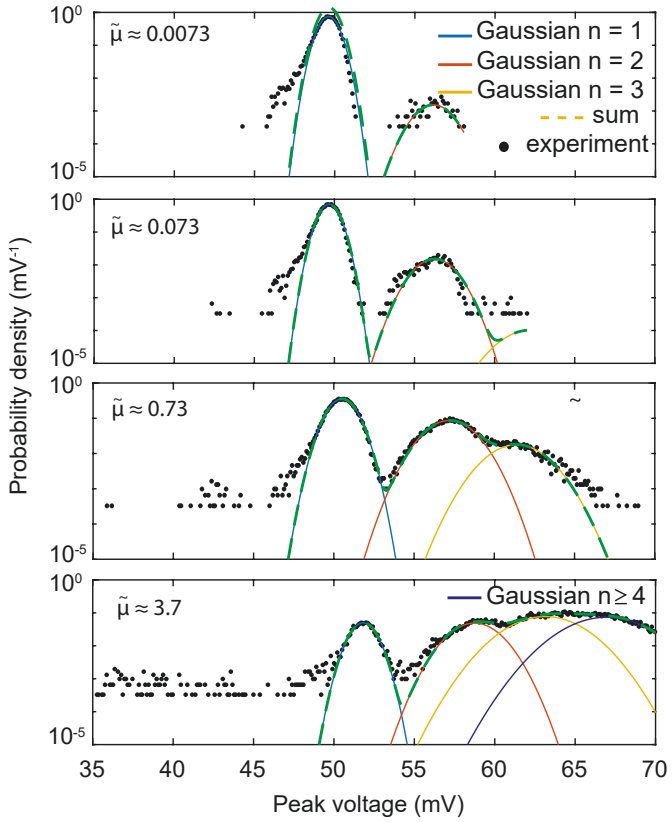

Figure 4-23: Gaussian fitting of the pulse amplitude histograms for several effective photon numbers.

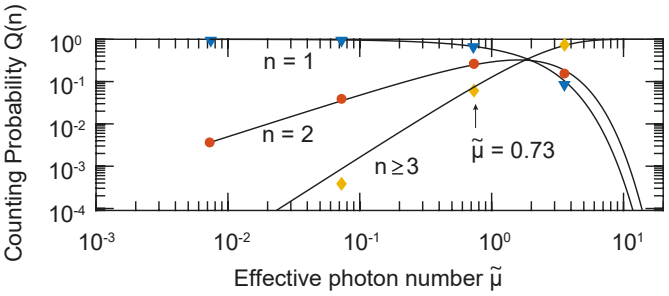

Figure 4-24: Photon counting statistics reconstructed from the pulse height distributions under different illumination conditions.

Moreover, our detectors have photon number resolution and imaging capabilities. However, there are a few outstanding limitations and discussion items that we want to highlight.

Limited performances Although our design delineates a path to demonstrate an all-rounder detector, in the current demonstration, the performance is still below what could be achieved with designs focused on a single metric.

- **Maximum count rate** One remaining limitation of our design is the maximum count rate. We expect it to be ultimately limited to about 5 Mcps to 10 Mcps due to the detector reset time. To address this issue, an active quenching circuit could be coupled to the device [150] and integrated into the chip in future iterations.

- **SDE** For the system detection efficiency, assuming an optimal fiber alignment, the current limitations are attributed to the detector fill factor and the cavity design. Both design elements were solely selected to facilitate fabrication and design and could be improved in future iterations, pushing these values to $> 90\%$

- **System jitter** The detector jitters are still two to three times higher than the values obtained with specialized low-jitter devices: e.g., 4.3 ps is the record jitter at 1550 nm. [42]. While the differential design effectively cancels the geometric contribution, large active area devices can be affected by defects induced by nanofabrication (e.g. line edge roughness) or intrinsic to the film (e.g. natural constrictions and grain boundaries) with a higher probability. In fact, the record jitter device was operating at a 0.8 fraction of the critical depairing current (I_{dep}) while, based on previous measurements [71, 72], we expect our device to operate between $0.5\,I_{\mathrm{dep}}$ to $0.7\,I_{\mathrm{dep}}$. This explains the overall higher jitter values obtained in our meandered SNSPDs compared to the record value. In this demonstration, we did not explicitly focus on optimizing the fabrication and film quality. We expect that by improving these technical aspects in the future, we will reach timing resolutions closer to the current record values, mostly limited by the intrinsic Fano fluctuations of the energy downconversion process [42, 136].

Need for external electronics The differential-to-single-ended setups rely on external components (balun or differential comparator) at room or cryogenic temperature. Although

our experiments show that the system performance is minimally degraded compared to the detector-only performance (system jitter is just 6% higher), external components make the detector prone to added electrical noise, which can ultimately degrade the system jitter. Similar electrical circuits could be custom-designed, integrated, and co-located on-chip with the differential impedance-matched detector to make the system more compact and improve performance. The technology introduced in the earlier chapters could be integrated here into a monolithic technology. Integrating nanowire-based electronics for on-chip signal conditioning could significantly improve system performance and avoid additional post-processing (e.g., photon-number discrimination).

4.10 Application and perspective

The performance obtained with our architecture may enable quantum communication at clock-rates >20 GHz, high-resolution single-photon laser ranging, faint optical-waveform reconstruction and previously unachievable capabilities in biomedical imaging applications. The possibility of discriminating the number of photons from optical radiation with high efficiency and timing resolution will enable the use of our detectors in applications such as non-classical state generation [151, 152], novel protocols in quantum networking [153, 154], and quantum information processing and linear optical quantum computing [155, 156, 157]. Our prototype detectors are currently in use in single-photon LIDAR [158] experiments, quantum information processing [159], and proposed as an experimental platform to probe fundamental superconducting nanowire switching phenomena [160]. We expect wide adoption of this architecture in commercial systems and in demanding applications needing an all-rounder single-photon detector technology. A promising future direction is the on-chip integration of the external processing electronics (balun, comparator, amplifiers) and quenching circuits with the detectors, possibly using monolithic nanowire-based superconducting elements. Minimizing external electronics and redesigning cabling and interconnects towards high-density architectures will reduce the deployment cost per channel and enable lower SWaP systems. This could help to scale experiments and applications which currently require and use tens to hundreds of free-space coupled detectors [26, 161].

4.11 Conclusion

In this chapter, we focused on the first direction for SNSPDs improvement. We demonstrated a single design that has the potential of becoming an all-rounder detector useful in novel highly demanding experiments. In the next chapter, we will focus on the second direction: integration and arraying technology.

Chapter 5

Waveguide-integrated superconducting nanowire detectors

Photonic integrated circuit (PIC) technology is expected to play a central role in advancing the frontiers of quantum information science applications. The required scaling and functional complexity of these quantum experiments will only be possible through the high density, enhanced performance, and environmental stability afforded by integrated elements [56]. As such, it is fundamental to develop processes to fabricate integrated linear and non-linear optical devices and heterogeneously integrate photon sources and single-photon detectors. This chapter discusses the integration of SNSPDs with current PICs and their potential scalability to many channels.

5.1 Waveguide-integrated SNSPD technology

With the advent of PICs and their increasing functional complexity, SNSPD technology has followed suit and evolved from a free-space coupled technology to waveguide-integrated demonstrations. In this section, we describe the waveguide-integrated SNSPD (WGSNSPD) and demonstrate integration on lithium-niobate-on-insulator (LNOI), one of the most attractive platforms for integrated quantum photonics.

5.1.1 Working principle

Unlike free-space coupled SNSPDs (i.e., our devices in Chapter 4), waveguide-integrated SNSPDs exploit the efficient coupling between the evanescent field of the guided optical

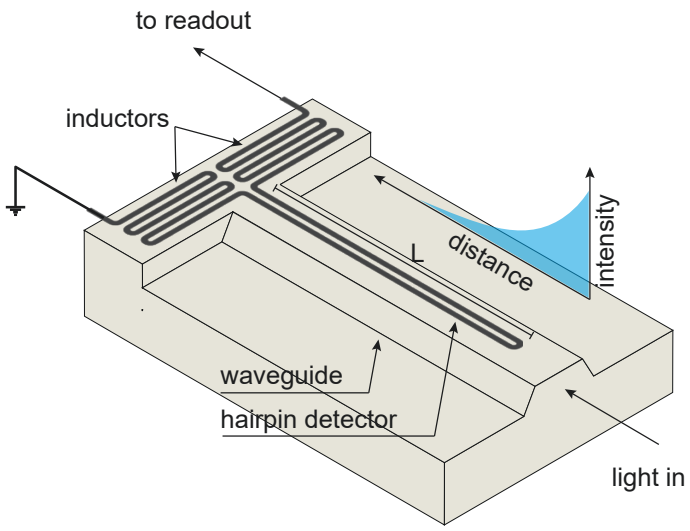

Figure 5-1: Artistic sketch of a waveguide-integrated SNSPD. A single nanowire hairpin, with length L, is fabricated on top of the waveguide, represented with a rib architecture. The light travels in the waveguide towards the SNSPD and gets completely absorbed over a certain distance. Side inductors are co-fabricated with the hairpin to mitigate latching behavior.

mode and the superconducting nanowire placed directly atop optical waveguides. Fig. 5-1 shows an artistic sketch of the general architecture of these devices. The detecting element consists of a single hairpin on the waveguide. The hairpin length L determines the maximum theoretical detection efficiency. If L is larger than $l_{100\%}$ (a characteristic length after which the hairpin completely absorbs the light), the detector can ideally get to 100% on-chip detection efficiency (OCDE). However, this is rarely the case due to optical losses in the materials.

In Fig.5-1, we also included two side inductors usually fabricated with WGSNSPDs. These inductors are needed to mitigate latching, a common problem with short/low-inductance detectors [162, 163]. Thanks to the reduced footprint, WGSNSPDs can have several advantages in terms of timing resolution, reset time, and count rates [51]. As we showed in the previous chapter, these metrics are inversely proportional to the detector's active area.

5.1.2 Platform integration challenges

WGSNSPDs have been successfully demonstrated on many photonic platforms, such as silicon-on-insulator [164, 165], silicon nitride [166, 167], aluminum nitride [168], diamond

[169], gallium arsenide [170], and tantalum oxide [171]. However, integration on quantum photonics platforms is being slowed down due to technical compatibility issues. Thin-film lithium-niobate-on-insulator (LNOI), one of the most attractive platforms for quantum photonics, presents some critical challenges for integrating WGSNSPDs [52]. First, the deposition of the superconducting films must be tailored to avoid excessive substrate heat, which could damage the LNOI films and the pre-patterned structures. Second, while the detector integration is generally *detector-first* (SNSPDs fabricated before the waveguides), this approach would expose the nanowires to the aggressive dry etching and wet cleaning required for optimal waveguide fabrication on this platform. To address the above challenges, researchers have tailored superconducting thin-film conformal deposition processes at low temperature [172, 173], and fabrication processes, including encapsulation layers [174] to minimize the degradation of the nanowires. *Waveguide-first* approaches (nanowires fabricated after waveguide etching), including buffer layers and conformal films, improved the fabrication yield [173]. The next section describes our work toward developing an integrated process for WGSNSPDs on LNOI waveguides.

Once a good yield is established, integrating multiple detectors on the same chip is another challenge. While it is feasible to read out tens of SNSPDs with a direct approach (each device has an individual readout channel), this becomes infeasible if we scale to hundreds of channels. For this reason, it is fundamental to develop multiplexing strategies to ensure that the number of readout channels does not grow linearly with the number of detecting elements. We will address this challenge in the second part of this chapter.

5.2 WGSNSPDs on thin-film LNOI

This section demonstrates a molybdenum-silicide (MoSi) WGSNSPD on thin-film LNOI. For brevity, we will refer to this demonstration as LNSNSPD. Our device follows an earlier work published at Ref. [163] where we demonstrated an NbN WGSNSPD on LNOI. Unfortunately, this device had a very limited OCDE ($< 1\%$), and the yield was suboptimal. Here, we describe our new approach, design, and measurement setup and report the OCDE and jitter results for our MoSi LNSNSPD. I want to acknowledge Prof. Limbo Shao, Prof. Boris Desiatov, and Dr. Jeffrey Holzgrafe, for fabricating the lithium niobate photonic integrated circuit, Dr. Bart Machielse for his help with the atomic layer deposition, Dr. Di Zhu, for his

help with the characterization setup, Ian Christen for help with the piezo positioner setup, and Prof. Marko Loncar for the collaboration on the project.

5.2.1 Approach

In this demonstration, we introduced an improved approach that increased the device yield. This consisted of three main principles, which are summarized here:

- **Waveguide-first fabrication** To avoid exposing the SNSPDs to harsh etching chemistry involved in fabricating the LNOI elements, we took a waveguide-first approach. In the early stage of this project, we attempted a detector-first approach, but the results were less than optimal. Most of the devices, which were functional before processing, were electrically open after waveguide fabrication [163].

- **Amorphous superconductor** We used a 6.4 nm-thick molybdenum silicide (MoSi) thin-film, which we previously characterized to be amorphous [175]. In the early stage of the project, we used our standard polycrystalline niobium nitride thin films [163]. However, the properties of our devices were suboptimal, with efficiency far from saturation and reduced yield. Instead, the literature has shown that integrating amorphous thin films leads to higher yield for integrated superconducting nanowire detectors [176]. Amorphous materials have fewer constraints related to substrate lattice matching and can be deposited very thinly with a lower concentration of defects.

- **Thin-film buffer layer** By selecting a waveguide-first approach, the superconducting thin-film is generally blanket deposited on the whole photonic circuit. A few concerns are raised here. The thin-film etching might be ineffective on the vertical or diagonal waveguide sidewalls, inducing unwanted optical loss. Uncontrolled material redeposition might increase the optical losses even more. Over-etching can clean away the residues but will damage the waveguide layer and consume the detector mask. A solution exists in integrating a thin-film buffer layer between the photonic layer and the superconducting layer [173]. While this spacer effectively reduces the coupling between the evanescent field and the detector, it mitigates the optical losses and protects the waveguide in case of over-etching. Here, we used a 10 nm-thick hafnium dioxide film deposited with atomic layer deposition.

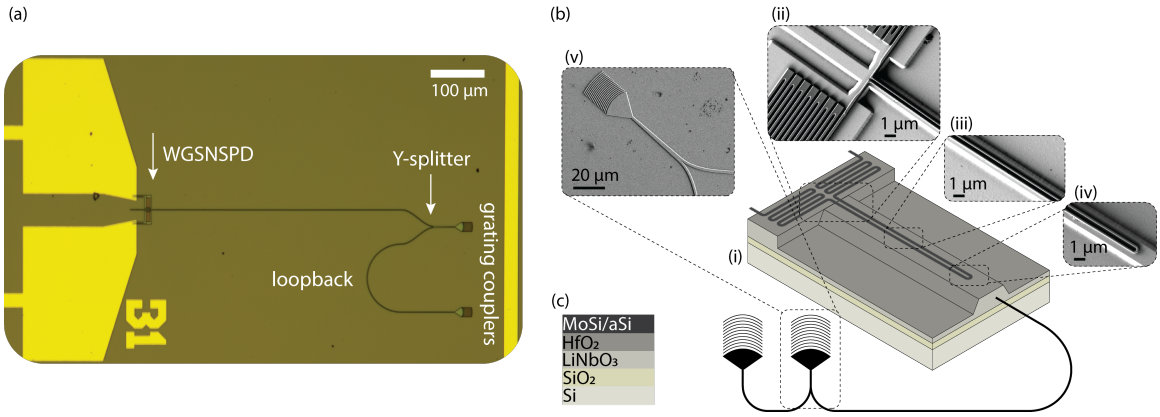

Figure 5-2: Fabricated device. (a) Optical micrograph showing an overview of the fabricated device. (b) Scanning electron micrographs of the devices (hairpin and PIC), accompanied by an artistic sketch. (c) Materials stack.

5.2.2 Device design

Our device consists of a photonic integrated circuit with a waveguide-integrated SNSPD. Fig. 5-2(a) shows an optical micrograph of one of the design variations after fabrication. The LNOI PIC consists of an input grating coupler interfaced to a 3 dB Y-splitter. One output of the Y-splitter is connected to another nominally identical grating coupler completing a loop-back monitoring structure. The other output is a 400 µm-long 1 µm-wide waveguide (single-mode at 1550 nm). The superconducting detector is a Si-capped 6.4 nm-thick MoSi U-shaped 100 nm-wide hairpin (200 nm-wide spacing) fabricated on top of the waveguide, connected on each side to a meandering nanowire inductor terminated to contact pads. Between the nanowire and the waveguide, we have a 10 nm hafnium dioxide protection layer. Fig. 5-2(b) shows a device sketch (i), and scanning electron micrographs of the hairpin (ii, iii, iv) and the PIC (v). Fig. 5-2(c) shows the overall stack.

In Fig. 5-3(a), we show the refractive index of the MoSi thin film (including the a-Si capping layer), measured with ellipsometry, after sputtering. The data are used to simulate (ANSYS Lumerical) the fundamental waveguide modes and the corresponding optical losses in the presence of the hairpin. Fig. 5-3(b) shows the optical loss as a function of the wavelength for TE and TM modes. We included all the layers in the material stack (i.e. hafnium dioxide buffer, amorphous silicon capping layer, residual HSQ mask on the hairpin), and assumed the hairpin to be the only absorber. The modes at 1550 nm are shown in 5-3(c-i) and (c-ii)). At this wavelength, the absorption for TE and TM modes are 0.089 $\mathrm{dB\mu m^{-1}}$

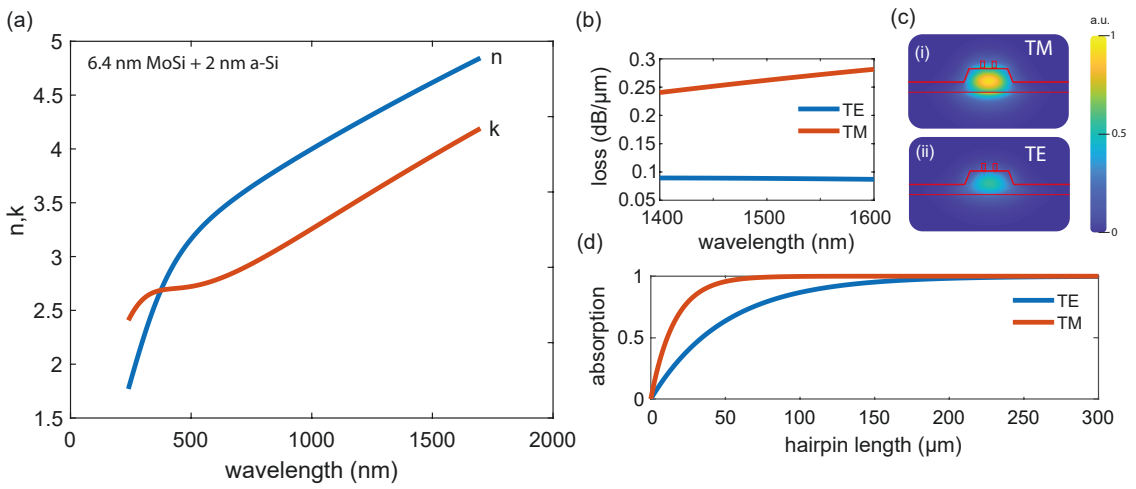

Figure 5-3: (a) Refractive index of 6.4 nm MoSi with amorphous silicon capping layer. (b) Simulated optical loss for TE and TM modes as a function of the wavelength. (c) TE and TM modes. (d) Total absorption in the waveguide as a function of the hairpin length for TE and TM modes.

and $0.272\,\mathrm{dB\mu m^{-1}}$, respectively. To ensure unity absorption for both modes (Fig.5-3(d)), we designed the length of our hairpin to be 250 μm.

5.2.3 Fabrication

The PIC was fabricated on a commercial X-cut lithium-niobate-on-insulator wafer (NanoLN) at CNS, Harvard University. The LN device layer was 600 nm thick, on top of a 2 μm-thick buried thermal oxide on a silicon handle. The photonic circuit was patterned on hydrogen silsesquioxane (FOx-16) with electron beam lithography (EBL) and transferred into the LN layer using Ar^+-based reactive ion etching (RIE). The etching depth was 350 nm. This part of the fabrication is not shown in the flow of Fig. 5-4. After substrate cleaning (piranha solution + solvent clean), a 10 nm-thick hafnium dioxide layer was deposited by atomic layer deposition (90 °C, 100 cycles). A 6.4 nm-thick molybdenum silicide (MoSi) film was co-sputtered on the substrate at room temperature, protected by 2 nm-thick sputtered amorphous silicon capping layer. The Mo/Si sputtering conditions were tuned towards a higher silicon content (50 W DC / 120 W RF) to reduce the crystalline fraction, as demonstrated in our previous investigations [177, 175]. The sheet resistance was $R_s = 475\,\Omega$ per square and the critical temperature $T_c = 3.4\,\mathrm{K}$. Electrical contacts were fabricated with positive-tone direct writing photolithography, followed by two angled evaporation of a 10 nm-thick

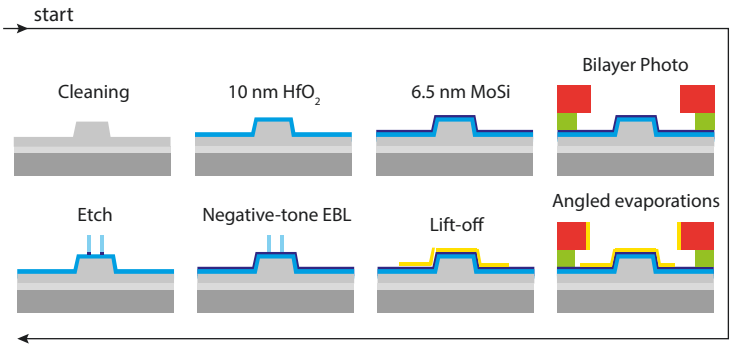

Figure 5-4: Detector fabrication flow. The fabrication of the PIC is not shown in this sketch.

titanium adhesion layer and a 100 nm-thick gold electrical layer, followed by liftoff. The nanowire detector was patterned with aligned EBL using negative tone resist (HSQ) and transferred into the MoSi with RIE in a CF_4 chemistry. More details on the lithographic processes are available in Appendix A.

5.2.4 Measurement setup

To measure the on-chip performance of the LNSNSPD, we built an optical alignment setup. The chip was mounted (GE Varnish) on a copper plate with a custom-printed circuit board and wire-bonded. This first assembly was mounted on a second copper platform where we also placed a 3-axis piezo positioner (Attocube) with a custom 8° fiber-array with telecom fibers, mounted on top. The whole assembly is shown in Fig. 5-5(a). We used two cameras (top and front) to align the fiber array to the PIC. We assessed the coupling by measuring the power through the loop-back monitoring structure. After pre-alignment at room temperature, the assembly was mounted and thermalized to the coldest stage of a closed-loop cryostat and the fiber array was spliced in place.

The characterization setup is shown in Fig. 5-5(b). The LNSNSPD was biased in a single-ended configuration with a current source through a bias tee. The RF terminal of the bias tee was connected to an oscilloscope (jitter characterization) or a universal counter (efficiency characterization), after room temperature amplification. To increase the bias margin of our detector and mitigate latching, we included an in-line cryogenic inductive shunt. Light from an attenuated (VOA) 1550 nm femtosecond laser was coupled to the PIC through the input of the fiber array. The coupling was monitored with the loopback structure, whose output

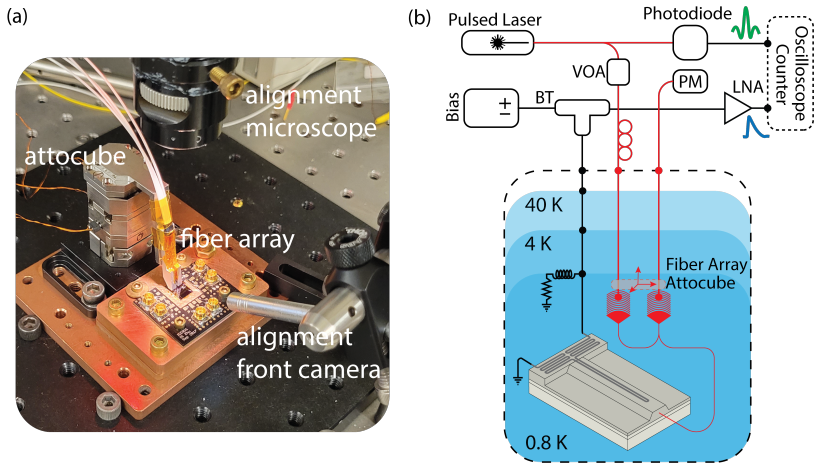

Figure 5-5: Characterization setup for the LNSNSPD. (a) Picture of the optical coupling platform. (b) Sketch of the measurement setup.

Reference	Instrument
Room temperature LNA	RF-Bay LNA-2500 + LNA-2000
Real-time oscilloscope	LeCroy WavePRO 760i (6 GHz)
Variable optical attenuator	JDS Fitel HA1
Power meter	Thorlabs S155C
Inductive shunts	Custom: 1.2 µH + 25 Ω
Photodiode	Thorlabs DET08CL
Pulsed laser	Calmar Mendocino 1550 nm 40 MHz repetition rate
Universal counter	Keysight 53131A
Nanopositioner	3x Attocubes

Table 5.1: Overview of the instruments for the measurement setups shown Fig. 5-5.

was interfaced to a calibrated power meter. To characterize the jitter, we also acquired an optical reference signal from a fast photodiode. Table 5.1 contains the list of the equipment used in this measurement setup.

5.2.5 Results and discussion

DC characteristic and impact of shunting circuit

Our setup used a custom shunting circuit (series combination of a 1.2 µH inductor and a 25 Ω resistor) placed at the cryogenic stage to mitigate the detector latching behavior. This technique has been shown to improve the detection capabilities of latching detectors and extend their bias margin. In Fig. 5-6, we compare the DC switching characteristics of our 250 µm-long hairpin at 0.78 K in the presence vs. absence of the shunt. The shunted detector

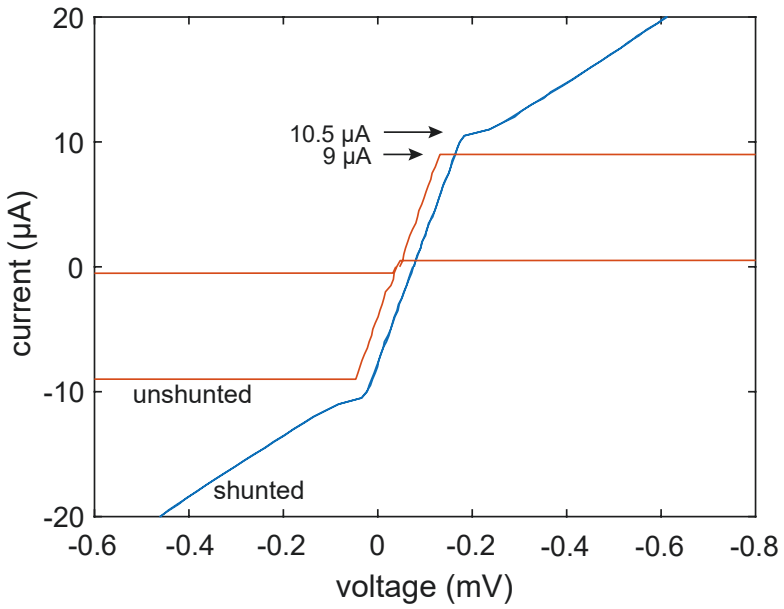

Figure 5-6: Impact of the shunting circuit on the DC characteristic at 0.78 K.

achieves a switching current of about $I_{\mathrm{sw}} = 10.5\,\mu\mathrm{A}$, while the unshunted detector is limited to $9\,\mu\mathrm{A}$. This represents a 15% extension of the bias margin.

Optical coupling alignment and loss estimation

The optical coupling routine consisted of a few defined steps that we found produced repeatable results. First, we pre-aligned the fiber array to the PIC by operating the nanopositioner at room temperature, maximizing the transmitted power through the loopback. During the cooldown (18 hours), we automatically scanned the fiber array onto the grating couplers every 10 minutes. We positioned the array at approximately the maximum transmission at every scan. Note that during this automatic alignment optimization routine, we did not operate the Z-axis positioner to avoid the possibility of crashing the array into the detector chip. After completing the cooldown, we manually operated the nanopositioner in the three axes to find the maximum transmission. Once at the maximum coupling point, we operated the polarization paddles to maximize the transmission as a function of the input polarization. We can calculate the loss of the grating coupler with the following relations:

$$\eta_{\mathrm{gc}} = \frac{P_{\mathrm{out}} - P_{\mathrm{in}} + \eta_{\mathrm{Y}}}{2} \tag{5.1}$$

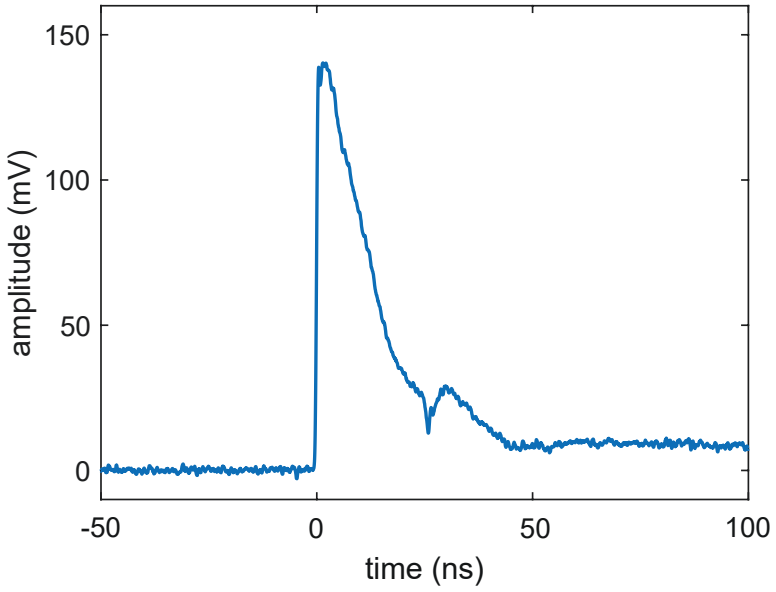

Figure 5-7: Averaged detector output pulse at 0.78 K.

where P_{in}, is the power measured at the input of the loopback structure, P_{out}, the power measured at the output of the loopback structure, η_{Y} is the loss of the Y-splitter, which we assume to be 3 dB. Note that P_{in} and P_{out} include the insertion loss to the fiber array. Our grating couplers have a loss $\eta_{\text{gc}} = 9.96\,\text{dB}$.

Output pulse

In Fig. 5-7, we show the output pulse in response to 1550 nm photons at 0.78 K, with a bias current of 10 μA. The bump at about 25 ns is attributed to reflections in the amplifier chain. The reset time constant $\tau = 14.5\,\text{ns}$, extracted from fitting the relaxation of the pulse with an exponential function, is in slight disagreement with the estimated $\tau = \frac{L_{\text{kin}}}{R_{\text{L}}} = 25\,\text{ns}$. Here the superconducting detector has 7256 squares and $L_{\text{kin,s}} = 167\,\text{pH}$ per square, calculated with the relations presented in Chapter II. We attribute the incongruence to the presence of the inductive shunt (1.2 μH inductor terminated to ground with a 25 Ω resistor) affecting the detector relaxation dynamics. An identical detector, measured without the shunt inductor at the same temperature, had a $\tau = 23.5\,\text{ns}$ in agreement with the theoretical estimations.

We simulated the relaxation dynamics of unshunted Fig. 5-8(a) and shunted Fig. 5-8(b) detectors using SPICE. The detector was modeled using Berggren et al. [140], the shunt inductor and resistor matched the ones used in the experimental setup. In Fig. 5-8(c), we

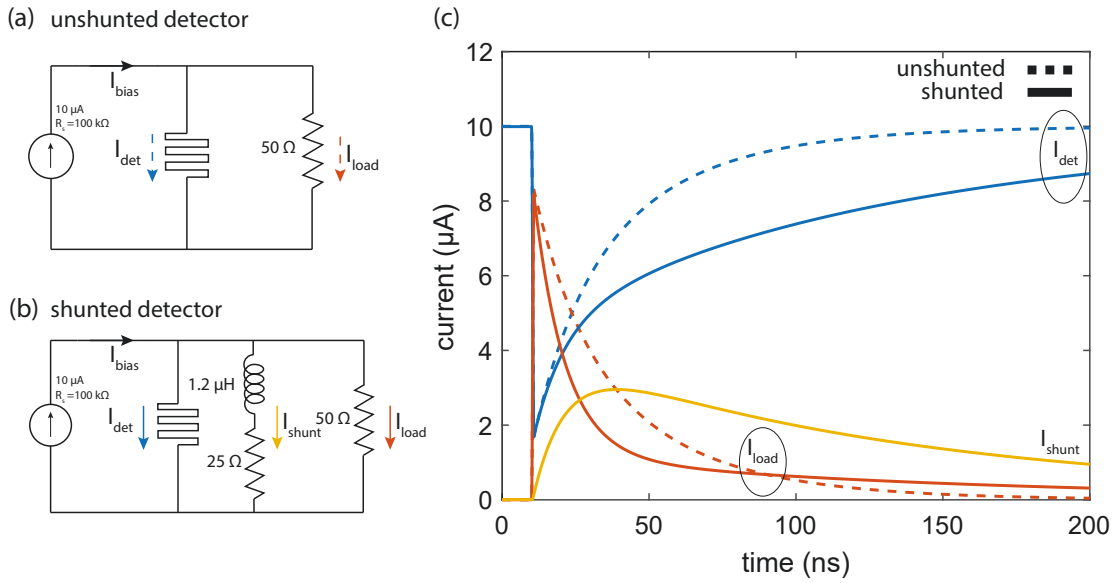

Figure 5-8: Simulation of current dynamics in unshunted and shunted detectors. (a) Simulation circuit for the unshunted detector. (b) Simulation circuit for the shunted detector. (c) Simulation results. The shunted detector is governed by more complex pulse dynamics than the unshunted case. Due to the indicative shunt, the bias current takes more time to load the detector after the pulse, mitigating the latching behavior.

show the time-dependent currents in the two cases. In the unshunted detector, the pulse relaxation is governed by the L_{kin}/R time constant. In the shunted detector, the second inductor introduces an additional time constant, altering the simple first-order dynamic. As a result, after the detection event, the bias current returns to the detector inductor more slowly than in the unshunted case, reducing the latching phenomenon. The output dynamics is instead governed by a faster initial decay followed by a longer return to zero. The simulation results agree with the experimental observation.

On-chip Detection Efficiency

To characterize the on-chip detection efficiency, light was coupled into the waveguide through the input grating coupler, and the coupling was optimized following the procedure described above. Fig. 5-9 shows the measured on-chip detection efficiency. The OCDE is estimated with the following relation:

$$\text{OCDE} = \frac{\text{PCR} - \text{DCR}}{\text{ph}_n} \tag{5.2}$$

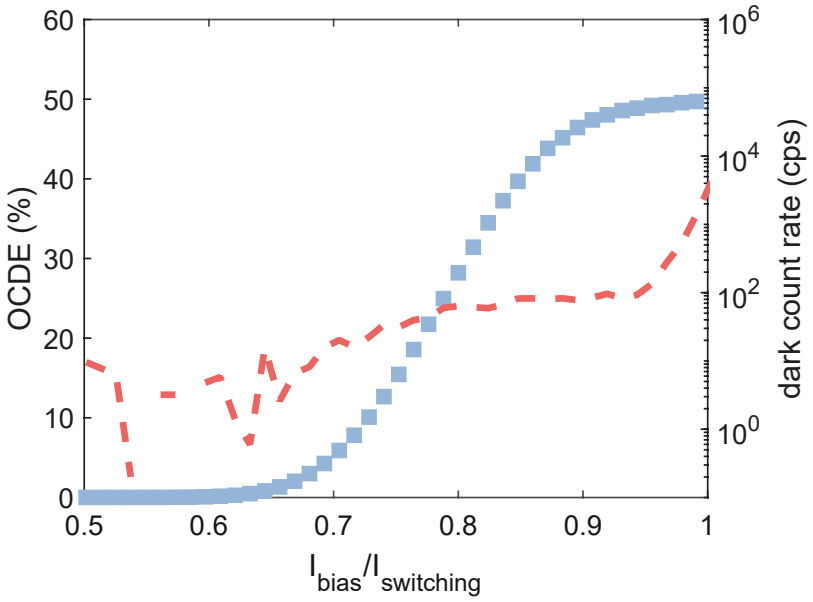

Figure 5-9: On-chip detection efficiency and dark count rate for 1550 nm photons, at 0.78 K

where PCR is the count rate of the detector measured with illumination, DCR is the dark count rate, and ph_n is the number of photons in the detector waveguide. The number of photons per second can be estimated with the following relation:

$$\mathrm{ph}_n = \frac{1}{h\nu}\sqrt{\frac{P_{\mathrm{in}}\,P_{\mathrm{out}}\,\eta_{\mathrm{attn}}}{2}} \tag{5.3}$$

where $h\nu$ is the energy associated with a photon of frequency ν, P_{in} is the optical power in the input fiber P_{out} is the optical power at the output of the loopback structure, and η_{attn} is the attenuation applied with the variable optical attenuator. These relations assume a perfect 3 dB Y-splitter and identical grating couplers. Our devices has a saturated efficiency of about 50%, with a $100\,\mathrm{s}^{-1}$ to $2000\,\mathrm{s}^{-1}$ dark count rate, according to the bias level. We estimate the relative uncertainty of the reported OCDE to be ±10% dominated by the uncertainty of the power meter. Compared to our estimation, the obtained OCDE is significantly degraded. For a 250 μm-long hairpin, we would have expected an OCDE approaching unity. We attribute this discrepancy to two main factors:

- our efficiency calculation assumes a perfect 3 dB Y-splitter and identical grating couplers; a 5% splitting unbalance could result in a $\approx \pm 15\%$ relative discrepancy in the efficiency.

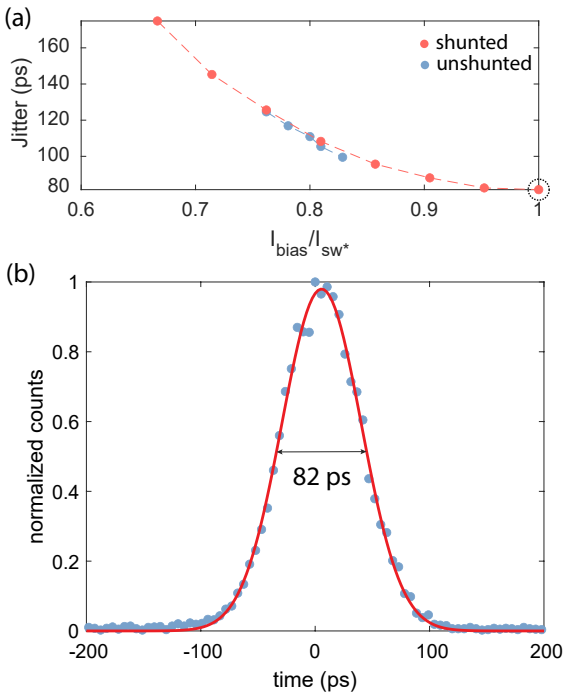

Figure 5-10: System jitters of our LNSNSPDs. In (a) we compare the impact of shunting circuit on the timing resolution. In (b) we show the system jitter, for our shunted LNSNSPD biased at I^*_{sw}.

- our efficiency calculation assumes zero waveguide loss and lossless materials; this is unlikely.

To better estimate the efficiency, it would be fundamental to calibrate the material loss and accurately measure and characterize each PIC component.

System jitter

To measure the system jitter, we used a real-time oscilloscope with the highest sampling rate setting (40 GSample/s). We also acquired a reference optical signal generated with a fast photodiode. In this case, to measure the impact of the shunt on the timing performance, we lifted up the fiber array to flood illuminate the original detector together with a nominally identical neighbor detector.

Fig. 5-10(a) shows the measured detector jitters as a function of the bias current (normalized by the switching current of the shunted detector, I^*_{sw}) for the shunted and unshunted detector. The shunted detector achieves an 82 ps system jitter. The unshunted detector is limited to 100 ps. These results show that the inductive shunt is very effective in extending

the bias margin of the detector, as we also demonstrated in the previous section. The unshunted detector reaches a jitter value matching one of the shunted detectors biased at 85% of its bias margin.

For the shunted detector, the jitter saturates with the bias current at a relatively large value compared to other results on the same platform [173, 174]. This effect is attributed to three elements. First, the detector has a total length of about 1 mm, and the kinetic inductance of the material is particularly high due to reduced critical temperature and the relatively high measurement temperature. Therefore, we expect the geometric contribution to the timing jitter to be particularly elevated in our detector. Second, our measurement setup is not optimized for low-jitter measurements. We did not use cryogenic amplifications. Third, the shunt circuit reduces the signal-to-noise ratio, increasing the impact of the electrical noise. We expect a better system jitter by measuring this device with the setup of Chapter 3, using differential readout and cryogenic amplification.

5.2.6 Conclusions and perspectives

We demonstrated a MoSi waveguide-integrated SNSPD on a lithium-niobate waveguide. Our detector has a $50\% \pm 5\%$ saturated on-chip detection efficiency and an 82 ps jitter. The efficiency saturation plateau and its value are larger than previous demonstrations in the literature on the same platform. However, the jitter is not as low. Lomonte et al. [174] demonstrated a 25% efficiency with 40 ps jitter using NbTiN with a detector-first approach. Sayem et al. [173] demonstrated a 45% efficiency with 32 ps jitter with ALD NbN. We expect to improve the efficiency and timing resolution with better characterization equipment (Lomonte [174] decreased the jitter to 17 ps using cryogenic amplifiers) and with a better understanding of the optical losses involved in the system.

Our work shows that sputtered MoSi detectors can be integrated on a lithium-niobate waveguide using a hafnium dioxide buffer layer. Our process opens the possibility of fabricating other superconducting components on this platform, combined into more complex circuits and architectures. For example, superconducting nanowire digital circuits [31] can be used with SNSPDs to perform simple on-chip post-processing operations, such as checking for coincidence detection. The results of the operation could be amplified with nanowire devices [29] to drive integrated optoelectronic LNOI components (e.g., modulators [52]), realizing operations and protocols applicable to quantum information processing, i.e., feed-

forward [178].

5.3 Progress on waveguide integrated delay-line multiplexed detector

In this section, we report our progress on the realization of a waveguide-integrated delay-line multiplexed detector. An earlier version of this device was presented by Dr. Zhu in their doctoral dissertation [43]. In the following, we first summarize the motivation behind this project and describe the architecture of this device. Then, we report our progress on its fabrication and characterization. I want to acknowledge Dr. Di Zhu, for the design of the device, development of the initial fabrication processes, and discussion on data processing and measurement strategy, and Ian Christen for help with the piezo positioner setup.

5.3.1 Motivation and device architecture

In Section 5.2, we demonstrated the integration of a single detector on a photonic platform. One of the challenges for scaling to many integrated channels is their readout. While it is possible to use discrete electronics with a few elements (i.e., every channel is biased and read out separately, using dedicated lines and components), this approach is not scalable when thousands of these detectors need to be integrated. To address this challenge, we apply the differential impedance-matched architecture introduced in Chapter II to read out an array of sixty-five elements/channels using the time-delay multiplexing paradigm. The same concept was used by Zhao et al. [54] to demonstrate the superconducting single-photon imager, by Zhu et al. [41] to demonstrate an earlier version of this device (on aluminum nitride, without waveguides), and previously, in this thesis, with the detector mode imaging capabilities.

Our device comprises sixty-five waveguide-integrated nanowire detectors intertwined with superconducting nanowire delay-line sections and a photonic integrated circuit. In this case, we selected silicon-on-insulator as the photonic platform due to its simpler fabrication processes and wider material integration compatibility. The PIC consists of a 3-input 65-channel waveguide directional coupler (3-to-65 coupler), whose ends are coupled to the single-photon detectors. A sketch of the base architecture is shown in Fig. 5-11. The device was designed in this way to perform a continuous quantum random walk experiment similar to Ref. [179]. Our impedance-matched differential multi-element detector allows si-

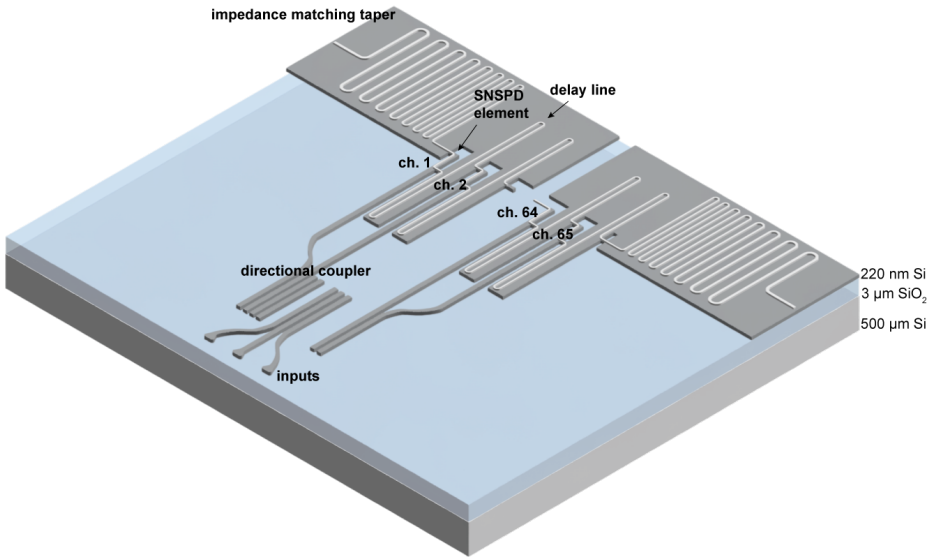

Figure 5-11: Sketch of the base architecture of the sixty-five channel waveguide integrated detectors. The sketch shows the three grating coupler inputs, the 3-to-65 directional coupler, four channels separated by the delay line and the impedance matching tapers for differential readout.

multaneous mapping of coincidence over sixty-five spatial modes in a compact footprint. The 3-input design of the directional coupler allows the injection of single photons and/or indistinguishable photons (e.g., from SPDC). The coincidence counting statistics measured on the detector array is expected to render some non-classical features due to quantum interference. More details are available in Ref. [43, 180].

5.3.2 Design specifications

The PIC was designed for an SOI platform (220 nm silicon device layer on 3 μm buried oxide on silicon handle) and TE single-mode operation at 1550 nm. The waveguide width is 500 nm. In the directional coupler, the waveguides are spaced 200 nm, giving a coupling length of about 37.8 μm for complete power transfer between optical waveguides [43, 180]. The detector array consists of sixty-five 20 μm-long 100 nm-wide nanowires intertwined by 420 μm-long 150 nm-wide nanowire transmission line sections. In Fig. 5-12, we show the simulation of the microwave characteristics of the detector stack, assuming nominal dielectric constants and NbN with a $L_{\mathrm{kin,s}} = 80\,\mathrm{pH}$ per square. The stack is a covered microstrip, similar to the one introduced in Chapter II: the nanowire is referenced to the top ground

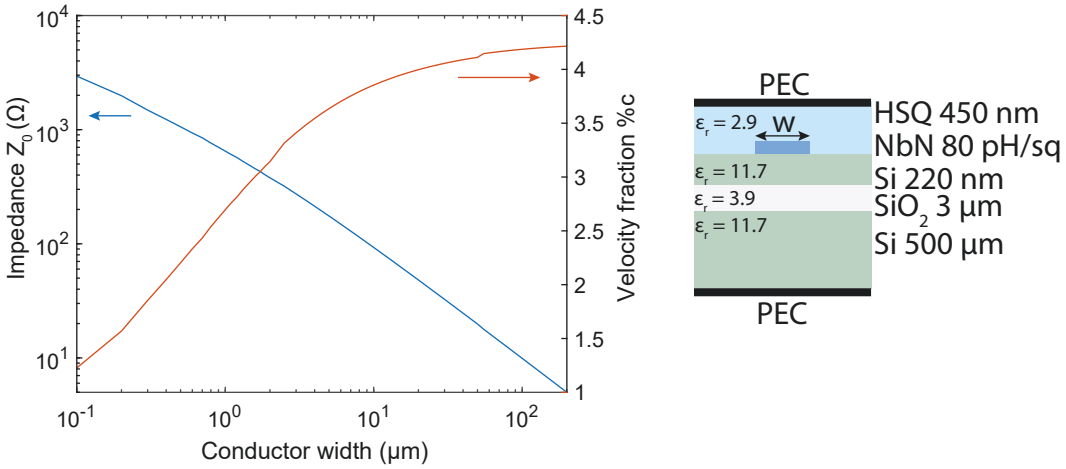

Figure 5-12: Simulation of characteristic impedance and velocity fraction for the nanowires used in the delay-line multiplexed detector. The stack is shown on the right.

layer through a fabricated dielectric spacer. The 100 nm-wide detector has phase velocity 1.22% c ($n_{\text{eff}} = 81.46$) and an impedance $Z_0 = 2.946\,\text{k}\Omega$. The 150 nm-wide delay-line has a phase velocity 1.43% c ($n_{\text{eff}} = 69.65$) and an impedance $Z_0 = 2.898\,\text{k}\Omega$. The delay lines give a time separation of about $t_{\text{delay}} = 100\,\text{ps}$ per pixel. The total number of squares of the detector area (detector + delay line) is 197990. Each end of the device is interfaced with Klopfenstein impedance-matching tapers designed for a return loss of $-20\,\text{dB}$ and a cutoff frequency of 580 MHz. The taper is $\approx 9\,\text{mm}$ long, with 8477 squares. Including the tapers, the total inductance of the detector is 17.2 μH. Note that, the sheet inductance value selected for the simulation is generally appropriate for films thicker than what was used with this device. Therefore, we expect a higher inductance and an overall slower propagation speed in both the detector and delay lines.

5.3.3 Fabrication

We restructured the fabrication process starting from Ref. [43]. Figure 5-13 shows the final fabrication flow. (a) We started with a $1\,\text{cm} \times 1\,\text{cm}$ SOI substrate (220 nm Si device layer, 3 μm buried oxide BOX), diced from a 150 mm wafer and cleaned with solvent clean, piranha solution, and HF dip. (b) We deposited a 5 nm-thick NbN film following the method of Ref. [96]. (c) We fabricated wire-bonding pads using the positive-tone bilayer-liftoff direct-writing photolithography process described in Appendix A. We evaporated and lifted off

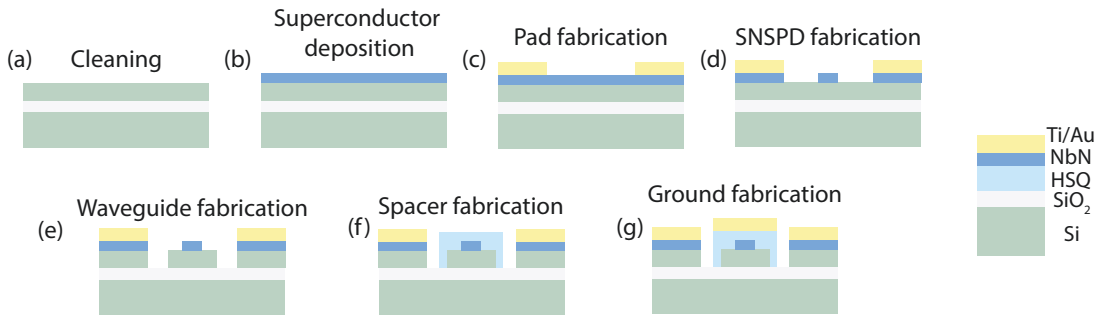

Figure 5-13: Fabrication process flow for the 65-channel waveguide-integrated detector.

10 nm titanium (adhesion layer) + 50 nm gold. (d) We fabricated the superconducting nanowire device using a negative-tone electron-beam lithography process with 6% HSQ (Appendix A). We etched the superconducting layer using RIE in CF_4 plasma. (e) We patterned the photonic integrated circuit using the thick positive tone ZEP-520A process (Appendix A). We etched the PIC into the silicon device layer using RIE in a SF_6 + C_4F_8 plasma. (f) We fabricated a 450 nm-thick HSQ spacer using the low-contrast process. (g) We fabricated the top ground plane using the positive-tone direct-writing photolithography process. We evaporated and lifted off 10 nm titanium (adhesion layer) + 100 nm gold.

Fig. 5-14 shows pictures of one of the fabricated devices. For every substrate, we fabricated four identical devices. Sub-figure 5-14(a) shows the loopback structure (two grating couplers connected by a waveguide) that we used to calibrate losses and perform and check optical alignment. A scanning electron micrograph shows a representative grating coupler. Sub-figure 5-14(b) shows the 3-to-65 directional coupler. This is a 300 µm-long PIC consisting of sixty-five 500 nm-wide silicon waveguides nearest-neighbor coupled through a 200 nm-wide gap. The SEM shows the 3-to-65 transition and the first 50 µm of the device. At the end of the directional coupler, the waveguides separate as a straw broom and are coupled to the detectors fabricated on top. The nanowires are 100 nm-wide and have a 200 nm alignment buffer on each side. The coupling region is 20 µm long. Each detector channel is time-multiplexed through a delay line supported in a broader silicon platform. Sub-figure 5-14(c) shows an integrated detector and delay lines, before spacer and top-ground plane fabrication.

We want to mention that the detector yield was suboptimal: in our last fabrication attempt, of four devices per chip, only one was functional (the one that is tested here).

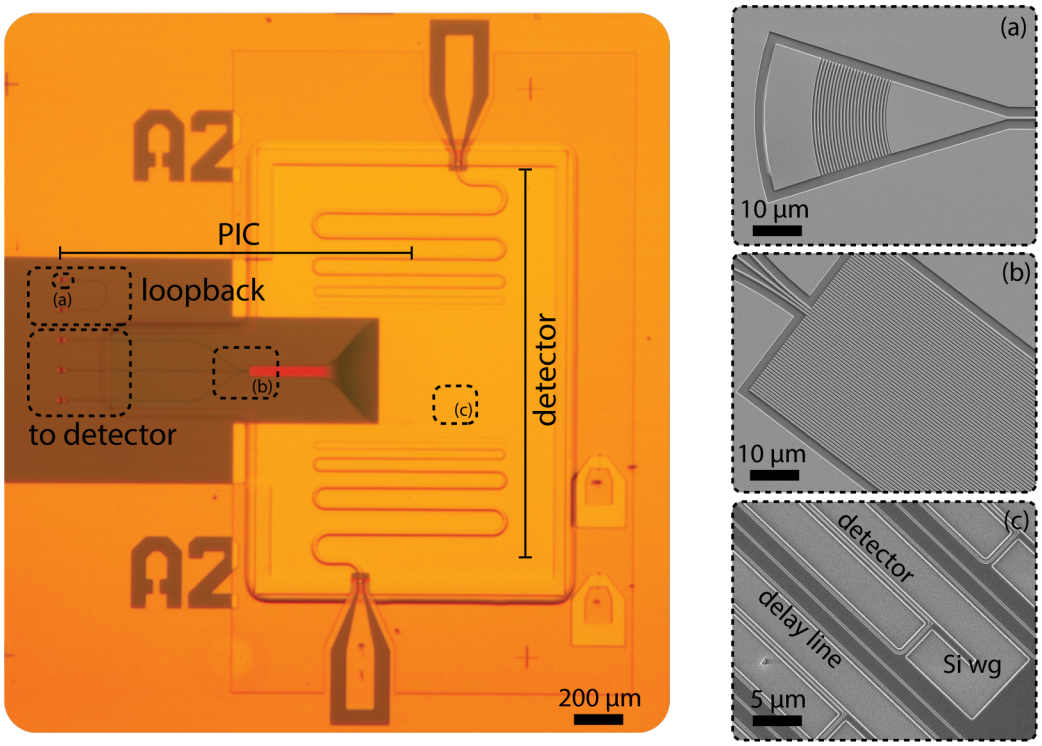

Figure 5-14: Picture and scanning electron micrographs of a fabricated 65-channel waveguide integrated SNSPD. The optical micrograph shows the completed device, after the fabrication of the HSQ spacer and the top ground plane. For clarity, we included indications to the several sections of the detector. In (a) we show the SEM of a grating coupler, which is used for the loopback calibration structure and for the input of the 3-to-65 directional coupler. In (b), we show the transition from the input waveguides to the directional coupler. In (c), we show the nanowire detector and the delay lines integrated on the silicon waveguides and support structures.

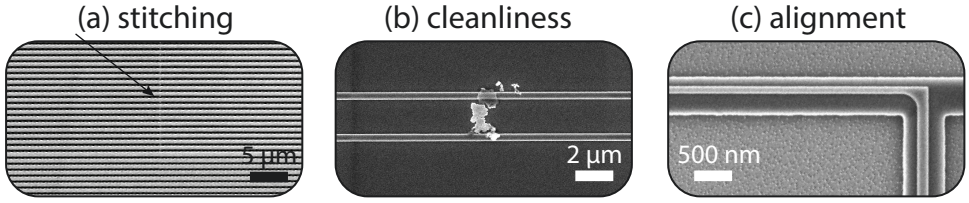

Figure 5-15: Examples of fabrication issues with our large area devices. (a) Stitching errors due to the limited field size. (b) Cleanliness issues. (c) Alignment issues.

Moreover, several fabrication runs gave no functional devices. Fabrication is exceptionally complex (at our academic research laboratory), and several factors might lead to nonfunctional devices. Below we list a few of those and provide possible improvement paths.

- **Intrinsic material issue** We used NbN as the superconducting layer. We occasionally experienced devices that, while looking pristine, were highly resistive or open. Given the large area of our detector, we cannot exclude this issue from being caused by intrinsic material defects. A solution exists in using an amorphous material such as MoSi, following the same methods presented in Section 5.2.

- **Field stitching** Due to the limited field size of our EBL system ($500\,\mu m \times 500\,\mu m$ in the Elionix ELS-F125), we encountered several stitching errors in our patterned layers. Stitching errors in the detector layers can be easily mitigated by integrating transition patches and manually setting the writing field locations. This was shown in Ref. [43]. Stitching issues can be pretty significant and impactful in the PIC layer, particularly in the directional coupler. Although manual field alignment and programmed shifts can partially solve the problem, getting a perfect/pristine photonic device was challenging. The stitching issues mentioned here can all be solved by fabricating the devices using an EBL with wider fields. This is now available at MIT.nano (Elionix HS-50). Although, it was not possible with this device. An example of stitching is shown in Fig.5-15(a). This SEM is from the center section of the 65-waveguide directional coupler. The top part of the coupler has narrower waveguides compared to the bottom. It is possible to notice the field stitching transition. Note that this device already implemented manual field alignment and overlaps to reduce stitching problems. As a matter of fact, this is a functional device, although it is far from perfect.

- **Cleanliness** As we will explain in Appendix A, substrate cleanliness is fundamental to yielding large-area devices. Our device has an area of $2.5\,mm \times 1.8\,mm$. Occasionally, particles were found to be responsible for devices short or open. This was likely because the nanofabrication tools were in different buildings, and the chip was transported out of the cleanroom several times during the fabrication. Fig.5-15(b) shows a cleanliness issue found in one of our devices. In this case, a residue was shorting parts of the delay line.

- **Misalignment** The 100 nm-wide nanowire detectors are aligned to 500 nm-wide waveg-

uides, over mm-long distances. While the alignment buffer is significant (200 nm on each side), field shifts and stitching issues might lead to severe misalignment. In Fig. 5-15(c), we show an example of misalignment from a functional device. We can observe that the detector is shifted up compared to the waveguide layer of about 100 nm. This shift does not impact the device's overall electrical functionality. Although, a larger shift could expose the detector to the etching region and lead to an electrically open section.

5.3.4 Characterization Setup

In Figure 5-16, we show a sketch of the measurement setups used to characterize the device. Sub-figure (a) shows the setup used to characterize the DC electrical properties and photon count rate curves. To measure the PCR we converted the differential readout into a single-ended readout using a balun (methods shown in Chapter 3). Sub-figure (b) shows the setup used to characterize the pulse traces and their timing properties. Here, we used the differential readout in combination with a real-time oscilloscope. We also acquired a reference optical pulse generated by a fast photodiode. In both setups, the detector is biased in a fully differential mode, using two bias tees and two room-temperature LNAs. We also included two cryogenic shunts to increase the bias margin of the detector. The chip is mounted on the same optical alignment platform presented in Sec. 5.2. A 4-channel telecom fiber array is mounted on a three-axis piezo-positioner pre-aligned at room temperature, monitored during the cooldown, and finally optimized at base temperature. In the sketches, we show the optical configuration used to calibrate and optimize the alignment through the loopback structure. To characterize the detector, the input is moved to channels 3 or 4 of the fiber array, interfaced to the left and central input of the 3-to-65 directional coupler, respectively. A picture of the setup mounted in the cryostat is shown in sub-figure (c). We highlighted the cryogenic shunts, the alignment platform, and the thermal braids to anchor the assembly to the 1 K stage of the cryostat. We also show the fiber array mounted on the Attocube tower and zoom on the chip-array interface during the alignment. Table 5.2 lists the instruments used in these setups.

5.3.5 Preliminary results

In this section, we present our preliminary results of the characterization of our device.

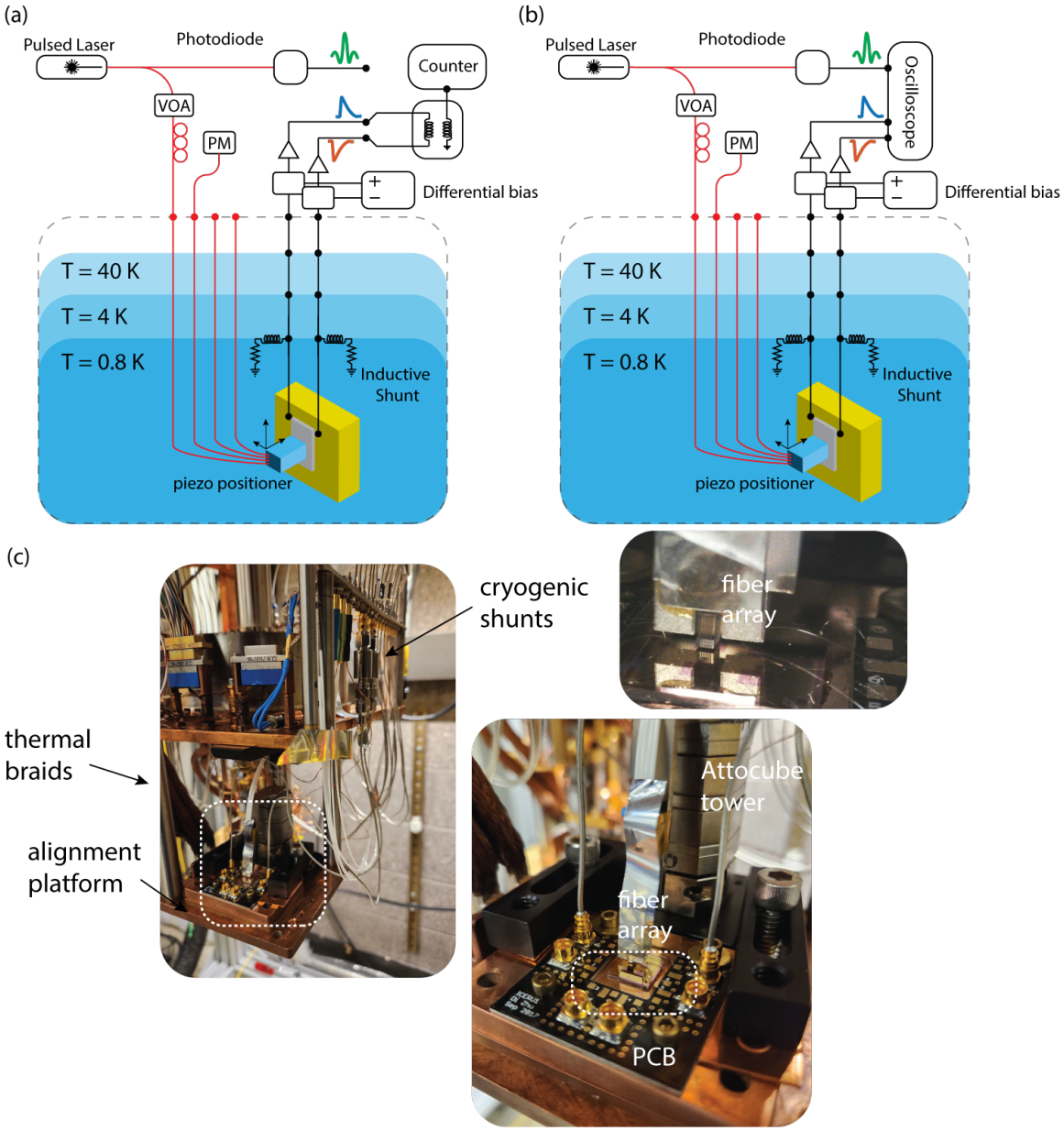

Figure 5-16: Characterization setups. (a) Sketch of the setup for DC characteristics and PCR measurement. (b) Sketch of the setup for pulse processing and jitter characterization. (c) Pictures of the optical coupling platform and details.

Reference	Instrument
Room temperature LNA	MITEQ 1 GHz
Real-time oscilloscope	LeCroy WavePRO 760i (6 GHz)
Variable optical attenuator	JDS Fitel HA1
Power meter	Thorlabs S155C
Inductive shunts	Custom: 1.1 µH + 50 Ω
Photodiode	Thorlabs DET08CL
Pulsed laser	Calmar Mendocino 1550 nm 40 MHz repetition rate
Universal counter	Keysight 53131A
Differential bias	SRS800 + 2 × 100 kΩ resistors
Balun board	Texas Instruments ADC-WB-BB/NOPB (4.5 MHz – 3 GHz)

Table 5.2: Overview of the instruments for the measurement setups shown in Fig. 5-16

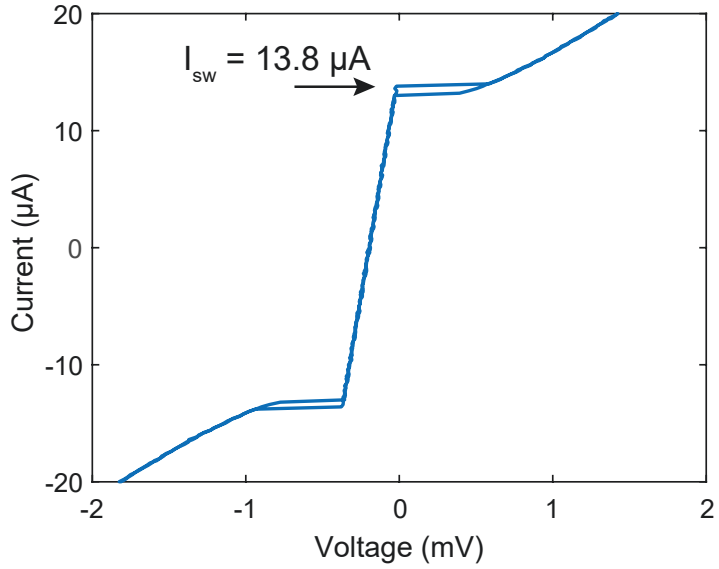

Figure 5-17: IV characteristic of the integrated 65-channel SNSPD at 1.3 K.

DC characteristics

We measured the switching current in a fully differential configuration using cold shunts. The setup is shown in Fig. 5-16(a). Figure 5-17 shows the IV characteristic of the device. The switching current I_{sw} at 1.3 K is 13.8 μA. The reduced hysteresis, due to the presence of the shunt inductors, suggests a reduced sustained Joule heating. This was suggested and shown in Ref. [181]. We note that the switching current is lower than the earlier demonstration of Ref. [43]. This is due to a lower thickness of the niobium nitride, which was specifically selected to obtain efficiency saturation at 1550 nm. The cryogenic shunts give about a 7% increase in bias margin, before the detector latches.

Optical alignment and loss calibration

Optical alignment was performed following a similar protocol as the LNSNSPD, in Section 5.2. After pre-alignment at room temperature, we monitored the coupling during cooldown, and we optimized it before measurement. We measured the grating coupler loss using the loopback calibration structure. The input optical power at 1550 nm was measured with a calibrated power meter $P_{\text{in}} = -15.357\,\text{dBm}$. After alignment optimization, the optical output power (coupled back to the grating coupler through the loopback) is $P_{\text{out}} = -47.253\,\text{dBm}$. Assuming negligible waveguide loss, the grating coupler loss is estimated to be $\eta_{\text{gc}} = -15.858\,\text{dB}$. We tested the polarization sensitivity of the grating coupler at the optimal coupling configuration. Fig. 5-18 shows the polarization extinction when moving the polarization paddles placed in the optical path towards the loopback input grating coupler. We used a 3-paddle manual polarization controller, where two paddles were set up to act as quarter-wave plates and one paddle as a half-wave plate. We started with an optimized polarization (measurement sample 1) and progressively rotated the three paddles to obtain a polarization state with minimal transmission through the input grating coupler. We obtained a polarization extinction of more than 30 dB. The sensitivity of the power meter limited our measurement. Using a stronger input optical power, we observed a polarization extinction of more than 50 dB. This measurement verifies that the measured power is effectively coupled in and out of the loopback structure and that the alignment is optimized.

Photon count rate

We sent light through the input grating coupler to measure the photon count rate. In this case, we selected the second/central grating coupler, aligned to the fiber array channel 4. We biased the detector at $0.72I_{\text{sw}}$ and supplied attenuated 1550 nm light. We first maximized the number of counts to the detector by moving the fiber array. In principle, the fiber array should be in the optimal position after alignment optimization on the loopback. However, small angles θ, could make the alignment suboptimal, as shown in Fig. 5-19(a). We moved the fiber array a few steps down and right, while checking the count rate on the detector, and we maximized its value. Then we operated the polarization paddles to verify polarization sensitivity. As shown in Fig. 5-19(b), we observed a maximum 3 dB

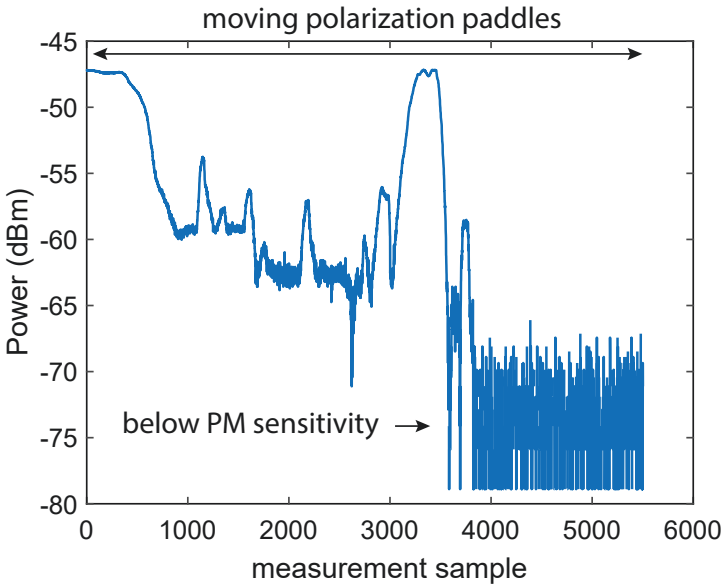

Figure 5-18: Polarization sensitivity of the loopback grating couplers.

extinction. Before alignment optimization, we did observe a smaller polarization sensitivity, confirming that the alignment was a little off due to θ rotations. We should expect a more significant polarization extinction based on the loopback measurement. Unfortunately, this result indicates the presence of spurious counts from the detector due to stray light, likely scattered by the fiber array.

We measured the photon count rate curve versus bias current for maximum polarization and optimized alignment. Fig. 5-20 show two PCR datasets, where we used (a) 70 dB attenuation (power to the detector < -101 dBm) and (b) 50 dB (power to the detector < -81 dBm). We can observe three main features.

- The PCR curve shape is independent of the optical attenuation, indicating a linear scaling in the device sensitivity.
- Differently from the preliminary device reported in Ref. [43], our SNSPD achieves a saturated behavior at 1550 nm.
- Similar to Ref. [43], the counts exponentially increase at $0.8I_{\mathrm{sw}}$. We speculate that at this bias level, the delay line separating the coupled pixel becomes sensitive to photons. Unfortunately, this also confirms our previous observation that the SNSPD is illuminated by stray photons, likely scattered from the fiber array.

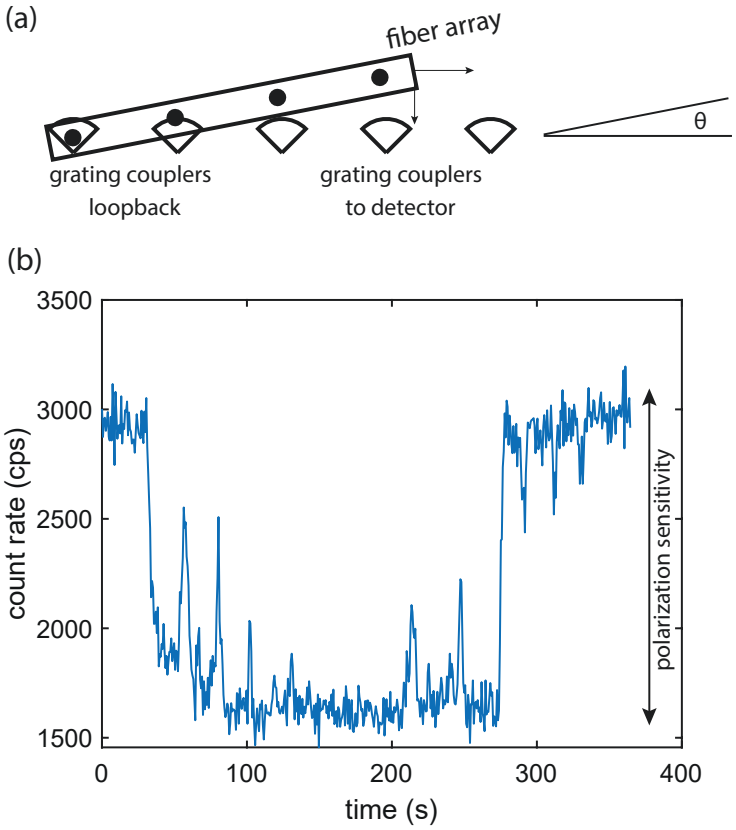

Figure 5-19: (a) Sketch showing misalignment due to unwanted rotations. (b) Detector polarization sensitivity.

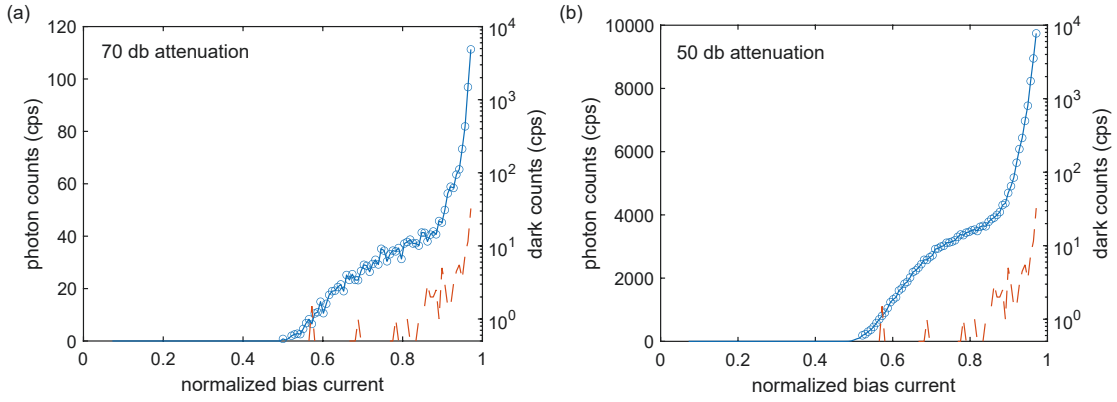

Figure 5-20: PCR curves for our device measured applying (a) a 70 dB optical attenuation and (b) a 50 dB optical attenuation, using a variable optical attenautor.

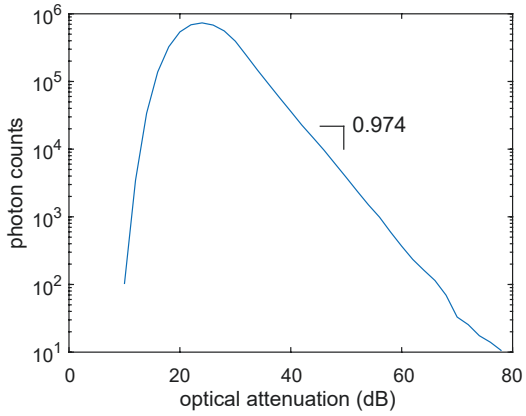

Figure 5-21: Linearity check for our device at 1550 nm biased at $0.72I_{\mathrm{sw}}$.

Linearity check

We performed a linearity check to prove the single photon detection regime. Fig. 5-21 shows that the device operates in a single-photon detection regime at both the selected attenuators, given the linear proportionality between attenuation and counts.

Characteristic detector pulses

We show here the characteristic pulses from the detector obtained when shining 1550 nm light with 70 dB optical attenuation into the second/central grating coupler. Fig. 5-22(a) shows the pulses in the differential configuration (setup (b) in Fig. 5-5). The characteristic ripple on the pulse is due to the limited impedance-matching taper bandwidth. In Fig. 5-22(b), we show the pulse obtained using the balun (configuration in setup (a) in Fig. 5-5). Note that this is equivalent to taking the difference between the differential pulses ($V_{\mathrm{pos}} - V_{\mathrm{neg}}$). However, the amplitude is lower due to the insertion loss of the balun. We fit the pulse decay with an exponential function and obtained a reset time constant $\tau \approx 501$ ns. From this fitting, the estimated inductance of our NbN detector is 117 pH per square. This agrees with a 5 nm-thick film. In Fig. 5-22(c), we show a zoom on the pulse rising edge for 100 pulses acquired with the balun. Note that the pulses have different heights based on the different absorption locations.

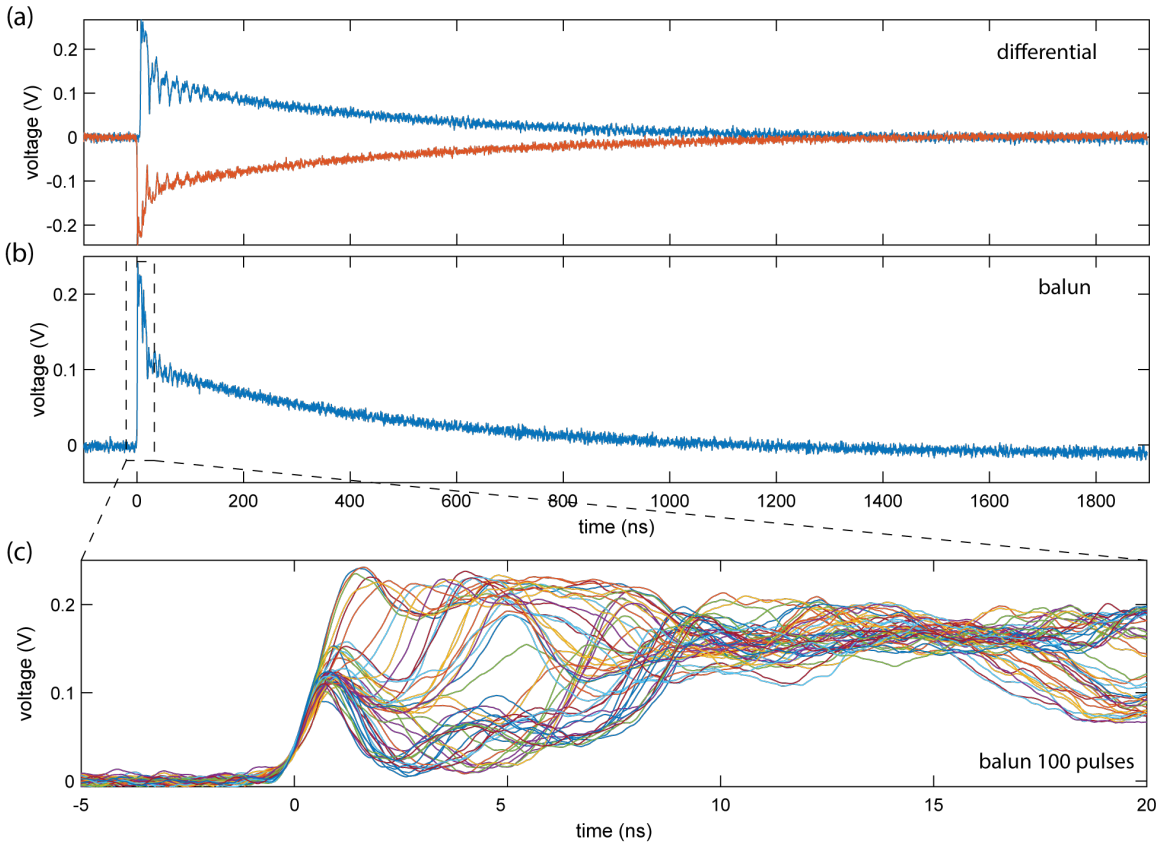

Figure 5-22: Characteristic detector pulse. (a) Differential pulsed. (b) Pulse from a balun readout. (c) Zoom in the balun pulse rising edge.

Differential pulses processing

In a delay-line multiplexed device, the differential pulses will appear at the readout with a certain relative delay based on the firing location. For example, pulses from pixel 33 will have a zero relative delay. Pulses from pixel 1 or 65 will have the maximum relative delay, corresponding to $64 \times t_{\mathrm{delay}} = 6.4\,\mathrm{ns}$, using values calculated with a thin-film sheet kinetic inductance of 80 pH per square. In Fig.5-23, we show the rising edge of the differential pulses collected at $0.65 I_{\mathrm{sw}}$ with 70 dB attenuation. Here we are triggering on the negative pulse. We can observe that the positive pulses dispose into several groups separated by a time delay. Each of these groups corresponds to a different pixel firing. We processed the pulses using the same procedure explained in Chapter III for the differential impedance matched single-pixel. In Fig.5-23(b), we plot the time difference $t_{\mathrm{diff}} = \frac{t_{\mathrm{pos}} - t_{\mathrm{neg}}}{2} = \frac{x_{\mathrm{p}}}{v_{\mathrm{ph}}} - \frac{L}{2v_{\mathrm{ph}}}$, where t_{pos} and t_{neg} are the time-tags of the positive and negative pulses corresponding to the threshold shown in the figure, x_{p} is the detection coordinate, and L is the length of the detector. Assuming a negligible geometric contribution in the elements, the relation can be expressed as:

$$t_{\mathrm{diff}} = N\, t_{\mathrm{delay}} - 64\, t_{\mathrm{delay}}/2 = 100[\,\mathrm{ps}]\, N - 3200[\,\mathrm{ps}] \tag{5.4}$$

where N is the pixel number. We fit the probability distribution of Fig. 5-23 to verify Eq. 5.4. Each pixel distribution is fit with a single Gaussian function. Fig. 5-23(c) zooms on the distribution of pixels 31, 32, and 33. We obtained $t_{\mathrm{diff}} = 137.4[\,\mathrm{ps}]\, N - 4495[\,\mathrm{ps}]$, which implies a $t_{\mathrm{delay}} = 137.4\,\mathrm{ps}$, giving a speed of light of 3.065 μm/ ps (1.02% c), corresponding to a sheet kinetic inductance of 113 pH per square. This value agrees with our expectations for a thin film and with the fitting to the reset pulse. Moreover, we also extracted the geometric contributions due to the pulse propagation in each single-pixel element, corresponding to the FWHM of each fitting Gaussian. On average, the propagation delay is about 55 ps. This value is larger than the maximum geometric contribution, 6.5 ps, expected for 100 nm-wide 20 μm-long detector element with a sheet kinetic inductance 113 pH per square. These results indicate that our measurement is impacted by additional contributions, which we mostly attribute to electrical noise jitter, as described in Chapter III. There are two other additional features that we want to point out. First, in Fig. [**?**](a), the output pulse do not all have the same amplitudes. We can note the leftmost/rightmost four pulse groups have a lower/higher amplitude than average, with increasing trends. We attribute this effect to

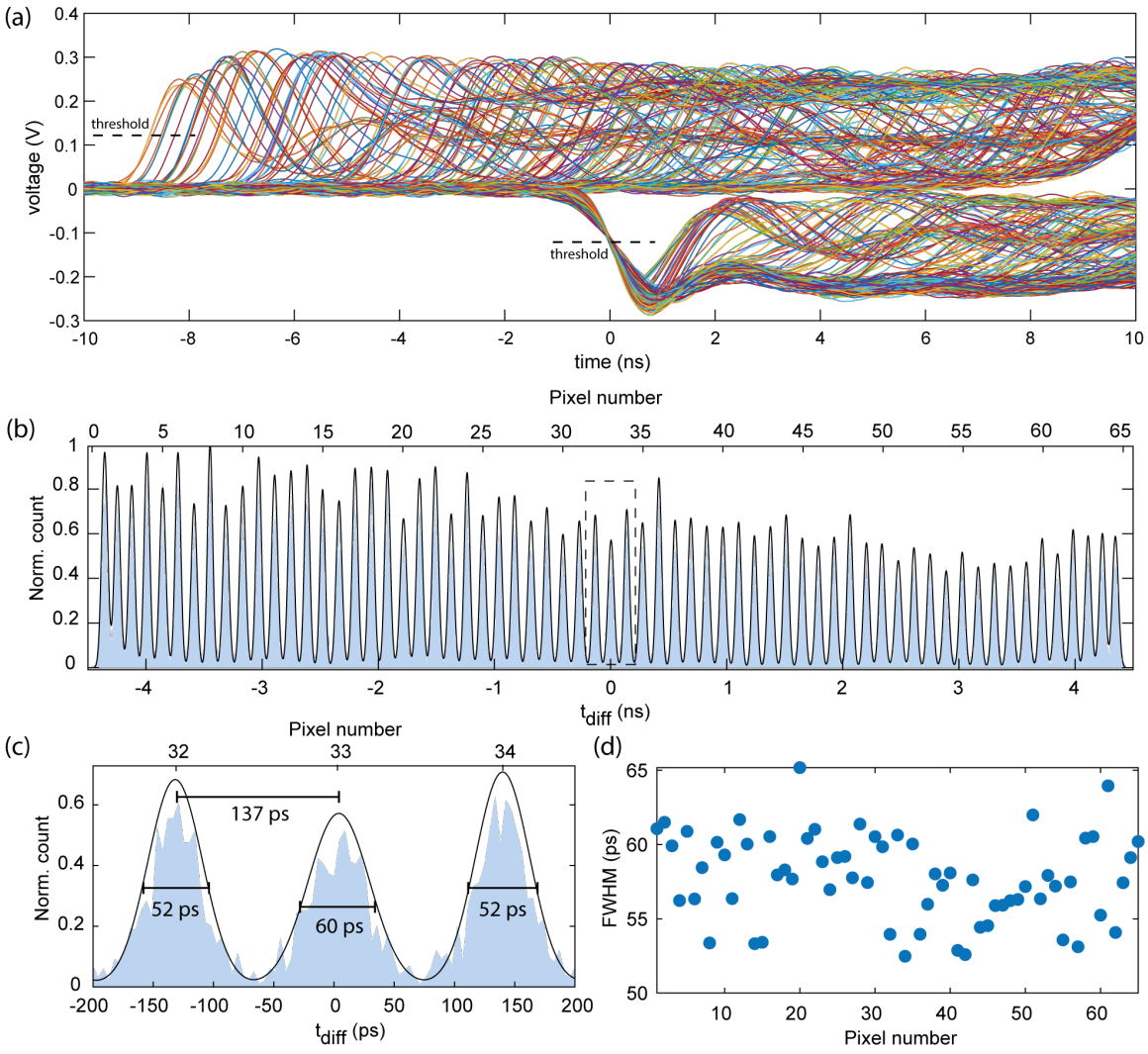

Figure 5-23: Differential pulse processing. (a) Positive and negative differential pulses collected at $0.65I_{\text{sw}}$ with 70 dB attenuation. The dashed line represents the threshold used to extract the time-tags; in this case, $V_{\text{threshold}} = 0.11\,\text{V}$. (b) t_{diff} distribution and Gaussian fitting. From here we can extract $t_{\text{delay}} = 137\,\text{ps}$. (c) Zoom on the distribution of pixels 32, 33, and 34. (d) FWHM of the t_{diff} distribution, i.e. jitter associated to t_{diff}.

the reflections from the taper sections, which mostly influence pulses from pixels closer to the array ends. Second, we note in Fig. [?](b) a non-uniform counting distribution across the array. As this observation is not accompanied by a similar trend in the FWHM of the Gaussian in Fig. [?](d), we attribute it to either a speckled pattern on the detector due to scattering or a non-uniform detection efficiency.

Finally, we studied the pulse distribution as a function of bias current, input polarization, and optical attenuation. In Fig. 5-24, we show the aggregated processed data. In particular, we plot the normalized distribution of the pixel photon count rate for several combinations of the parameters. Each dataset is processed from 50000 differential traces. There are a few results that are worth mentioning:

- For measurements with polarization minimizing the number of counts (min. polarization), we observe an almost flat count rate over the pixels. This indicates that the detector is flooded with scattered stray photons. For 70 dB attenuation, we observe a lower count rate towards the right of the distribution, indicating either a lower detector efficiency or a lower incidence of stray photons on the corresponding side.

- For measurements with 70 dB optical attenuation, we note that the counts from pixel 19 dramatically increase at 13 μA. This indicates that pixel 19 might be constricted and has a lower switching current than the other pixels.

- For both attenuations, when the polarization is tuned for the maximum number of counts (max polarization), we note that pixels 32 and 35 produce the largest number of counts. This is attributed to direct coupling through the PIC.

Unfortunately, we could not proceed with further experiments due to the present pulse dynamics and constricted pixels. We attempted to reduce the scattered photons by screening the detector elements, but we could not mitigate the problem. Moreover, the PIC does not behave as expected: injection of single photons in the directional coupler should result in patterns peaking towards the ends of the array. More details on the simulation are available in Ref.[43].

5.3.6 Conclusions

This section showed the successful fabrication of a 65-channel waveguide-integrated SNSPD array. We performed preliminary testing with coupled light into the photonic integrated

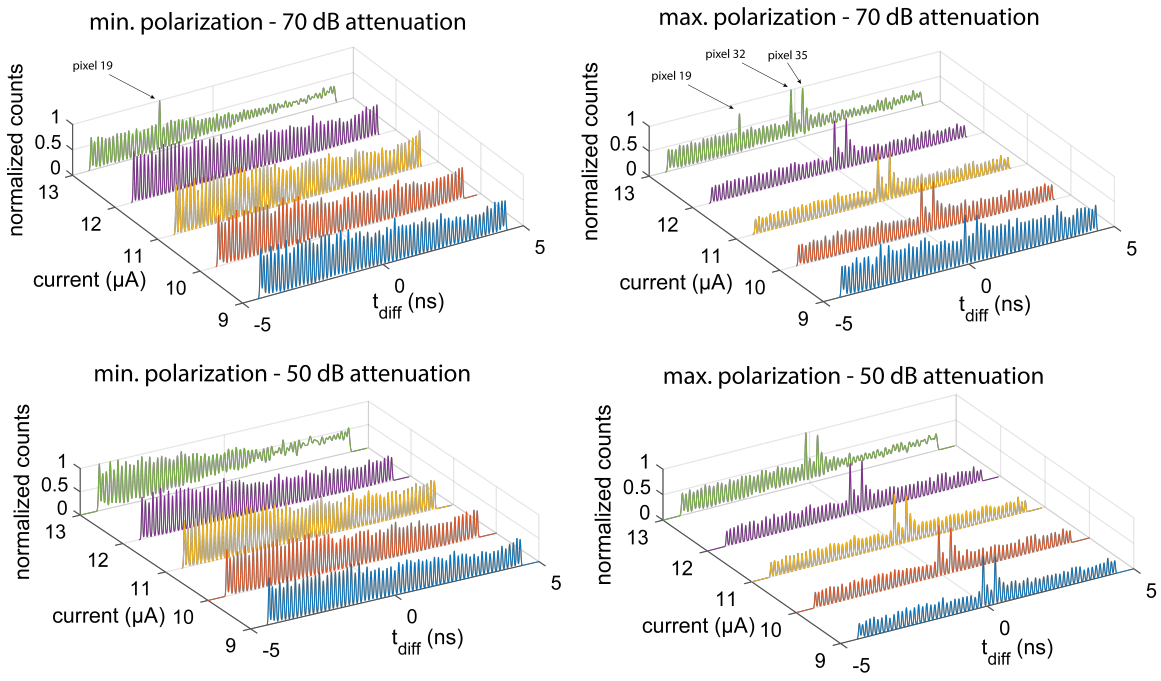

Figure 5-24: Detector response dynamics for several parameters: bias current, input polarization, and optical attenuation.

circuit and were able to observe the response to testing parameters. Unfortunately, our detector has constricted areas, is strongly affected by light scattering, and the PIC behaves suboptimally. A new fabrication round implementing specific design changes should result in a fully functional device. In particular, great attention should be placed on optimizing the photonic integrated circuit and the grating couplers to minimize light scattering. We believe a dramatic improvement could be achieved by isolating and protecting the detector; this could be achieved by extending the top ground plane and including an absorber to avoid scattered light impinging on the detector. The superconducting thin film, currently NbN, should be replaced with an amorphous material (e.g., MoSi) to minimize detector constrictions due to material imperfections. Moreover, a waveguide-first approach could be used here, with the same benefit shown with the LNSNSPD.

5.4 Summary and perspectives

In this chapter, we focused on integrating single-photon detectors on photonic platforms. We specifically addressed two critical challenges for realizing integrated quantum technology.

First, we demonstrated detector integration on thin-film LNOI with state-of-the-art de-

tection efficiency performance. LNOI is a promising integrated quantum photonics platform. However, the heterogeneous integration of detectors is exceptionally challenging due to the incompatibility of the lithium niobate platform with SNSPDs fabrication processes. Our work shows that one can fabricate integrated high-performance superconducting devices using an amorphous superconductor, a buffer interlayer, and a bottom-up fabrication approach. This demonstration opens the prospect of complex integrated circuits on this photonic platform. Moreover, our methods can be translated to other photonic platforms allowing streamlined heterogeneous integration of quantum detectors.

Second, we addressed the scalability of those integrated detectors. Larger and more complex quantum experiments will require thousands of integrated detectors. Direct-readout paradigm is unfeasible at scale due to the many external components required (cables, bias source, low-noise amplifiers). Here we showed that by implementing differential impedance-matched readout, combined with time-delay multiplexed architecture, we could read sixty-five integrated elements with just two readout lines, cables, and amplifiers. The number of integrable channels is limited by the measurement equipment's timing resolution and bandwidth and by large-scale fabrication capabilities.

Chapter 6

Summary and outlook

This thesis demonstrates the potential impact of superconducting nanowire devices, architectures, and engineering in microwave and photonics applications. Adopting this technology could help address the hardware scalability and integration challenges of superconducting and photonic quantum information processing and computing. Here we summarize the main results and discuss future directions.

Superconducting nanowire transmission line devices

Thin-film superconducting nanowires exhibit extraordinary microwave properties thanks to their high kinetic inductance. Transmission line architectures designed with superconducting nanowires have kΩ characteristic impedance, phase velocity just a tiny fraction of the speed of light in vacuum (about 1%), and experience extreme compression of the microwave wavelength (about 100 times).

By exploiting these characteristics, we demonstrated an ultra-compact tunable 3 dB forward directional coupler, operating at 5 GHz, based on coupled nanowire transmission lines in a covered microstrip architecture. Many other cryogenic microwave distributed components (e.g., hybrids, interferometers, phase shifters) can be built using the same concepts and architectures. The natural cryogenic operation, exceptional compressed footprint, material compatibility, and virtual zero power operation may allow direct integration with superconducting quantum computing platforms as a signal processing and routing technology. We suggested a direct application of our coupler with nanowire-based phase-shifters [34] to create a programmable MZI-based linear matrix-vector product processor in the microwave

domain [118]. The footprint reduction achieved with our structures could make this possible.

We also showed that combining high kinetic inductance nanowires with exotic ultra-high dielectric constant substrates can decrease the impedance to 50 Ω and boost the microwave compression even more. We demonstrated 100 µm-long 50 Ω coplanar waveguide stub resonators at GHz frequencies, made with superconducting nanowires fabricated on strontium titanate on silicon, achieving a footprint reduction of about 200 times.

A promising future direction is combining superconducting nanowires with dielectric substrates exhibiting non-linear properties, such as ferroelectrics, piezoelectrics, and electrooptics. Examples of these platforms are: aluminum nitride, lithium niobate, strontium titanate, lead zirconate titanate, hafnium zirconium dioxide, etc. Coupling the properties of kinetic inductive nanowires with these substrates might lead to non-linear non-reciprocal devices with applications in quantum transduction and sensing. Traveling wave parametric amplifiers, circulators, and transducers could be realized towards a complete nanowire-based superconducting MMIC technology.

Impedance-matched differential single-photon detectors

We engineered the nanowire microwave properties and transmission lines architectures for application in single-photon detection. We demonstrated SNSPDs with differential impedance-matched readout achieving state-of-the-art system detection efficiency, sub-10 ps system jitter, photon-number resolution, and imaging capabilities, all in the same design. This architecture breaks the trade-off in detector performances typical of traditional designs. Our prototype devices are currently in use in single-photon LIDAR experiments [158], quantum information processing [159], and proposed as an experimental platform to probe fundamental superconducting nanowire switching phenomena [160]. We expect widespread adoption of the differential design in demanding applications needing an all-rounder single-photon detector technology. A promising future direction is the on-chip integration of the external processing electronics (balun, comparator, amplifiers) and quenching circuits with the detectors, possibly using monolithic nanowire-based superconducting elements. Minimizing external electronics and redesigning cabling and interconnects towards high-density architectures will reduce the deployment cost per channel and enable lower SWaP systems. This could help to scale experiments and applications which currently require and use tens to hundreds of free-space coupled detectors [26, 161].

Waveguide-integrated SNSPDs

We demonstrated the integration of superconducting nanowire detectors on photonic platforms. Our molybdenum silicide SNSPD integrated on a lithium niobate waveguide has one of the highest on-chip detection efficiency reported on this platform to date. Our fabrication methodology is based on a bottom-up approach and exploits protection buffer layers to solve the challenging interface between lithium niobate and superconducting processing. The same fabrication process can be used to integrate several other nanowire elements on the same platform. For example, by combining detectors with nanowire processing electronics (logic circuits [31], amplifiers [29], memories [34]), and interfacing them to optoelectronics devices on lithium-niobate, one could realize quantum interconnects and feed-forward architectures which are fundamental for advanced protocols in quantum communications and networking [182, 178]. The adoption of nanowire technology has the potential to enable the scalability of quantum information processing architectures toward the realization of functional quantum networks.

We also demonstrated the integration of a 65-element nanowire detector array on a silicon photonic platform. The array is based on a time-delay multiplexed architecture in combination with differential impedance-matched readout. We showed successful optical coupling and preliminary testing, Unfortunately, due to design and fabrication imperfections, we could not complete the full experiments. Immediate improvements could result in a fully functional device demonstrating the integration of scalable quantum detectors for large-scale experiments. Current quantum-advantage experiments rely on free-space optical components and detectors [26]. Our demonstration shows that it is possible to scale those experiments with on-chip integration.

Appendix A

Fabrication technology for superconducting nanowires

The nanowire-based devices shown in this thesis were all fully or partially nanofabricated in the MIT cleanrooms. A significant portion of the project time was spent optimizing the fabrication processes for these devices.

In this Appendix, I will report a few fundamental nanofabrication procedures and details, focusing primarily on electron-beam lithography (EBL). EBL is fundamental for fabricating superconducting nanowires, particularly at this academic research level. I will also discuss cleaning, direct-writing photolithography for liftoff, process development optimization, and metrology. It is essential to mention that etching is also a fundamental process for superconducting nanowires: optimizing the etching chemistry, rate, and mask is key to ensuring a good yield. With the discontinuation of the Nanostructure Laboratory (NSL), the etcher used for the fabrication of the devices shown in this work was also discontinued in favor of modern etching systems. For this reason, I am not going to discuss etching in this Appendix, as the specific information would be obsolete.

This Appendix serves as a guide and a reference for other researchers approaching the fabrication process of superconducting nanowires.

A.1 Cleaning

Cleaning is fundamental for successfully fabricating the superconducting nanowire structures shown in this thesis. Our devices include both nanometric (e.g., nanowire) and micrometric

(e.g., tapers) features, spanning several millimeters in interconnected large-area formats. For this reason, preserving cleanliness during fabrication and over the device area is of fundamental importance. The functionality of our large-area devices might be compromised by just a single nanometric particle shorting terminals/sections. Here, we mention three cleaning stages crucial for nanowire fabrication:

- **Pre-deposition**. It is important to start with a clean substrate to avoid contaminating the sputtering chamber and ensure good quality and homogeneity of the thin film.

- **Post-deposition**. Post-deposition cleaning could be important if the dedicated sputtering chamber is outside the cleanroom.

- **Post-process**. Resid residue cleaning is always recommended to facilitate wire bonding and measure true device performance.

A.1.1 Pre-deposition cleaning

When possible, we perform a thorough pre-deposition substrate cleaning. These steps should be customized based on the chemical compatibility of the material and targeted at the type of contaminants to be cleaned/removed. Typical processes for silicon wafers are RCA standard cleaning, piranha solution, and hydrofluoric acid (HF) dips. More information on wafer cleaning is available in Ref. [183]. These harsh cleaning processes are incompatible with superconducting thin films and should only be performed before deposition. Whenever a thorough wafer cleaning is impossible (e.g., the substrate is pre-patterned), we run the solvent cleaning described below.

A.1.2 Post-deposition solvent cleaning

For reference we report here our standard solvent cleaning procedure.

1. Sonication in Acetone - 5 minutes

2. Sonication in Iso-Propyl Alcohol (IPA) - 5 minutes

3. Blow dry with N_2 gun.

This cleaning procedure is run before and after superconducting thin-film deposition, and whenever necessary. This is particularly important for the devices reported in this thesis: the sputtering system is located outside the cleanroom so as to limit access to just the group members and minimize internal contamination. Unfortunately, by doing so, deposited wafers are exposed to external environment, making cleaning necessary after deposition before proceeding to lithography.

A.1.3 Post-process cleaning

To remove post-lithography and processed resist residues, we place the samples in a bath of N-Methyl-2-pyrrolidone (NMP). An overnight bath at room temperature is often enough for unetched resists (e.g., cleaning or liftoff). For etched resist or to improve the effectiveness, heating the bath to 70 °C gives noticeable results. Note that NMP is not compatible and ineffective with hydrogen silsesquioxane (HSQ). After exposure/baking, HSQ is turned into a low-density oxide. A standard solvent clean is also recommended after the NMP process.

A.2 Electron-beam lithography processes

Electron-beam lithography (EBL) is an established technique to pattern nanometric structures by scanning a focused beam of electrons on an electron-sensitive resist film. While it is not suitable for industrial application levels yet, due to its low throughput, it is a fundamental tool for academic research. For details on EBL technology, we refer the readers to a few publications and reviews on the topic: [184, 185]. Here we focus on EBL applications for superconducting nanowire applications.

A.2.1 Nanowire fabrication flows

In Fig. A-1, we introduce two fabrication flows for electron-beam lithography of superconducting nanowires. The two flows differ just in the tone of the electron-beam resist: positive or negative. It is essential to mark this difference: selecting a negative vs. positive resist might significantly impact the pattern's final quality and the exposure time. Before going into the details, one crucial remark is necessary: all our processes are "superconducting thin-film first." To ensure the quality and long-term reproducibility of our thin-film compounds, we do not allow the introduction of polymers in the superconductor sputtering chambers.

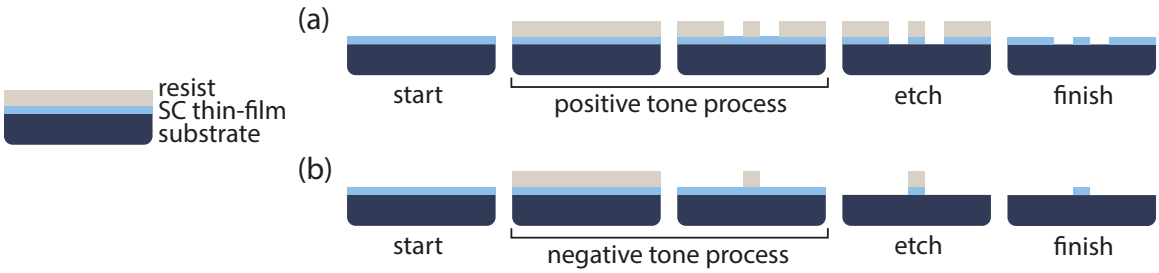

Figure A-1: General fabrication flows. (a) Positive tone fabrication flow. (b) Negative tone fabrication flow

This imposition precludes the use of lift-off techniques to define superconducting structures. For this reason, all our processes start with depositing a blanket layer of the superconducting thin film of choice and end with an etching step.

Positive-tone fabrication flow This process flow uses positive-tone EBL. In positive-tone processing, the mask is the inverse of the target structure, Fig.A-1(a). Positive-tone processing is advantageous when the target structure is large (pads, multi-element circuit), in the creation of a CPW geometry, and when the substrate or the superconducting thin film does not tolerate harsh development chemistry.

Negative-tone fabrication flow This process flow uses negative-tone EBL. In negative-tone processing, the mask is the same as the target structure, Fig.A-1(b). Negative-tone processing is advantageous when extreme resolution is required ($< 30\,\text{nm}$) and when the target structure is relatively small (single element, a few elements circuit).

A.2.2 Positive-tone processes

This section describes the process flow and general operating procedure details for selected positive tone resists. In general, positive resists require a lower dose than negative tone resists, and it is often convenient to consider fabricating devices in this process. To do so, one needs to take the inverse of the mask to be patterned or to define an etching outline around the target structures. For example, a straightforward application is patterning coplanar geometry structures. With a positive tone, one writes the CPW gaps instead of patterning the center conductor and the ground layers, resulting in a much shorter write.

The process recipes below should result in successful exposure with a 5 nm-thick NbN

film sputtered on top of 300 nm-thick thermal oxide on 500 µm-thick silicon substrate. The processes are calibrated on an Elionix ELS-F125 tool.

ZEP-520A

ZEP-520A is a high-resolution positive-tone electron beam lithography resist from ZEON Inc. Below is our standard process.

1. **Solvent clean** Solvent clean the substrate.
2. **Dispense ZEP-520A** Cover about 1/2 of the sample diameter.
3. **Spin** 5000 RPM for 60 seconds with maximum acceleration (300 nm thick layer).
4. **Bake** 180 °C for 90 seconds.
5. **EBL Dosing** 550 µC cm^{-2} with 125 kV EBL
6. **Cold development** o-Xylene at 5 °C for 90 s followed by IPA at room temperature for 30 s
7. **Dry** Nitrogen gun dry
8. **Inspect** Optical microscope on larger features to check for under-development
9. **Etch** Etching process of choice OR **Deposition** Electron-beam evaporation of metallic layer
10. **Clean** OR **Lift-off** Overnight NMP at 70 °C
11. **Inspect** Scanning electron microscopy

Fig. A-2(a) and (b) show the result of this standard process after etching and cleaning. This process was calibrated to fabricate 100 nm-wide structures to be transferred into NbN with a 50 W CF_4 reactive ion etching process. The thickness of the mask can be tuned by reducing the spin speed, and in turn, by adjusting (shortening) the time of cold development in o-Xylene. We developed a modified process recipe for 500 nm-thick ZEP-520A to etch silicon in SF_6 plasma. The spin speed was 2500 RPM, and the cold development time in o-Xylene was adjusted to 135 seconds. Fig. A-2(c) shows the result after etching and cleaning.

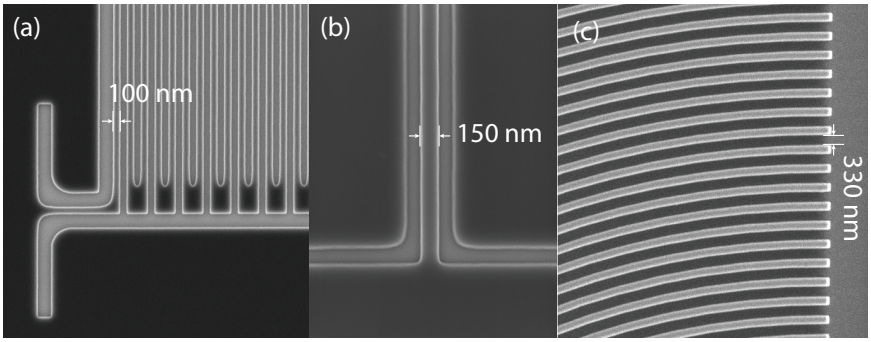

Figure A-2: Examples for ZEP-520A process. (a-b) Standard process after etching and cleaning. (c) Results from thicker ZEP-520A process after etching and cleaning

ZEP-530A

ZEP-530A is based on a similar formulation to ZEP-520A but has a lower polydispersity and a lower concentration of soluble molecules without irradiation [186]. These characteristics make it slightly less sensitive than ZEP520A but more uniform in dense patterns with small half-pitch structures. In a comparative study across the ZEP resist family, Nakajima et al. [186] successfully demonstrated a 18 nm half-pitch grating using ZEP530A in combination with development in ZED-N60. Our standard process:

1. **Solvent clean** Solvent clean the substrate.
2. **Dispense ZEP-530A** Cover about 1/2 of the sample diameter
3. **Spin** 5000 RPM for 60 seconds with maximum acceleration (140 nm thick layer)
4. **Bake** 180 °C for 90 seconds
5. **EBL Dosing** 600 $\mu C\,cm^{-2}$ with 125 kV EBL
6. **Cold development** o-Xylene at 0 °C for 60 s followed by IPA at room temperature for 30 s
7. **Dry** Nitrogen gun dry
8. **Inspect** Optical microscope on larger features to check for under-development
9. **Etch** Etching process of choice OR **Deposition** Electron-beam evaporation of metallic layer
10. **Clean** OR **Lift-off** Overnight NMP at 70 °C

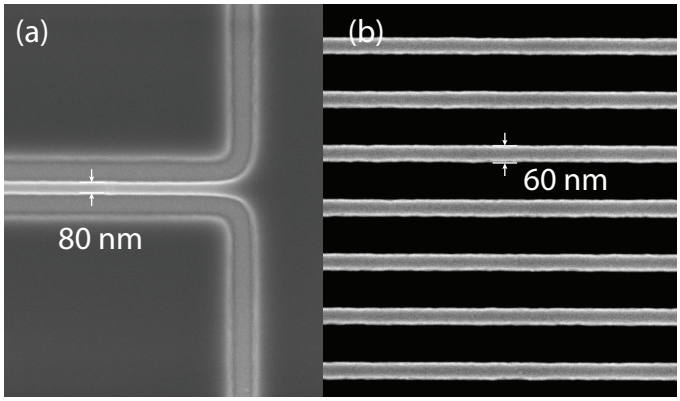

Figure A-3: Examples for ZEP-530A process. (a) Standard ZEP-530A process before etching and cleaning. (b) Diluted ZEP-530A process after etching and cleaning

11. **Inspect** Scanning electron microscopy

Fig .A-3(a) shows the result of the standard process after etching and cleaning. To fabricate narrower nanowires, we calibrated a process for thinned ZEP-530A. We diluted the resist with Anisole 1:1 in volume. At 5000 RPM this dilution spins to 68 nm. We adjusted the cold development time in o-Xylene to 30 seconds. Fig.A-3(b) shows the result for diluted ZEP-530A after etching and cleaning.

Insulating substrates

Electron-beam lithography on insulating substrates might be extremely tedious due to charging issues. We suggest modifying the processes above to include a conductive discharge layer to mitigate these problems. In our process, we successfully used All-Resist AR-PC 5090.02 (Electra-92). The modified ZEP-530A process for insulating substrates:

1. **Solvent clean** Solvent clean the substrate.
2. **Dispense ZEP-530A** Cover about 1/2 of the sample diameter
3. **Spin** 5000 RPM for 60 seconds with maximum acceleration (140 nm thick layer)
4. **Bake** 180 °C for 90 seconds
5. **Warm-up** Electra-92 is stored at 5°C. We suggest warming the chemical to room temperature, for consistent spins
6. **Dispense Electra-92** Cover about 1/2 of the sample diameter

7. **Spin** 2000 RPM for 60 seconds with maximum acceleration (60 nm thick layer)
8. **Bake** 90 °C for 60 seconds
9. **EBL Dosing** 600 $\mu C\,cm^{-2}$ with 125 kV EBL
10. **Electra-92 Rinse** DI water for 60 seconds
11. **Cold development** o-Xylene at 0 °C for 60 s followed by IPA at room temperature for 30 s
12. **Dry** Nitrogen gun dry
13. **Inspect** Optical microscope on larger features to check for under-development
14. **Etch** Etching process of choice OR **Deposition** Electron-beam evaporation of metallic layer
15. **Clean** OR **Lift-off** Overnight NMP at 70 °C
16. **Inspect** Scanning electron microscopy

A.2.3 Negative-tone processes

This section describes the process flow and general operating procedure details for selected negative tone resists. These resists have a higher dose compared to positive tone layers. However, they can achieve higher resolution and better line-edge roughness [187]. The process recipes below should result in successful exposure with a 5 nm-thick NbN film sputtered on top of 300 nm-thick thermal oxide on 500 µm-thick silicon substrate.

HSQ and FOx

HSQ, short for hydrogen silsesquioxane, is a popular negative-tone electron beam resist. It's not a conventional resist because it's not an organic polymer. It's a spin-on-glass material that leaves behind a SiO_2-like layer in exposed areas after development. HSQ processes can achieve extreme resolutions in the single-digit nanometer [185, 188]. However, it is challenging to store (requires refrigeration at −60 °C, if not lower) and has a fairly short shelf-life. It is sometimes referred to as FOx (flowable oxide), the old-trade name. The thickness of a spun layer can vary a lot depending on its concentration: it is dissolved in

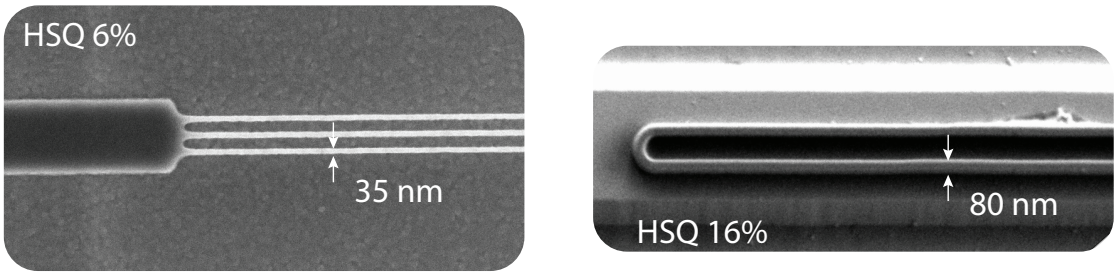

Figure A-4: Example of feature fabricated with HSQ at 6% and 16% concentration.

methyl isobutyl ketone (MIBK). Cleanroom facilities (e.g., MIT.nano) provide pre-diluted HSQ vials with 2%, 4%, 6%, and 16% concentration. Within this range, one can achieve layers between 40 nm and 600 nm. Our standard HSQ process:

1. **Solvent clean** Solvent clean the substrate.
2. **Warm-up** Warm up the HSQ vial to room temperature.
3. **Dispense HSQ** Cover about 1/2 of the sample diameter
4. **Spin** 6% concentration at 3000 RPM for 60 seconds with maximum acceleration (140 nm thick layer)
5. **EBL Dosing** 4000 $\mu C\,cm^{-2}$ with 125 kV EBL
6. **Development** 25% Tetramethylammonium Hydroxide (TMAH) for 120 s followed by IPA at room temperature for 30 s
7. **Dry** Nitrogen gun dry
8. **Etch** Etching process of choice
9. **Inspect** Optical microscopy on larger features or scanning electron microscopy

In Fig.A-4, we show an example of a 35 nm feature fabricated with the process above using 6% HSQ, and an 80 nm feature fabricated with 16% HSQ. A few important details:

- TMAH (i.e., the developer) is a highly hazardous chemical and should be handled with extreme care at these concentrations. An alternative developer is the *Salty Developer* [188]. However, it requires a larger dose (about 2.5 times higher).

- A prolonged exposure of NbN to TMAH might lead to degraded superconducting properties. TMAH reacts with Nb to form niobium salts, reducing the film's thickness [189].

- HSQ process results are highly dependent on its time-to-expiration. Using expired or close-to-expiration or poorly-stored HSQ might lead to unsuccessful or unreproducible results.

- The required dose is quite high and might lead to long write times. The dose might be reduced with a pre-baking process. However, this will lead to a slightly degraded resolution.

Low contrast HSQ process

We modified our standard HSQ process to fabricate dielectric spacers with sloped sidewalls. In this case, we introduce a high-temperature baking step to pre-cure the resist and reduce its contrast. More details are available in [190]. Here we provide an outline of the process.

1. **Solvent clean** Solvent clean the substrate.

2. **Warm-up** Warm up the HSQ vial to room temperature.

3. **Dispense HSQ** Cover about 1/2 of the sample diameter

4. **Spin** 16% concentration at 3000 RPM for 60 seconds with maximum acceleration (450 nm thick layer)

5. **Bake** 250 °C for 90 seconds

6. **EBL Dosing** $3000\,\mu C\,cm^{-2}$ with 125 kV EBL

7. **Development** < 5% Tetramethylammonium Hydroxide (TMAH) for 90 s + DI water rinse + IPA rinse. Standard photoresist developers (CD-26, MIF 321), satisfy this requirement

8. **Dry** Nitrogen gun dry

9. **Inspect** Optical microscopy on larger features or scanning electron microscopy

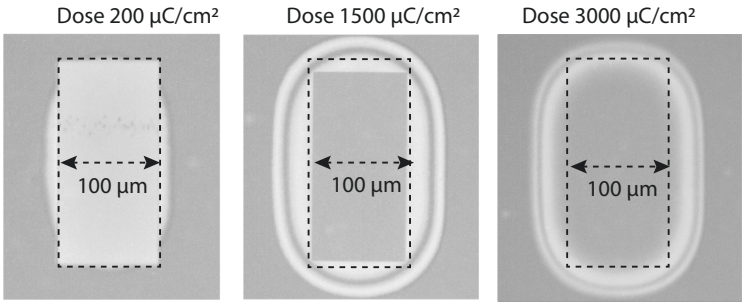

Figure A-5: Low-contrast HSQ process.

In Fig.A-5, we show an example of a 100 μm-wide 450 nm -thick HSQ spacer fabricated with 16% concentration resist and exposed with 3 different doses. The rectangular shape vanishes at 3000 $\mu C\,cm^{-2}$, and the sidewalls show a pronounced curvature. We used this process to fabricate dielectric spacers and avoid using other oxide deposition processes (e.g., PECVD), which could degrade the properties of our superconductor.

ma-N 2401

As mentioned in the previous section, HSQ is the best resist for high-resolution applications. However, it has several downsides in high dose requirements, dangerous development chemistry, and short shelf life. ma-N 2400 series is a polymer-based negative tone resist. It is an excellent alternative to HSQ with features down to 18 nm. More details are available at [191]. Our standard process is as follows:

1. **Solvent clean** Solvent clean the substrate.
2. **Dispense ma-N 2401** Cover about 1/2 of the sample diameter
3. **Spin** 3000 RPM for 60 seconds with maximum acceleration (100 nm thick layer)
4. **Bake** 90 °C for 60 seconds
5. **EBL Dosing** 1000 $\mu C\,cm^{-2}$ with 125 kV EBL
6. **Development** $< 5\%$ Tetramethylammonium Hydroxide (TMAH) for 10 s + DI water rinse
7. **Dry** Nitrogen gun dry

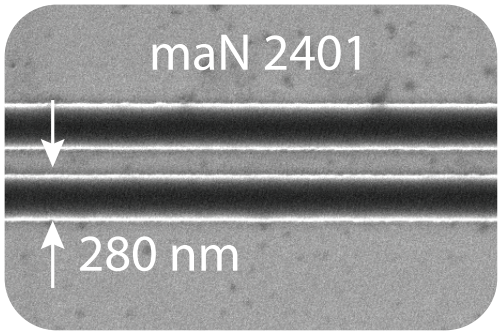

Figure A-6: maN 2401 process.

8. **Etch** Etching process of choice

9. **Clean** Overnight NMP at 70 °C

10. **Inspect** Optical microscopy on larger features or scanning electron microscopy

The development time, which is fairly short in the current version of the process, can be increased with a longer baking time. In Fig.A-6, we show an example of a 280 nm-wide line fabricated with the ma-N process. In Ref. [191], we showed features down to 18 nm with the process above.

A.3 Direct-write photolithography

Electron-beam lithography is a direct-write technique. The corresponding technology for photolithography is the so-called direct-write (photo)lithography (DWL). A popular DWL tool is the Heidelberg MLA-150, which is starting to be available in several academic fabrication sites. In this case, a laser is scanned, projected, or both at the same time, to write the layout features. DWL is gaining popularity in applications requiring fast prototyping as it removes the necessity of writing a mask for every layout. Here, we report two DWL processes for metallic layer patterning via lift-off. The process are calibrated for Heidelberg MLA-150 tools equipped with 375 nm sources.

A.3.1 Positive-tone photolithography

In the following, we report a photolithography process using positive tone photoresists. We use a bilayer stack with PMGI SF9 and Shipley S1813. The bilayer is needed to produce an

undercut and obtain a good liftoff.

1. **Solvent clean** Solvent clean the substrate.
2. **Dispense PMGI-SF9** Cover about 1/2 of the sample diameter
3. **Spin** 4500 RPM for 60 seconds with maximum acceleration (500 nm thick layer)
4. **Bake** 180 °C for 90 seconds
5. **Dispense S1813** Cover about 1/2 of the sample diameter
6. **Spin** 4500 RPM for 60 seconds with maximum acceleration (1.2 µm thick layer)
7. **Bake** 100 °C for 90 seconds
8. **MLA Dosing** 160 mJC cm^{-2} at 375 nm
9. **Development** AZ726 for 80 s + DI water rinse
10. **Dry** Nitrogen gun dry
11. **Inspect** Optical microscopy
12. **Deposition** Deposition of metal layer
13. **Lift-off** Overnight NMP at 70 °C
14. **Inspect** Optical microscopy

Fig. A-7 shows the results for this bilayer positive tone process after liftoff of 10 nm titanium + 50 nm gold evaporated layers.

A.3.2 Negative-tone photolithography

In the following, we report a photolithography process using a negative tone photoresist. We use nLOF 2035. Unlike the positive-tone process above, nLOF resist is specifically designed for liftoff applications and features a natural undercut after development. Therefore, it does not require an underlayer.

1. **Solvent clean** Solvent clean the substrate.
2. **Dispense nLOF 2035** Cover about 1/2 of the sample diameter

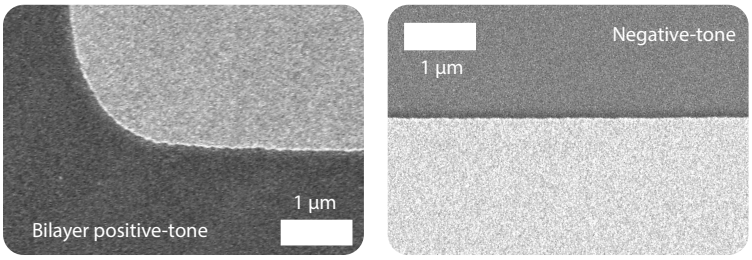

Figure A-7: Lift-off results for 10 nm Ti + 50 nm Au with DWL process. (a) Bilayer positive tone. (b) Negative tone.

3. **Spin** 3000 RPM for 60 seconds with maximum acceleration (3.5 µm thick layer)
4. **Bake** 100 °C for 90 seconds
5. **MLA Dosing** 300 mJC cm^{-2} at 375 nm
6. **Post Bake** 100 °C for 90 seconds
7. **Development** AZ726 for 90 s + DI water rinse
8. **Dry** Nitrogen gun dry
9. **Inspect** Optical microscopy
10. **Deposition** Deposition of metal layer
11. **Lift-off** Overnight NMP at 70 °C
12. **Inspect** Optical microscopy

Fig. A-7 shows the results for this negative process after liftoff of 10 nm Titanium + 50 nm Gold evaporated layers.

A.4 Process Optimization

A large portion of the effort in developing the processes described above consists of their tuning and optimization. There is no established rule in process development. However, in the following, I will delineate the general principles I followed to design my lithography processes.

Preliminary steps Before going into a trial-and-error mode, there are a few preliminary steps extremely useful when designing a nanofabrication process:

1. **Read the datasheet** Most resist companies provide a suggested process that should give benchmarked resolution. The initial process could be a great starting point.

2. **Read the MSDS** Most of the time, resists comes with proprietary developers and removers. The MSDS will contain the principal chemicals of those solutions. Often, those solutions are based on common chemicals already available in the cleanroom facility. For example: resist removers are often based on NMP, ZEP developers are often based on o-Xylenes and hexyl acetate. These are generally available in cleanrooms. If the resist material is unknown, the MSDS might shed some light on its chemical composition and drive further process development

3. **Run quick calculations** Most of the time, the processes provided on the datasheet are calibrated for tools with different characteristics. For example, EBL processes are often calibrated at 50 kV, while MIT.nano and Harvard CNS have popular high-resolution 125 kV tools. While the resist dose does not scale linearly with acceleration voltage, an initial guess based on linear scaling is acceptable. The required dose for similar perfomance with a 50 kV system is about 40% the dose at 125 kV.

4. **Ask your peers and check literature** Often, someone has already tried the process and the results are shared in the literature. Often in the supplementary materials.

Trial-and-error The preliminary steps will provide a first starting point for the process parameters. The datasheet will likely give out spin curves, baking temperature, and times.

1. **Compose a test pattern** Compose a small 1-field test pattern including at least the smallest and the average target feature.

2. **Use the actual substrate** To better estimate the process parameters, use the substrate of interest (instead of a simple dummy silicon sample). This will also allow estimating proximity effects early in the process, instead of performing a secondary correction. If the substrate is insulating, include a discharge layer in the process. If the pattern is dense, consider using proximity effect correction strategies.

3. **Select an appropriate beam current and a number of points** It is important to select the correct beam current and discretization for the needed resolution. For example: if 50 nm is the target resolution, we will need a small current with a small beam waist (e.g. 500 pA in Elionix ELS-F125 has a beam waist of about 1.7 nm), and a fine discretization (e.g. 1 nm shots).

4. **Dose range** Set a dose sweep with ±50% the guessed/suggested dose, in reasonable increments.

5. **Development** After exposure (and post-bake if required), start developing with half the guessed/suggested development time. Keep developing with manageable increments until some test doses and desired features are correctly developed.

6. **Inspect** It is essential to have a way to inspect the sample. If in-process inspection is impossible, multiple samples developed for different times, followed by a final inspection, will serve the same purpose.

Following the steps above should result in quick process development.

A.5 Process metrology

Process metrology is fundamental to estimating fabrication yield and informing following process optimization. Here, we show an example of direct applications of metrology techniques to analyze the process variation for the diluted ZEP-530A recipe reported above. This process was calibrated to fabricate large-area ultra-narrow nanowire meanders for single-photon detection in the mid-IR band. For these applications, it is fundamental to yield single-photon detectors with a critical current reaching a high fraction of the theoretical depairing current ($> 50\%$). When the width of the nanowire becomes narrower (< 100 nm) - this is required to increase the sensitivity to mid-IR [72] - defects induced by fabrication or intrinsic to the material will have a significant impact on the current carrying capability of the nanowire. To yield a detector with saturating efficiency in the mid-IR, minimizing these defects is essential [187]. Here we focused on trying to decrease the post-fabrication line-width roughness. We followed the empirical method described in the previous section to calibrate our lithography process. In particular, we started with the parameters of the ZEP-520A process and adapted to the ZEP-530A by running dose, development time, and

development temperature sweeps. Then we adapted the process to a diluted ZEP-530A in Anisole by optimizing dose and development time to yield narrower nanowires. The process recipes are reported in previous sections.

To characterize the line-width roughness (LWR) we took high-resolution scanning electron micrographs of the fabricated structures after etching and resist removal. To minimize inconsistency due to stage drifts and vibration, we scanned a reduced central portion of the meander as shown in Fig.A-8(a). We then analyzed these SEMs using ProSEM by GeniSys. We used the software to calculate the LWR and the critical dimension of each nanowire in the meander (w^*), such as to establish a limited statistics (51 nanowire sections in this case). In Fig.A-8(b) and (c), we show the results for the w^* and LWR of the wires for two nominal widths, 50 nm and 60 nm. We also calculated the absolute average effective width ($\overline{w}^*$) and its distributions, and we compread it across the meander.

The results obtained for LWR are in agreement with other optimized electron-beam lithography processes for near-IR SNSPDs [187]. For each of the analyzed patterns, the $\overline{w}^*$ is at most 13% higher than the nominal width. The 50 nm meander has an $\overline{w}^* = 55.3$ nm with a LWR of 4.4 nm. The 60 nm meander has $\overline{w}^* = 62.8$ nm with $LWR = 4.9$ nm. Note that the averages are calculated over all segments. The distributions of the effective width versus the number of segments do not show any specific trend and thus demonstrate spatial uniformity across the meander. The LWR rarely exceeds 14% of the effective width, for each segment. In conclusion, these aggregated results show that our process can reliably yield large-area meanders with a nanowire width down to 55 nm and an average roughness below 5 nm.

A.6 Conclusion

In this Appendix, we reported a few processing recipes and methods for superconducting nanowire fabrication. We mainly focus on electron-beam lithography, a standing challenge in nanostructure fabrication. We hope this Appendix is a useful resource for students and researchers approaching the fabrication of nanowires.

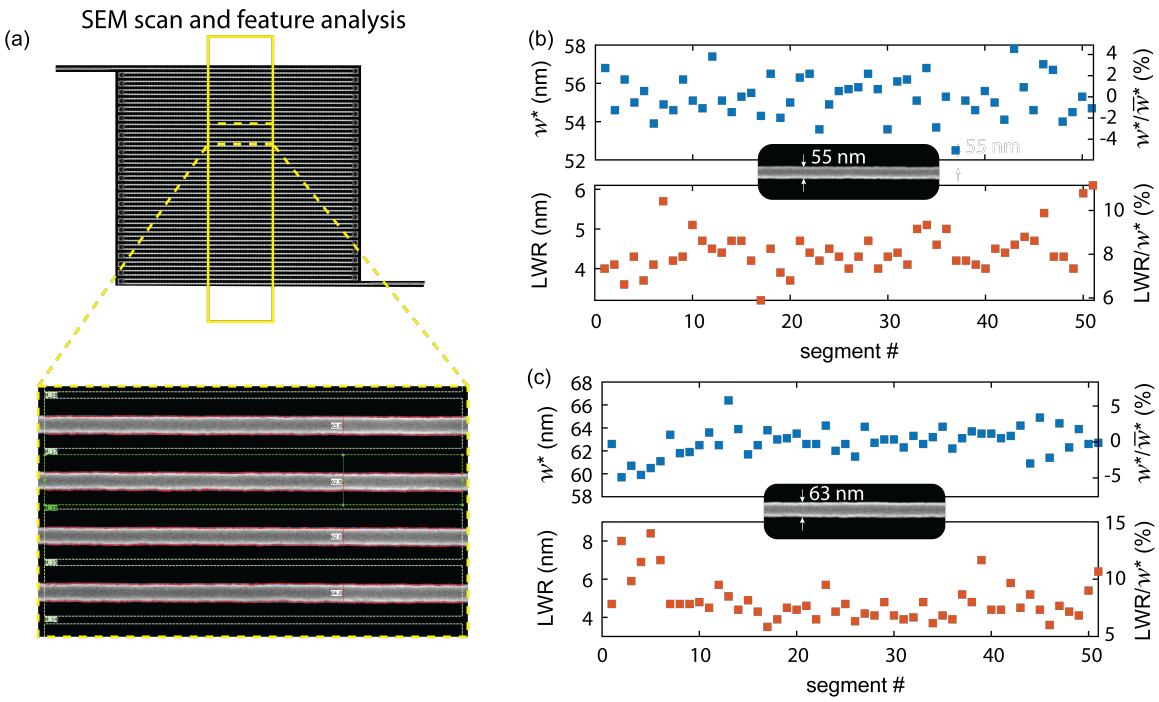

Figure A-8: Process metrology for ZEP-530A process. (a) SEM scans used for the analysis. (b) Average effective width and average line width roughness of 55 nm-wide nanowire meanders. (c) Average effective width and average line width roughness of 63 nm-wide nanowire meanders.

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