A Continuous-Time Pipeline ADC with Reduced Sensitivity to Clock Jitter

by

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B.Tech., Indian Institute of Technology, Delhi (2017)
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Abstract

With the advent of the fifth-generation (5G) standard for cellular networks, direct RF receivers are becoming popular in applications such as cellular base stations. Such systems require analog-to-digital converters (ADC) with a high dynamic range over a large digitization bandwidth (> 500 MHz). For high-speed high-resolution ADCs with an upfront sampler, the clock jitter poses a fundamental bottleneck for the maximum achievable signal-to-noise ratio (SNR). In applications requiring 10-12 bit resolution for 1 GHz digitization bandwidth, the clock jitter values must be no more than a few tens of femtoseconds. This poses significant design challenges for the clock generator.

The continuous-time (CT) pipeline ADC is an emerging architecture that combines the benefits of a discrete-time pipeline ADC and a continuous-time $\Delta\Sigma$ ADC architecture. In this thesis, we explore the clock jitter sensitivity of the CT pipeline ADC. We derive the SNR limitations in a CT pipeline ADC and propose a new CT pipeline ADC design with improved tolerance to clock jitter. We also present a design methodology for the delay line and propose a novel inductor-less delay line that provides a good amplitude and phase matching between the stage 1 signal path and the sub-ADC-DAC path from DC to 1.6 GHz to minimize the signal leakage in the first stage residue.

A prototype ADC was fabricated in 16nm Fin- FET process. The ADC achieves 61.7/60.8dB (low/high frequency) SNR over 1-GHz bandwidth. The active area is 0.77mm^2 and the ADC consumes 240mW. The Schreier figure- of-merit (FOMS) is 157.9dB which is amongst the best in comparison to other state-of-the-art continuous-time ADCs with digitization bandwidth greater than 500MHz.

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port that Hajime has provided for this research, but here is a gist. Hajime provided valuable feedback on CT pipeline ADC architecture at all critical decision-making moments throughout the project, he helped me with circuit design, simulations, layout, verification, and evaluation. There is no exaggeration in saying this, but without his help, this research work could not have been completed. Additionally, he helped in getting tapeout and evaluation support and always made sure that I got the help that I needed. I am very grateful to Hajime for his mentorship, and working with him made my Ph.D. so much more enjoyable!

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Chapter 1

Introduction

1.1 Motivation

An analog-to-digital converter (ADC) is a device that converts analog signal (continuous-time, continuous-amplitude) into digital signals (discrete-time, discrete-amplitude). Most real world signals are analog, such as the sound waves produced by a microphone, or the electromagnetic (EM) waves transmitted and received by cellphones. In modern electronic systems, most signal processing is performed in the digital domain, owing to the rapid advances in the integrated circuit (IC) technology. The transistor dimensions have shrunk by several orders of magnitude in the past three decades - from 3 μm process nodes in late 1980s to 5 nm process nodes in early 2020s.

The rapid miniaturization of the transistor has unlocked incredible computing power while minimizing the cost per transistor. The digital signal processing (DSP) has become increasingly area- and power-efficient over time. Owing to this, most of the computation on ICs has shifted to the digital domain. ADCs are an essential component of most electronic systems because they provide an interface between the real world analog signals and the digital domain on ICs (DSP and memory). In many systems, the analog and mixed-signal (AMS) components can consume a significant fraction of the overall system power. Therefore, to reduce the overall system power, the AMS circuits need to be designed for more power efficiency while maintaining a similar or higher computing capability and functionality.

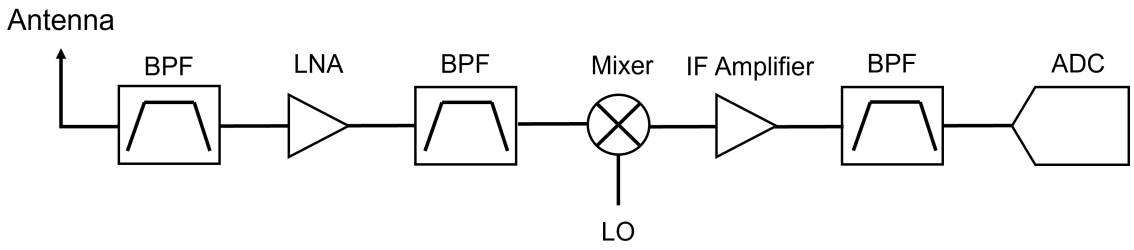


Figure 1-1: A heterodyne receiver.

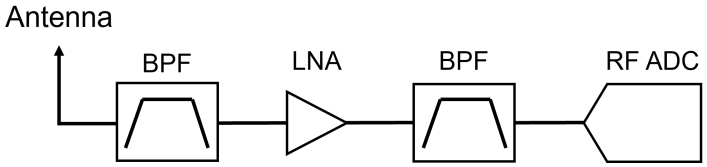


Figure 1-2: A direct RF sampling receiever.

One of the key applications for modern ICs is in the telecommunication sector. The market size of the telecommunication industry in 2021 was $1.7 trillion, and the projected revenue for 2028 is $2.46 trillion [15]. The communication standards have progressed greatly in the past four decades – analog voice in 1980s (1G), digital voice in 1990s (2G, 10-500 kbps), mobile broadband in 2000s (3G, 2 Mbps), high-speed internet and streaming in 2010s (4G, 20-50 Mbps) to the era of internet of things (IoT) with interconnected devices, sensors and systems in 2020s (5G, $>$ 500 Mbps). Heterodyne receivers are widely used in modern communication systems (Figure 1-1). However, advances in the data converter technology have enabled simplified receiver architectures using direct RF conversion (Figure 1-2). A direct RF sampler consists of a low-noise amplifier (LNA), a bandpass filter (BPF) and a wideband ADC. The receiver does not use mixers and local oscillators (LO), rather, the ADC digitizes the RF signal which is processed by the backend DSP. This simplifies the receiver design, resulting in a smaller form factor and reduced cost. Also, a single reciever can be used over multiple communication standards.

There are several different types of ADCs such as Flash ADCs, successive approximation ADCs, pipelined ADCs, and $\Delta\Sigma$ ADCs [16–24]. The choice of ADC type depends on the accuracy, speed, and resolution required for a particular application. The direct RF sampling receivers used in wired and wireless communication systems

for 5G network require about 1 GHz digitization bandwidth along with a large dynamic range. The discrete-time (DT) pipeline ADC and continuous-time (CT) $\Delta\Sigma$ ADC are popular choices for the above-mentioned application. The CT $\Delta\Sigma$ ADC can provide a high dynamic range due to oversampling and noise shaping. They also provide inherent anti-aliasing because of a continuous-time front end. However, since a high oversampling ratio (OSR[1]) is required in CT $\Delta\Sigma$ (usually > 8) which limits the ADC bandwidth [25–29]. DT pipeline ADCs can operate at Nyquist rate, i.e. the digitization bandwidth can be as high as half the sampling frequency. However, an anti-alias filter (AAF) must precede the ADC to prevent aliasing. For Nyquist rate operation, the anti-alias filter must have a sharp cut-off resulting in significant power overhead. Additionally, the input buffer preceding the DT pipeline ADC must drive a switched capacitor load. To charge and discharge the sampling capacitor, the input buffer must be able to supply a large current. In discrete-time front-end designs, the input buffer consumes a significant fraction of the total ADC power. For example, in [30], the input buffer consumes 55% of the total ADC power.

In addition to the above-mentioned practical design challenges, in upfront sampled ADCs, such as the DT pipeline ADC, the maximum achievable signal-to-noise ratio (SNR) is fundamentally limited by the clock jitter (Section 2.1.3). This bottleneck becomes apparent in high bandwidth applications such as wireline (the clock rates can be upwards of 112 Gb/s) and wireless (5G radios can operate around 30 GHz) transceivers. For example, with 100 fs RMS jitter, the SNR of an upfront sampled ADC is limited to 64 dB, 10.3 effective number of bits, for a 1-GHz single-tone input. To achieve a higher SNR, the clock jitter must be reduced to tens of femtoseconds. Reference [31] has derived the lower bounds on the power consumption of the clock generators to achieve tens of femtoseconds of clock jitter. For a 10-bit resolution 1-GHz bandwidth ADC, the tolerable jitter for a 3 dB and 1 dB SNR penalty due to clock jitter are 126 fs and 64 fs respectively[2]. Figure 1-3 shows that the VCO power consumption increases by 15x to reduce the jitter-related SNR penalty from

[1]OSR $= (f_S/2)/\text{BW}$ where f_S is the sampling rate of the ADC, and BW is the digitization bandwidth.

[2]Assuming that the SNR is limited by quantization noise.

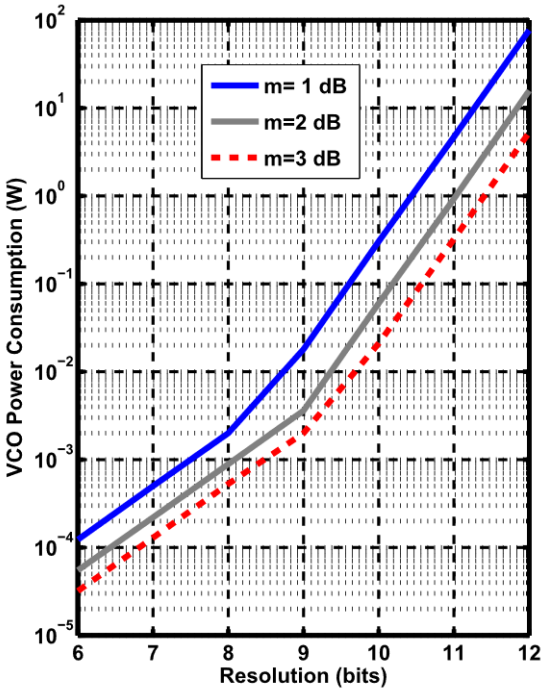


Figure 1-3: Estimated VCO power consumption v.s. the resolution for a 10-GS/s ADC comparing 1 dB, 2 dB and 3 dB jitter-induced SNR penalty. The SNR is assumed to be limited by the quantization noise [1].

3 dB to 1 dB. As the ADC resolution and bandwidth increase, the VCO power can become prohibitively large. To summarize, if the ADC necessitates a very low-jitter clock, then it leads to a challenging clock generator design, and can impact the overall system power consumption adversely. Therefore, it is essential to come up with ADC architectures that are less sensitive to clock jitter.

In this thesis, we explore the continuous-time (CT) pipeline ADC architecture with a focus on improving its clock jitter tolerance. Before delving into the details of the proposed ADC, we present an overview of the past work related to CT pipeline ADCs.

1.2 Literature Survey

1.2.1 A Pipeline ADC with Continuous-Time Input Stage

The first CT pipelined ADC was implemented by Gubbins *et al.* [2]. The key benefits that the authors presented in this work were: (1) a resistive front-end which eases the driving requirement for the external circuitry, (2) relaxed distortion requirements since the switched-capacitor sampler is moved to the second stage, and (3) inherent anti-aliasing. The overall ADC architecture is shown in Figure 1-4. Stage 1 is implemented in continuous time. There is no sample-and-hold upfront. Sampling occurs at the input of stage 2. All subsequent stages are switch-capacitor based, i.e., they are implemented in discrete time.

Figure 1-5 shows the basic operation of this ADC by presenting a contrast with the conventional DT pipeline ADC. In a DT pipeline ADC, stage 1 samples the input at the stage-1 clock (ϕ_1) falling edge (labeled as t_2 in Figure 1-5). The stage-1 sub-ADC digitizes the sampled input from time t_2 to t_3. The stage-1 sub-DAC output settles from t_3 to t_4. Then, stage 2 samples the residue at the stage-2 clock (ϕ_2) falling edge (labeled as t_4 in Figure 1-5). Since the stage-1 input is sampled and held, the stage-1 residue is given by:

$$V_{res,DT} = R_f \cdot (I_{in}(t_2) - I_{dac}(t_2)) \tag{1.1}$$

where R_f is the feedback resistor in the interstage amplifier. The residue magnitude is confined within ± 1-LSB because the subtraction occurs for the input sampled at time t_2, and the DAC output also corresponds to the input at time t_2. On the other hand, if stage 1 is implemented in continuous time, then the input current I_{in} can change between t_2 and t_4 when the stage-1 sub-ADC-DAC is processing the input $V_{in}(t_2)$. The residue in the case of a CT first stage is given by:

$$V_{res,CT} = R_f \cdot (I_{in}(t_4) - I_{dac}(t_2)) \tag{1.2}$$

The residue may no longer be confined within ± 1-LSB. In fact, if the input changes significantly from t_2 and t_4, then the amplified residue could potentially saturate the

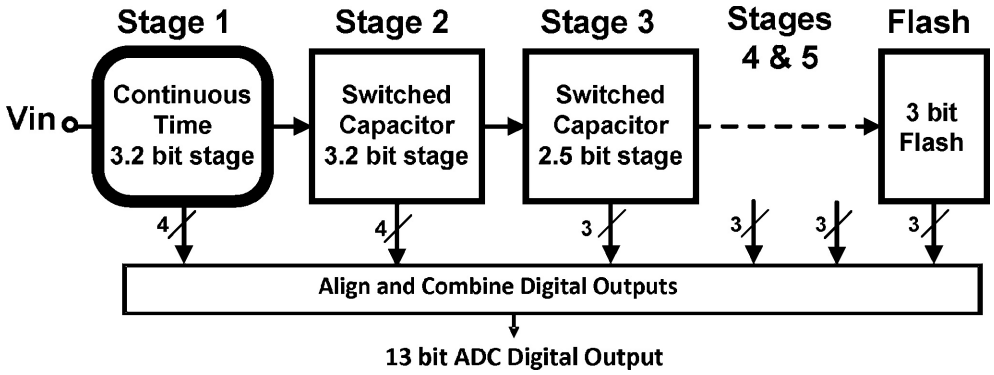


Figure 1-4: The CT pipeline ADC architecture as implemented in [2].

second stage thereby resulting in incorrect digital output.

To mitigate this problem, Gubbins *et al.* implemented a prediction filter [2]. The backend overloading [3] risk can be reduced if the sub-DAC output maps to the input at the time of subtraction. To achieve this, the authors placed a prediction filter before the stage-1 sub-ADC to estimate $V_{in}(t_4)$. While this reduces the timing error caused in the residue by the delay in the sub-ADC-DAC path, there are several limitations to this approach. First, the prediction filter has a positive group delay across the ADC bandwidth. This limits the usable bandwidth – to maintain causality, the filter's phase response must go down at higher frequencies. Second, the prediction filter accuracy is important to achieve a good cancellation for the residue. The cancellation is only as good as the estimate of the input by the prediction filter $V_{in}(t_4)$. Also, this can limit the stage 1 resolution since a higher-order prediction filter will be required for better stage 1 resolution. For instance, in the ADC presented in [2], a fourth-order filter is needed to accurately predict the input signal for 80% of the Nyquist rate (50 MSPS gives 20 MHz input bandwidth). Lastly, even with the prediction filter, the interstage gain was limited to just 1.3 (the typical gain with a 3-bit sub-ADC-DAC in a DT pipeline ADC is $2^{3-1} = 4$). A smaller gain is not desirable because it results in less noise suppression from the backend stages.

Despite the above-mentioned shortcomings, the work by Gubbins *et al.* success-

[3] In pipelined ADCs, each stage residue is processed by the following ADC stage. If the residue amplitude exceeds the full-scale of the next stage, then this condition is called overloading. It is sometimes referred to as *backend overloading* if this happens in the last stage of a pipelined ADC.

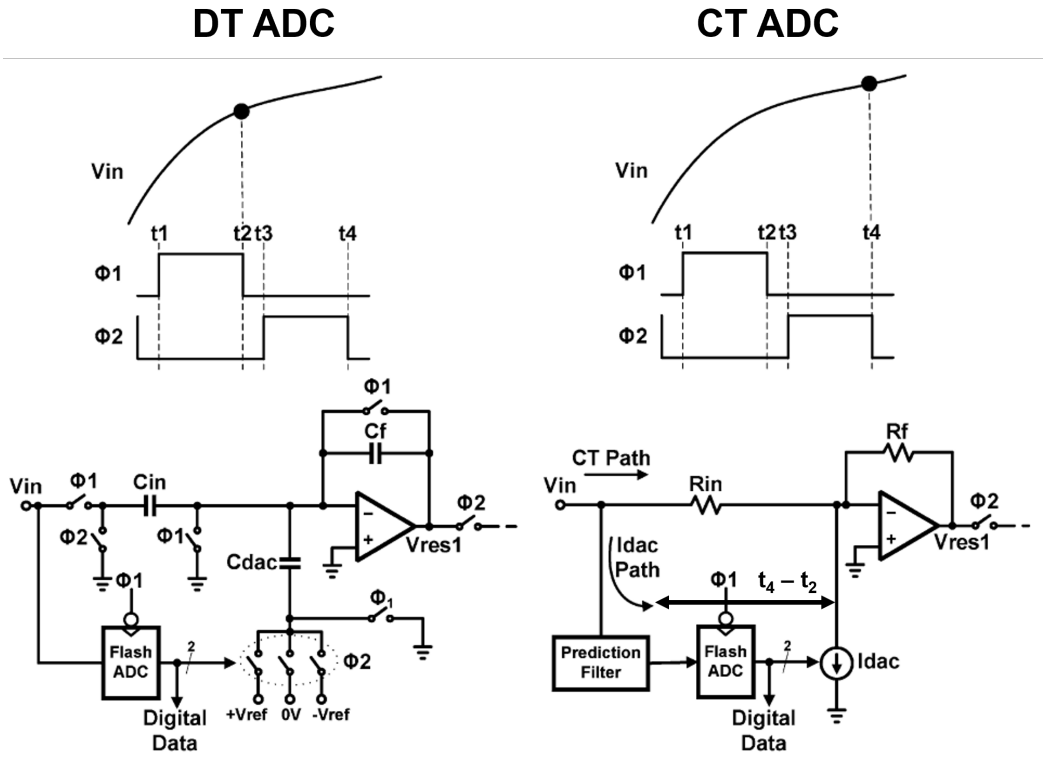


Figure 1-5: A simplified diagram showing the stage-1 operation for the DT and CT pipeline ADC [2].

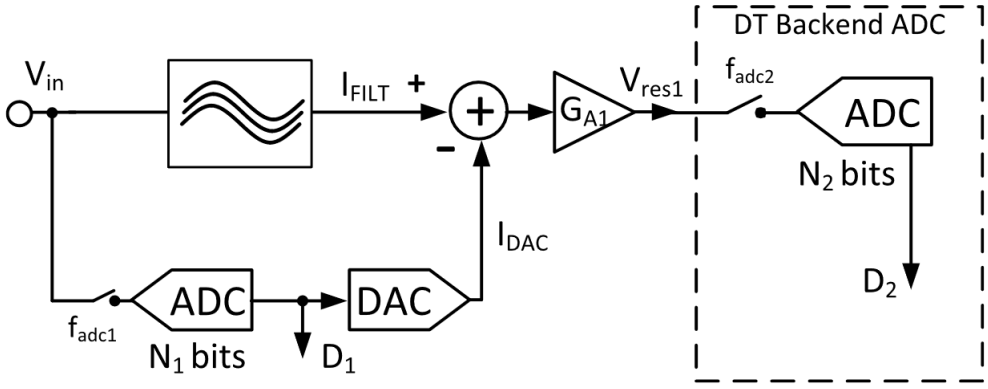


Figure 1-6: A pipelined ADC with a continuous-time first stage having an analog delay and filter in the signal path [3].

fully implemented the first CT pipeline ADC.

1.2.2 Bandwidth Extension in CT Input Pipeline ADC

O'Hare *et al.* presents an analysis of the signal bandwidth in a continuous-time pipeline ADC [3]. A continuous-time stage-1 leads to a timing mismatch between the signal path and the sub-ADC-DAC path. This increases the residue signal and can potentially saturate the backend ADC. The authors propose incorporating a positive delay in the signal path to match the sub-ADC-DAC path delay as shown in Figure 1-6. A simple way to achieve this could be by using an RC low-pass filter. However, that would create a magnitude mismatch as well as present a phase-mismatch problem because the phase will saturate to 90° for a single-pole delay filter in the signal path, limiting the usable bandwidth for the ADC. Therefore, the authors propose an all-pass RC-lattice-based delay filter as shown in Figure 1-7. The delay transfer function is given by:

$$H_{DLY}(s) = \frac{V_{OUT}}{V_{IN}} = \frac{1 - j\omega C_{\text{FILT}} R_1}{1 + j\omega C_{\text{FILT}} R_1} \tag{1.3}$$

where C_{FILT} and R_1 are the capacitor and resistor values in the RC lattice. Such a delay line achieves a flat magnitude response and a phase that is relatively linear in-band and saturates to 180° at high frequencies $\left(\phi = 2\tan^{-}1(\omega C_{\text{FILT}} R_1)\right)$.

To validate the increase in ADC bandwidth, the authors present simulation results comparing the SNDR for the case of no filter, low-pass filter, and all-pass filter as

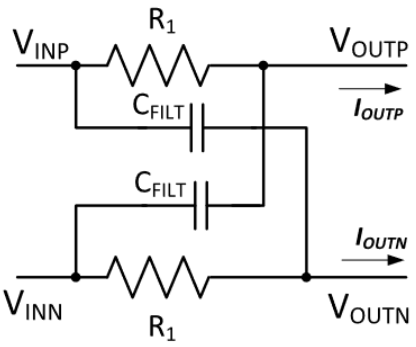


Figure 1-7: An all-pass filter delay line using RC-lattice [3].

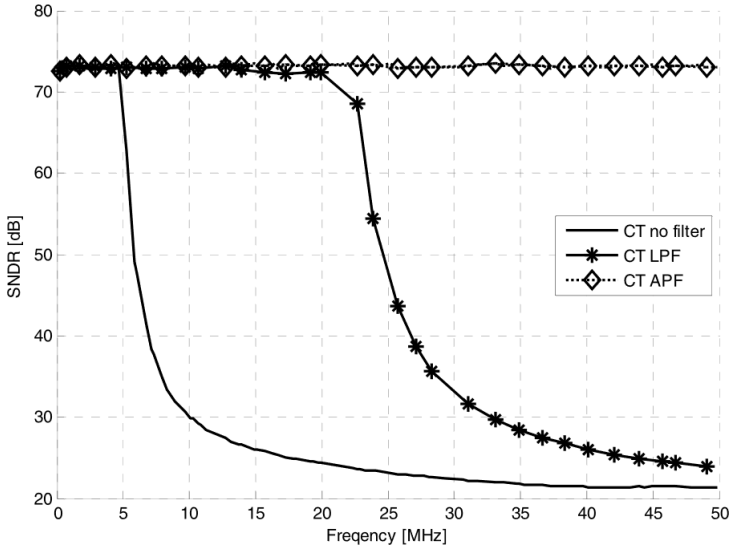


Figure 1-8: A continuous-time input pipeline ADC showing the signal bandwidth comparison for different filters in the signal path. The phase response of the low-pass filter and the all-pass filter was optimized for maximum bandwidth [3].

shown in Figure 1-8. Although no silicon results have been presented, this work proposed the idea of using a positive delay in the signal path of a CT pipeline ADC. As will be shown in the following subsections of this Chapter, and later in Chapter 3, several other CT pipeline ADCs [4–7,9,32], including the proposed CT pipeline ADC in this thesis have used this technique in silicon implementations to improve the ADC bandwidth.

1.2.3 A Multi-Stage Continuous-Time Pipeline ADC

Shibata *et al.* implemented a 7-stage CT pipeline ADC as shown in Figure 1-9 [4]. All stages are implemented in continuous time. Instead of using a prediction filter (as used in [33]), the authors have implemented a positive delay in the signal path as shown in Figure 1-10. The delay line is designed to match the signal path delay with the sub-ADC-DAC path delay. This is accomplished by matching the phase response of the delay line to the sub-ADC-DAC path within the ADC bandwidth. The residue has a sawtooth-like waveform in the time domain as shown in Figure 1-10. If the signal path delay is perfectly matched to the sub-ADC-DAC path delay, then the signal leakage in the stage-1 residue is minimized [4]. For a sinusoidal input to the ADC, in presence of delay mismatch, the sawtooth residue waveform rides on a sinusoidal signal. The magnitude of the sinusoidal carrier depends on the extent of the signal leakage.

In the frequency domain, the sawtooth shape of the residue corresponds to the sub-DAC tones near multiples of the sampling frequency f_s as shown in Figure 1-11 ($f_S \pm f_{IN}$, $2f_S \pm f_{IN}$ and so on). To suppress the DAC images in the frequency domain, or equivalently, to smoothen the amplified residue in the time domain, the stage-1 residue is low-pass filtered in the interstage amplifier. For the back-end digitization of the amplified residue, the authors have used multiple continuous-time stages (2-7). The final ADC output is obtained by performing digital reconstruction on the data from all the stages of the pipeline. Unlike a DT pipeline ADC, a simple shift-and-add cannot be used because of the fully-continuous-time operation of the ADC. Instead,

[4]Signal leakage in the stage 1 residue is defined as $V_{IN} \cdot (G_{DLY}(s) - F(s)D(s))$ where $G_{DLY}(s)$, $F(s)$ and $D(s)$ are the delay line, sub-ADC and sub-DAC transfer function.

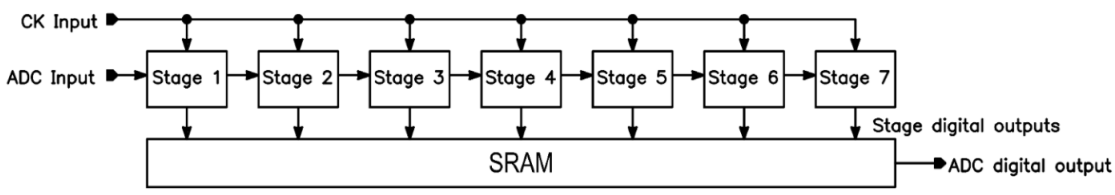


Figure 1-9: The 7-stage CT pipeline ADC implemented in [4].

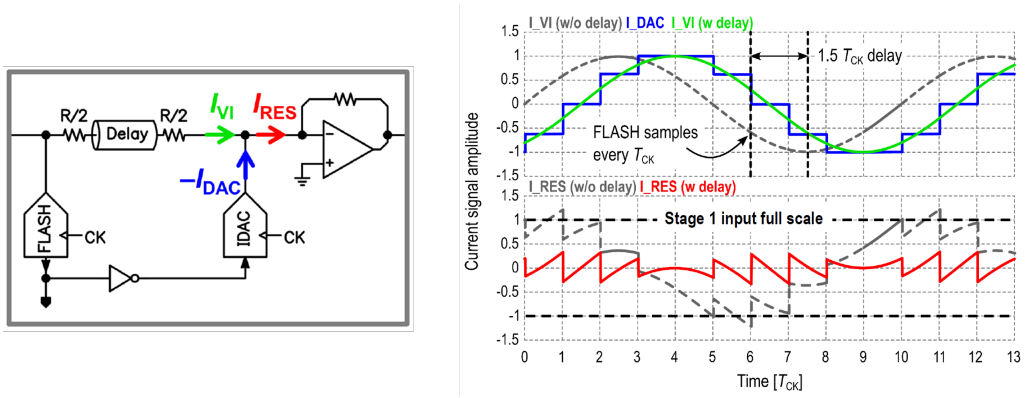


Figure 1-10: A schematic of the CT stage-1 implemented in [4] showing the positive delay in the signal path. The relevant time-domain waveforms are shown on the right.

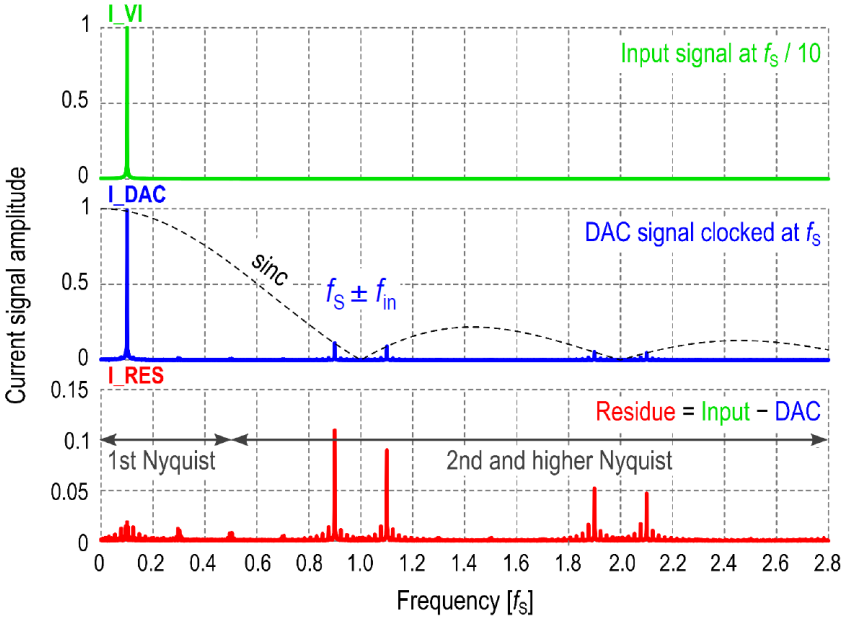


Figure 1-11: Spectrum for the stage 1 signals: delay input current, sub-DAC output current, and the residue current [4]. The sawtooth-like residue waveform results in DAC images at multiples of f_S which show up in the stage 1 residue.

several digital filters are used to perform the back-end recombination to get the final ADC output.

The authors have implemented the signal path delay with cascaded LC-lattice (stage 1) and single RC-lattice structures (stage 2-7) as shown in Figure 1-12 [4]. The cascaded LC-lattice has a better phase matching to the sub-ADC-DAC phase response in comparison to the RC-lattice. Since the first stage of a pipelined ADC

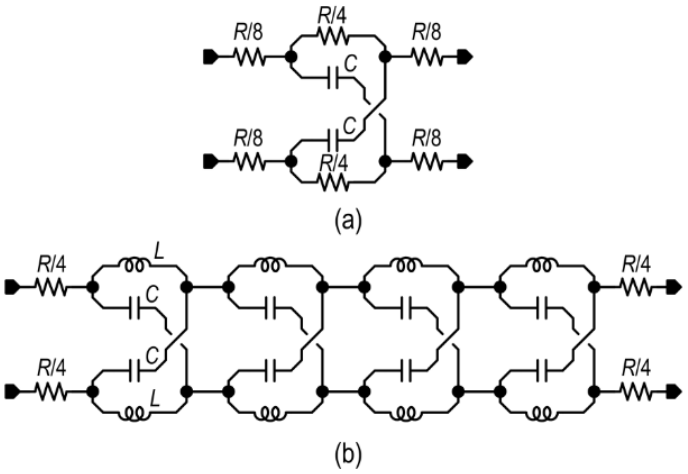


Figure 1-12: The schematic for the delay line using (a) RC lattice and (b) cascaded LC lattice, as implemented in [4].

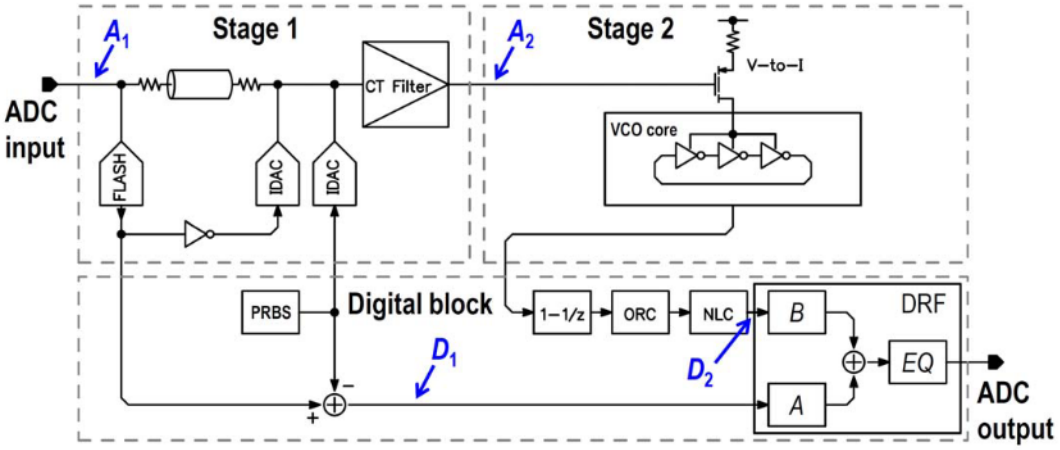


Figure 1-13: The block diagram for a 2-stage CT pipeline ADC. The front-end is a continuous-time stage while the back-end uses a VCO-based ADC to digitize the stage-1 residue [5].

is most critical and necessitates a higher interstage gain, a cascaded LC-lattice delay line has been used to minimize the signal leakage. However, the cascaded LC-lattice line occupies a large area. Therefore, to save area, the authors have used a single RC-lattice-based delay line in stages 2-7 where the signal leakage is not a major concern.

While this ADC achieves exceptional performance: 1125 MHz BW, -156 dBFS/Hz noise spectral density (NSD), 73 dB SFDR, 68 dB inherent anti-aliasing, and a Schrier

figure-of-merit (FoM_S) of 159 dB, which is comparable to other state-of-the-art DT pipeline ADCs [30,34,35] and CT $\Delta\Sigma$ ADCs [28,36], the ADC occupies 5.1 mm^2 area and consumes 2330 mW power (excluding digital signal processing power and area). The primary reason for the large area and power consumption is that all 7-stages use continuous-time architecture. Not only does the ADC core consume more power, but also the associated DSP required to reconstruct the digital output is complex and power-hungry.

To address the area and power concerns of [4], Shibata *et al.* have implemented a voltage-controlled oscillator (VCO)-based CT pipeline ADC [5]. The first stage is a continuous-time stage and the back-end is a VCO-based ADC as shown in Figure 1-13. This greatly reduces the complexity and power consumption of the overall ADC. This ADC has a bandwidth of 800 MHz and achieves -148dBFS/Hz NSD, 73 dB SFDR and 41 dB inherent anti-aliasing while occupying 0.34 mm^2 area (15x smaller than [4]) and consuming only 280 mW power (8x less than [4]). This work successfully demonstrated that it is possible to retain the CT front-end benefits such as relaxed input buffer requirements and inherent anti-aliasing while using a relatively simple back-end ADC to reduce the hardware complexity, area, and power.

1.2.4 Stage-1 Innovations in CT Pipeline ADCs

In this subsection, we present some of the previous works which have done innovations in stage 1 of CT pipeline ADCs to improve certain performance aspects of the overall CT pipeline ADC.

Manivannan *et al.* have presented an analysis of a multi-stage CT pipeline ADC and propose using non-identical stages [6]. If identical interstage amplifiers are used throughout the pipeline (for example, Butterworth filters), then the overall signal transfer function has a droop because of cascading multiple stages. Assuming that the quantization spectral density is relatively white, the SNR of the converter will degrade because of the signal transfer function droop. To achieve a flat SNR in the entire bandwidth, some digital equalization will be required, increasing the system complexity and power consumption. The authors propose designing the individual

pipeline stages such that the overall transfer function has a Butterworth response, rather than individual stages having a Butterworth response, as shown in Figure 1-14.

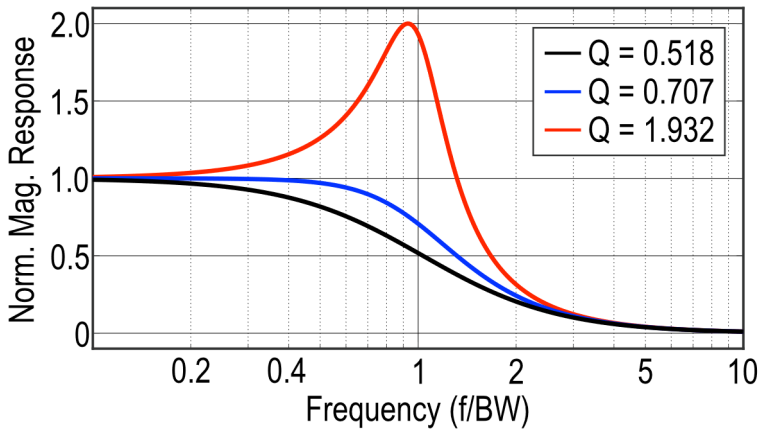


Figure 1-14: Magnitude response for individual interstage amplifiers in a 3-stage CT pipeline ADC. Cascading these filters can achieve an overall Butterworth response [6].

Basvaraj *et al.* have presented a technique to estimate the signal transfer function (same as the anti-alias transfer function) in a CT pipeline ADC [7]. Instead of characterizing the signal transfer function by exciting the ADC with multiple sinusoidal signals, they demonstrate a method that only uses a single tone to characterize the signal transfer function. A conceptual block diagram is shown in Figure 1-15. A 3-stage CT pipeline ADC is considered in this work, where stages 1 and 2 are continuous-time stages, and stage 3 is a standalone time-interleaved SAR-ADC. The digital sequences from stages 1-3 are represented by $v_1[n]$, $v_2[n]$, and $v_3[n]$ respectively. The impulse response for the stage 1 and 2 digital filters are denoted by $h_1[n]$ and $h_2[n]$. The filter coefficients are computed by minimizing the in-band noise after (digitally) removing the signal and the DC bins. The ADC output is given by:

$$v[n] = v_1[n] * h_1[n] + v_2[n] * h_2[n] + v_3[n] \tag{1.4}$$

The signal transfer function can be approximated by taking the Z-transform of $h_1[n]$. Due to the DAC sinc response, there will be some inaccuracy near $f_S/2$, but a sinc-correction can be applied to get a more accurate estimate of the signal transfer function. A single-tone-based characterization of the signal transfer function can be useful

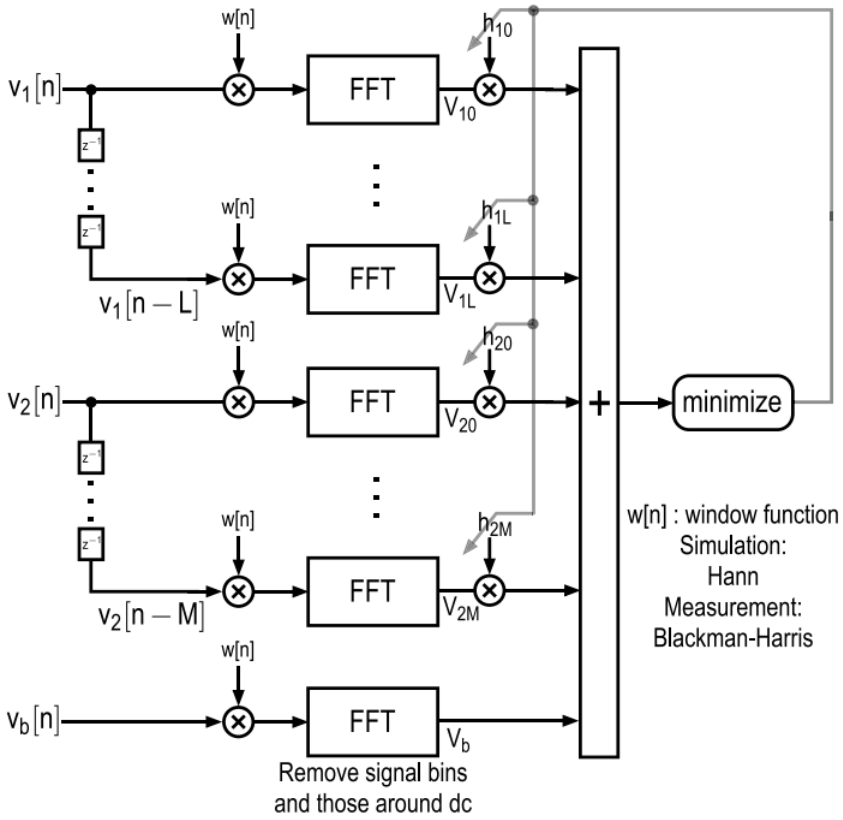


Figure 1-15: A schematic of the digital reconstruction filter showing the computation of the filter coefficients using a single-tone excitation. The Z-transform of $h_1[n]$ is used to estimate the signal transfer function [7].

for mass testing during product development.

Ungethüm *et al.* have analyzed and optimized the all-pass delay line to minimize the signal leakage component in the residue in simulation [8]. The authors have simulated the signal leakage for a first-order all-pass delay line (with and without an additional low-pass filter to match the sinc response of the sub-DAC) as shown in Figure 1-16. While the optimal delay value to time-align the signal path and sub-ADC-DAC path is $1.5T_S$ [5], the authors show that for OSR < 8, designing the delay line for $T_d = 1.5T_S$ is sub-optimal (see Figure 1-17). The best delay value can be found by optimizing the stage-1 transfer function, and it turns out that for a first-order all-

[5]The sub-ADC output comes after 1 clock cycle, resulting in a delay of T_{CK}. For a non-return-to-zero shaped DAC pulse, the sub-DAC delay is $T_{CK}/2$, resulting in the overall sub-ADC-DAC path delay to be $1.5T_{CK}$.

pass delay line, $T_d = 1.65T_S$ is the optimal value for the delay in the signal path which minimizes the signal leakage across the entire ADC bandwidth. Instead of minimizing the leakage at bandedge ($T_d = 1.702T_S$), a local minima can be created in the stage transfer function resulting in the most optimal signal leakage ($T_d = 1.65T_S$) [6]. For OSR = 4 operation of the CT pipeline, the maximum signal leakage with $T_d = 1.5T_S$ is -19.7 dBFS (interstage gain $\leq$ 10), whereas with $T_d = 1.65T_S$ is -28.4 dBFS. A reduction in the signal leakage by 8.7 dB equates to about a factor of 2.7 increase in the interstage gain (only considering the signal leakage component in the stage-1 residue).

Taking this a step further, Ismail *et al.* have presented a general design methodology to further reduce the signal leakage, opening up the possibility of near-Nyquist operation of a CT pipeline ADC [9]. The authors propose using an n$^{\text{th}}$-order delay line given by:

$$G_{DLY}(s) = \frac{b_0 + b_1 s + b_2 s^2 + ... + b_n s^n}{a_0 + a_1 s + a_2 s^2 + ... + a_n s^n} \tag{1.5}$$

[6]The most optimal signal leakage happens when the signal transfer function does not exceed a set threshold value (usually governed by the full-scale of the following stage) over the entire digitization bandwidth.

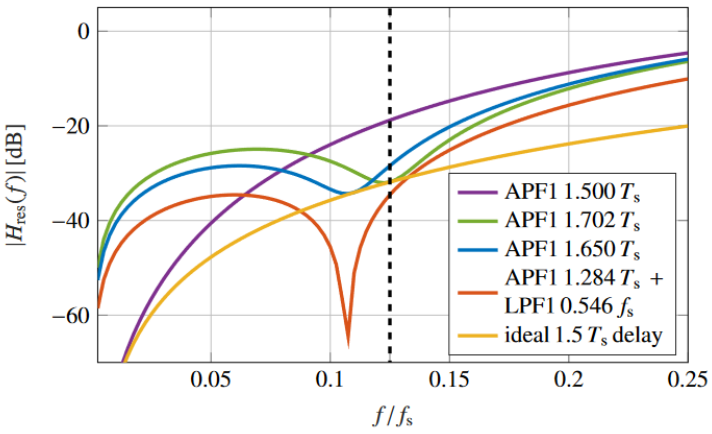


Figure 1-16: Simulated transfer function for the stage-1 residue in a CT pipeline ADC for various combinations of all-pass and low-pass response [8]. The blue curve ($T_d = 1.65T_S$) shows the most optimal signal leakage for an all-pass response delay line. Adding an additional LPF in the signal path is usually beneficial to reduce the signal leakage because it results in a better magnitude matching with the sub-DAC sinc response.

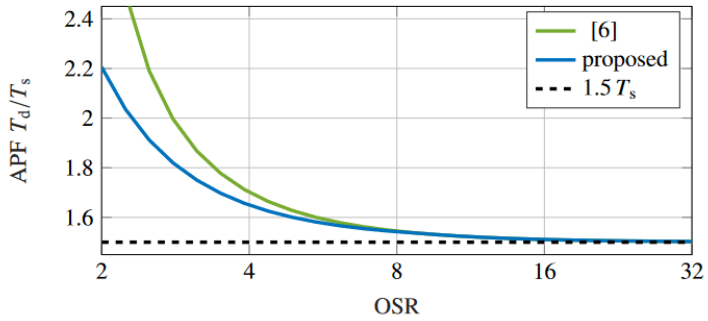


Figure 1-17: Simulation results showing the optimal delay for an all-pass delay line vs. OSR [8]. For lower OSR, there is significant signal leakage which can be minimized with an optimal design for the delay line.

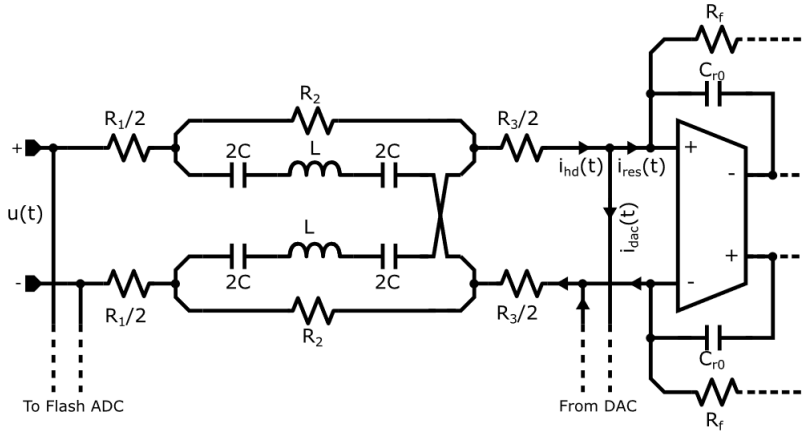
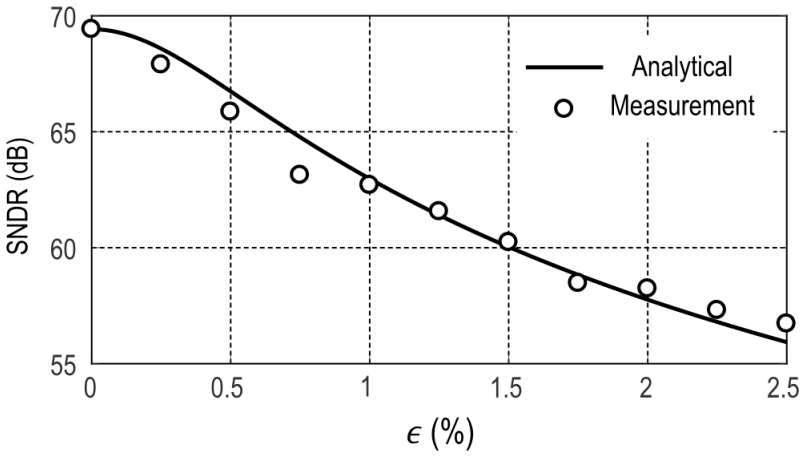


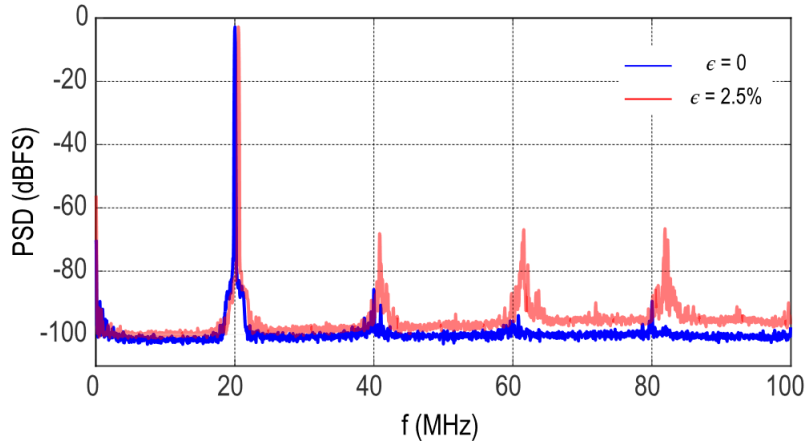
Figure 1-18: A CT pipeline stage 1 showing a 2nd-order RLC lattice-based delay line optimized for near nyquist operation [9].

where the coefficients $a_0...a_n$ and $b_0...b_n$ must to optimized to minimize the signal leakage across the ADC bandwidth. Such a structure can be implemented by using a combination of series resistors and L-C cross-connected lattices. The delay line implemented in [9] is shown in Figure 1-18.

From the works of Ungethüm *et al.* [8] and Ismail *et al.* [9], it is clear that the accuracy of the delay line is very important to minimize the signal leakage in the residue, and ultimately realize a high interstage gain. Pavan *et al.* have looked at the problem of RC variation and its impact on the ADC performance [10]. A 2.5% variation in the RC value results in roughly 12-13 dB SNDR degradation as shown in Figure 1-19. The reason for this performance degradation is the backend



(a) SNDR vs. percentage RC variation.



(b) Measured spectrum with and without RC mismatch.

Figure 1-19: Impact of *small* RC-variations on the performance of a CT pipeline ADC [10].

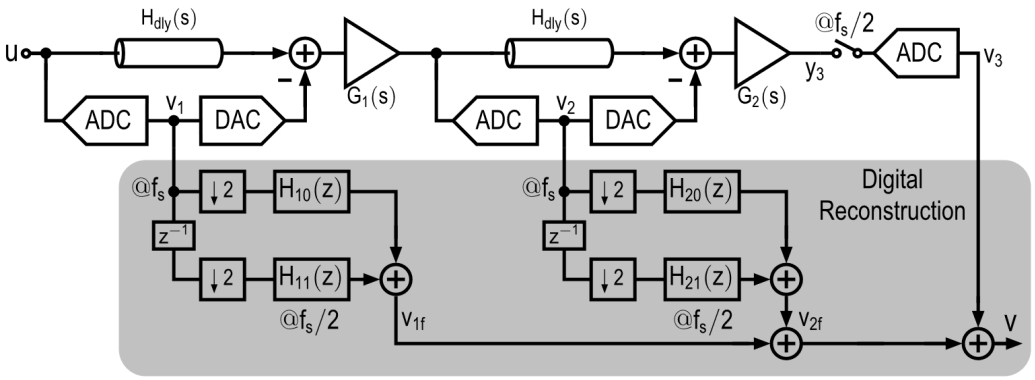
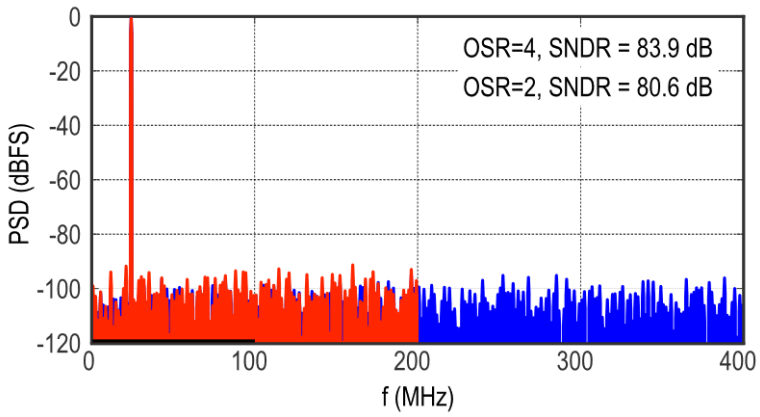


Figure 1-20: Schematic of a 3-stage CT pipeline ADC showing the decimation property in the digital reconstruction [6].

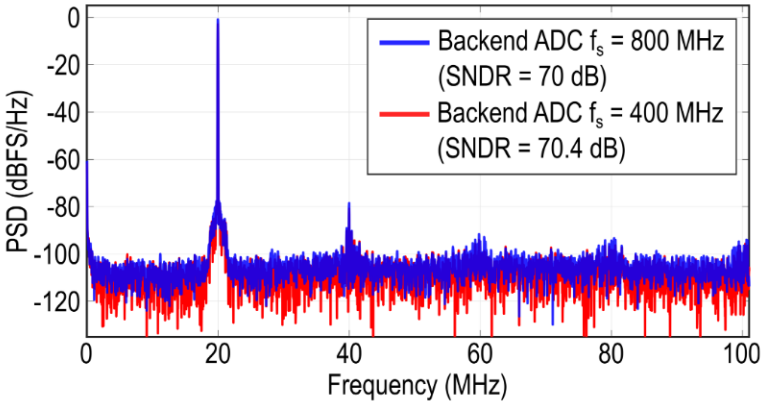
saturation. To emulate the impact of RC variations, the authors varied the clock frequency instead, keeping all other parameters the same. A 2.5% mismatch case was realized by using $f_S = 780$ MHz instead of the nominal $f_S = 800$ MHz.

1.2.5 Implicit Decimation Property in CT Pipeline ADCs

Manivannan *et al.* have presented the implicit decimation property in CT pipeline ADCs [6]. A schematic for the pipeline stages, including the digital reconstruction with decimation is shown in Figure 1-20. Instead of processing the pipeline stages outputs at full rate (f_S), they are decimated by a factor of 2. For a sharp roll-off in the interstage amplifier, the aliased interferer and noise will be negligible and will not have a significant impact on the SNR of the ADC. Figure 1-21a shows about 3 dB degradation in the SNR (from 83.9 dB to 80.6 dB) for the case where the CT pipeline ADC has OSR = 4 (the backend ADC operates at $f_S/2$). In a practical design, if the noise floor is limited by quantization noise, thermal noise, or jitter noise, then the decimation in the digital reconstruction does not become a bottleneck for the overall SNR of the ADC. Figure 1-21b shows the measured results for the same scenario demonstrating that the backend can operate at a lower rate without causing any noticeable SNR degradation.



(a) Simulated spectrum.



(b) Measured spectrum.

Figure 1-21: Simulated and measured spectrum for the 3-stage CT pipeline ADC with the backend ADC operating at f_S and $f_S/2$ [6]. There is no degradation in the measured SNR because of the decimation in the digital reconstruction.

1.3 Research Goals and Contribution

The goal of this thesis is to explore the CT pipeline ADC with a focus on its jitter sensitivity. We present a detailed analysis of the impact of clock jitter on the CT pipeline ADC performance. Specifically, we look at the impact of the sub-ADC clock jitter, the backend ADC clock jitter, and the sub-DAC clock jitter. We also compare the jitter sensitivity of a CT pipeline ADC with conventional upfront sampled ADCs. The stage 1 sub-DAC is the most jitter sensitive sub-block in the system, and can potentially limit the SNR if the noise floor is limited by the jitter noise. In this work, we propose a new CT pipeline ADC which achieves a reduced sensitivity to clock

jitter.

The first innovation is the time-interleaved sub-ADC-DAC path in stage 1 of CT pipeline ADC. The idea is to increase the effective sampling rate in the sub-ADC-DAC path to achieve a higher effective OSR. This reduces the in-band jitter-induced noise at the DAC output and improves the maximum achievable SNR for the CT pipeline ADC by a factor of $10\log_{10}(\text{OSR})$. In the prototype ADC, we implement 2-way time-interleaving in the sub-ADC-DAC path as a proof-of-concept, and the ADC achieves 3 dB better suppression in the jitter-induced noise. Although, a higher interleaving factor can increase the jitter tolerance.

The second innovation is the new delay line design in stage 1 of CT pipeline ADC which is critical to the performance of CT pipeline ADCs. As described in section 1.2, the previous works have implemented an LC-lattice-based delay line to achieve a good phase matching between the signal path and the sub-ADC-DAC path. However, using inductors is not desirable because they occupy a large area to achieve a similar delay. Also, since the inductors are used in the signal path, any coupling with close-by circuitry is detrimental to the ADC performance. RC lattice-based delay lines have also been implemented, but they do not provide good phase matching over a larger bandwidth. Hence, they are only useful for applications with OSR ≥ 4. In this work, we propose a new 4x-cascaded RC lattice-based delay line that achieves a good phase matching between the signal path and the sub-ADC-DAC path up to OSR = 2.5. This plays a crucial role in extending the bandwidth of CT pipeline ADCs.

The proposed ADC has been implemented in a 16 nm FinFET technology node. The ADC operates at 6.4 GS/s and achieves 61.7 dB SNR, 9.8 effective number of bits (ENOB) across 1000 MHz bandwidth. The ADC occupies 0.77 mm^2 active area and consumes 240 mW. The Schrier figure-of-merit (FoM_S[7]) for the prototype ADC is 157.9 dB, which is amongst the best in comprison to other continuous-time state-of-the-art ADCs achieving 500+ MHz bandwidth.

[7] $\text{FoM}_S = \text{SNDR} + 10\log_{10}(\text{BW/P})$

1.4 Thesis Organization

The remainder of the thesis is organized as follows:

Chapter 2 presents a detailed background of the pipelined A/D conversion. We first describe the more conventional discrete-time (DT) pipeline ADC architecture. Then, we present the continuous-time (CT) pipeline ADC, which is an emerging A/D architecture and a variation of the conventional DT pipeline ADC. The CT pipeline ADC leverages the benefits of a continuous-time front-end while maintaining the benefits of a pipelined converter. The system architecture has been presented followed by the key design considerations. Finally, we conclude this chapter by presenting a detailed analysis of the impact of clock jitter in CT pipeline ADCs.

In Chapter 3, we present the details of the prototype ADC. First, the system architecture, focusing on the time-interleaved sub-ADC-DAC path has been discussed. Next, the design methodology for the delay line has been presented, followed by the details of the proposed 4x-cascaded RC lattice based delay line. Finally, we give an overview of the circuit and layout implementation of various sub-blocks used in the prototype ADC.

In Chapter 4, we describe the experimental setup and the measurement results. The key performance specifications of the prototype ADC have been compared with previously published CT pipeline ADCs, as well as with other ADC architectures achieving similar bandwidth and resolution.

Finally, in Chapter 5, conclusion and future research directions are discussed.

Chapter 2

Pipelined Analog-to-Digital Conversion

The idea of a pipelined ADC architecture was first conceived back in the 1950s [37]. Smith *et al.* proposed that multiple ADC stages can be cascaded to get parallel digital output. Since its conception, numerous pipelined ADCs have been implemented with a competitive SNR and figure-of-merit (FoM) [38]. A pipelined ADC architecture is advantageous for high bandwidth applications due to the parallel data processing in the cascaded stages. Also, the overall ADC resolution can be increased by cascading more stages (although this may come at the cost of increased area, power, and hardware complexity). The most popular implementation of a pipelined ADC is a discrete-time (DT) pipelined ADC. In this ADC, the analog input is sampled upfront, and the discrete-time analog data is digitized in the various pipeline stages, and finally recombined to get the digital output. In the past few years, continuous-time (CT) pipelined ADC architecture has emerged. This implementation retains the benefits of a pipeline structure while leveraging the benefits of a continuous-time front end, such as low driving current and inherent anti-aliasing. The DT pipeline and the CT pipeline architectures have been explained in detail in the remainder of this chapter.

2.1 Discrete-Time Pipeline ADC

2.1.1 System Architecture

The schematic of a conventional DT pipeline ADC is shown in Fig. 2-1. The analog input is processed in sequential stages: $\mathrm{STG_1}$, $\mathrm{STG_2}$ ... $\mathrm{STG_N}$. Each stage is comprised of a sub-ADC, sub-DAC and an interstage amplifier. The sub-ADC digitizes the input to give an m-bit digital code $V_{\mathrm{ADC_1}}[n] = V_{in}[n] + Q_1[n]$, where $V_{in}[n]$ is the $\mathrm{n^{th}}$ sample of the analog input and $Q_1[n]$ is the first stage quantization error for the $\mathrm{n^{th}}$ sample. The sub-DAC converts the digital bits to an analog voltage (or current) for subtraction from the sampled input to give the stage residue:

$$\begin{aligned} V_{\mathrm{RES_1}} &= V_{in}[n] - V_{\mathrm{DAC_1}} \\ &= V_{in}[n] - V_{\mathrm{ADC_1}} - Q_1[n] - E_{\mathrm{DAC_1}} \end{aligned} \tag{2.1}$$

where $E_{\mathrm{DAC_1}}$ is the stage-1 DAC error. For simplicity, if we assume an ideal sub-DAC, then $E_{\mathrm{DAC_1}} = 0$ and $V_{\mathrm{RES_1}} = -Q_1[n]$. Since the stage-1 residue is equal to the stage-1 quantization error, it has a small magnitude, less than 1/2 LSB ($= V_{\mathrm{FS}}/2^M$). The quantization error is amplified by a factor of 2^{M-1} to match the full-scale of the

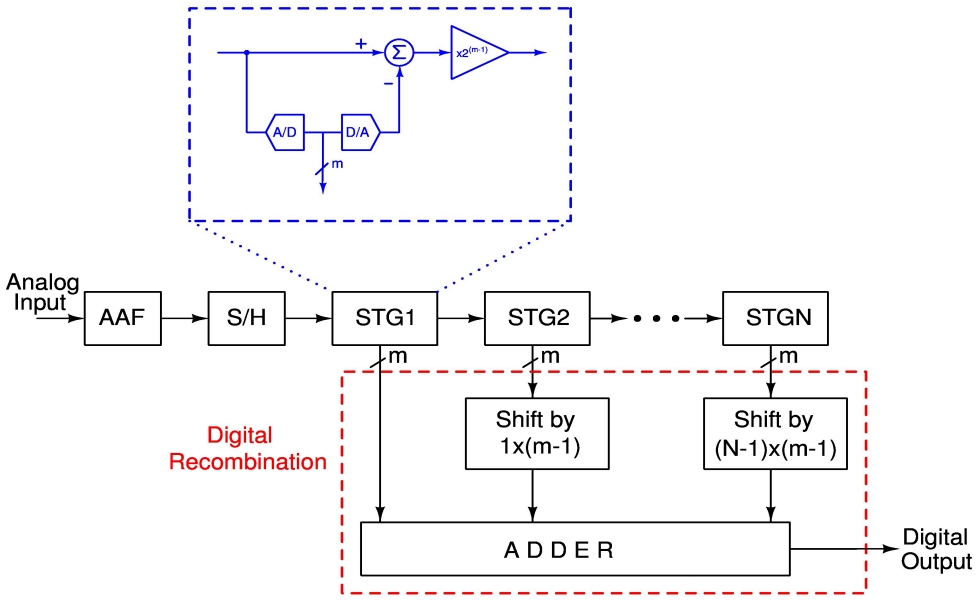


Figure 2-1: Block diagram of a conventional discrete-time pipeline ADC.

stage-2 ADC (see Section 2.1.2). The following sub-ADC outputs are obtained when the n$^{\text{th}}$ sample passes through the pipeline:

$$\begin{aligned} V_{\text{ADC}_1} &= V_{in}[n] && + Q_1[n] \\ V_{\text{ADC}_2} &= -Q_1[n] \cdot 2^{M-1} && + Q_2[n] \\ V_{\text{ADC}_3} &= -Q_2[n] \cdot 2^{M-1} && + Q_3[n] \\ &\vdots \\ V_{\text{ADC}_N} &= -Q_{N-1}[n] \cdot 2^{M-1} && + Q_N[n] \end{aligned} \tag{2.2}$$

where M is the sub-ADC resolution and $Q_i[n]$ is the quantization error in the i$^{\text{th}}$ stage for the n$^{\text{th}}$ sample ($i = 1, \ldots, N$). The sub-ADC outputs are added in a way that all intermediate quantization errors are canceled:

$$D_{OUT} = V_{\text{ADC}_1} + \frac{V_{\text{ADC}_2}}{2^{M-1}} + \frac{V_{\text{ADC}_3}}{2^{(M-1)\cdot 2}} + \ldots + \frac{V_{\text{ADC}_N}}{2^{(M-1)\cdot(N-1)}} \tag{2.3}$$

$$\begin{aligned} &= V_{in}[n] + Q_1[n] \\ &\quad + \frac{1}{2^{M-1}} \cdot \left(-Q_1[n] \cdot 2^{M-1} + Q_2[n] \right) \\ &\quad + \frac{1}{2^{(M-1)\cdot 2}} \cdot \left(-Q_2[n] \cdot 2^{M-1} + Q_3[n] \right) + \\ &\quad \vdots \\ &\quad + \frac{1}{2^{(M-1)\cdot(N-1)}} \cdot \left(-Q_{N-1}[n] \cdot 2^{M-1} + Q_N[n] \right) \end{aligned} \tag{2.4}$$

$$= V_{in} + Q_N / 2^{(M-1)(N-1)} \tag{2.5}$$

This equation shows that the quantization error from intermediate stages is canceled as long as the stage residue is within the full-scale of the subsequent ADC [1]. Also, the quantization error of the last stage is suppressed by the cumulative gain of all preceding stages. The reconstruction can be achieved by performing a shift-and-add inside the digital recombination block as shown in Fig. 2-1. Therefore, N cascaded stages of M-bit DT pipeline ADC can resolve $(M-1)\cdot(N-1)+M$ bits.

[1] The analysis shown in Eq. 2.2-2.5 holds true for any non-idealities of the sub-ADCs (such as comparator offset) as long as the residue is confined to the full-scale of the subsequent stage.

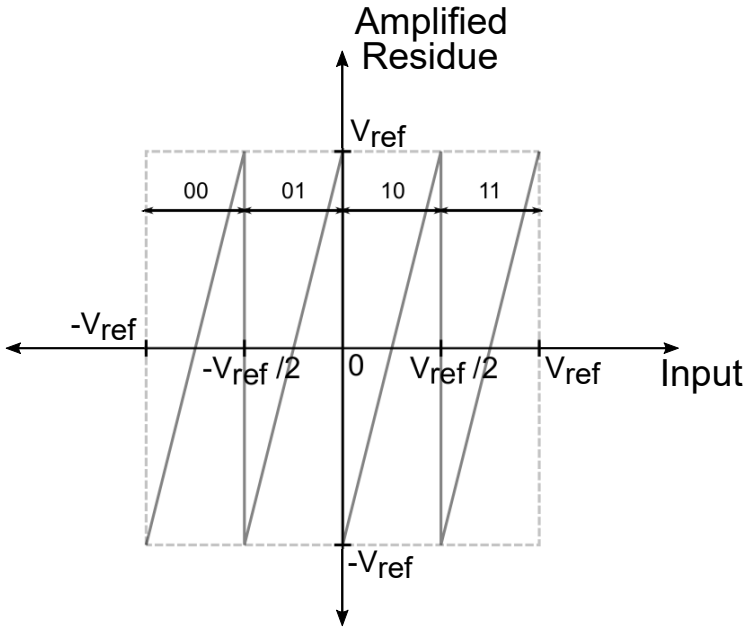


Figure 2-2: Amplified residue vs. held input for a 2-bit discrete-time pipeline stage having interstage gain = 4.

2.1.2 Residue Transfer Function and Redundancy

For an M-bit resolution sub-ADC-DAC, the interstage amplifier can ideally have a gain of 2^M to amplify the residue to the full scale of the following pipeline stage. As an example to demonstrate the residue calculation, we assume a 2-bit stage where the input varies from $-V_{ref}$ to $+V_{ref}$, the sub-ADC comparison levels are at $\{\frac{-V_{ref}}{2}, 0, \frac{V_{ref}}{2}\}$, and the interstage amplifier gain is 4. Based on the held input value and the comparison levels, the amplified residue V_{RES} can be calculated as shown below:

$$V_{RES} = \begin{cases} 4\left(V_{IN} + \frac{3V_{ref}}{4}\right) & -V_{ref} \leq V_{IN} \leq \frac{-V_{ref}}{2} \\ 4\left(V_{IN} + \frac{V_{ref}}{4}\right) & \frac{-V_{ref}}{2} \leq V_{IN} \leq 0 \\ 4\left(V_{IN} - \frac{V_{ref}}{4}\right) & 0 \leq V_{IN} \leq \frac{V_{ref}}{2} \\ 4\left(V_{IN} - \frac{3V_{ref}}{4}\right) & \frac{V_{ref}}{2} \leq V_{IN} \leq V_{ref} \end{cases} \tag{2.6}$$

where V_{IN} is the held input and V_{ref} is the reference voltage for the sub-ADC-DAC. Figure 2-2 shows the amplified residue vs. the held input for the above-mentioned pipeline stage. As the held input increases from $-V_{ref}$ to $+V_{ref}$, the digital code for

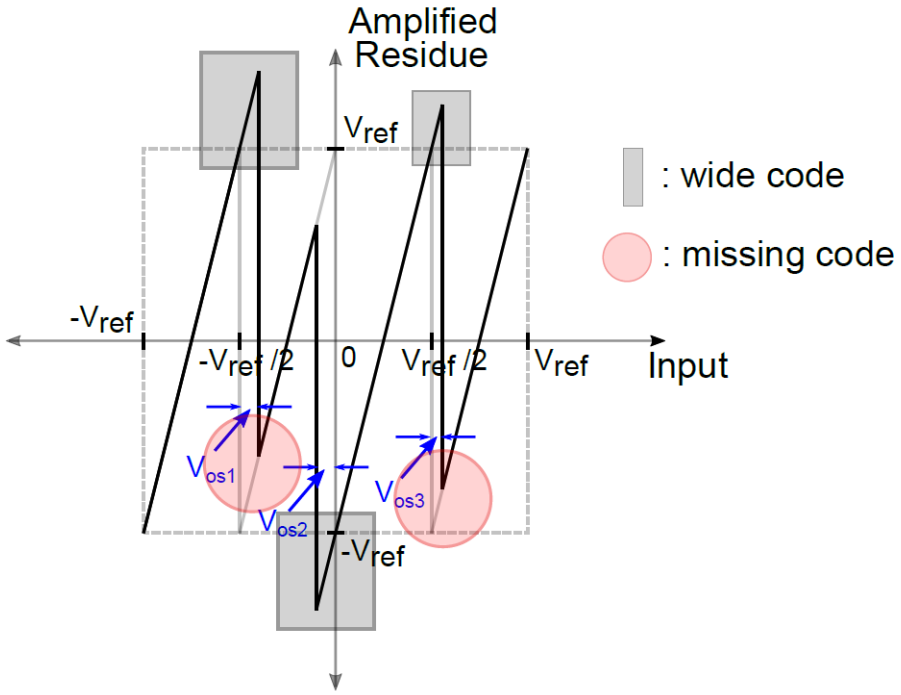


Figure 2-3: Amplified residue vs. held input with comparator offsets V_{os_1}, V_{os_2} and V_{os_3} for a 2-bit discrete-time pipeline stage having interstage gain = 4.

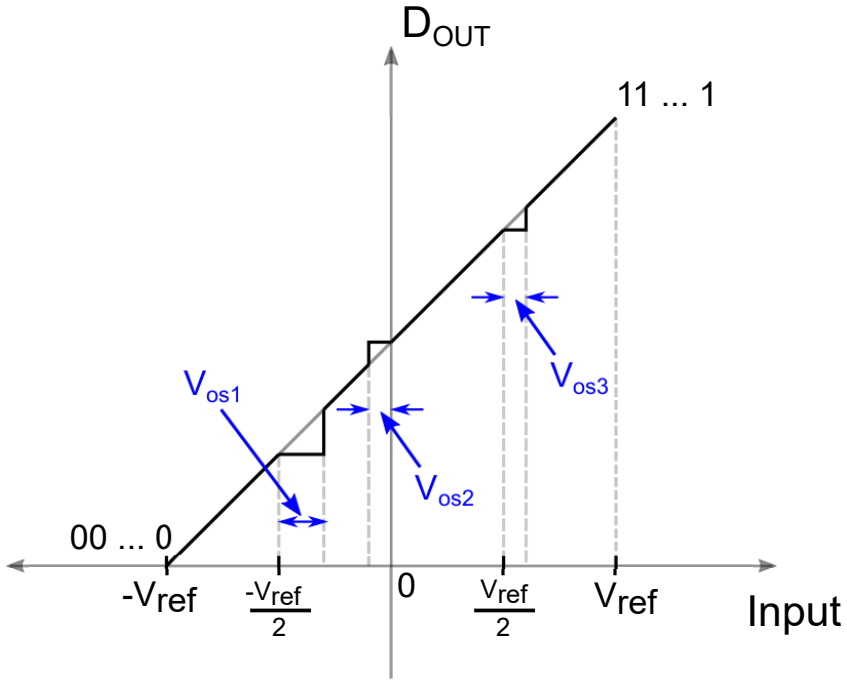


Figure 2-4: ADC Characteristic showing wide codes and missing codes due to stage-1 comparator offset.

the stage 1 increases from 00 to 11. The residue also varies from $-V_{ref}$ to $+V_{ref}$ for every digital code. Figure 2-4 shows the ideal characteristic of the ADC (assuming a very large resolution for the overall ADC).

However, in a real implementation, non-idealities such as comparator offsets, charge injection, finite opamp gain, capacitor mismatch, etc. impact the amplified residue profile by introducing gain and offset error terms. As a consequence, the amplified residue is no longer constrained to be within $\pm V_{ref}$ with an interstage gain of 2^M. This results in undesirable wide codes and missing codes in the ADC characteristic as explained below. To illustrate this, Figure 2-3 shows the amplified residue profile vs. the held input in presence of comparator offset (denoted as V_{os_1}, V_{os_2} and V_{os_3} for the comparison levels $\frac{-V_{ref}}{2}$, 0 and $\frac{V_{ref}}{2}$ respectively). Since the following pipeline stage has a limited full-scale (say within $-V_{ref}$ and V_{ref}), the amplified residue saturates the following stage for certain values of the input as shown below:

$$V_{RES} = \begin{cases} 4\left(V_{IN} + \frac{3V_{ref}}{4}\right) & -V_{ref} \leq V_{IN} \leq \frac{-V_{ref}}{2} \\ V_{ref} & \frac{-V_{ref}}{2} \leq V_{IN} \leq \frac{-V_{ref}}{2} + V_{os_1} \\ 4\left(V_{IN} + \frac{V_{ref}}{4}\right) & \frac{-V_{ref}}{2} + V_{os_1} \leq V_{IN} \leq -V_{os_2} \\ -V_{ref} & -V_{os_2} \leq V_{IN} \leq 0 \\ 4\left(V_{IN} - \frac{V_{ref}}{4}\right) & 0 \leq V_{IN} \leq \frac{V_{ref}}{2} \\ V_{ref} & \frac{V_{ref}}{2} \leq V_{IN} \leq \frac{V_{ref}}{2} + V_{os_3} \\ 4\left(V_{IN} - \frac{3V_{ref}}{4}\right) & \frac{V_{ref}}{2} + V_{os_3} \leq V_{IN} \leq V_{ref} \end{cases} \tag{2.7}$$

where V_{os_1}, V_{os_2} and V_{os_3} are the comparator offsets at the $\frac{-V_{ref}}{2}$, 0 and $\frac{V_{ref}}{2}$ comparison level respectively. When the residue exceeds the range of the following stage, i.e. $V_{RES} > V_{ref}$ or $V_{RES} < -V_{ref}$, then the subsequent pipeline, and thereby the digital code, gets stuck at the maximum or the minimum codes for the following stages. This shows up as a wide code i.e., a digital code for which the corresponding analog input range is substantially wider than 1 LSB in the ADC characteristic. When the residue range is smaller than $-V_{ref}$ to $+V_{ref}$, then the digital code jumps to a higher

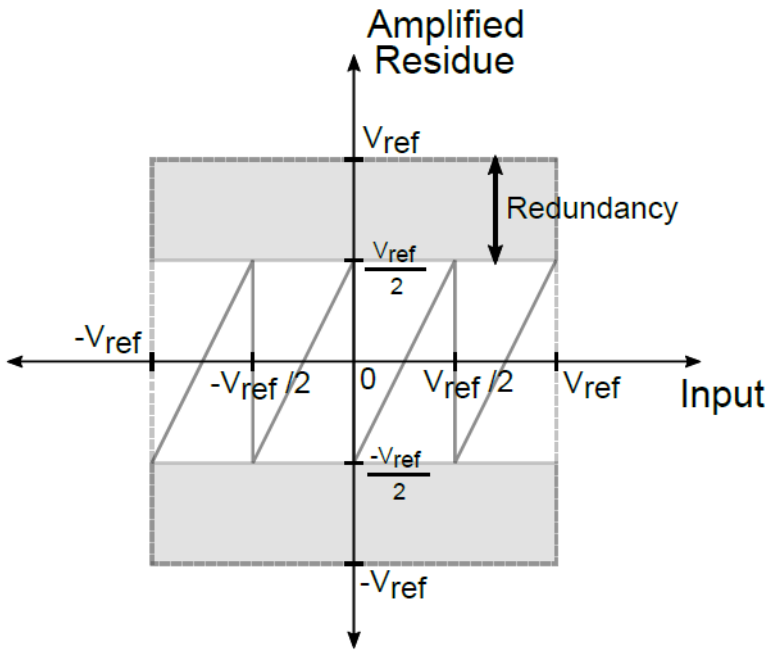


Figure 2-5: Amplified residue vs. held input demonstrating the concept of redundancy. The pipeline stage resolves 2 bits and interstage gain = 2.

value resulting in missing codes in the ADC characteristic. Figure 2-4 shows the ADC characteristic for a high-resolution multi-stage pipeline ADC where stage-1 is a 2-bit stage with comparator offsets.

To avoid saturating the residue in presence of non-idealities, redundancy can be used in the interstage gain. For an M-bit stage, the gain can be reduced by a factor of 2 and set to 2^{M-1}. This sets the residue range to $\left[\frac{-V_{ref}}{2}, \frac{V_{ref}}{2}\right]$ in the absence of non-idealities as shown in Figure 2-5. For a two-stage pipeline ADC where the stage-1 and stage-2 resolutions are n_1-bits and n_2-bits respectively, the overall ADC resolution will be $(n_1 + n_2 - 1)$-bits if there is a factor of 2 redundancy in the interstage gain. Although reducing the interstage gain reduces the overall ADC resolution, several errors due to non-idealities such as comparator offsets can be mitigated by digital recombination.

2.1.3 Design Challenges and Limitations

While a DT pipeline ADC is a popular choice for medium-resolution applications, some of its limitations have been presented in this subsection.

A DT pipeline ADC requires a sampler upfront. To avoid aliasing, an anti-alias filter must be placed before the sampler. Since the analog input passes through the anti-alias filter, its noise and distortion specifications must be at least as good as the ADC itself. Also, if the ADC bandwidth is close to half the sampling rate, then the anti-alias filter must have a sharp roll-off to avoid aliasing near the band edge. These factors increase the design complexity and power consumption of the anti-alias filter that precedes the ADC.

The ADC driver is also a power-hungry block [30, 34, 35, 39]. In some cases the input buffer's power can be a significant fraction of the overall system's power consumption. For example, in [34], the input buffer consumes 282 mW which is about 55% of the total system power (513 mW). One of the reasons for such high power consumption is that a DT pipeline ADC requires a switched-capacitor sampling upfront. The input buffer must supply the large peak currents during the charging and discharging of the capacitors, necessitating a high power consumption.

In addition to this, the upfront sampler in a DT pipeline ADC presents a fundamental bottleneck on the maximum achievable SNR in the presence of clock jitter. A timing error in the sampler clock introduces a voltage error in the sampled signal given by:

$$\Delta V_{in} = \frac{dV_{in}}{dt} \cdot \Delta t \tag{2.8}$$

where V_{in} is the analog input and Δt is the timing error in the sampling clock w.r.t. an ideal clock. As the input signal frequency increases, the jitter-induced error also increases which limits the maximum achievable SNR for a given RMS clock jitter. For a sinusoidal input with amplitude A and frequency f, the jitter-induced SNR limit

can be calculated as shown [40]:

$$\text{Signal power} = \frac{A^2}{2} \tag{2.9}$$

$$\text{Noise power} = \left(\left. \frac{dV}{dt} \right|_{rms} \times \sigma_{\Delta t} \right)^2 \tag{2.10}$$

$$= 2\pi^2 f^2 A^2 \times \sigma_{\Delta t}^2 \tag{2.11}$$

Therefore, the signal-to-noise ratio is given by:

$$\text{SNR} = \frac{\text{Signal power}}{\text{Noise power}} = \frac{1}{4\pi^2 f^2 \times \sigma_{\Delta t}^2} \tag{2.12}$$

In many cases, the ADC is oversampled. In such cases, the in-band noise power is reduced by a factor of 1/OSR. Hence, the maximum achievable SNR is given by:

$$\text{SNR}_{\text{MAX}} = \frac{\text{OSR}}{4\pi^2 f^2 \sigma_{\Delta t}^2} \tag{2.13}$$

For high-frequency inputs, clock jitter severely limits the maximum achievable SNR. For example, if a 1-GHz sinusoidal input is sampled with a clock having 500 fs RMS jitter, then the maximum achievable SNR is limited to just 50 dB (or 8 ENOB[2]). Figure 2-6 shows the deleterious effect of clock jitter as the signal frequency increases.

The above-mentioned SNR bottleneck due to the upfront sampler can be circumvented by implementing a continuous-time front end obviating the need for an upfront sampler. However, as discussed later in Section 2.2.3, the clock jitter on the DAC needs to be addressed. In addition to this, a CT input pipeline ADC offers several architectural benefits such as inherent anti-aliasing and a low driving current. These benefits make the CT pipeline ADC an attractive choice for analog-to-digital conversion in high-bandwidth integrated applications.

[2]Effective number of bits, ENOB = $\frac{\text{SNR(in dB)} - 1.76}{6.02}$

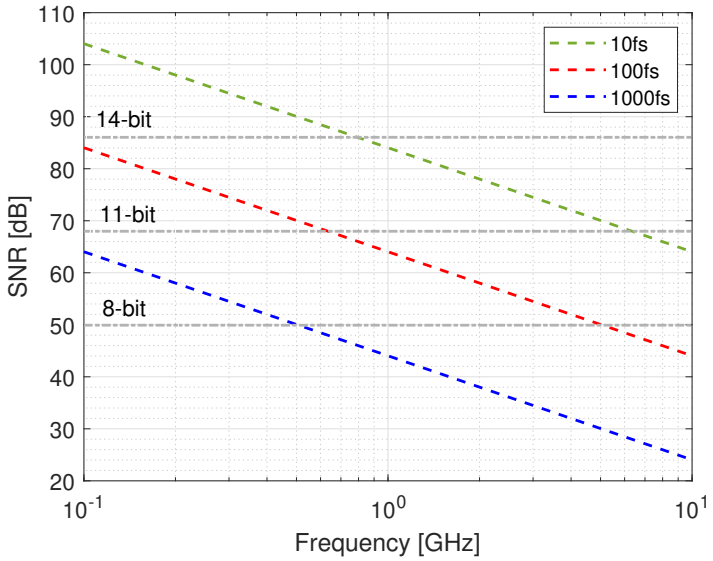


Figure 2-6: SNR v.s. the input signal frequency for various values of RMS clock jitter. For a 1-GHz sinusoidal input, the SNR is limited to 44 dB with 1 ps RMS jitter, 64 dB with 100 fs RMS jitter, and 84 dB with 10 fs RMS jitter.

2.2 Continuous-Time Pipeline ADC

A CT pipeline ADC is a multi-stage pipeline architecture in which stage 1 is continuous-time [41]. This is the defining characteristic of this ADC. The subsequent stages (stage 2 and later) can either be discrete-time [2, 5] or continuous-time [4, 6]. For simplicity, we explain the CT pipeline ADC with a 2-stage example. We assume a continuous-time first stage and a discrete-time second stage.

2.2.1 System Architecture

A 2-stage CT pipeline ADC is shown in Figure 2-7. There is no sample-and-hold upfront. The analog input V_{IN} is processed in the first stage sub-ADC-DAC path (ADC_1 and DAC_1 in Figure 2-7) to give a coarse digital estimate:

$$D_1 = V_{IN} + Q_1 \tag{2.14}$$

where Q_1 is the quantization error of the stage-1 sub-ADC. The stage-1 sub-ADC output D_1 is converted to a continuous-time voltage (or current) by the stage-1 sub-

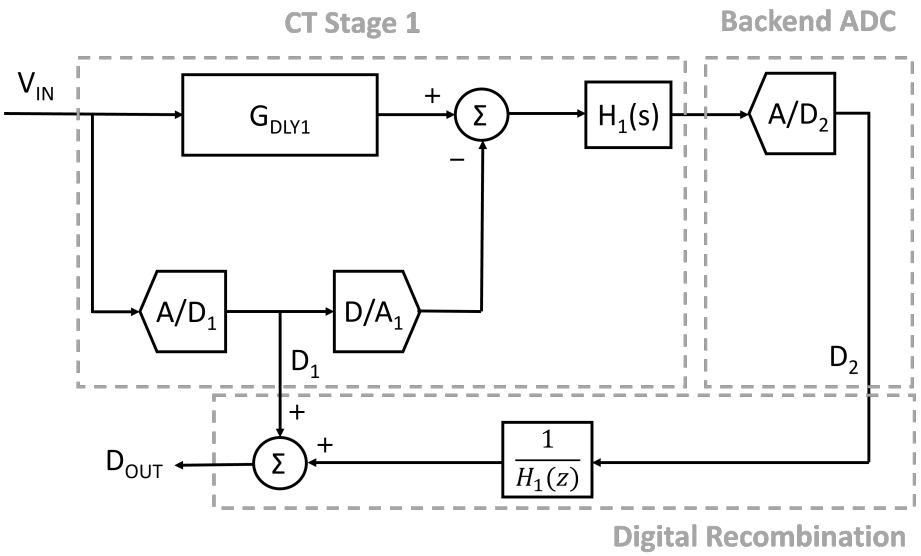


Figure 2-7: Block diagram of a 2-stage CT pipeline ADC. Stage 1 is a continuous-time stage and stage 2 is a discrete-time ADC.

DAC, which is subtracted from the delayed input signal to give the stage-1 residue:

$$R_1 = V_{IN} \cdot \Big(G_{\mathrm{DLY}_1}(s) - F_1(s) \cdot G_{\mathrm{DAC}_1}(s) \Big) - Q_1 \cdot G_{\mathrm{DAC}_1}(s) - E_{\mathrm{DAC}_1} \qquad (2.15)$$

where $G_{\mathrm{DLY}_1}(s)$, $F_1(s)$ and $G_{\mathrm{DAC}_1}(s)$ are the stage-1 delay line, sub-ADC and sub-DAC transfer functions respectively, Q_1 is the stage-1 quantization error, and E_{DAC_1} is the sub-DAC error. Figure 2-8 shows the typical stage-1 waveforms in the time domain (assuming stage-1 resolution = 4 bits and OSR = 4). It is important to note that the residue is a continuous-time signal. Therefore, the sub-DAC settling time requirement in a CT pipeline ADC is much more relaxed in comparison to a DT pipeline ADC provided the settling is linear. The linearity of the sub-DAC is still an important consideration because DAC non-linearity shows up in the digital output, and is often determined by the distortion specification of the target application.

The first term in Eq. 2.15 denotes the signal leakage component in the residue, the second term denotes the sub-ADC and sub-DAC errors, and the third term accounts for the sub-DAC errors. Stage 1 of a CT pipeline ADC must be designed such that the overall residue lies within the full scale of the following pipeline stage. If V_{FS} is

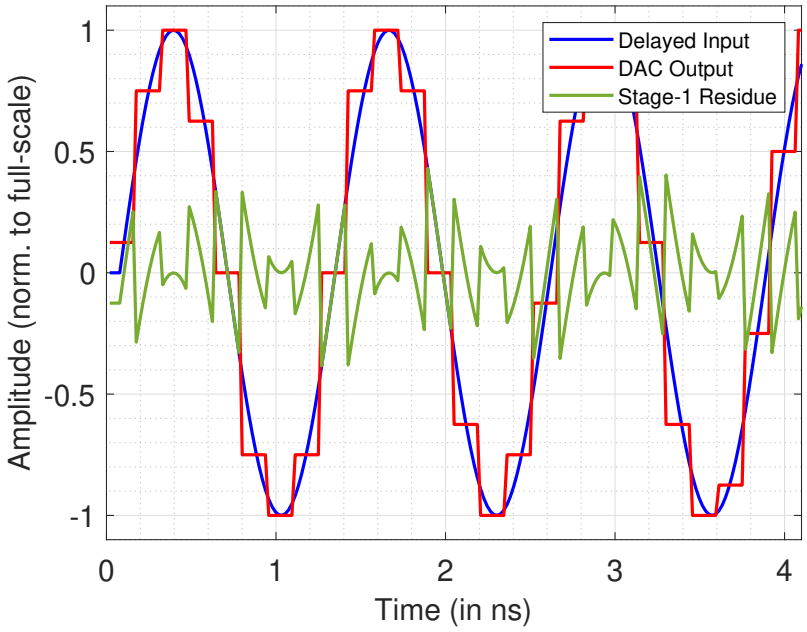


Figure 2-8: Time domain waveforms for the delayed input signal, the DAC output, and the residue for stage-1 of a CT pipeline ADC.

the full-scale of the following stage and A_1 is the stage-1 interstage gain, then the stage-1 residue must be less than V_{FS}/A_1. We call this the "residue budget".

To proceed with the CT pipeline design in a systematic manner, a certain percentage of the residue budget can be allocated to the stage-1 sub-ADC errors (such as quantization error, comparator offset, etc.) and the signal leakage component. The sub-DAC errors can be ignored for residue budget allocation since it does not affect the residue significantly since (1) the DAC images (at $f_s \pm f_{in}$, $f_s \pm 2f_{in}$ and so on) are filtered by the interstage amplifier, and (2) the noise floor of the DAC output is very low – of the order of the noise floor for the entire pipelined ADC – therefore, it does not increase the residue amplitude significantly.

As a good rule of thumb, about 30% of the residue budget can be allocated to the signal leakage component. The rest of the residue budget can be allocated for the sub-ADC errors. This means that the signal transfer function G_{DLY_1} should be sufficiently matched to the sub-ADC-DAC transfer function $F_1(s) \cdot G_{\mathrm{DAC}_1}(s)$ such that the signal leakage component occupies no more than 30% of the residue budget across the entire ADC bandwidth. This can be used as a guiding principle to design

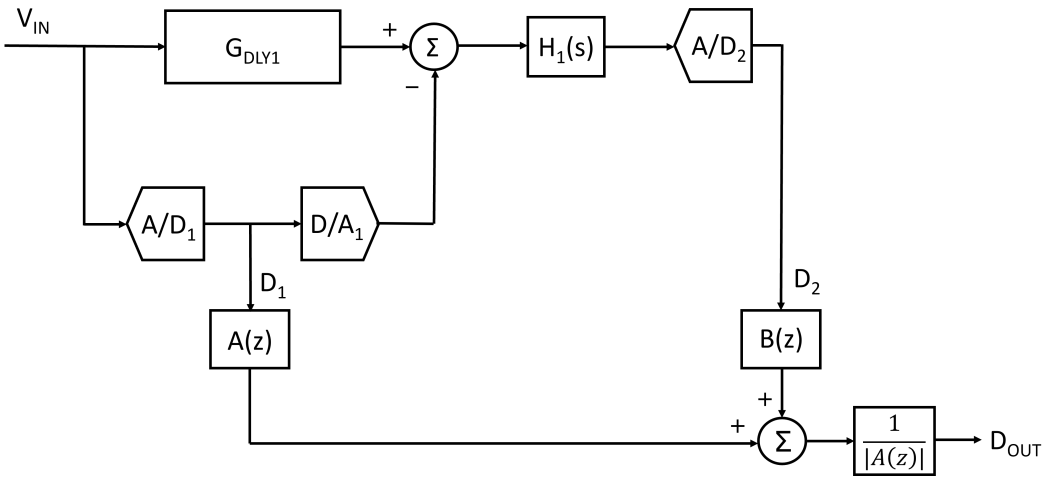


Figure 2-9: A block diagram for a CT pipeline ADC showing the digital recombination filter implemented as 2 FIR filters $A(z)$ and $B(z)$.

the delay line and is explained in further detail in section 3.2.

The stage-1 residue is amplified and low-pass filtered by the interstage amplifier. The interstage amplifier transfer function is denoted as $H_1(s)$. Typically, the DC gain of the interstage amplifier is 2^{M-1}, where M is the resolution of the stage-1 sub-ADC and the cut-off frequency is set to be the bandwidth of the ADC. The stage-2 input is given by:

$$V_{\mathrm{STG_2}} = V_{\mathrm{RES}} \cdot H_1(s) \tag{2.16}$$

$$= V_{IN}\Big(G_{\mathrm{DLY_1}}(s) - F_1(s)G_{\mathrm{DAC_1}}(s)\Big) \cdot H_1(s) \tag{2.17}$$

$$- Q_1 \cdot G_{\mathrm{DAC_1}}(s) \cdot H_1(s) - E_{\mathrm{DAC_1}} \cdot H_1(s)$$

The stage 2 of the CT pipeline ADC digitizes V_{STG_2} to give the stage-2 digital output:

$$D_2 = V_{STG_2} + Q_2 \tag{2.18}$$

where Q_2 is the quantization error of the stage 2 ADC. Similar to a DT pipeline ADC, each stage output in a CT pipeline ADC are combined digitally to give the final ADC output:

$$D_{OUT} = D_1 + H_{DRF} \cdot D_2 \tag{2.19}$$

where H_{DRF} is the transfer function of the digital reconstruction filter (DRF). To get a high resolution from the CT pipeline ADC, the stage-1 quantization error term needs to be canceled from the individual stage digital data. If the impulse invariant transformation is denoted by $\mathcal{I}$, then the DRF transfer function is nominally designed to be:

$$H_{DRF}(z) = \mathcal{I}\left(\frac{1}{G_{DAC_1}(s) \cdot H_1(s)}\right) \tag{2.20}$$

The extent of cancellation of the stage-1 errors is contingent upon the accuracy of the DRF transfer function. In practice, the DRF is implemented as 2 FIR filters to reduce the number of taps, and thereby the power consumption, for the digital filter. For instance, if $H_{DRF}(z) \equiv B(z)/A(z)$, then $D_{OUT} = A(z)D_1 + B(z)D_2$ along with appropriate magnitude scaling as shown in Figure 2-9.

2.2.2 Choice of Stage-1 Resolution and Oversampling Ratio

The continuous-time operation of the first stage presents an interesting situation where the stage-1 resolution and the oversampling ratio parameters must be co-designed. One of the primary considerations for choosing these parameters is that the residue must not saturate the following pipeline stage. Also, a stage-1 resolution of 3-5 is preferred, to allow for a larger interstage gain, so that the backend noise is suppressed well without a significant power penalty in stage 1.

The stage-1 residue is determined by (a) how fast the signal varies w.r.t. the clock frequency of the sub-ADC-DAC (a sampling speed problem, shows up on the time-axis), and (b) how fine the stage-1 sub-ADC-DAC resolves the signal (a quantization problem, shows up on the amplitude-axis). For instance, for lower values of OSR (≤ 4), the DAC output jump from sample to sample is determined mostly by the sub-ADC-DAC sampling rate and not by the stage-1 resolution. Therefore, increasing the stage-1 resolution beyond a certain point without changing the OSR will have almost no effect on the residue shape or its amplitude as shown in Figure 2-10. Similarly, for relatively higher OSR values (≥ 16), the DAC output closely tracks the input signal. In such cases, the DAC step size depends on the stage-1 resolution. Increasing the

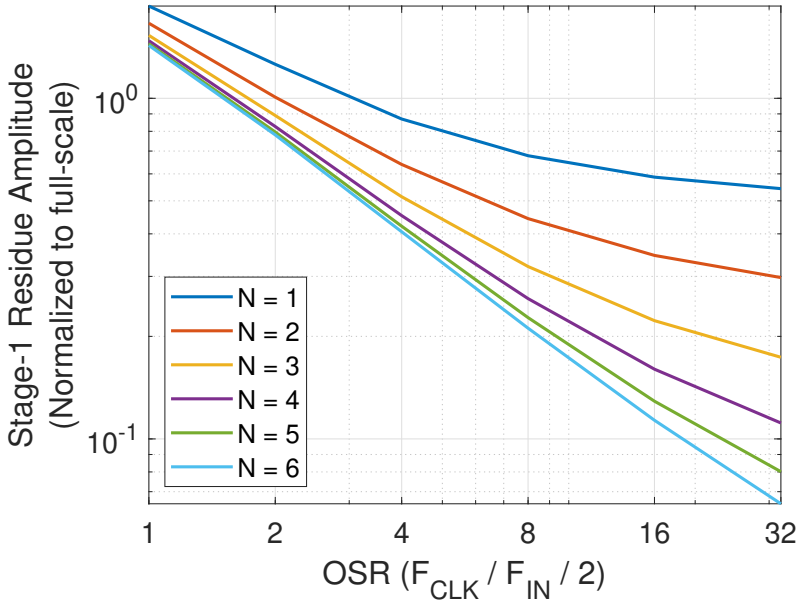


Figure 2-10: Variation of stage-1 residue amplitude vs. ADC OSR for different values of stage-1 resolution ($N_{STG_1} = 1 : 6$).

stage-1 resolution directly impacts the residue shape and can significantly reduce its amplitude. Given a residue budget, the resolution and the OSR of Stage 1 must be carefully selected.

Figure 2-10 shows the variation of residue amplitude with OSR for different values of stage-1 resolution. Assuming that the residue can occupy 80% of the full scale without causing significant non-linearity in the interstage amplifier, the stage-1 resolution should be more than 4 bits for OSR = 2, and more than 2 bits for OSR = 4. There are two key observations from Figure 2-10. First, for small OSR (≤ 2), the residue amplitude is almost the same for stage-1 resolution > 3. This shows that increasing the resolution beyond a certain number of bits does not help in reducing the amplitude magnitude for low OSR. Second, for large OSR, the residue amplitude begins to saturate for lower stage-1 resolution. This suggests that increasing the OSR at that resolution gives diminishing returns w.r.t. reducing the residue amplitude. Also, for higher sampling rates, increasing the resolution is a good option to keep the residue amplitude small.

In addition to the analysis of the stage-1 residue, the stage-2 input (low-pass

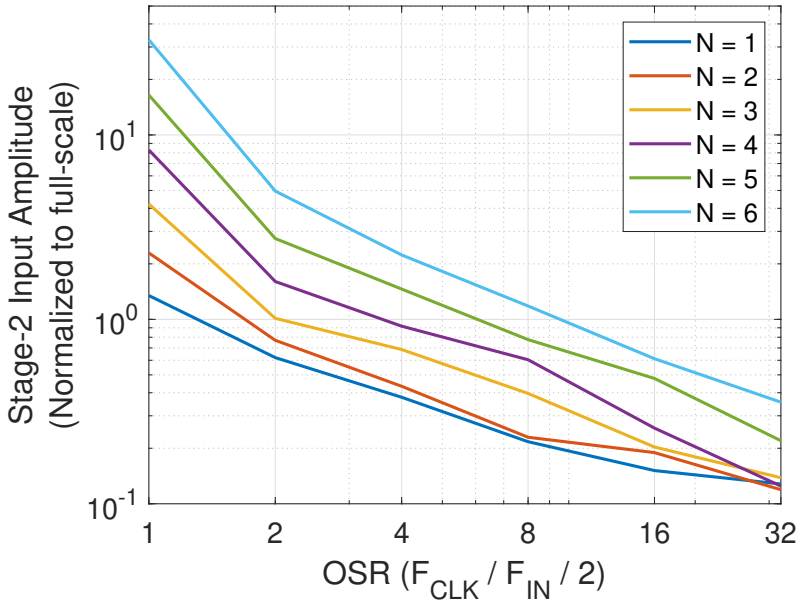


Figure 2-11: Variation of stage-2 input amplitude vs. ADC OSR for different values of stage-1 resolution ($N_{STG_1} = 1 : 6$).

filtered and amplified residue) must also be analyzed to ensure that the subsequent ADC does not saturate. Figure 2-11 shows the stage-2 input (amplified and low-pass-filtered residue) vs. OSR for varying stage 1 resolution. The interstage gain is set to be 2^{N_1-1} where N_1 is the stage-1 resolution. It is instructive to see the $N_1 = 6$ graph. For OSR = 4, a 6-bit resolution stage 1 seems to be no better than a 4-bit resolution stage 1 because the additional quantization levels do not help in reducing the residue amplitude. Since the interstage gain is set to 32, the residue magnitude goes beyond the full scale of the subsequent ADC. To prevent stage 2 from saturating, the interstage gain must be reduced. This negates the benefits of using a higher resolution in the first stage. Therefore, unless the sub-ADC-DAC path is sampling fast enough, increasing the stage 1 resolution beyond a certain value does not yield any significant benefits at the system level. In typical CT pipeline designs, a 3- or 4-bit first stage is good enough to achieve signal cancellation, and to strike a balance between the number of quantization levels and the sampling rate of the sub-ADC-DAC path for OSR = 4 operation.

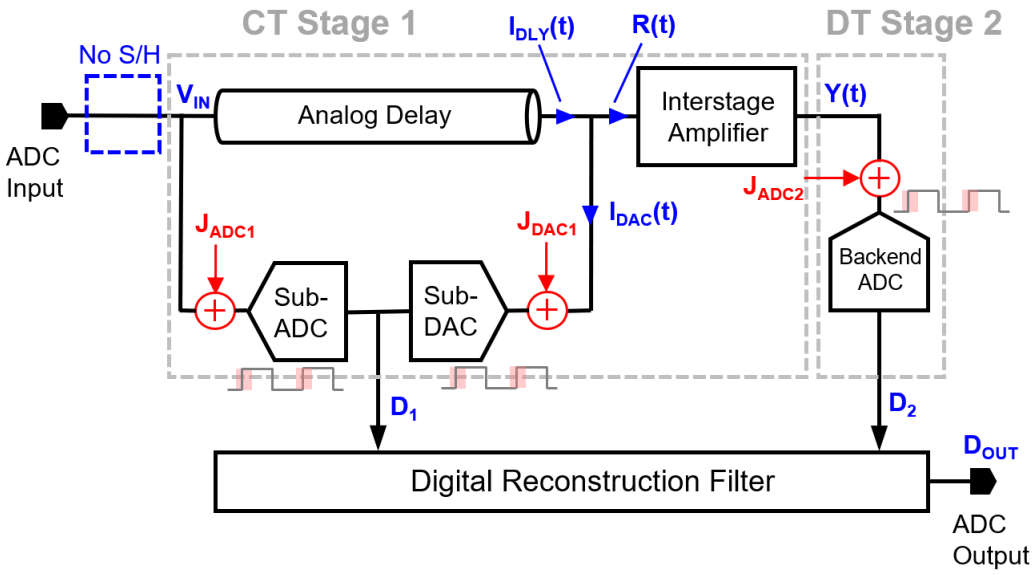


Figure 2-12: A block diagram for a CT pipeline ADC showing the various sources of clock jitter-induced error.

2.2.3 Impact of Clock Jitter in a CT Pipeline ADC

While a continuous-time front end in a CT pipeline ADC circumvents the problem of upfront sampling jitter as discussed in section 2.1.3, clock jitter may still impact the following sub-blocks: (1) stage-1 sub-ADC, (2) stage-2 ADC, and (3) stage-1 sub-DAC (see Figure 2-12). The clock jitter-induced errors have been shown as additive errors J_{ADC_1},J_{ADC_2}, and J_{DAC_1} respectively, and their effects are discussed next.

The jitter error added at the stage-1 sub-ADC affects the individual stage data as shown below:

$$D_1 = V_{IN} + Q_1 + J_{ADC_1} \tag{2.21}$$

$$D_2 = (-Q_1 - J_{ADC_1}) \cdot H_1 + Q_2 \tag{2.22}$$

If we assume an accurate digital reconstruction, then J_{ADC_1} gets canceled, similar to the stage-1 quantization error. Thus, the stage-1 sub-ADC jitter error does not impact the overall digital output significantly. One might think that since J_{ADC_1} gets added to the sub-ADC-DAC path, it might increase the residue and overload the backend ADC. But this does not happen because typically the residue noise floor is

dominated by the sub-ADC quantization noise[3].

At the stage-2 input, the clock jitter acts on the amplified residue signal. Typically, the residue has a small amplitude because of the signal cancellation in the first stage. In the worst case, if the signal leakage is significant, then the residue can occupy the entire full scale of the stage-2 ADC. Since the residue is bandlimited by the low pass characteristic of the interstage amplifier, the maximum signal-slope is limited to $2\pi f_{BW} A_m$ where A_m is the maximum amplitude ($= V_{FS}/2$) and f_{BW} is the ADC bandwidth. Therefore, an upper bound on the stage-2 jitter error can be calculated as shown:

$$J_{ADC_2} = \frac{dV_{RES}}{dt} \cdot \Delta t_j \tag{2.23}$$

$$\leq 2\pi f_{BW} A_m \cdot \Delta t_j \tag{2.24}$$

where Δt_j is the timing error due to the stage-2 clock jitter. Similar to the stage-2 quantization error, the jitter-induced error is also reduced by a factor of the first-stage gain when stage 1 and stage 2 digital outputs are combined:

$$D_1 = V_{IN} + Q_1 \tag{2.25}$$

$$D_2 = (-Q_1) \cdot H_1 + Q_2 + J_{ADC_2} \tag{2.26}$$

$$\begin{aligned} D_{OUT} &= D_1 + D_2 \cdot \frac{1}{H_1} \\ &= V_{IN} + \frac{Q_2 + J_{ADC_2}}{H_1} \end{aligned} \tag{2.27}$$

Therefore, in a case where the clock jitter is the dominant noise source, then the

[3]Typically, the stage 1 resolution is only 3 to 4 bits.

signal-to-noise ratio is given by:

$$\begin{aligned} \mathrm{SNR_j} &= \frac{A_m^2/2}{J_{ADC_2}^2/A_{v_1}^2} \\ &\geq \frac{A_m^2/2}{4\pi^2 f_{BW}^2 \frac{A_m^2}{2}\sigma_{\Delta t_j}^2/A_{v_1}^2} \\ &\geq \frac{A_{v_1}^2}{4\pi^2 f_{BW}^2 \sigma_{\Delta t_j}^2} \end{aligned} \tag{2.28}$$

where A_{v_1} is the low-frequency interstage gain and $\sigma_{\Delta t_j}$ is the RMS value of the clock jitter. Equation 2.28 shows that the noise due to stage-2 clock jitter is suppressed by the gain of the interstage amplifier even in teh worst case when the residue occupies the full scale input of stage 2. For a 4-bit stage-1 resolution, i.e. an interstage gain of 8, the stage-2 jitter noise is suppressed by 18 dB. Therefore, in a practical CT pipeline implementation, the stage-2 jitter does not limit the performance of the overall ADC.

Finally, the stage-1 sub-DAC clock jitter also impacts the ADC performance. Its effect on digital data is as shown below:

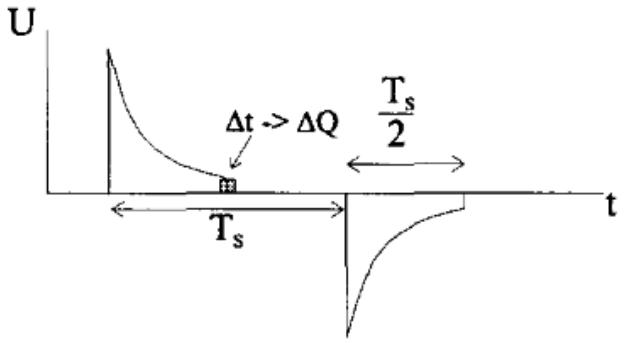
$$D_1 = V_{IN} + Q_1 \tag{2.29}$$

$$D_2 = (-Q_1 + J_{DAC_1}) \cdot H_1 + Q_2 \tag{2.30}$$

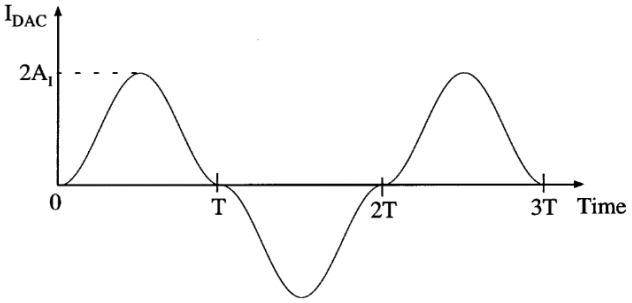
$$D_{OUT} = D_1 + D_2 \cdot \frac{1}{H_1} = V_{IN} + \frac{Q_2}{H_1} + J_{DAC_1} \tag{2.31}$$

Since the sub-DAC errors are added after stage-1 sub-ADC, or after D_1 in the signal chain, they only show up in the stage-2 digital data D_2. This error does not get canceled and shows up in the final digital output. The DAC jitter error J_{DAC_1} will depend on the sub-DAC architecture, the shape of the DAC pulse, and its resolution. Further analysis is required to assess the severity of the sub-DAC clock jitter on the overall ADC performance. We first present a discussion on choosing a suitable pulse shape for the sub-DAC output, followed by a jitter analysis showing the SNR limitation due to the DAC jitter.

In previous works related to D/A converters, several DAC pulse shapes have been implemented, such as non-return-to-zero (NRZ), return-to-zero (RZ), dual return-to-



(a) A switched-capacitor-based DAC with an exponential pulse shape [42].



(b) A raised-cosine DAC pulse [43].

Figure 2-13: Pulse-shaped DACs with reduced sensitivity to clock jitter.

zero, exponential (switched capacitor implementations) and raised cosine [11, 43–49]. These DAC pulses provide a varying degree of tolerance to the clock jitter. For example, the switched capacitor-based DAC and the raised cosine DAC have been shown to be less sensitive to clock jitter because the DAC output has a smaller slope near the clock edges, and thereby less sensitive to timing jitter (Figure 2-13). Ortmanns *et al.* [49] have shown an in-band noise reduction of 15 dB with a switched-capacitor-based feedback (SCR) DAC in comparison to an RZ DAC in a continuous-time $\Delta\Sigma$ modulator (assuming RMS jitter to be 1% of the clock period). Luschas *et al.* [43] have shown that in a continuous-time $\Delta\Sigma$ modulator, using a raised-cosine DAC pulse provides 17 dB jitter noise suppression compared to NRZ DAC, and 8 dB jitter noise suppression compared to upfront sampled ADCs.

However, the SCR DAC and the raised-cosine DAC are not suitable for use as the stage-1 sub-DAC in a CT pipeline ADC for the following reason: at the stage-1 summing node, the delayed input and the sub-DAC output are subtracted. Since

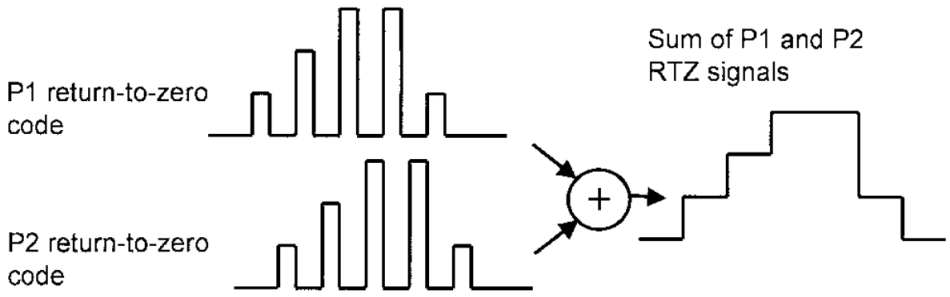


Figure 2-14: Dual return-to-zero DAC [11].

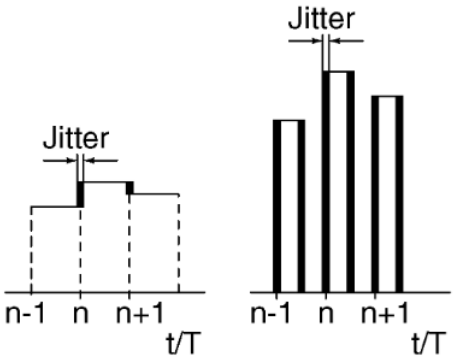


Figure 2-15: The effect of timing jitter on an NRZ- and RZ-DAC waveforms [12]. Theoretically, the dual-RZ and the NRZ-DAC have the same sensitivity to clock jitter.

the residue is a continuous-time signal, it is not held at a constant value and it can swing across the ADC full-scale. If the DAC output is pulse-shaped, then for certain portions of the clock period, the subtraction of delayed input and the sub-DAC output gives a large residue. This may not only cause a linearity issue in the interstage amplifier but also has the potential to saturate the subsequent ADC stage. However, if the DAC clock jitter is the dominant source of noise, then pulse-shaped DACs wtih higher OSR still may prove to be a good solution.

Although an RZ DAC also faces the above-mentioned issue, a dual-RZ DAC (Figure 2-14) can be used to provide a non-zero DAC output for the entire clock period. Additionally, as shown in Figure 2-15 compared to an RZ DAC, the dual-RZ DAC is less sensitive to the clock jitter because the timing jitter acts on the amplitude difference of the consecutive DAC output instead of the full DAC output:

$$J_{\mathrm{RZ}} = v[n] \cdot \Delta t_j \tag{2.32}$$

$$J_{\mathrm{dual-RZ}} = (v[n] - v[n-1]) \cdot \Delta t_j \tag{2.33}$$

where J_{RZ} and $J_{\mathrm{dual-RZ}}$ are the DAC jitter error at the n-th sample for a return-to-zero and a dual return-to-zero DAC, $v[n]$ is the DAC output at the n-th clock edge, and Δt_j is the timing error at the n-th clock edge. For improving the jitter tolerance of the CT pipeline ADC, both dual-RZ and NRZ DAC are good candidates for the sub-DAC. However, in a dual-RZ DAC, there can be glitches at $T_{CK}/2$ if the fall time for the phase-1 pulse is different than the rise time for the phase-2 pulse. This is an intentional feature of the dual-RZ DAC which helps in canceling the errors due to intersymbol interference [11]. However, such glitches at the phase-1-2 transition will introduce undesirable glitches in the stage-1 residue. Considering the above-mentioned factors, an NZR DAC is a good candidate for sub-DAC in stage 1 of a CT pipeline ADC. Since the DAC jitter error directly adds to the digital output (Equation 2.31), we now present an analysis of the DAC jitter error for an NRZ DAC.

Any clock jitter in the NRZ DAC introduces a timing error in the DAC output edge which injects an error voltage (or current) in the DAC output given by:

$$e_j(t) = \sum_n (v[n] - v[n-1]) \cdot \Delta t_n \tag{2.34}$$

where $e(t)$ is the error in the DAC output voltage (or current), v[n] is the n-th sample at the DAC input, and Δt_n is the timing error for the n-th edge of the clock. When Δt_n is much smaller than the clock period (T_{CK}), then the output error pulses can be approximated with error impulses. Thus, the DAC jitter error can be modeled as a fictitious digital error sequence at the input of the DAC, given by:

$$e_j[n] = (v[n] - v[n-1]) \cdot \frac{\Delta t_n}{T_{CK}} \tag{2.35}$$

Note that the power of the DAC output error pulse because of this error sequence will still be $(v[n] - v[n-1]) \cdot \Delta t_n / T_{CK} \times T_{CK} = (v[n] - v[n-1]) \Delta t_n$, consistent with

Eq. 2.34. Since $v[n]$ and Δt_n are independent variables, the variance of the DAC input error sequence is given by:

$$\overline{e_j^2} = \frac{\sigma_{\Delta v}^2 \sigma_{\Delta_t}^2}{T_{CK}^2} \tag{2.36}$$

where $\sigma_{\Delta_v}^2$ is the variance of $(v[n] - v[n-1])$ and $\sigma_{\Delta_t}^2$ is the variance of timing jitter. Assuming that the PSD of $(v[n] - v[n-1])$ and clock jitter is white, the in-band jitter-induced noise power P_j is given by:

$$P_j = \frac{\sigma_{\Delta v}^2 \sigma_{\Delta_t}^2}{T_{CK}^2} \cdot \frac{1}{\text{OSR}} \tag{2.37}$$

For a sinusoidal analog input $u(t) = A\cos(2\pi f_{in} t)$, the corresponding digital sequence $v[n]$ is given by:

$$v[n] = u(t)\Big|_{t=nT_{CK}} = A\cos(2\pi f_{in} \cdot nT_{CK}) \tag{2.38}$$

The variance of $v[n] - v[n-1]$ can be calculated as shown below:

$$v[n] - v[n-1] = A\Big(\cos(2\pi f_{in} \cdot nT_{CK}) - \cos(2\pi f_{in} \cdot \overline{n-1}\ T_{CK})\Big) \tag{2.39}$$

$$= -2A\sin\left(2\pi f_{in} T_{CK} \frac{\overline{n-(n-1)}}{2}\right) \sin\left(2\pi f_{in} T_{CK} \frac{\overline{n+(n-1)}}{2}\right) \tag{2.40}$$

$$= -2A\sin\Big(\pi f_{in} T_{CK}\Big) \sin\Big(2\pi f_{in} T_{CK}\ \overline{n-0.5}\Big) \tag{2.41}$$

For a relatively higher OSR, $f_{in} << 1/T_{CK}$. In such cases, $\sin(\pi f_{in} T_{CK}) \approx \pi f_{in} T_{CK}$, and the expression in Eq. 2.41 can be simplified as:

$$v[n] - v[n-1] = -2\pi f_{in} T_{CK} \cdot A\sin\Big(2\pi f_{in} T_{CK}\ \overline{n-0.5}\Big) \tag{2.42}$$

Thus, the variance of $v[n] - v[n-1]$ is given by:

$$\sigma_{\Delta v}^2 = 4\pi^2 f_{in}^2 T_{CK}^2 \cdot \frac{A^2}{2} \tag{2.43}$$

Plugging the above expression in Eq. 2.37, the jitter-induced in-band noise power can be calculated as:

$$P_j = 2\pi^2 f_{in}^2 \sigma_{\Delta t}^2 A^2 \cdot \frac{1}{\text{OSR}} \tag{2.44}$$

If the jitter-induced noise is the largest noise contributor in the overall system, then the signal-to-noise ratio will be given by:

$$\text{SNR}_j = \frac{A^2/2}{2\pi^2 f_{in}^2 \sigma_{\Delta t}^2 A^2} \cdot \text{OSR} = \frac{\text{OSR}}{4\pi^2 f_{in}^2 \sigma_{\Delta t}^2} \tag{2.45}$$

This expression is identical to the SNR limitation for upfront sampled ADCs as shown in Equation 2.13. In the context of $\Delta\Sigma$ modulators, CT-$\Delta\Sigma$ modulators have been shown to be more susceptible to clock jitter in comparison to DT-$\Delta\Sigma$ modulators [50,51]. However, in a CT pipeline ADC, under the assumption of a high OSR [4], the sub-DAC jitter presents the same SNR bottleneck as the sample-and-hold in a conventional DT pipeline ADC.

In conclusion, for applications requiring high bandwidth, and/or, where having a low jitter clock is not feasible (perhaps due to other on-chip components generating noise), the sub-DAC jitter can become the bottleneck for SNR in a CT pipeline ADC.

2.3 Summary

In this chapter, we presented a comprehensive analysis of the discrete-time and continuous-time pipeline A/D converters. The system architecture, design considerations, and limitations were discussed. The proposed CT pipeline ADC is described in Chapter 3. In a CT pipeline ADC, the signal leakage in the first stage residue can substantially increase the residue amplitude, resulting in either the saturation of the backend ADC, or in the reduction of the interstage gain, resulting in reduced backend ADC noise suppression. Also, as discussed in section 2.2.3, the sub-DAC

[4]The DAC resolution should be high enough so that the effect of quantization noise can be ignored in the noise computation. For a given OSR, it turns out that increasing the DAC resolution beyond a certain number of bits does not reduce the noise floor any further because the DAC step size will be limited by the sampling rate relative to the input frequency.

jitter can limit the overall SNR if the noise floor is dominated by the jitter-induced noise. In the following chapter, we present a CT pipelined ADC with time-interleaved sub-ADC-DAC path which addresses the above-mentioned issues in the CT pipeline ADC architecture (section 3.1.2). In section 3.2, we present the design methodology for the stage 1 delay line, and propose an inductorless 4x-cascaded RC lattice based delay line to minimize the signal leakage in the first stage residue.

Chapter 3

Proposed CT Pipeline ADC

3.1 System Architecture

As discussed in the previous chapter (subsection 2.2.3), for high bandwidth applications, the SNR of the CT pipeline ADC may be limited by the DAC jitter. While there has been some previous work on jitter tolerant DAC designs [43, 44, 46, 47], shaped DAC pulses such as a switched capacitor or raised-cosine are not suitable for use as the sub-DAC in CT pipeline ADCs because they result in an imperfect cancellation of the input signal resulting in a large residue. This results in either the saturation of the backend ADC or the reduction of the interstage gain, thereby reducing the backend ADC noise suppression.

A non-return-to-zero DAC is the most suitable DAC type in a CT pipeline ADC as decsribed in Section 2.2.3. However, due to a relatively small OSR (≈ 4), the DAC step size is usually much larger than 1 LSB (full-scale / 2^{N_1} where N_1 is the stage 1 resolution). For example, in a 4-bit sub-ADC-DAC path, the least possible DAC step-size is $I_{FS}/16 = 0.0625\ I_{FS}$, but for OSR = 4, the average DAC step-size is $0.25 I_{FS}$ [1]. Despite having a 4-bit resolution in the sub-ADC-DAC path, the benefit of an NRZ-DAC w.r.t. jitter tolerance is not realized.

In the next section, we present some ideas for improving the jitter tolerance of

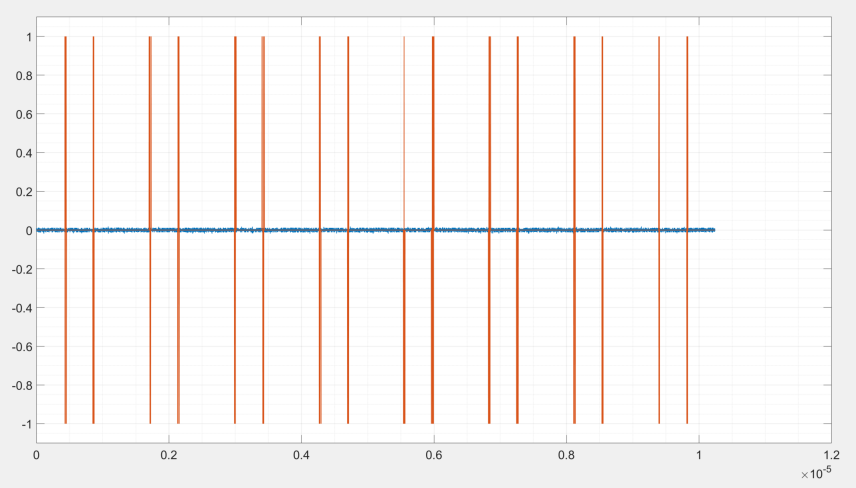
[1] We have calculated the average DAC step size as $\frac{1}{N}\sum_{n=1}^{N}\big(v[n] - v[n-1]\big)$ where v[n] is the n-th DAC output.

a CT pipeline ADC. Then, we present the proposed CT pipeline architecture which achieves an improved clock jitter tolerance in comparison to the previously works on CT pipeline ADCs.

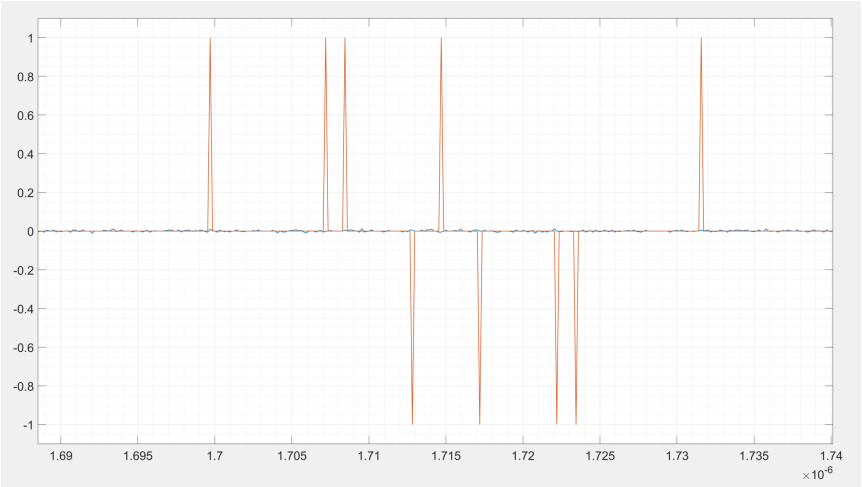
3.1.1 A Level-Crossing-Based CT Pipeline ADC

One way to realize a 1 LSB DAC step-size could be to use level-crossing-based non-uniform sampling [52–66]. In such a scenario the sub-ADC output transition is triggered when the signal crosses a particular comparator threshold. By definition, the DAC output step size will be 1 LSB for all transitions. While this technique certainly helps in reducing the sensitivity to sub-DAC jitter, there are a few practical problems with this approach: (1) the sub-ADC comparators are continuous-time, thus must be always on. This will increase the static power consumption of the ADC. (2) the stage-1 digital output is a continuous-time signal. There are two options to perform digital recombination: (A) to go through the rest of the pipeline in a continuous-time manner. In this case, all stage outputs are continuous-time. The digital recombination for such a system will necessitate a continuous-time digital filter increasing the system's complexity. Also, this will create an incompatibility with the subsequent digital processing because, in almost all hardware systems, digital signal processing (DSP) is done in the discrete-time domain. (B) An alternative to processing all stage outputs in continuous-time could be to re-time the stage-1 continuous-time discrete-amplitude signal. Then, in principle, the digital recombination can be performed with standard digital filters, and this method will preserve compatibility with the rest of the DSP.

However, re-timing the stage-1 digital output creates a different jitter-related problem – the re-timing clock has jitter and this results in a severe SNR degradation for the overall ADC. Since the stage-1 output is discrete-amplitude (i.e. held constant till a level-crossing event triggers a sub-ADC transition), there is no impact of clock jitter while re-timing the stage-1 output. This holds true when the ideal clock edge is sufficiently distant from a sub-ADC level transition ($< -3\ \sigma_{\Delta t}$ or $> +3\ \sigma_{\Delta t}$ where $\sigma_{\Delta t}$ is the RMS clock jitter). However, there is no way to ensure that this condition



(a) Zoomed-out time-domain simulation showing the jitter error during re-timing (orange). The aperture error has been shown in blue.



(b) Zoomed-in time-domain simulation showing the jitter error during re-timing (orange). The aperture error has been shown in blue.

Figure 3-1: Time-domain illustration of the jitter-induced error in stage-1 digital output during re-timing. A 3-level sub-ADC is assumed to simplify the illustration.

will hold true in a real implementation. In fact, for a periodic input to the ADC, the clock edge will fall close to the sub-ADC level transition periodically, based on the least common multiple of the input frequency and the clock frequency.

This will also happen for a non-periodic input signal albeit sporadically. The impact of clock jitter in such scenarios is deleterious. Figure 3-1 shows the error in the re-timed stage-1 output (shown in orange) compared to the aperture error in an upfront sampled ADC (shown in blue, it stays very close to zero because it

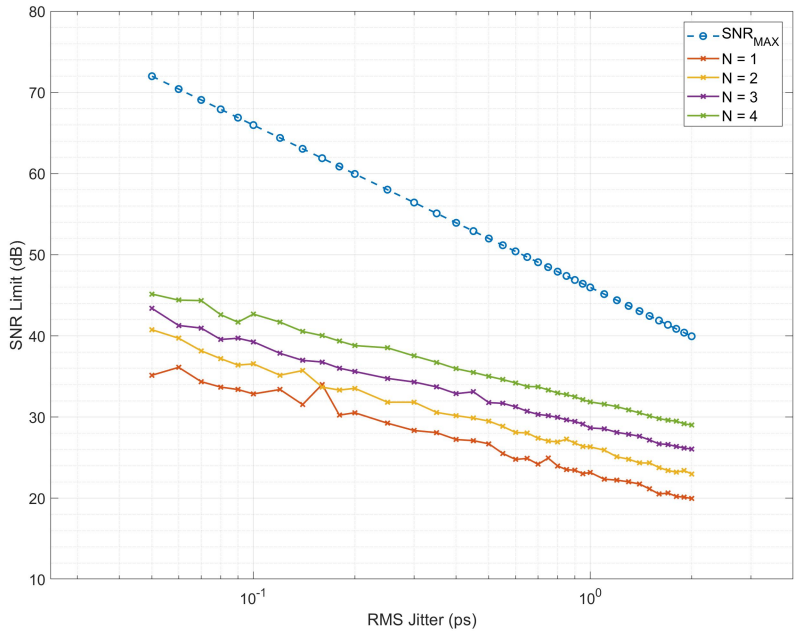


Figure 3-2: Comparison of jitter-induced SNR limitation of a level-crossing based CT pipeline ADC with an upfront sampled ADC.

is proportional to the derivative of the input signal). A 3-level quantizer and a sinusoidal input is assumed for the purpose of illustration. The error in the re-timed signal happens infrequently when the clock edge is within $\pm 3\ \sigma_{\Delta t}$ of the sub-ADC level transitions. However, the error magnitude is 1 LSB, orders of magnitude higher than the error in an upfront sampler. This increases the error power in the stage-1 digital output and limits the SNR of the entire ADC. To make matters worse, since this error adds outside the pipelined signal chain, there is fundamentally no way to estimate this error either through the sub-DAC or digitally. Hence, this error cannot be subtracted out digitally as is usually done in pipelined converters.

Figure 3-2 compares the SNR limitation of the level-crossing-based CT pipeline (sub-ADC-DAC resolution is varied from 1-bit to 4-bit, the input frequency is 800 MHz, and the clock frequency is 6.4GHz) with an upfront sampled A/D converter. The jitter error during re-timing the stage-1 digital output degrades the SNR by about 20 dB for 100 fs jitter, and about 26 dB for 50 fs jitter. Intuitively, this can be understood as follows: hypothetically, if we keep on increasing the number of threshold levels in

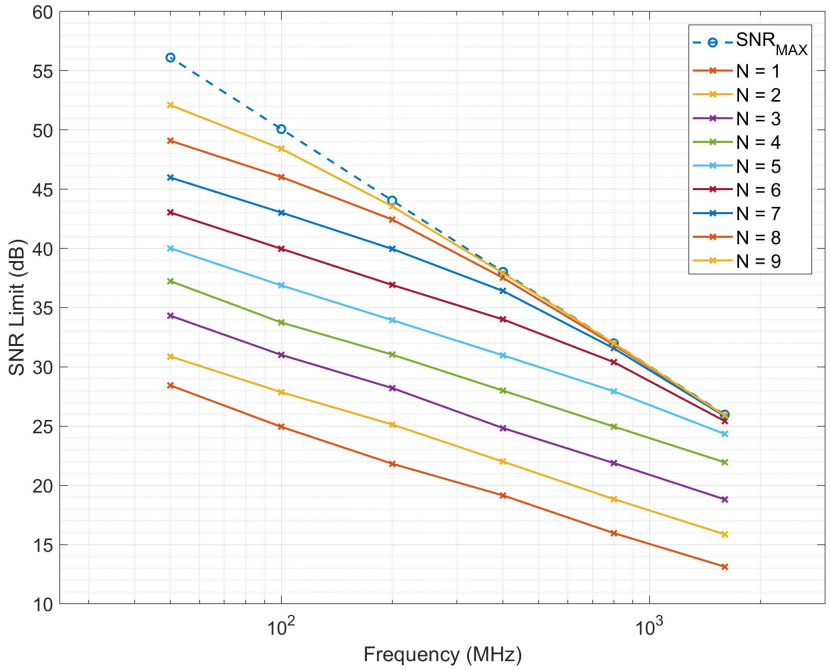


Figure 3-3: SNR limitation for a level-crossing-based CT pipeline ADC for different sub-ADC resolutions.

the sub-ADC of the CT pipeline, the jitter error magnitude will decrease, while its frequency of occurrence will increase. For infinite threshold levels, the stage-1 digital output will become identical to the ADC input. If the RMS jitter is assumed to be the same in both cases, then the SNR limitation for the level-crossing-based CT pipeline will be identical to upfront sampling ADCs. Figure 3-3 shows the simulated SNR for level-crossing-based CT pipeline ADC with varying resolution and compares it to the upfront sampling SNR limit (RMS jitter of 5 ps has been assumed for this simulation). As expected, for higher sub-ADC resolutions ($>$ 6-7 bits), the SNR limit for the level-crossing-based CT pipeline ADC approaches that of an upfront sampled ADC.

In conclusion, although a level-crossing-based sub-ADC-DAC path may seem a good choice because it fundamentally eliminates the clock and thereby the limitations of the aperture error, in practice, however, the need for a discrete-time DSP necessitates re-timing of the non-uniformly sampled stage-1 sub-ADC continuous-time output, resulting in a far worse SNR degradation caused by the jitter in the re-timing

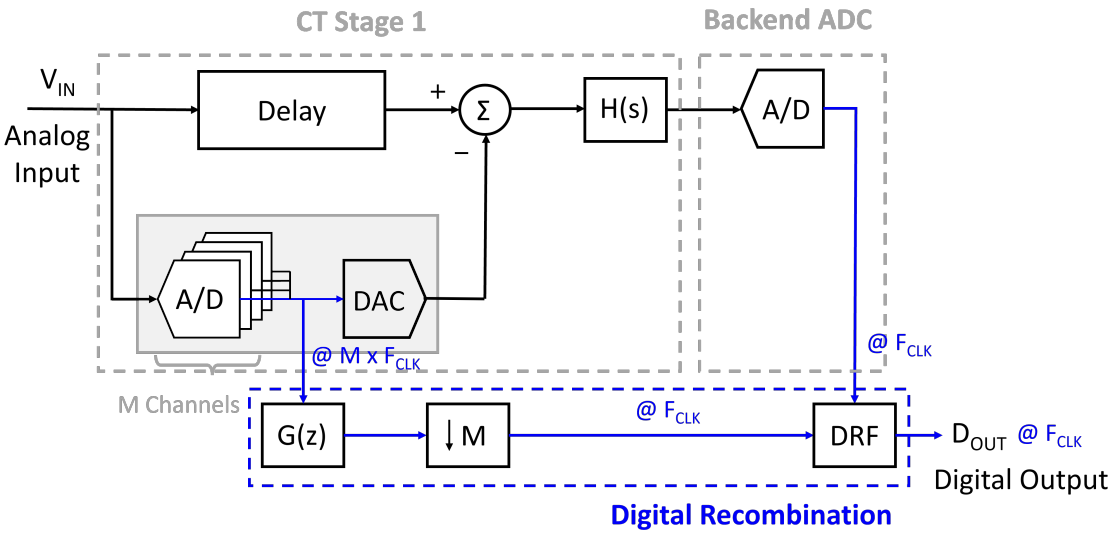


Figure 3-4: A simplified block diagram for a 2-stage CT pipeline ADC with M-way interleaved sub-ADC-DAC path. The wires corresponding to digital signals are shown in blue. The sub-ADC output rate is $M \cdot F_{CLK}$, the sub-DAC operates at $M \cdot F_{CLK}$, and the backend operates at F_{CLK}. The digital output is received at F_{CLK}.

clock. In the following subsection, we present a technique to achieve a smaller DAC step size leveraging the benefits of an NRZ-DAC, while maintaining discrete-time operation for the DSP.

3.1.2 CT Pipeline ADC with Interleaved sub-ADC-DAC Path

As described in previous sections, the SNR of the CT pipeline ADC may be limited by the sub-DAC jitter for high bandwidth applications. To reduce the impact of clock jitter on the ADC performance, we propose time-interleaving the stage-1 sub-ADC-DAC path. The motivation behind doing this is to increase the effective sampling rate in the sub-DAC so that the DAC step size is closer to 1 LSB. From a jitter sensitivity standpoint, for a given sub-ADC-DAC resolution, the best-case scenario is to sample fast enough such that every DAC step equals 1 LSB. Conceptually, it approximates a level-crossing-based sub-ADC-DAC path while maintaining an overall clocked system. A simplified block diagram with a time-interleaved sub-ADC-DAC path in stage 1 is shown in Figure 3-4. Since stage 1 and stage 2 operate at different rates, it is not immediately obvious why this ADC should give a correct digital output. The system

operation can be understood as follows:

First, let us take a step back and look at a conventional 2-stage CT pipeline ADC as shown in Figure 3-5. Stage 1 and stage 2 both operate at sampling rate f_S. A digital filter $H_1(z)$ is applied to the stage-1 digital output ($d_1[n] \overset{\mathcal{F}}{\longleftrightarrow} D_1(Z)$). The filtered digital sequence is then summed with the backend digital output ($d_2[n] \overset{\mathcal{F}}{\longleftrightarrow} D_2(Z)$) to give the ADC output:

$$d_{OUT}[n] = d_1[n] * h_1[n] + d_2[n] \tag{3.1}$$

where $h_1[n]$ is the impulse response of the digital filter applied to $d_1[n]$. Ideally, the filter $H_1(z)$ must replicate whatever processing d_1 goes through in the entire pipeline: sub-DAC, interstage amplifier (provides gain and low-pass filtering), and the backend ADC (sampler followed by quantizer). Then, the addition of $d_1[n] * h_1[n]$ to $d_2[n]$ will cancel the stage 1 errors, and d_{OUT} will only contain the errors from the backend ADC (suppressed by the interstage gain). Conceptually, a (digital) impulse can be applied at the sub-DAC output to estimate $h_1[n]$.

Now, keeping everything the same as in Figure 3-5, we increase the sampling rate in the sub-ADC-DAC path by a factor of 2. The modified block diagram for this system is shown in Figure 3-6. We postulate that for an appropriately chosen filter $H_1(z)$, the stage-1 digital sequence can be decimated by a factor of 2, and then added to the stage-2 digital output (data rate = f_S) to get the ADC output without any significant degradation in the signal-to-noise ratio. Since the interstage amplifier has a low-pass characteristic, $H_1(z)$ is also low-pass shaped. Decimation can cause out-of-band noise to alias into the signal band and degrade the SNR. However, if $H_1(z)$ has a sharp roll-off, then it attenuates the out-of-band noise significantly. At this point, the stage-1 digital signal can be decimated without incurring a noise penalty due to decimation. Therefore, it is possible for stage 1 to operate at a higher sampling rate while maintaining overall ADC performance.

The stage-1 digital filter $H_1(z)$ can be decomposed into polyphase components as shown in Figure 3-7 [13]. If the stage-1 operates at $M \cdot f_S$, then each phase output

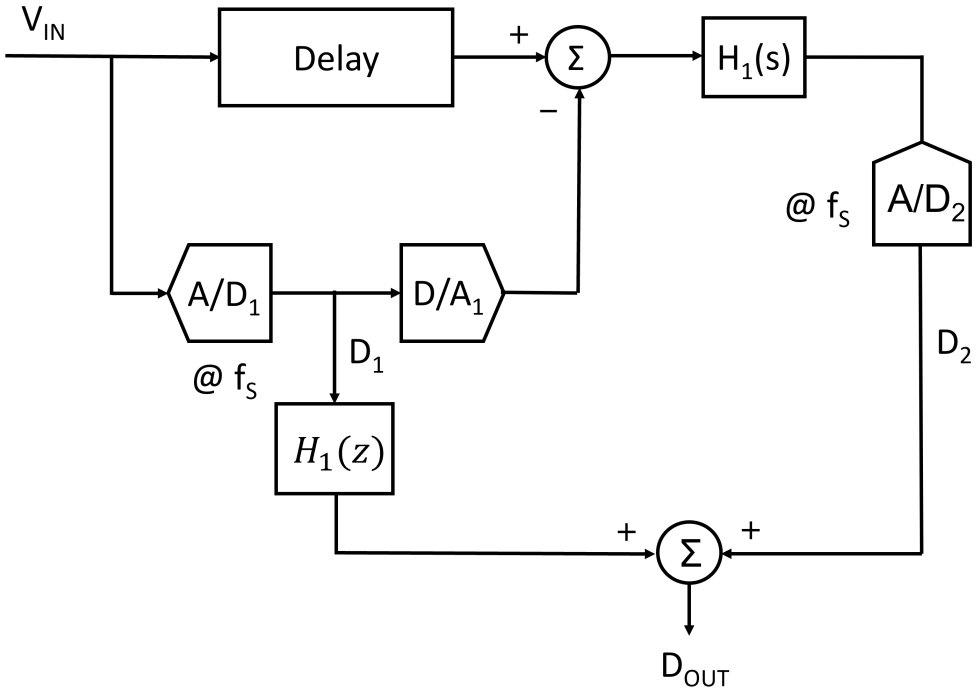


Figure 3-5: A 2-stage CT pipeline ADC where stage 1 and stage 2 operate at sampling rate f_S.

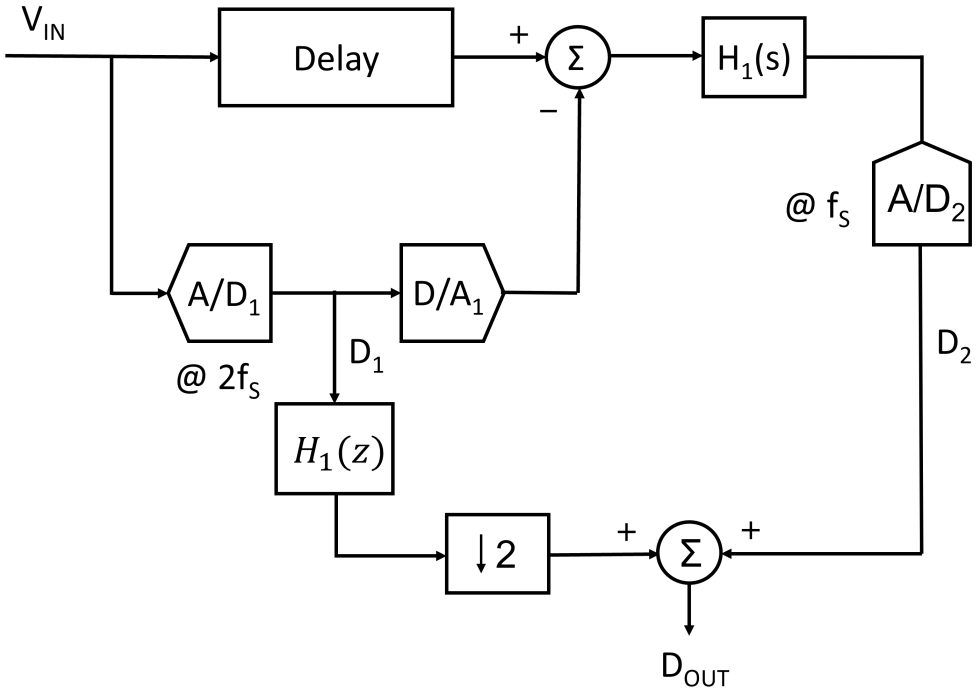


Figure 3-6: A 2-stage CT pipeline ADC where stage 1 operates at $2f_S$ and stage 2 operates at f_S.

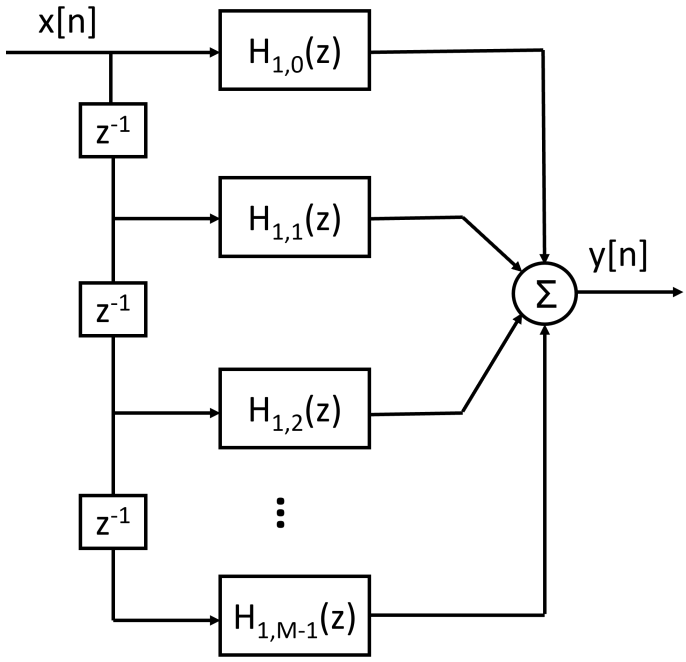


Figure 3-7: Stage-1 digital filter $H_1(z)$ can be decomposed into polyphase components [13].

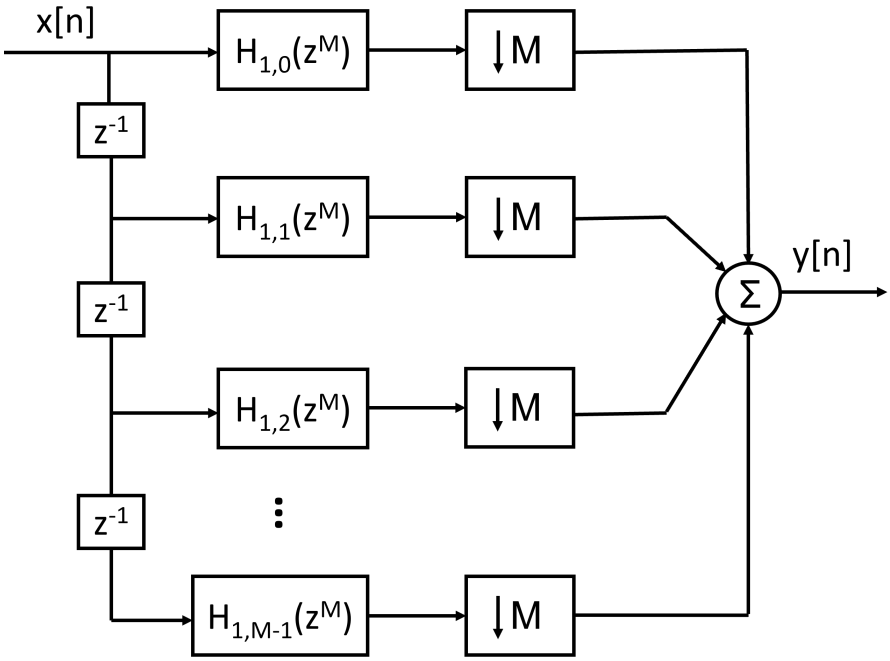


Figure 3-8: Implementation of $H_1(z)$ and decimation by a factor of M using polyphase decomposition [13].

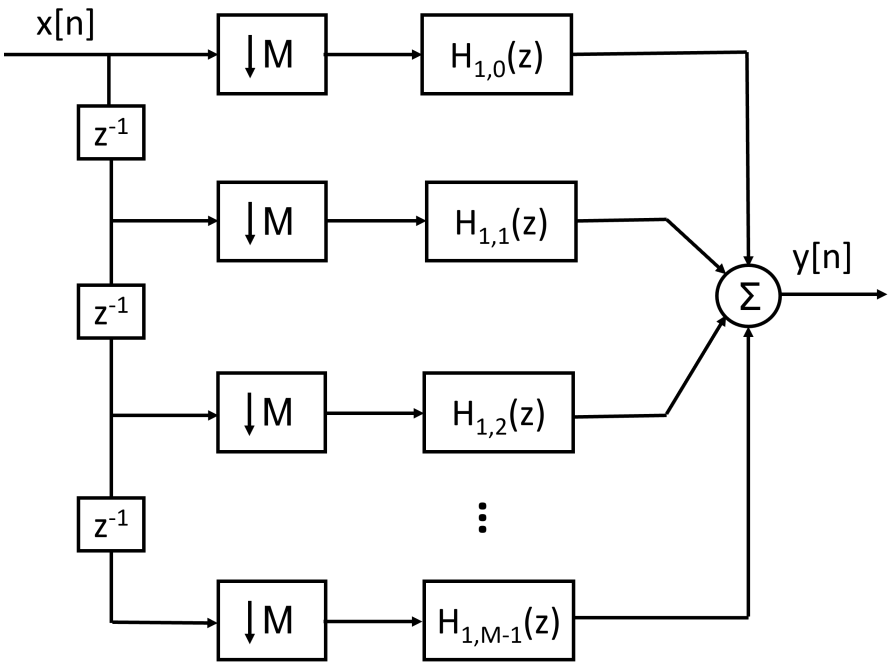


Figure 3-9: A block diagram showing the stage-1 digital filter implementation by swapping the decimate by M and $E_i(z)$ blocks using the downsampling identity [13].

can be decimated by a factor of M to get the filtered stage-1 output (Figure 3-8). Finally, the decimation operation can be swapped with the individual polyphase components (denoted as $H_{1,0}(z^M)$, $H_{1,1}(z^M)$, ..., $H_{1,(M-1)}(z^M)$ in Figure 3-8) using the downsampling property. Figure 3-9 shows one such implementation. This results in an interesting filter configuration where each phase processing starts with a decimator. Instead of operating the stage-1 sub-ADC at $M \cdot f_S$, multiple channels can be M-way interleaved, with each channel operating at f_S. The clocks for the M-way interleaved sub-ADC must have a relative phase shift of $2\pi/M$. Then, each of the sub-ADC/decimator/filter slices can be separated, and the filter coefficients for $h_{1,0}[n]$, $h_{1,1}[n]$, ..., $h_{1,(M-1)}[n]$ can be computed independently. The resulting stage-1 configuration is shown in Figure 3-10.

For the test chip, we implemented a two stage CT pipeline ADC with 2-way time-interleaved sub-ADC-DAC path as shown in Figure 3-11. The interleaved channels are clocked by two clocks which are 180° out-of-phase. The sub-DAC full-scale for each channel is ± 625 μA. The two channel sub-DAC outputs are summed at the

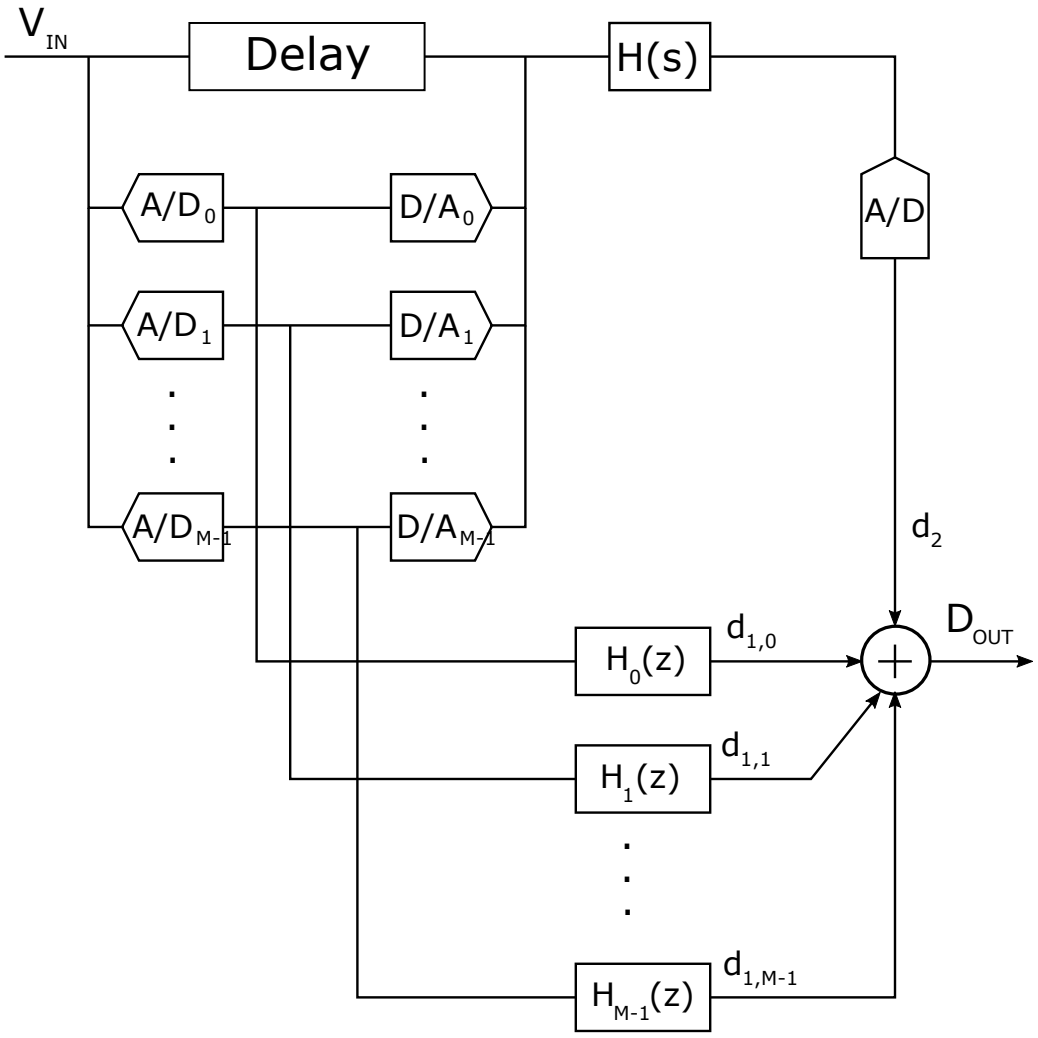


Figure 3-10: Block diagram for a 2-stage CT pipeline ADC with M-way interleaved sub-ADC-DAC path. The stage-1 digital reconstruction filter is implemented using M-way polyphase decomposition.

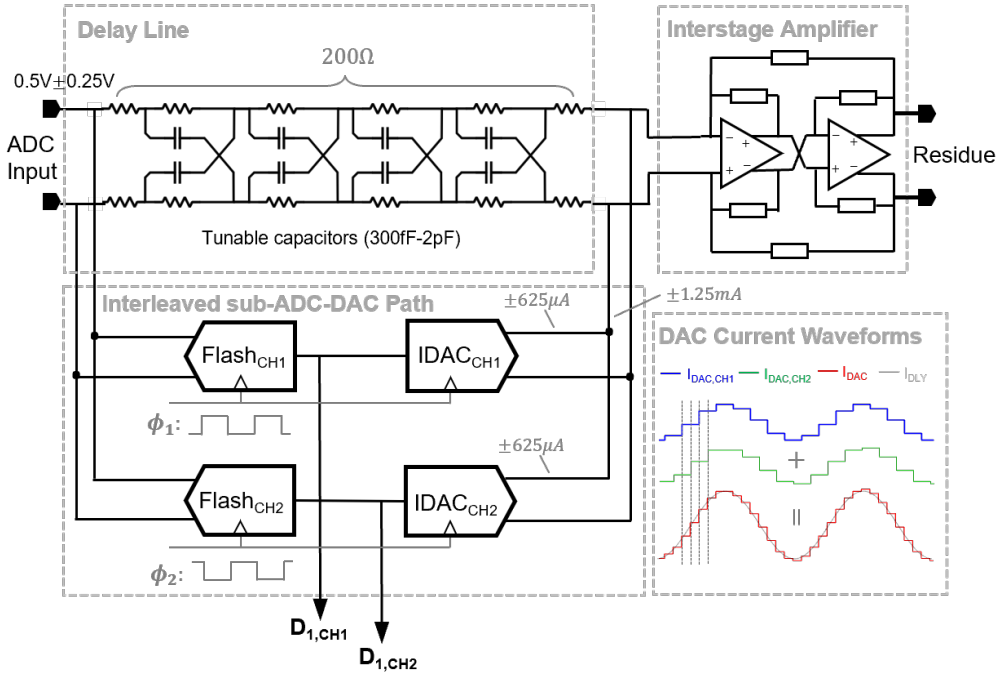


Figure 3-11: A schematic of the CT first stage of the proposed ADC. The sub-ADC-DAC path is 2x-interleaved to achieve a higher effective sampling rate at the DAC output.

stage 1 summing node to give the net DAC output:

$$I_{DAC}(t) = I_{DAC_{CH1}}(t) + I_{DAC_{CH2}}(t) \tag{3.2}$$

where $I_{DAC_{CH1}}(t)$ and $I_{DAC_{CH2}}(t)$ are the channel 1 and channel 2 sub-DAC outputs. The full-scale for the net DAC output is ±1.25 mA. The series resistors in the delay line are chosen such that the full-scale of the delayed input current matches the full-scale of the sub-DAC current. The sub-ADC and sub-DAC in each channel is clocked at 6.4 GHz. Because of interleaving, the effective sampling rate in the stage 1 sub-ADC-DAC path becomes 12.8 GHz.

The impact of DAC jitter can be understood in two ways: (1) since the jitter in channel 1 and channel 2 are uncorrelated, the net jitter-induced noise power at the sub-DAC output increases by a factor of 2 (w.r.t. a CT pipeline ADC with a single sub-ADC-DAC path, assuming that the DAC full-scale is 625 μA). However, the signal amplitude at the sub-DAC output also increases by a factor of 2. The signal

power increases by a factor of 4. Hence, the overall SNR improves by a factor of 2, or equivalently 3 dB, and (2) alternatively, we can make the assumption of same signal power, i.e. the proposed architecture can be compared with a CT pipeline ADC with without any interleaving in the sub-ADC-DAC path, and assuming that the net DAC full-scale current is the same in both cases (say for instance 625 μA). With this set of assumptions, we can use Equation 2.45 to derive the SNR improvement. For a 2-way interleaved sub-ADC-DAC path, the OSR increases by a factor of 2, resulting in an in-band noise reduction by a factor of 2. This means that the SNR improves by 2x, or equivalently 3 dB.

To summarize, the analysis presented in this section shows that it is possible to operate the stage-1 sub-ADC-DAC path at a higher effective sampling rate. By choosing appropriate digital filters, it is possible to maintain the functionality and performance of the overall ADC. In a CT pipeline ADC, running the sub-ADC at a higher sampling rate offers the following benefits: (1) a smaller DAC step-size is achieved, which reduces the impact of clock jitter, (2) owing to the continuous-time operating of the first stage, the residue can get large if the sub-ADC-DAC path is not clocked fast enough. Time-interleaving the sub-ADC-DAC helps in reducing the residue amplitude. This allows for a high interstage gain resulting in higher backend noise suppression, (3) typically, CT pipeline ADCs can only handle a small-amplitude interferer near f_S because a large interferer can saturate the backend ADC. With an interleaved sub-ADC-DAC path, the ADC can handle a large interferer near f_S because it falls in the Nyquist band for the sub-ADC-DAC path and gets canceled at the stage-1 summing node.

3.2 Delay Line

The stage-1 delay line is a critical block in the CT pipeline ADC because it impacts the residue amplitude. The delay line must be carefully designed to minimize signal leakage [8] (defined later in Equation 3.4). In the past, several delay line designs have been implemented, such as RC-lattice based [3], LC-lattice based [4] and RLC-

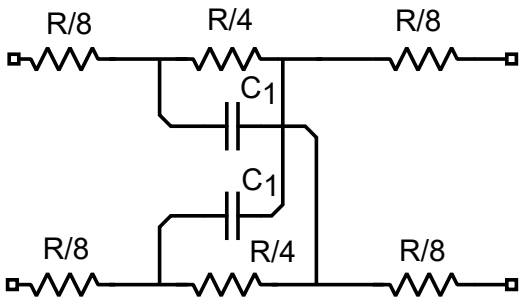


Figure 3-12: A RC-lattice-based delay line having an all-pass response.

lattice based [9]. The basic idea behind any delay line design is to provide a good timing match between the signal path and the sub-ADC-DAC path while minimizing the signal leakage in the residue. To achieve a good signal rejection, the delay line phase must remain linear (or close to linear) over the entire ADC bandwidth. This can be achieved by using inductor-based lattice structures. However, using inductors for on-chip applications is not desired because (1) they occupy a large area, and (2) in complex integrated designs, the inductors can couple with nearby circuitry and induce noise in the signal path of the CT pipeline ADC. This could potentially degrade the ADC performance. In the past, inductor-less delay lines have also been implemented [3–5, 32]. The phase of an RC-lattice-based delay line is given by:

$$\phi_{RC} = -2\tan^{-1}\left(\frac{\omega RC_1}{4}\right) \tag{3.3}$$

where R is the (differential) series resistance and C_1 is the cross-connected capacitance (see Figure 3-12). At higher frequencies, the phase begins to get non-linear. The phase difference between an ideal delay line (linear phase for all frequencies) and an RC-lattice-based delay line is 10% when $\omega RC = 0.55$. This means that to achieve a better phase matching over a larger bandwidth, either R or C must be decreased. The value of the series resistance is often set by the sub-DAC full-scale current. Therefore, the only option to get a better phase matching over a larger bandwidth is to reduce the capacitor value. Unfortunately, reducing the capacitor value (while keeping the resistor value the same) changes the group delay of the signal path, resulting in a significant signal leakage.

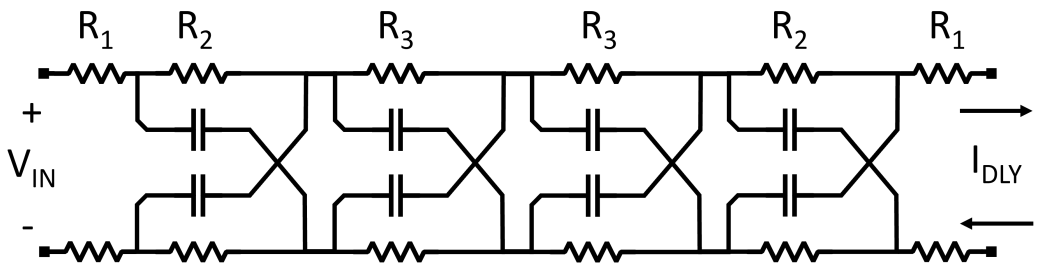


Figure 3-13: The proposed 4x-cascaded RC lattice-based delay line. $2(R_1+R_2+R_3) = V_{FS}/I_{FS,DAC} = 400\Omega$. All capacitors in the delay line are tunable.

We propose cascading multiple RC lattice sections to build the signal path delay line. The net series resistance is set by the input voltage full-scale and the sub-DAC full-scale current: $R_S = V_{FS}/I_{FS,DAC}$. The capacitor value for each lattice section is reduced such that each section has a linear phase across the desired ADC bandwidth. Then, multiple sections are cascaded to compensate for the reduced group delay because of choosing a smaller capacitor. The proposed 4x-cascaded delay line is shown in Figure 3-13.

The resistors and capacitors values must be chosen carefully to minimize signal leakage. The next subsection describes the design methodology for the delay line.

3.2.1 Design Methodology for Delay Line

The goal of the delay line is to match the signal path delay with the sub-ADC-DAC path delay. The residue transfer function (assuming no quantization noise in stage 1) is a proxy for the signal leakage and is given by:

$$V_{RES}(s) = (G_{DLY}(s) - F(s)D(s)) \cdot H(s) \tag{3.4}$$

where $G_{DLY}(s)$, $F(s)$, $D(s)$, and $H(s)$ are the delay line, sub-ADC (Flash), sub-DAC and interstage amplifier transfer functions respectively.

Assuming one clock cycle delay from the sub-ADC input to the output (T_{CK}) and half clock cycle delay in the DAC impulse response ($T_{CK}/2$), the net delay in the sub-ADC-DAC path is 1.5 T_{CK}. The phase response for the sub-ADC-DAC is linear

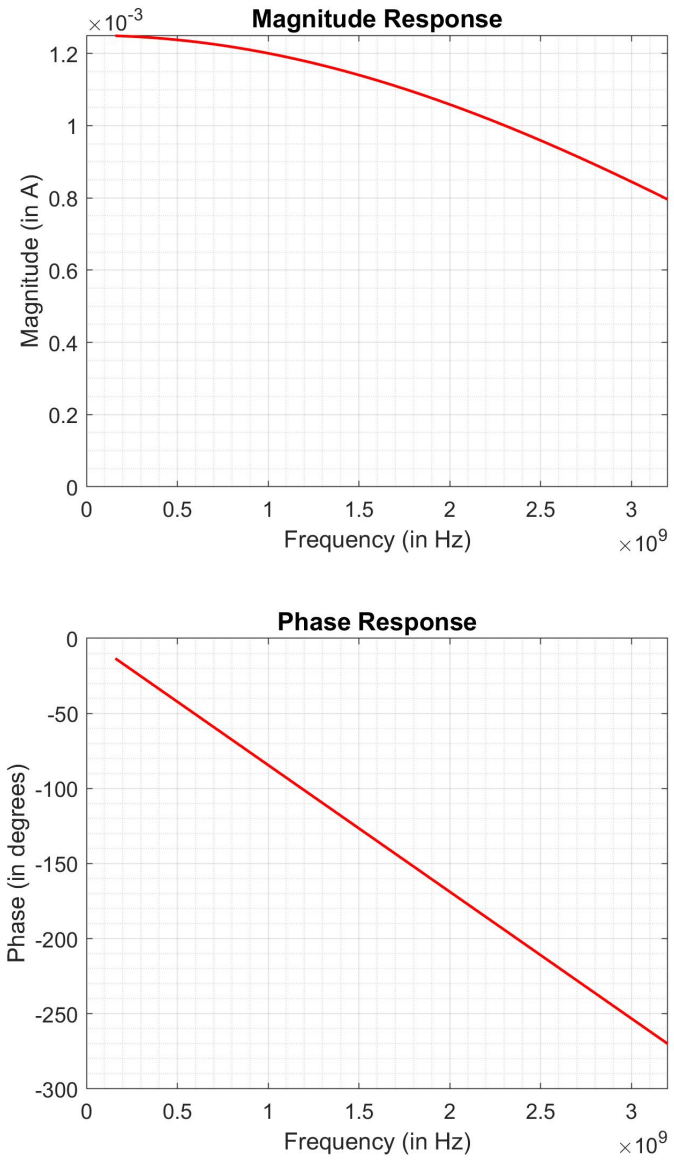


Figure 3-14: Magnitude and phase response for the sub-ADC-DAC path in the first stage of a CT pipelined ADC ($f_S = 6.4$ GHz, sub-ADC-DAC path delay = 234 ps.).

with a slope corresponding to a delay of 1.5 T_{CK}. Also, assuming a flat frequency response for the sub-ADC, the overall sub-ADC-DAC path's magnitude response is a sinc function (null at f_S)[2]. The typical magnitude and phase response for the sub-ADC-DAC path are shown in Fig. 3-14.

An ideal transfer function for the delay line could be achieved by using a transmis-

[2]If the sub-ADC has a buffer, its response can be captured in $F(s)$ without any loss of generality.

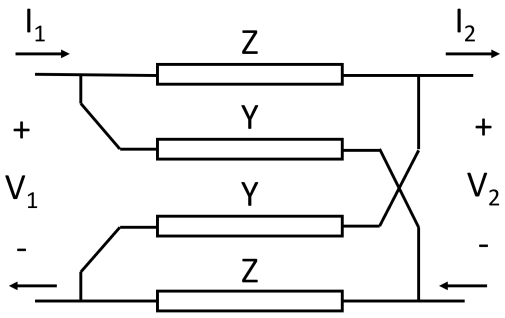


Figure 3-15: A 2-port lattice structure with series impedance Z and cross-connected shunt admittance Y.

sion line. For a 6.4 GHz sampling rate CT pipelined ADC, the delay required in the signal path is about 234 ps. The length of the transmission line needed to implement this delay is given by:

$$L = \frac{c \cdot T_{DLY}}{\sqrt{\epsilon_{SiO_2}}} \tag{3.5}$$

$$= \frac{(3 \cdot 10^8)\ \text{m/s} \cdot (234 \cdot 10^{-12})\ \text{s}}{\sqrt{3.9}} = 35\ \text{mm} \tag{3.6}$$

where c is the speed of light, T_{DLY} is the delay in the signal path, and ϵ_{SiO_2} is the relative permittivity of silicon dioxide. Based on this calculation, it is clear that using a transmission line for the signal path delay requires a very large length.

To implement an on-chip delay line with a reasonable area, lattice structures using passive components such as resistors, capacitors, and inductors can be used. A general lattice structure is shown in Figure 3-15. The transfer function for a lattice-based delay can be obtained by using the 2-port ABCD parameters as defined below:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \tag{3.7}$$

where V_i and I_i are the voltages and currents at the i-th port. Assuming the delay line output is loaded with Z_L:

$$Z_L = V_2/I_2 \tag{3.8}$$

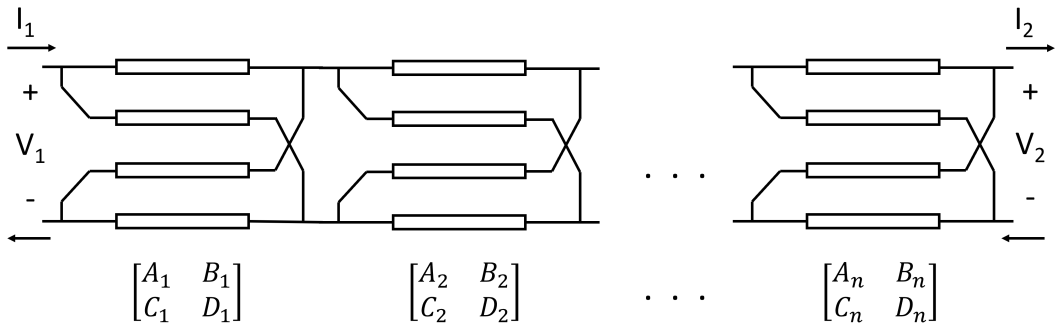


Figure 3-16: A generalized 2-port cascaded lattice structure.

The delay line output current and transfer function G_{dly} can be found as follows:

$$V_1 = A(Z_L I_2) + BI_2 \tag{3.9}$$

$$I_2 = \frac{V_1}{B + AZ_L} \tag{3.10}$$

$$G_{dly} = \frac{I_2}{V_1} = \frac{1}{B + AZ_L} \tag{3.11}$$

For a CT pipeline ADC, the delay line is loaded by the sub-DAC (Z_{dac}) in parallel with the interstage amplifier (Z_{amp}). Since the input impedance of the interstage amplifier (a transimpedance amplifier) is very small, $Z_L \approx Z_{amp} \to 0$. Therefore, the delay line transfer function can be approximated as:

$$G_{dly} = \frac{1}{B} \tag{3.12}$$

As an example, the parameter B for the general lattice structure shown in Figure 3-15 is given by:

$$B = \left.\frac{V_1}{I_2}\right|_{V_2=0} = \frac{2Z}{1 - YZ} \tag{3.13}$$

where Z and Y are the impedance and admittance of the series and shunt elements. To obtain good phase matching between the delay and the sub-ADC-DAC path, a single lattice structure is usually not sufficient. A more complex delay line can be designed by cascading several lattice structures to get the desired transfer function

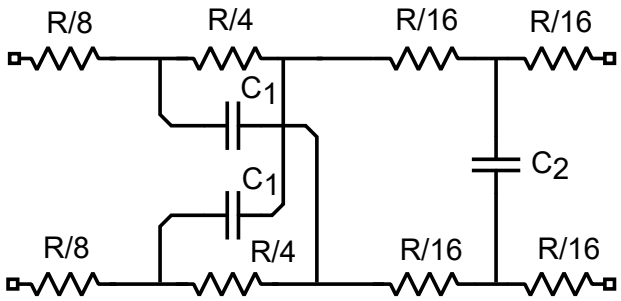


Figure 3-17: A RC-lattice delay line structure with a low-pass response to match the sinc magnitude response in the sub-ADC-DAC path.

as shown in Figure 3-16. The delay line transfer function can be evaluated by finding the ABCD parameters for the cascaded network as follows:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \cdots \begin{bmatrix} A_N & B_N \\ C_N & D_N \end{bmatrix} \tag{3.14}$$

where A_i, B_i, C_i, and D_i are the ABCD parameters for the i-th structure in the cascaded network. The delay line transfer function can then be evaluated from Eq. 3.12.

With the above-mentioned framework, we compared the signal transfer function for a conventional RC-lattice-based delay line (Figure 3-17) with the proposed 4x-cascaded RC-lattice delay line (Figure 3-13). In the single RC-lattice-based delay line, the ratio of the series resistors is set to 1:2:1 to get an all-pass response. The R/8 resistor on the right is split into two R/16 resistors with a shunt capacitor to provide a low-pass magnitude response. This is done to match the delay line magnitude response to the sinc response of the sub-DAC. The values for the resistors and capacitors in both topologies were chosen such that the signal leakage is minimized across the ADC bandwidth (set as 1600 MHz in the comparison). Figure 3-18 shows the magnitude and phase response of the 2 delay lines and compares it against the sub-ADC-DAC response. The 4x-cascaded RC lattice provides a better magnitude and phase matching compared to a simple RC lattice-based delay line. Figure 3-19 compares the signal transfer function $H(s) \cdot \big(G_{DLY}(s) - F(s)D(s)\big)$ for the 2 delay line topologies. For the single RC-lattice-based delay line, the signal leakage can be as high as 0.62 of the full scale. We target the signal leakage to be less than 30%

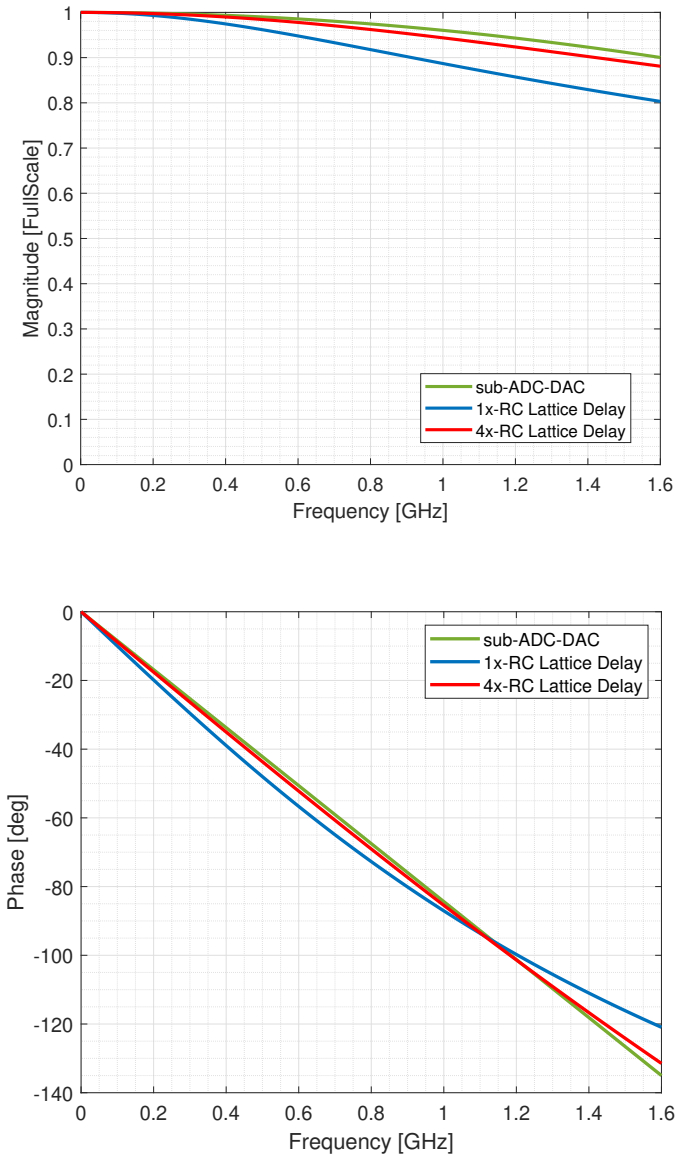


Figure 3-18: Magnitude and phase response for 1x- and 4x-RC lattice delay lines.

of the full scale of the subsequent ADC to allow room for other errors such as the sub-ADC quantization noise and comparator offsets. For the case of a 4x-cascaded RC lattice delay line, the signal leakage is limited to just 0.16 of the full scale. This means that the signal leakage is reduced by a factor of 3.9, or equivalently 11.7 dB (at the frequencies with the highest signal leakage). The following conclusions can be drawn from this comparison: (1) using a 4x-cascaded RC lattice delay line can enable bandwidth extension in CT pipeline ADCs by minimizing the signal leakage

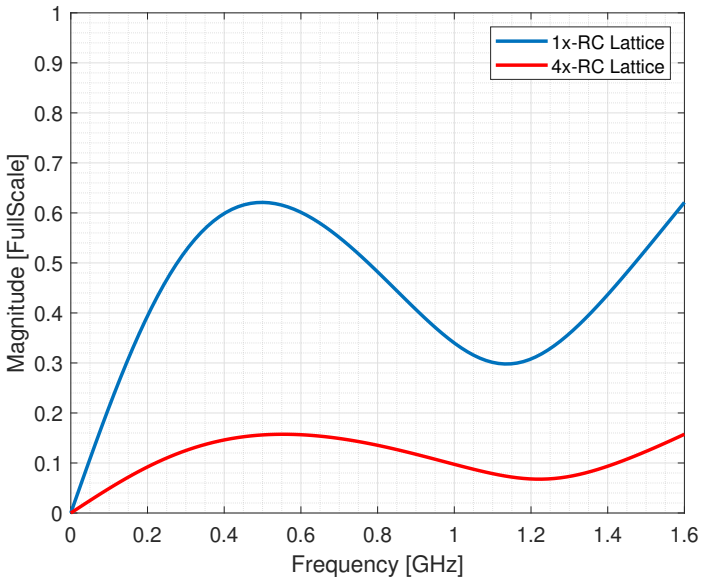


Figure 3-19: Signal transfer function (from the ADC input to the interstage amplifier output) for the 1x- and 4x-RC lattice delay lines.

without using inductors, thereby saving area as well as avoiding inductive coupling in the signal path, and (2) the interstage gain can be increased by approximately a factor of 2 (assuming that the signal leakage is no more than 30% of the full-scale of the stage-2 ADC). This helps in suppressing the backend ADC noise.

3.2.2 Group Delay and Phase Delay

For a CT pipeline ADC, it is important to match both the phase delay (ϕ/ω) and the group delay ($d\phi/d\omega$) for the signal path and the sub-ADC-DAC path. The reason for this is as follows: assume an amplitude-modulated signal $V_{in} = a(t)\sin(\omega t + \phi)$ where $a(t)$ is a slowly varying signal, setting the envelope for the sinusoidal signal. In a CT pipeline ADC, the goal is to match the *delay* of the signal path and the sub-ADC-DAC path sufficiently well across the ADC bandwidth such that the residue does not become too large. Two scenarios of delay mismatch are possible: (1) group delay mismatch: this can be detrimental because there will be a misalignment of the envelope from the signal path and the sub-ADC-DAC path resulting in a large residue signal overloading the backend ADC, and (2) phase delay mismatch: assuming that

the group delay is matched perfectly, phase delay mismatch will also increase the residue signal, in a time-variant manner, based on the envelope $a(t)$. Intuitively, this effect will be less detrimental because the envelope from the signal and sub-ADC-DAC path are aligned. Nonetheless, this will require further analysis and/or simulation for definite proof.

This means that neither the group delay matching nor the phase delay matching by itself will be sufficient to ensure a good signal cancellation in stage 1 of a CT pipeline ADC. Therefore, to have a conservative delay line design, we can impose the constraint that the group delay must be equal to the sub-ADC-DAC path delay, and simultaneously, the phase delay must also be equal to the sub-ADC-DAC delay (over the entire ADC bandwidth). This constraint can be fulfilled by designing a linear phase response for the delay line across the ADC bandwidth (with the assumption that the magnitude response in the signal path and the sub-ADC-DAC path is accurately matched). The proposed delay line meets this condition by design.

3.2.3 Matching Signal Path and sub-ADC-DAC Path Delay

In a CT pipeline ADC with time-interleaved sub-ADC-DAC, the delay line must be designed such that it accurately matches the delay of the sub-ADC-DAC path. In this section, we present an analysis for the delay in the sub-ADC-DAC path and use that to estimate the nominal delay required in the signal path.

Let the ADC input be $x(t) = A\sin(2\pi f_{in}t)$. Assuming no quantization error for simplicity, the sub-ADC output for channel 1 and channel 2 is given by:

$$x_1[n] = A\sin(2\pi f_{in}nT) \tag{3.15}$$

$$x_2[n] = A\sin\left(2\pi f_{in}\left(n+\frac{1}{2}\right)T\right) \tag{3.16}$$

where $x_1[n]$ and $x_2[n]$ are the channel 1 and channel 2 sub-ADC outputs respectively. To get the channel 1 sub-DAC output, we can multiply $x_1[n]$ with an impulse train (time period = T_{CK}) and then convolve the resulting signal with the DAC impulse response $p(t) = u(t) - u(t - T_{CK})$ (where $u(t)$ is the unit-step function) for an NRZ-

DAC response. The channel 1 sub-DAC output $y_1(t)$ can be calculated as shown below:

$$x_1(t) = \sum_n A \sin(2\pi f_{in} nT) \cdot \delta(t - nT) \tag{3.17}$$

$$p_1(t) = u(t - T) - u(t) \tag{3.18}$$

$$y_1(t) = x_1(t) * p_1(t) \tag{3.19}$$

The Fourier transform of $y_1(t)$ is given by:

$$Y_1(j\omega) = X_1(j\omega) \cdot P_1(j\omega) \tag{3.20}$$

$$= \left[\sum_n \frac{A}{2}\delta(\omega - n\omega_{in})\right] \cdot \left[\frac{\sin(\omega T/2)}{\omega T/2} e^{-j\omega T/2}\right] \tag{3.21}$$

Since the DAC output is low-pass filtered, we can ignore the higher-order harmonics for further analysis. The fundamental tone in the sub-DAC output is given by:

$$Y_1(j\omega) = \frac{A}{2}\frac{\sin(\omega T/2)}{\omega T/2} e^{-j\omega T/2} \tag{3.22}$$

Equation 3.22 suggests that the channel delay is $T_{CK}/2$ if we assume no delay in the sub-ADC. Typically, the sub-ADC output is delayed by one clock cycle. Hence, the overall channel-1 delay is $1.5T_{CK}$.

A similar calculation can be performed for channel-2 sub-DAC. The difference is that channel 2 sees an input that is half-clock cycle delayed. The channel 2 sub-DAC output $y_2(t)$ can be calculated as shown:

$$x_2(t) = \sum_n A \sin\left(2\pi f_{in}\left(n + \frac{1}{2}\right)T\right) \cdot \delta\left(t - \left(n + \frac{1}{2}\right)T\right) \tag{3.23}$$

$$p_2(t) = u(t - T) - u(t) \tag{3.24}$$

$$y_2(t) = x_2(t) * p_2(t) \tag{3.25}$$

The Fourier transform of $y_2(t)$ is given by:

$$Y_2(j\omega) = X_2(j\omega) \cdot P_2(j\omega) \tag{3.26}$$

$$= \left[\sum_n \frac{A}{2}\delta(\omega - n\omega_{in})e^{-j\omega T/2}\right] \cdot \left[\frac{\sin(\omega T/2)}{\omega T/2}e^{-j\omega T/2}\right] \tag{3.27}$$

Considering the fundamental tone, as we did in the analysis for channel 1 sub-DAC output, we get:

$$Y_2(j\omega) = \frac{A}{2}\frac{\sin(\omega T/2)}{\omega T/2}e^{-j\omega T} \tag{3.28}$$

From equation 3.28, the channel 2 sub-DAC delay is T_{CK}. Hence, the total channel 2 delay including the sub-ADC delay is $2T_{CK}$. The combined DAC output $y(t)$ is given by:

$$y(t) = y_1(t) + y_2(t) \tag{3.29}$$

$$= \frac{A}{2}\frac{\sin(\omega T/2)}{\omega T/2}\left(e^{-j\omega T/2} + e^{-j\omega T}\right)$$

$$= \frac{A}{2}\frac{\sin(\omega T/2)}{\omega T/2}\cos(\omega T/4)\ e^{-j\omega 3T/4} \tag{3.30}$$

From the above equation, it can be deduced that the overall delay for the proposed 2-way interleaved sub-ADC-DAC path is $T_{CK} + \frac{3T_{CK}}{4} = 1.75\ T_{CK}$. The delay line must be designed such that the signal path delay equals $1.75\ T_{CK}$ in the nominal case.

3.3 Circuit Implementation

The stage 1 sub-ADC was implemented as a 17-level fully differential Flash ADC. Figure 3-20 shows a simplified single-ended schematic of the Flash ADC. The digital output $< b_{15} : b_0 >$ is thermometric coded and is stored in the on-chip RAM as such. The thermometric data is converted to decimal format during the off-chip processing at the time of digital reconstruction. The nominal operation frequency for the Flash ADC is 6.4 GHz. However, we parallelize the data to 1.6 GHz before routing to the

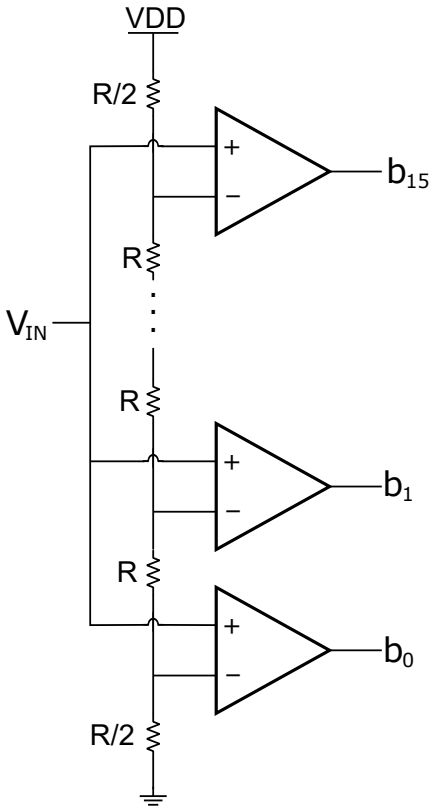


Figure 3-20: A simplified single-ended schematic of the 17-level Flash ADC.

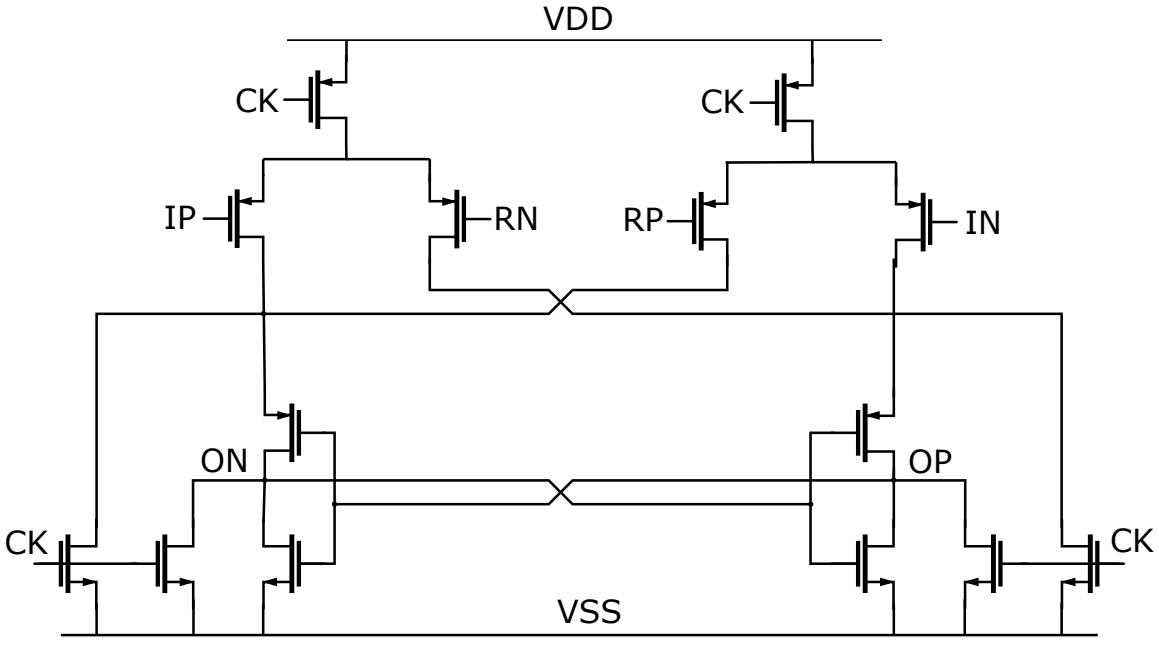


Figure 3-21: A schematic of the fully differential comparator used in the stage 1 Flash ADC.

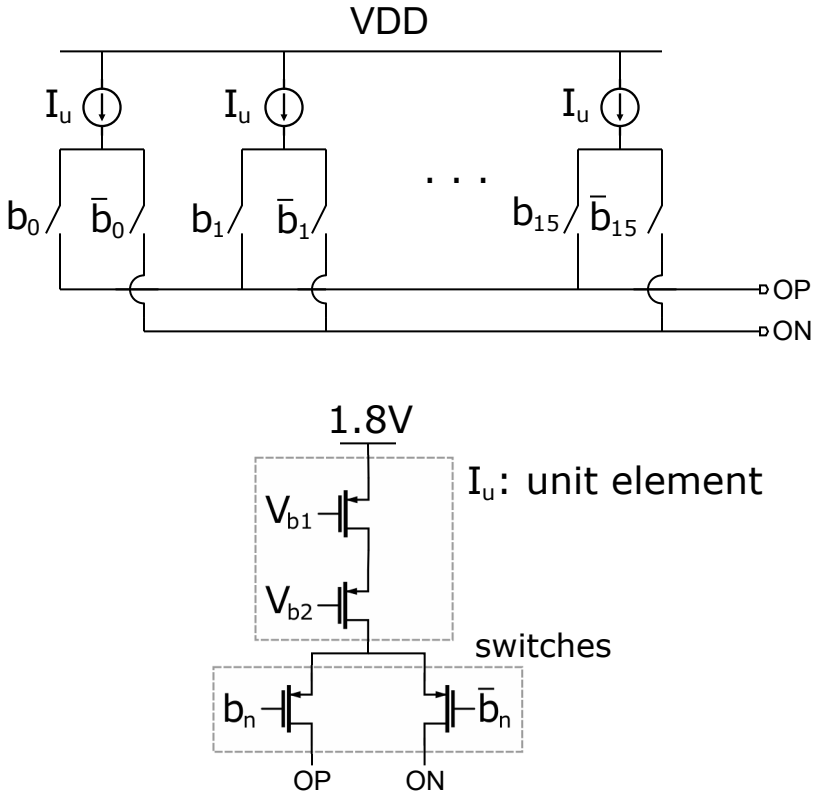


Figure 3-22: Top: A schematic of the current steering sub-DAC; Bottom: the unit elements and switches. OP and ON are connected to the negative summing node SN and the positive summing node SP respectively.

on-chip RAM to preserve signal integrity and ease the design of the routing path (described further in section 3.4). The comparator schematic is shown in Figure 3-21.

The sub-DAC was implemented as a current-steering DAC as shown in Figure 3-22. The current source is cascoded to increase the output resistance and reduce signal-dependent activity on the source node of the switches during bit transition. A 1.8 V supply is used to provide sufficient voltage headroom for the cascoded current source and the DAC switches. The common mode voltage for the output node (this is also the stage 1 summing node) is 0.5 V (this is maintained using a separate feedback loop. A dedicated 0.5 V reference voltage is used for this purpose). Additionally, an NMOS current sink has been used to prevent any common-mode current from going to the summing node. Each unit current source is biased to provide 78 μA current, meaning that the DAC current varies from 0 to 1250 μA nominally. The NMOS current sinks 625 μA. A negative feedback loop is used to control the gate

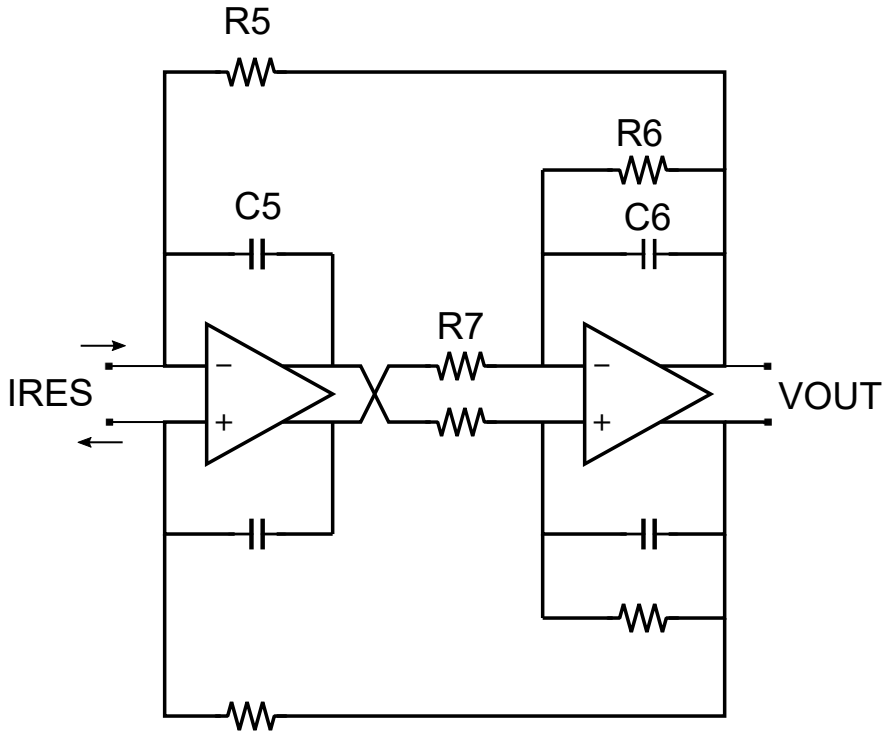


Figure 3-23: A schematic of the interstage amplifier. The values for all resistors and capacitors are listed in Table 3.1.

voltage of the NMOS transistors in the current sink which ensure that the DAC output common-mode voltage is maintained at 0.5 V.

The schematic for the interstage amplifier is shown in Figure 3-23. The transfer function is given by:

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_5}{R_{dly}} \cdot \frac{1}{1 + \left(\frac{R_5 R_7 C_5}{R_6}\right) s + (R_5 R_7 C_5 C_6) s^2} \tag{3.31}$$

where V_{OUT} is the interstage amplifier output voltage, V_{IN} is the ADC input voltage, R_{dly} is the single-ended series resistance of the delay line (200 Ω), and R_5, R_6, R_7, C_5 and C_6 are the resistor and capacitor values as shown in Figure 3-23 and Table 3.1. Based on Equation 3.31, the DC gain, 3 dB bandwidth (ω_{3-dB}) and the filter Q can

be derived, and the final values are given by:

$$\text{DC Gain} = \frac{R_5}{R_{dly}} \tag{3.32}$$

$$\omega_{3-dB} = \sqrt{\frac{1}{R_5 R_7 C_5 C_6}} \tag{3.33}$$

$$Q = \sqrt{\frac{R_6^2 C_6}{R_5 R_7 C_5}} \tag{3.34}$$

In our design, the interstage amplifier resistors and capacitors are tunable. We incorporated two operation modes for the interstage amplifier: (1) performance mode where the DC gain is 8 (or 18 dB), and (2) test mode where the DC gain is 5 (or 14 dB). The test mode was incorporated as a backup option to prevent backend saturation only for test purposes. The default operating mode for the interstage amplifier is the performance mode with DC gain = 8. The values for all the resistors and capacitors for both modes of operation are shown in Table 3.1.

Parameter	Mode 1 Gain = 5 (14 dB)	Mode 2 Gain = 8 (18 dB)
R_5	1 kΩ	1.6 kΩ
R_6	482 Ω	350 Ω
R_7	245 Ω	100 Ω
C_5	242 fF	242 fF
C_6	90 fF	90 fF

Table 3.1: The two modes of operation for the interstage amplifier. The filter Q is chosen such that the peaking is 1 dB at the band edge.

The backend ADC in the prototype ADC is VCO-based ADC as implemented in [5,14,67]. This architecture was used to reduce the area and power consumption of the backend ADC. The problem of systematic non-linearity in a VCO-ADC is addressed by digital calibration (second, third and fourth harmonics are cancelled, other higher order harmonics do not degrade the VCO-ADC performance significantly, $<$ -90 dBc post digital cancellation) [67]. Figure 3-24 shows a simplified system-level diagram of the VCO-based ADC. The VCO instantaneous frequency is modulated by the input

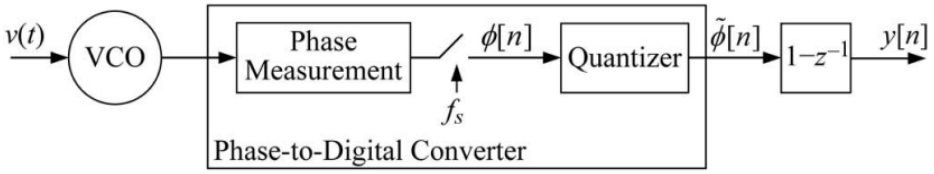


Figure 3-24: A simplified block diagram for a VCO-ADC [14].

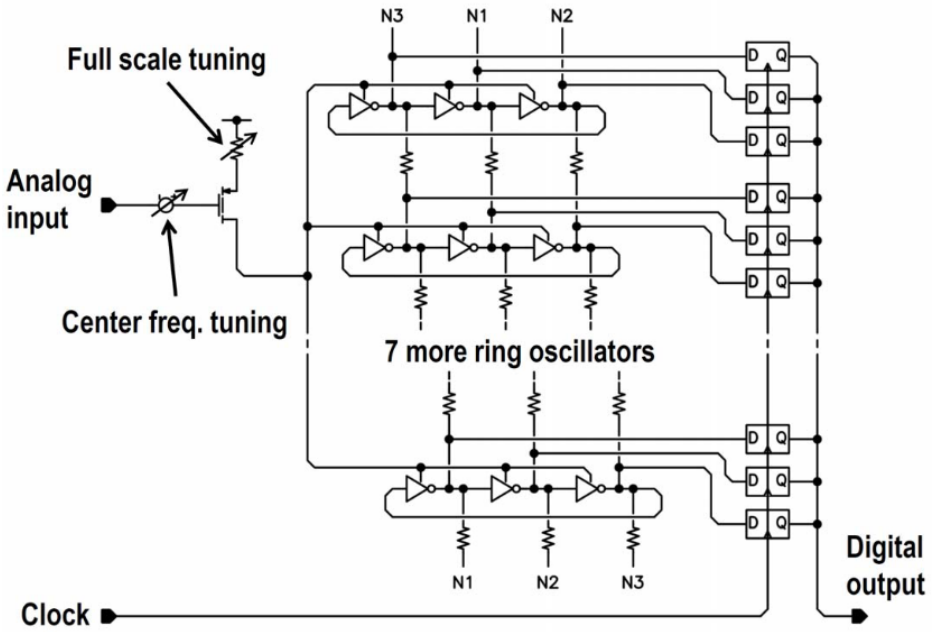


Figure 3-25: A simplified schematic of the VCO-ADC [5].

voltage. The VCO phase (time integral of instantaneous frequency) is quantized by the phase-to-digital converter and then processed by a discrete-time differentiator to give the VCO-ADC digital output. In a real implementation, the time period of the VCO output is linear w.r.t. the VCO input. However, the VCO quantizes the phase resulting in inherent non-linearity in the system because of a reciprocal relationship between the time period and the frequency. This is a property of the system itself, and not caused by circuit non-idealities. This non-linearity in the VCO-ADC output is corrected digitally as described in [67].

3.4 Layout

The proposed CT pipelined ADC was taped out in a 16 nm FinFET process. Figure 3-26 shows the floorplan of stage 1 of the proposed CT pipeline ADC. Our ADC was part of a shared tapeout with Analog Devices Inc. Therefore, several floorplan decisions were guided by other top-level considerations which are beyond the scope of this thesis. The general idea in our floorplan was to keep the stage-1 core components such as the delay line, sub-ADC-DAC and interstage amplifier in close proximity to each other to reduce the interconnect parasitics. Peripheral blocks such as bias and remote serial peripheral interface (RSPI) were placed in a way to minimize the area.

Figure 3-27 shows the overall stage 1 layout for the proposed ADC. The stage 1 area is 0.49 mm^2. The differential analog input comes from the left. The input splits into 3 paths approximately at the centroid of delay line, channel 0 sub-ADC-DAC and channel 1 sub-ADC-DAC to minimize any systematic delay mismatch in the signal path and the sub-ADC-DAC path. The output of the delay line (and the 2

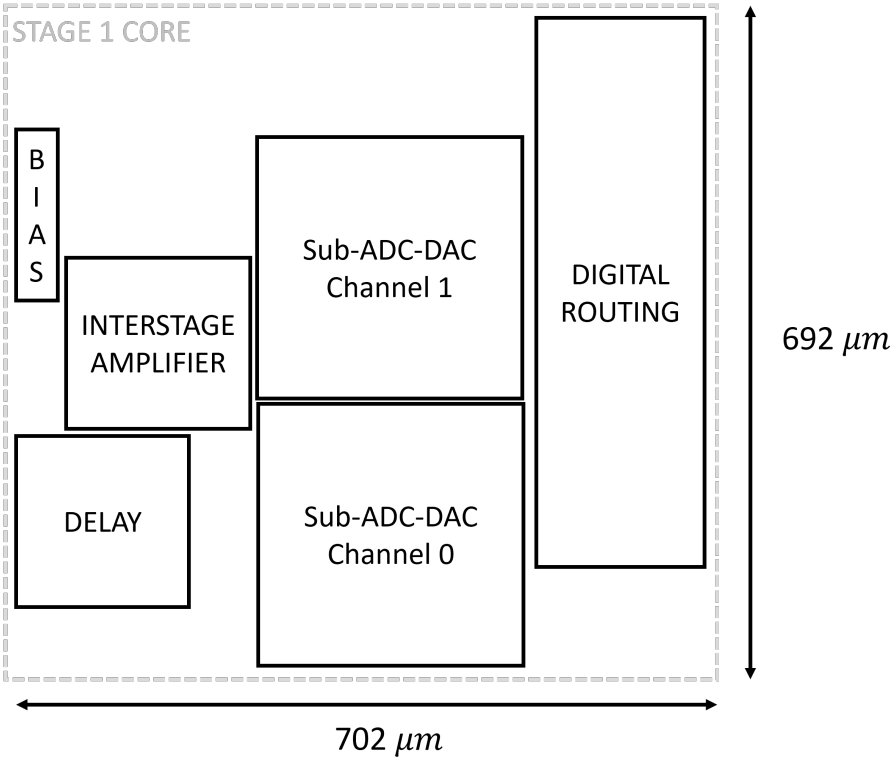


Figure 3-26: Floorplan of stage 1 in the proposed CT pipeline ADC.

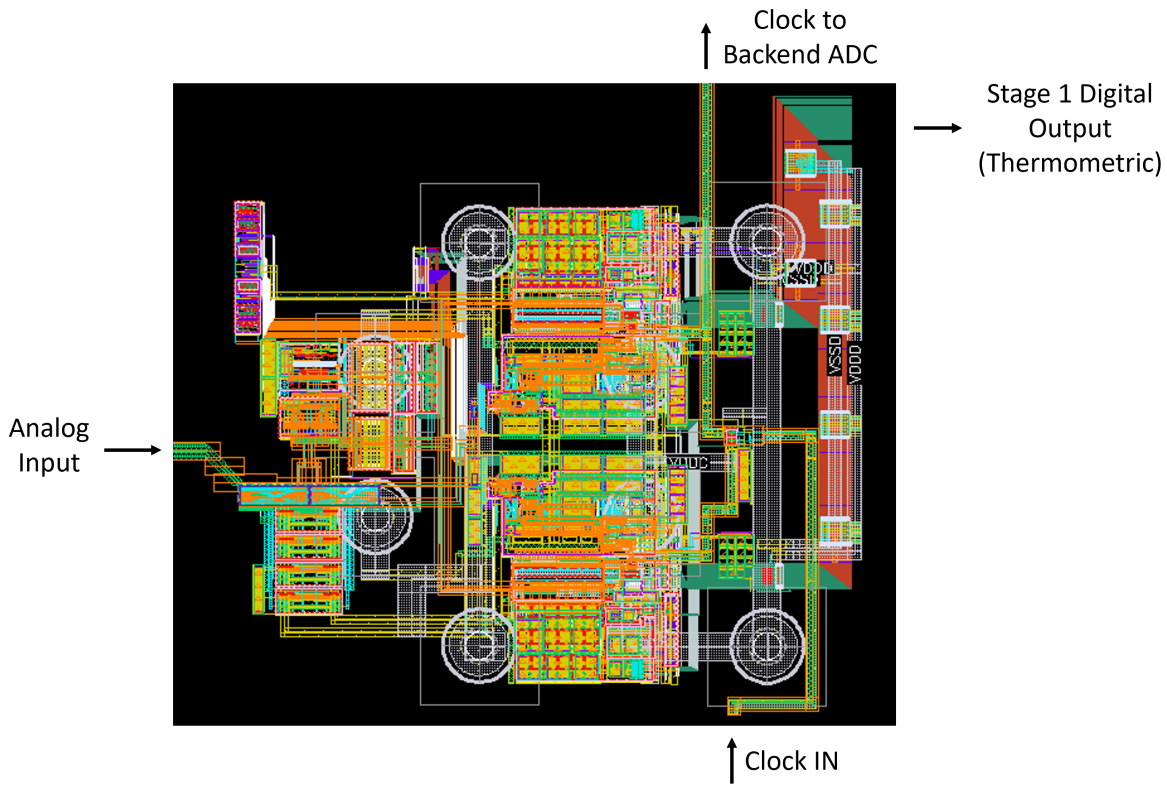


Figure 3-27: Layout of stage 1 in the proposed CT pipeline ADC.

sub-ADC-DACs) is called the summing node, and it is also the input to the interstage amplifier. The layout of the summing node is critical because any parasitic coupling to the stage-1 summing node injects noise and/or non-linearity in the signal path. To minimize coupling, we take the following layout precautions: (1) keep the delay line output, channel 0/1 sub-ADC-DAC output, and interstage amplifier input as close as possible to minimize the routing, (2) place dummy exclude around the summing node symmetrically to avoid unnecessary coupling during the metal fill step, and (3) visually inspect the summing node environment (on the same metal layer, as well two layers on the top and two layers on the bottom) to ensure there is no source of systematic differential mismatch. In case there is an unavoidable metal trace passing in the vicinity of the summing node, then we intentionally duplicate that trace to maintain symmetric coupling for the differential signal on the summing node. Similar precautions are taken for the residue signal (output of the interstage amplifier). On the residue node, additional ground lines are placed on the adjacent metal layers,

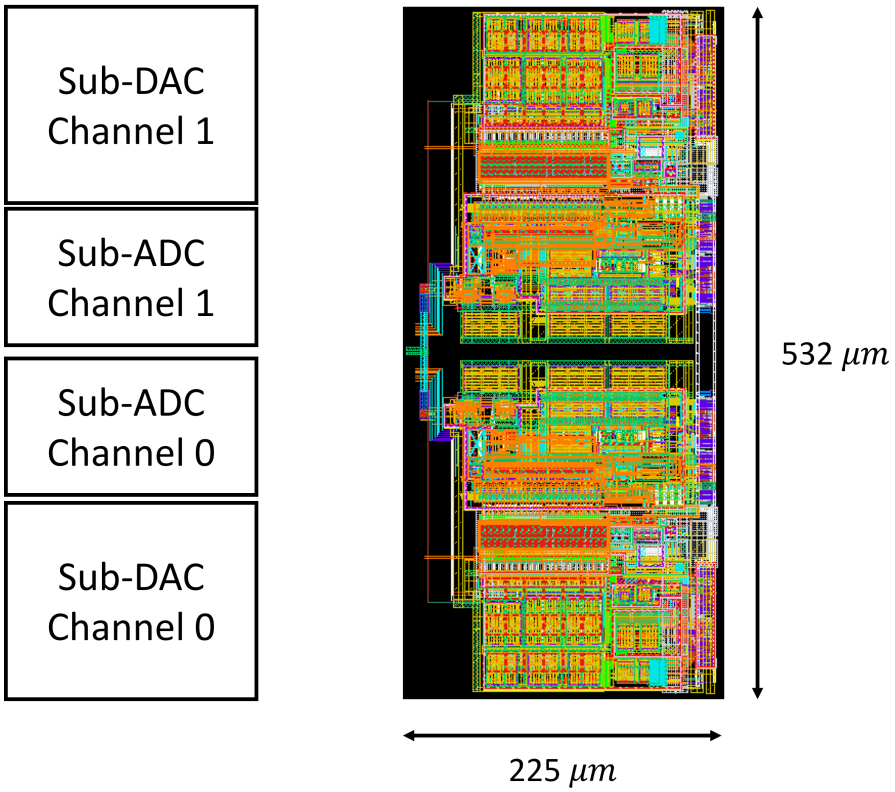


Figure 3-28: Layout of the stage 1 sub-ADC-DAC.

creating a box-like structure around the residue node, to provide better shielding.

Figure 3-28 shows the layout of the time-interleaved sub-ADC-DAC path. Channel 0 is placed on the bottom, and channel 1 is flipped and placed symmetrically on the top. Channel 0/1 sub-ADCs is placed in the center whereas the sub-DACs are placed on the outer side for the following reasons: the sub-ADC input needs to be approximately the same distance from the delay line from the point where the differential input is split into 3 paths. Placing the sub-ADCs in the middle portion helped in satisfying this constraint. In the layout, all traces such as bias, input, and output are routed symmetrically to and from the center-left to avoid any systematic mismatch between channel 0 and channel 1. The sub-ADC output is a 4-bit thermometric coded digital word ($D_1 < 15 : 0 >$), and it is parallelized from 6.4 GHz to 1.6 GHz ($\widehat{D}_1 < 63 : 0 >$ [3]) to prevent signal degradation caused by high-frequency routing. Figure 3-29 shows the routing of the parallelized stage 1 digital output to

[3] $D_1 < 0 >$ is split into $\widehat{D}_1 < 0 >$, $\widehat{D}_1 < 1 >$, $\widehat{D}_1 < 2 >$ and $\widehat{D}_1 < 3 >$.

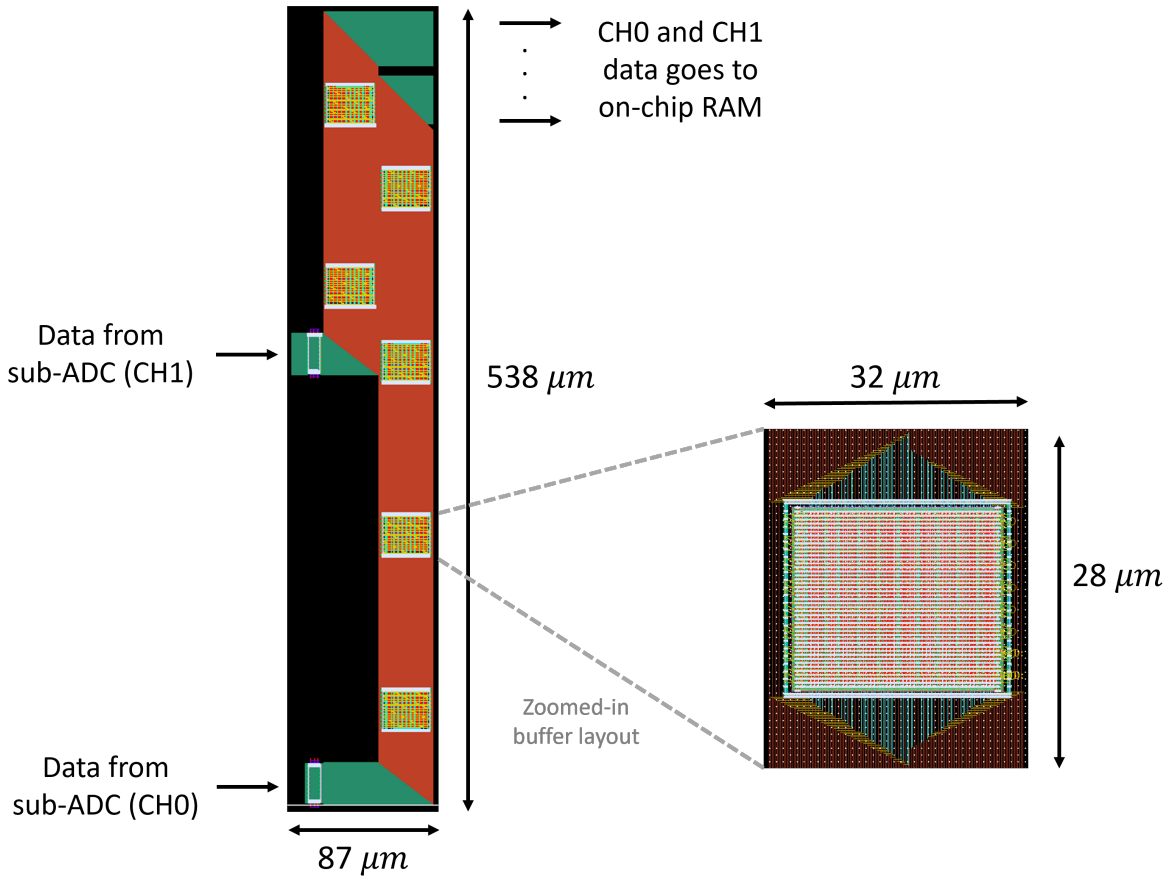


Figure 3-29: Layout of the digital routing for stage-1 data. Thermometric data is down-converted from 6.4 GHz to 1.6 GHz to reduce signal degradation while routing. Additionally, digital buffers are placed approximately 90 μm apart to restore the signals on the digital bus.

the on-chip RAM. Even after down-conversion by a factor of 4, the signal was significantly degraded because of long interconnects ($>$ 600 μm). The time constant of the RC-parasitic of the interconnect increases in proportion to the square of the length of the interconnect, which makes routing challenging. To mitigate signal degradation, we placed multiple buffers along the digital route. For estimating the optimal buffer spacing to prevent signal degradation while minimizing the power penalty, we performed transient simulations at the worst PVT corner for different interconnect lengths using the post-extracted model for interconnects. To have a conservative design, we aimed to get the RC time constant of the interconnect to be less than 10% of the clock period (625 ps). In addition to this, we added a 20% margin-of-safety, re-

sulting in approximately 90 μm spacing between buffers to prevent signal degradation across $>$ 600 μm routing for 1.6 GHz digital signals. The layout of a zoomed-in buffer is shown in Figure 3-29. The buffer block contains 77 individual buffers [4], where each buffer has 22 inverters. The inverters are placed in 1x, 3x, 6x and 12x sequences to provide an appropriate fan-out for driving the next interconnect. Each buffer block comprises of 1,694 inverters and occupies only 32x28 μm^2 area. A total of 6 such buffer blocks have been used in our design, 4 for channel 0, and 2 for channel 1.

The delay line layout is shown in Figure 3-30. The series resistors (denoted as R_{DLY} in Figure 3-30 are placed on the bottom left and bottom right. The capacitors C_1 through C_4 are stacked vertically. The intermediate nodes of the delay line are brought out to the periphery for easier routing. The series connections within R_{DLY} are made with higher metal layers to reduce the parasitic resistance. Based on the post-extraction simulations, we notice that the parasitic resistance can be as high as 15% if lower-level metal layers are used. With higher-level metal layers (M9 – M13), the parasitic resistance is only 2% of the total series resistance value ($R_{DLY} = 200\Omega$, $R_{par} = 4\Omega$). For the same reason, the delay line input and output are also routed on higher-level metal layers. The output is taken out at the bottom and placed very close to the interstage amplifier input to minimize parasitics on the summing node.

[4] 64 buses for thermometric data, 4 buses for dither, 8 buses for over-range and under-range flag, and 1 bus for 1.6 GHz clock.

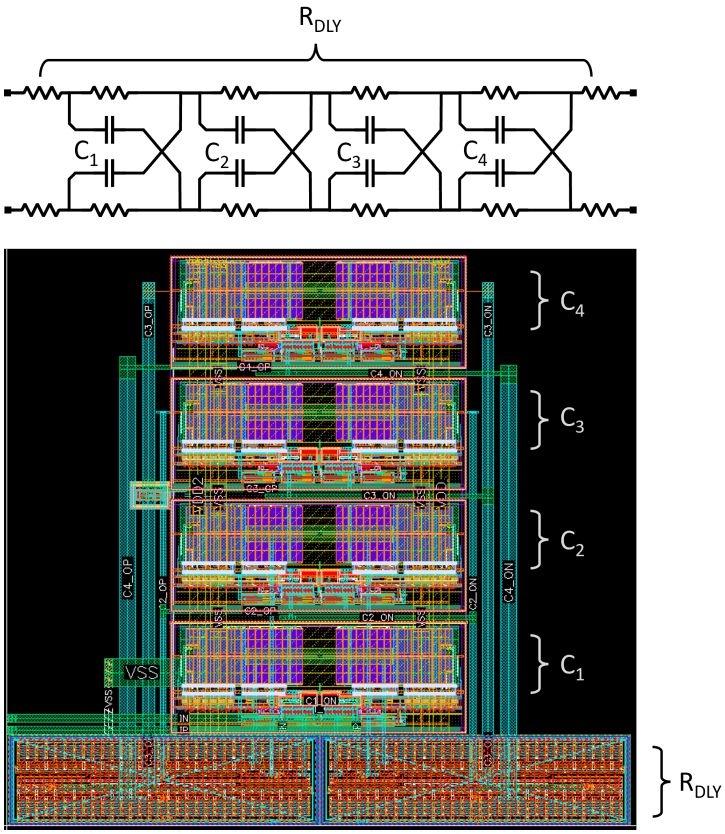


Figure 3-30: Layout of the 4x-cascaded RC lattice-based delay line.

Chapter 4

Measurement Results

The proposed CT pipeline ADC with a time-interleaved sub-ADC-DAC path was fabricated in a 16 nm FinFET process. The chip micrograph is shown in Figure 4-1. The ADC occupies an active area of 0.77 mm^2.

The measurement setup is shown in Figure 4-2. The prototype ADC uses 5 supplies: (1) A 1.0 V supply for analog/mixed-signal circuits, (2) a 1.8 V supply for the DAC core, (3) a 0.8 V supply for the digital, (4) a 1.0 V supply for the clock receiver, and (5) a 1.8 V supply for the bias circuitry. The input signal varies from 250 mV to 750 mV (common mode voltage = 500 mV, and differential peak-to-peak voltage = 500 mV).

At startup, foreground calibration is performed for the center frequency of the VCO-based stage 2 ADC. Then, the sub-DAC unit elements (UEs) for channel 0 and channel 1 are calibrated. First, all the UEs are calibrated to match each other. All UEs have the option for a hard set (UE set to 1: current goes to the positive sub-DAC output) or reset (UE set to 0: current goes to the negative sub-DAC output). Half UEs are set to 1 and the other half is set to 0. The input is turned off, and only the sub-DAC channel under calibration is turned on. One of the UE is set as the reference, and one UE is calibrated in each run. The average of the stage 2 output is noted. The polarity of the reference UE and the UE under calibration is flipped, and then the average of the stage 2 output is noted again. The UE under calibration is tuned till the difference between the two averages approaches zero. This process is

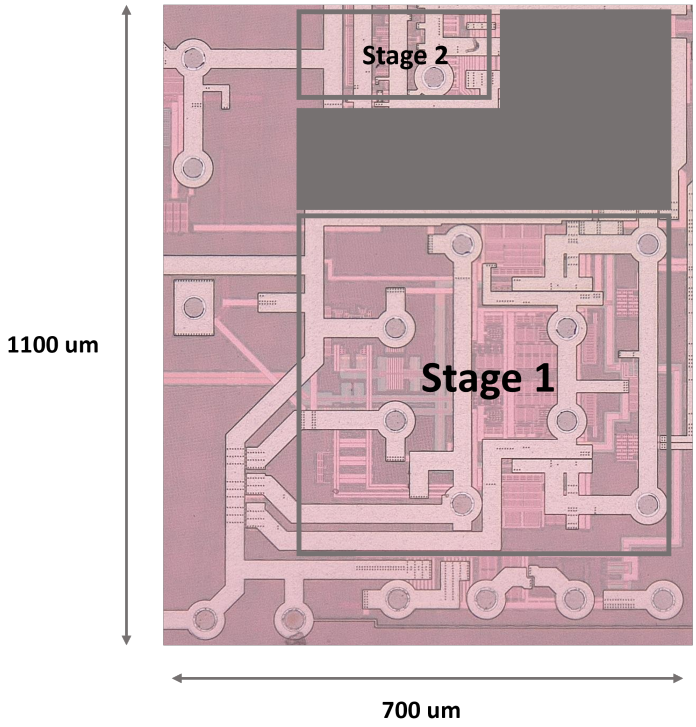


Figure 4-1: Die photo of the prototype ADC.

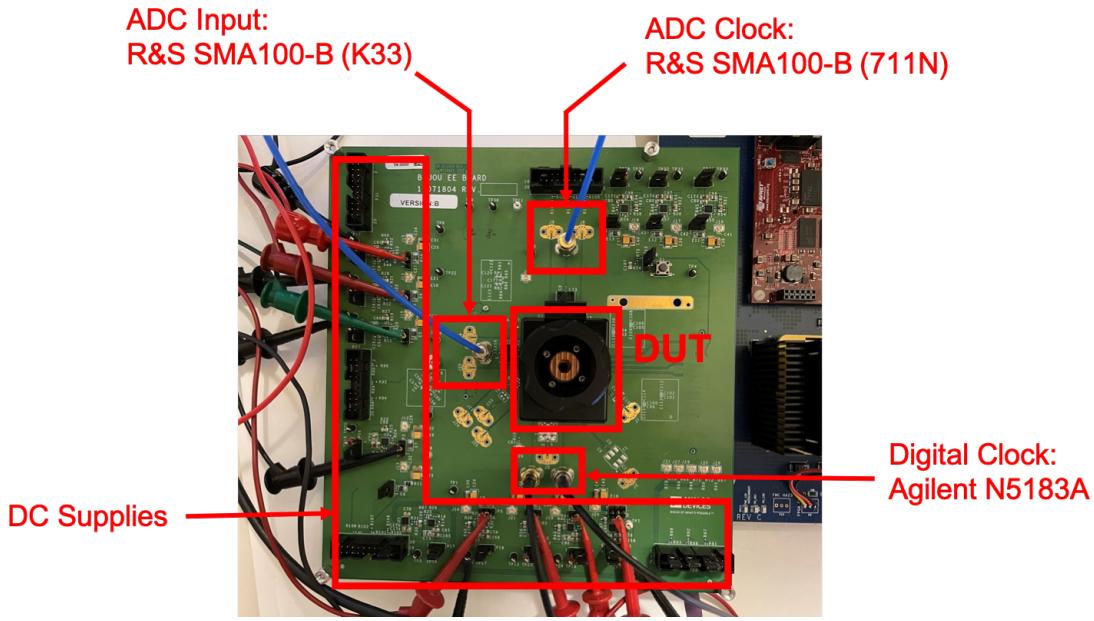


Figure 4-2: The measurement setup showing the test board and device under test (DUT).

repeated for all UEs in a channel, and then for all channels in stage 1. Finally, the values for all UEs are changed in sync to match the sub-DAC full-scale current to that of the output of the delay line.

Next, the comparator offsets of the sub-ADCs are calibrated. In the prototype, we have the option to swap the relative positions of the comparators on the Flash reference ladder. Using this option, we calibrate each comparator by setting it to the middle of the reference ladder, and a -10 dBm sinusoidal input is applied so that only the comparator under test is toggled. For zero comparator offset, the mean of the stage-1 digital output should be very close to zero. This process is repeated for all 32 comparators in stage 1 (17-level Flash output requires 16 comparators, and we have two time-interleaved channels making the total comparator count to be 32).

The interstage amplifier is calibrated next. To estimate the DC gain of the interstage amplifier, the inverse of the stage 2 reconstruction filter is used (as shown in Equation 2.19 and 2.20). Then, the feedback resistor in the interstage amplifier is tuned to get the desired DC gain. To tune the cut-off frequency and Q of the interstage amplifier, a small input signal is applied and the sub-ADC-DAC path is turned off. The input frequency is swept from 50MHz to 1000MHz, and the RMS value of stage 2 digital output is used as a proxy for the interstage amplifier gain at different frequencies. The overall transfer function is also shaped by the frequency response of the matching network at the input, but the above-mentioned method serves as a simple way to calibrate the cut-off frequency and Q of the interstage amplifier.

The delay is also calibrated in a similar fashion. A large amplitude sinusoidal signal is applied at the input, however, the sub-ADC-DAC path is turned on. The stage 1 residue amplitude is estimated from the stage 2 digital output. The capacitors in the delay line are tuned appropriately to get a near-optimal stage-1 transfer function across the ADC bandwidth (i.e. the shape of the transfer function should look similar to the magnitude response shown in Figure 3-19).

After the foreground calibration is performed, the test input signal is applied. The ADC performance has been presented in the following sub-sections.

4.1 Key Performance Specs

4.1.1 Dynamic Performance

Figure 4-3 shows the ADC output spectrum for a low-frequency small-signal sinusoidal input (-60 dBFS at 206.25 MHz). The digital reconstruction is performed offline in MATLAB. A 16-tap FIR filter has been used, and the filter coefficients are computed using the LMS algorithm [4, 7]. The LMS digitization bandwidth is set to 1000 MHz. The in-band noise (IBN) is -60.54 dB giving an average noise spectral density (NSD [1]) of -150.5 dBFS/Hz. Figure 4-4 shows the ADC output spectrum for a low-frequency large signal sinusoidal input (-1 dBFS at 206.25 MHz). The average NSD is -150.2 dBFS/Hz, and the measured HD2 and HD3 are less than -84.7 dBFS and -80.35 dBFS respectively. The peak SNR and SNDR are 61.7 dB and 61.6 dB respectively.

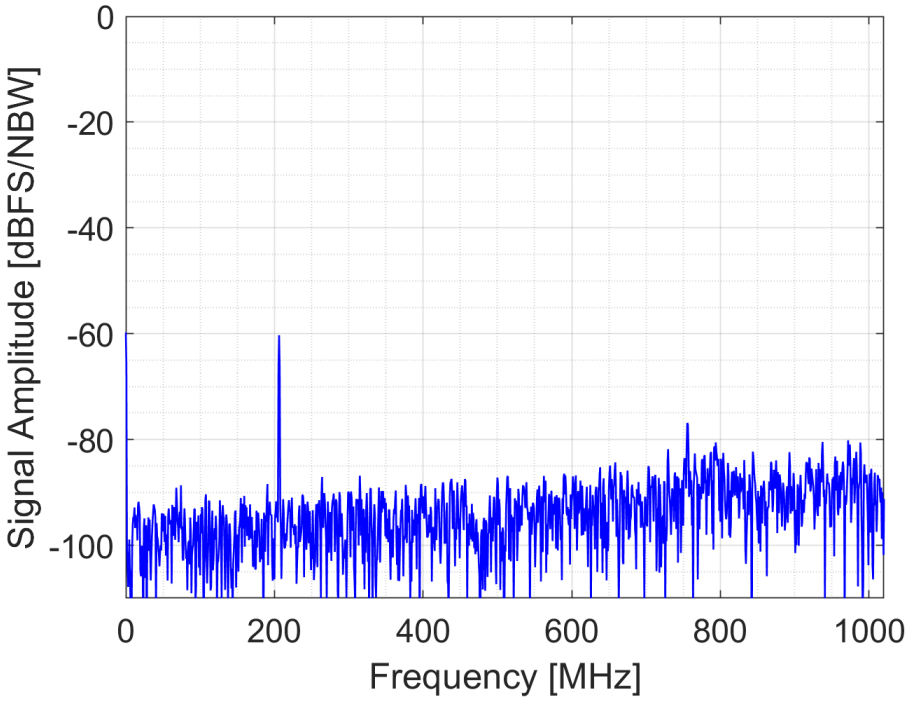


Figure 4-3: ADC output spectrum for a -60 dBFS tone at 206.25 MHz with a 8192-point FFT. The average NSD is -152.5 dBFS/Hz.

[1] NSD = In-band Noise - $10\log_{10}$(BW) [dBFS/Hz]

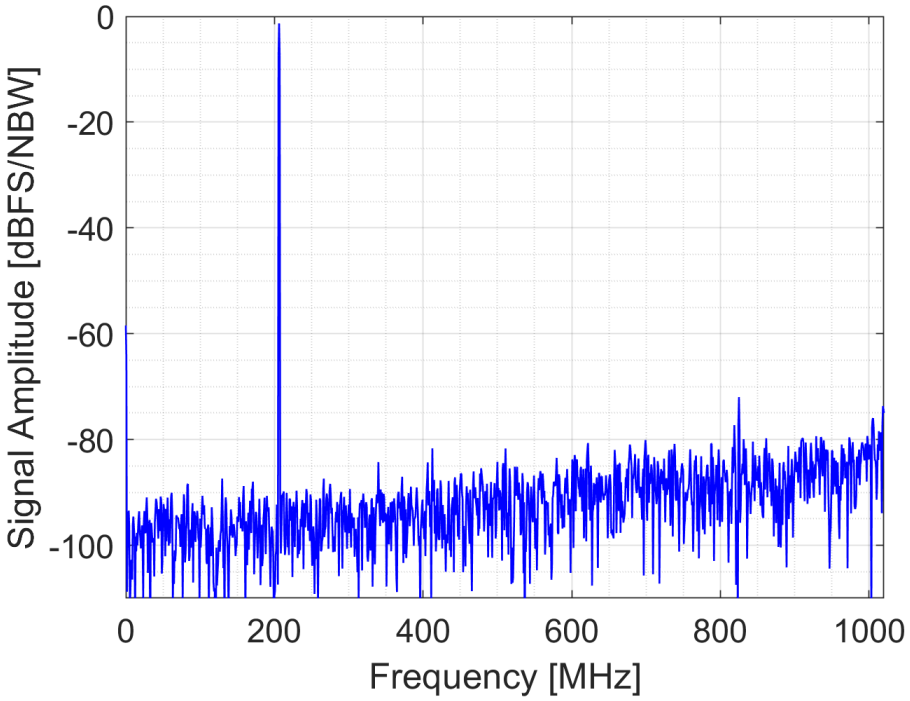


Figure 4-4: ADC output spectrum for a -6 dBFS tone at 206.25 MHz with a 8192-point FFT. The average NSD is -151.7 dBFS/Hz.

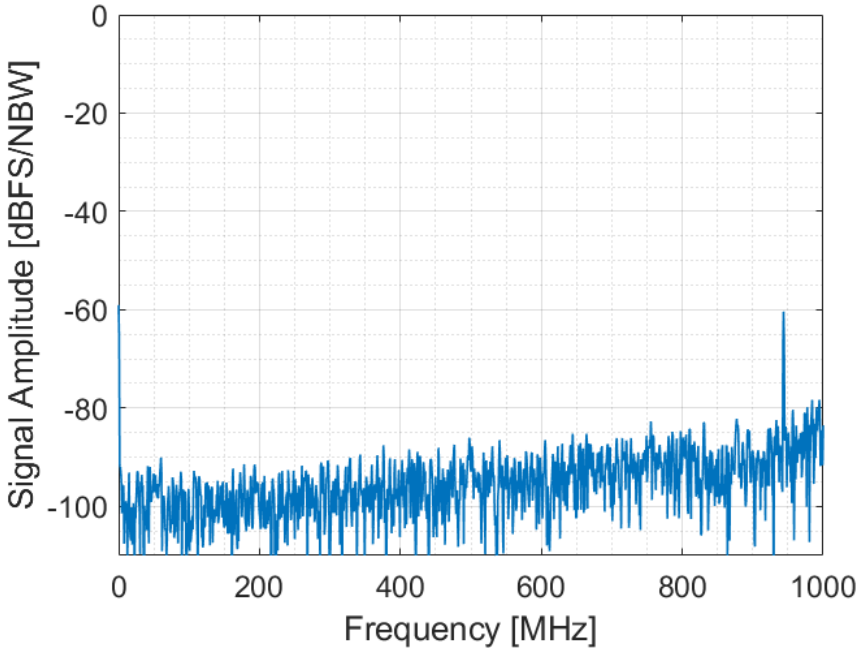


Figure 4-5: ADC output spectrum for a -60 dBFS tone at 943.75 MHz. The average NSD is -152.4 dBFS/Hz.

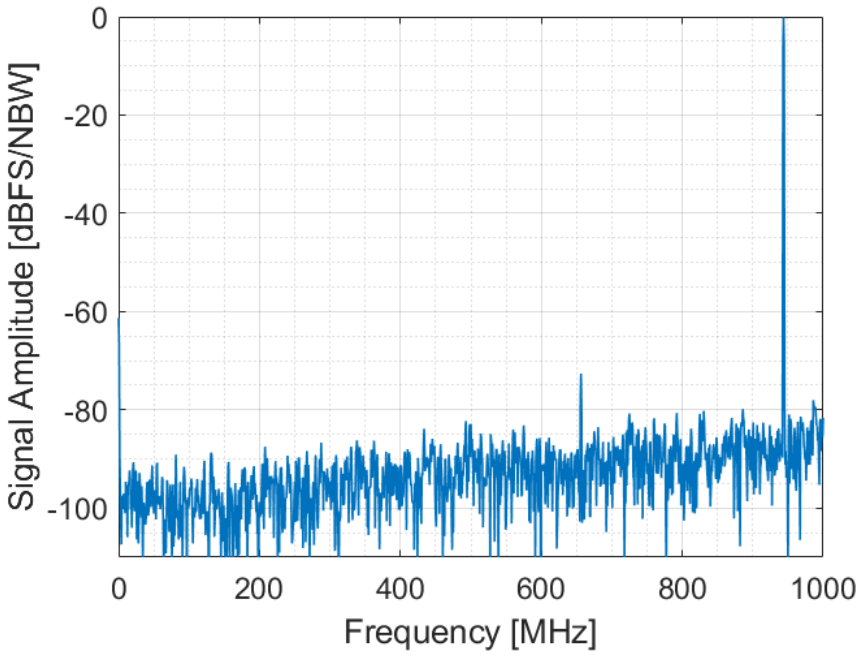


Figure 4-6: ADC output spectrum for a -1 dBFS tone at 943.75 MHz. The average NSD is -150.8 dBFS/Hz.

Figure 4-5 shows the ADC output spectrum with a high frequency small-signal sinusoidal input (-60 dBFS at 943.75 MHz) achieving -152.4 dBFS/HZ average NSD. The output spectrum with a large amplitude signal (-1 dBFS at 943.75 MHz) is shown in Figure 4-6. The average NSD is -150.8 dBFS/Hz giving a peak SNR of 60.8 dB.

The SNR and SNDR v.s. signal amplitude for a low-frequency input (f_{in} = 206.25 MHz) have been shown in Figure 4-7. The ADC achieves a peak SNR/SNDR of 61.7 dB and 61.6 dB resulting in a 9.9-bit ENOB. The dynamic range of the ADC is 62.6 dB. Figure 4-8 shows the SNR and SNDR vs. signal amplitude for a high-frequency input signal (f_{in} = 943.75 MHz). The ADC achieves a peak SNR of 60.8 dB (equivalent to 9.8-bit ENOB) and the dynamic range is 63.7 dB.

Figure 4-9 shows the SNR, SNDR, and SFDR v.s. input frequency. The measured signal transfer function (STF) and anti-aliasing are shown in Figure 4-10. The ADC achieves at least -40 dB and -29 dB inherent anti-aliasing for small- and large-amplitude interferer near the sampling frequency (6.4 GHz).

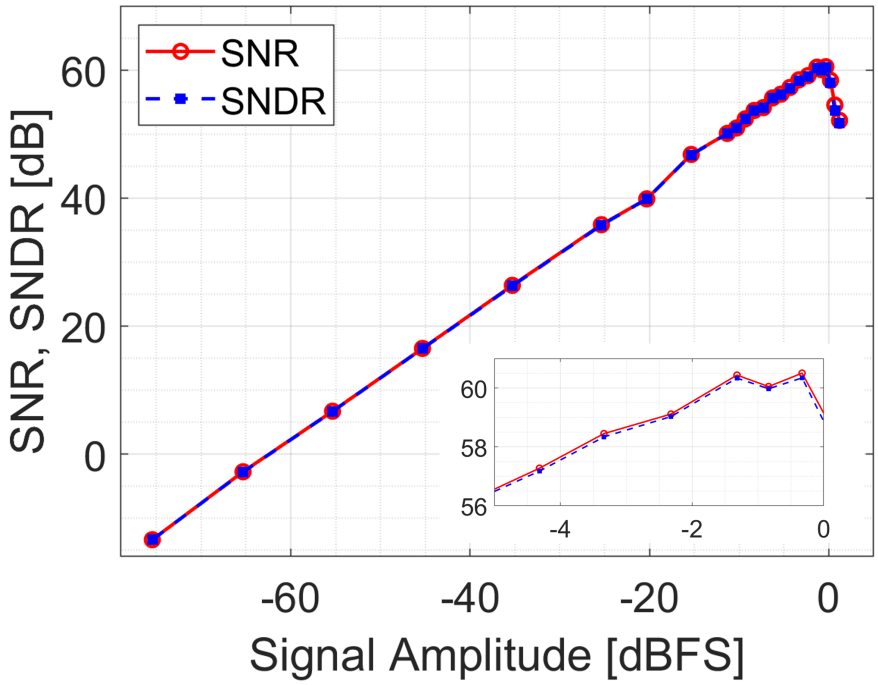


Figure 4-7: SNR and SNDR v.s. signal amplitude for a 206.25MHz input signal.

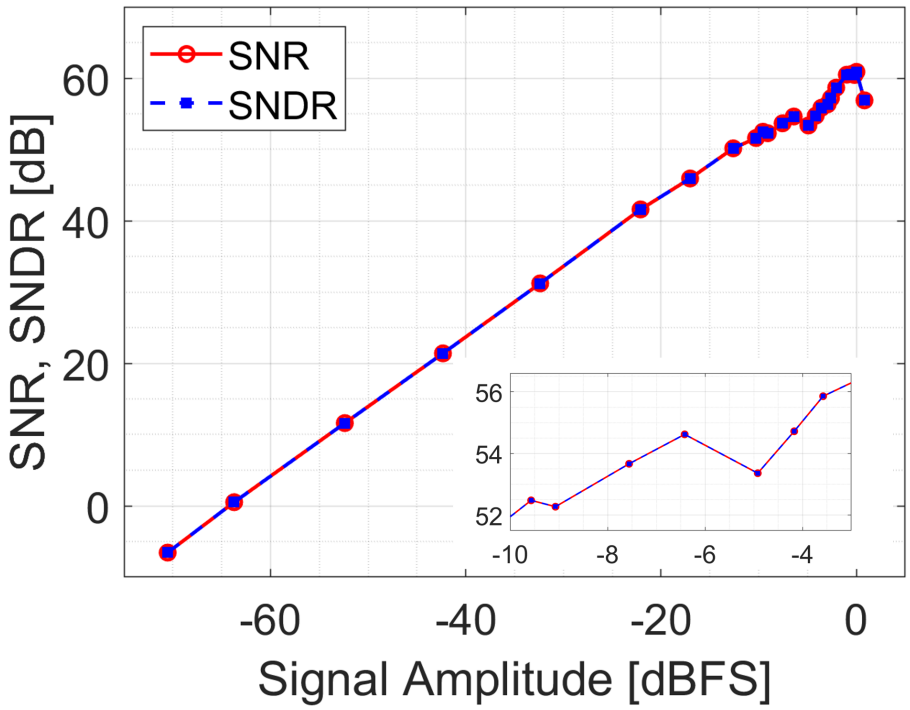


Figure 4-8: SNR and SNDR v.s. signal amplitude for a 943.75MHz input signal.

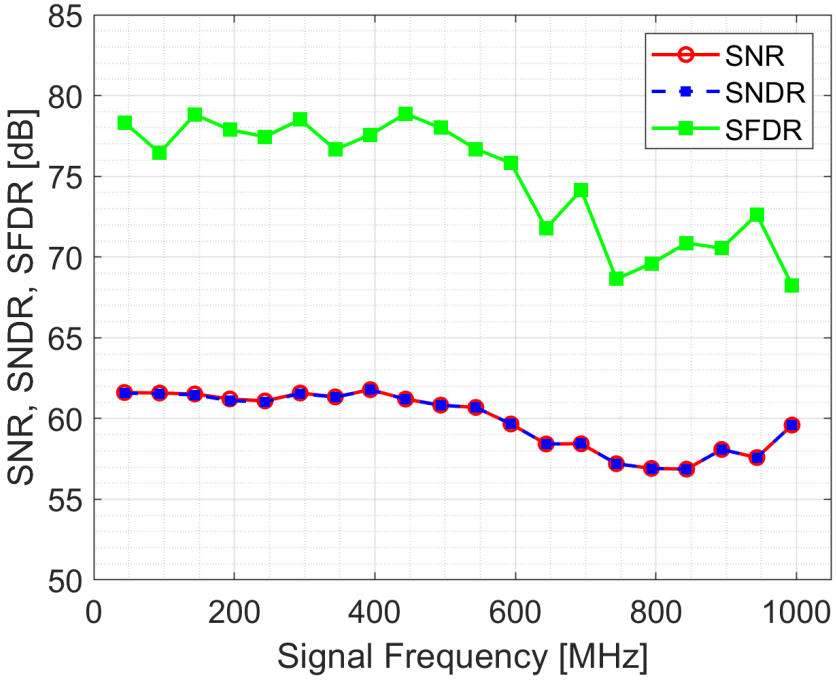


Figure 4-9: SNR, SNDR, and SFDR v.s. signal frequency.

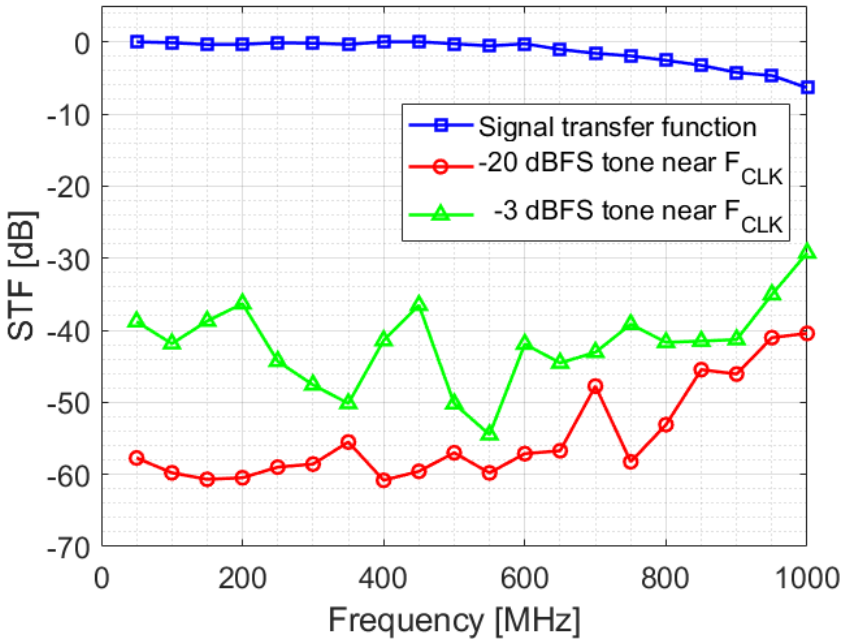


Figure 4-10: The signal transfer function and anti-aliasing vs. input frequency. The small signal interferer is a -20dBFS tone applied from 5400 MHz to 6350 MHz. The large signal interferer is a -3dBFS tone applied from 5400 MHz to 6350 MHz.

4.1.2 Jitter Sensitivity

In this sub-section, we present the ADC performance with a clock having higher jitter. The goal for this experiment is to validate the jitter limitations in a CT pipeline ADC (as presented in section 2.2.3) and to estimate the clock jitter tolerance for the proposed ADC.

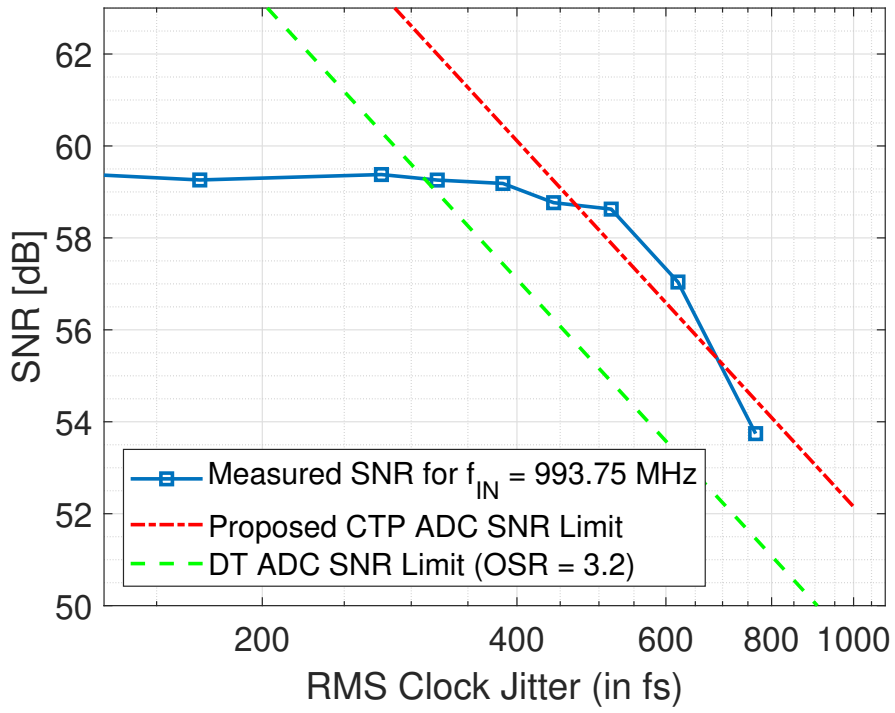


Figure 4-11: The measured SNR vs. RMS clock jitter for a 793.75 MHz single-tone input signal.

Figure 4-11 shows the SNR vs. RMS clock jitter for a near-800MHz input tone. The measured SNR matches closely with the estimated CT pipeline ADC jitter limitations (see Equation 2.45). To emulate a high clock jitter at the ADC, we reduce the amplitude of the external signal generator which worsens the jitter of the on-chip clock receiver. The relationship between the signal amplitude and clock receiver jitter is found using simulations to avoid additional on-chip circuitry. The ADC output spectrum with 100 fs and 517 fs RMS clock jitter is shown in Figure 4-12. There is almost no degradation in the output SNR. In comparison to an upfront sampled ADC with similar input signal and clock (F_{in} = 793.75 MHz, f_{clk} = 6.4 GHz having 500 fs

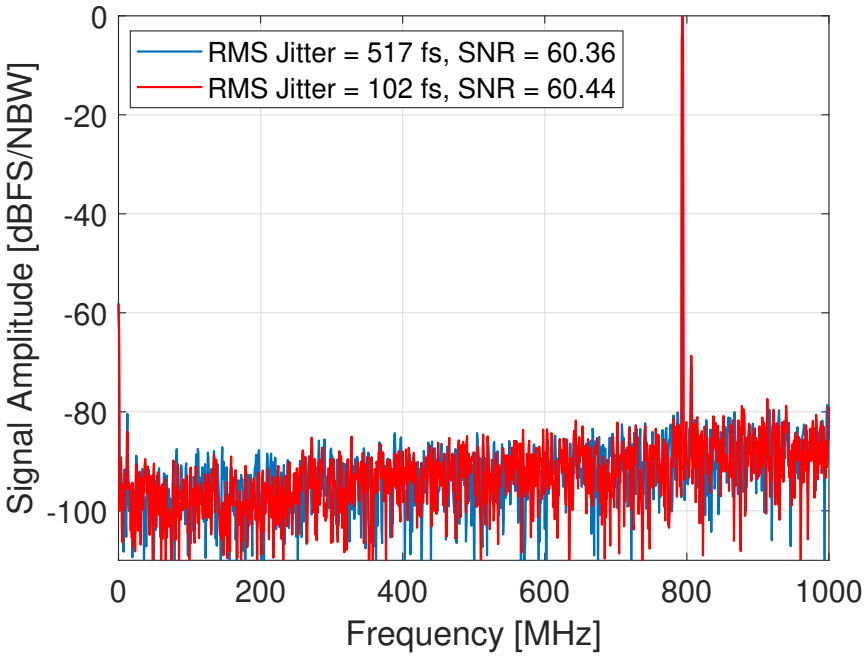


Figure 4-12: The ADC output spectrum for a 793.75 MHz input tone with 100 fs and 517 fs RMS clock jitter.

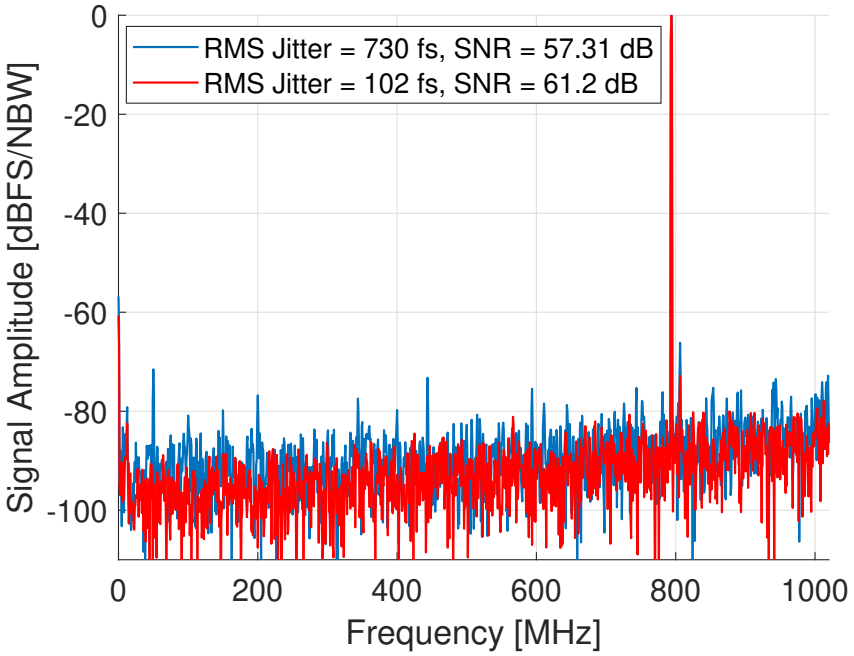


Figure 4-13: The ADC output spectrum for a 793.75 MHz input tone with 100 fs and 730 fs RMS clock jitter.

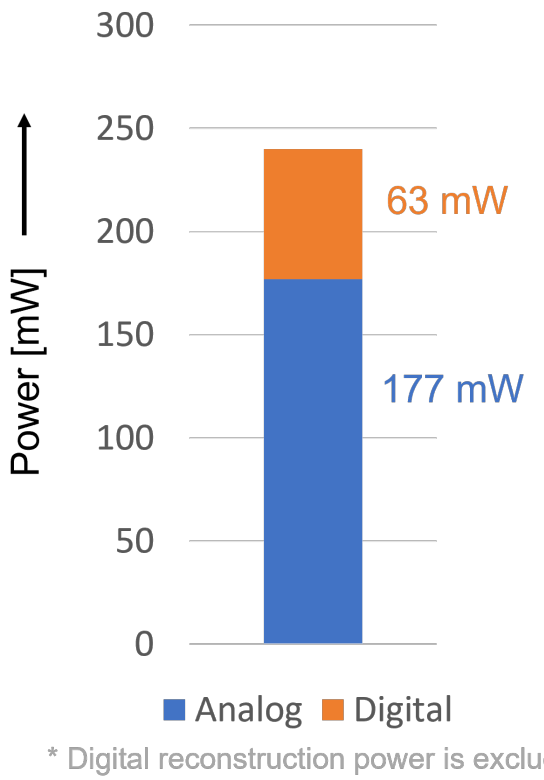


Figure 4-14: Measured power consumption of the proposed CT pipelined ADC. Digital reconstruction filter power is excluded since it was implemented off-chip.

RMS jitter and OSR = 3.2), the proposed CTP ADC achieves $\tilde{3}$.5 dB better SNR owing to the 2x time-interleaved sub-ADC-DAC path. The ADC output spectrum with 100 fs and 730 fs RMS clock jitter is shown in Figure 4-13, showing a SNR degradation (w.r.t. the low-jitter SNR) of 3.9 dB for the high clock jitter test.

4.1.3 Power Consumption

The prototype ADC consumes 240 mW power. The power breakdown for the analog and digital is 177 mW and 63 mW respectively. The analog power breakdown is shown in Figure 4-15. The stage 1 sub-ADC-DAC path consumes 88 mW, split almost evenly between channel 1 and channel 2, the interstage amplifier consumes 9 mW, and the stage 2 ADC consumes 80 mW power.

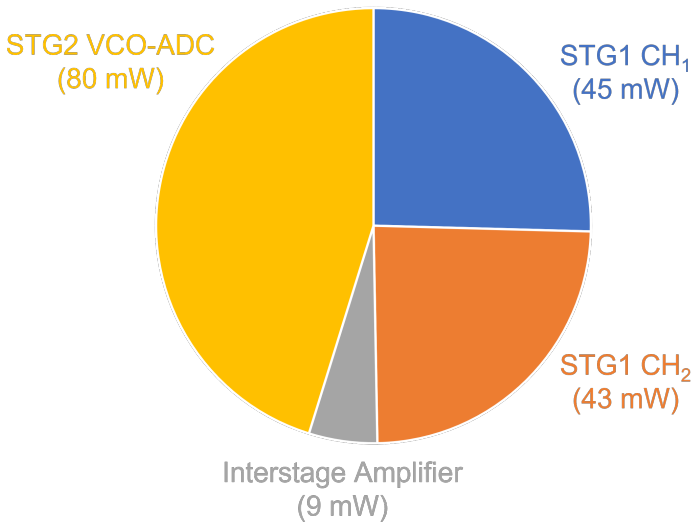


Figure 4-15: Measured analog power breakdown for the proposed CT pipeline ADC. The channel-1 power is slightly higher in comparison to channel-2. A possible reason could be the non-identical supply routing.

4.2 Performance Summary and Comparison

A performance summary of the proposed CT pipeline ADC is shown in Table 4.1. The measured results are also compared with previously published CT pipeline ADCs. In comparison to [5], [6] and [2], the proposed ADC achieves a higher bandwidth, owing to (a) better phase matching in the signal path and the sub-ADC-DAC path thanks to the cascaded RC lattice delay line, and (b) time-interleaved sub-ADC-DAC path. When compared to [4], although the ADC bandwidth is similar to [4], the area and power consumption are smaller by a factor of 6.6x and 9.7x respectively. The primary reason for such a large difference in the area and power is the use of the RC delay line and the VCO-based stage 2 instead of the 7 continuous-time stages in [4].

The proposed CT pipelined ADC also fairs well when compared to other ADC architectures popularly used in high bandwidth applications, such DT pipeline and CT $\Delta\Sigma$ ADCs. In comparison to the DT pipeline ADC implemented in [35], the proposed ADC achieves 3.3x lower digitization bandwidth. This is expected because of the Nyquist rate operation of the DT pipeline ADC. However, the proposed ADC provides inherent anti-aliasing, thereby greatly reducing the power of the anti-alias

	This work	ISSCC 2020 [4]	ISSCC 2017 [3]	TCAS-I 2022 [5]	ISSCC 2017 [1]	JSSC 2016 [2]
Architecture	**CT Pipeline Interleaved**	CT Pipeline VCO-based	CT Pipeline Multistage	CT Pipeline w/ Decimation	DT Pipeline Interleaved	CT MASH ΔΣ
Technology	**16 nm FinFET**	16 nm FinFET	28 nm CMOS	65 nm CMOS	28 nm CMOS	28 nm CMOS
f_S [MHz]	**6400**	6400	9000	800	10000	8000
OSR	**3.2**	4.0	4.0	4.0	1.5	8.6
BW [MHz]	**1000**	800	1125	100	3300	465
Peak SNR/SNDR [dB]	**61.7/61.6**	58	65.4	70.4 / 70.0	56 / 55	68
SFDR [dB]	**68**	73	73	-	71	83
HD2 [dB]	**< -84.7**	-93	-79	-79.7	-77	-90
HD3 [dB]	**< -80.3**	-84	-86	< -77.2	-73	-86
DR [dB]	**63.7**	60	73	73	60	72
Inherent Anti-Aliasing	**Yes**	Yes	Yes	Yes	No	Yes
Power [mW]	**240**	280*	2330	29	2900	890
Area [mm^2]	**0.77**	0.34*	5.1	0.77	7.4	1.2
FoM_S = SNDR + $10\log_{10}$(BW/P) [dB]	**157.9**	152.5*	152.2	165.4	147	155

* Includes the digital reconstruction filter power (estimated 68mW) and/or area.

Table 4.1: Performance comparison with previously published CT pipelined ADCs and other state-of-the-art high bandwidth ADCs.

filter that precedes the ADC. In addition to this, the design of the driving buffer is relaxed because the proposed ADC presents a resistive load rather than a switched capacitor load. As discussed in previous chapters, a CT pipeline ADC presents a good trade-off between the digitization bandwidth and the ease of design of the input buffer and the anti-alias filter. In comparison to the CT ΔΣ ADC implemented in [28], the proposed ADC achieves 2.1x higher bandwidth, the reason being that CT ΔΣ ADCs require a higher OSR, limiting the digitization bandwidth for a given clock frequency. In comparison to [2, 4, 5] the proposed ADC achieves the highest bandwidth owing to the time-interleaved sub-ADC-DAC in the first stage. In comparison to [1] and [3], i.e., ADCs having $\geq$ 1 GHz digitization BW, the proposed ADC occupies less than 10x area and consumes 21x less power, thanks to the simplified 2-stage pipeline implementation. The figure-of-merit vs. application BW, fs /(2ŒOSR), is shown in Figure 4-16 [38]. The proposed ADC achieves a competitive FOMS of 157.9dB, which is amongst the best in comparison to other state-of-the-art high bandwidth CT ADCs.

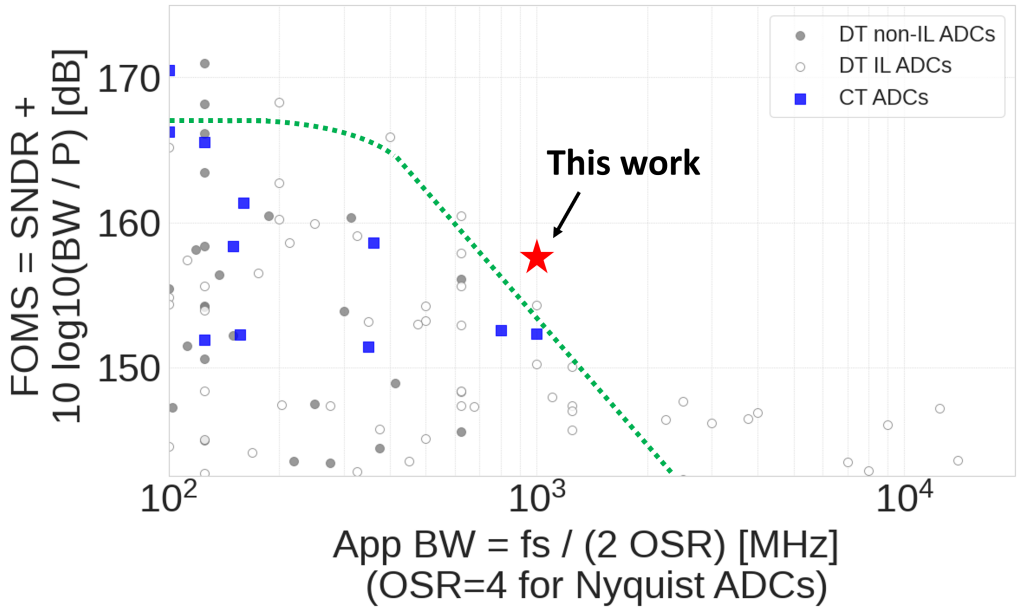


Figure 4-16: The Schreier figure-of-merit (FOM_S) vs. application bandwidth plot.

Chapter 5

Conclusion

5.1 Thesis Contribution

A continuous-time pipelined ADC with a 2-way time-interleaved sub-ADC-DAC has been presented in this thesis. The CT pipeline ADC is an emerging architecture that leverages the benefits of both the DT pipeline ADC and the CT $\Delta\Sigma$ ADC. A CT pipeline ADC is easy to drive because it presents a resistive load to the input buffer. Also, a CT pipeline ADC provides inherent anti-aliasing, thereby relaxing the design requirements or eliminating the anti-alias filter altogether. Additionally, since CT pipeline ADCs operate at a relatively low OSR, they can support higher bandwidth for a given clock frequency in comparison to CT $\Delta\Sigma$ ADCs.

In this thesis, we presented an analytical framework to assess the impact of clock jitter in CT pipeline ADCs. Since stage 1 is a continuous-time stage, there is no sample-and-hold upfront. Although a CT pipeline ADC's SNR is not limited by the upfront sampling jitter, the clock jitter impacts the sub-ADC output, stage 2 ADC output, and the sub-DAC output. The clock jitter in the stage 1 sub-ADC does not impact the overall ADC performance because it gets canceled by digital recombination (as long as the stage 1 residue remains within the full scale of stage 2 ADC). The stage 2 jitter error is reduced by the gain of the first stage when referred to the input, which is typically around 14 to 18 dB for a 4-bit stage 1. The stage 1 sub-DAC jitter error is added at the digital output and could potentially limit the

maximum achievable SNR in high-jitter environments for high-frequency inputs. We derived the upper bound on the SNR when an NRZ-DAC is used as the sub-DAC. With the assumption of a high oversampling ratio, the jitter-induced SNR limit in a CT pipeline ADC approaches the SNR limit presented in upfront sampled ADCs.

To improve the jitter sensitivity of CT pipeline ADCs, we implemented a time-interleaved sub-ADC-DAC path in stage 1 to increase the effective oversampling rate in stage 1. For proof-of-concept, we chose 2-way interleaving, although the interleaving factor can be increased for higher jitter tolerance. This reduces the in-band noise by a factor of 2 in the sub-DAC output, reducing the overall ADC noise floor by 3 dB. In addition to the reduced sensitivity to clock jitter, interleaved sub-ADC-DAC path also reduce the stage 1 residue because of faster effective sampling in the sub-ADC-DAC path. This enables a higher interstage gain resulting in better suppression of the backend ADC noise. Furthermore, a higher effective sampling rate in the sub-ADC-DAC path allows for an opportunity to increase the ADC bandwidth.

To that end, we implemented a 4x-cascaded RC lattice-based delay line. Inductor-based delay lines provide better phase matching between the signal path and the sub-ADC-DAC path. However, to reduce the area and eliminate inductive coupling with neighboring circuitry, an inductorless delay line was designed in the prototype. For an RC-lattice-based delay line with just one lattice element, the choice of R and C are strictly constrained: (1) the lattice resistance R must be chosen such that the delayed current full-scale matches the sub-DAC output current full-scale, (b) the lattice capacitance C must be chosen such that the signal path delay matches the sub-ADC-DAC path delay. This puts a constraint on the pole/zero locations, limiting the bandwidth of the delay line. To address this problem, we implemented a cascaded RC lattice structure allowing more degree of freedom in the design. Reducing the capacitor value shifts the pole/zero to higher frequencies, and by cascading several RC lattices, the delay in the signal path can be matched appropriately to the delay in the sub-ADC-DAC path. The cascaded RC delay line opens a path towards good phase matching to higher frequencies without large inductors. With further optimization of the cascaded RC delay line, higher bandwidth and/or better anti-aliasing can be

achieved in CT pipeline ADCs.

A prototype ADC was fabricated in 16nm FinFET process. The ADC achieves 61.7/60.8 dB (low/high frequency) SNR over 1-GHz bandwidth. The active area is 0.77 mm^2 and the ADC consumes 240 mW. The Schreier figure-of-merit (FOM_S) is 157.9 dB which is amongst the best for ADCs with digitization bandwidth greater than 500 MHz.

5.2 Future Work

In this thesis, we explored the jitter sensitivity aspects of the CT pipeline ADC architecture and presented a novel architecture with an interleaved sub-ADC-DAC path to improve CT pipeline ADC's jitter tolerance. However, the CT pipeline being a relatively new architecture presents the opportunity for further research.

The delay line plays a crucial role in a CT pipeline ADC. Since the delay line presents a fixed transfer function, the delay in the signal path is fixed for a given set of RLC values. This necessitates using a fixed sampling frequency in the sub-ADC-DAC path, else there will be a timing mismatch in the signal path and the sub-ADC-DAC path. One direction for future research could be to explore adaptive delay lines that could match the sub-ADC-DAC path delay in the foreground. This will also be useful for tracking timing mismatches caused by PVT variations. Additionally, the RC delay line can be further optimized for higher bandwidth and/or better anti-aliasing.

Another important research direction is to explore the CT pipeline architecture for near-Nyquist rate operation. Hypothetically, if there was no full-scale limitation due to the backend ADC, the CT pipeline ADC could operate at the Nyquist rate. If there could be a way to limit the residue within the backend ADC full-scale without oversampling the ADC, that will enable the CT pipeline ADC to operate at the Nyquist rate. The work presented in this thesis lays some groundwork for the possibility of a near-Nyquist rate operation because the time-interleaved sub-ADC-DAC path helps in preventing the backend ADC saturation. However, there are still some challenges in fully realizing a Nyquist rate CT pipeline ADC. For example, the digi-

tal reconstruction must be modified appropriately to match the modifications in the sub-ADC-DAC path. It is non-trivial to prove or disprove the feasibility of this idea, making it an interesting research direction for future work.

In a CT pipeline ADC, the digital reconstruction filter increases the hardware complexity and incurs an area and power penalty. The work presented in this thesis was implemented in a 16-nm FinFET process. However, with more advanced technology nodes such as 5-nm and smaller, the digital signal processing area and power can be significantly reduced, making the CT pipeline ADC architecture an attractive choice for near-GHz bandwidth integrated applications.

Finally, the sub-ADC-DAC path can be implemented with level-crossing-based ADC. This concept was briefly presented in Chapter 3 in the context of sensitivity to clock jitter. Although the level-crossing-based sub-ADC-DAC path is not suitable for high-jitter applications, it has some advantages that can be leveraged in low-jitter applications. For instance, the DAC output step size is always 1 LSB. If the signal path delay is matched correctly to the sub-ADC-DAC path delay, then the stage 1 residue ($I_{DLY} - I_{DAC}$) will be less than 1 LSB. Upon low-pass filtering in the interstage amplifier, the residue amplitude will reduce even further, allowing for a relatively large interstage gain. More importantly, since the sub-ADC-DAC path operates based on the input signal crossing the comparator thresholds, the stage 1 will have a so-called adaptive oversampling ratio - the sub-ADC will sample faster if the input is changing fast, and the sub-ADC will sample slower for slowly varying signals. This addresses the bandwidth limitation encountered in CT pipeline ADCs with a uniformly sampled sub-ADC-DAC path. However, the digital recombination for such an ADC will be complex, requiring further investigation to confirm the feasibility of this research direction.

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