Enhancement-Mode GaN Transistor Technology for Harsh Environment Operation

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***Abstract*—This letter reports an enhancement-mode (E-mode) GaN transistor technology which has been demonstrated to operate in a simulated Venus environment (460 °C, ~ 92 atm., containing CO_2/N_2/SO_2 etc.) for 10 days. The robustness of the W/p-GaN-gate AlGaN/GaN high electron mobility transistor (HEMT) was evaluated by two complementary approaches, (1) *in-situ* electrical characterization, which revealed proper transistor operation (including E-mode V_{TH} with < 0.09 V variation) in extreme environments; and (2) advanced microscopy investigation of the device after test, which highlighted the effect of the stress conditions on the epitaxial and device structures. To the best of the authors' knowledge, this is the first demonstration and comprehensive analysis of E-mode GaN transistors in such harsh environments, therefore establishing the proposed GaN technology as a strong contender for harsh environment mixed-signal electronics.**

***Index Terms*—GaN, transistor, enhancement-mode, mixed-signal, harsh environment, Venus, high temperature, high pressure, corrosive gas, degradation, microscopy**

I. Introduction

ELECTRONICS operating at high temperature (HT), well above the effective 250–300 °C rating of silicon-on-insulator (SOI) technology, are critical in extreme industrial applications (e.g. jet engines, nuclear reactors, deep oil well drilling), as well as in outer space, from the solar system to exoplanetary exploration [1], [2]. A promising solution, which avoids the thermal generation of carriers in conventional Si electronics, is the use of GaN and other wide band gap materials. Thanks to their wide band gap, and superior electrical, mechanical, and chemical properties, these materials have enabled a wide range of devices including transistors, MEMS and solar cells [3]–[5]. GaN electronics have demonstrated excellent performance in extreme environments (from cryogenic to high temperatures) across RF [6]–[8], power [9], [10] and mixed-signal applications [11].

Although initial experiments have highlighted the promising potential of E/D-mode GaN n-FETs (E: enhancement; D: depletion) [12] and complementary (GaN n-FET and GaN p-FET) configurations [13], [14] for GaN HT integrated circuits, more work is needed to improve the performance and robustness of the E-mode GaN transistor. These devices, as exemplified by p-GaN-gate AlGaN/GaN HEMTs, are of significant interest thanks to their possibility of monolithic integration in both E/D-mode and complementary platforms [15]. Given the rapid advancement of GaN HT technology, in particular in mixed-signal circuits [11], [16]–[18], it is an opportune time to examine the robustness of E-mode GaN technology under harsh environments to further optimize these transistors.

This letter presents advancements in GaN HT electronics in the following aspects, when compared to other works and the authors' earlier report [19]: (1) an E-mode GaN transistor technology has been demonstrated, characterized, and analyzed up to 500 °C; (2) testing of the transistor in harsh environment beyond SOI rating (simulated Venus environment), therefore revealing the unexplored potential of E-mode GaN technology for these applications; (3) *in-situ* electrical measurement confirms the continuous operation of the DUT over a prolonged period in harsh environment; (4) after harsh environment testing, a comprehensive microscopy investigation of the p-GaN-gate HEMT structure was conducted. This reveals the intactness/degradation of various device components and offers insights on areas of improvement in device design and fabrication.

II. Transistor Technology

The process flow of the proposed p-GaN-gate AlGaN/GaN-on-Si HEMTs [Fig. 1(a)] begins with the RF magnetron sputtering of tungsten (W, 200 nm) on p-GaN. W and p-GaN are patterned using an optimized low-damage GaN/AlGaN

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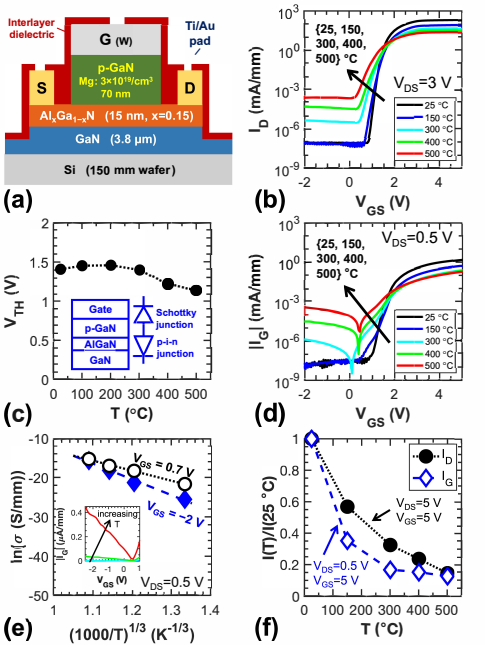

Fig. 1. Temperature dependency of the Tungsten/p-GaN-gate AlGaN/GaN HEMT up to 500 °C. (a) Device structure. (b) I_D *vs.* V_{GS}. (c) V_{TH}. (Inset: A simple two-diode model for the gate region.) (d) $|I_G|$ *vs.* V_{GS}. (e) 2D-VRH model. I_G (linear scale) *vs.* V_{GS} near $V_{GS} = 0$ V bias is shown in the inset. (f) I_D and I_G *vs.* temperature normalized to their room temperature values, for $V_{GS} = 5$ V, corresponding to the ON-state of the transistor.

selective etch recipe, while maintaining self-alignment between the two layers [20]. A combination of gate-first process, a refractory metal gate, and self-alignment in metal/p-GaN-gate distinguish the proposed transistor from a conventional p-GaN-gate HEMT. It is noted that, sputtering of W has been reported to cause some damage under the gate for an AlGaN MESFET [21], while its specific effect in p-GaN-gate HEMTs remains to be studied. Nevertheless, the above-mentioned device features have resulted in improved thermal stability, reduced hysteresis [22], and high scaling potential [15]. Next, Ti/Al/Ni/Au (20/100/25/50 nm) ohmic metal stack is deposited by electron beam evaporation and alloyed at 825 °C in N_2 ambient. As an improvement to [19], a SiO_2 layer (200 nm) was deposited using tetraethoxysilane (TEOS) precursor to passivate the device. After via opening, Ti (20 nm)/Au (300 nm) bonding pads were formed.

III. Temperature Dependency

The bare die was characterized in a probe station with a thermal chuck (rating of 500 °C) in air. As shown in Fig. 1(b)–(c), V_{TH} is relatively stable below 300 °C. The small initial increase of V_{TH} from room temperature to 200 °C could be attributed to a higher acceptor (Mg) ionization ratio in p-GaN at increasing temperature. Above 300 °C, a decrease in V_{TH} is observed. The gate region may be modeled as two back-to-back junctions [Fig. 1(c) inset] [23]. The trend of V_{TH} can be explained by the lower forward turn-on voltage of p-i-n junction, and the reduced Schottky barrier height.

The gate leakage current characteristics is shown in Fig. 1(d). Below the turn-on voltage of the p-i-n junction, the vertical junction current is blocked by the p-i-n junction. The gate leakage current is dominated by the surface current (two-dimensional variable range hopping, 2D-VRH), as shown in

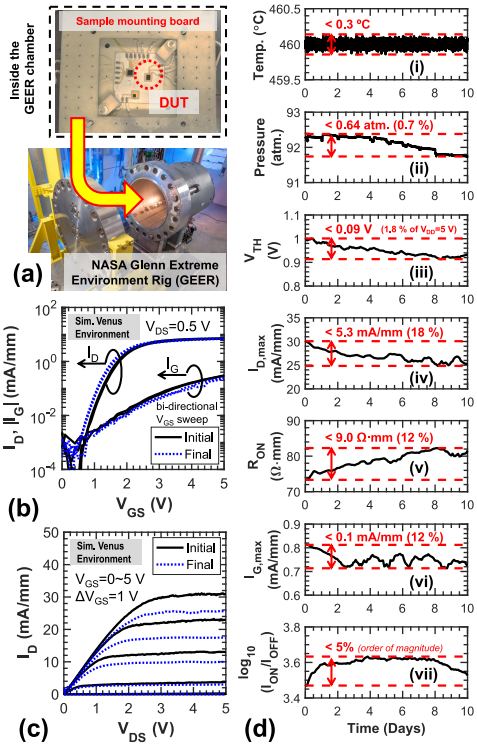

Fig. 2. (a) Setup which allows for the *in-situ* measurement of the DUT in a simulated Venus environment. (b)–(c) Transfer and output characteristics of the DUT for the initial measurement and the final measurement of the DUT in the simulated environment. (d) Variation of (i)–(ii) chamber conditions and (iii)–(vii) key transistor performance metrics during the reported duration of the test. For each metric, the absolute peak-to-peak value (in parenthesis: percentage of the peak-to-peak value with respect to the initial value, unless otherwise stated) are labelled.

the good fit of $\sigma \propto \exp\left(-T^{-1/3}\right)$ [Fig. 1(e)] [23]. Therefore, I_G increases with temperature. Here, a reasonable approximation for 2D-VRH was made using I_D-V_{GS} data at a small $V_{DS} = 0.5$ V. At highly positive V_{GS}, which corresponds to the ON-state of the transistor and the forward bias regime of the p-i-n junction, the vertical junction current dominates. The turn-on current I_G decreases with increasing temperature due to increased resistance in the drift region of p-i-n junction. I_G shows a similar trend as I_D up to 500 °C due to the reduced mobility [Fig. 1(f)] [24].

IV. Robustness in Harsh Environment

The device under test (DUT) was packaged using HT-rated components [2], [19] and placed in a simulated Venus environment (460 °C, ~ 92 atm., mainly CO_2/N_2, traces of SO_2 [25]) for 11 days in the NASA Glenn Extreme Environments Rig (GEER) [Fig. 2(a)] [26]. The length of 11 days excludes ramp up and cool down times, and is pre-determined by the test facility. A burn-in effect was observed in the transistor characteristics over the first day of the test, where $I_{D,max}$ started from 5 mA/mm (first instance of Venus surface conditions being met) and experienced large fluctuation before settling down at 30 mA/mm (at the time instance defined as day 0). In this letter, the data presented is taken from the remaining 10 days. An automated setup ensured that *in-situ* measurements of the DUT could be made at regular time intervals (≈ 70 min.). Given that the measurement setup was shared among several devices (through a switching matrix), the DUT of this work was left unbiased during each measurement. A comparison

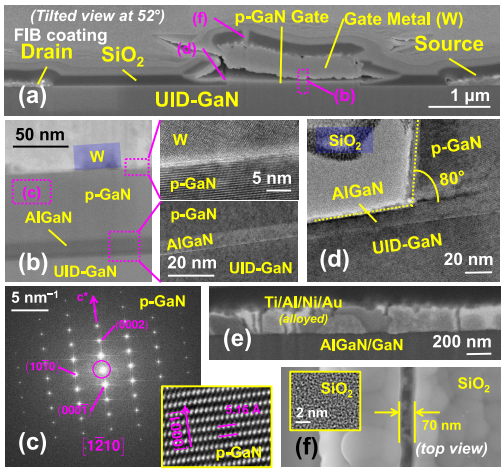

Fig. 3. Advanced microscopy investigation of the device after test. (a) FIB cross-sectional image of the DUT after the testing. (b) Zoom-in view of an intact region of the W/p-GaN/AlGaN/GaN structure (HAADF-STEM). The interfaces are shown in the insets (TEM). (c) Crystallinity (reciprocal lattice) of p-GaN (FFT of TEM). The inset shows the corresponding HRTEM image. (d) Sidewall of the p-GaN-gate region (TEM). (e) Drain contact located on the AlGaN/GaN surface (SEM). The original p-GaN on top of AlGaN was etched to expose the AlGaN surface for formation of ohmic contacts. (f) Small crack in the SiO_2 layer (top view, SEM). The inset shows the amorphous SiO_2 (TEM). All images are cross-sections unless otherwise stated. (FIB: focused ion beam; SEM: scanning electron microscope; TEM: transmission electron microscope; HAADF-STEM: high-angle annular dark-field scanning TEM; FFT: fast Fourier transform; HRTEM: high resolution TEM; UID: unintentionally doped.)

of the DC characteristics [Fig. 2(b)–(c)] reveals that good transistor operation was maintained at the end of the test. The chamber temperature and pressure were accurately maintained over the duration of the test [Fig. 2(d)(i)–(ii)]. $I_{D,max}$ of the packaged DUT (30 mA/mm) was lower than that of the bare die DUT (50 mA/mm), likely due to the degradation of the packaging (e.g. bond pad) [19].

The transistor performance metrics over time during the harsh environment stress are presented in Fig. 2(d)(iii)–(vii). A stable V_{TH} of $0.9 \sim 1$ V (E-mode) was maintained. Assuming $V_{DD} = 5$ V operation and no V_{SS} [22], the peak-to-peak variation (< 0.09 V) corresponds to 1.8 % of the rail-to-rail voltage. The current decreased by < 5.3 mA/mm (18 %), and R_{ON} increased by 9 Ω·mm (12 %), likely caused by degradation of the intrinsic transistor (e.g. ohmic contacts, two-dimensional electron gas channel) and bond pad in the test environment. A stable gate leakage (< 0.1 mA/mm variation, 12 %) and current ON-OFF ratio (< 5 % variation in terms of order of magnitude, limited by gate leakage) was maintained.

At the end of the test, the DUT was characterized using advanced microscopy. The device structure was found to be largely intact [Fig. 3(a)]. The p-GaN-gate region deserves special attention because it enables E-mode operation of the DUT, but the effect of harsh environment conditions has not been well studied. A p-GaN/AlGaN/GaN heterostructure was maintained, as reflected in the smooth interface between the epitaxial layers [Fig. 3(b)], and the crystallinity in p-GaN [Fig. 3(c)]. No noticeable degradation was found in the etched sidewall and AlGaN surface (etch stop layer) [Fig. 3(d)]. Similarly, the Ti/Al/Ni/Au contacts remained structurally intact [Fig. 3(d)–(e)], though it has been noted in other works that

TABLE I
ROBUSTNESS STUDIES OF GAN HEMTS IN HARSH ENVIRONMENT.

E/D-mode	Epitaxial Structure	Reference	Temp. (°C)	Ambient	Duration (h)	$\Delta I_{D,max}$ (%) [2]	ΔV_{th} (V) [2]
D	AlGaN /GaN	[7]	250	5% H_2/95% N_2	24	3	0.2
		[28]	400	Air	25	72	1.4
		[29]	175	N.A.	500	5	0.1
		[30]	525	N.A.	25	10	0.6
	InAlN /GaN	[31]	900	Vacuum	50	100	N.A.
		[6]	1000	Vacuum	25	55	0.3
		[2]	465	Venus	240	30	0.04
E	p-GaN /AlGaN /GaN	[32]	125	N.A.	5000	N.A.	0.15
		[33]	85	High humidity	1000	N.A.	1
		[19]	500	N_2	24	35	0.05
		This Work	**460**	**Venus (complete chemical env.)**	**240**	**18**	**0.09**

[1] Duration of *in-situ* measurement at the specified HT. [2] Peak-to-peak data across the duration of test at the specified temperature. Values, if not explicitly reported, are based on best estimates from the published data.

prolonged HT exposure might lead to degradation [27]. A small crack (width 70 nm) was found in the SiO_2 layer [Fig. 3(f)], likely resulting from a mismatch in the thermal expansion coefficient between W (gate metal) and the surrounding SiO_2. As compared to [19], W remained intact despite the presence of corrosive gases (e.g. SO_2), which could be attributed to the passivation.

The robustness of the proposed transistor [Fig. 2(d)] was benchmarked against similar studies of GaN HEMTs in Table I [2], [6], [7], [19], [28]–[33]. To the best of the authors' knowledge, this is the first study of an E-mode GaN transistor working above 300 °C, in high pressure and under a highly harsh environment (simulated Venus atmosphere). The reported transistor features competitive robustness, as reflected in the relatively small degradation in both $I_{D,max}$ and V_{TH}.

V. CONCLUSION

An E-mode GaN transistor technology was proposed and characterized up to 500 °C. Its robustness in harsh environment was evaluated through both *in-situ* electrical characterization, and comprehensive microscopy of the epitaxial and device structures. This work demonstrated continued operation of the transistor over 10 days in simulated Venus condition, while slight degradations of transistor operation and structure were observed. The results establish the proposed GaN technology a strong contender for harsh environment mixed-signal electronics. This study also offers insights to p-GaN-gate HEMTs for harsh environment power electronics.

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REFERENCES

[1] P. Neudeck, R. Okojie, and L.-Y. Chen, "High-temperature electronics - a role for wide bandgap semiconductors?" *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1065–1076, June 2002. doi: 10.1109/JPROC.2002.1021571

[2] S. R. Eisner, H. S. Alpert, C. A. Chapin, A. S. Yalamarthy, P. F. Satterthwaite, A. Nasiri, S. Port, S. Ang, and D. G. Senesky, "Extended exposure of gallium nitride heterostructure devices to a simulated venus environment," in *2021 IEEE Aerospace Conference (50100)*, March 2021. doi: 10.1109/AERO50100.2021.9438131 pp. 1–12.

[3] K. H. Teo, Y. Zhang, N. Chowdhury, S. Rakheja, R. Ma, Q. Xie, E. Yagyu, K. Yamanaka, K. Li, and T. Palacios, "Emerging GaN technologies for power, RF, digital, and quantum computing applications: Recent advances and prospects," *Journal of Applied Physics*, vol. 130, no. 16, p. 160902, October 2021. doi: 10.1063/5.0061555

[4] W. Sui, H. Wang, J. Lee, A. Qamar, M. Rais-Zadeh, and P. X.-L. Feng, "AlScN-on-SiC thin film micromachined resonant transducers operating in high-temperature environment up to 600 °C," *Advanced Functional Materials*, vol. 32, no. 34, p. 2202204, 2022. doi: 10.1002/adfm.202202204

[5] Y. Zhao, M. Xu, X. Huang, J. Lebeau, T. Li, D. Wang, H. Fu, K. Fu, X. Wang, J. Lin, and H. Jiang, "Toward high efficiency at high temperatures: Recent progress and prospects on InGaN-based solar cells," *Materials Today Energy*, vol. 31, p. 101229, Jan 2023. doi: 10.1016/j.mtener.2022.101229

[6] D. Maier, M. Alomari, N. Grandjean, J.-F. Carlin, M.-A. Diforte-Poisson, C. Dua, S. Delage, and E. Kohn, "InAlN/GaN HEMTs for operation in the 1000 °C regime: A first experiment," *IEEE Electron Device Letters*, vol. 33, no. 7, pp. 985–987, July 2012. doi: 10.1109/LED.2012.2196972

[7] P. Waltereit, W. Bronner, R. Quay, M. Dammann, M. Cäsar, S. Müller, R. Reiner, P. Brückner, R. Kiefer, F. van Raay, J. Kühn, M. Musser, C. Haupt, M. Mikulla, and O. Ambacher, "GaN HEMTs and MMICs for space applications," *Semiconductor Science and Technology*, vol. 28, no. 7, p. 074010, jun 2013. doi: 10.1088/0268-1242/28/7/074010

[8] Q. Xie, N. Chowdhury, A. Zubair, M. S. Lozano, J. Lemettinen, M. Colangelo, O. Medeiros, I. Charaev, K. K. Berggren, P. Gumann, D. Pfeiffer, and T. Palacios, "NbN-gated GaN transistor technology for applications in quantum computing systems," in *2021 Symposium on VLSI Technology*, June 2021, pp. T10–3.

[9] K. Fu, H. Fu, X. Huang, T.-H. Yang, H. Chen, I. Baranowski, J. Montes, C. Yang, J. Zhou, and Y. Zhao, "Threshold switching and memory behaviors of epitaxially regrown GaN-on-GaN vertical p-n diodes with high temperature stability," *IEEE Electron Device Letters*, vol. 40, no. 3, pp. 375–378, March 2019. doi: 10.1109/LED.2019.2891391

[10] B. Wang, R. Zhang, H. Wang, Q. He, Q. Song, Q. Li, F. Udrea, and Y. Zhang, "Dynamic gate breakdown of p-gate GaN HEMTs in inductive power switching," *IEEE Electron Device Letters*, vol. 44, no. 2, pp. 217–220, Feb 2023. doi: 10.1109/LED.2022.3227091

[11] A. Li, Y. Shen, Z. Li, F. Li, R. Sun, I. Z. Mitrovic, H. Wen, S. Lam, and W. Liu, "A 4-transistor monolithic solution to highly linear on-chip temperature sensing in GaN power integrated circuits," *IEEE Electron Device Letters*, vol. 44, no. 2, pp. 333–336, Feb 2023. doi: 10.1109/LED.2022.3226684

[12] G. Tang, A. M. H. Kwan, R. K. Y. Wong, J. Lei, R. Y. Su, F. W. Yao, Y. M. Lin, J. L. Yu, T. Tsai, H. C. Tuan, A. Kalnitsky, and K. J. Chen, "Digital integrated circuits on an E-mode GaN power HEMT platform," *IEEE Electron Device Letters*, vol. 38, no. 9, pp. 1282–1285, Sep. 2017. doi: 10.1109/LED.2017.2725908

[13] N. Chowdhury, Q. Xie, M. Yuan, K. Cheng, H. W. Then, and T. Palacios, "Regrowth-free GaN-based complementary logic on a Si substrate," *IEEE Electron Device Letters*, vol. 41, no. 6, pp. 820–823, June 2020. doi: 10.1109/LED.2020.2987003

[14] L. Zhang, Z. Zheng, Y. Cheng, Y. H. Ng, S. Feng, W. Song, T. Chen, and K. J. Chen, "SiN/in-situ-GaON staggered gate stack on p-GaN for enhanced stability in buried-channel GaN p-FETs," in *2021 IEEE International Electron Devices Meeting (IEDM)*, Dec 2021. doi: 10.1109/IEDM19574.2021.9720653 pp. 5.3.1–5.3.4.

[15] Q. Xie, M. Yuan, J. Niroula, B. Sikder, J. A. Greer, N. S. Rajput, N. Chowdhury, and T. Palacios, "Highly scaled GaN complementary technology on a Silicon substrate," *IEEE Transactions on Electron Devices*, vol. 70, no. 4, pp. 2121–2128, 2023. doi: 10.1109/TED.2023.3247684

[16] M. Yuan, Q. Xie, K. Fu, T. Hossain, J. Niroula, J. A. Greer, N. Chowdhury, Y. Zhao, and T. Palacios, "GaN ring oscillators operational at 500 °C based on a GaN-on-Si platform," *IEEE Electron Device Letters*, vol. 43, no. 11, pp. 1842–1845, Nov 2022. doi: 10.1109/LED.2022.3204566

[17] R. Wang, L. Jia, X. Gao, J. He, Z. Cheng, Z. Liu, L. Zhang, and Y. Zhang, "Dynamic performance analysis of logic gates based on p-GaN/AlGaN/GaN HEMTs at high temperature," *IEEE Electron Device Letters*, pp. 1–1, 2023. doi: 10.1109/LED.2023.3267835

[18] Q. Xie, M. Yuan, J. Niroula, B. Sikder, S. Luo, K. Fu, N. S. Rajput, A. B. Pranta, P. Yadav, Y. Zhao, N. Chowdhury, and T. Palacios, "Towards DTCO in high temperature GaN-on-Si technology: Arithmetic logic unit at 300 °C and CAD framework up to 500 °C," in *2023 Symposium on VLSI Technology and Circuits*, June 2023. doi: 10.23919/VLSITechnologyandCir57934.2023.10185364

[19] M. Yuan, Q. Xie, J. Niroula, M. F. Isamotu, N. S. Rajput, N. Chowdhury, and T. Palacios, "High temperature robustness of enhancement-mode p-GaN-Gated AlGaN/GaN HEMT technology," in *2022 IEEE 8th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Nov 2022. doi: 10.1109/WiPDA56483.2022.9955304

[20] Q. Xie, M. Yuan, J. Niroula, J. A. Greer, N. S. Rajput, N. Chowdhury, and T. Palacios, "Highly-scaled self-aligned GaN complementary technology on a GaN-on-Si platform," in *2022 International Electron Devices Meeting (IEDM)*, Dec 2022. doi: 10.1109/IEDM45625.2022.10019401 pp. 35.3.1–35.3.4.

[21] A. M. Potts, S. Bajaj, D. R. Daughton, A. A. Allerman, A. M. Armstrong, T. Razzak, S. H. Sohel, and S. Rajan, "$Al_{0.7}Ga_{0.3}N$ MESFET with all-refractory metal process for high temperature operation," *IEEE Transactions on Electron Devices*, vol. 68, no. 9, pp. 4278–4282, Sep. 2021. doi: 10.1109/TED.2021.3095138

[22] M. Yuan, Q. Xie, J. Niroula, N. Chowdhury, and T. Palacios, "GaN memory operational at 300 °C," *IEEE Electron Device Letters*, vol. 43, no. 12, pp. 2053–2056, Dec 2022. doi: 10.1109/LED.2022.3218671

[23] N. Xu, R. Hao, F. Chen, X. Zhang, H. Zhang, P. Zhang, X. Ding, L. Song, G. Yu, K. Cheng, Y. Cai, and B. Zhang, "Gate leakage mechanisms in normally off p-GaN/AlGaN/GaN high electron mobility transistors," *Applied Physics Letters*, vol. 113, no. 15, p. 152104, Oct 2018. doi: 10.1063/1.5041343

[24] H. S. Alpert, C. A. Chapin, K. M. Dowling, S. R. Benbrook, H. Köck, U. Ausserlechner, and D. G. Senesky, "Sensitivity of 2DEG-based Hall-effect sensors at high temperatures," *Review of Scientific Instruments*, vol. 91, no. 2, p. 025003, Feb 2020. doi: 10.1063/1.5139911

[25] P. G. Neudeck, L. Chen, R. D. Meredith, D. Lukco, D. J. Spry, L. M. Nakley, and G. W. Hunter, "Operational testing of 4H-SiC JFET ICs for 60 days directly exposed to Venus surface atmospheric conditions," *IEEE Journal of the Electron Devices Society*, vol. 7, pp. 100–110, 2019. doi: 10.1109/JEDS.2018.2882693

[26] T. Kremic, D. Vento, N. Lalli, and T. Palinski, "Extreme environment simulation - current and new capabilities to simulate Venus and other planetary bodies," in *2014 IEEE Aerospace Conference*, March 2014. doi: 10.1109/AERO.2014.6836350 pp. 1–9.

[27] Z. Dong, J. Wang, C. Wen, S. Liu, R. Gong, M. Yu, Y. Hao, F. Xu, B. Shen, and Y. Wang, "High temperature induced failure in Ti/Al/Ni/Au Ohmic contacts on AlGaN/GaN heterostructure," *Microelectronics Reliability*, vol. 52, no. 2, pp. 434–438, 2012. doi: 10.1016/j.microrel.2011.09.021

[28] S. Kargarrazi, A. S. Yalamarthy, P. F. Satterthwaite, S. W. Blankenberg, C. Chapin, and D. G. Senesky, "Stable operation of AlGaN/GaN HEMTs for 25 h at 400 °C in air," *IEEE Journal of the Electron Devices Society*, vol. 7, pp. 931–935, 2019. doi: 10.1109/JEDS.2019.2937008

[29] M. Mao, S. Tang, Z. Wang, R. Deng, C. Deng, S. Chen, and Y. Ren, "Effect of temperature cycling, high temperature storage and steady-state operation life test on reliability of GaN HEMTs," in *2021 22nd International Conference on Electronic Packaging Technology (ICEPT)*, Sep. 2021. doi: 10.1109/ICEPT52650.2021.9568117 pp. 1–4.

[30] H. Lee, H. Ryu, and W. Zhu, "Thermally hardened AlGaN/GaN MIS-HEMTs based on multilayer dielectrics and silicon nitride passivation," *Applied Physics Letters*, vol. 122, no. 11, p. 112103, March 2023. doi: 10.1063/5.0134475

[31] D. Maier, M. Alomari, N. Grandjean, J.-F. Carlin, M.-A. Diforte-Poisson, C. Dua, A. Chuvilin, D. Troadec, C. Gaquière, U. Kaiser, S. L. Delage, and E. Kohn, "Testing the temperature limits of GaN-based HEMT devices," *IEEE Transactions on Device and Materials Reliability*, vol. 10, no. 4, pp. 427–436, Dec 2010. doi: 10.1109/TDMR.2010.2072507

[32] E. Dechant, N. Seliger, and R. Kennel, "Power cycling and temperature endurance test of a GaN switching cell with substrate integrated chips," *Microelectronics Reliability*, vol. 100-101, p. 113372, Sep 2019. doi: 10.1016/j.microrel.2019.06.064 30th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis.

[33] J. A. Rodriguez, T. Tsoi, D. Graves, and S. B. Bayne, "Evaluation of GaN HEMTs in H^3TRB reliability testing," *Electronics*, vol. 11, no. 10, May 2022. doi: 10.3390/electronics11101532