A HIGH PERFORMANCE DIELECTRIC MEASUREMENT SYSTEM

by

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ABSTRACT

Measurements of the low-frequency dielectric properties of polymers can provide information useful for process control applications as well as scientific studies of materials. This thesis develops techniques that provide high performance in a dielectric measurement microsensor system consisting of an integrated circuit sensor chip together with associated support instrumentation.

The goal of this thesis was to improve on an existing system that used an impedance-divider sensor and a zero-crossing phase detector. Three different sensor circuit configurations have been analyzed and a sampled-data digital signal processing system has been developed. The closed-loop integrator and monolithic bridge circuits both offer increased resolution over the conventional impedance divider. but suffer from other disadvantages. The digital signal processing system includes a sensor excitation waveform synthesizer and synchronous data acquisition. The sensor response at a particular frequency is obtained from the sampled data using a digital correlation algorithm executed on a microcomputer. The excitation waveform can be constructed from multiple frequency components and the signal analysis can check for linearity in each system component.

The final system achieves a factor of ten better resolution for low loss factors than was previously available. The low frequency measurement limit has been extended by more than two orders of magnitude, and the measurement speed has been increased by a typical factor of five.

Thesis Supervisor: Dr. Stephen D. Senturia

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CHAPTER 0

Introduction

This thesis presents techniques developed for achieving high performance in a dielectric measurement system consisting of an integrated microsensor chip and signal analysis instrumentation.

The starting point for the work documented here is the original microdielectrometer [1] developed for monitoring the dielectric properties of epoxy resins during a curing reaction. The key element of the microdielectrometer is an integrated circuit microsensor. The sensor chip includes a planar electrode structure with known geometry, and is placed in contact with or embedded within the sample being examined. Also included on the chip are MOS field effect transistors operating at extremely high input impedance levels, that serve to buffer the sensor response signal. The photolithographic process used to fabricate the electrodes insures precise, reproducible geometry of the electrode system; and this allows the sensor to be used for calibrated quantitative dielectric measurements.

The original microdielectrometer was comprised of several subsystems in addition to the monolithic sensor. These subsystems include the sensor excitation signal

source, a magnitude and phase meter for monitoring the sensor response, and tables incorporating the calibration functions for the sensor chip.

The motivation for this thesis work was the need for better microdielectric measurement data for continuing resin cure research. Better experimental data required the development of better instrumentation. There was special interest in two areas: making measurements of lower dielectric loss factors, and extending the low frequency range of the instrumentation. As an example, a low conductivity resin near the end of cure may have a loss tangent of 0.001, and a permittivity of about 3. The goal of making measurements of this 0.003 loss factor sample requires development of phase measurement instrumentation with a resolution of 0.06 degree.

The microdielectrometer sensor monitors charge, and has no intrinsic lower frequency limit. Measurements at lower frequencies allow lower conductivity samples to be studied. A second goal therefore was to develop signal analysis instrumentation to exploit the sensor low frequency capability.

The thesis work began with a review of the subsystems in the microdielectrometer instrument to find opportunities for meeting the above goals. The sensor circuit was studied

to determine if an alternative circuit configuration could relax the phase meter specifications. A test sensor chip was designed to verify the results of the sensor analysis. In parallel with the test sensor design, a digital synchronous excitation-response meter was developed that included special hardware and software for testing both itself and the test sensor. The new meter included a microcomputer controlled programmable waveform synthesizer that forced synchronization between the generated excitation signal and the sampling of the sensor response. Digital signal processing of the response samples using a true correlation algorithm provided excellent noise immunity.

The development of the excitation-response meter included testing to measure both the noise and distortion characteristics of the instrumentation and sensors. Analysis of error sources in the sampled-data meter revealed a potentially significant systematic aliasing error. Interestingly, this error was not detectable by a "loop-back" test that directly connects the synthesizer output to the sampling input of the meter.

One conclusion of the thesis analysis is that the original sensor circuit configuration is best for microdielectrometry. The other sensor designs have marginally better resolution for large loss factors, but do not enhance low loss measurements. Worse, one of these

"virtual ground" techniques (the integrator), is not useable at low frequencies; while the other, the monolithic bridge, suffers from slow measurement speed.

The second major thesis result is the development and characterization of a sampled data excitation-response instrument. The correlation algorithm implemented in the meter is an "optimum" receiver function and has excellent noise rejection. The instrument can measure to better than 0.01 decibel and 0.1 degree over the 40 decibel signal range produced by the sensor. This is a factor of 10 better phase resolution than what was available in the original microdielectrometer system. The measurement speed has also been increased by a typical factor of 5. The digital waveform generation and sampling, just like the sensor, has no intrinsic low frequency limit. The hardware and software has been designed for use down to 0.005 Hz, a factor of 200 below the capability of the original instrument.

The synchronous excitation waveform generation and response sampling insures excellent absolute phase calibration. The aliasing effects due to the digital synthesis of the excitation waveform are now understood and predictable, and the systematic errors can be reduced to insignificant levels by design.

The development of the excitation-response meter also produced a bonus result. The true correlation function that

was implemented allows the meter to analyze signals equally well at frequencies other than the synthesizer excitation signal. It is possible to look for harmonic or intermodulation tones to directly test the assumption of linearity in each subsection of the microdielectrometer system. As an example, 0.2 percent second order distortion has been measured in the microsensor chips. The multiple frequency capability of the excitation-response instrument can also be used to increase the experimental measurement speed in some cases. This is accomplished by analysing the sensor response to an excitation signal containing several frequency components.

0.1 Organization

Chapter 1 of the thesis presents background information on the history of the sensor and the characteristics of the planar electrode array used in the monolithic design. The original dielectric measurement system is reviewed, and the goals for the new instrument are presented.

Chapter 2 considers the sensor circuitry. The sensor is analyzed as an impedance or admittance measurement device and alternative circuit topologies with different parametric transfer functions are presented. The advantages and disadvantages of each category are compared from the perspective of the performance of the complete monitoring system.

Measurement and analysis instrumentation is the topic of chapter 3. The sensor exhibits a test-sample-dependent AC transfer function that is monitored by measuring the response to an excitation waveform. Possible choices for the excitation signal and the response receiver are considered. A high-performance sampled-data digital signal processing design is presented. An analysis of the sampled data design exposes the possibility of significant errors due to aliasing effects. Techniques for limiting these errors are discussed.

Chapter 4 is devoted to a performance analysis of the new microdielectrometer system. Experimental measurements of the system noise and distortion characteristics are presented. These measurements are reconciled with expected noise sources and the noise rejection of the signal processing software. The capability of the system for detecting nonlinear sample effects is demonstrated. Finally, the measurement speed of the system and further opportunities for faster computation are discussed.

Chapter 5 comprises a summary of the results of the work.

CHAPTER 1

Background

This chapter reviews the development of dielectric measurement techniques based on the microdielectrometer, a semiconductor sensor and related instrumentation.

The first section presents a brief history of the development of the sensor chip, and initial applications of the sensor. Following discussion centers on the characteristics of the electrode structure used in the microsensor. The third section describes the original microdielectric measurement system, and the goals selected for the new system.

1.1 History

Since the development of integrated circuit fabrication technology around 1957, the number of components per chip has increased dramatically [2]. The size, power consumption and, particularly, cost of a system has been impressively reduced. Advances have been especially evident in digital systems, notably in random access memory devices and microprocessors. However, the new capability has also been applied in the analog domain, leading to the development of integrated sensors.

Sensor systems have benefitted in two ways from advances in microfabrication. First, developments in semiconductor processing techniques have provided the means to fabricate innovative sensor structures with excellent reproducability. Second, the cost of digital computation has been reduced to such an extent that sensor calibration information and complex digital signal processing software may be incorporated in a sensor system, again removing constraints on the underlying sensor chip design.

A number of environmental characteristics, including temperature, pressure, humidity, acceleration, magnetic fields, and the dielectric properties of polymers can be measured by monolithic sensors [1,3-8]. Dielectric sensors see use in process control applications as well as

scientific studies of the properties of materials. For crosslinking resin curing applications it is desirable that measurements be possible at frequencies in the range of one Hertz, to monitor structural relaxation times of the material during the latter part of the cure. In comparison with conventional parallel plate capacitor dielectric measurement systems, the high impedance monolithic sensor is easily capable of operation in this frequency range. An additional advantage of the planar, monolithic sensor structure in industrial cure monitoring is that stresses in the material will not affect the geometry of the electrodes and dielectric, and the calibration of the sensor will therefore remain valid.

The dielectric sensor studied in this thesis evolved from the charge-flow transistor, itself developed as a smoke or humidity sensor [9]. The charge-flow transistor was designed as a modified MOS field effect transistor, and sensed changes in the sheet resistance of a thin polymer layer that replaced the normal gate electrode and was exposed to the ambient environment. Subsequent investigations centered on the study of epoxy polymerization reactions, and demonstrated a sensor sensitivity to the dielectric properties of a resin during the cure process. The development of a model for the results suggested a modification of the design to separate the sensitive electrode region from the active MOS transistor, and the

inclusion of a second (reference) transistor for differential measurements [5]. A two-dimensional numerical analysis of the electrostatic potentials in the electrode region has provided greater accuracy than the previously used transmission line model [10]. This has provided a calibration of the sensor design and allowed quantitative rather than qualitative studies of dielectric characteristics [11].

1.2 The Sensor Electrode Array

Conventional measurements of the dielectric properties of materials rely on a parallel plate capacitor technique. A thin layer of the dielectric is placed between two sheets of metal foil. A time-varying voltage excitation, often a sinusoidal signal, is impressed across the electrodes and the resulting displacement and conductive currents that flow through the circuit are measured.

The admittance of the system is dependent on the complex dielectric constant of the sample. The permittivity (ε') is the real part of the dielectric constant and arises from the capacitive characteristic of the sample. The loss factor (ε'') is the imaginary component, and is proportional to the AC conductivity of the sample. Both the permittivity and loss factor are, in general, expected to be functions of the excitation frequency.

If the geometry of the electrodes and dielectric is known, the permittivity and loss factor of the material under test can be evaluated (at a particular frequency) from the measured magnitude and phase of the response current in the circuit. In industrial applications the resin is often cured under pressure to remove voids in the structure. The resulting deformation will make the determination of the electrode spacing difficult if a parallel plate

configuration is used. Under these conditions, only the loss tangent (the ratio of the imaginary component to the real component of the dielectric constant) can be determined. The maximum excitation signal field that can be applied to the electrodes, and the maximum reasonable area of the parallel electrodes, together limit the magnitude of the currents that must be measured. For low loss materials, the admittance is proportional to frequency and becomes difficult to measure with conventional instruments at frequencies below 10 Hz.

Interdigitated or comb electrodes avoid the geometry variations of the parallel plate structure. The electrodes are fixed to a rigid, planar substrate, and the material under test forms a semi-infinite medium above the electrodes. The calibration relationship, between the measured magnitude and phase response and the underlying permittivity and loss factor, is more complex than the calibration of the parallel plate system. This disadvantage is outweighed by the predictability and stability of the system. Another advantage of comb electrodes is that the overall structure is thin, a convenience for industrial monitoring of laminate or composite structures.

The remaining limitation on low frequency measurements is addressed by the microdielectrometer structure [10]. The microdielectrometer sensor includes a pair of interdigitated

electrodes with the addition of MOS field effect transistors. The matched pair of transistors, in conjunction with circuitry external to the sensor chip, form a very high impedance buffer for the sensor output signal. The buffer input and other parasitic elements loading the electrode system are all capacitive rather than resistive in nature, so the buffered output signal is proportional to charge and the sensor retains full sensitivity to arbitrarily low frequencies.

1.3 The Original Dielectric Measurement System

The existing microdielectrometer system includes several subsections, including the sensor chip, sensor support circuitry, measurement and analysis instrumentation, and experiment control and data logging.

A sensor chip is the primary transducer, converting the dielectric parameters of interest into modulation of the transconductance of the on-chip MOS transistors. Support circuitry external to the sensor chip applies the electrode excitation signal, establishes the bias conditions of the sensor transistors, and converts the transistor source currents into the response signal. The signal analysis instrumentation measures the magnitude and phase relationship between the excitation and response signals. Further analysis software, containing the sensor calibration functions, converts the magnitude and phase information into the desired permittivity and loss factor. The overall control and data logging functions of the experimental system reside in a desktop computer.

A schematic top view of the existing sensor chip is shown in Figure 1.1 [10]. The large upper region is covered by the interdigitated metal electrode array that forms the sensitive surface of the chip. The lower center portion of the chip is the location of the matched pair of MOS

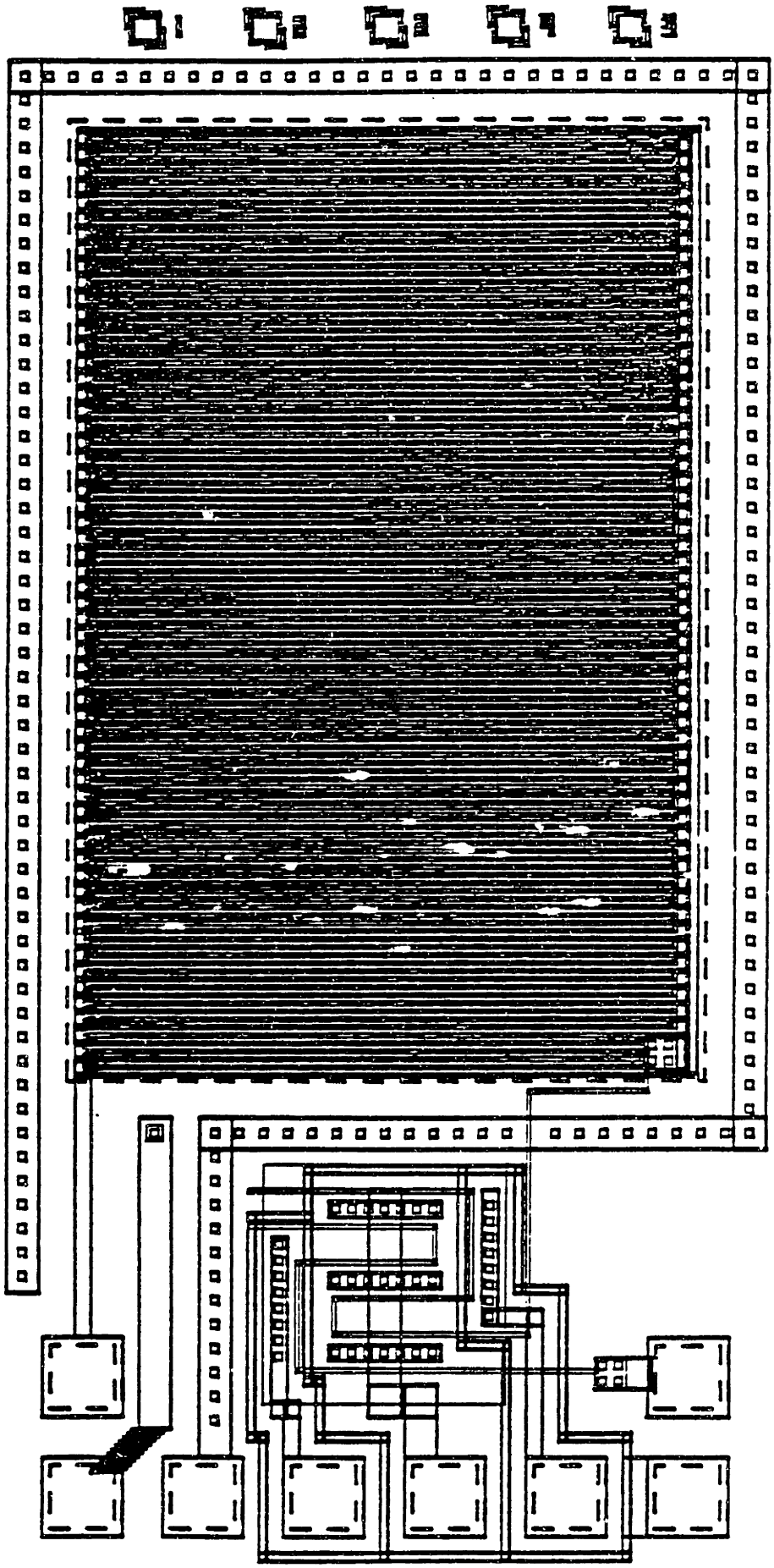


Figure 1.1 Schematic Top View of Sensor Chip [10]

transistors. These transistors are laid out in a serpentined pattern with a common centroid geometry. This layout of the transistors minimizes the differences in their transconductance and threshold characteristics caused by first order gradients in the process parameters, and by any substrate currents coupled in from the electrode array. Details of the design minimize parasitic errors and aid in the mechanical packaging of the sensor [10]. The overall size of the sensor is approximately 4.5 mm by 2.2 mm. The coupling capacitance between the two electrodes when the sensor is located in air is 0.5 pf. If this sensor is embedded in a material with a permittivity of 3 (typical for epoxy resins at the end of cure) and measured at a frequency of 0.1 Hz, a loss factor of 0.01 corresponds to a resistance between the electrodes of about 10^{15} ohms.

As mentioned earlier, the existing sensor includes two transistors on the chip are used together with an external feedback loop to minimize the effects of transistor parameter variations. The circuit is shown schematically in Figure 1.2 [12]. Only the two transistors and the electrode structure at the gate of the leftmost transistor are included on the sensor chip. The remainder of the circuitry resides in a separate enclosure with benign environmental conditions. The two transistors are depletion mode devices, operated in the unsaturated region with a source to

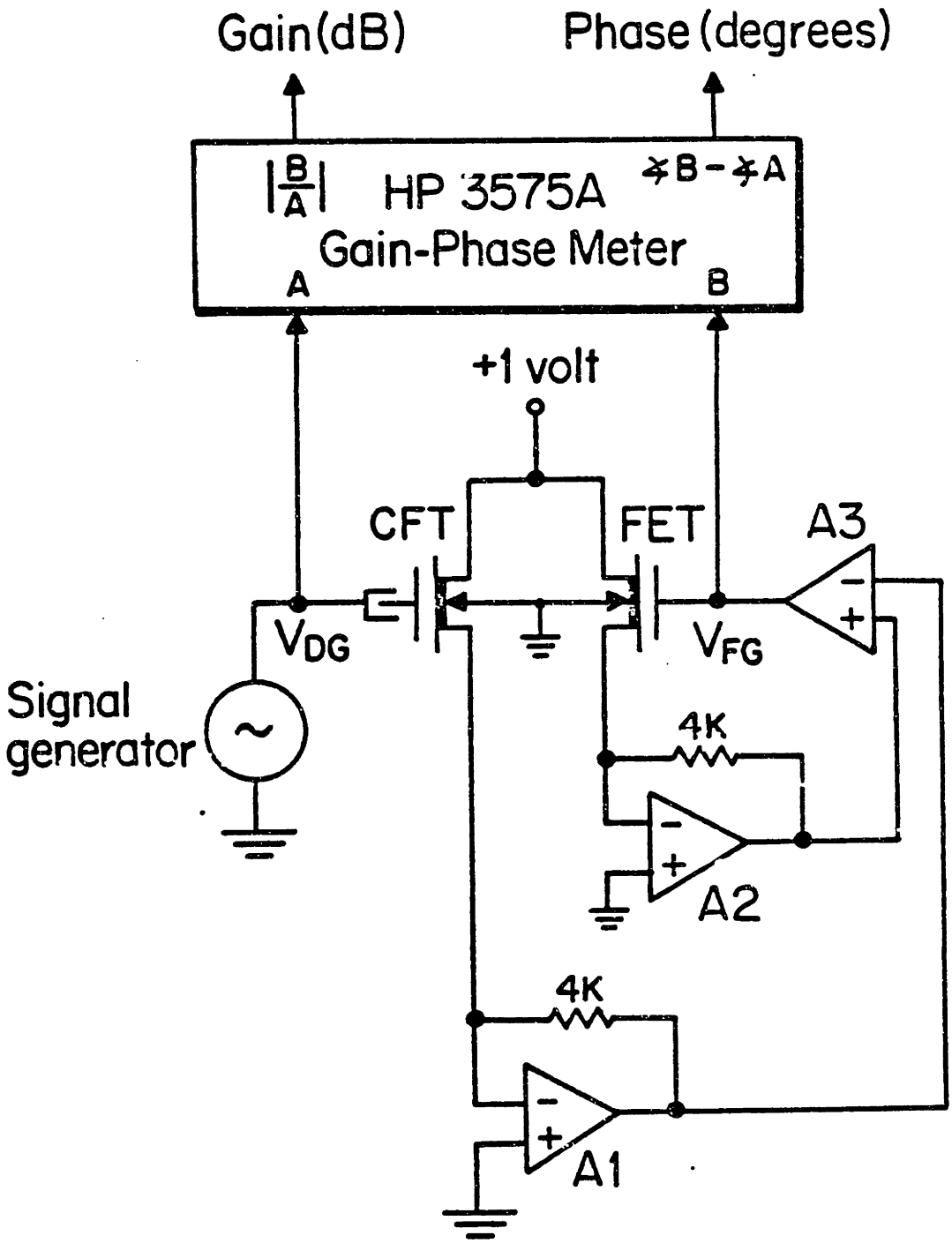


Figure 1.2 Original Sensor, Interface Circuit and Gain-Phase Meter [12]

substrate voltage of virtually zero, a zero mean gate voltage, and a small drain bias.

The operational amplifiers A1 and A2 have resistive feedback and operate as transresistance elements, providing output voltages proportional to the source currents of their respective transistors. The non-inverting inputs of A1 and A2 are at ground, so (assuming the circuit is not saturated) the sources of the two sensor transistors are kept at a virtual ground potential. Amplifier A3 is an error amplifier and drives the gate of the reference transistor from the amplified difference between the output voltages of amplifiers A1 and A2. The feedback loop therefore attempts to equalize the source currents in the chip transistors. Since source, drain and substrate potentials of the two transistors are identical and the drain currents are identical, then to the degree that the transistors are matched, their gate voltages will also be equal. If changes in the characteristics of the transistors occur from chip to chip, or from (for example) changes in the temperature of the experiment, the matched transistors should be perturbed equivalently and the gate voltages should remain equal.

The entire conventional system from the floating gate electrode onward can be viewed as an extremely high input impedance voltage follower. If a sinusoidal excitation waveform is applied to the input, the magnitude and phase of

the output signal (at the gate of the second transistor) with respect to the excitation signal is dependent on the real and imaginary parts of the dielectric constant of the material placed on the electrodes. The conductivity of the material under test dominates parasitic leakage currents that would accumulate on the input of the voltage follower. Therefore, the mean voltage across the electrodes is zero, and if the excitation signal has zero mean value the output signal will also have a zero offset voltage.

The excitation signal is generated by an HP-3325A function generator. The relative magnitude and phase of the excitation and response signals are measured by an HP-3575A gain-phase meter and transmitted to an HP-85 desktop computer, the system controller. Software resident in the controller allows the experimenter to select the parameters for the experiment including the excitation frequencies of interest, the time between measurements and the total length of the experiment. The experiment can then proceed without any necessary intervention by the experimenter.

The lower limit of measurement frequencies is not constrained by the sensor chip or circuit design, but rather by the gain-phase meter. The HP-3575A has a low frequency limit of 1 Hz, and a newer instrument, the HP-4192A impedance analyzer will not operate below 5 Hz. Lower frequency measurements, to at least as low as 0.1 Hz, are

useful when probing the structural relaxation of cured polymers or the low temperature properties of resins. The dynamics of the sensor support circuitry and the phase shift that is introduced limits high frequency measurements to the 10 kHz range. This is currently considered sufficient.

The resolution of measurements of permittivity and loss factor is dependent on both the sensor design and the response signal measurement instrumentation. The sensor determines the sensitivity of the transformation that occurs between the sample dielectric constant parameters and the resultant magnitude and phase response. The magnitude and phase perturbations must then be accurately measured by the gain-phase meter. The published specifications for the HP-3575A gain-phase meter are summarized in Table 1.1 for the 40 decibel dynamic range of signals that the sensor produces [13].

As will be seen in the sensor analysis of chapter 2, significantly better resolution is desirable in both the magnitude and phase measurement. The goal selected for the new excitation-response meter that will be developed is a magnitude resolution of 0.01 decibel and a phase resolution of 0.1 degree. This measurement performance translates into a loss factor sensitivity limit of 0.005 for a sample dielectric medium that has a permittivity of 3 (typical for

TABLE 1.1

HP-3575A Gain-phase Meter Specifications [13]

(signal between 0 and -40 decibels relative to 1 volt)

Frequency	Magnitude (decibels)	Phase (degrees)
1 Hz	± 1.0	± 1.0
10 Hz	± 1.0	± 0.5
100 Hz	± 1.0	± 0.5
1000 Hz	± 1.0	± 1.0
10000 Hz	± 1.0	± 2.0

epoxy resin at the end of cure), and represents more than an order of magnitude increase in performance.

The measurement rate is eventually limited by the time needed to acquire a sample of the response signal. A reasonable minimum aperture time that allows rejection of DC offsets is to sample for one cycle of the excitation frequency. The analog measurement technique used in the HP-3575A meter reduces noise by averaging with long time constant filters, and a recommended minimum acquisition time for a 1 Hz signal is 30 seconds.

CHAPTER 2

Sensor Design

This chapter discusses alternative dielectric sensor circuitry designs. The first section presents the structure and general characteristics of three basic circuit categories that can be used for impedance measurements. Next follows an evaluation of the measurement sensitivity of each configuration. The mapping of dielectric properties of the material under test (permittivity and loss factor) to the measured quantities (magnitude and phase) is nonlinear, and the mapping varies for the different measurement categories. Thus for a particular magnitude and phase resolution in the following measurement instrumentation, the choice of sensor design will affect the resolution in the inferred dielectric properties. The third section contains a summary and evaluation of the design issues, and the last section presents a description of a test sensor chip that demonstrates the results of the engineering analysis.

2.1 Impedance Measurement Techniques

The microdielectrometer sensor is fundamentally a (complex) impedance or admittance measurement device. Admittance measurement involves a determination of the incremental current-voltage relationship of a system, and a classic implementation would apply a voltage to the system under test and measure the response current. Typically a second, reference, component is connected so that identical current must flow through the unknown and known admittances. An excitation voltage is applied to the system, and the measured response is the voltage across one or the other of the admittances.

For dielectric measurements, where the unknown admittance is generally capacitive, it is appropriate to use a capacitor as the reference component. Though the currents through the system will scale with the excitation frequency, to the degree that the sample is a fixed value pure capacitance, the response voltage magnitude will be unaffected by the frequency selection. This is an important advantage for the microdielectrometer, where frequency may be adjusted over a six decade range.

Several circuit configurations are available to implement the general admittance or impedance measurement described above. These techniques can be segregated into

three categories: the open-loop or divider, closed-loop or integrator, and the bridge or modified bridge. Each one of the different implementations has characteristics that may make it unsuitable for a particular application, as well as advantages and disadvantages in sensitivity and complexity. The three techniques will be discussed from the perspective of their use in a microsensor for dielectric measurements.

2.1.1 Open-Loop Impedance Divider

The open-loop impedance divider is schematically shown in Figure 2.1. The excitation signal (a sinusoid at the frequency of interest, for example) is applied to one electrode of the sensor structure (often called the driven gate [1]). The parasitic capacitance connected between ground and the other sensor electrode (the floating gate) includes the input capacitance of the buffer amplifier and any other interconnection capacitances. The buffer amplifier generates a low impedance facsimile of the voltage on the floating node that is available for measurement and analysis.

The planar electrode structures and associated sample used in microdielectrometry can only be modeled as distributed systems, rather than simple resistor-capacitor networks. However, the magnitude and phase of the output signal with respect to the excitation signal will nevertheless be a function of the real and imaginary parts

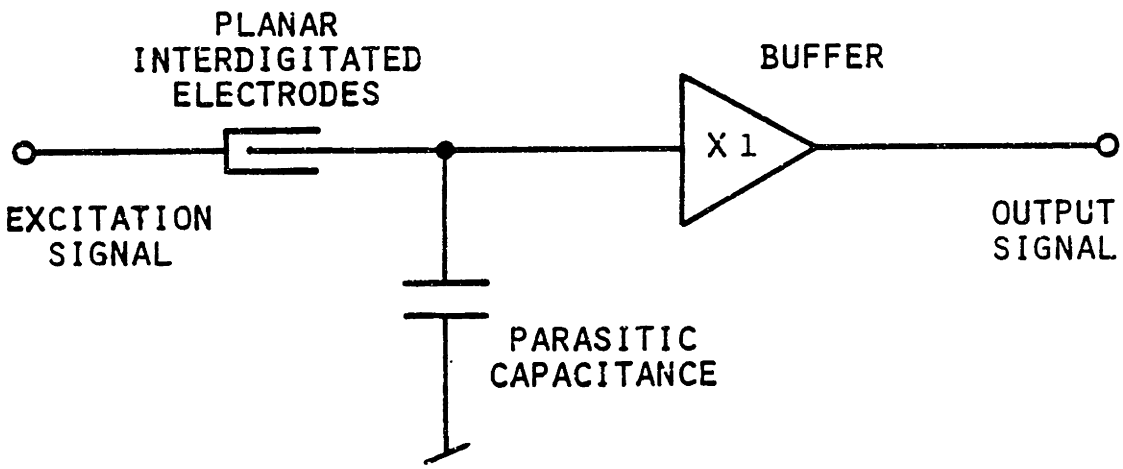


Figure 2.1 Open-Loop Impedance Divider with Buffer

of the dielectric constant of the material placed on the electrodes. The impedance at the floating node is very high, particularly at the lower excitation frequencies. The buffer amplifier must have an extremely large input resistance, and be in close proximity to the electrode structure to avoid parasitic conductances between the floating gate node and other circuit nodes. In microdielectrometer sensors this requirement is satisfied by including MOS field effect transistors with the electrode array on the same silicon sensor chip. The transistors form the input stage of the buffer amplifier, and fulfill the input impedance requirement.

In conventional MOS circuit design, the use of a "floating" node is not useful. Parasitic sources cause the accumulation of charge on such a node, eventually leading to saturation of the system. Therefore a conductive path must be provided from any given node to a voltage source. In the sensors discussed here, the conductive element is the material under test, connecting the otherwise floating node to the excitation source. Though the conductivity of the material may be quite low, it dominates any parasitic sources and maintains the mean potential on the otherwise floating node equal to the mean voltage of the excitation source. Net charge transfer from the excitation electrode through the sample to ground may lead to electrochemical attack of the electrodes as well as affecting the sample

under test. To minimize such errors, the excitation source should be a zero mean signal.

2.1.2 Closed-Loop Admittance Measurement

A closed-loop measurement technique using an integrator is shown in Figure 2.2. As in the impedance divider design, the excitation signal is applied to the material under test. Currents flowing from the second (floating) electrode are integrated on the feedback capacitor and generate the output signal.

There are two principal advantages of this technique when compared with the impedance divider. First, variations in the (perhaps difficult to calibrate) parasitic capacitances associated with the sensitive node do not affect the output signal. The loop transmission provided by the integrator acts to maintain the "floating" node at ground potential. Both the parasitic capacitance and the gate capacitance of the (MOS) input transistor in the operational amplifier have minimal effect on the signal, and all charge from the sensor electrode is deposited on the integrator feedback capacitor. The effect of the stray capacitance is to reduce the loop transmission, and this does not affect the output signal if the amplifier has sufficient gain at the signal frequency.

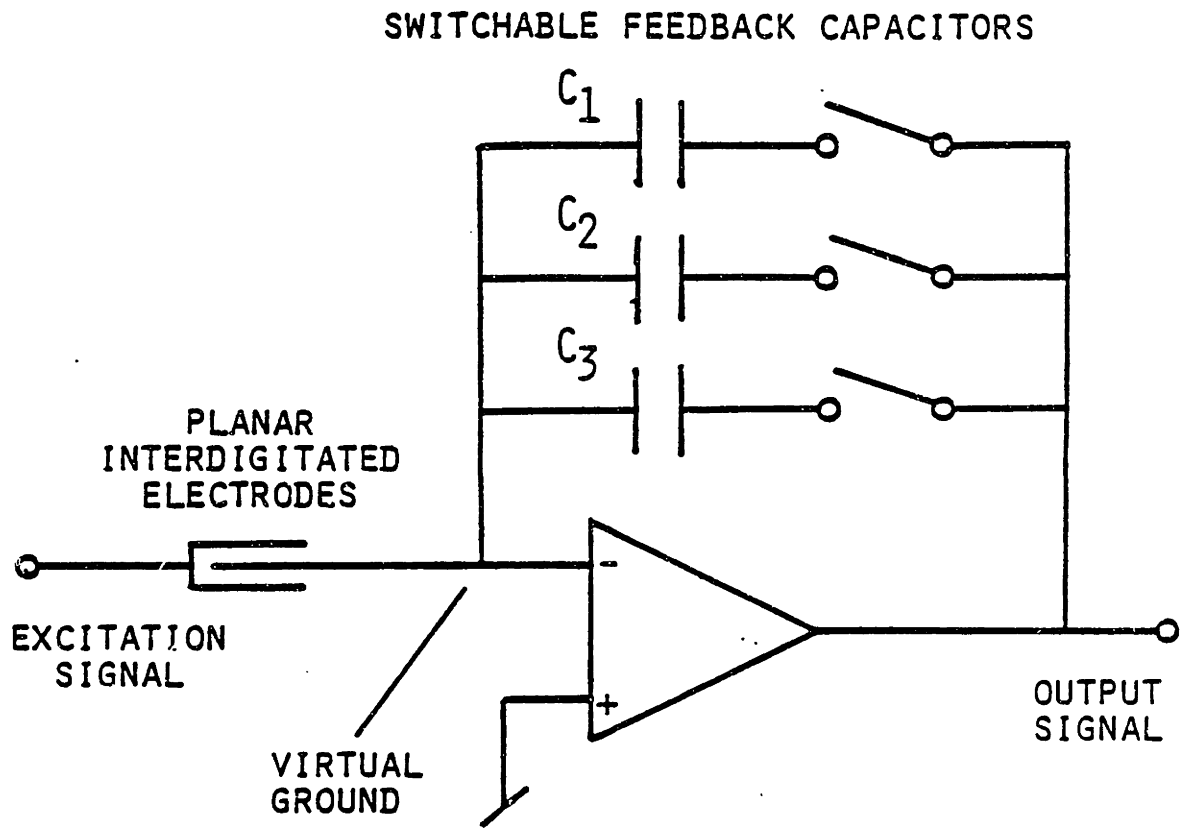


Figure 2.2 Closed-Loop Measurement using Integrator

The second advantage of the integrator technique is that the feedback can be selected from a set of capacitors (all on the sensor chip) by analog switches (MOS transistors). This enhancement makes it possible to modify the gain of the system and limit the dynamic range of the output signal, while accommodating changes in test material dielectric properties from chemical reactions, or variations from one material to another.

Since the closed-loop circuit configuration operates as an integrator, input offset voltages in the amplifier will force a current through the sample. This current will be deposited on the feedback capacitor leading to saturation of the system. Additional sources of "offset" voltage include any electrochemical potentials developed in the electrode and sample system. In use, DC offsets have been observed as large as 1 to 2 volts, that have been attributed to electrochemical potentials developed in the electrode and sample system [14]. The conventional approach to avoiding saturation from small offsets is to introduce a resistive feedback path from the output to the inverting input of the operational amplifier. This limits the low frequency gain of the circuit and prevents saturation. The feedback can be provided by a normal linear resistor, or simulated with a switched capacitor filter network [15] in the integrated MOS environment. To avoid degrading the response of the integrator to the desired signals, the feedback resistance

must be significantly larger than the impedance of the dielectric under test. A resistance of this magnitude is not feasible, on or off the chip. Use of a switched capacitor network is also unacceptable, since the junctions in the necessary MOS switches degrade the extremely low leakage required at the virtual ground node.

An alternative technique that can stabilize the integrator offset is to take the time average of the integrator output (ideally zero) and use any error to adjust the offset of the integrator amplifier (at the non-inverting input, for example). The mean signal output can be driven to zero by the use of a second integrator as a filter, connected to the normal signal output. A particularly low offset amplifier is not required for the second amplifier, since the large low frequency gain of the first amplifier is within the feedback path of the filter. Therefore, any input offset in the filter amplifier will merely produce an equal magnitude offset in the time averaged output of the system.

The difficulty with the offset nulling scheme arises in the selection of the proper time constant for the filter. The filter must be slow enough that the signals of interest are not distorted by the nulling loop. However, the filter must respond to and eliminate error sources from, for example, component drift due to temperature changes of the

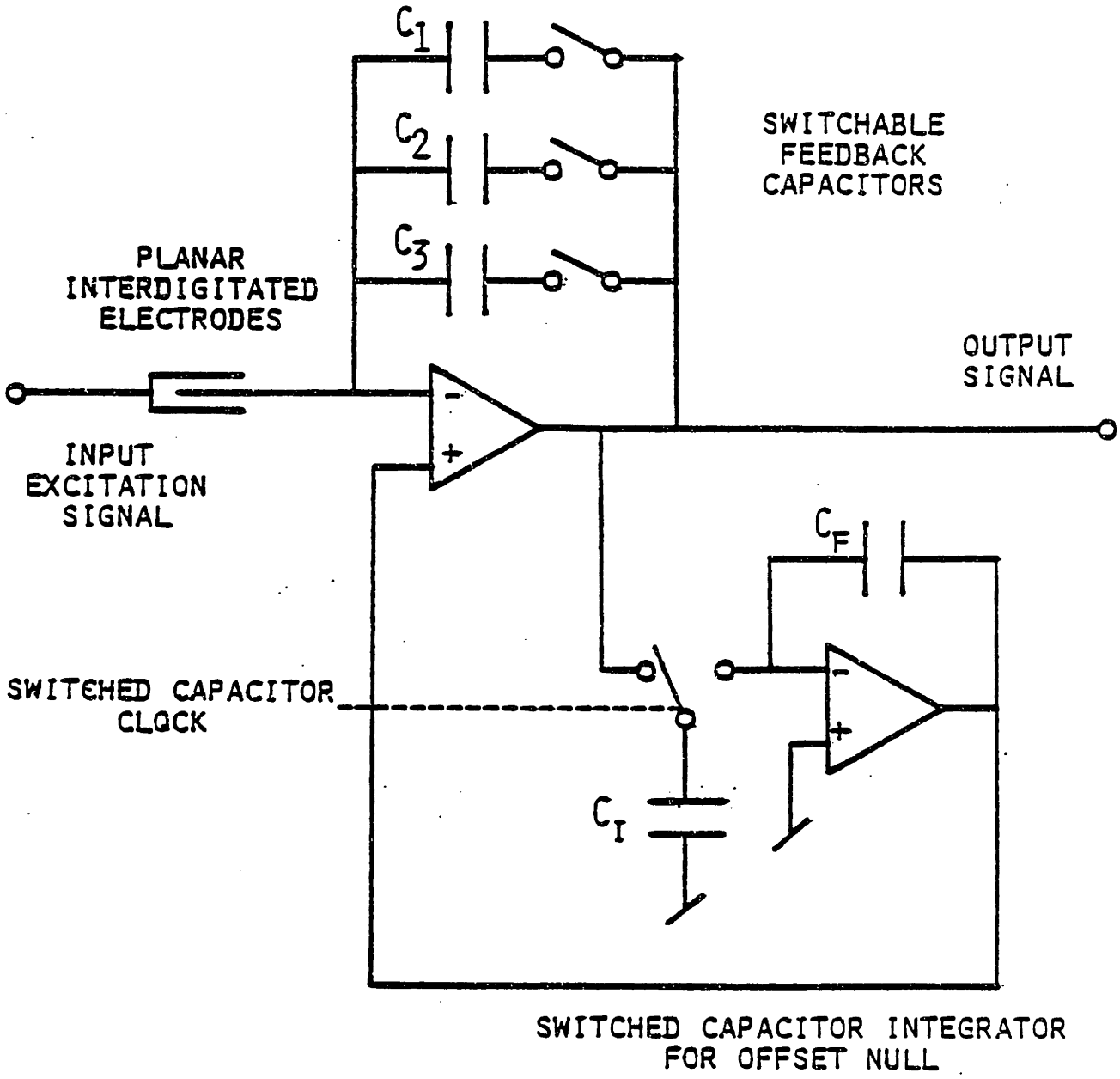


Figure 2.3 Switched Capacitor Filter for Offset Null

sensor chip during an experiment. Phase accuracy of 0.1 degree in the output signal, while measuring at a frequency of 0.01 Hz, requires a filter time constant of approximately 16 hours. At the higher measurement frequencies, where more realistic (but still large) filter time constants are desired, a switched capacitor design for the filter is convenient. Figure 2.3 shows the design of such a system. The time constant of the filter can be selected simply by scaling the clocking frequency, and the complete sensor circuitry, including the integrator and the switched capacitor offset nulling filter, can be integrated on a single chip.

2.1.3 Monolithic Impedance Bridge

The conventional instrument used for making measurements on components of arbitrary reactance is an impedance bridge, shown in schematic form in Figure 2.4. It is assumed for the purpose of initial discussion that the excitation signal is a single frequency sinusoid. In this case, Z_X can be modeled by a parallel combination of a single resistor and capacitor. The reference elements C_r and R_r are adjusted until the null detector indicates no signal potential between nodes "A" and "B". In the simplest case, when R_1 and R_2 are identical, at null C_r and R_r are equal to the corresponding elements in Z_X. Since at null there is no voltage applied across the detector, the

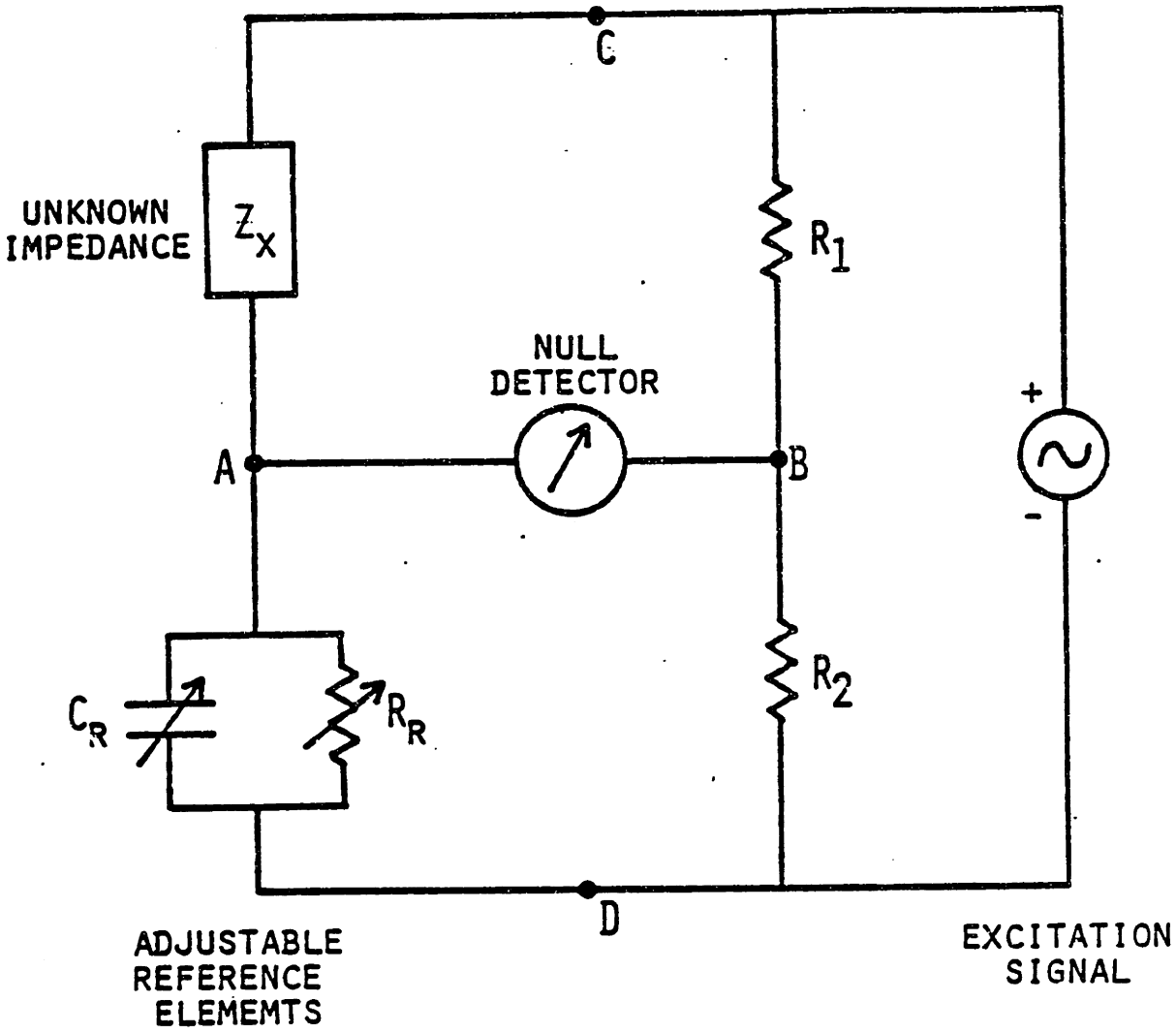


Figure 2.4 Conventional Impedance Bridge

parasitic conductance and capacitance of the null detector do not affect the accuracy of the measurement.

The impedance bridge can be rearranged into a more appropriate form for an integrated sensor. It is necessary to eliminate adjustable components, and it is desirable to produce a single-ended output signal referenced to ground. First, node "B" is defined to be the ground node of the circuit, and the excitation source is replaced by a pair of ground referenced signal sources that drive nodes "C" and "D". At this point R_1 and R_2 can be eliminated, and the reference elements C_r and R_r can be replaced by a single fixed capacitor. The revised circuit is shown in Figure 2.5. The modified bridge must be brought to a null by adjustment of the magnitude and phase of the nulling signal applied to the reference capacitor. As before, the parasitics associated with node "A" and the null detector do not affect the accuracy of the measurement.

Bridge configurations have advantages and disadvantages when compared with the more direct measurement techniques discussed earlier. The balanced condition in the bridge is achieved when there is no signal energy applied to the detector. Detecting a lack of signal is an easier requirement than the accurate determination of the magnitude and phase of the output signal, as required in the impedance divider or integrator techniques. A nonlinear detector with

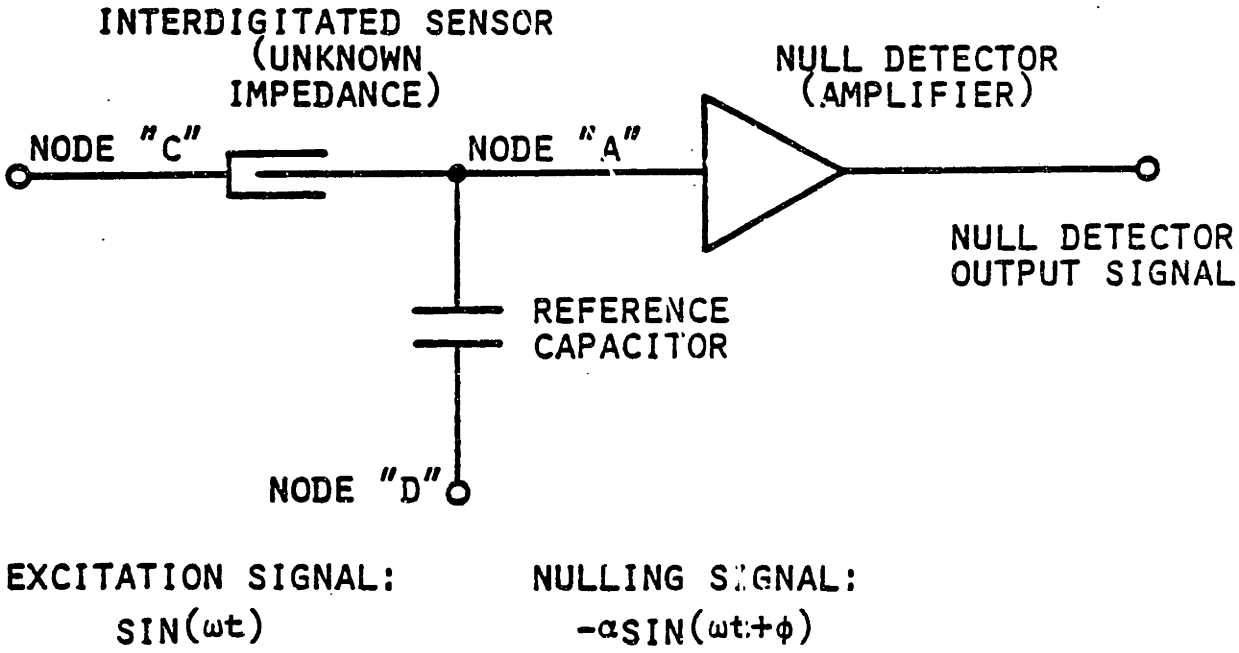


Figure 2.5 Modified Impedance Bridge

significant (and unpredictable) phase shift does not prevent detection of the null condition (though it likely becomes significantly more difficult to determine how to adjust the bridge so as to achieve the balanced condition).

A major disadvantage of the bridge techniques is the lower measurement speed. In general, a number of measurements of the null detector error output must be made, as the bridge is brought to a balanced condition. This system feedback loop is dependent on the time required for the detector to acquire an error output, and the time required to adjust the magnitude and phase relationship of the excitation and nulling signals. Increased sophistication in the analysis of the error signal can lead to faster convergence to a null. In the limiting case, where a single measurement is made, the bridge techniques simplify to the impedance divider configuration.

The advantage of a possibly simpler detector used by the bridge configurations is replaced in the case of the integrated bridge with the added complexity involved in the generation of the two excitation and nulling signals with a precise magnitude and phase relationship. A significant disadvantage occurs in the case that a measurement of the dielectric material properties is performed simultaneously at more than one frequency. In general, it is not possible to reach a null for an arbitrary sensor admittance function

unless the magnitude and phase of each nulling signal frequency component can be adjusted independently. This increases the complexity of the hardware and the software associated with the synthesizer that generates the excitation and nulling signals. In addition, the null detector must independently determine the error signal associated with each frequency component, and this requirement removes many of the advantages of the simpler null detector.

2.2 Parametric Sensitivity of Measurement Techniques

The impedance or admittance measurement configurations described in the previous section generate as the fundamental measured quantities the magnitude and phase relationship between two signals. The mapping of the measured magnitude and phase to the inferred permittivity and loss factor describes the calibration function of the sensor. This calibration function is dependent on the geometry of the sensor and sample, and also is affected by the sensor circuit configuration used for the measurement.

For the sensors and circuit topologies here discussed, the mapping between the sample dielectric properties and the measured magnitude and phase is a nonlinear function. This means that there exist regions of permittivity and loss factor where the measured magnitude and phase vary only slowly with respect to perturbations in the sample dielectric. The unavoidable small uncertainties in the experimental magnitude and phase measurement then lead to large uncertainties in the inferred sample permittivity and loss factor.

Techniques for optimizing the sensor geometry have been developed by Lee [10]. In addition to a number of considerations in the design that minimize parasitic effects, Lee has noted the importance of the ratio of

electrode spacing to the thickness of the underlying dielectric layer. This ratio determines the range of sample dielectric properties where the sensor output signal exhibits good sensitivity to variations in the sample properties. In this desired range, accurate sample measurements can be made.

The remainder of this section addresses the effects of the sensor circuit design choice on the parametric mapping between the measured signal and the underlying sample properties. Both of the circuit configurations are analysed assuming an identical sensor electrode and sample geometry, following the Lee guidelines. In addition, both configurations assume that the magnitude and phase measurement system has a phase accuracy of 0.1 degree and a magnitude resolution of 0.01 decibel (the goals set out in the introduction for the new gain-phase measurement system). These values are also consistent with experimental results that will be seen in Figures 4.2 and 4.3.

2.2.1 Impedance Divider Sensor Parametric Sensitivity

The simple model of the open-loop impedance divider configuration applies the excitation signal to a series connection of the unknown and reference impedances. The output signal is measured across the load (reference) capacitance. For samples that are of low impedance (high permittivity or highly conductive) the input-output transfer function approaches unity. Under these conditions the output signal is insensitive to changes in the sample.

The comb electrodes used in microdielectric sensors have a complex input-output response function, as displayed in Figure 2.6. This Figure shows the simulated characteristics of an optimized sensor geometry, as proposed by Lee. The plot indicates contours of constant permittivity (ε') and contours of constant loss factor (ε'') as a function of the measured magnitude and phase relationship between the excitation and response signals. Successive contours differ by a factor of the square root of two.

Consider first a purely capacitive sample applied to the sensor. The loss factor is zero, and the phase of the output will be zero. Increases in permittivity from the minimum possible value of one will be reflected in the response magnitude increasing from a minimum value of about -41 decibels toward unity. If the sample now has a non-zero

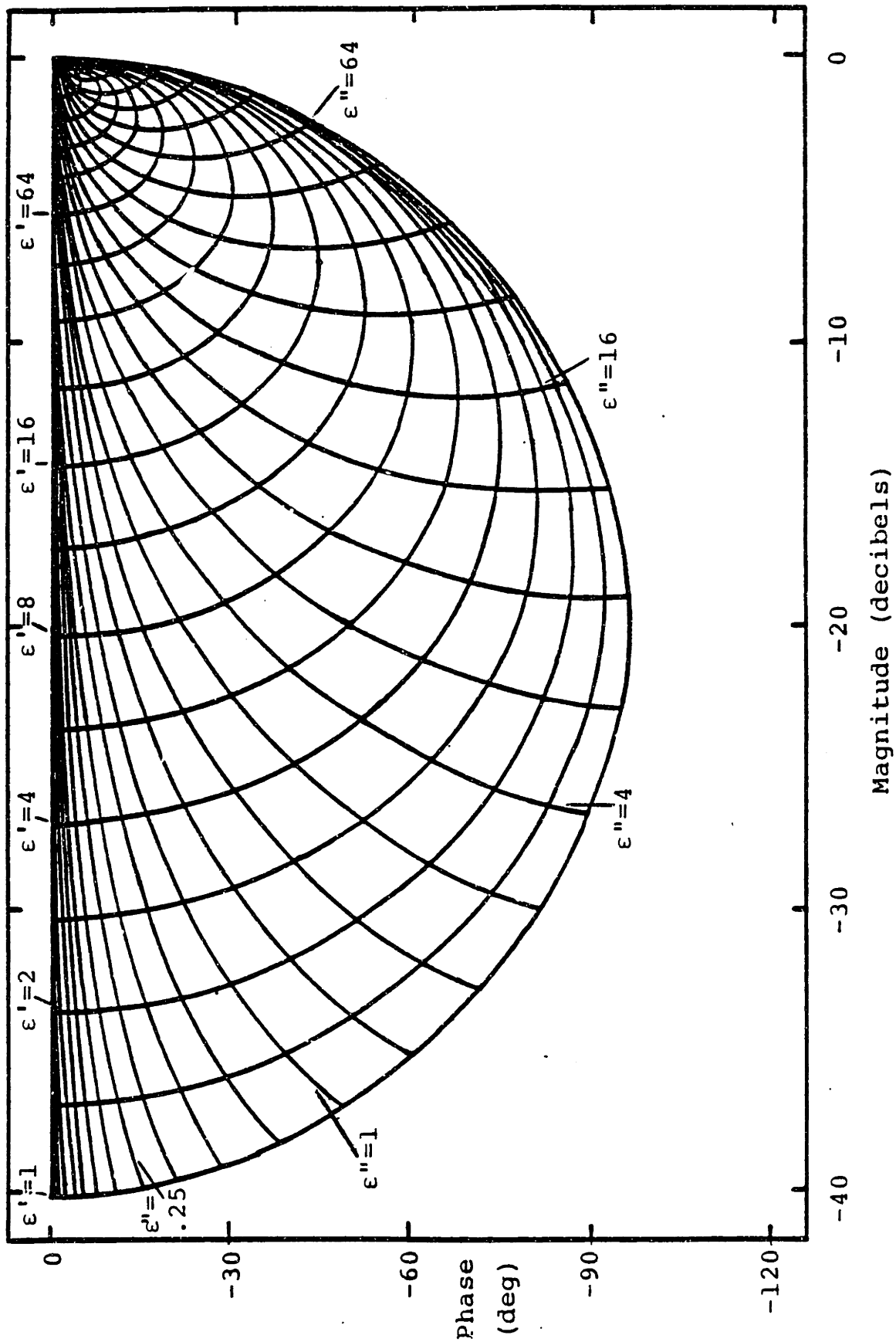


Figure 2.6 Calibration Curves for Impedance Divider Sensor

loss factor, the output signal will exhibit a phase lag with respect to the input excitation signal.

There are no dynamic range limitations on the open loop sensor. Any possible permittivity and loss factor combination will fall in the 41 decibel magnitude range visible on the plot. However, there are regions where the parametric sensitivity of the sensor is very low. For low loss factors, the phase approaches zero, and there is minimal sensitivity to ratiometric changes in the loss factor. For large loss factors the magnitude approaches zero decibels, and there is low sensitivity to variations in permittivity.

The above sensitivity arguments can be seen more explicitly by referring to Figures 2.7 and 2.8. Figure 2.7 shows the uncertainty in the inferred permittivity of a sample, as a function of the actual permittivity and loss factor, assuming for this and following Figures that the response signal measurement system has a magnitude resolution of 0.01 decibel, and a phase resolution of 0.1 degree, independent of the response signal level. For example, when measuring a sample dielectric with a permittivity of 10 and a loss factor of 3, the permittivity measurement will have an accuracy of better than one percent.

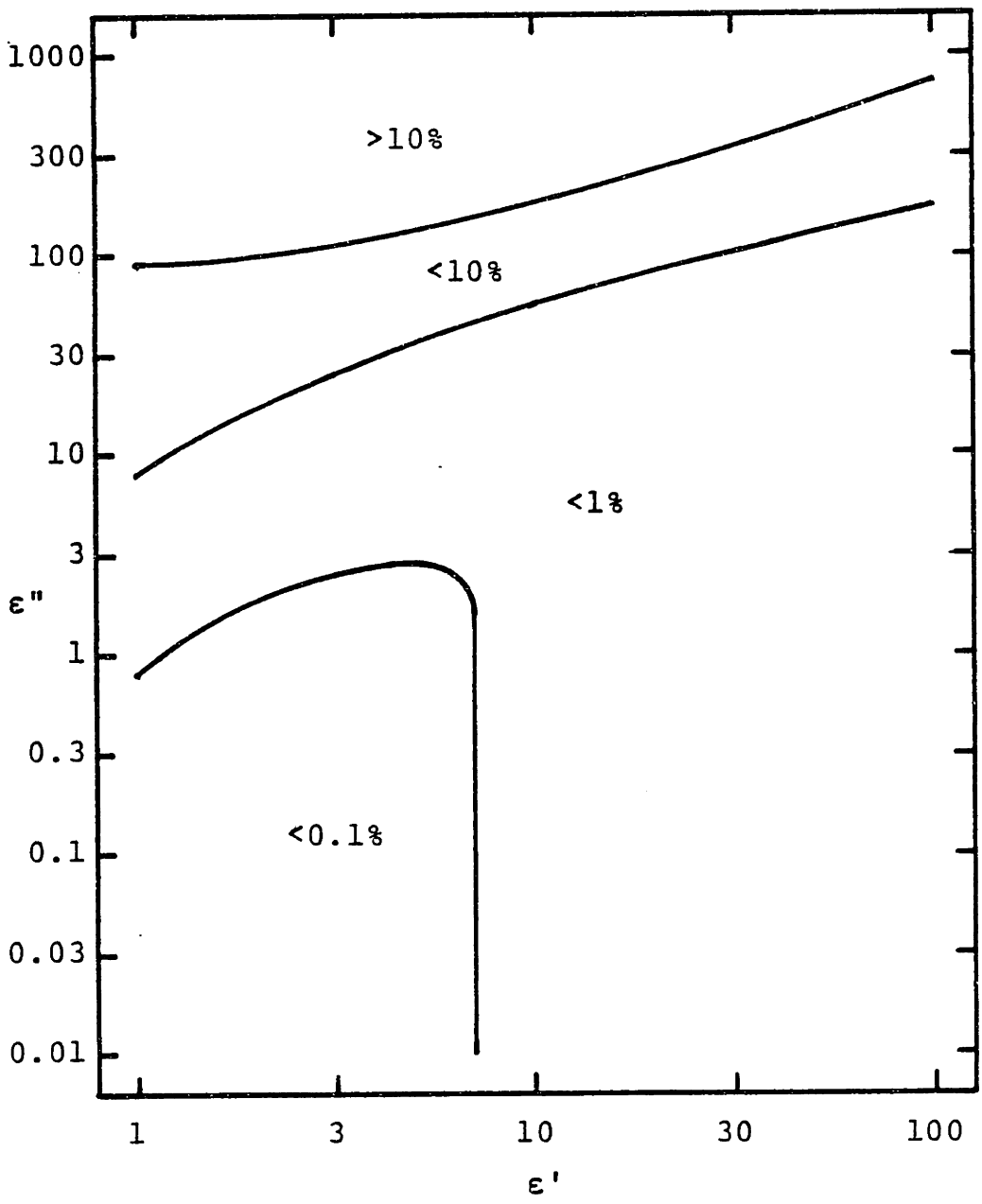


Figure 2.7 Resolution of ε' Measurement for Impedance Divider Sensor

Shown in Figure 2.8 are similar accuracy contours for the loss factor, again as a function of the sample dielectric properties. In general, measurements of the permittivity are seen to be difficult at large sample loss factors, while loss factor measurements become uncertain at the lower loss factors, particularly when coupled with large permittivity.

When the sample under test has a low impedance, the impedance divider configuration approaches a transfer function of unity. Since the excitation signal is fixed, there is only a small magnitude signal applied across the electrodes. This contributes to the poor resolution of the impedance divider configuration for low impedance samples, and provides motivation for consideration of a "virtual ground" system. Figure 2.9 indicates the fraction of the applied excitation signal that is applied to the electrode system as a function of the response signal magnitude and phase.

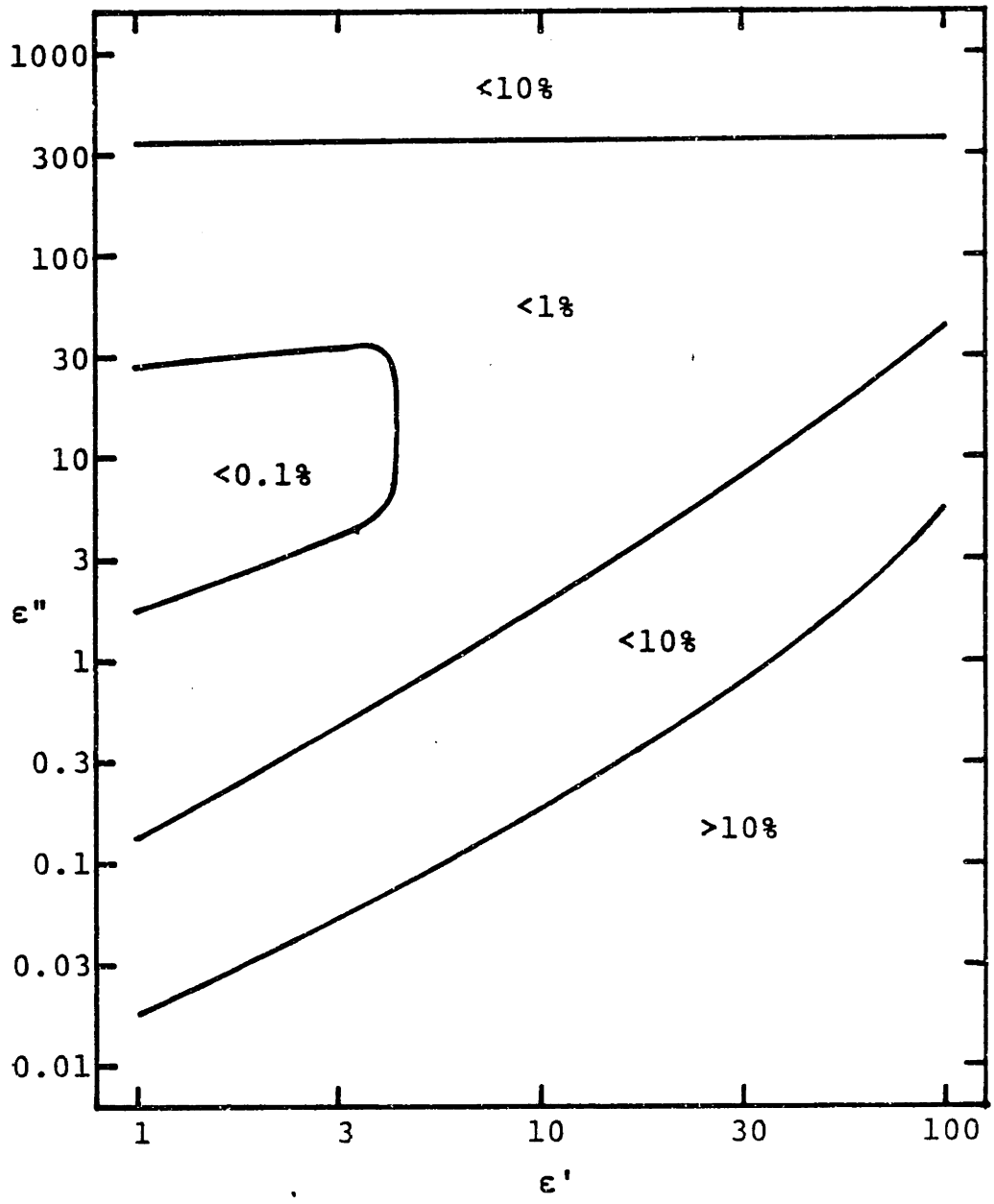


Figure 2.8 Resolution of ε" Measurement for Impedance Divider Sensor

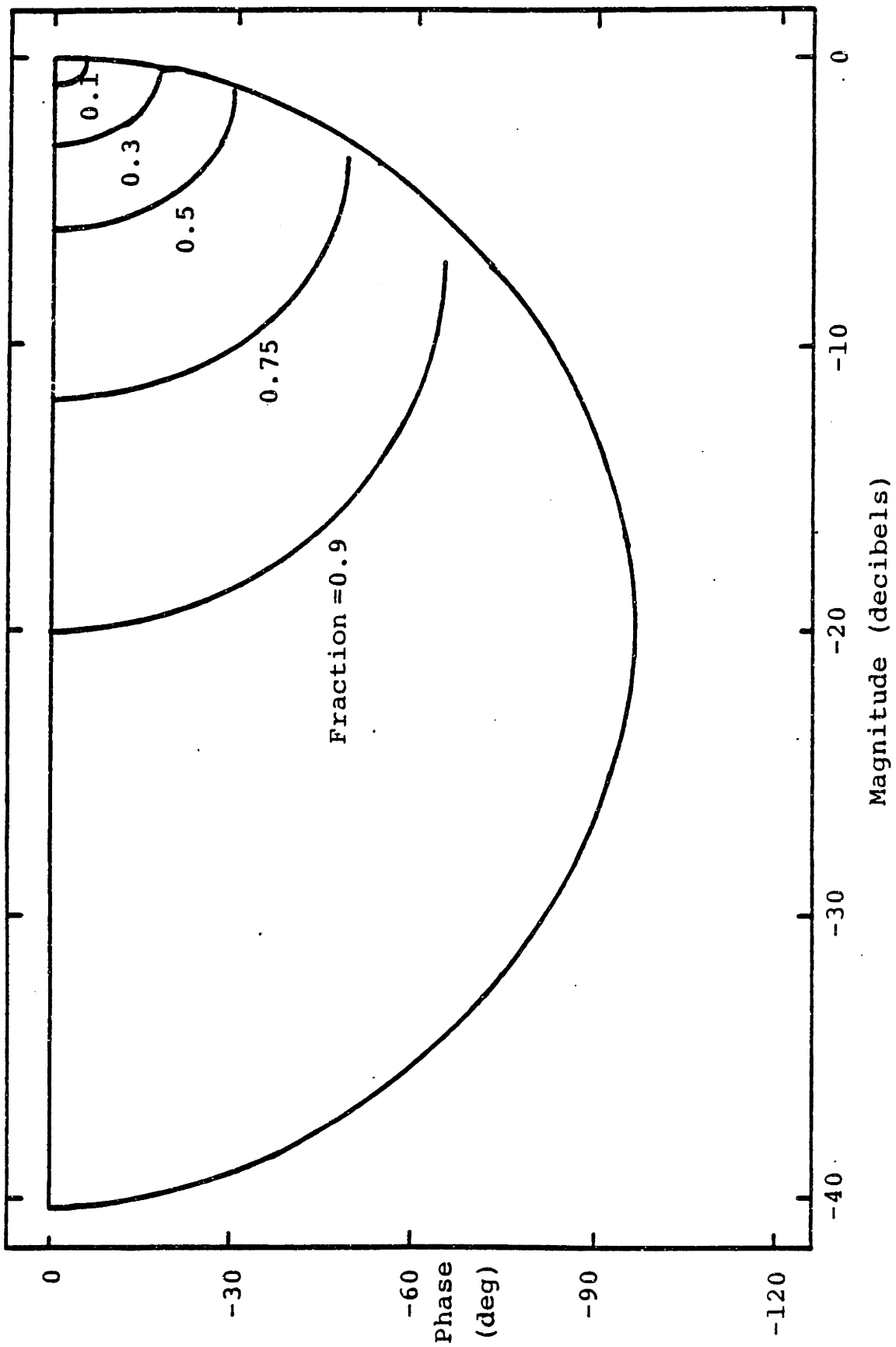


Figure 2.9 Fraction of Excitation Signal Applied to Electrodes for Impedance Divider Sensor

2.2.2 Virtual Ground Sensor Parametric Sensitivity

In contrast to the divider discussed in the previous section, the closed-loop (integrator) and the bridge techniques force the "floating" electrode to be at a virtual ground. Therefore, the full excitation signal is applied to the sample under all conditions. A plot of the simulated permittivity and loss factor contours of such a "virtual ground" sensor is shown in Figure 2.10. As in the impedance divider plot of Figure 2.6, the successive contours of constant permittivity and loss factor differ by a factor of the square root of two. The sensor electrode and sample geometry is unchanged from the previous case. The magnitude scale shown corresponds to a reference capacitor of value 1.0 pF. As would be expected, for low response signal magnitudes the calibration characteristics of the two configurations are similar. However, for a sample with a low impedance the virtual ground sensor does not exhibit saturation of the output signal magnitude. If the capacitive impedance is low compared to the conductance of the sample, the phase will approach zero; while if the conductance dominates, the phase will tend to -90 degrees. The continued sensitivity to sample properties does not come for free -- the measurement system must operate over a dynamic range that increases in proportion to extensions of the impedance range of interest.

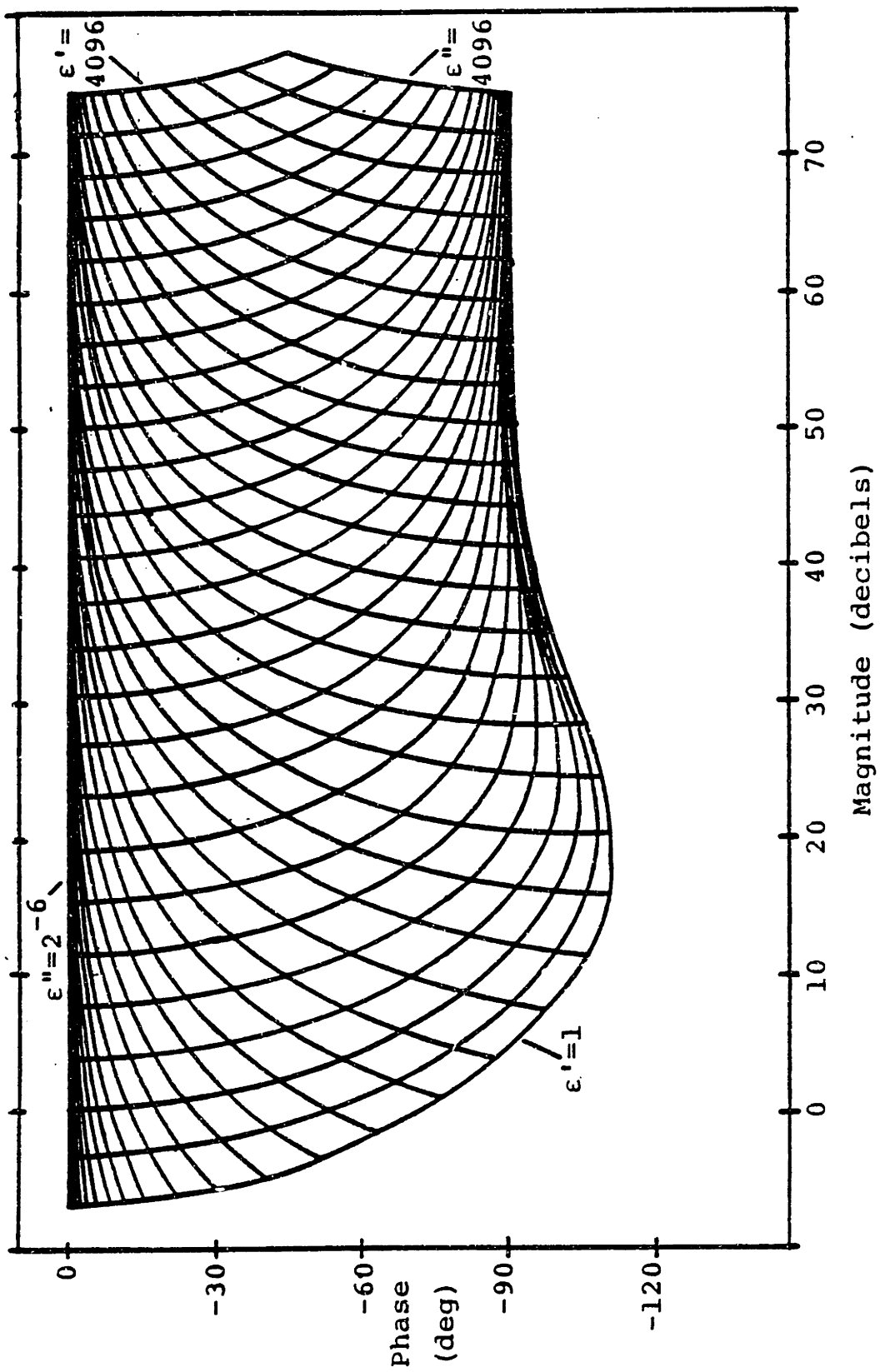


Figure 2.10 Calibration Curves for Virtual Ground Sensors

The measurement uncertainty for the virtual ground sensor over a range of sample dielectric properties can be seen in Figures 2.11 and 2.12. Figure 2.11 shows the accuracy of the measured permittivity, as a function of the sample permittivity and loss factor, assuming as before that the magnitude and phase measurement system can determine magnitude to 0.01 decibel and phase to 0.1 degree. For example, using this sensor configuration a sample dielectric of permittivity 10 and loss factor 3 will give permittivity measurements to an accuracy better than 0.1 percent.

In Figure 2.12 are shown accuracy contours for loss factor measurements made with the virtual ground sensor, once again plotted with respect to the permittivity and loss factor of the sample dielectric. Not unexpectedly, loss factor measurements remain as difficult at low loss factors as with the impedance divider sensor. Both sensor configurations have similar calibration functions in this region. The accuracy of the virtual ground sensor is, however, improved over the divider circuit for measurements at large loss factors.

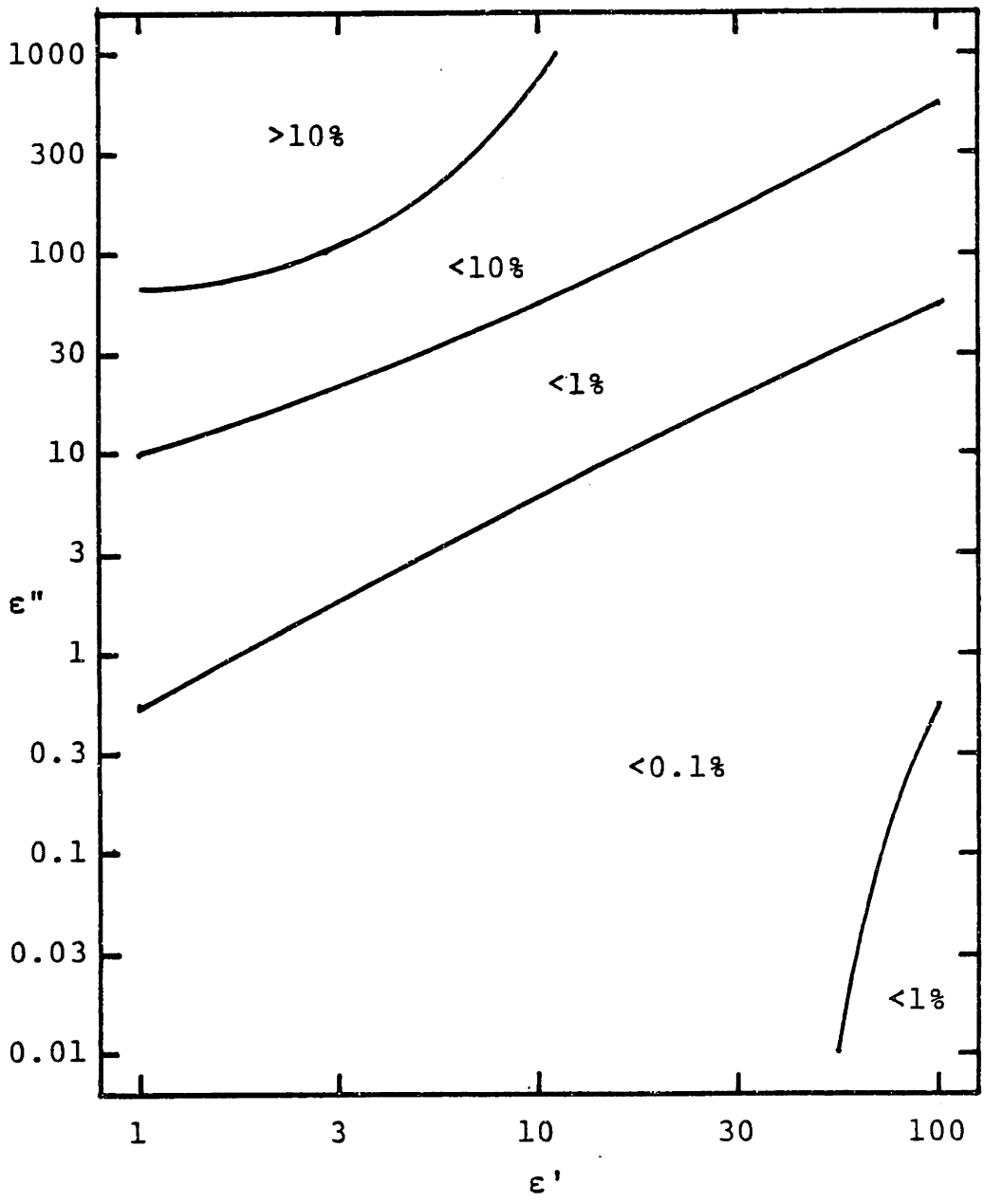


Figure 2.11 Resolution of ε' Measurement for Virtual Ground Sensor

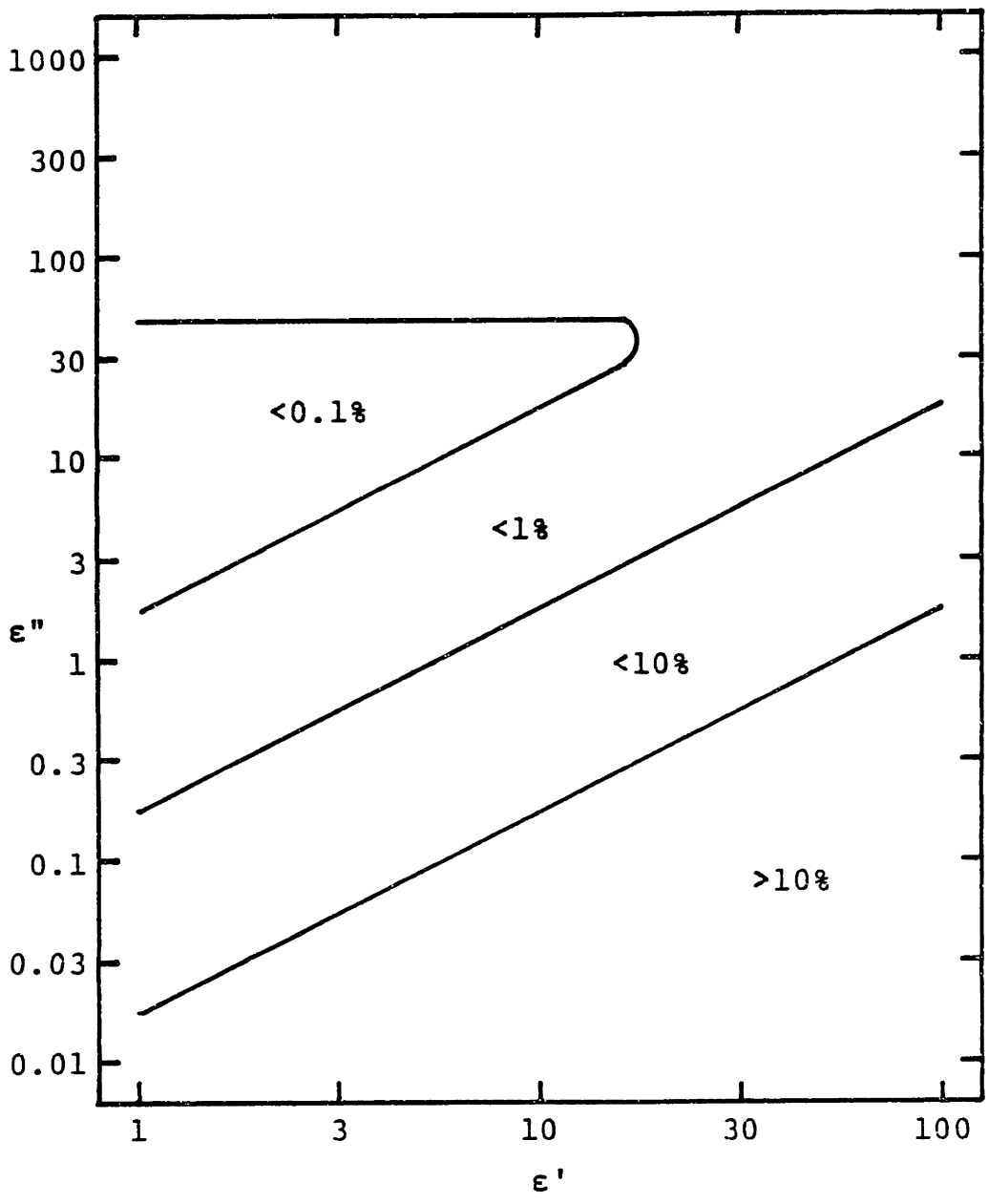


Figure 2.12 Resolution of ε" Measurement for Virtual Ground Sensor

2.2.3 Comparison of Sensitivity of Sensor Circuits

Observation of the accuracy contour plots presented in the previous section reveals the advantages of the virtual ground circuit configurations over the impedance divider design. One area of significant enhancement occurs for measurements of permittivity when both the permittivity and the loss factor are large. Permittivity measurement to an accuracy of 10 percent is possible for the virtual ground sensor when the sample has a permittivity of 10 and a loss factor of 300. This capability is not available with the impedance divider circuit.

Loss factor measurements with the virtual ground circuit also exhibit improvement at large loss factors, however the low loss regime has poor characteristics for both sensor designs. In the low loss region the phase is small. Minimal absolute variations in the measured phase then correspond to large ratiometric changes in the inferred loss factor.

The virtual ground configurations have the disadvantage that a significantly larger dynamic range for the response signal magnitude must be accommodated. In this particular case, a 70 decibel range is required for the virtual ground systems, compared with a 40 decibel range for the impedance divider. In a realistic engineering environment, the

increased dynamic range necessary would increase the difficulty in maintaining the high quality magnitude and phase measurement specifications that have been assumed. Degradation of these specifications would tend to cancel the advantage in accuracy enjoyed by the virtual ground system.

2.3 Summary of Sensor Design Issues

This section summarizes the results of the sensor circuit design analysis of the three basic circuit configurations presented in the preceding two sections. Each has advantages, and disadvantages, if all of the issues of the overall design of a dielectric measurement system are considered. These issues include the sensor chip calibration function, the frequency range of interest, the complexity of the supporting measurement system not including the sensor, and the measurement speed necessary.

Open-Loop

Disadvantages:

1) Limited range of sample properties can be measured due to poor resolution at large loss factors.
2) Phase measurement errors at high frequencies from dynamics of buffer circuit.
3) Difficulty of accurate absolute magnitude and phase measurements.

Advantages:

1) Simple on-chip circuitry so sample property measurement range can be extended by including a set of electrode structures, each optimized for part of the range.
2) Fast measurements since sample properties are derived

from a single sampling run of the sensor response signal.

3) Amenable to measurements at multiple frequencies concurrently.

Integrator

Disadvantages:

1) Extended dynamic range of response signal must be measured accurately.
2) Phase measurement errors at high frequencies from dynamics of integrator amplifier.
3) Difficulty of making absolute magnitude and phase measurements.
4) Offset voltages integrate, saturating the output unless a null circuit is included. Null circuit limits low frequency range.

Advantages:

1) An extended range of sample properties can be measured.
2) Fast measurements are possible since sample properties are calculated from one sampling run of the response signal.
3) Amenable to simultaneous measurements at multiple frequencies.

Monolithic Bridge

Disadvantages:

1) Slow measurements since convergence of the bridge to null requires several samplings of the detector error.
2) Additional complexity of the two channel signal synthesizer.
3) Multiple frequency measurements are difficult. Detector and synthesizer complexity increases.

Advantages:

1) A virtual ground is implemented, so an extended range of sample properties can be measured.
2) The dynamics of the null detector do not affect the accuracy of the magnitude and phase measurements.
3) The detector can be simple if multiple frequency measurements are not required.

Microdielectrometer measurements of dielectrics are often performed at frequencies well below 1 Hz. At these low frequencies the offset voltage problem of the integrator configuration is a fatal flaw, since the time constant of the necessary offset nulling loop becomes ridiculously long.

The advantages of the bridge technique are apparent at high frequencies, where the simplified null detector is decidedly preferable to the high frequency buffer and accurate magnitude and phase receiver required in the

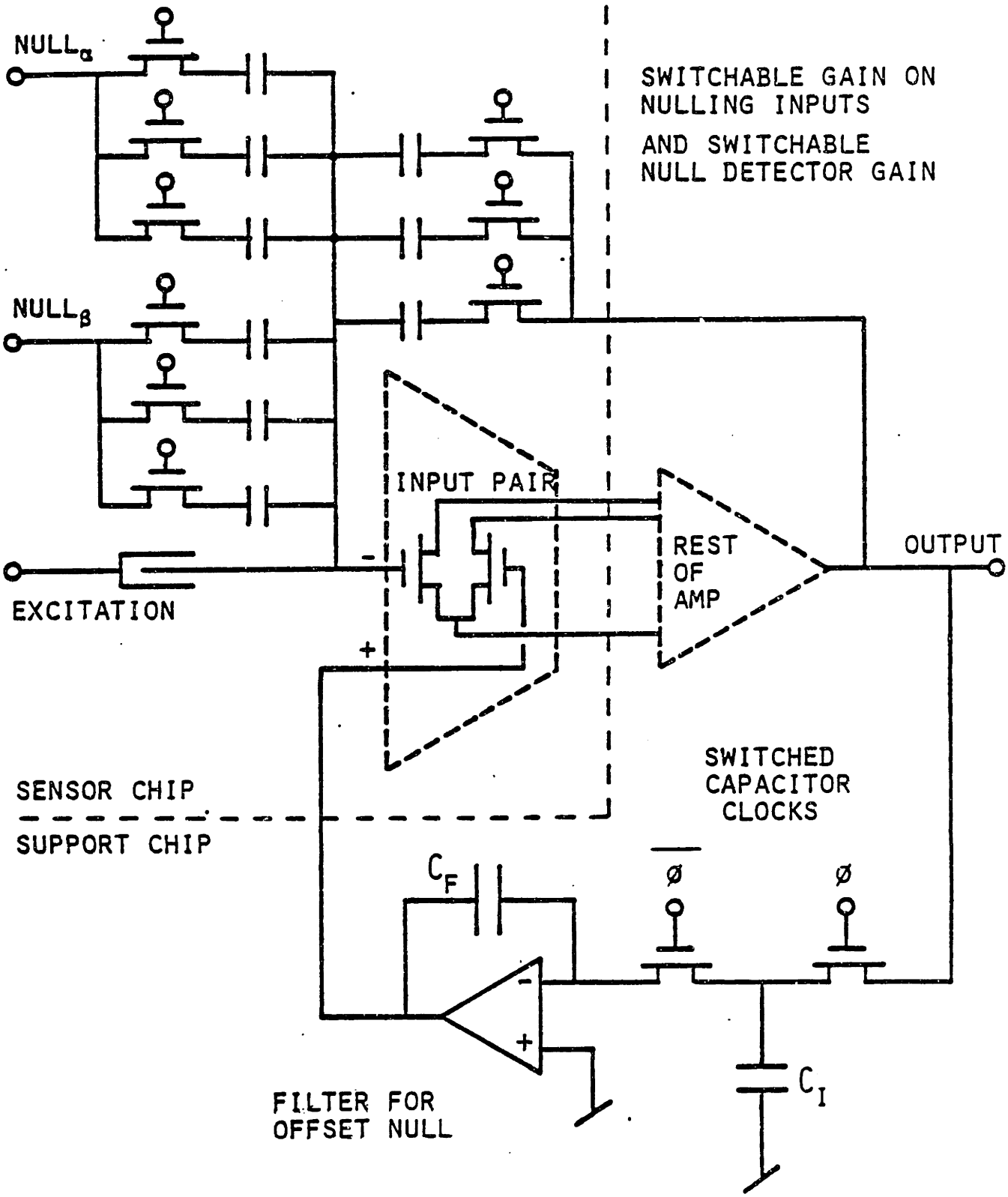
divider configuration. At these higher frequencies the additional time necessary to drive the bridge to a null is also less noticeable, as is the time required to make successive measurements at a number of individual frequencies, rather than a single simultaneous measurement.

In the low frequency range where a single sampling run of the response signal involves a significant time period (either on the scale of the experiment or the experimenter), the divider topology has the best collection of features. Techniques for making accurate absolute magnitude and phase measurements are addressed in Chapter 3. The sensitivity problem that limits the range of resolvable dielectric properties can be avoided by including a number of electrode structures on the sensor chip, each optimized for a section of the total permittivity and loss factor space.

2.4 The Sensor Test Chip

A test sensor design that incorporates provisions for operation in both the integrator and monolithic bridge configurations is shown in Figure 2.13. Control signals applied to the chip determine the mode of operation selected. The design uses a standard enhancement/depletion NMOS process. It is difficult to design amplifiers that operate over the temperature range required for the sensor. Polymer curing reaction temperatures can be as high as 250 C, and experiments measuring the low temperature dielectric properties of polymers and their precursors have ranged nearly as low as -200 C. Maintaining gain, frequency response and stability over such an extended range was not deemed feasible.

Fortunately, it is only necessary that all components directly connected to the floating gate node (the inverting node of the first integrator) be on the sensor chip. The sensor circuitry is partitioned so that the remainder of the support circuit can be located on a second chip, separated from the sensor and located in a more benign environment. This partition is shown in Figure 2.13, with the electrodes, integration and nulling capacitors, capacitor switches, and the two differential input transistors fabricated on the sensor chip. All other circuitry resides on the "support" chip. Careful attention to the design of the first



NULL$_\alpha$: $\alpha SIN(\omega t-\pi)$

NULL$_\beta$: $\beta SIN(\omega t-\pi-\phi)$

EXCITATION: $SIN(\omega t)$

Figure 2.13 Test Sensor Circuit Design

amplifier is required to insure that the large parasitics associated with the cabling between the differential transistors and the rest of the amplifier do not adversely affect the response and stability of the overall system. Details of the sensor and support chip design are included in Appendix A.

The semiconductor fabrication process available was fixed, so the electrode geometry could not be optimized. Consequently, no attempt was made to match the characteristics of the simulated sensors shown in Figures 2.6 and 2.10. The two test chip designs (sensor and support) were included together on an analog multiproject chip [16]. The returned samples were tested to confirm the characteristics of the different sensor circuit configurations. Three of the seven test devices available were found to be electrically functional. It was necessary to passivate the sensor used for further tests by isolating the sensor electrode area from the chip bonding pads and wires with silicone rubber. Noise performance of the chips is discussed in section 4.1.5.

The passivated test device was used to make two measurements each of the characteristics of polyethylene glycol and automotive oil. These materials were chosen as sample dielectrics because a generous range of magnitude and phase response values were covered, and because the

materials could easily be removed from the electrode structure without damage to the sensor. Measurements were made over a frequency range of 0.05 Hz to 10 kHz. Experimental results for the integrator sensor configuration with the automotive oil sample can be seen in Figure 2.14. The second loop in the magnitude and phase trajectory is due to boundary layer effects at the electrodes [17]. The effect is particularly pronounced on this sensor geometry because of the small electrode spacing used in the design (4 μm) to maintain strong coupling over the fairly thin field oxide substrate dielectric.

Results for the monolithic bridge circuit with otherwise equivalent experimental conditions are shown in Figure 2.15. Both sensors operate with a virtual ground at the "floating" node, so the close match between the two sets of data is as expected. The differences visible at the lowest frequencies are due to distortion in the sensor amplifier from the large signal levels. The dynamic range of the response signal varies over 60 decibels for this sample, demonstrating the extended magnitude measurement range necessary to take advantage of virtual ground sensors.

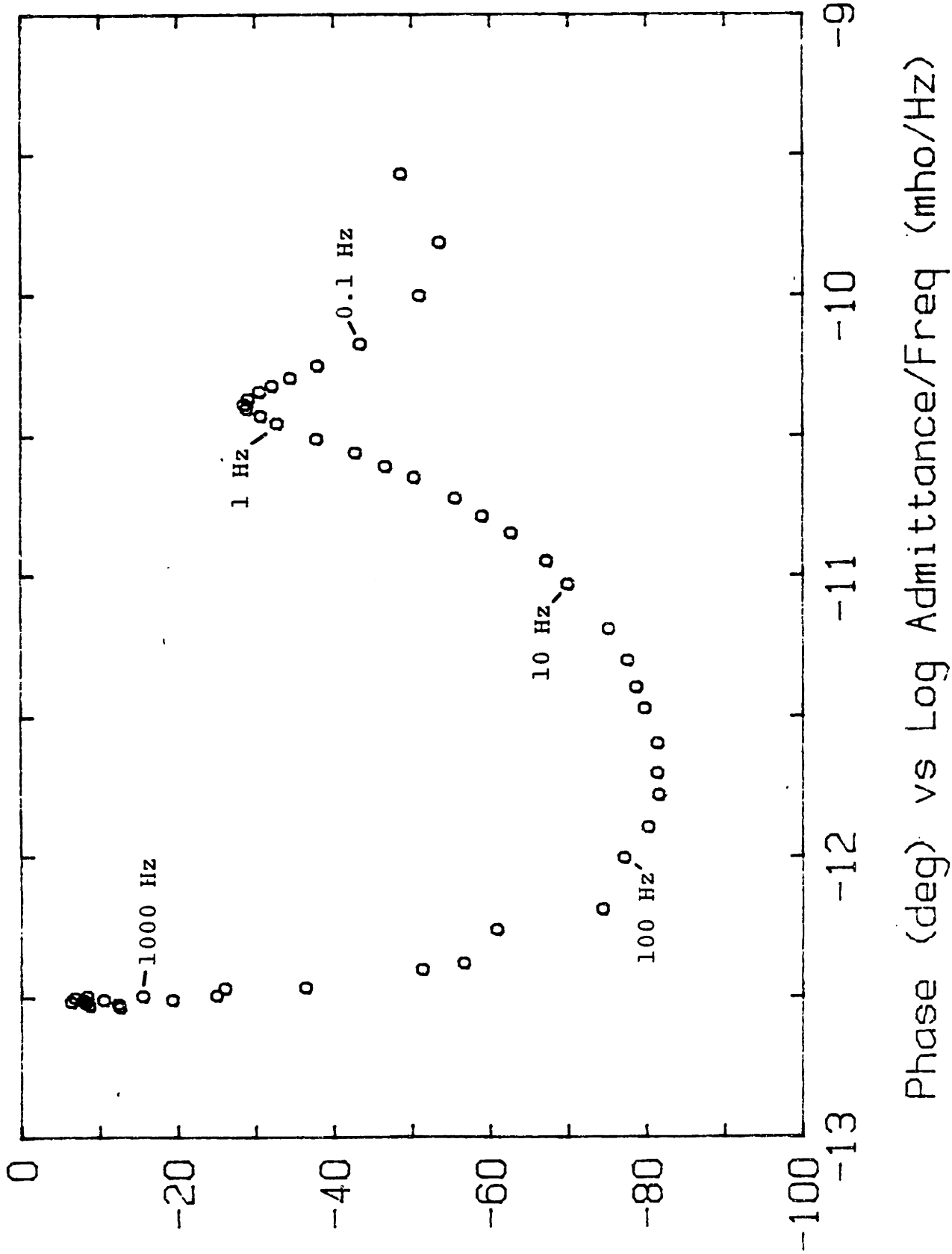


Figure 2.14 Magnitude and Phase Response of Automotive Oil on Test Chip in Integrator Configuration

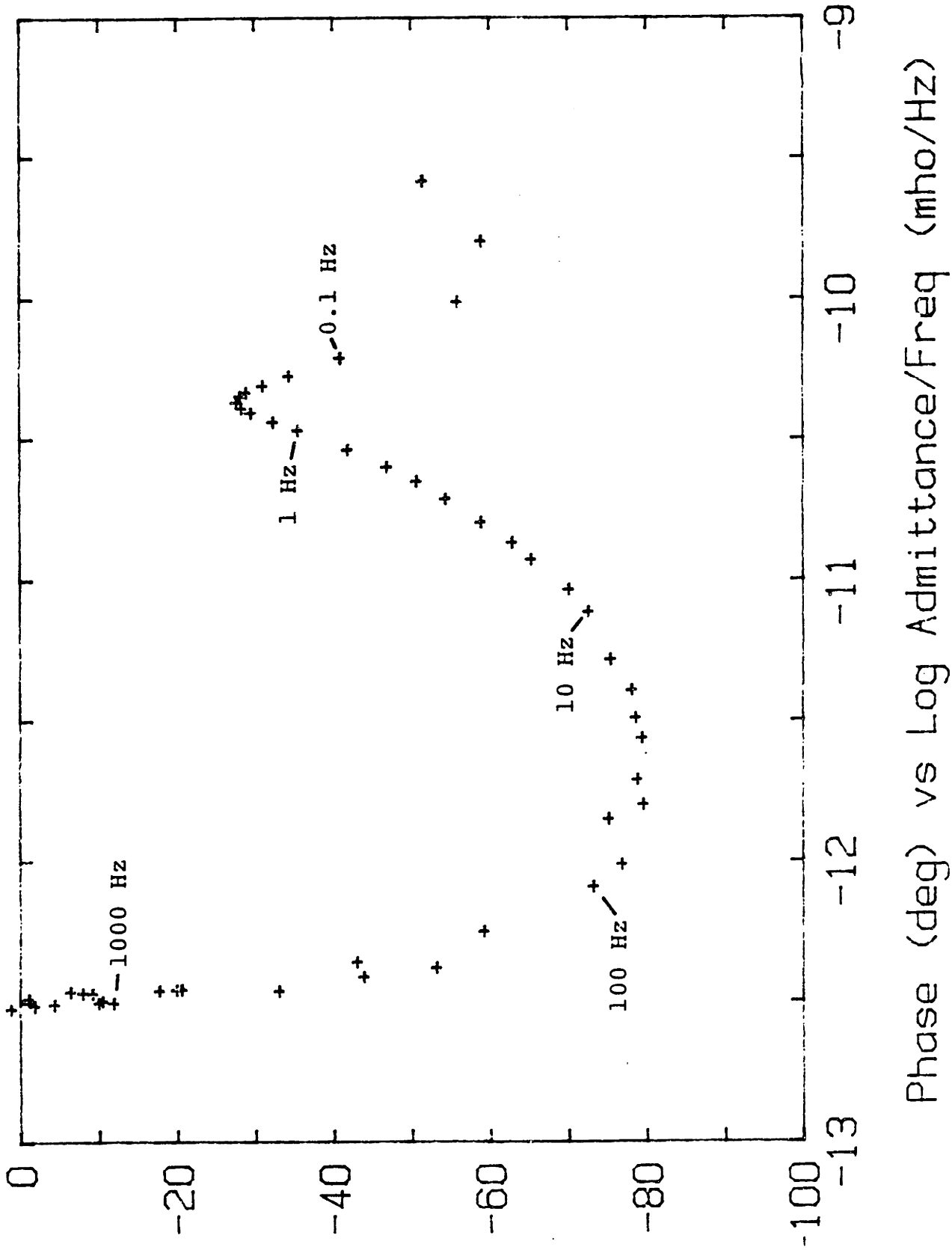


Figure 2.15 Magnitude and Phase Response of Automotive Oil on Test Chip in Monolithic Bridge Configuration

CHAPTER 3

Measurement and Analysis Instrumentation

This chapter discusses the design of instrumentation for use with the dielectric sensors discussed in Chapter 2. The choice of measurement technique is affected by the frequency range and desired performance of the system in the areas of amplitude and phase sensitivity, speed of measurement, concurrent measurements at multiple frequencies, and complexity/cost considerations. The final design uses a programmable waveform synthesizer and sampled data digital signal processing techniques implemented on a microcomputer.

The first section of the chapter discusses the selection of the general method used for measuring the magnitude and phase of the sensor signal. Second, a number of alternatives for the sensor excitation waveform are compared. The next section describes the instrumentation design selected. The final section analyzes the effect of aliasing due to the discrete time measurement technique, and possible techniques to reduce this effect.

3.1 Optimum Receiver Design

The dielectric sensor considered in this thesis is a "spectroscopic" sensor, that is, a sensor where the excitation signal contains the frequency or frequencies of interest. The excitation-response behavior of the sensor is parametrically related to the dielectric properties of the medium in contact with the sensor, and it is the task of the measurement system to extract key features of the excitation-response function so that the dielectric properties can be inferred. If it can be assumed that the combination of the medium and the sensor together is linear, then the system can be described by the frequency dependent magnitude and phase response. This requirement for linearity in the system under test is a key point--many of the design decisions for the measurement instrument are predicated on the use of the superposition principle. Small deviations from linearity are in fact of interest, since the distortion will produce harmonics or combination tones that can be used to probe the limits of linear behavior in the sample, or measure the non-linearities in the instrumentation.

A number of techniques are available for extracting the magnitude and phase relationship between a pair of signals (in this case, the excitation and response signals of the system under test) and these can often be implemented in

either the analog (continuous time) or the digital (sampled data) domain. A fairly crude instrument could estimate magnitude using an envelope detector. Relative phase could be measured by evaluating the relative timing of the "zero-crossings" of the signals. The above design was implemented in the gain-phase meter that was used for the early studies of dielectric sensors and cure monitoring [13]. The envelope and zero-crossing detector technique is, however, not usable if the excitation signal contains energy at more than one frequency. Even in the case of a single applied frequency the phase measurement is particularly sensitive to noise, as the timing is taken when the signal is crossing zero and therefore is smallest relative to any noise.

The above concerns suggest that more successful measurements require the use of an optimal receiver such as a matched filter or a correlation detector [18]. A true correlation detector has better performance than a synchronous switching, or chopper, implementation since a matched filter or correlation detector uses all of the energy in the waveform for the detection process and rejects energy that does not match the template, including noise. Analog implementations of these techniques are typified by a phase locked loop receiver using a four-quadrant multiplier as the phase detector. For the sensor application under discussion, the excitation signal can provide reference

signals, allowing correlation detectors to determine both phase and amplitude information.

Since the excitation-response function is assumed linear, if an excitation signal containing energy at a variety of frequencies is applied to the sensor, it is possible to recover the dielectric properties of the material at all of these frequencies from a single measurement.

3.2 Choice of Excitation Waveform

The spectroscopic measurement used in this system extracts as primary measurement quantities the frequency dependent magnitude and phase response of the system. It is assumed that the system being measured is linear, so that an optimum detector can measure the system response at all frequencies that are present in the excitation waveform. The choice of waveform to be used is then determined by the desired set of frequencies, and the signal to noise ratio (SNR) required at each frequency to meet the accuracy specifications. In general, the total excitation energy can be increased to enhance the SNR, but this requires higher peak power in the waveform, or a longer acquisition interval [18]. Higher power eventually results in non-linearity in the system, while a longer acquisition interval impacts the speed of the measurement. It is therefore advantageous to tailor the spectrum of the excitation waveform to match the frequencies of interest to the experimenter. Several possible choices of excitation spectra will be considered below, with their advantages and disadvantages in this application.

1) Impulse function (or approximation by short pulse)

Advantages: An impulse function contains equal energy at all frequencies, so a Fourier transform of the response

waveform yields the entire spectral response of the system under test.

Disadvantages: All the excitation energy is applied to the sample during an "infinitesimal" (very short) time period, leading to "infinite" (very large) peak power. To avoid non-linearity the signal level, and thus the SNR, must be reduced. If only a specific set of frequencies is of interest, the energy at all other frequencies is wasted.

2) Step function [19]

Advantages: The excitation energy is applied during the entire measurement, reducing the peak applied power.

Disadvantages: The 1/f spectrum of the excitation waveform includes very little energy at higher frequencies. As in the case of the impulse function, energy at frequencies not of interest is wasted, and reduces the SNR at the desired frequencies.

3) Random noise

Advantages: The excitation signal is applied during the entire measurement. The spectrum can be tailored to match the specific set of frequencies that are of interest.

Disadvantages: Generating truly random noise with a particular spectrum requires significant overhead for analog filters or digital computation. If a physical noise source is used (a diode in avalanche breakdown, for example), both

the excitation signal and the response signal must be sampled and analyzed to derive the spectral response of the system under test. Since the signal is stochastic, a given measurement may exhibit poor signal to noise ratio.

4) Pseudo-random noise

Advantages: The excitation energy is applied during the entire measurement, reducing peak power for a given SNR. The spectrum can be tailored to match the specific set of frequencies that are of interest. The generation of the pseudo-random noise does not have to be done in "real time" during the experiment, and since it is a deterministic signal the excitation waveform does not have to be sampled as in the truly random case above.

Disadvantages: The extraction of the spectral response of the system under test requires more computation than the alternatives to be described next.

5) Sequential measurements at frequencies of interest, in each case applying a sinusoidal signal at one frequency.

Advantages: The analysis requires only a simple correlation between the excitation and response waveforms. The simple analysis allows an analog circuit implementation for low resolution or high frequency application. The generation of the excitation waveform is simplified. This

technique gives the maximum SNR possible for a fixed length single measurement.

Disadvantages: The large SNR carries a burden of a proportionally increased total measurement time as the number of frequencies increases. The transition from one excitation frequency to the next will cause a transient that can perturb the following measurements.

6) A sum of sinusoids at the frequencies of interest.

Advantages: The excitation energy is exactly matched to the information desired, giving the maximum SNR for a fixed length measurement. Though the generation of the excitation waveform is proportionately slower than the procedure for the above single frequency excitation, it is still straightforward. The measurement is faster than the above sequential sinusoid technique, since the response waveform is only sampled once. If the set of frequencies is small, a sequence of correlation operations on the response signal can be used instead of a complete transform. This may reduce the computation required. The applied signal does not contain transients from the transitions between successive single frequency sinusoids. Non-linearities in the system under test (or the instrumentation) can be detected by observation of the response signals at frequencies other than those contained in the excitation set.

Disadvantages: The set of frequencies of interest must be determined at the beginning of the experiment, so the proper excitation waveform can be generated. If the set of frequencies is large, the SNR is proportionally reduced.

In summary, a variety of spectra for the excitation waveform have been proposed, with a corresponding variety of advantages and disadvantages. The final alternative listed above, using an excitation signal consisting of a sum of sinusoids at the frequencies of interest, has the best overall characteristics. This technique was chosen for implementation. Two particular points should be noted. First, if the set of frequencies used is reduced to a single element, the multi-frequency technique reduces to the single frequency sinusoidal excitation alternative also discussed above. Second, the system can be used to measure the linearity of its constituent parts by observing signals at frequencies not included in the excitation set.

3.3 Design of the Sampled Data System

Section 3.1 included a discussion of the receiver characteristics desirable in a magnitude and phase measurement system. The true correlation detector chosen has the properties of an optimum receiver, and supports analysis of all components of a multiple frequency excitation, as discussed in section 3.2. The frequency range of interest for the dielectric sensor is wide, but limited to low frequencies: 0.005 Hz to 10 kHz. Precise measurement of the magnitude and phase response of the sensor (as determined by the material under test) is required for signal levels ranging over two orders of magnitude. The low frequencies and wide frequency range make accurate measurements impractical for analog techniques, whether sampled data or continuous time designs. In comparison, a system using an analog to digital converter to sample the response signal and convert it to a digital data array becomes easier to design as the frequencies are reduced.

In a digital sampled data system, the correlation detector function is implemented using digital signal processing, avoiding many of the accuracy limitations of analog multipliers and integrators. The sensor excitation signal is digitally synthesized from a stored data array, with timing derived from a crystal controlled clock. This

same clock triggers the sampling of the sensor response. The common clock provides an absolute phase reference and avoids the need to sample both the excitation and the response waveforms. A simple block diagram of such a sampled data system is shown in Figure 3.1.

The signal synthesizer must generate the desired excitation waveform, and synchronized pulses to trigger the analog to digital converter. The wide variety of possible waveforms, the high accuracy required, and the potential for very low frequencies suggests a synthesizer design with digital storage of a precomputed waveform. During an actual measurement, successive elements of the array of numeric waveform data are converted to analog voltages by a digital to analog converter. The interaction of several constraints in the design of the synthesizer strongly impacts the overall performance of the measurement system. These constraints include the number of steps per cycle of the highest frequency component of the synthesized waveform (to avoid undesired high harmonics that will produce aliasing upon subsequent sampling), the clock rate of the synthesizer, the sampling rate of the response channel (which must exceed the Nyquist rate at the highest frequency), and the size of the synthesized and sampled data arrays, which determine the set of available harmonics that can be analyzed. The size of the sampled data array also

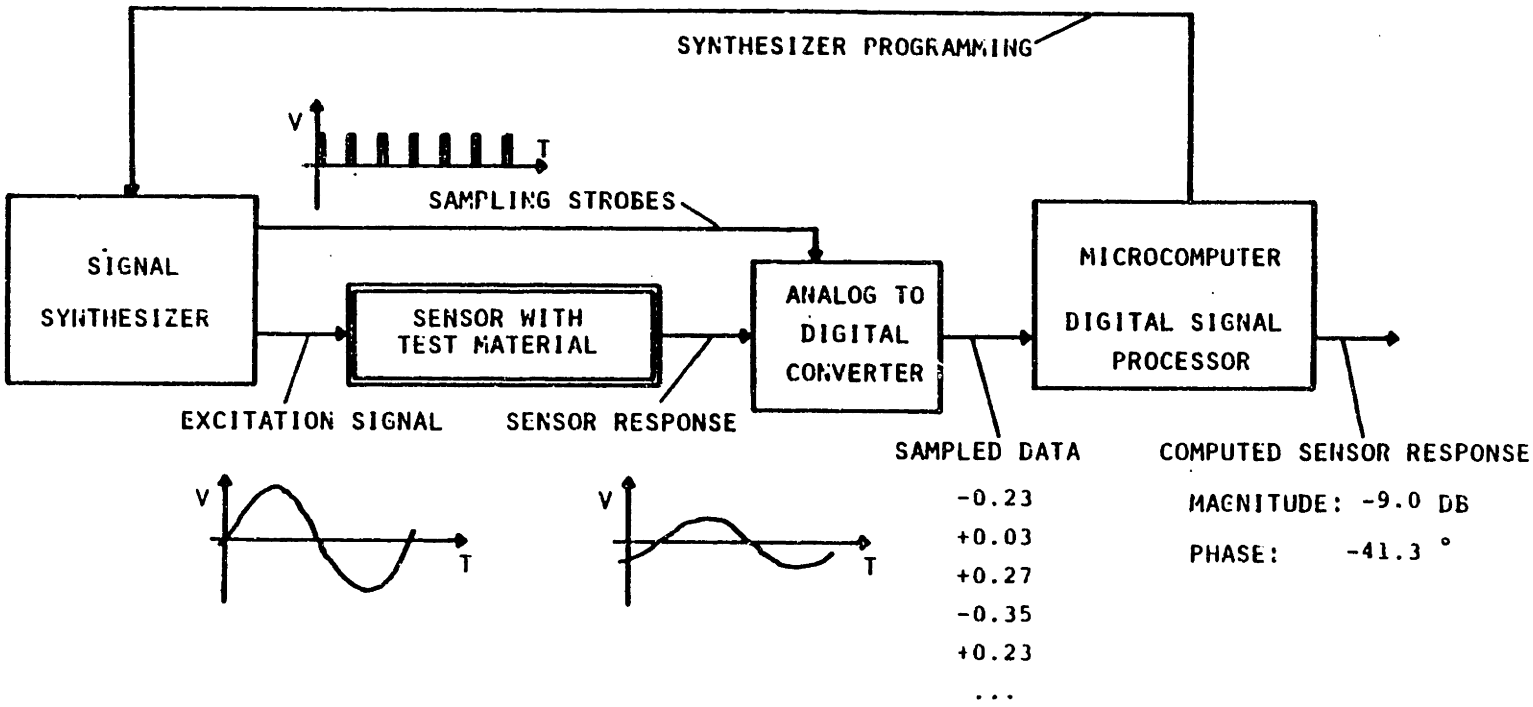


Figure 3.1 Block Diagram of Sampled Data System

affects the noise rejection of the system. The systematic error introduced by aliased high harmonics is analysed in detail in section 3.4, and the effect of noise is considered in section 4.1.

A microcomputer is included in the design shown in Figure 3.1 to implement all aspects of the digital signal processing. This processing involves both the selection or generation of an appropriate excitation waveform to be loaded into the synthesizer, and also the analysis of the sampled response data array gathered by the analog to digital converter, to find the magnitude and phase of the response. Additional software containing knowledge of the geometric and electric properties of the sensor can be added to allow the computer to estimate the underlying dielectric properties of the material under test. A hardware enhancement can be included if the processor calculation performance is poor, to increase the speed of the magnitude and phase analysis.

The digital signal processor analyses the array of samples of the response signal collected by the analog to digital converter, and calculates the magnitude and phase of each frequency component of interest. This transformation from a time sequence of samples to a frequency spectrum is typical of spectroscopic measurements [19]. Normally a computation of the discrete Fourier transform of the samples

is used to find the corresponding real and imaginary frequency spectrum samples. A fast Fourier transform (FFT) algorithm is typically implemented to efficiently calculate the discrete Fourier transform. Despite the efficiency of the FFT algorithm, the large sample array size used in this instrument to meet noise and harmonic performance requirements would require a special purpose processor to achieve an analysis time comparable to the data acquisition time.

In contrast to such applications as Fourier transform infrared spectroscopy, the dielectric properties measured by the sensor show fairly gradual variations as a function of frequency, and there is little interest in evaluating all available values of the frequency spectrum. For a sparse set of frequency samples, a simple correlation of the sampled response waveform with in-phase and quadrature template sinusoids at each frequency proves to be faster than evaluation of the entire transform using a FFT algorithm. The correlation operation can be efficiently programmed on the fairly low performance microcomputer used, while the "bit-reversal" array element scrambling required for the FFT algorithm [20] is particularly difficult to program efficiently on the microcomputer.

The included microprocessor greatly eases modifications to the instrument, since many changes can be implemented

through reconfiguration of the software rather than redesign of the hardware. In particular, the instrument can easily be arranged for use with any of the sensor configurations discussed in Chapter 2. In the case of the "voltage divider" or "integrator" configurations (sections 2.1.1 and 2.1.2) the system runs in a direct, single pass mode. The excitation signal is selected (from the experimenter's knowledge of the measurement conditions) and applied to the sensor. The response signal is then sampled and analysed to immediately find the frequency dependent magnitude and phase, which can be further analysed to evaluate the dielectric under test.

The "monolithic bridge" sensor configuration (discussed in section 2.1.3) requires multiple pass, feedback operation of the measurement instrument. Not shown explicitly in Figure 3.1 are additional excitation signal channels on the synthesizer. These additional channels are equivalent to the main excitation output, and generate signals of the same frequency, but with adjustable relative magnitudes and phases. The added signals are used as the "nulling" signals for the sensor. In this sensor configuration the bridge error output becomes the "response" signal. The sampled data analysis software is used to derive corrections to the synthesizer programming of the nulling signals. The software feedback loop can therefore servo the error output to zero. The nulling signals required to reach a null

implicitly describe the transfer function of the sensor, and allow the dielectric properties of the material under test to be evaluated.

An independent nulling signal frequency component is required for each frequency component in the excitation signal. This can be generated by individual output channels in the synthesizer, each of which introduces a different frequency sinusoidal waveform, or, a single nulling signal can be generated that contains a sum of the desired components. The hardware in the synthesizer that is shared between channels is rather small, so the hardware cost of separate nulling channels is high. More important, the sensor complexity, (particularly the added connections on the package), is undesirable. In a similar fashion, the speed penalty for software calculation to generate a single waveform containing the entire set of scaled and phase shifted components required is high. In either case, to implement the software driven nulling loop, a sequence of measurements must be made with an adjustment of the nulling waveform after each measurement of the residual error. The cycle is repeated until the error signal is negligible. The iterative technique is necessarily slower than measurements made using a direct analysis structure. The above penalties all weigh against the use of the bridge nulling technique.

3.4 Aliasing

The synthesizer generates a step approximation to a sinusoidal waveform. This excitation is applied to the assumed linear, real, continuous time system that is being analysed. The response waveform is sampled and correlated with template sinusoid and cosinusoid signals to extract the real and imaginary parts of the system response.

Because the excitation signal is generated in a sampled data environment and is periodic in time with a period that is commensurate with the sampling rate, the frequency spectrum of the excitation is also periodic. When this periodic signal spectrum is applied to the linear, continuous time system under test, the response waveform will have energy at every frequency represented in the excitation signal. The subsequent sampling of the response waveform will alias the various frequency components of the response, leading to an erroneous value for the supposed system response. The following analysis will quantify this error in the estimation of the response of the system under test.

3.4.1 Analysis of System Response

To simplify the analysis, a single frequency (sampled) signal will be used for excitation, of frequency ω_0 (ω_0 a positive integer.) There are N steps per period of the

excitation signal, as shown in Figure 3.2. Such a waveform can be modeled as a continuous time sinusoid, sampled and then filtered by a hold function. The resulting signal is applied to the system under test, as shown in Figure 3.3. The continuous time sinusoid is denoted x(t):

$$x(t) = \sin(\omega_0 t) \tag{3.1}$$

and has a Fourier transform:

$$X(\omega) = j\pi[\delta(\omega-\omega_0)-\delta(\omega+\omega_0)] \quad . \tag{3.2}$$

The sampling impulses occur every $2\pi/N$:

$$p(t) = \sum_{n=-\infty}^{\infty} \delta(t - \frac{n2\pi}{N}) \tag{3.3}$$

and the impulse train has a transform:

$$P(\omega) = N \sum_{n=-\infty}^{\infty} \delta(\omega-nN) \quad . \tag{3.4}$$

The sampled waveform y(t) is the product of x(t) and p(t). Recalling that multiplication in the time domain corresponds to convolution in the frequency domain:

$$Y(\omega) = \frac{1}{2\pi} X(\omega) * P(\omega) \quad . \tag{3.5}$$

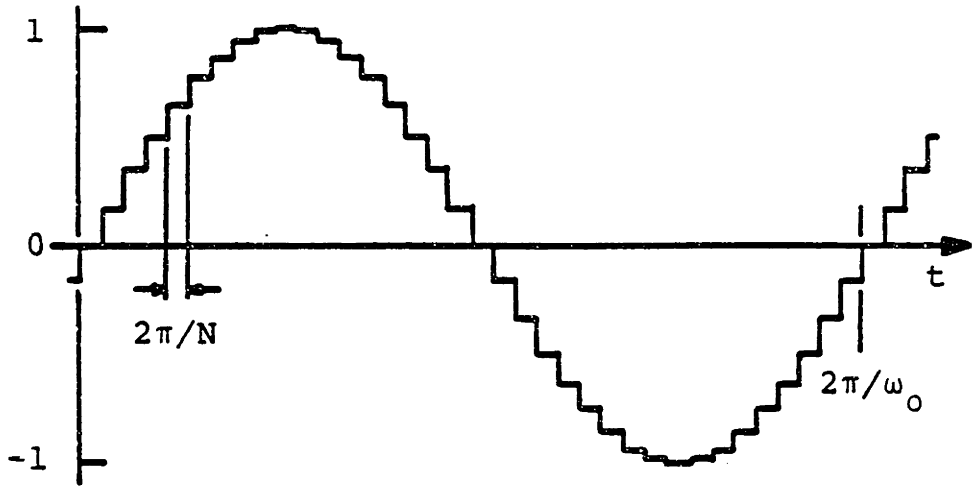


Figure 3.2 Synthesizer Excitation Signal

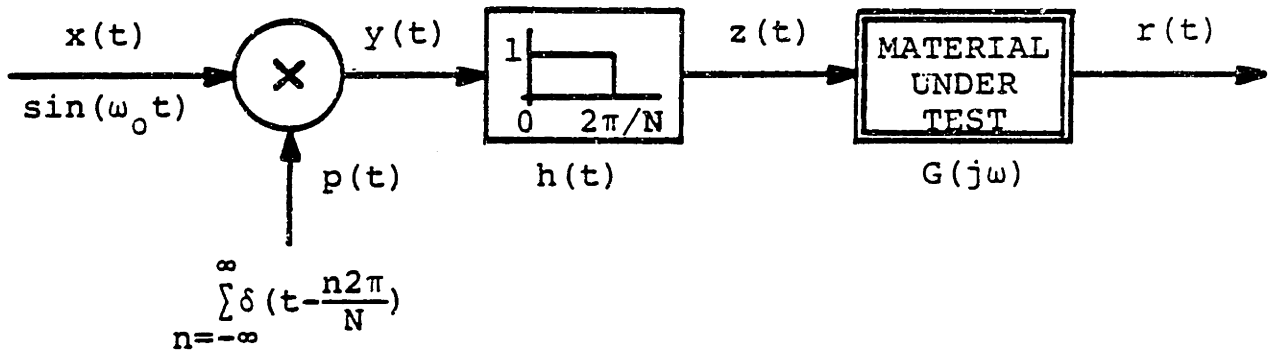


Figure 3.3 Model for Excitation Signal Synthesis

Therefore the transform of the sampled sinusoid is:

$$Y(\omega) = \frac{jN}{2} \sum_{n=-\infty}^{\infty} [\delta(\omega-\omega_0-nN) - \delta(\omega+\omega_0-nN)] \quad . \tag{3.6}$$

Now the signal is convolved with a hold filter that has impulse response:

$$h(t) = 1 \quad : \quad 0 \leq t < 2\pi/N \tag{3.7}$$

$$0 \quad : \text{otherwise}$$

and transform:

$$H(\omega) = \frac{2 \sin(\omega\pi/N)}{\omega} e^{-j\omega\pi/N} \quad . \tag{3.8}$$

This is the classic (sin x)/x response, with a time delay for causality. The frequency domain signals are multiplied to derive the spectrum of the excitation signal:

$$Z(\omega) = jN \sum_{n=-\infty}^{\infty} [\delta(\omega-\omega_0-nN) - \delta(\omega+\omega_0-nN)] \frac{\sin(\omega\pi/N)}{\omega} e^{-j\omega\pi/N} \quad . \tag{3.9}$$

The excitation signal is next applied to the system under test. Assume that the system function is G(ω). Multiply in the frequency domain to find the frequency spectrum of the response signal:

$$R(\omega) = jN \sum_{n=-\infty}^{\infty} [\delta(\omega-\omega_0-nN) - \delta(\omega+\omega_0-nN)] \frac{\sin(\omega\pi/N)}{\omega} e^{-j\omega\pi/N} G(\omega) \quad . \tag{3.10}$$

Now consider how the continuous time response signal is sampled and then correlated with template sinusoid and cosinusoid reference signals. Assume that the sampling and correlation can be delayed by an interval ε to counteract the delay introduced in the hold filter (see equation 3.7), and any residual delay in the system. Note that the sampling rate $M/2\pi$ need not equal the excitation rate $N/2\pi$. A block diagram of the analysis section of the instrument is shown in Figure 3.4. This block diagram can be rearranged to avoid one of the sampling multiplies. A windowing signal can remove the limits on the integrator and the ε delay can be included in the v(t) signal path. The overall block diagram model for the system is shown in Figure 3.5. In the following analysis, the signals associated with the sinusoidal correlation will be given a subscript (1), and those involved with the cosine correlation will have a subscript (2).

The reference sinusoid or cosinusoid can be represented by:

$$t_1(t) = \sin(\omega_0 t) \qquad (3.11a)$$

and:

$$t_2(t) = \cos(\omega_0 t) \quad . \qquad (3.11b)$$

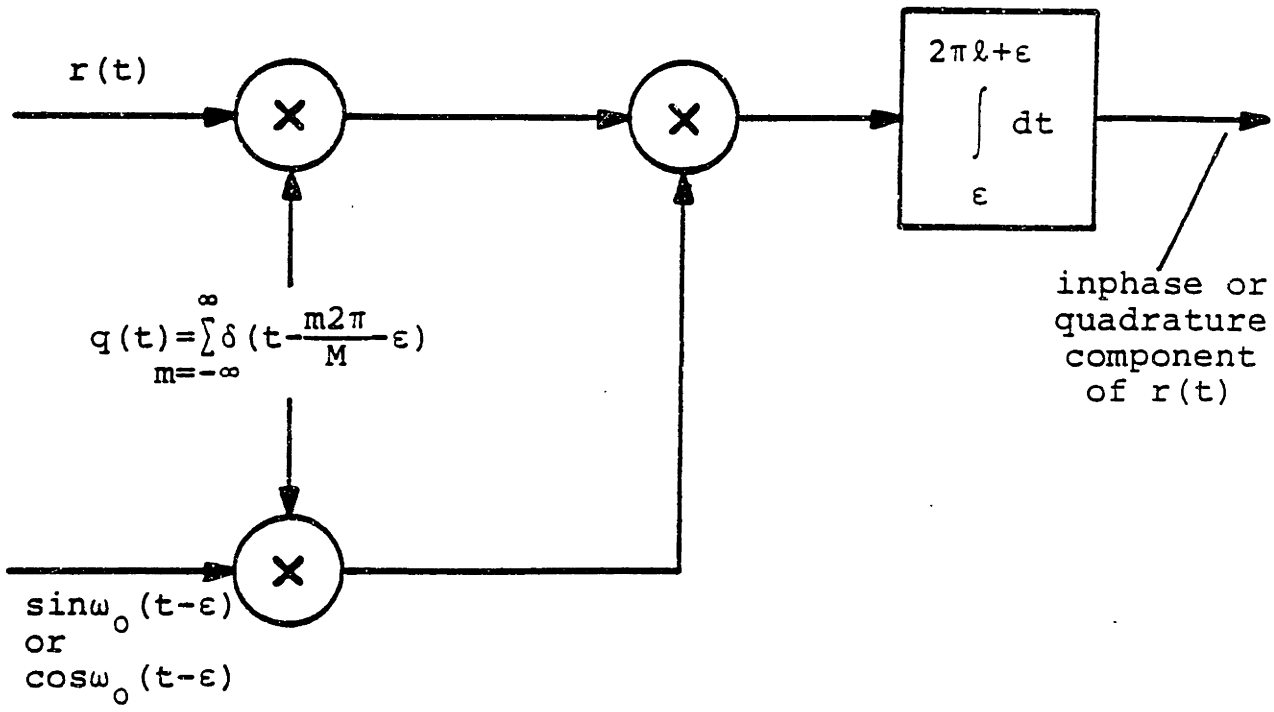


Figure 3.4 Model for Sensor Response Signal Analysis

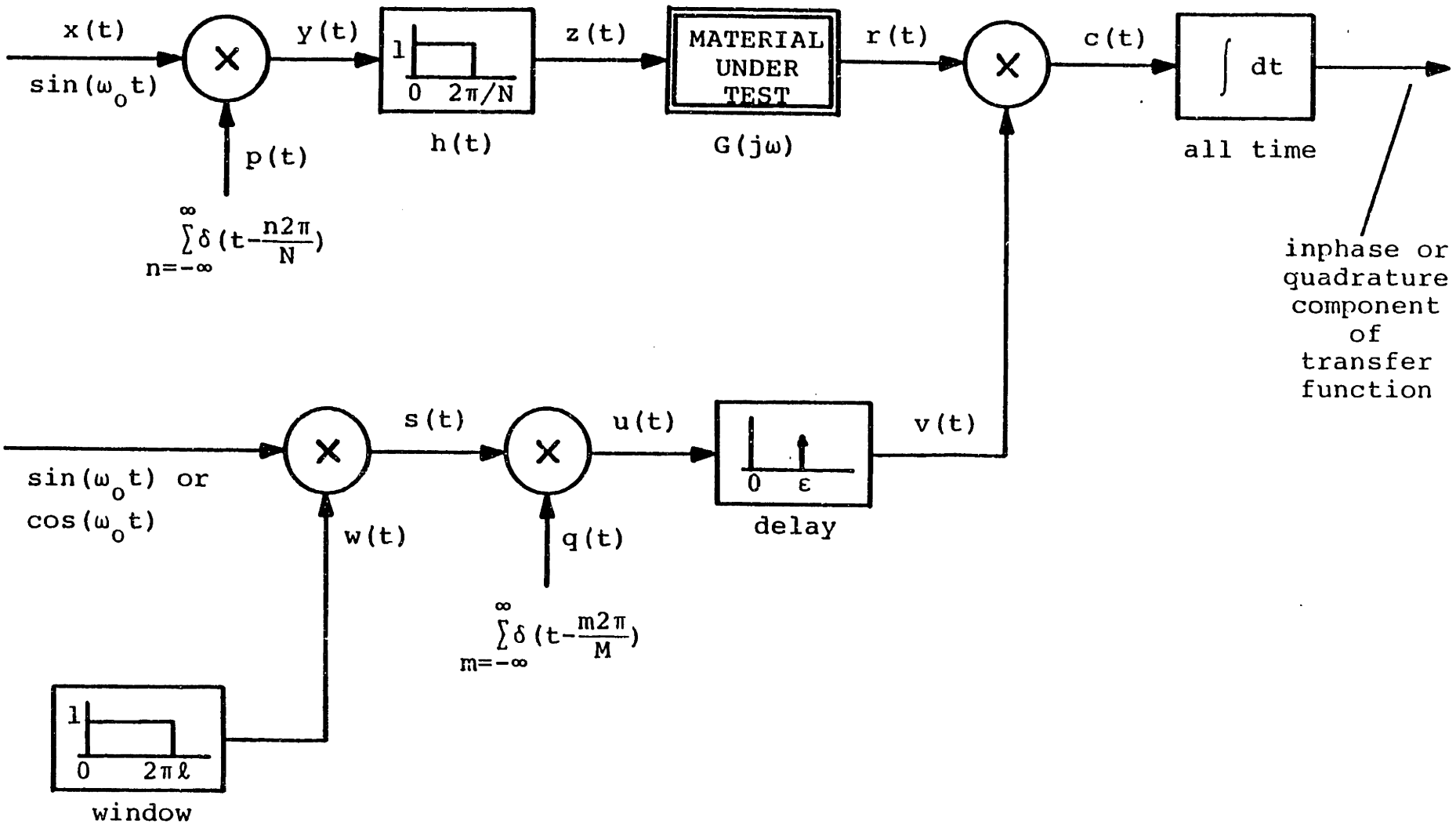


Figure 3.5 Model of Complete Sampled Data System

By analogy with (3.2) the corresponding transforms are:

$$T_1(\omega) = j\pi\left[\delta(\omega-\omega_0)-\delta(\omega+\omega_0)\right] \qquad (3.12a)$$

$$T_2(\omega) = \pi\left[\delta(\omega-\omega_0)+\delta(\omega+\omega_0)\right] \quad . \qquad (3.12b)$$

The reference signal is multiplied by the windowing function that has time response:

$$w(t) = \begin{cases} 1 & : 0 \leq t < 2\pi/ \\ 0 & : \text{otherwise} \end{cases} \qquad (3.13)$$

and as in (3.8) has the transform:

$$W(\omega) = \frac{2\sin(\omega\pi/)}{\omega} e^{-j\omega\pi/} \quad . \qquad (3.14)$$

The frequency response of the windowed signals can be found by convolution using the relationship used in (3.5) above:

$$S_1(\omega) = j\left[\frac{\sin\pi/(\omega-\omega_0)}{\omega-\omega_0} e^{-j(\omega-\omega_0)\pi/} - \frac{\sin\pi/(\omega+\omega_0)}{\omega+\omega_0} e^{-j(\omega+\omega_0)\pi/}\right] \qquad (3.15a)$$

$$S_2(\omega) = \left[\frac{\sin\pi/(\omega-\omega_0)}{\omega-\omega_0} e^{-j(\omega-\omega_0)\pi/} + \frac{\sin\pi/(\omega+\omega_0)}{\omega+\omega_0} e^{-j(\omega+\omega_0)\pi/}\right] \quad . \qquad (3.15b)$$

Next sample the signal every $2\pi/M$:

$$q(t) = \sum_{m=-\infty}^{\infty} \delta\left(t - \frac{m2\pi}{M}\right) \quad . \qquad (3.16)$$

The impulse train has a transform:

$$Q(\omega) = M \sum_{m=-\infty}^{\infty} \delta(\omega - mM) \quad . \tag{3.17}$$

The spectrum of the sampled signal is found by a convolution of $Q(\omega)$ with $S_1(\omega)$ and $S_2(\omega)$ similar to (3.5) above:

$$U_1(\omega) = \frac{1}{2\pi} \int_{-\infty}^{\infty} jM \sum_{m=-\infty}^{\infty} \left[\frac{\sin\pi((\omega'-\omega_0)}{\omega'-\omega_0} e^{-j(\omega'-\omega_0)\pi(} \delta(\omega-\omega'-mM) \right.$$
$$\left. - \frac{\sin\pi((\omega'+\omega_0)}{\omega'+\omega_0} e^{-j(\omega'+\omega_0)\pi(} \delta(\omega-\omega'-mM) \right] d\omega' \quad . \tag{3.18}$$

The delta function exists only when $\omega' = \omega - mM$:

$$U_1(\omega) = \frac{jM}{2\pi} \sum_{m=-\infty}^{\infty} \left[\frac{\sin\pi((\omega-\omega_0-mM)}{\omega-\omega_0-mM} e^{-j\pi((\omega-\omega_0-mM)} \right.$$
$$\left. - \frac{\sin\pi((\omega+\omega_0-mM)}{\omega+\omega_0-mM} e^{-j\pi((\omega+\omega_0-mM)} \right] \quad . \tag{3.19a}$$

Similarly:

$$U_2(\omega) = \frac{M}{2\pi} \sum_{m=-\infty}^{\infty} \left[\frac{\sin\pi((\omega-\omega_0-mM)}{\omega-\omega_0-mM} e^{-j\pi((\omega-\omega_0-mM)} \right.$$
$$\left. + \frac{\sin\pi((\omega+\omega_0-mM)}{\omega+\omega_0-mM} e^{-j\pi((\omega+\omega_0-mM)} \right] \quad . \tag{3.19b}$$

Next incorporate the ε time delay:

$$V_1(\omega) = \frac{jM}{2\pi} \sum_{m=-\infty}^{\infty} \left[\frac{\sin\pi((\omega-\omega_0-mM)}{\omega-\omega_0-mM} e^{-j\pi((\omega-\omega_0-mM)} e^{-j\varepsilon\omega} - \frac{\sin\pi((\omega+\omega_0-mM)}{\omega+\omega_0-mM} e^{-j\pi((\omega+\omega_0-mM)} e^{-j\varepsilon\omega} \right] \quad (3.20a)$$

and:

$$V_2(\omega) = \frac{M}{2\pi} \sum_{m=-\infty}^{\infty} \left[\frac{\sin\pi((\omega-\omega_0-mM)}{\omega-\omega_0-mM} e^{-j\pi((\omega-\omega_0-mM)} e^{-j\varepsilon\omega} + \frac{\sin\pi((\omega+\omega_0-mM)}{\omega+\omega_0-mM} e^{-j\pi((\omega+\omega_0-mM)} e^{-j\varepsilon\omega} \right] . \quad (3.20b)$$

Now the response signal r(t) (equation 3.10) must be multiplied by the windowed, sampled and delayed template signals $v_1(t)$ and $v_2(t)$. Since the analysis is being done in the frequency domain, this calls for another convolution:

$$C_1(\omega) = \frac{jjMN}{(2\pi)^2} \int_{-\infty}^{\infty} \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} [\, AC - AD - BC + BD \,]\, d\omega' \quad (3.21a)$$

and:

$$C_2(\omega) = \frac{jMN}{(2\pi)^2} \int_{-\infty}^{\infty} \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} [\, AC + AD - BC - BD \,]\, d\omega' \quad (3.21b)$$

where:

$$A = \delta(\omega'-\omega_0-nN) \frac{\sin(\omega'\pi/N)}{\omega'} e^{-j\omega'\pi/N} G(\omega') \quad (3.21c)$$

$$B = \delta(\omega'+\omega_0-n\dot{N})\ \frac{\sin(\omega'\pi/N)}{\omega'}\ e^{-j\omega'\pi/N}\ G(\omega') \qquad (3.21d)$$

$$C = \frac{\sin\pi[(\omega-\omega'-\omega_0-m\dot{M})}{\omega-\omega'-\omega_0-m\dot{M}}\ e^{-j\pi[(\omega-\omega'-\omega_0-m\dot{M})}\ e^{-j\varepsilon(\omega-\omega')} \qquad (3.21e)$$

$$D = \frac{\sin\pi[(\omega-\omega'+\omega_0-m\dot{M})}{\omega-\omega'+\omega_0-m\dot{M}}\ e^{-j\pi[(\omega-\omega'+\omega_0-m\dot{M})}\ e^{-j\varepsilon(\omega-\omega')} \qquad (3.21f)$$

The correlation integral as defined above is over all time. By the definition of the transform integral:

$$X(\omega) = \int_{-\infty}^{\infty} x(t)\ e^{-j\omega t}\ dt \qquad \text{so:} \qquad X(0) = \int_{-\infty}^{\infty} x(t)\ dt$$

and the result of the correlation operation can be found by evaluating the spectral analysis function at $\omega = 0$. Assume that the response waveform is sampled only every "a" steps of the excitation waveform where "a" is a positive integer. This will constrain the delta functions in equations (3.21c) through (3.21f) above. The term (3.21c) exists only when $\omega' = \omega_0 + naM$. For this value of ω':

$$C = \frac{\sin\pi[(-2\omega_0-(m+na)M)}{-2\omega_0-(m+na)M}\ e^{-j\pi[(-2\omega_0-(m+na)M)}\ e^{-j\varepsilon(-\omega_0-naM)} \qquad (3.22a)$$

and:

$$D = \frac{\sin\pi[(-(m+na)M)}{-(m+na)M}\ e^{-j\pi[(-(m+na)M)}\ e^{-j\varepsilon(-\omega_0-naM)} \qquad (3.22b)$$

Equivalently, the term (3.21d) exists for $\omega' = -\omega_0 + naM$. Substituting in the value of ω':

$$C = \frac{\sin\pi\ell((-(m+na)M)}{-(m+na)M} e^{-j\pi\ell((-(m+na)M)} e^{-j\varepsilon(\omega_0-naM)} \qquad (3.22c)$$

and:

$$D = \frac{\sin\pi\ell((2\omega_0-(m+na)M)}{2\omega_0-(m+na)M} e^{-j\pi\ell((2\omega_0-(m+na)M)} e^{-j\varepsilon(\omega_0-naM)} . \qquad (3.22d)$$

By the original statement of the problem, the variables ℓ, ω_0, m, n, a, and M are all non-zero integer. This forces (3.22a) and (3.22d) to be zero. In addition, (3.22b) and (3.22c) only exist when $m = -na$. Finally, if the adjustable delay term ε is set equal to π/N, the linear phase term vanishes. The correlation outputs found above (3.21a,b) can be re-written in the form:

$$C_1 = \frac{NM\ell}{4\pi} \sum_{n=-\infty}^{\infty} \left[\frac{\sin((\omega_0+nN)\pi/N)}{\omega_0+nN} G(\omega_0+nN) + \frac{\sin((-\omega_0+nN)\pi/N)}{-\omega_0+nN} G(-\omega_0+nN) \right] \qquad (3.23a)$$

and similarly:

$$C_2 = \frac{jNM\ell}{4\pi} \sum_{n=-\infty}^{\infty} \left[\frac{\sin((\omega_0+nN)\pi/N)}{\omega_0+nN} G(\omega_0+nN) - \frac{\sin((-\omega_0+nN)\pi/N)}{-\omega_0+nN} G(-\omega_0+nN) \right] . \qquad (3.23b)$$

Noting that n is integer and rearranging the signs of the second term in (3.23), the following trigonometric identities can be used to simplify the result:

$$\sin((\omega_0+nN)\pi/N) = (-1)^n \sin(\omega_0\pi/N) \qquad (3.24a)$$

$$\sin((-\omega_0+nN)\pi/N) = -(-1)^n \sin(\omega_0\pi/N) \quad . \qquad (3.24b)$$

This leads to:

$$C_1 = \frac{NM\ell}{4\pi} \sin(\omega_0\pi/N) \sum_{n=-\infty}^{\infty} (-1)^n \left[\frac{G(\omega_0+nN)}{\omega_0+nN} + \frac{G(-\omega_0+nN)}{\omega_0-nN} \right] \qquad (3.25a)$$

and:

$$C_2 = \frac{jNM\ell}{4\pi} \sin(\omega_0\pi/N) \sum_{n=-\infty}^{\infty} (-1)^n \left[\frac{G(\omega_0+nN)}{\omega_0+nN} - \frac{G(-\omega_0+nN)}{\omega_0-nN} \right] \qquad (3.25b)$$

The sums can be rewritten as:

$$C_1 = \frac{NM\ell}{4\pi} \sin(\omega_0\pi/N) \left[\frac{G(\omega_0) + G(-\omega_0)}{\omega_0} + \sum_{n=1}^{\infty} (-1)^n \left[\frac{G(\omega_0+nN)+G(-\omega_0-nN)}{\omega_0+nN} + \frac{G(\omega_0-nN)+G(-\omega_0+nN)}{\omega_0-nN} \right] \right] \qquad (3.26a)$$

and:

$$C_2 = \frac{jNM\ell}{4\pi} \sin(\omega_0\pi/N) \left[\frac{G(\omega_0) - G(-\omega_0)}{\omega_0} + \sum_{n=1}^{\infty} (-1)^n \left[\frac{G(\omega_0+nN)-G(-\omega_0-nN)}{\omega_0+nN} - \frac{G(\omega_0-nN)-G(-\omega_0+nN)}{\omega_0-nN} \right] \right] . \qquad (3.26b)$$

If the signs in the second term of each of the above sums are rearranged, then the correlated outputs can be written in terms of the real and imaginary parts of the test system function. Recall:

$$X(\omega) + X(-\omega) = 2\,\mathrm{Re}[X(\omega)]$$

$$X(\omega) - X(-\omega) = 2j\,\mathrm{Im}[X(\omega)] \quad .$$

So the sinusoidal correlation is found to be:

$$C_1 = \frac{NM\ell}{2\pi} \sin(\omega_0\pi/N) \left[\frac{\mathrm{Re}[G(\omega_0)]}{\omega_0} + \sum_{n=1}^{\infty} (-1)^n \left[\frac{\mathrm{Re}[G(nN+\omega_0)]}{nN+\omega_0} - \frac{\mathrm{Re}[G(nN-\omega_0)]}{nN-\omega_0} \right] \right] \qquad (3.27a)$$

and the cosinusoidal correlation is:

$$C_2 = \frac{NM\ell}{2\pi} \sin(\omega_0\pi/N) \left[\frac{\mathrm{Im}[G(\omega_0)]}{\omega_0} + \sum_{n=1}^{\infty} (-1)^n \left[\frac{\mathrm{Im}[G(nN+\omega_0)]}{nN+\omega_0} - \frac{\mathrm{Im}[G(nN-\omega_0)]}{nN-\omega_0} \right] \right] \quad .(3.27b)$$

The above estimates (3.27a,b) of the response of the system under test can be compared with an "ideal" instrument. In such an instrument, sampling "ℓ" cycles with M points per cycle, the correlation results would be of the form:

$$C_1(\mathrm{ideal}) = \frac{M\ell}{2} \mathrm{Re}[G(\omega_0)] \qquad (3.28a)$$

and:

$$C_2(\text{ideal}) = \frac{M\ell}{2} \, \mathrm{Im}[G(\omega_0)] \quad . \tag{3.28b}$$

The "fundamental" term in the estimate differs from the ideal response only by a (sin x)/x term. This term approaches unity if ω_0 is small compared with N. The additional terms that make up the sum are of cancelling sign, and are small if N is large compared to ω_0. The error introduced by these terms will be estimated next.

3.4.2 Estimate of Error Due to Aliasing

The stepped nature of the excitation signal that is applied to the sensor will cause aliasing when the response signal is subsequently sampled. The previous section derived an expression for this error term, as a function of the sampling parameters and the spectral response of the sensor and material under test. The expression includes an infinite sum, and can not be solved in closed form for an arbitrary spectral response. Instead, a computer program was written to estimate the error under the simplifying assumption that the sensor could be modeled as a single pole low pass filter. The low pass characteristic is typical of materials under test, and certainly the spectral energy of the excitation waveform will eventually roll off, due to the limited bandwidth of the remaining circuitry in the system. In the event that the response exhibits a resonance that

matches the frequency of one of the terms in the sum, the error could be greater.

The program evaluates the correlations in equations (3.27a,b) including terms in the sum until the effect of each additional term becomes negligible. The error attributed to aliasing is defined as the change in the evaluated magnitude and phase between when these are calculated from the sum, and the result of a calculation including just the "fundamental" term. The results of the computer simulation are shown in Table 3.1.

TABLE 3.1

Error in Estimated Magnitude and Phase due to Aliasing

N	$\lvert\delta_M\rvert$ (db)	f_M	$\lvert\delta_P\rvert$ (deg)	f_P
3.6	1.5	~8	2.75	~2
36	0.013	~50	0.047	~20
360	<0.001	-	0.001	~200
3600	<0.001	-	<0.001	-

The error indicated is the maximum value found over the range of 0.01 to 900 for the ratio of the low pass breakpoint to the excitation frequency. The number "N" is the number of steps per cycle of the excitation signal. As this number is increased, the magnitude of each individual

step decreases, and the error due to aliasing of the response decreases rapidly. δ_M and f_M are the worst case error in magnitude and the ratio of filter cutoff to excitation frequency at which it occurs, while δ_P and f_P are the corresponding values for the phase. The digital signal processing system described in section 3.3 has been designed with a minimum of 36 steps per cycle at the highest frequency used (10 kHz), increasing to 3600 steps per cycle at lower excitation frequencies. This limits the error due to aliasing to less than 0.02 decibels and 0.05 degrees at all frequencies. It should be noted again that the above calculations assumed a low pass characteristic for the sensor system response.

3.4.3 Techniques for Reducing Aliased Harmonics

The errors calculated from the above analysis are within the specifications of the instrument and are similar to the uncertainty introduced by noise. Therefore no additional hardware was included in the design to increase the performance of the synthesizer. If it were necessary, there are several techniques available to reduce errors that can be incorporated within the general synthesizer and sampled data signal processing design. First, the step size can be reduced by an increase in the number of steps per cycle of the excitation signal. A second choice is to low pass filter the output of the synthesizer to eliminate the

undesired harmonics. As a third alternative, additional circuitry can be included in the synthesizer so that the output voltage does not instantaneously step from one value to the next, but rather performs a linear or higher order interpolation between successive output points.

An increase in the number of steps per cycle of the excitation waveform requires a corresponding increase in the clock rate of the synthesizer, and in the size of the stored data array that defines the waveform. A higher speed digital to analog converter is necessary, and extra memory on the synthesizer. In addition, the time required for the processor to generate a waveform consisting of several frequency components may increase excessively. The present system takes approximately 0.5 second per frequency component to generate and load a waveform. This time increases in direct proportion to an increase in the size of the data array.

The use of a low pass filter to reduce the high frequency harmonic energy is simple, but will introduce a frequency dependent phase shift (and to a lesser degree an amplitude reduction) in the excitation signal. The size of this perturbation will vary as different synthesizer fundamental frequencies are selected. In addition, the characteristics of the filter will depend on the initial tolerance of the analog components used to build the filter,

and will shift due to the long term instability of these components. The above effects introduce difficulties in calibration of the filter, and it is necessary to incorporate an automatic calibration technique for the measurement system. This calibration consists of sampling data from both the excitation and the response waveforms, and analysing the relative magnitude and phase between the signals. The technique requires either two analog to digital converters triggered simultaneously, or sequential measurement of the two waveforms [21]. The first of these possibilities impacts the system cost and complexity, the second doubles the data acquisition time, and both choices increase the time required to perform the correlation analysis.

The third technique suggested above is to modify the synthesizer so that instead of the output changing by discrete steps, it passes more smoothly from one value to the next. The simplest enhancement is to perform a linear interpolation between successive array values. Two digital to analog converters are used to generate the output waveform, updated alternately from the excitation waveform data array in a "leap-frog" fashion (one converter receives data from "odd" array elements on "odd" clock cycles, the other from "even" addresses on "even" cycles). The converter outputs are combined to deliver the actual

synthesizer output. To produce a linear interpolation is is necessary to generate an output of the form:

$$\text{Output} = \frac{(1-\alpha)}{2}\,\text{DAC}_{\text{even}} + \frac{(1+\alpha)}{2}\,\text{DAC}_{\text{odd}} \qquad (3.29)$$

where DAC_{even} is the output from the "even" digital to analog converter and DAC_{odd} is the output from the "odd" DAC. The coefficient "α" is a triangle wave signal that sweeps between -1 and +1 with period equal to twice the time between synthesizer sampling impulses (recall from equation 3.3 that the synthesizer clock period is $2\pi/N$):

$$\alpha(t) = \frac{Nt}{\pi} - 1 - 4b \quad : \frac{2\pi}{N}(2b) \leq t < \frac{2\pi}{N}(2b+1) \qquad (3.30)$$

$$- \frac{Nt}{\pi} + 3 - 4b \quad : \frac{2\pi}{N}(2b+1) \leq t < \frac{2\pi}{N}(2b+2) \quad .$$

(b is integer)

The block diagram for the interpolation circuit is shown in Figure 3.6 and a sketch of the signal "α" can be seen in Figure 3.7. It is important to note that each DAC output changes at the instant that it makes no contribution to the output. This has the convenient benefit of removing DAC output glitches from the synthesizer output. A circuit that implements the interpolation function of Figure 3.6 is similar to the topology used in conventional four-quadrant multipliers [22].

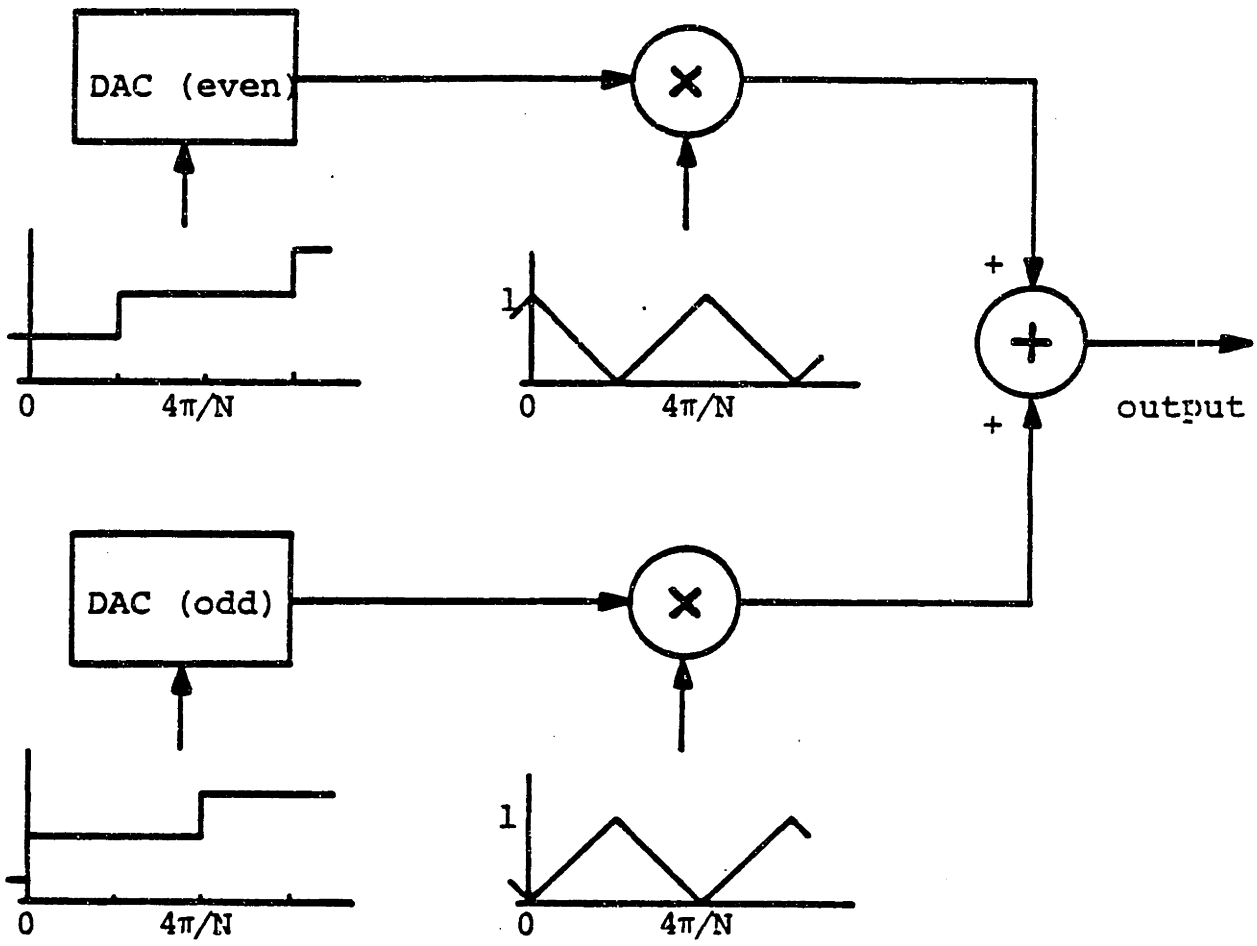


Figure 3.6 Model of Interpolation Synthesizer

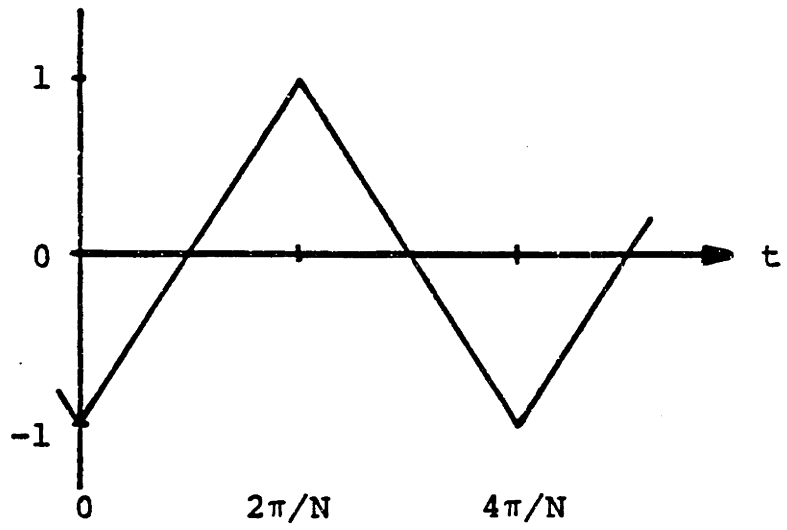


Figure 3.7 Triangle Wave used in Interpolation Synthesizer

The triangle wave signal "a" is difficult to generate. The period and therefore the slope of the waveform must vary over several orders of magnitude depending on the output frequency of the synthesizer, but the extrema of the triangle must remain accurate to avoid gross distortion of the final excitation signal. A good approximation to the desired triangle can be generated by a low resolution (less than eight bit) digital to analog converter driven at a corresponding multiple of the synthesizer clock. This is an implementation similar in spirit to the two stage flash converters often used as a compromise between complexity and speed [23]. The small DAC must be high speed, but is only required to have sufficient resolution that the harmonic energy in the new small steps be less than the residual error from the linear interpolation.

The harmonic energy produced by a synthesizer using linear interpolation can be estimated by comparison with the original "stepped" output. The hold filter h(t) (equation 3.7) in the model must now be replaced by a triangular filter:

$$h_T(t) = \begin{cases} \frac{Nt}{2\pi} + 1 & : -\frac{2\pi}{N} \leq t < 0 \\ -\frac{Nt}{2\pi} + 1 & : 0 \leq t < \frac{2\pi}{N} \\ 0 & : \text{otherwise} \end{cases} \qquad (3.31)$$

which has a transform:

$$H(\omega) = \frac{2N \sin^2(\omega\pi/N)}{\pi\omega^2} \quad . \tag{3.32}$$

This filter term carries through the analysis in the same fashion that equation 3.8 propagated through the analysis of the "stepped" waveform. The harmonic terms in this case are reduced by a factor of $(nN \pm \omega_0)^2$ as compared with $(nN \pm \omega_0)^1$ for the stepped waveform. Table 3.2 shows the errors in magnitude and phase measurement due to aliasing for the linear interpolation synthesizer. In the case of the minimum 36 element per cycle waveform chosen for the standard design, the error due to aliasing is limited to 0.001 decibel and 0.002 degree at all frequencies.

TABLE 3.2

Error in Estimated Magnitude and Phase due to Aliasing for Linear Interpolation Synthesizer

N	$\lvert\delta_M\rvert$ (db)	f_M	$\lvert\delta_P\rvert$ (deg)	f_P
3.6	0.85	~7	1.48	~2
36	0.001	~400	0.002	~20
360	<0.001	-	<0.001	-
3600	<0.001	-	<0.001	-

3.4.4 Summary of Aliasing Issues

The synthesizer generates an output waveform that only approximates the ideal signal, due to the finite number of array elements. The error is manifested as added high order harmonics on the signal. The energy at these frequencies produces aliasing upon subsequent sampling of the sensor response signal. The effect of this error on magnitude and phase measurements has been analysed, and estimated assuming that the sensor and material under test can be modeled as a single pole low pass filter. The chosen design of the synthesizer is found to introduce less than 0.02 decibels and 0.05 degrees of error in the magnitude and the phase measurements, respectively.

CHAPTER 4

System Performance

This chapter presents the results and analysis of performance measurements of the dielectric measurement system consisting of the sensor chip designs discussed in Chapter 2 and the instrumentation described in Chapter 3. Measurements have been made to determine noise, harmonic and intermodulation distortion in the major subsystems, and system measurement speed.

One performance measure, the ultimate sensitivity of the instrument, is limited by several factors, including noise and distortion. The first section of the chapter discusses noise in the system and the resulting limits on measurement sensitivity. The following section analyses distortion in the instrument and the sensor, and demonstrates the capabilities of the system for the measurement of sample non-linearity. Another performance specification is the measurement speed. The third section discusses the measurement speed of the instrument under a variety of choices for the set of excitation frequencies.

4.1 System Noise Performance

The noise analysis of the system proceeds on two separate paths. First, experimental results measured by three different techniques are used to derive the underlying noise energy in the sampled data measurement subsystem. Second, a priori estimates of the noise sources in the subsystem are used to make a prediction for the expected noise performance. The results of these two alternative analyses are compared, and reasons for any discrepencies are noted. In the final section, the noise performance of the sensor subsystem is characterized.

4.1.1 Experimental Results

These experiments measure the noise performance of the subsystem consisting of only the excitation waveform synthesizer, the response signal sampler, and the analysis software. The sensor, di ectric material and sensor support electronics were removed so that the ultimate noise performance of the basic magnitude and phase measurement instrument could be evaluated. Three somewhat different techniques were used. The first and most direct of these is simply to "ground" the response signal input, and then make measurements of the magnitude of the "response" as a function of frequency. The two alternate techniques observe the perturbing effect of the system noise when making a

measurement of each of the magnitude and the phase of a known reference signal, as the reference signal is varied in magnitude. As before, the measurements are made as a function of frequency. For a large reference signal, the additive noise will introduce only a small standard deviation in a set of measurements of the reference. As the reference signal level is reduced, the signal to noise ratio will decrease correspondingly, and the standard deviation of measurements of the reference plus noise will increase.

The synthesizer is designed to allow the magnitude (and the phase) of the excitation signal to be adjusted under software control for use with the "bridge nulling" sensor design. The adjustable excitation signal can therefore be used as a programmable precision magnitude reference. Ideally, one would like to measure the reference signal as a dependent variable, with a particular standard deviation (due to the noise) as the independent variable. This is not feasible with the instrumentation. Instead, a large, closely spaced set of reference signal levels is selected. Each level is measured a sufficient number of times to establish an estimate of the standard deviation of the measurement. The reference level that most closely approximates (from above) the desired deviation is chosen. For these measurements, the reference signal level was stepped in 5 decibel increments. All signal levels are

referenced such that zero decibels corresponds to a one volt sinusoidal waveform (two volts peak to peak).

The tests are repeated over a large set of frequencies to observe the spectral distribution of the noise. If the underlying noise source has a spectrum that is white, the sampled (and aliased) noise will again approximate a white noise source. However, noise sources related to the synthesizer or the correlation detector could introduce a frequency dependent component. The background noise from a grounded response input is shown in Figure 4.1. Figure 4.2 plots contours of the level of the reference signal for constant magnitude perturbations, for perturbations of 0.01 decibel and 0.1 decibel. In Figure 4.3 is a similar plot, but showing contours of constant phase perturbation, for perturbations of 0.01, 0.1 and 1 degree. All three plots are reasonably flat, indicating a constant noise spectral density and supporting the contention that the noise can be modeled as white noise over the measured frequency range.

The average magnitude of the noise, estimated from Figure 4.1, is -102 decibels (as always, relative to one volt). Arriving at an estimate for the noise magnitude from the data in Figure 4.2 is a bit more complex. It is assumed that the signal to noise ratio is large. With this approximation, the variance of the signal plus additive noise is equal to the variance of the noise alone. A

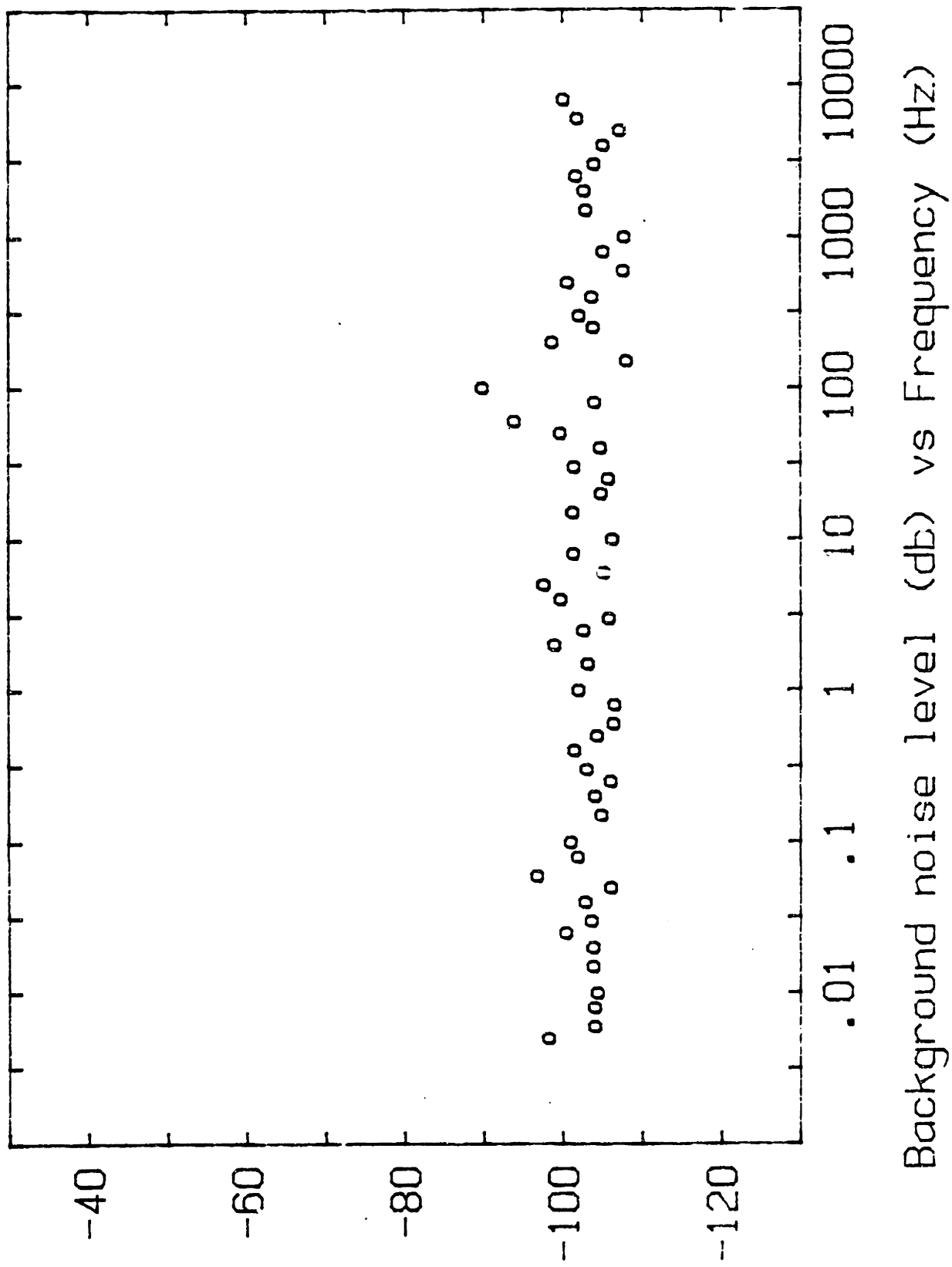


Figure 4.1 Background Noise Magnitude with Grounded Input

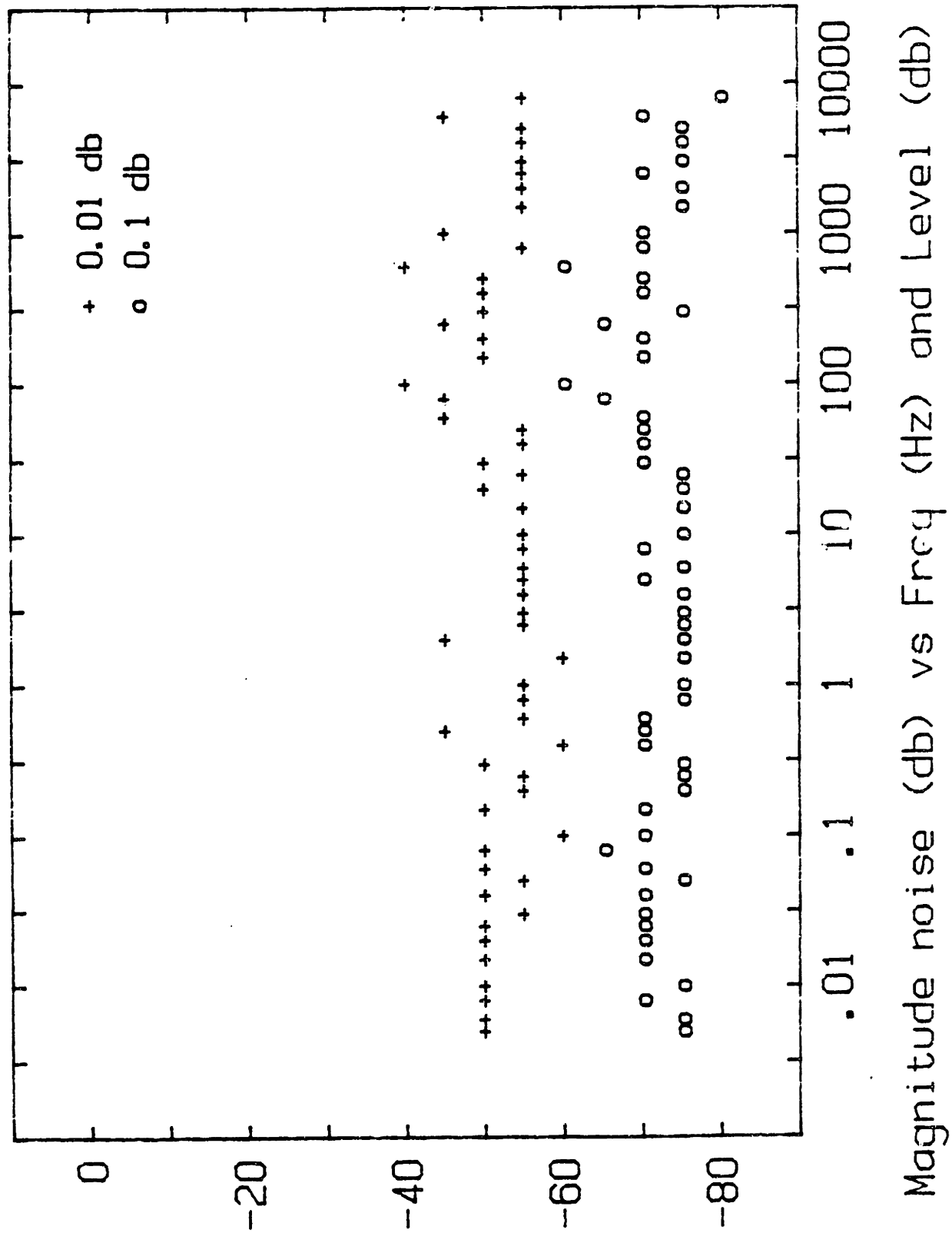


Figure 4.2 Contours of Constant Magnitude Noise

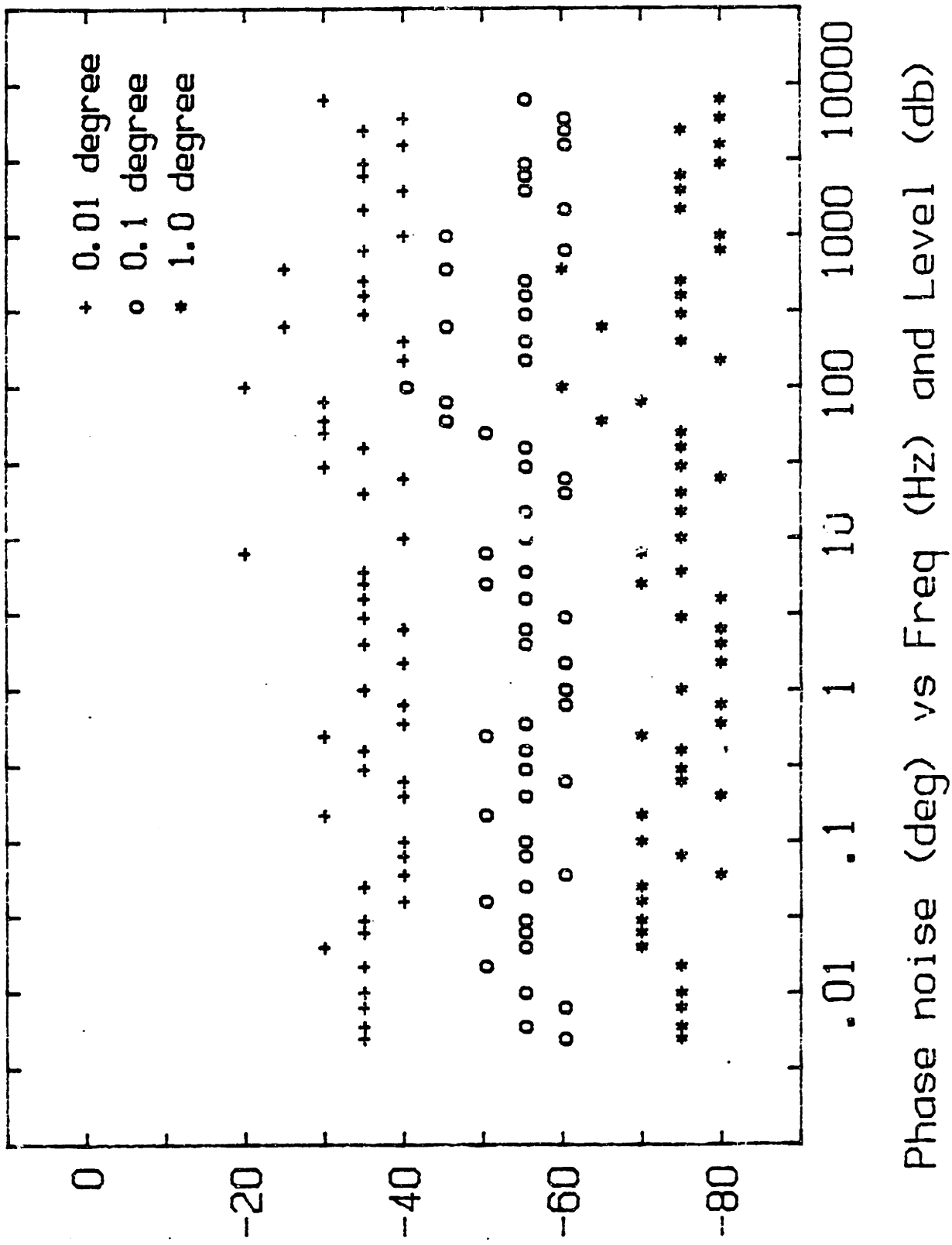


Figure 4.3 Contours of Constant Phase Noise

measured standard deviation of 0.01 decibel, for example, corresponds to a variation in signal plus noise magnitude by a factor of 1.0012. The noise magnitude of 0.0012 is equivalent to an in-phase noise signal 58.8 decibels below the reference signal. In similar fashion, a standard deviation of 0.1 decibel implies an in-phase noise signal at a level 38.8 decibels below the reference. The noise is assumed to be white, (and therefore independent of the reference), so the in-phase and quadrature components of the noise with respect to the signal are independent. The total noise power is then twice that in the in-phase component alone.

A similar analysis is used for the phase variation data shown in Figure 4.3. Again it is assumed that the signal to noise ratio is large, so that the variation of the measured phase is small. For these small angles, the tangent of the angle is almost equal to the angle itself. The tangent of the angle is equal to the ratio of the noise that is in quadrature to the reference signal, to the reference signal. As in the previous measurement, the total noise power is twice that in the quadrature component. A summary of the results from Figures 4.1, 4.2 and 4.3 is listed in Table 4.1. The estimates cluster closely around a value of -106 decibels, or 4.9 microvolts.

TABLE 4.1

Experimental Measurements of System Noise Magnitude

Measurement Technique		Signal Level (db)	SNR (db)	Estimated Noise (db)
Direct (grounded input)		-102.3	0	-102.3
Magnitude deviation	0.01 db	-51.6	55.8	-107.4
	0.1 db	-71.6	35.8	-107.4
Phase deviation	0.01 degree	-34.9	72.2	-107.1
	0.1 degree	-54.4	52.2	-106.5
	1. degree	-74.5	32.2	-106.6
Average				-106

4.1.2 Performance With White Noise

The expected noise performance of the sampled data magnitude and phase measurement system is first estimated assuming that the total effect of all noise sources can be modeled by a single "white" noise source connected to the response input of the system. The analysis can be performed in the frequency or time domain. A frequency domain calculation requires evaluation of the spectral response of the system including the effect of aliasing of high frequency noise components. In the present case, it is more effective to evaluate the characteristics of the sampled data system in the time domain [24]. The measurement system

is assumed to be linear, so the effect of additive noise can be analysed by considering the noise alone.

Referring back to Figure 3.4, the sampled data system generates a correlation output by taking the sum of a product of two trains of impulses. The first train consists of samples of the input waveform while the second set of impulses is the template sinusoidal waveform. There are "M" impulses per cycle of the reference, and "ℓ" cycles, so the noise voltage is:

$$\text{noise} = \sum_{i=0}^{M\ell-1} n_i \quad , \tag{4.1}$$

where the n_i are the noise samples. The noise energy is the mean square:

$$\text{expected energy} = \overline{\text{noise}^2} = \overline{\sum_{i=0}^{M\ell-1} n_i \sum_{j=0}^{M\ell-1} n_j} \quad . \tag{4.2}$$

Since the noise is white, the samples are independent and identically distributed, and:

$$\overline{n_i n_j} = 0 \quad \text{unless} \quad i = j \quad . \tag{4.3}$$

Therefore,

$$\overline{\text{noise}^2} = M\overline{n^2} \quad . \tag{4.4}$$

It is assumed that the incoming noise is bandlimited to frequencies within the range of ±W, and has spectral density $N_0/2$. Then

$$\overline{n^2} = WN_0 \tag{4.5}$$

and the magnitude of the noise voltage is:

$$V_n = (MWN_0)^{\frac{1}{2}} \quad . \tag{4.6}$$

The noise signal is multiplied separately by the sinusoidal and cosinusoidal template waveforms. One half of the noise energy will correlate with each template, but the total magnitude calculated by the measurement system is the sum of the energy in the in-phase and quadrature correlations. The result for the noise sensitivity found in equation 4.6 must now be compared with the sensitivity of the system to a pure sinusoidal signal, to arrive at a measure of the noise rejection of the instrument.

If a pure sinusoid is applied to the sampling input, the correlation output will consist of a sum of impulses formed as the product of the input and the template sine waves. It is assumed that the frequencies are equal, and

without loss of generality one can assume the relative phase is zero. The correlation output will then be:

$$V_s = \sum_{i=0}^{M\ell-1} \sin^2(2\pi\omega_o i/M) \quad . \tag{4.7}$$

Since ω_o is defined to be a positive integer (see section 3.4.1), equation 4.7 simplifies to:

$$V_s = \frac{M\ell}{2} \quad . \tag{4.8}$$

The measurement system scales the output so that a unity magnitude sine wave will be measured as such. Therefore the measured magnitude of the noise signal with spectral density N_o bandlimited to $\pm W$ will be:

$$M_n = \left[\frac{4WN_o}{M\ell} \right]^{\frac{1}{2}} \quad . \tag{4.9}$$

4.1.3 Noise from Quantization

The sampled data measurement system operates with signals that are discrete in value as well as discrete in time. The quantization of the sampled values to the nearest available numeric equivalent introduces errors. Subsequent calculations can introduce additional errors due to rounding or truncation. The software developed for this system operates with high resolution integer arithmetic, and

introduces rounding only during later calculations where it will have little effect.

The initial quantization occurs in the analog to digital converter, which is assumed to have a resolution of X bits plus a sign. The errors introduced can be modeled as additive noise with a value that has a uniform probability density function for values between -1/2 and +1/2 of the least significant bit of the analog to digital converter. The variance of such a uniform PDF is 1/12 of the squared width [25]:

$$\text{Variance of sampling errors} = \frac{1}{12}\left[\, 2^{-X} \,\right]^2 . \qquad (4.10)$$

Calculations involve the accumulation of a large number of signal samples, and therefore the accumulation of many samples of this noise. The central limit theorem indicates that the statistics of the resultant sum will approximate a Gaussian process, and the noise can therefore be modeled as white noise:

$$V_s = \left[\, \frac{M}{12} \,\right]^{\frac{1}{2}} 2^{-X} . \qquad (4.11)$$

As before, the correlation output must be normalized to match sinusoidal inputs. In addition, one must include a scale factor for any gain that occurs before the analog to

digital converter. Such preamplifier gain reduces the size of the analog to digital converter quantization steps, and reduces the quantization noise in proportion. The magnitude of the noise due to quantization is:

$$M_S = \left[\frac{1}{3M\ell} \right]^{\frac{1}{2}} \frac{2^{-X}}{G} \qquad (4.12)$$

where "M" is the number of samples per reference signal cycle, "ℓ" is the number of cycles sampled, "X" is the number of bits in the analog to digital converter, and "G" is the preamplifier gain.

4.1.4 Noise Sources

The noise source calculations found in the previous two sections can now be evaluated for the particular hardware used in the measurement system, and then compared with the actual measurements made in section 4.1.1. The noise rejection of the system is governed by the product Mℓ, the total number of samples that are accumulated for a measurement. The noise to signal rejection ratio increases in proportion to the square root of increases in the number of samples. The hardware and software in the constructed system sets the value of Mℓ to 3600 for measurements at all frequencies, though the number of samples per cycle may range as low as 36 for high frequencies (the number of cycles measured increases in proportion). The analog to

digital converter has a resolution of 12 bits, but one of these is effectively a sign bit, so the value of "X" is 11. The noise in the system becomes most significant at low signal levels. The preamplifier applies a gain of 100 to the nominal ±10 volt analog to digital converter, leading to a value for the scaling factor "G" of 10.

The preamplifier is constructed of two operational amplifiers (a type 301 and a type 741) that subtract a DC offset from the input signal, and then amplify the remaining signal by a factor of 10. Both amplifiers contribute noise to the signal, but the following stages of the system (including the analog to digital converter) introduce insignificant additional noise because of the preamplifier gain. The amplifier specifications [26] indicate that the type 741 amplifier has an input noise of approximately 25 nV per $Hz^{\frac{1}{2}}$, while the type 301 has input noise of about 14 nV per $Hz^{\frac{1}{2}}$. Both amplifiers have a bandwidth of close to 1 Mhz (the 301 is operating at a gain of 10, but is decompensated correspondingly). The amplifiers have single pole response, and therefore an effective noise bandwidth of $\pi/2$ times their signal bandwidth, or 1.57 MHz [27]. The noise voltage of the two amplifiers together is 36 μV RMS. This noise voltage is equal to the square root of the noise power WN_o.

Equation 4.9, when evaluated, is found to make a white noise contribution to the system of 1.2 μV, or about -118 decibels. The quantization noise contribution of equation 4.12 is smaller: -127 decibels. The two contributions together suggests an expected system noise of -118 decibels. This is a factor of four (in voltage) smaller than the -106 decibel experimental value. The disagreement is resolved by the character of the analog ground. The commercial analog to digital converter used in the measurement system does not allow the analog and digital grounds to be separated. Similarly, on the synthesizer board, the monolithic digital to analog converters in the excitation signal source have a common analog and digital ground pin. An attempt was made to isolate the analog and digital ground conductors, but the converters create a ground loop, and there is coupling of digital ground noise onto the analog ground. The digital circuitry of the microcomputer includes a great deal of digital logic operating at 6 MHz clock rates. The noise voltage across the analog ground was estimated from oscilloscope traces to be 100 μV. Again using Equation 4.9, this makes an equivalent noise contribution of 3.3 μV, and this -110 decibel level is comparable to experimental results. Though the noise performance of the system is acceptable, it is the ground loop noise that dominates.

4.1.5 Sensor Noise Performance

The noise performance of two different sensor subsystems has been measured. The first of these is the test sensor chip discussed in Chapter 2, with design details collected in Appendix A. The second sensor subsystem tested is manufactured by Micromet Instruments [28], and consists of a sensor chip and additional support electronics, as described in section 1.3. The noise introduced by the sensors was estimated by comparing measurements of system noise without the sensors (as described in section 4.1.1) with similar measurements including the sensors and any support circuitry. The difference in noise was assigned to be the contribution of the sensor. The excitation input of the sensors was grounded instead of receiving a signal from the waveform synthesizer. This method was preferred to an independent measure of the noise by a wave or spectrum analyser. As implemented, the sensor could be operated in its normal system environment, including any effects due to the characteristics of the sampled data system.

The noise contribution of the sensor described in Appendix A was too small to be discerned. This is consistent with estimates derived from the device geometries and circuit design of the sensor. These estimates indicate "flicker" noise dominance (with a 1/f characteristic spectrum) over the frequency range of interest. For typical

semiconductor fabrication conditions [27], the sensor noise power at 0.01 Hz of -111 decibels remains below the measurement subsystem noise floor of -106 decibels. The perhaps surprisingly low noise performance of this MOS amplifier is principally due to the large bias current in the input differential stage, used to lower the impedance level of the transistor pair. The differential transistors reside on a sensor chip separate from the support chip that contains the rest of the amplifier, and the low impedance is necessary for acceptable bandwidth.

Measurements of noise using the Micromet sensor and support electronics can be seen in Figure 4.4. This is total system noise, including both the sensor and measurement subsystems. Results of experiments using the same support electronics, but with the sensor chip replaced by a resistor network, are shown in Figure 4.5. A summary of the results from the two Figures is listed in Table 4.2. There is no significant noise contribution from the sensor chip itself.

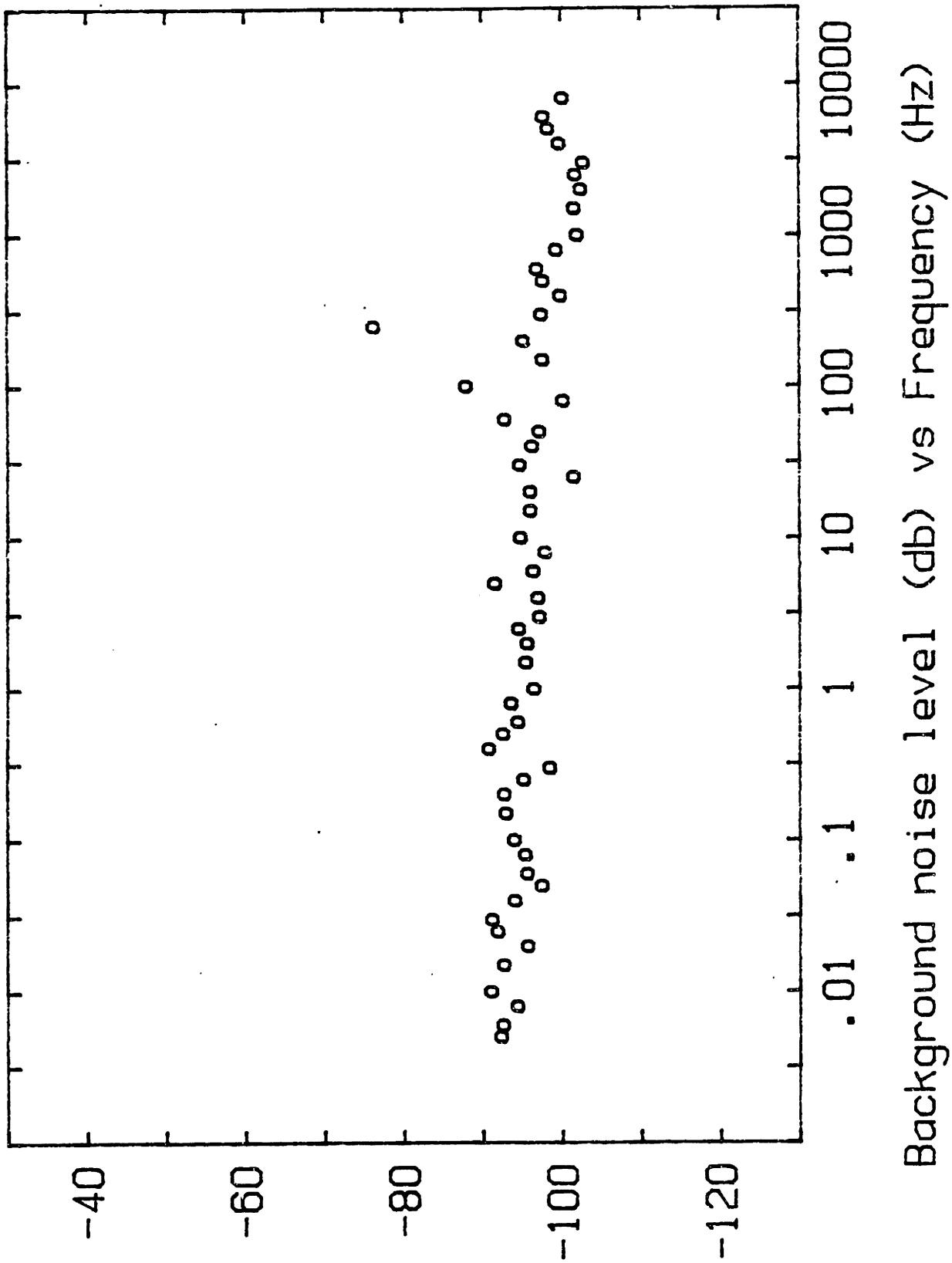


Figure 4.4 Background Noise Magnitude including Sensor

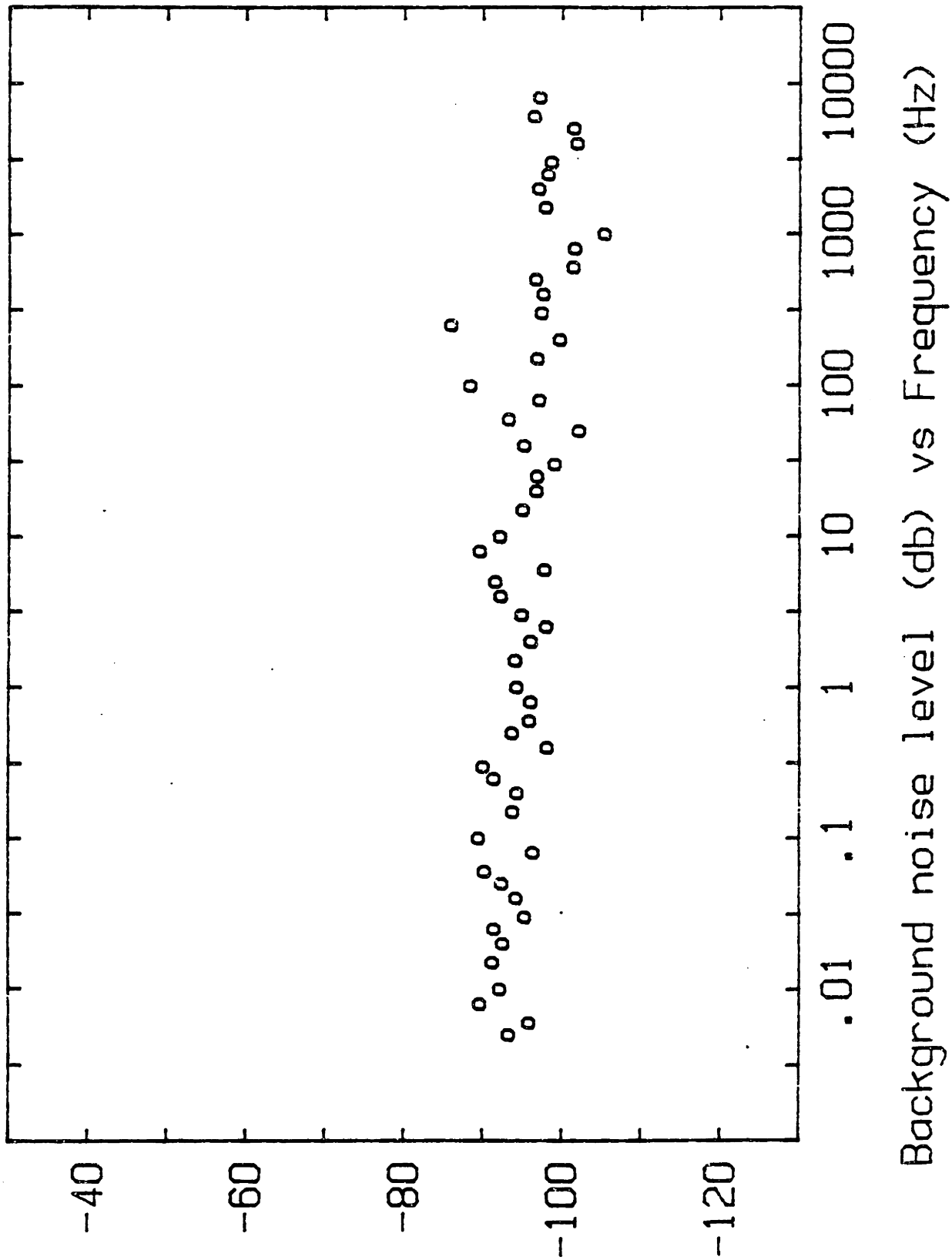


Figure 4.5 Background Noise Magnitude from Sensor Interface

TABLE 4.2

Experimental Measurements of System Noise Magnitude Including Micromet [28] Sensor Subsystem

Configuration	Measured Noise (db)	Sensor Subsystem Noise (db)
Grounded sensor	-95.3	-96.3
Resistor network	-95.0	-95.9

The transresistance and feedback amplifiers in the support circuit were designed to introduce minimum phase at the higher measurement frequencies. The design therefore includes high speed AD509 operational amplifiers [29] that dominate the noise performance. These amplifiers have a noise spectral density that breaks between flicker noise and white noise at approximately 300 Hz. The aliasing introduced by the sampled data system is such that the total noise will be dominated by the white noise of 19 nV per $Hz^{\frac{1}{2}}$, for this frequency spectrum. The amplifier equivalent input noise is subject to a gain of 7 for two of the amplifiers, and a gain of 6 for the third one, leading to an equivalent total noise of 220 nV per $Hz^{\frac{1}{2}}$ at the response input of the sampled data system. An analysis equivalent to the one in section 4.1.4 leads to an expected noise contribution of the commercial sensor subsystem of -101 decibels. This is about 5 decibels (a factor of 3 in power) below the experimental estimate.

It should be noted that the ultimate noise performance of the complete instrument using the Micromet sensor is limited by the noise introduced in the interface electronics. However, other sources of noise are not wildly smaller, and a reduction of the interface circuitry noise would soon lead to a limit from the input amplifiers in the measurement subsystem, and thereafter, noise due to the analog to digital quantization.

4.2 Distortion

Distortion of waveforms can occur in every subsection of the instrument, just as in the case of noise, and the distortion will introduce systematic errors in measurements. However, distortion or nonlinearity occurring in the material applied to the sensor also opens the possibility for acquiring additional information about the properties of the material under test. The correlation function implemented in the sampled data measurement system has the capability of detecting small amounts of distortion by measuring harmonic and intermodulation frequency components. These capabilities are studied in the following sections. First, the sampled data measurement subsystem is tested for harmonic distortion, and a controlled distortion is introduced to demonstrate the capability for harmonic and intermodulation distortion measurement. Next the distortion introduced by the sensor and sensor support circuitry is studied. Third, a simple example of a nonlinear material applied to the sensor is demonstrated.

4.2.1 Harmonic and Intermodulation Measurement

The harmonic distortion of the synthesizer and sampled data analysis subsystem is measured by directly coupling the excitation waveform of the synthesizer to the response waveform input. Correlation analyses are performed at a

large set of frequencies and the signal levels at these harmonics are evaluated. Figures 4.6, 4.7 and 4.8 show the measured harmonic energy for a fundamental excitation signal of 2 volts peak to peak, at 10 Hz, 100 Hz and 1000 Hz, respectively.

Intermodulation distortion is measured by programming the synthesizer to deliver a waveform consisting of both a fundamental and the third harmonic (equal magnitude) to the response input. The distortion leads to combination tones at the second and fourth harmonics of the fundamental. The peak output of the synthesizer is limited to one volt, so the fundamental and third harmonic excitation waveforms are each reduced by a factor of two in voltage. Selected results of the harmonic and intermodulation tests are summarized in Table 4.3. The lower levels for the intermodulation distortion results are artifacts of the scaled excitation signals generated by the synthesizer.

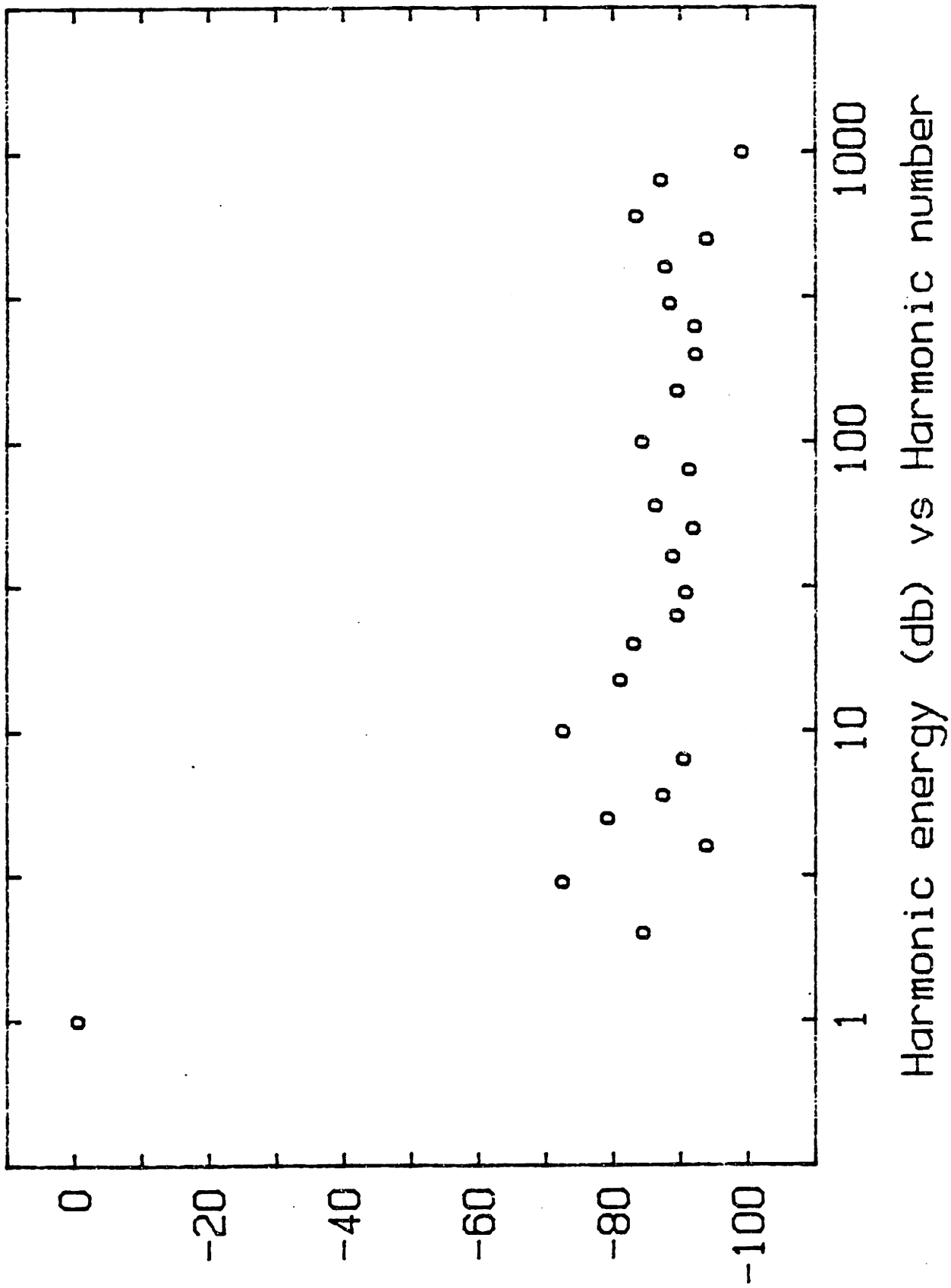


Figure 4.6 Harmonic Response of Measurement System at 10 Hz Excitation

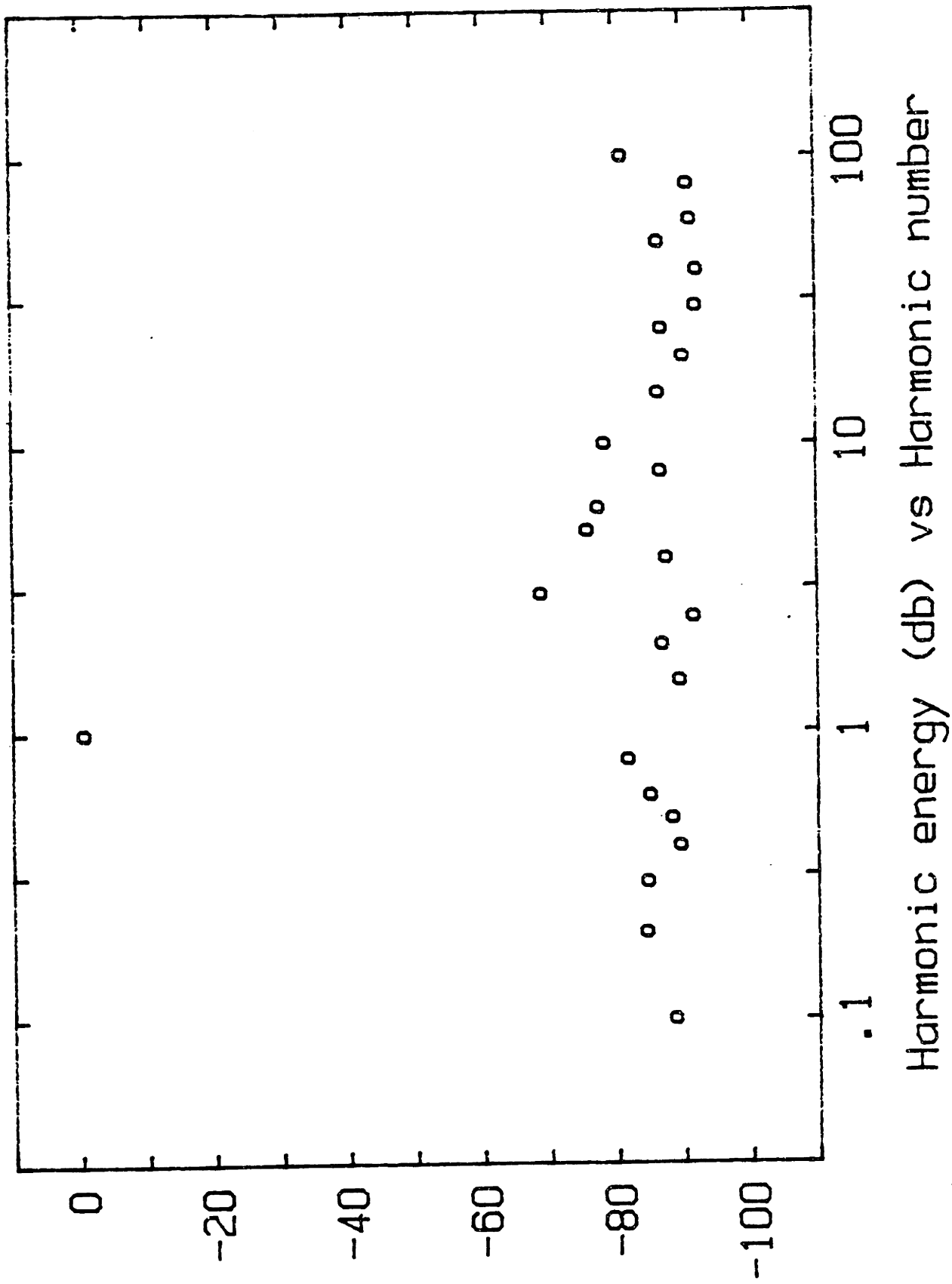


Figure 4.7 Harmonic Response of Measurement System at 100 Hz Excitation

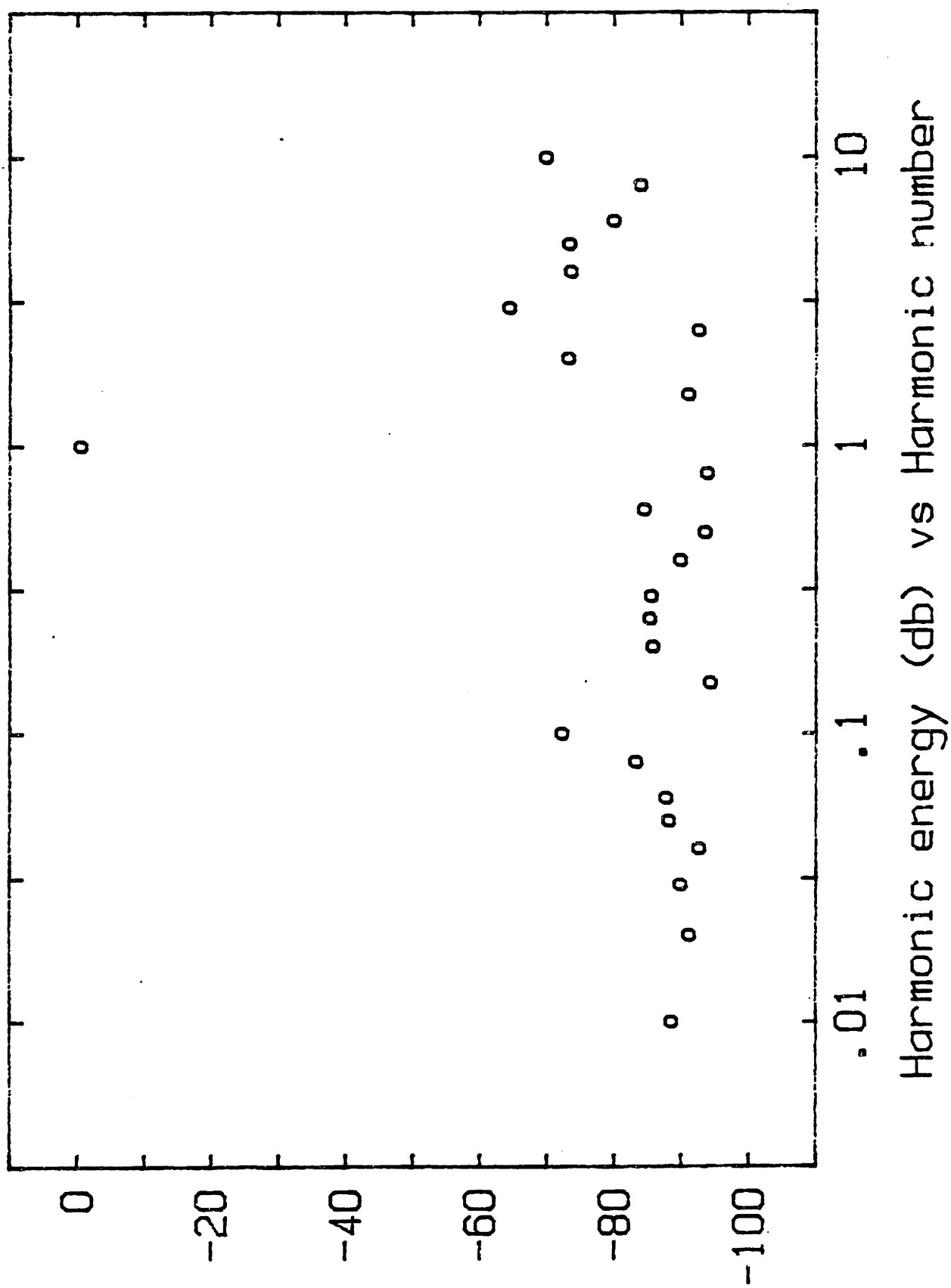


Figure 4.8 Harmonic Response of Measurement System at 1000 Hz Excitation

TABLE 4.3

Harmonic and Intermodulation Distortion
in Measurement Subsystem

Excitation	Measurement Frequency	Harmonic	Signal Level (db)
10 Hz	20 Hz	2	-83.9
	30 Hz	3	-71.9
100 Hz	200 Hz	2	-86.3
	300 Hz	3	-68.2
1000 Hz	2000 Hz	2	-72.6
	3000 Hz	3	-63.9
10 Hz, 30 Hz	20 Hz	3-1	-95.7
	40 Hz	3+1	-95.5

Unlike the earlier noise measurements, the distortion sensitivity of the measurement subsystem is ultimately limited by the resolution of the analog to digital converter used as the sampler. The preamplifier gain is determined by the peak level of the overall signal (usually dominated by the fundamental), and quantization noise (section 4.1.3) determines the minimum detectable signal at other harmonics. If the system under test introduces only small amounts of harmonic energy, the detection threshold is described by equation 4.12 without additional preamplifier gain (worst case, "G" = 0.1). For the constructed system with a

fundamental transfer function magnitude close to 1, the threshold for detection of harmonics is 5×10^{-5}, or -87 decibels.

To demonstrate the distortion measurement capability of the system, a controlled square law transfer function is introduced between the excitation signal source and the response input. The square law device consists of a MOS field effect transistor biased in the saturation region so that the drain current exhibits an approximate square law characteristic with respect to the gate voltage. Additional circuitry cancels the DC offset and the first harmonic components. For the harmonic measurement, the applied signal is:

$$\text{Harmonic measurement excitation} = \sin(\omega t) \qquad (4.13)$$

leading to an ideal response of:

$$\text{Ideal square response} = \frac{1}{2} - \frac{1}{2}\cos(2\omega t) \quad . \qquad (4.14)$$

For the intermodulation test, the excitation signal is:

$$\text{Intermodulation excitation} = \frac{1}{2}\sin(\omega t) + \frac{1}{2}\sin(3\omega t) \qquad (4.15)$$

and the ideal squared response should be:

$$\text{Ideal response} = \frac{1}{2} + \frac{1}{4}\cos(2\omega t) - \frac{1}{2}\cos(4\omega t) - \frac{1}{4}\cos(6\omega t). \qquad (4.16)$$

Experimental results of measurements of the harmonic and intermodulation response of this transducer are tabulated in Table 4.4, along with the theoretical response of a perfect square law converter.

TABLE 4.4

Measurements of Square Law Converter

Measured Harmonic	Ideal Response		Measured Response	
(apply 100 Hz)	Magnitude (db)	Phase (deg)	Magnitude (db)	Phase (deg)
1	-∞	---	-30.2	110.3
2	-6.02	-90.0	-6.8	-89.1
3	-∞	---	-40.3	-2.4
4	-∞	---	-49.4	-89.3
5	-∞	---	-87.8	174.3
6	-∞	---	-71.0	-95.2
7	-∞	---	-75.8	-20.7
(apply 100 Hz, 300 Hz)				
1	-∞	---	-30.3	69.5
2	-12.04	+90.0	-12.6	89.3
3	-∞	---	-29.9	41.6
4	-6.02	-90.0	-6.6	-89.2
5	-∞	---	-74.2	-54.6
6	-12.04	-90.0	-12.6	-89.3
7	-∞	---	-43.0	-3.5

The correspondence between measured and expected results is good, particularly in the phase relationships. Experimental deviations from the ideal are attributed to incomplete cancellation of the fundamental signal in the square law converter.

The harmonic distortion levels in the sampled data measurement subsystem can be converted to sensitivity thresholds for detection of distortion in the system under test. Examples of thresholds for second and third order distortion at three frequencies are tabulated in Table 4.5, assuming that the network under test can be modeled by the function:

$$V_{out} = \text{DC offset} + V_{in} + \alpha V_{in}^{2} + \beta V_{in}^{3} + \text{higher order terms.} \quad (4.17)$$

TABLE 4.5

Distortion Detection Thresholds of Sampled Data System

Frequency	Parabolic (α) coefficient	Cubic (β) coefficient
10 Hz	6.3×10^{-5} (-84 db)	2.5×10^{-4} (-72 db)
100 Hz	7.1×10^{-5} (-83 db)	3.5×10^{-4} (-69 db)
1000 Hz	2.2×10^{-4} (-73 db)	6.3×10^{-4} (-64 db)

4.2.2 Distortion in Sensor Subsystem

Distortion in the sensor chip and interface electronics increases the distortion detection thresholds derived in the previous section. Measured harmonic response for the Micromet sensor at 10 Hz, 100 Hz and 1000 Hz with an excitation signal of 2 volts peak to peak is shown in Figures 4.9, 4.10 and 4.11, respectively. Additional experiments where the differential transistor pair in the sensor chip was replaced by a resistor network demonstrated that the interface circuitry contributes negligible additional distortion. The harmonic distortion in the sensor chip from second and third order nonlinearity is summarized in Table 4.6.

TABLE 4.6

Harmonic Distortion in Sensor Chip

Excitation	Measurement Frequency	Harmonic	Signal Level (db)
10 Hz	20 Hz	2	-51.6
	30 Hz	3	-68.8
100 Hz	200 Hz	2	-51.2
	300 Hz	3	-67.4
1000 Hz	2000 Hz	2	-51.6
	3000 Hz	3	-74.6

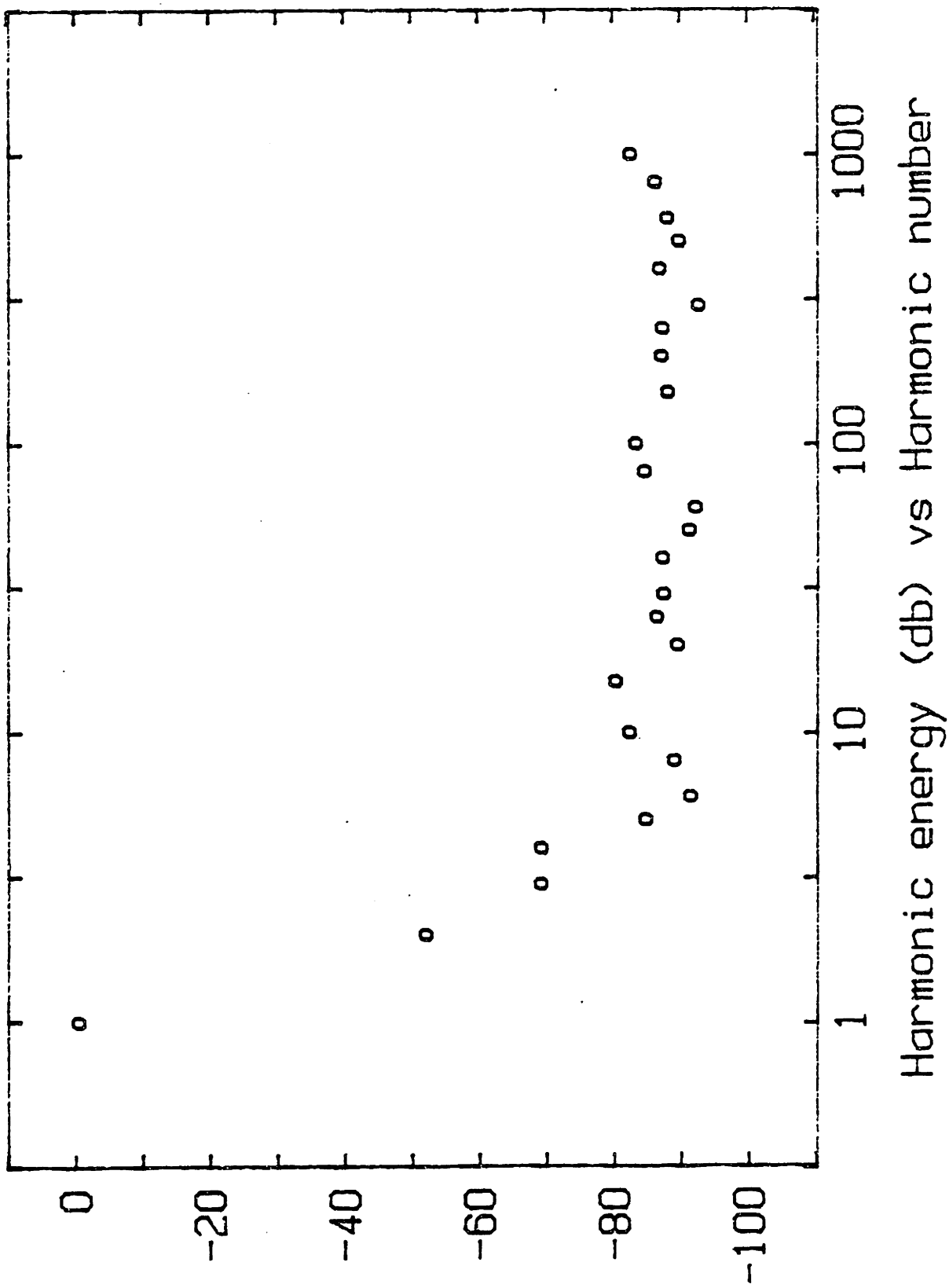


Figure 4.9 Harmonic Response of Sensor and Measurement System at 10 Hz

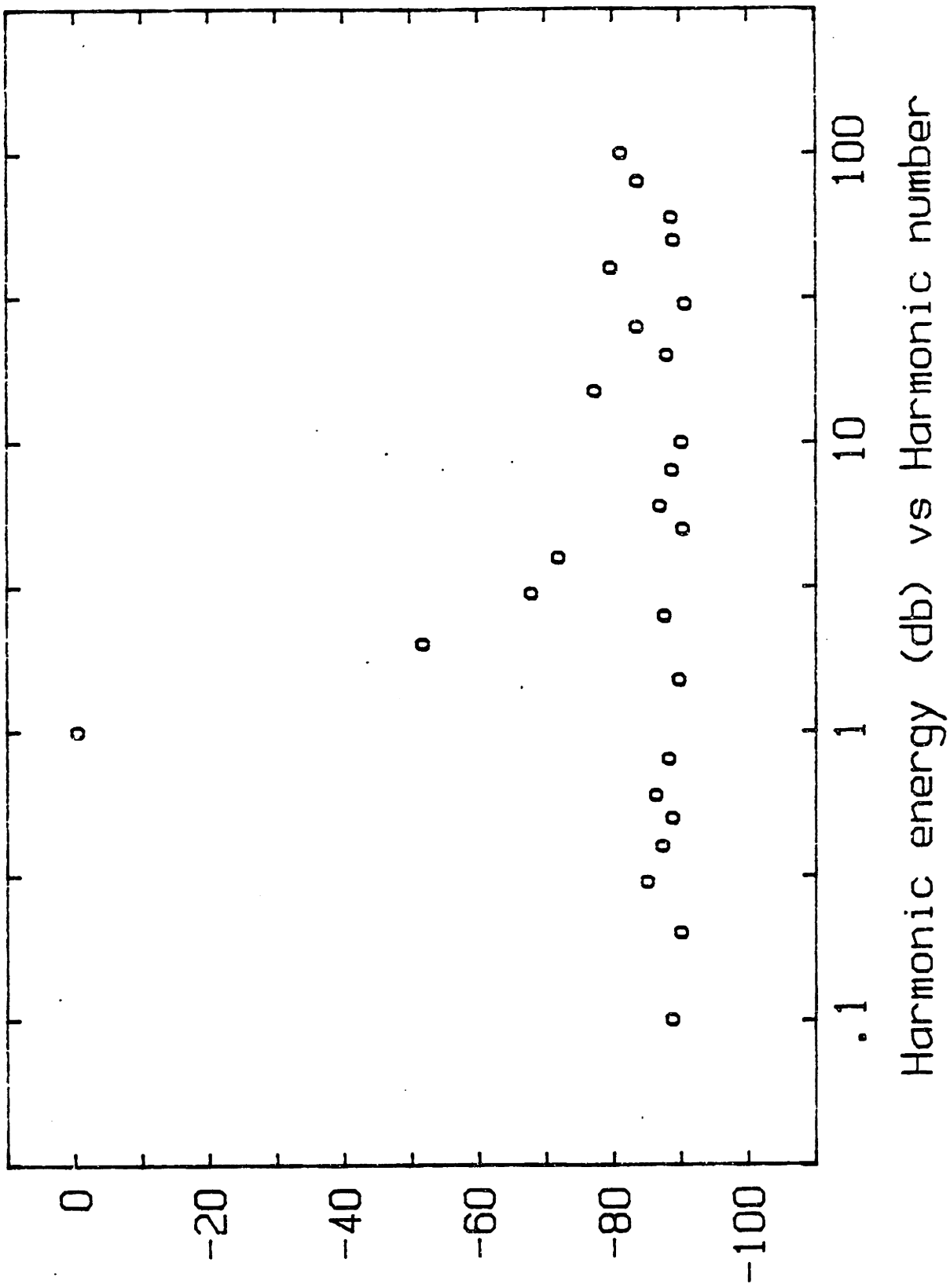


Figure 4.10 Harmonic Response of Sensor and Measurement System at 100 Hz

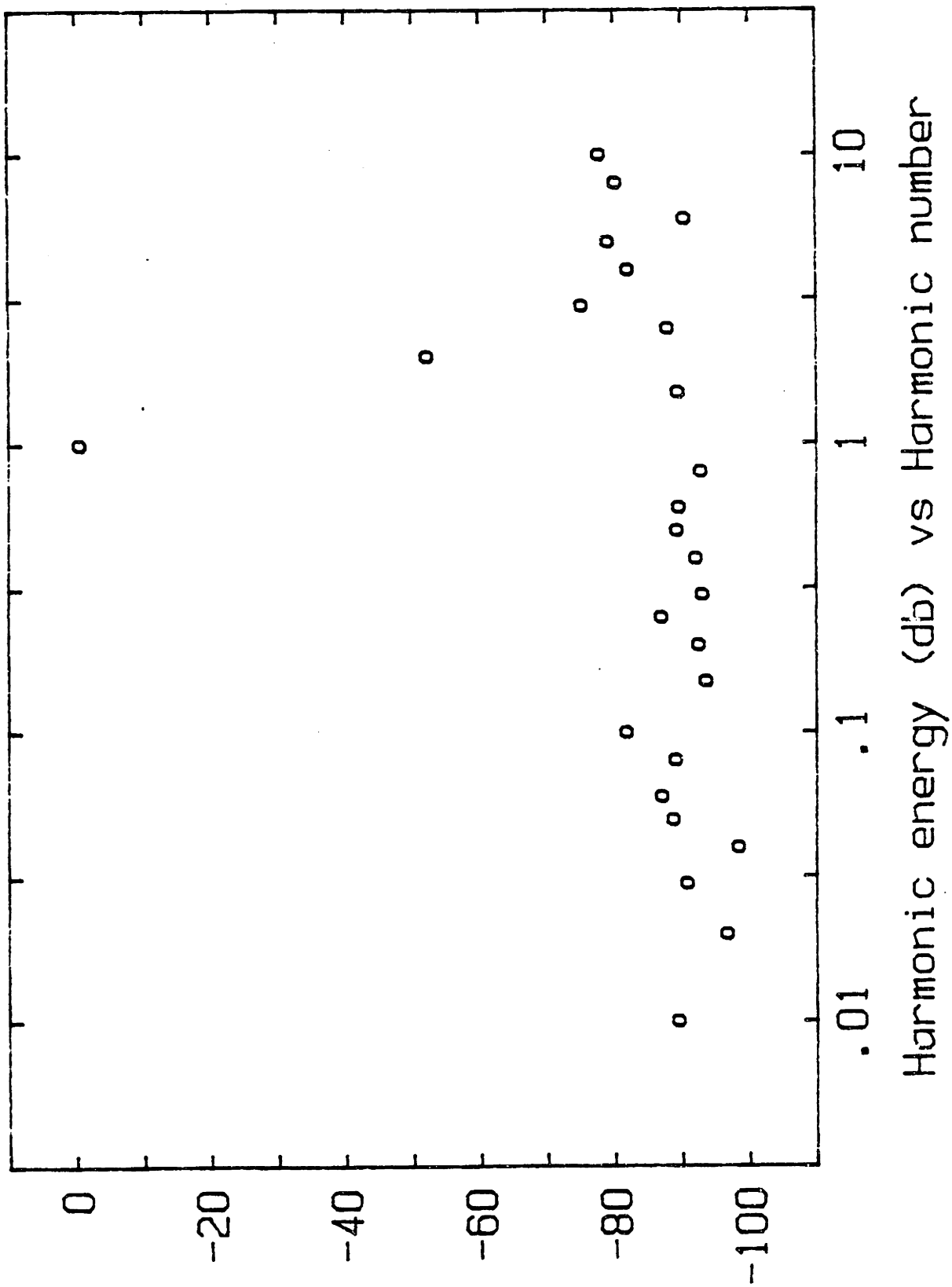


Figure 4.11 Harmonic Response of Sensor and Measurement System at 1000 Hz

Small but definite parabolic distortion in the sensor chip can be seen in these results, with a coefficient of 2.7×10^{-3} (one fourth of one percent).

4.2.3 Non-linearities in the Sample Under Test

The general design of the dielectric measurement system assumes that the material being tested is linear, so that the combination of the material and the sensor can be described by a frequency dependent magnitude and phase response. Excessive excitation signal levels lead to nonlinearities in the substance being tested, and the distortion can be measured to uncover additional information about the sample. Alternatively, if linear behavior is required (perhaps for a multiple excitation frequency measurement), the distortion may be detected and force a reduction in the excitation signal level to avoid errors.

A simple experiment was performed to demonstrate the capability of the dielectric measurement system to detect nonlinearities in the properties of trichloroethylene (TCE), of reagent grade. The sensor was immersed in the solvent and measurements of the dielectric properties were taken for a wide range of excitation frequencies. The sensor response was analysed for the fundamental, and second and third harmonics. Table 4.7 shows results from these measurements.

TABLE 4.7

Nonlinear Response of Trichloroethylene

Excitation frequency (Hz)	Harmonic response			
	Fundamental (db)	Fundamental (deg)	2nd (db)	3rd (db)
0.1	+1.1	-1.9	-30.0	-52.9
1	+0.6	-15.2	-30.9	-49.7
10	-8.1	-70.9	-49.5	-55.1
100	-27.5	-39.3	-63.0	-77.0
1000	-28.2	-4.5	-81.7	-90.2
10000	-28.9	-0.5	---	---

At higher frequencies the permittivity component of the admittance dominates the response, indicated by the small phase angle of the fundamental response. The magnitude of the response is almost independent of frequency, and the harmonics are small. At lower frequencies, the conductivity of the sample plays an increasing role in the response. The response at the second and third harmonic increases as well, indicating the presence of nonlinearities.

The total charge coupled through the material during each cycle of the excitation scales reciprocally with the frequency of excitation. It is proposed that, at the lower frequencies, the available ionic carriers in the solvent are

collecting at the (blocking) [17] electrodes of the sensor during each cycle and leaving the region between the electrodes depleted. This saturation effect would introduce a nonlinearity in the response, as is observed.

A typical epoxy resin, diglycidyl ether of bisphenol-A (DGEBA) was also tested to determine if non-linearities were observable at normal excitation signal levels. No additional distortion above the threshold introduced by the nonlinearity in the sensor chip could be distinguished. This sets an upper limit of approximately one quarter of one percent second order distortion, and less than one tenth of one percent third order distortion. This linear behavior at an excitation level of 2 volts peak to peak is consistent with previously reported results [10].

4.3 Measurement Speed

The measurement speed of the dielectric measurement system is dependent on several factors. Some of these constraints can be determined by the experimenter, while others are characteristic of the sampled data correlation function, and have been chosen to meet other performance requirements in the system. The first section analyses the interaction of the constraints and evaluates the resulting performance under a variety of experimental conditions. The following section proposes techniques that could be used to increase the measurement speed of the system.

4.3.1 The Measurement Process

The most general (and slowest) measurement of dielectric characteristics at a particular frequency consists of four functionally separate phases. First, an excitation waveform must be generated and downloaded to the synthesizer. Next, an array of samples of the response signal, properly synchronized with the excitation waveform, is collected. Third, the correlation analysis is performed on the sampled signal, to evaluate the magnitude and phase at a particular frequency. Finally, the magnitude and phase can be converted to a corresponding permittivity and loss factor from knowledge of the geometry of the sensor and sample.

Each of the above operations takes time, however some experiments can avoid the repetition of all phases for each measurement, thereby increasing the effective measurement rate. In particular, if a multiple frequency measurement can be performed, the response signal need be sampled only once and then separate correlation analyses may be performed for each component. The conversion of magnitude and phase results into dielectric properties is performed using a table lookup operation and requires negligible time. Even greater efficiency is possible if successive measurement cycles involve the same set of frequencies in the excitation waveform. In this case, the synthesizer does not need to be programmed again, avoiding the time required to generate and download the waveform array. This last alternative has the additional advantage that there are now no transients in the excitation signal, eliminating a possible source of error in the measurement.

The synthesizer software is designed to generate an array of numeric data that corresponds to the desired excitation signal. A template array of one quadrant of a unit sinusiod (901 points) is precalculated and contained as constant data in the software. Appropriately amplitude negated and time reflected copies of the template are used to build the waveform array. For generating harmonics, the subroutine "skips over" entries so that the "n-th" harmonic

contains in successive output points every "n-th" point in the template. In the case of multiple frequency component waveforms, the individual amplitudes are scaled by a power of two to insure that the peak voltage remains within the dynamic range of the system. The excitation array accumulates a waveform containing up to 16 frequency components. The 3600 point array is then programmed into the synthesizer. Each frequency component requires approximately 500 milliseconds to be generated, and the download operation adds insignificant time.

The sampling of the response signal can be separated into a sequence of steps. On entry, the response signal magnitude and possible DC offset is not known. First, an unsynchronized sampling of 3600 points (same size as the excitation array) is collected on the least sensitive range of the analog to digital converter. A simple (and quick) analysis is performed to find the peak to peak signal magnitude and the average DC value. The preamplifier gain is set for optimum analog to digital converter resolution, without overload. A digital to analog converter is loaded with the DC offset, and this voltage subtracts from the input voltage for the subsequent measurement. The "tare" subtraction occurs before the preamplifier, avoiding dynamic range limitations. The final step in the data acquisition is a second sampling of the input signal, but now with the DC offset and preamplifier gain applied. Again 3600 points

are sampled, but the beginning of the sampling is synchronized with the initial point of the next cycle generated in the synthesizer. This provides the absolute time reference required for phase measurement.

For low frequency measurements, the 3600 sampled points constitute one cycle of the "fundamental" excitation frequency. The analysis of the unsynchronized measurement is fast, but the following synchronization can take (in the worst case) one full cycle. Therefore the total response acquisition time at low frequencies is 3 cycles of the lowest excitation frequency. For higher frequencies, the sampling rate is limited by the maximum conversion rate of the analog to digital converter of 36000 samples per second. For frequencies above 10 Hz, the array of data is acquired in 100 milliseconds (so for a 10 kHz signal, there are 3.6 samples per signal cycle). The total acquisition time is thus the greater of 300 milliseconds, or 3 cycles of the fundamental synthesizer frequency.

The correlation analysis involves 7200 multiplication and accumulation operations, one half for generating the in-phase (or real) part of the response, and the rest for the quadrature (imaginary) part. All calculations are performed using integer arithmetic without truncation or rounding, thereby avoiding any additional error contribution. Further calculations to produce the magnitude and phase are

evaluated using floating point arithmetic, but add little error or calculation time. The integer multiply and accumulate routines are carefully coded in assembly language to proceed as rapidly as possible; nevertheless, analysis of the magnitude and phase of a frequency component requires close to 2.5 seconds.

Table 4.8 summarizes the measurement time of the instrument for a variety of experimental configurations, comparing a sequence of single frequency measurements with multiple frequency measurements both including and excluding the synthesizer setup times. The ratio of the measurement speed of the multiple frequency techniques to sequential measurements is also noted. The speed enhancement for the multiple frequency measurement over corresponding sequential measurements at single frequencies is only a factor between 1.1 and 2.7 for the various frequency sets. The reason for this relatively small improvement is that the total measurement time is typically dominated by the period of the lowest frequency. At higher frequencies, the synthesizer setup time and the magnitude and phase analysis time play a dominant role.

TABLE 4.8

Measurement Time

number	Frequency range (Hz)	Single (sec)	Multiple (sec)	Multiple (ratio)	Multiple (no setup) (sec)	Multiple (no setup) (ratio)
1	0.01	303	---	---	---	---
1	0.1	33	---	---	---	---
1	1	6	---	---	---	---
1	$\geq$ 10	3.3	---	---	---	---
6	0.1 - 10000	52.2	48.3	1.1	---	---
7	0.01 - 10000	355.2	321.6	1.1	---	---
15	0.01 - 1	898.3	345	2.6	357.5	2.7
15	0.1 - 10	130.3	75	1.7	67.5	1.9
15	1 - 100	55.1	48	1.1	40.5	1.4
15	10 - 1000	49.5	45.3	1.1	37.8	1.3
15	100 - 10000	49.5	45.3	1.1	37.8	1.3

4.3.2 Opportunities For Higher Performance

In specialized applications, such as rapidly reacting chemical systems, a faster measurement rate than indicated in Table 4.8 becomes desirable. Greater speed is applicable only to the higher frequencies, since measurements of frequency dependent properties that change significantly during a single cycle of the probe signal are not meaningful. Measurement speed at these frequencies is limited by software in the synthesizer waveform calculations and in the sampled data correlation algorithm used to extract the magnitude and phase.

The synthesizer setup time can be essentially eliminated for specialized applications by precomputing all excitation frequency sets, and merely selecting the desired waveform from "read-only" memory during the experiment. The correlation algorithm used to evaluate the magnitude and phase is implemented on a Zilog Z-80 microprocessor. Some improvement can be gained by the use of a higher performance processor, without changing the architecture of the system. For dramatic enhancement of the analysis speed, a hardware implementation can be used for either the current correlation operation, or the Fast Fourier Transform Algorithm [20]. The hardware can execute in a pipelined fashion with the sampling operation so that the next array is being acquired concurrently with analysis of the previous

array. In this case, the analysis time equals the sampling time, but the throughput rate is that of a system with zero analysis time. Alternatively, the correlation function may be performed on a "moving window" of the sampled response signal, where each sample point results in a new magnitude and phase result (once the window is full). Adjustments of the "depth" of the window scale the averaging operation applied to the data, so that a shorter window trades increased noise for reduced settling time.

The above alternatives can dramatically increase the performance of the dielectric measurement system, at the expense of increased complexity and possibly reduced versatility.

CHAPTER 5

Conclusions

A high performance dielectric measurement system has been developed. The new system is based on a previous microsensor system but offers an increased range of permitted measurement frequencies and higher resolution in the measurement of the dielectric properties of the sample.

5.1 Summary of Results

Three different sensor circuit configurations have been studied that each offer a different mix of advantageous and disadvantageous characteristics. All three structures provide similar resolution at low loss factors. When compared with the impedance divider design, the integrator circuit has higher sensitivity to dielectric properties in highly conductive dielectrics (an order of magnitude at a permittivity of 10 and a loss factor of 3). The integrator design does suffer from offset voltages that lead to saturation of the amplifiers, and the necessary nulling loop requires unacceptably long time constants to maintain accurate measurements at low frequencies.

A monolithic bridge circuit has been developed that has the same dielectric sensitivity as the integrator, and requires only a simple null detector rather than the accurate magnitude and phase meter required for either of the other two approaches. Unfortunately, for the desired measurement frequency range (as low as 0.005 Hz) the multiple samplings of the response required to drive the bridge to a null is a major disadvantage.

The divider circuit supports measurements at multiple frequencies simultaneously. This can significantly increase the data acquisition speed, and is difficult to implement

for the bridge design. It is concluded that the divider design, as used in the original instrument, offers the best overall collection of features. The sensitivity problem of the divider can be avoided by designing the sensor for greatest sensitivity in the range of dielectric properties of greatest interest. If a wide range is necessary, a selection of electrode structures can be included on the chip, each optimized for a particular range.

The performance of the microdielectrometer has been enhanced by the development of a sampled data digital signal processing system. The new excitation-response analysis instrument includes an excitation signal synthesizer and synchronized data acquisition of the sensor response. Strobe and synchronization signals are generated by the synthesizer in parallel with the digitized waveform data. The use of these signals to trigger the sampling analog to digital converter insures the absolute synchronization required to measure the phase response of the sensor.

The synthesized waveform can be constructed from as many as 16 simultaneous frequency components spanning two decades of frequency. Frequencies over the range of 0.005 Hz to 10 kHz are available. The sensor response at a particular frequency is obtained from the sampled data using a digital correlation algorithm executed on a microcomputer. As an example of the multiple frequency capability, Figure

5.1 shows a "time-lapse" plot of the sensor output waveforms during a polymer curing reaction. The excitation signal used in this experiment contained seven frequency components ranging over one decade of frequency. All frequency components were sampled simultaneously by the signal processing system and analysed to determine the sample response at each frequency.

It is also possible to analyze the response signal and measure frequency components not included in the excitation, thereby confirming the linearity of the sensor and data acquisition system and detecting nonlinearities in the sample. The signal analysis module can detect second and third order harmonic distortion of less than 0.1 percent. The sensor chip has been found to introduce approximately 0.2 percent parabolic distortion and insignificant cubic distortion.

The true correlation algorithm incorporated in the signal processing software provides excellent noise rejection, with magnitude and phase sensitivity of 0.01 decibel and 0.1 degree, respectively, over a dynamic range of 55 decibels. This performance translates into a loss factor sensitivity limit of 0.005 in a dielectric material with a permittivity of 3.

The loss factor sensitivity represents a factor of 10 greater resolution for low loss factors over the dielectric

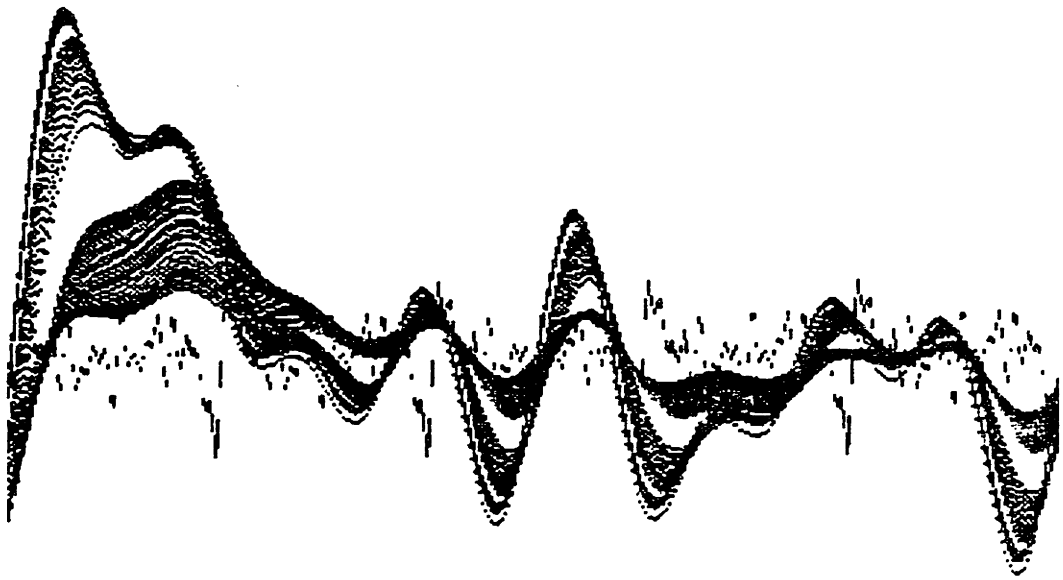


Figure 5.1 Example of Sensor Response Waveforms during Polymer Curing Experiment using Multiple Frequency Component Excitation

measurement system in use when this effort was begun. The low frequency measurement limit has been extended by more than two orders of magnitude. The single frequency measurement speed is increased by typically a factor of 5 and the capability for simultaneous measurements at multiple frequencies offers further speed enhancements.

APPENDIX A

Sensor Test Chip

A test sensor chip has been developed to demonstrate the design of the "closed-loop integrator" and "monolithic bridge" sensor configurations. The implementation has been designed in an enhancement/depletion n-channel MOS technology. Control voltages applied to MOS switches included in the design select the signal paths used.

As described in section 2.4, the circuitry is partitioned between two distinct subsystems that reside on different integrated circuit chips. The sensor chip is kept as simple as possible, thereby easing the design of a circuit that must operate over as wide a temperature range as possible. The support chip is expected to be operating in a benign environment and contains the greater part of the integrator (or bridge null detector) amplifier and the switched capacitor filter used for offset voltage cancellation.

To maintain the necessary extremely high impedance at the sensor output electrode, all components directly connected to this node must be on the sensor chip, including the feedback capacitor for the integrator configuration and the reference capacitor for the monolithic bridge. The two

MOS transistors that form part of the input differential stage of the amplifier must be matched, so both of these components also reside on the sensor chip. The layout of the 760 μm by 520 μm (active area) sensor chip is shown in Figure A.1. The electrode array is located in the lower right corner of the diagram. The differential transistors can be found immediately above the electrodes, interleaved to insure good matching. The remainder of the chip area is consumed by three sets of capacitors and selection transistors (operating as analog switches) for these components. One set is used as the feedback element in the integrator mode, and another set operates as the reference device when the chip is configured as a monolithic bridge. The third set of capacitors provide a secondary excitation signal input for testing, distinct from the electrode array. A second level of polysilicon was not available in the fabrication process used, so the capacitors were implemented as large depletion mode transistors. The polysilicon "gates" of these "capacitors" are connected to the high impedance node (rather than the "sources" and "drains") to avoid leakage currents between the substrate and the output electrode.

Two amplifiers of similar design are included on the support chip. The first of these is in the signal path as the integrator or null detector (depending on the application). The second amplifier is used for the switched

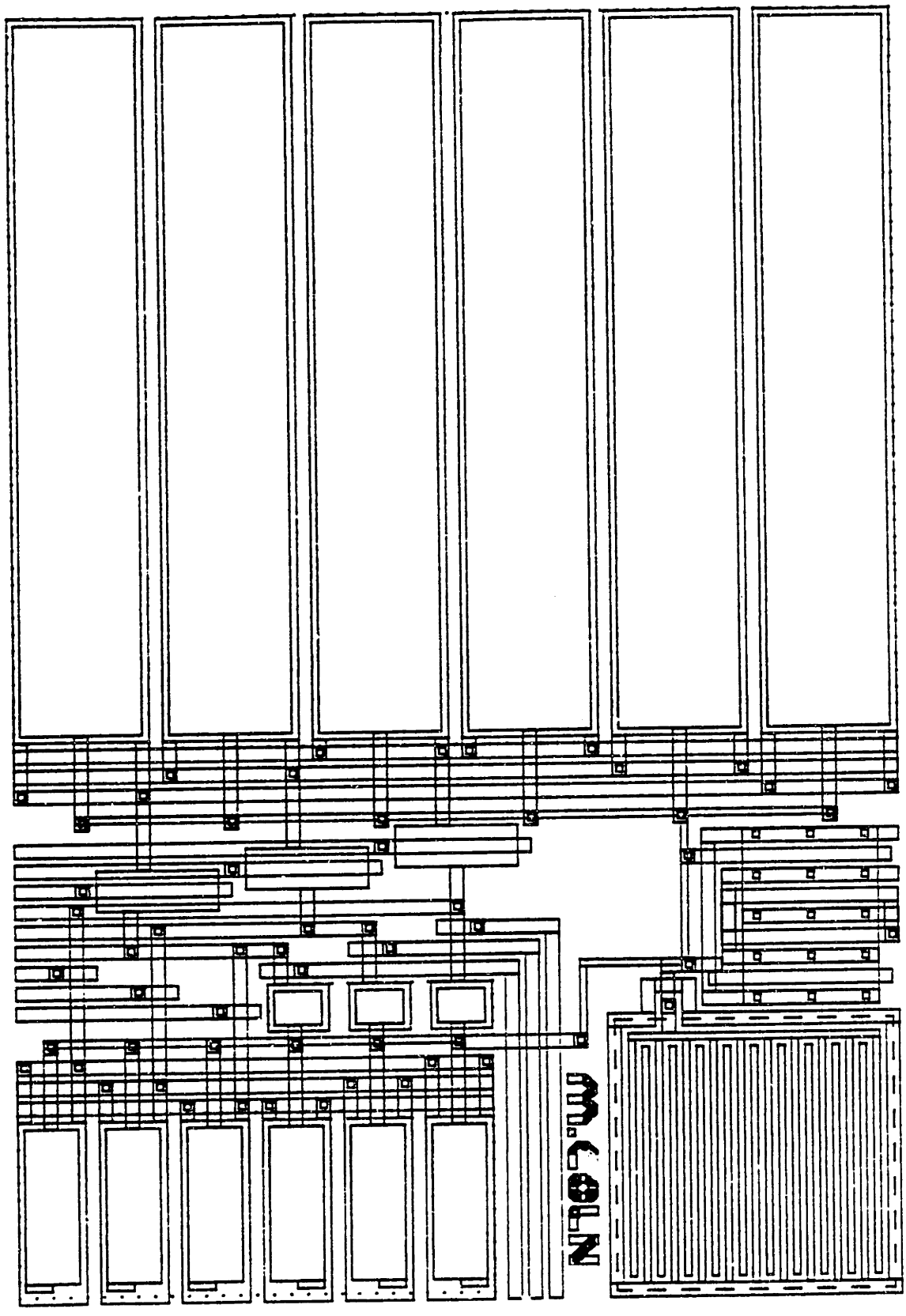


Figure A.1 Test Sensor Chip Layout (100 μm per inch scale)

capacitor filter. A schematic diagram for the amplifiers is shown in Figure A.2. Transistors M1 and M2 are the input differential pair (actually located on the sensor chip in the case of the signal amplifier). The input transistors are cascoded by M3 and M4 to reduce the effect of the capacitance that is parasitic on the drains of the input transistors. M5 and M6 are depletion devices and form the current source loads, providing a gain of approximately ten for the first stage.

M7 and M9 level shift the negative differential output from the first stage. M7A is included to reduce the otherwise excessive length required in M7. The level shifted signal is used to bias the input stage through the current source transistor M11. The loop seeks to pin the voltage at the drain of M3, thereby forcing the differential to single ended signal conversion to occur at the drain of M4. M27 is a feed-forward capacitor that increases the bandwidth of the "bias" loop since the bias loop must operate over the entire signal bandwidth.

The output from the first stage is level shifted by M8, M8A and M10, and applied to M15, the driver transistor of the second stage. The current source load for this stage is the depletion device M18. M17 operates as a cascode, isolating the load from the additional current source M16. The additional current flowing in M15 increases the

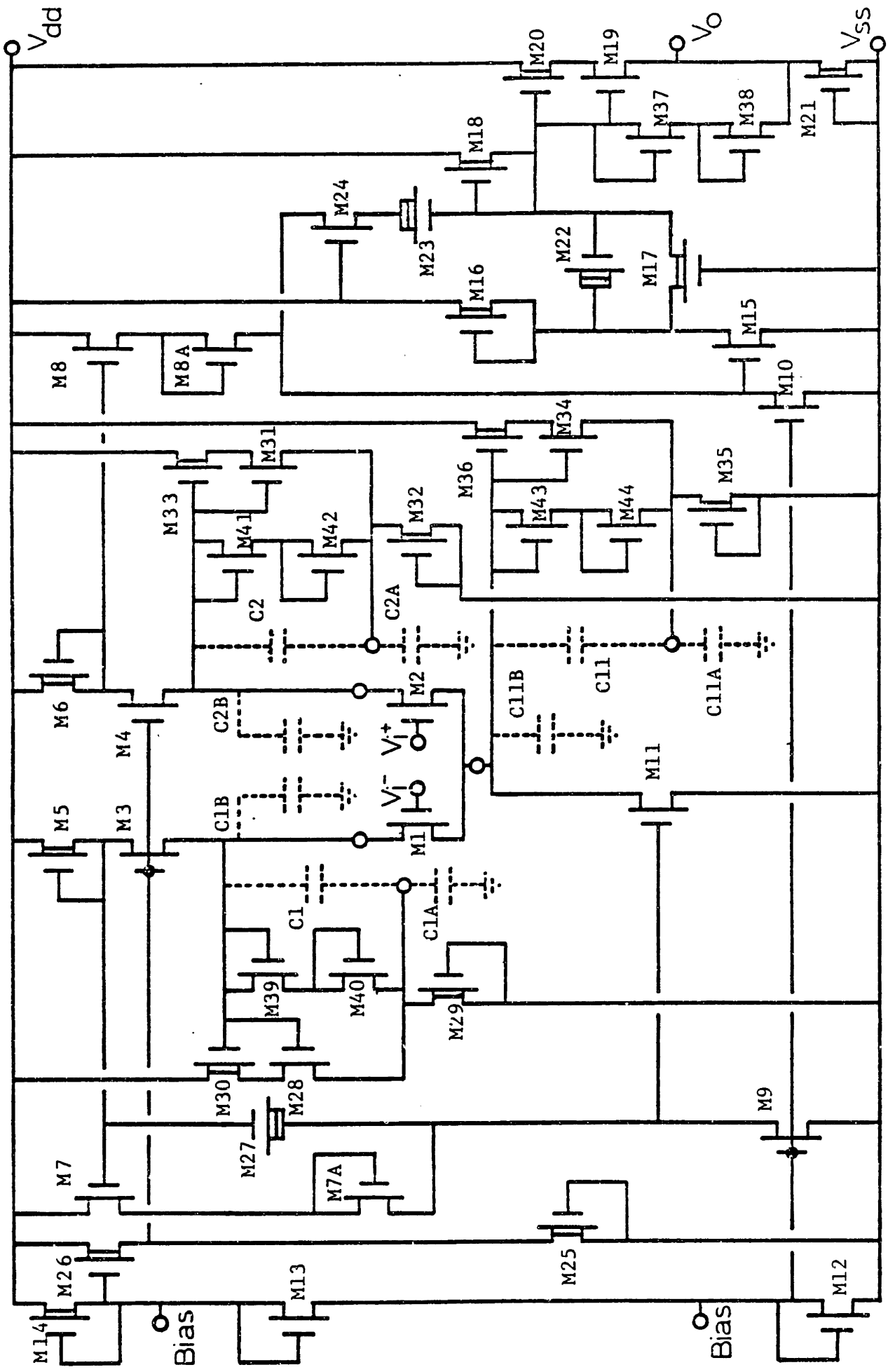


Figure A.2 Schematic Diagram of Operational Amplifier used on Support Chip

transconductance of the driver transistor, and therefore the gain of the second stage. M22 is a feed-forward capacitor that "shorts" the cascode at high frequencies and avoids the introduction of an extra pole from the cascode.

The amplifier is compensated by Miller feedback around the second stage through the capacitance of M23. The transistor M24 is biased in the unsaturated region and simulates a resistor. The resistance prevents a forward signal path through the compensation capacitor at high frequencies, that would introduce a right-half-plane zero. Crossover of the complete amplifier occurs at 1 MHz with a 60 degree phase margin. The overall low frequency gain of the amplifier is approximately 3000.

The output follower is M19, with the current source M21. M20 is a cascode device for M19, and reduces the maximum drain to source voltage that will be impressed across the source follower. With no risk of punch-through, M19 can be a minimum channel length transistor, lowering the output impedance of the follower. M37 and M38 operate as a clamp to protect the amplifier output against fault conditions. Without the protection circuit, if the amplifier output is shorted low a large gate to source voltage will be applied to M19. The low impedance follower will likely supply sufficient output current under these conditions to destroy the circuit. The clamp limits the

maximum gate to source drive voltage, and therefore the short circuit current, without affecting normal operation of the follower stage. Operation of the amplifier with the output shorted high is not dangerous, since the available current is merely that supplied by the current source M21.

M12, M13 and M14 are included in the design to form a bias network for the amplifier. The drain of M12 is used as a reference to set the bias currents in the level shifters. The voltage at the source of M14 is level shifted by M25 and M26 to provide a low impedance bias voltage to the cascode transistors in the first stage of the amplifier. Both bias voltages are made available on bonding pads to simplify the testing of the chip.

The amplifier used in the signal path incorporates additional circuitry because of its two chip, partitioned nature. Since the input differential pair consisting of transistors M1 and M2 are located on the sensor chip, macroscopic cabling is required to connect these transistors to the remainder of the amplifier. This cabling introduces large parasitic capacitances at the two drains and the common source of the transistors, and the capacitance will reduce the performance of the amplifier possibly to the point of instability. Voltage follower circuits are used to drive the shields of the coaxial cables that form the connections, so as to "bootstrap" the parasitic capacitance.

The gain of the followers is not quite unity, but the effective capacitance at the critical nodes is reduced by roughly one order of magnitude. The voltage followers are similar in design to the source follower used on the main amplifier output. Cascode devices are included so the output impedance can be lowered, and clamps protect against output shorts.

Both amplifiers operate from ±5 volt power supplies and the signal amplifier consumes 17 milliwatts. Sixty percent of the supply current is used by the four source follower stages.

The signal path amplifier (not including the input transistors) has a fabricated size of 300 μm by 375 μm. A plot of the layout is shown in Figure A.3. The four follower circuits together consume about one third of the total area and are located along the two sides of the layout. The large rectangular regions in the center of the layout are the compensation and feed-forward capacitors of the second stage. The first amplifier stage is located in the upper center. As on the sensor chip, the symmetric transistors in the differential stage are interleaved to enhance matching.

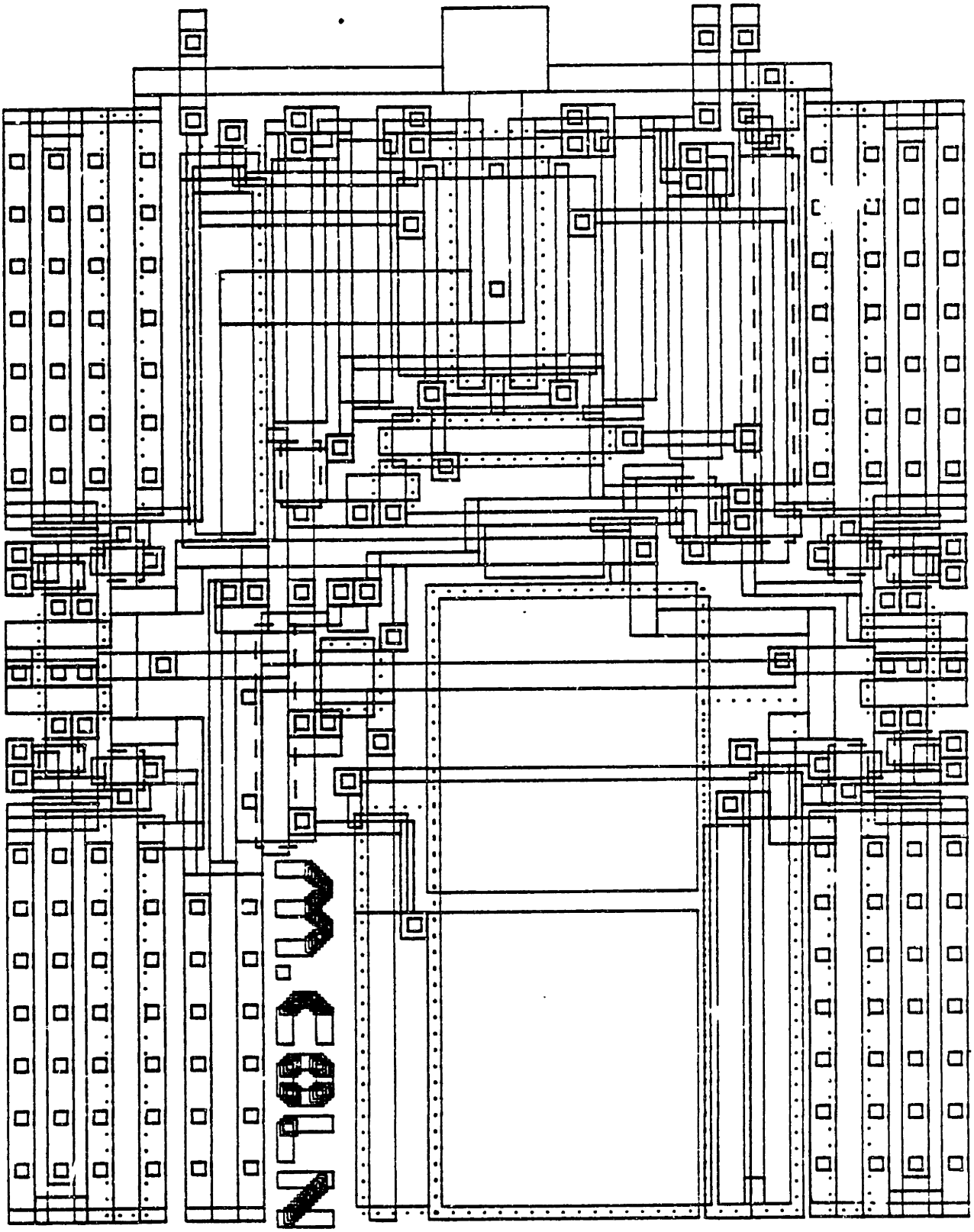


Figure A.3 Layout of Operational Amplifier used on Support Chip (50 μm per inch scale)

APPENDIX B

Synthesizer Hardware Design

The high performance excitation/response measurement system includes a special purpose signal synthesizer. The synthesizer operates as a peripheral device in the microcomputer system that implements the response signal sampling and the correlation algorithm.

The signal synthesizer produces the sensor excitation waveform, the second waveform channel used for the monolithic bridge nulling signal, and digital sampling pulses synchronized with the analog waveforms. These pulses trigger the analog to digital converter that captures the sensor response signal.

As described in section 3.3, the synthesizer generates signals by converting successive elements of precomputed arrays of numeric waveform data to analog voltages using digital to analog converters. The waveform data is computed by the microcomputer from a stored table of trigonometric values. To facilitate the monolithic bridge nulling operation, hardware in the synthesizer supports control of the relative phase and the amplitude of each of the two independent synthesizer channels. It is not necessary for the microcomputer to recompute a new nulling signal (with

adjusted magnitude and phase) on each iteration during the bridge balancing operation.

The synthesizer comprises two circuit boards, one containing the digital hardware and the other dedicated to the analog circuitry. The digital board layout is shown in Figure B.1 and the analog layout is indicated in Figure B.2. Three 26 conductor flat cables connect the two boards, and the analog board includes one additional 26 pin connector for the analog waveform outputs and digital sampling pulse output. Pin designations for the connectors present on both boards are shown in Figure B.3, and the pin designations for the external interface connector on the analog board can be found in Figure B.4.

The peripheral registers in the synthesizer that can be addressed by the microcomputer are shown in Figure B.5. These 8 bit write-only registers are referenced in the input/output address space of the Z-80 microcomputer. The function of each register will be described along with the circuitry that it controls. Integrated circuit chips will be referenced by their board layout location.

Figure B.6 shows the microcomputer bus (S-100 bus) interface circuitry. Chip B11 is the address comparator and detects a bus output transaction directed to the 16 address block associated with the synthesizer. The low order address decoding occurs in chips B9 and B10 (binary to one-

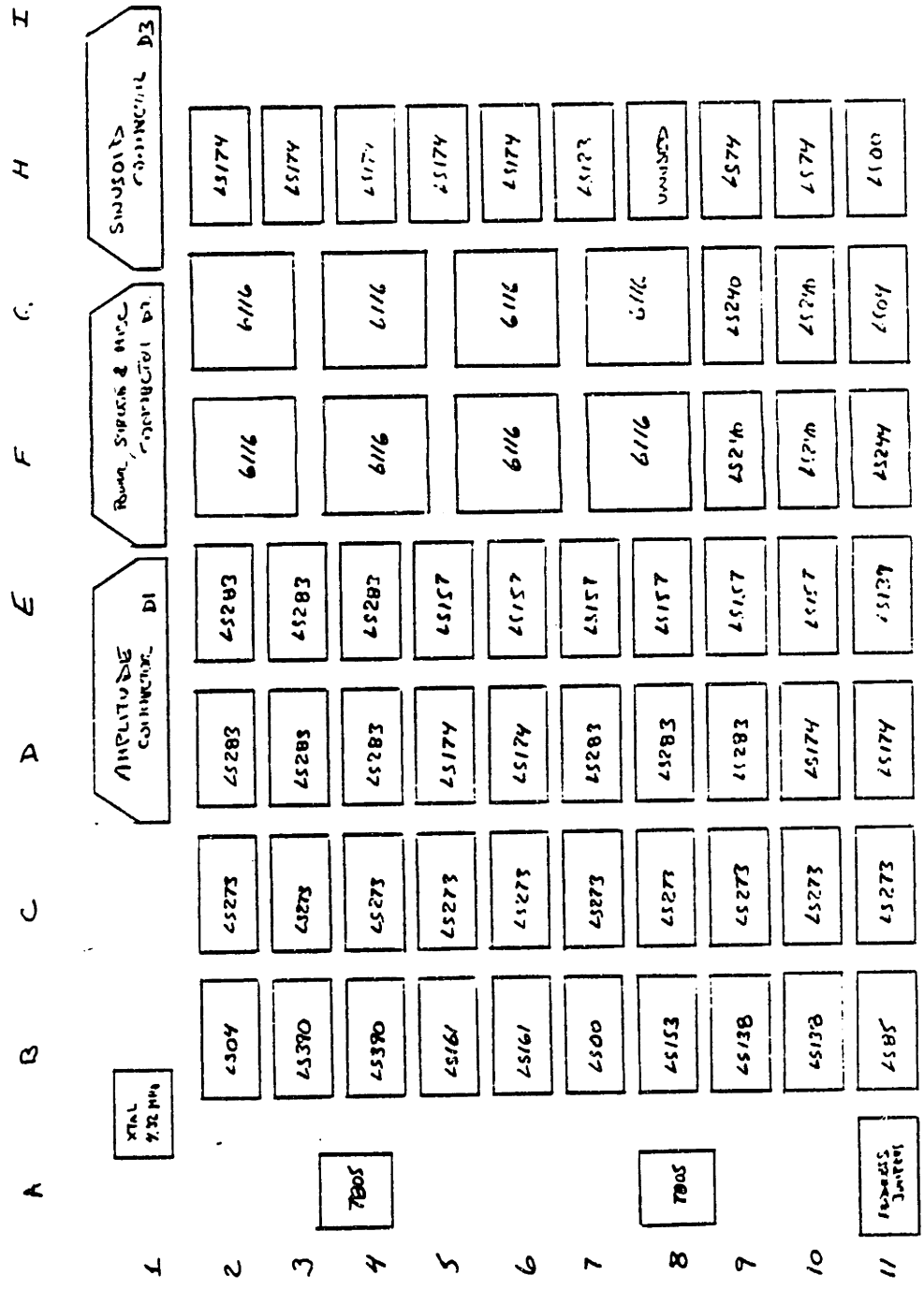


Figure B.1 Synthesizer Digital Board Layout

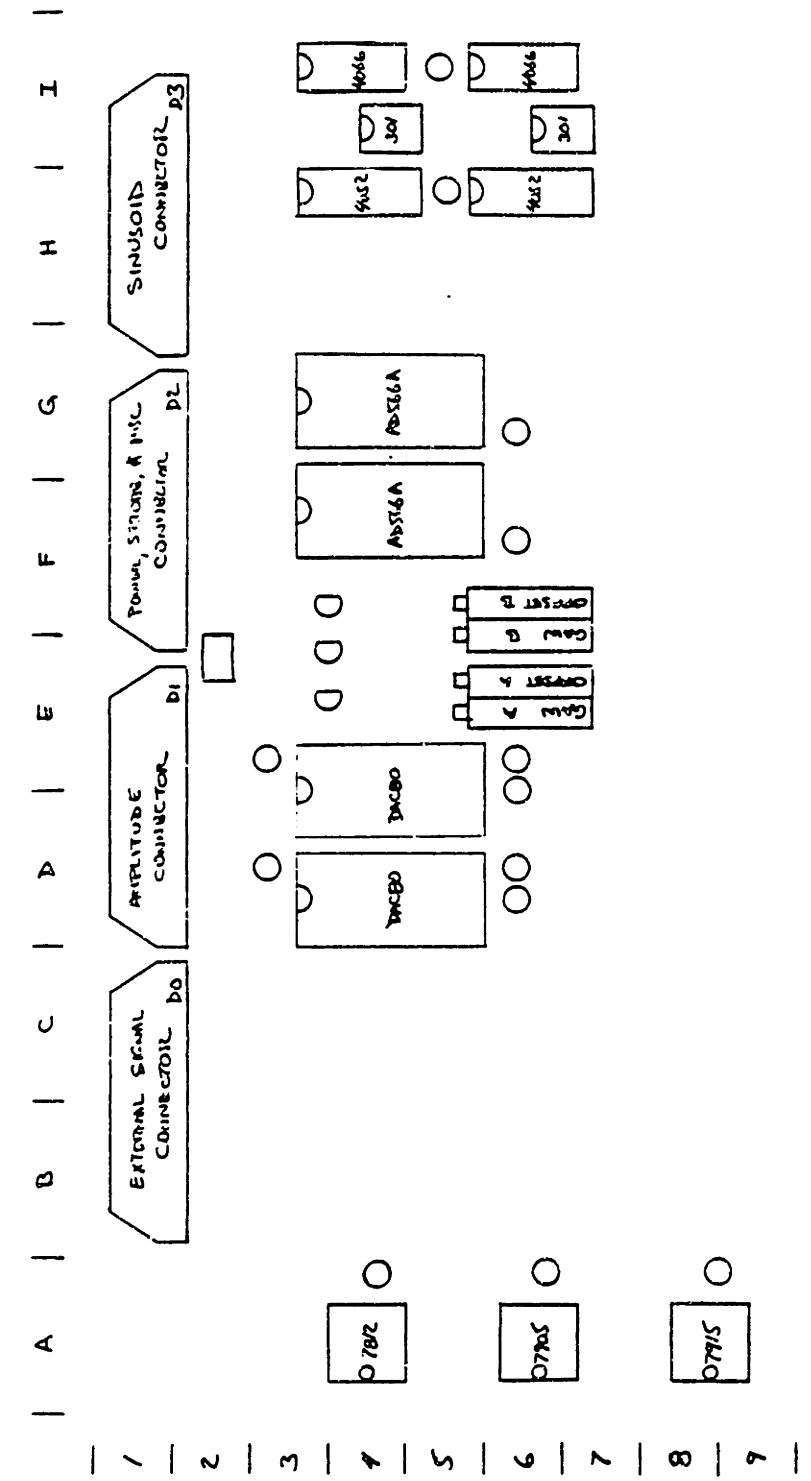


Figure B.2 Synthesizer Analog Board Layout

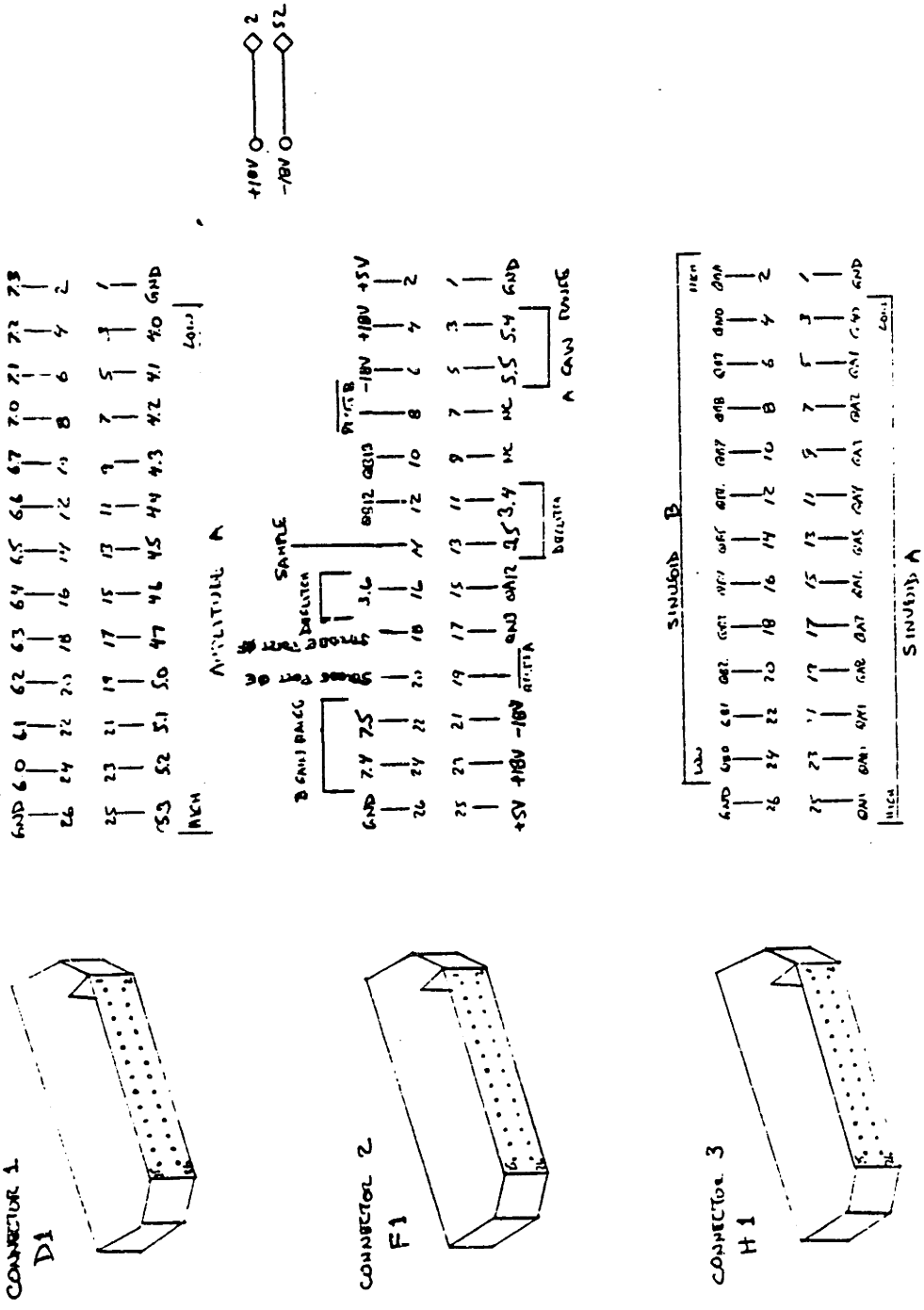


Figure B.3 Internal Connector Pin Designations

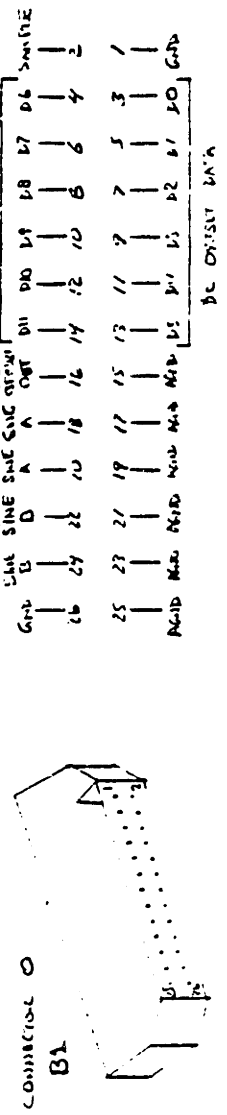


Figure B.4 External Connector Pin Designations

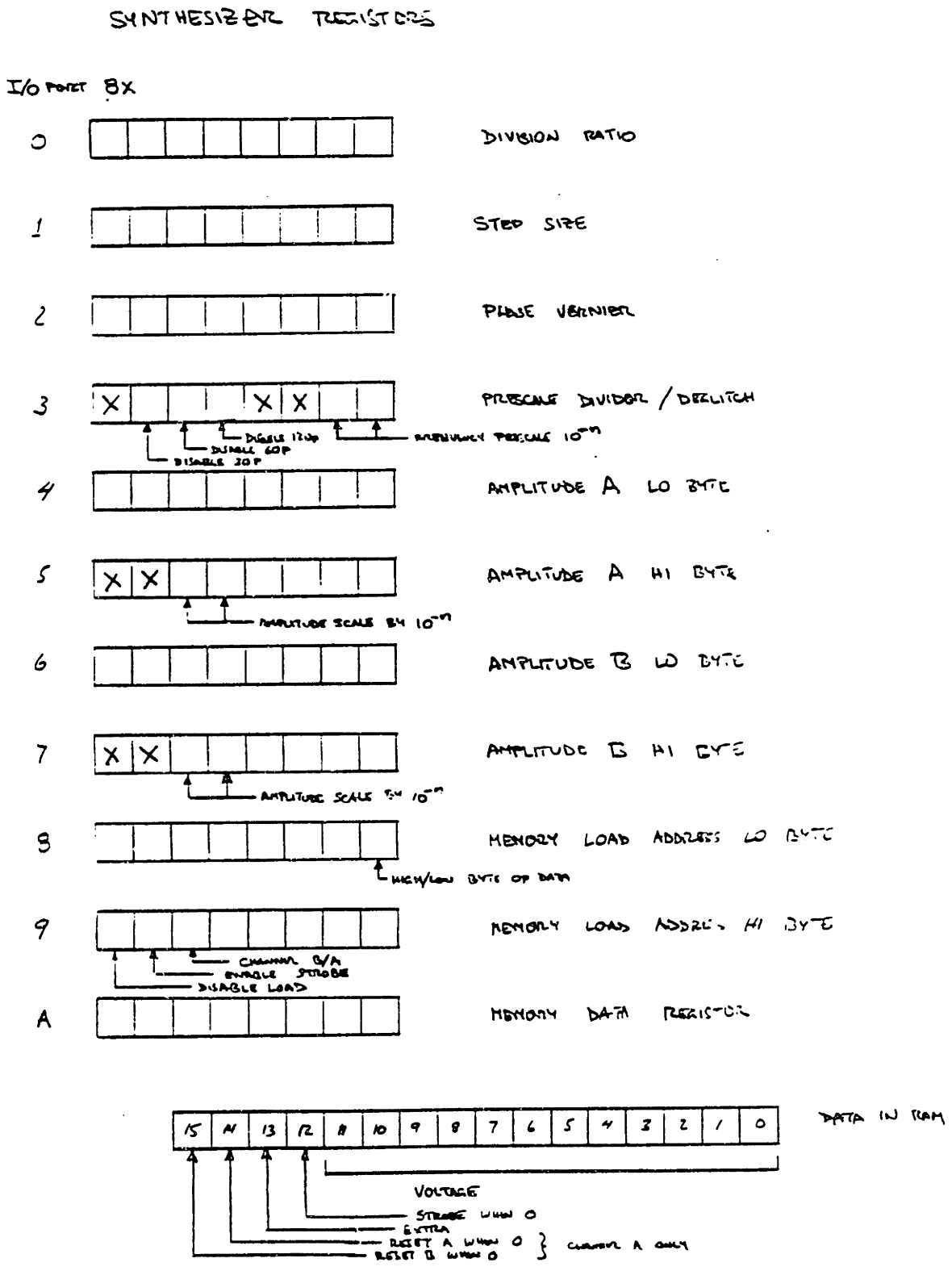


Figure B.5 Synthesizer Programming Registers

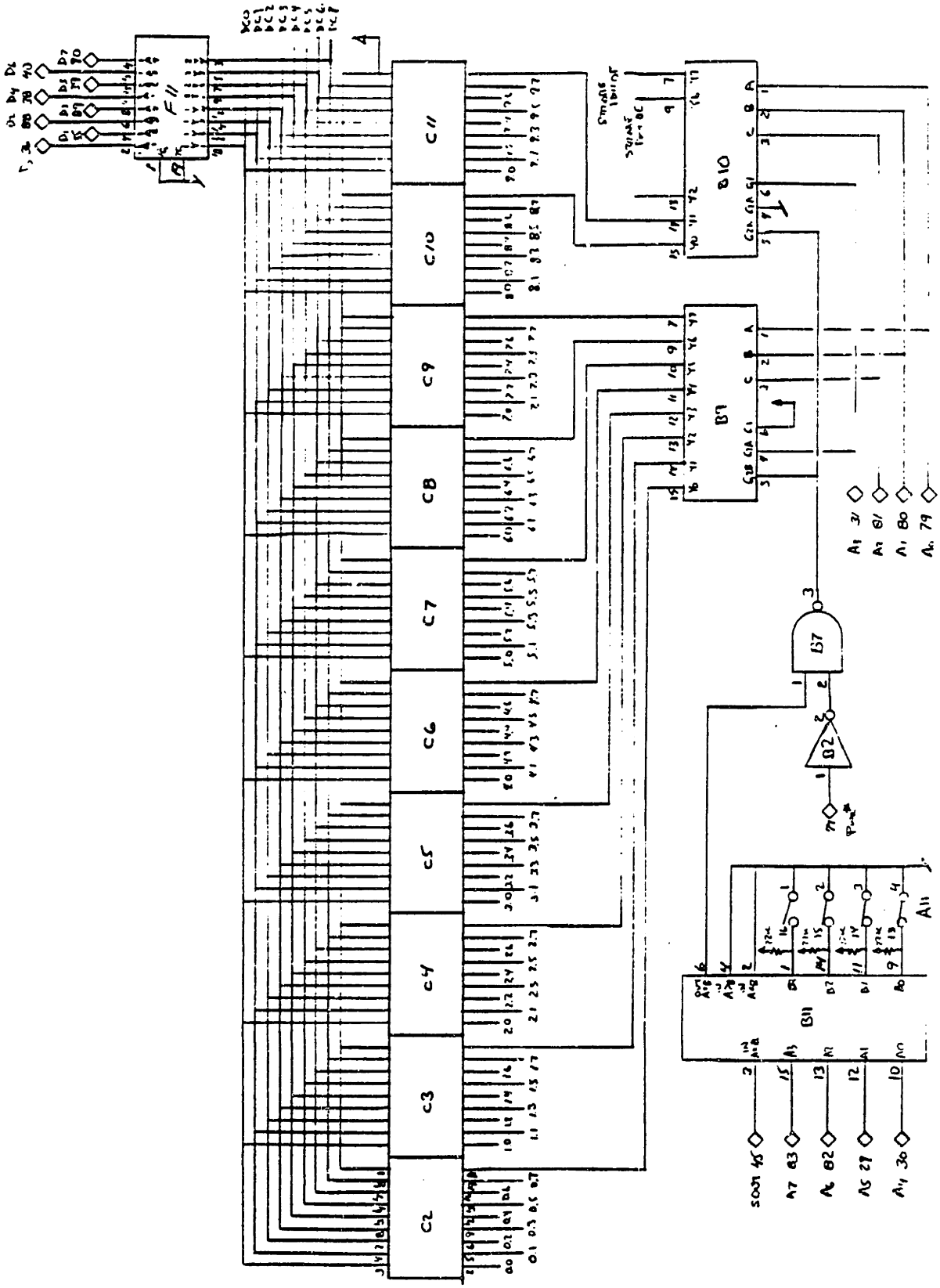


Figure B.6 Bus Interface Circuitry

of-eight decoders) that develop individual write strobes for each register. Eight bit latches C2 through C11 acquire data from the microcomputer bus through buffer F11 on their respective strobe edges. This data is then available to determine the operating parameters of the rest of the synthesizer.

The synthesizer generates frequencies over a wide range--from 0.005 Hz to 10 kHz. A crystal controlled clock is used as the primary frequency reference. Figure B.7 shows the circuitry that develops the synthesizer clocking signals. The quartz crystal (A1) and transistor oscillator (B1) generates the 4.32 MHz reference. For synthesizer output frequencies below 10 Hz, prescaling dividers in chips B3 and B4 divide the quartz reference by 5, 50 or 500 under control of the multiplexer B8. The prescale factor selected is determined by the two least significant bits in programming register 3 (refer to Figure B.5). The prescaled clock is further divided by the presettable binary counters B5 and B6. The loading data on these counters comes from the "division ratio" synthesizer register, and is used to select waveform output frequency values within the decade range chosen in the prescaling section. Load values between 120 and 12 allow selection of frequencies of, for an example decade, 1, 1.5, 2, 2.5, 3, 4, 5, 6, 8 and 10 Hz. The carry output of the presettable counters is divided by an

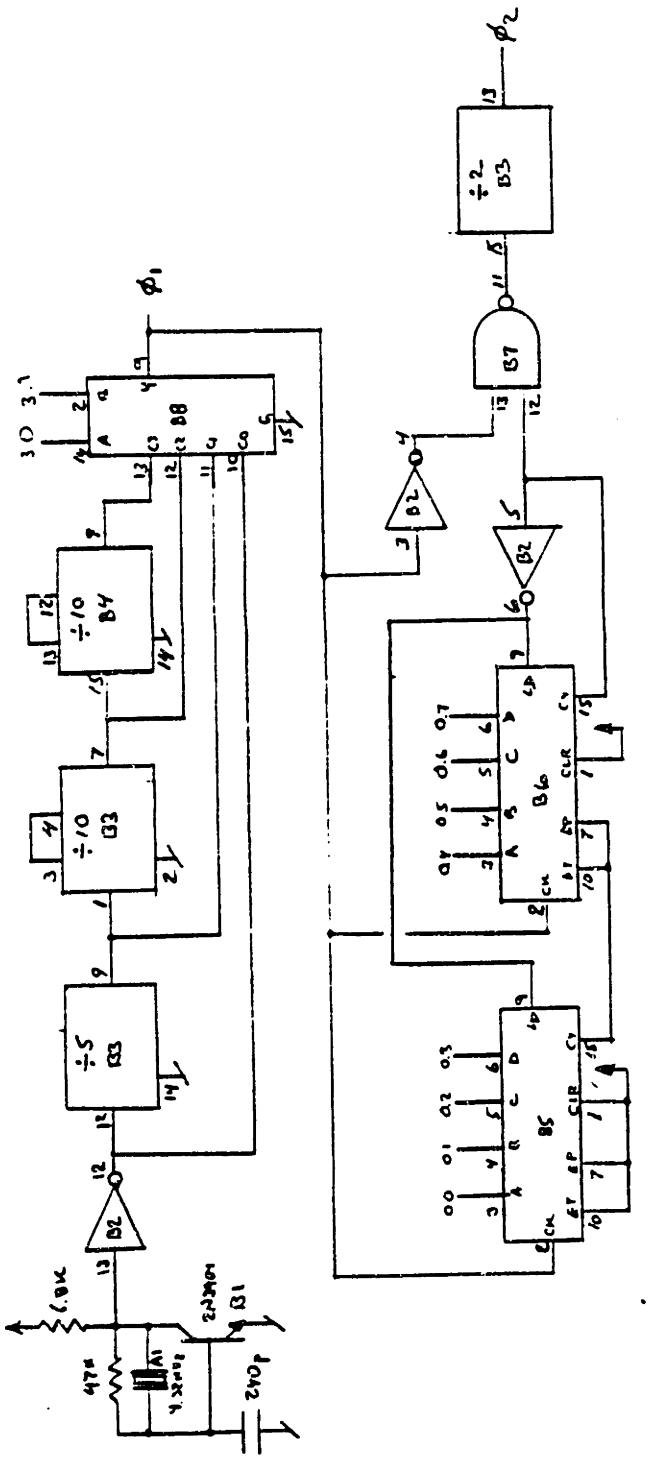


Figure B.7 Clock Generation

additional factor of two to produce a symmetric square wave clock called ø2.

The waveform array size is limited to a maximum of 4096 points; the development software has been written for an array size of 3600 points. For a desired synthesizer output of 100 Hz, the ø2 clock operates at a frequency of 360 kHz, or 2.78 μs for each step of the 3600 point waveform array. This is the maximum rate that the digital to analog converters can be updated. Higher frequencies than 100 Hz can be generated by reducing the number of array points in each complete cycle of the waveform. This reduction can be accomplished by either of two methods. The first method is to generate with the microcomputer and load into the synthesizer a waveform that contains a number of complete cycles in the normal 3600 point array. This method is necessary when a waveform containing several frequencies is to be synthesized, but requires extra synthesizer setup time due to the additional computation.

A second technique for generating higher frequencies is available for single frequency component applications, and this method leads to simpler control software. This hardware technique, shown in Figure B.8, retains the 3600 point data array, but at the higher frequencies steps through the array in units of more than one element at a time. For example, a 300 Hz output waveform is generated by

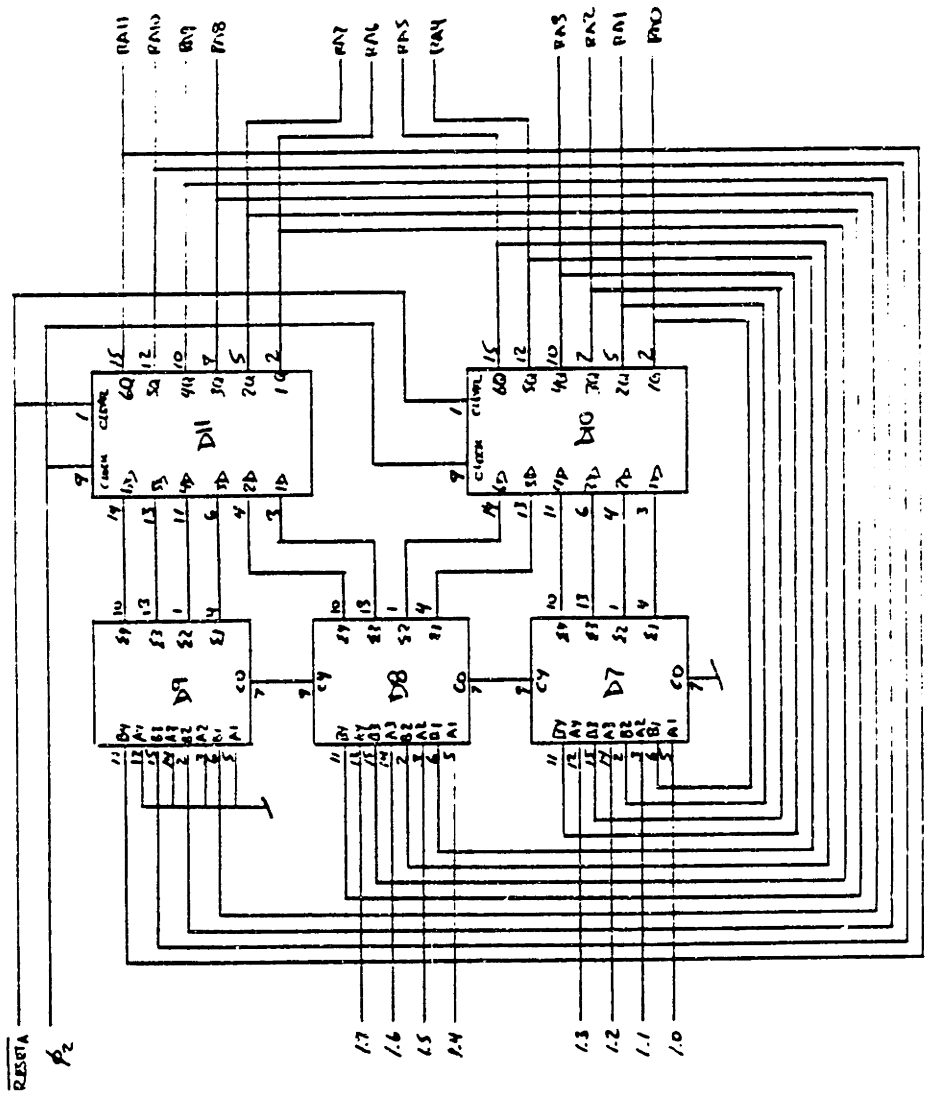


Figure B.8 Channel "A" Address Counters

picking every third element out of the array, and the maximum 10 kHz output selects only every one hundredth element (36 output values per cycle). Referring to Figure B.8, the six bit registers D10 and D11 together generate the twelve bit pointer into the data array memory. D7, D8 and D9 are adder circuits and pass to the register inputs the next address, latched on the ø2 clock. The next address is formed by adding to the present address the step size, maintained in the synthesizer "step size" register (Figure B.5).

The previously described Figure B.8 is the address counter for the synthesizer "A" channel, used to generate the excitation signal waveform. Shown in Figure B.9 is the similar circuit used in the "B" channel, that generates the "monolithic bridge" nulling signal. The additional adder circuits E2, E3 and E4 introduce a programmable phase shift of 0 to 255 steps. This phase vernier allows the relative phase of the excitation and nulling signals to be adjusted in 0.1 degree increments even when the step size is greater than one.

The waveform storage for the "A" and "B" channels is shown in Figures B.10 and B.11, respectively. In the "A" channel, memory circuits F6, F8, G6, and G8 provide 4096 elements of 16 bit storage each for the waveform array. The low order twelve bits are used to hold the digital

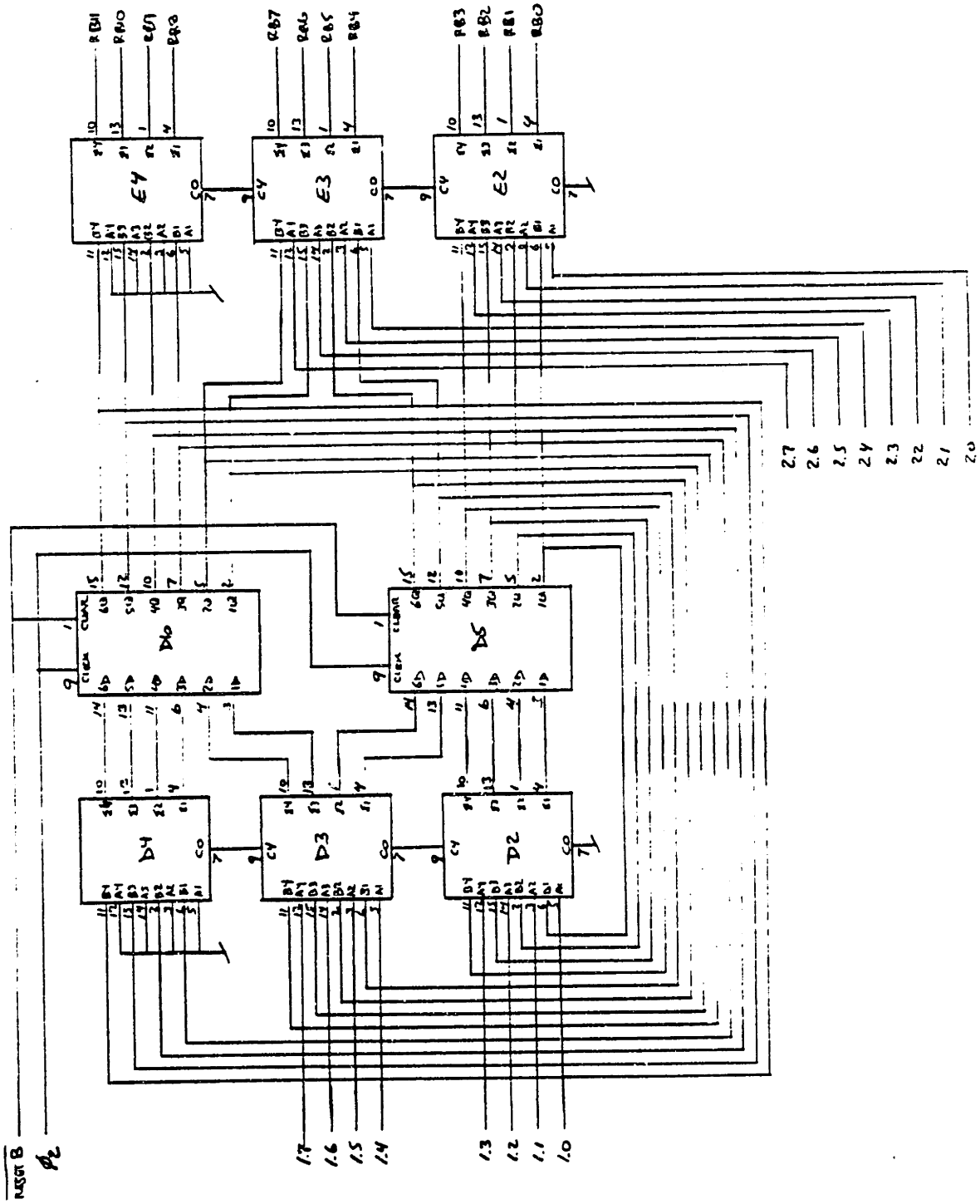


Figure B.9 Channel "B" Address Counters

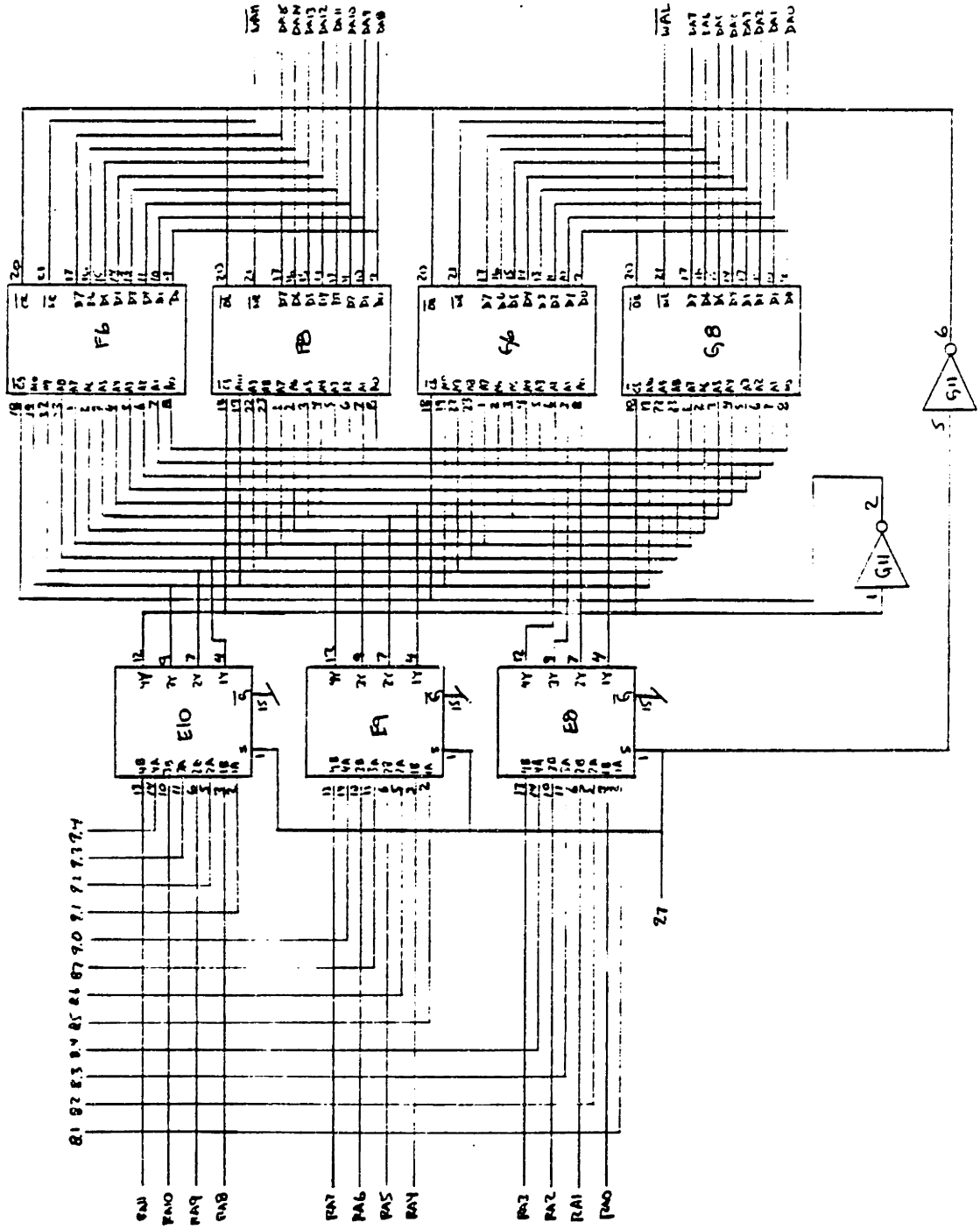


Figure B.10 Channel "A" Waveform Memory

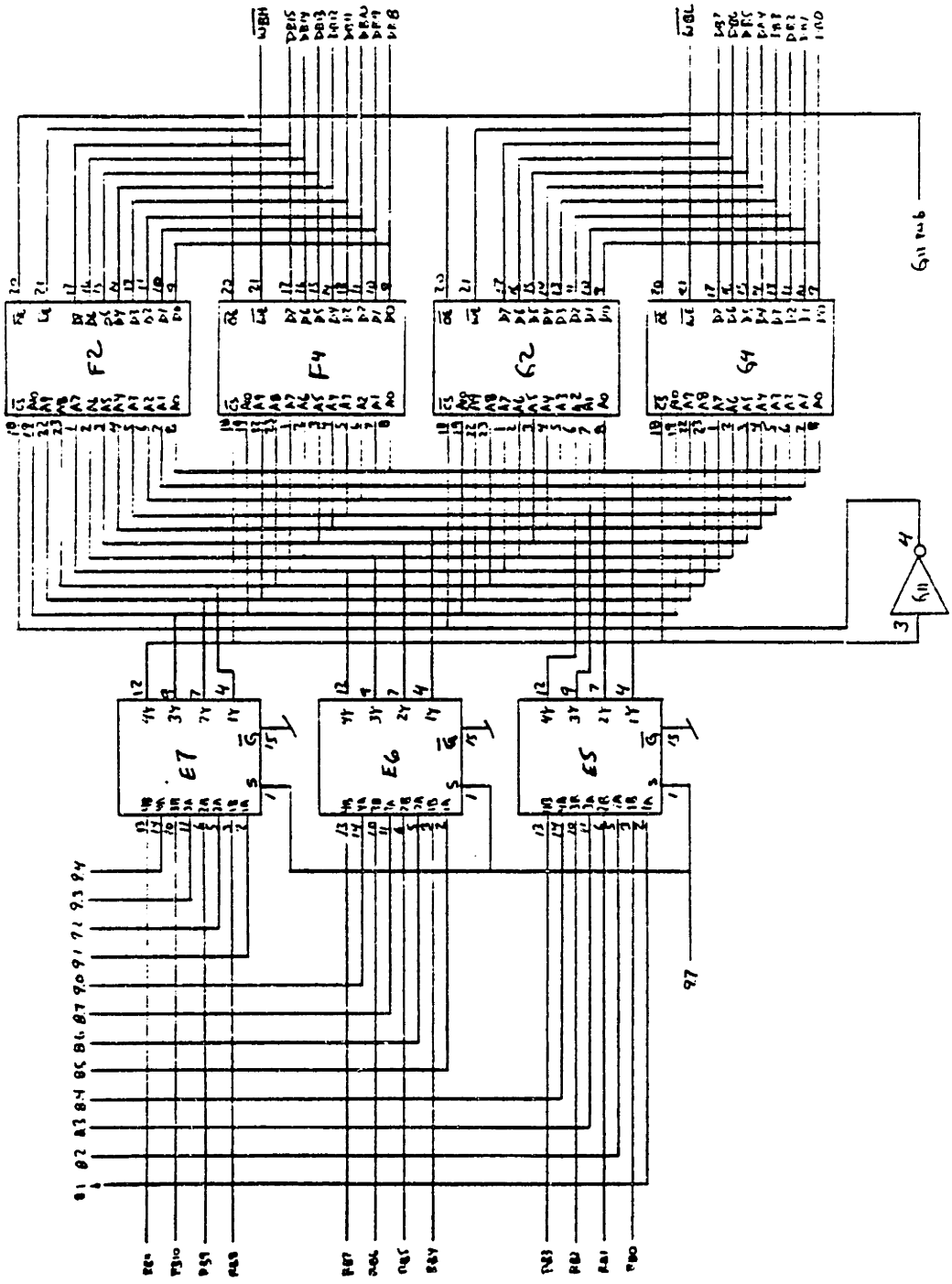


Figure B.11 Channel "B" Waveform Memory

equivalent of the desired output voltage, while the upper four bits are used as digital flags to reset the array counters and to generate the analog to digital converter sampling pulses. The selector circuits E8, E9 and E10 allow the memory to be addressed by the microcomputer through the "memory load" registers indicated on Figure B.5. The computer access is enabled by the high order bit in register 9, and is used when a waveform is to be downloaded into the memory array. The organization of the "B" channel is identical to that of the "A" channel.

The data path for the waveform array storage can be seen in Figure B.12. During microcomputer access, the buffered microcomputer data is directed to the desired memory chip through the eight bit buffers F9, F10, G9 and G10. The correct buffer is selected by the decoder E11, controlled by the memory addressing. The other half of decoder E11 generates the write strobe for the desired memory chip. When the synthesizer is active, waveform data is output from the memory chips in parallel, and loaded into the synchronization registers H2 through H6 on the positive going edge of $\phi 2$. The synchronization registers remove memory access time skew from the data, and thereby minimize output glitches from the digital to analog converters.

Figure B.13 shows the logic associated with the array counter reset, and generation of the sampling pulses for the

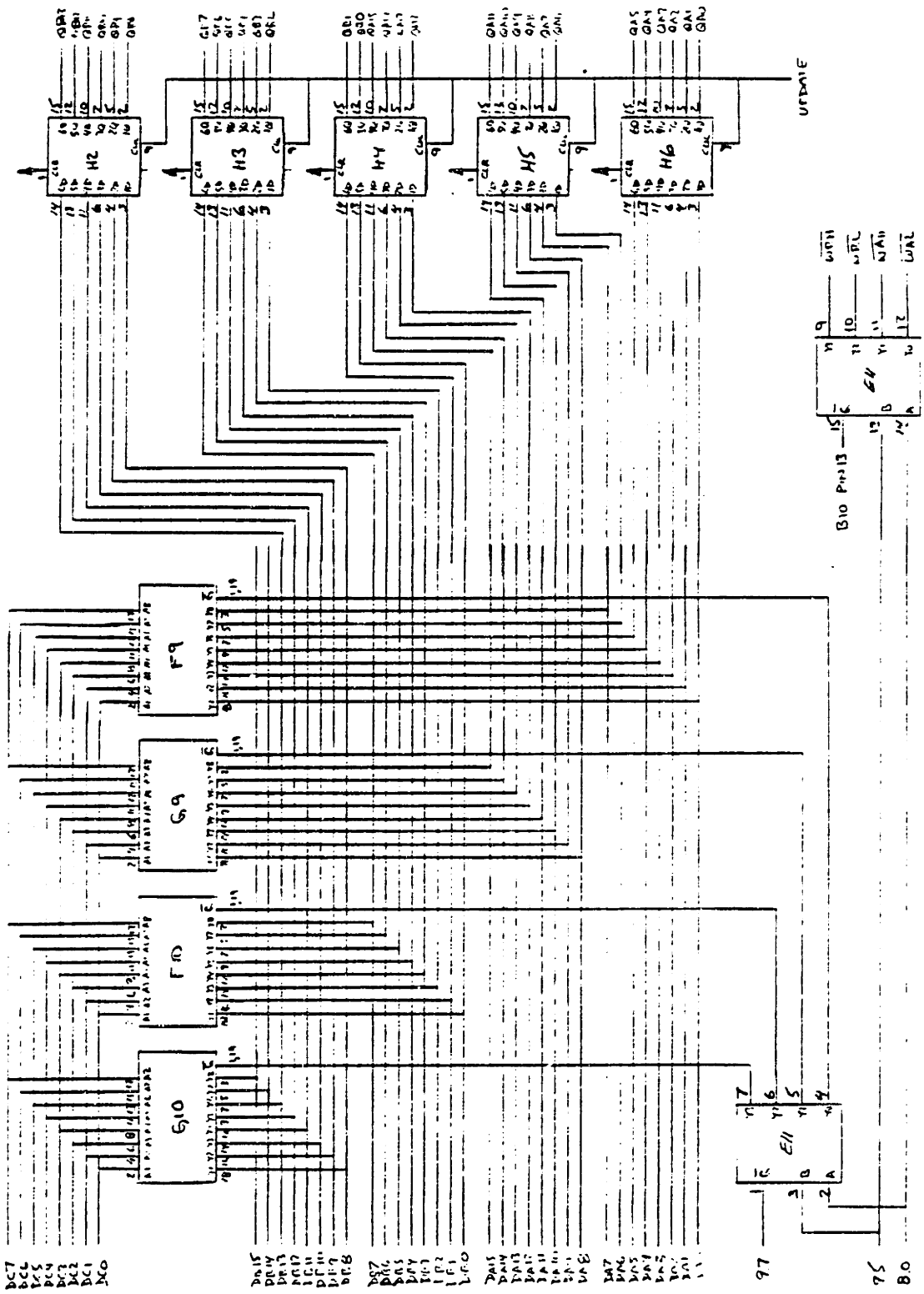


Figure B.12 Waveform Memory Data Path

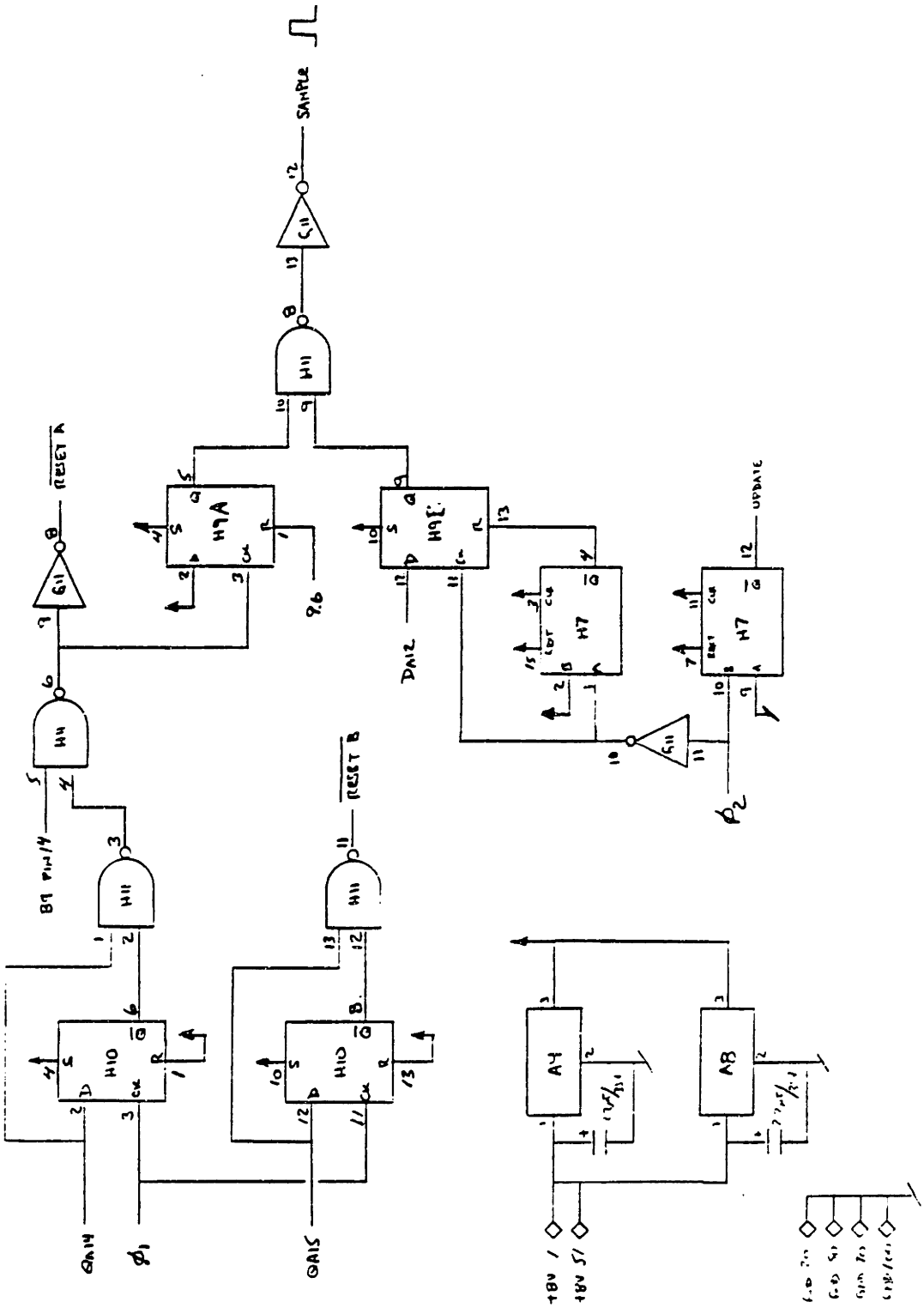


Figure B.13 Reset and Sampling Pulse Generation

analog to digital converter that acquires the sensor response. The array address counters are twelve bit binary counters and therefore will automatically loop with a period of 4096. This period must be changed to 3600 to match the waveform data. Two high bits in the "A" channel stored data are used as flags to independently trigger a reset of each of the two channels. It should be noted that the correct memory location for the flag is affected by the one stage pipeline data delay, and by the "step size" selected. Choosing the "B" channel reset to not coincide with that of the "A" channel introduces a relative phase shift between the "excitation" and "nulling" signals, as required to null the monolithic bridge sensor configuration.

Bit 12 of the memory array is used to trigger an output pulse to the sampling analog to digital converter. The synchronizing flip-flop H9B triggers the sample on the falling edge of the Ø2 clock. This edge is exactly centered between adjacent step changes in the output waveform (triggered on the rising edge), since the Ø2 clock is a square wave. As discussed in section 3.4.1, sampling must occur at the midpoint of a step to avoid aliasing errors. At the lower synthesizer output frequencies the analog to digital converter can acquire a response sample for each element in the synthesizer array. For higher frequencies the converter is limited to 36000 conversions per second. For example, at 10 kHz, one sample is taken for every ten

output waveform steps, or 3.6 samples per cycle of response signal.

Sampling of the response signal must be synchronized with the beginning of a cycle of the excitation waveform, or knowledge of the absolute phase will be lost. This synchronization function is provided by flip-flop H9A. The flop is maintained in a reset state (preventing sampling strobes) until the strobe enable bit in synthesizer register 9 is set high. Once enabled, pulses will only appear following the next channel "A" reset, or at the beginning of the next cycle. Sampling pulses will then continue indefinitely until the register bit is reset, so it is the duty of the microprocessor to cease accepting analog to digital conversions once the data acquisition array is full.

The circuitry on the analog board is shown in Figures B.14 and B.15. The first Figure includes the signal path for the "A" channel, and circuitry common to both channels. Concentrating on the "A" channel, the digital to analog converter D4 develops an output voltage proportional to the numerical value stored in the lower twelve bits of synthesizer registers 5 and 6. This "amplitude" voltage is used as the reference voltage for the multiplying digital to analog converter F4. The digital input to the multiplying converter is the digitized waveform values from the synthesizer memory. Thus, the signal waveform is scaled by

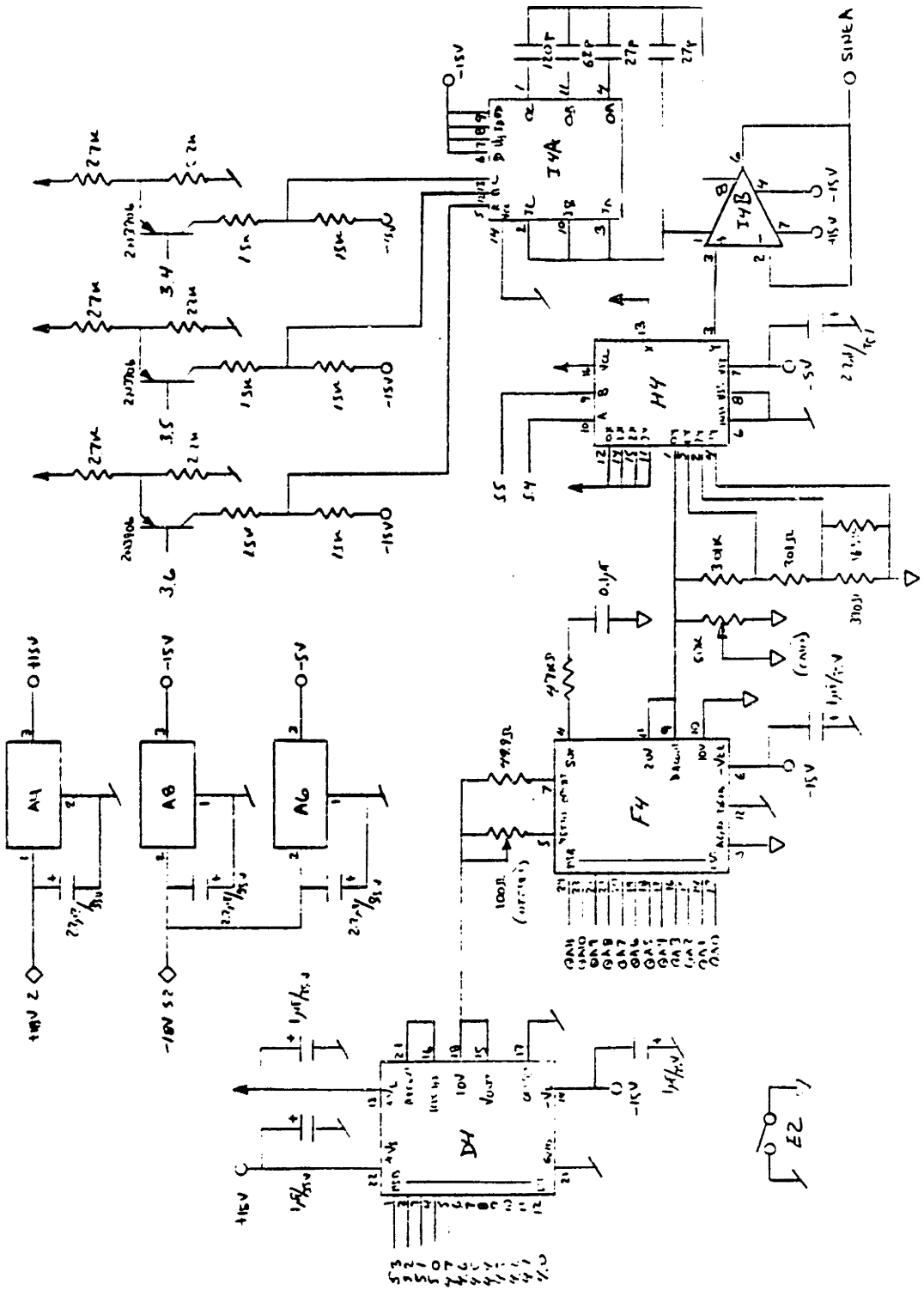


Figure B.14 Channel "A" Analog Circuitry

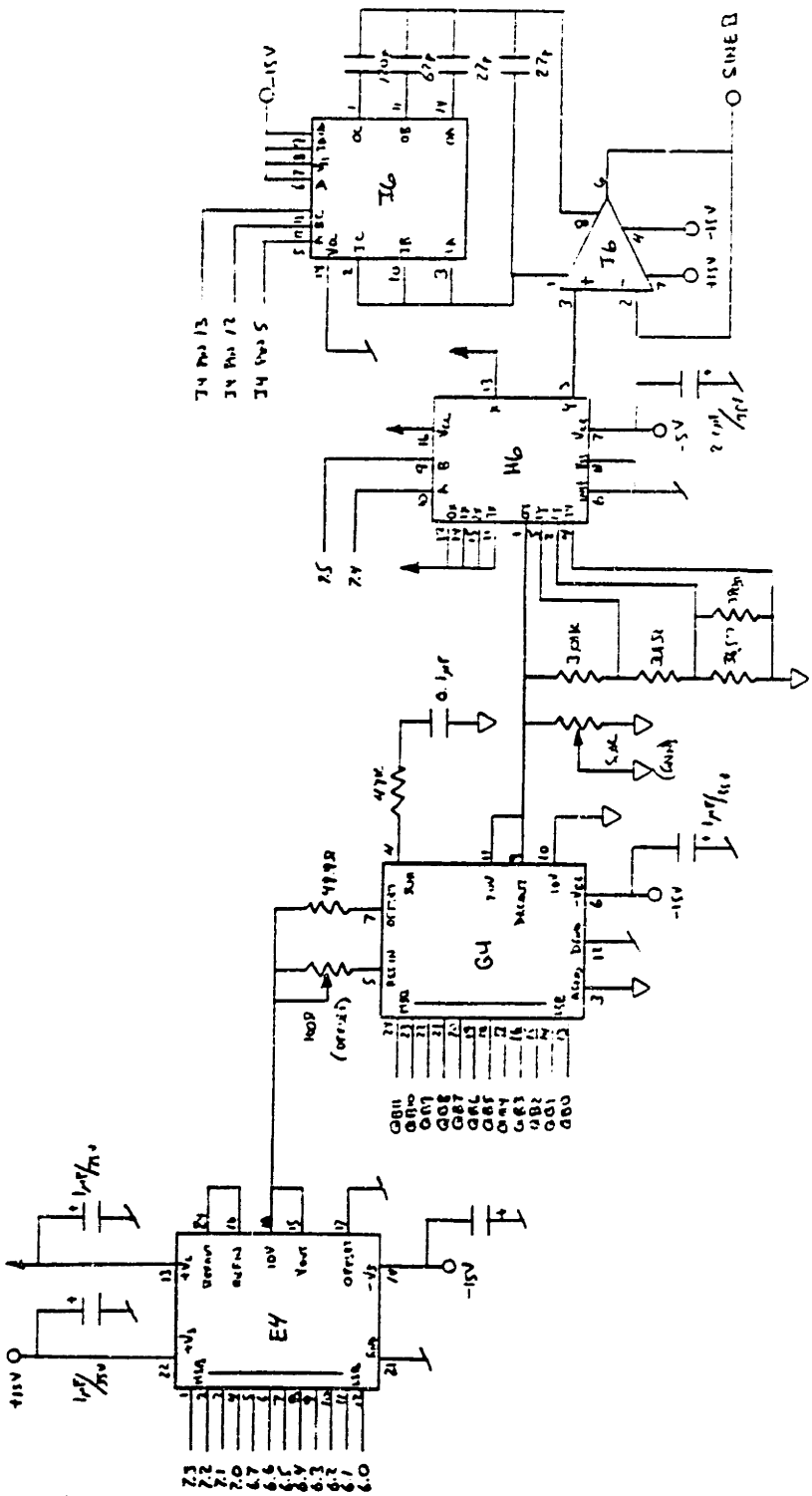


Figure B.15 Channel "B" Analog Circuitry

the synthesizer "amplitude" programming over the 20 decibel range of the multiplying converter reference input. Additional amplitude control is provided by the analog switches in integrated circuit H4. These switches select between taps on the resistor divider that loads the output of the multiplying converter. The divider introduces an additional amplitude scaling of 0, 20 or 40 decibels, selected by the high order bits in the "amplitude" registers. The output signal is buffered by the operational amplifier I4B, then routed to the output connector.

As mentioned earlier, the digital to analog converters are subject to output spikes during transitions from one voltage to the next, due to skew in the switching delays of the converter current switches. The glitches are short, so the error energy can be reduced significantly by incorporating a slew rate limited amplifier in the signal path. If the slew rate becomes too low, the step transition between successive points will suffer and the output error will again increase. The analog switches in circuit I4A allow the compensation capacitor, and therefore the slew rate, of the buffer to be varied depending on the selected frequency output. This deglitch control is implemented in the higher order bits of register 3 of the synthesizer.

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