Modeling, Analysis, and Design of
Switched-Capacitor Battery Cell Balancers

by

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S.B. Electrical Science and Engineering

Massachusetts Institute of Technology, 2021

Submitted to the Department of Electrical Engineering and Computer Science

in partial fulfillment of the requirements for the degree of

Master of Engineering in Electrical Engineering and Computer Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

September 2023

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Abstract

Battery systems have become crucial components in many modern technological solutions. Battery balancers are among the most important parts of these systems because they play a significant role in the battery's lifespan and performance. A novel capacitive-based balancer was designed and tested for two cell and four cell batteries. The key parameters that were optimized are efficiency, balancing time, volume, and cost. A theoretical model of the circuit was derived to guide design optimization. Additionally, simulations were created to predict performance. Custom printed circuit boards were developed and tested.

Thesis Supervisor: James L. Kirtley Jr.
Title: Professor of Electrical Engineering

Thesis Supervisor: William A. Lynch
Title: Research Specialist

Acknowledgments

I have been very fortunate to have Prof. James Kirtley and Dr. William Lynch as advisors. I am thankful for the opportunity to work in their lab group and the creative freedom they've allowed me in pursuing this research.

I would like to thank Navy Capt (RET) Lynn J. Peterson and the Office of Naval Research (ONR) for funding our research enterprise.

I am grateful for my lab mates, Ahmad Negm, Rolando Gonzalez, and Aklilu Aron. Their friendship was instrumental in pushing me through tough times.

I want to extend my thanks to Elaine Ng for her help with LaTeX formatting and the final push towards my thesis.

Finally, and most importantly, I would like to thank my family for their love and support. This work wouldn't have happened without my parents, Mario and Patricia, and brother, Alex.

Thank you all.

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Chapter 1

Introduction

With the latest trends towards electric vehicles and renewable energy storage, battery systems have continued to play an important role in the modern technological landscape. Many batteries are made up of multiple small cells in series (a battery with N cells is referred to as an NS battery) whose charge is nominally identical. However, due to manufacturing tolerances and temperature differences, when a battery pack is placed into operation, different cells in the system can discharge at different rates. This causes the state of charge (SOC) in the cells to differ, which can reduce the lifespan of the battery since some cells can overcharge or undercharge. Thus, battery balancing circuits are needed for batteries with greater longevity [2].

There are two primary ways of balancing: passive and active. Passive balancing involves removing excess charge from cells by using resistors. This means dissipating energy away as heat until the charge of higher SOC cells matches the charge of lower SOC cells in the battery pack. These balancers are simple and cheap, but are extremely inefficient as they bring high energy losses. Active balancing is much better in this regard since it involves moving charge from higher energy cells into lower energy cells. The main trade-off with active balancers is usually complex control circuitry. There are many topologies for active balancing including capacitive, inductive, and transformer based. This thesis will work primarily with capacitive-based balancing topologies [3].

1.1 Background

1.1.1 Batteries

Batteries are electrochemical devices that store and provide electrical energy for various applications. They are used in a wide range of devices, from small electronics like cell phones and laptops to larger applications like electric cars and power grids. The invention of the modern battery is often attributed to Alessandro Volta, who created the first true battery in 1800 [24].

Figure 1-1: Alessandro Volta with two of his inventions: the electric battery (left) and the electrophorus [22].

Batteries consist of one or more cells, which are units that convert chemical energy into electrical energy. Each cell contains an anode, a cathode, and an electrolyte. The anode is the negative electrode,and the cathode is the positive electrode. The electrolyte is the medium that allows the flow of ions between the anode and cathode. When a battery is connected to a circuit, a chemical reaction occurs in the cell that creates a flow of electrons, which generates an electrical current in the circuit [24].
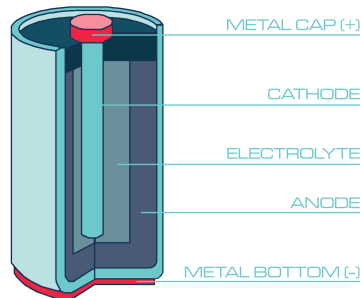
Figure 1-2: Battery Cell Diagram [23]

Figure 1-3: Lithium iron phosphate cell (LiFePO4 battery)

There are many different types of batteries, including alkaline, lead-acid, nickel-cadmium, and lithium-ion. Each type has its own unique characteristics, such as energy density, voltage, and lifespan [28]. Rechargeable batteries, also known as secondary cells, can be recharged and used multiple times, while non-rechargeable batteries, also known as primary cells, can only be used once and must be disposed of afterwards.

1.1.2   Battery Balancing
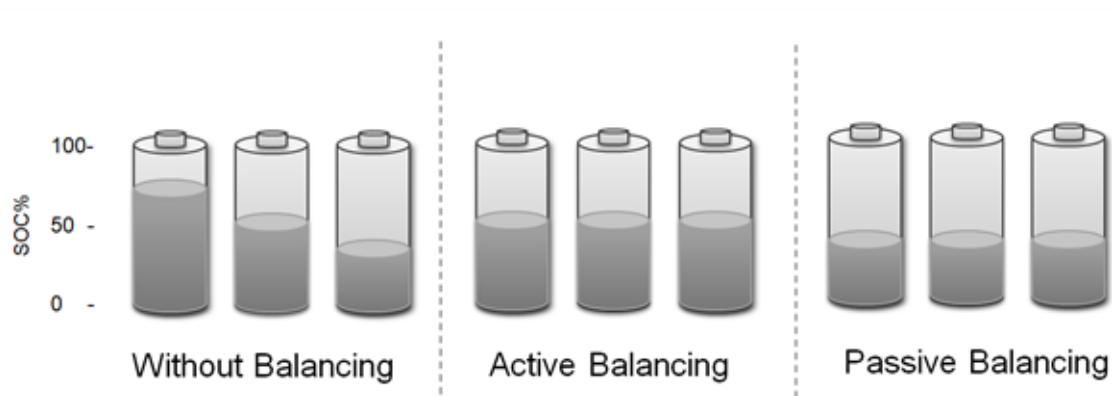
Figure 1-4: Battery state of charge in various balancing modes [25]

Passive and active battery balancing are two different techniques used to balance the state of charge (SOC) of individual cells in a battery pack. The main differences between passive and active battery balancing are [2, 3]:

Passive Battery Balancing:

- Dissipates excess charge from higher SOC cells through a bleed resistor or bypass route

- Simple and cost-effective to implement

- May result in energy losses and heat generation due to the dissipation of excess charge

- Does not redistribute charge between cells during the charging and discharging cycle

Active Battery Balancing:

- Redistributes charge between cells during the charging and discharging cycle

- Utilizes inductive or capacitive charge shuttling to transfer charge between cells

- More complex and expensive to implement compared to passive balancing

- Increases system run-time and charging efficiency by utilizing excess charge from higher SOC cells

Both passive and active battery balancing techniques have their advantages and disadvantages [2, 3]. The choice of balancing technique depends on factors such as the battery chemistry, desired balancing accuracy, power handling capability, and cost considerations. The remainder of the thesis will focus on a subset of active balancing techniques, namely capacitive based balancing in the form of switched-capacitor converters.

1.1.3   Switched-Capacitor Converters (SCC)

Switched capacitor converters are a fundamental building block of analog integrated circuit design [16]. They are electronic circuits that use capacitors to transfer charge when electronic switches are turned on and off. These circuits are used for a variety of applications, including voltage conversion and energy transfer. SCC have several trade-offs when compared to magnetic-based converters including:

Advantages of switched capacitor converters [8, 13]:

- Smaller size and lower weight due to the absence of magnetic components

- Higher efficiency at low power levels

- Easier to integrate into a chip due to their simple structure and lower output power requirements

Disadvantages of switched capacitor converters [8, 10]:

- Lower efficiency at high power levels

- Limited output power because of the limited charge transfer capability of capacitors

- Higher output voltage ripple due to the discrete nature of the capacitor charge transfer

- Limited frequency range due to component parasitics

Overall, switched capacitor converters are ideal for low-power applications, where size and weight are critical, and efficiency is more important than output power. However, for high-power applications, magnetic-based converters are preferred due to their higher efficiency and power handling capabilities.

1.2 Current Gaps in Literature

There is extensive analysis and study dedicated to 2S SCC balancers [7, 10, 11, 20, 21]. However, improvements can be made in low-entropy modeling of and theoretical insight into the behavior of higher order SCC balancers [18, 27, 30, 32, 33]. The author envisions an impedance-based approach to modeling of higher order balancers to yield balance time constants for every battery cell and gain intuition on how each cell voltage waveform evolves over time. The author believes that this can be achieved through the application of clever circuit techniques [6, 17, 19]. Lastly, there also seems to be some SCC balancer topologies that remain undiscovered.

1.3 Thesis Contributions

The shortcomings in the current state of SCC battery balancing as outlined in Section 1.2 presents opportunities for theoretical insights and improvement of practical circuit design. This thesis aims to address some of these gaps through the following contributions:

1. Insights into modeling and analysis of higher order balancers. A potential pathway to an analytical solution is shown.

2. Presentation of a new SCC balancing topology

3. Practical implementation of the latter.

1.4 Thesis Outline

The goal of this thesis is to address some of the gaps in SCC battery balancing circuits. In Chapter 2, we describe the modeling and analysis of these circuits starting from their fundamental building block: the canonical 2S SCC battery balancer. We perform a static and dynamic analysis on this balancer, deriving an average model of circuit behavior to gain intuition into its operation and to drive practical design methodology. This model is then generalized for higher order balancers. Additionally, a pathway for theoretical insights and meaningful analytical solutions are discussed. The chapter will also introduce a new balancing topology. Chapter 3 applies the derived models on various SCC topologies to compare their balancing times. In Chapter 4, we build three practical SCC battery balancers, the final one being our proposed balancer topology. Experimental results, practical design considerations, and part selection are also provided. Chapter 5 closes this thesis with conclusions on the modeling, analysis, and design of SCC battery balancers. We also present opportunities for future investigations.

Chapter 2

Modeling and Analysis of Switched-Capacitor Battery Balancers

2.1 Canonical 2-Cell SCC Balancer

The fundamental building block for all SCC balancer topologies is the canonical switching cell. It is comprised of two switches: one connected to the negative terminal of the battery cell, and the other connected to the positive terminal. This canonical switching cell connects to an energy tank (usually comprised of capacitors and/or inductors), which transfers charge efficiently from higher energy cells to lower energy cells.
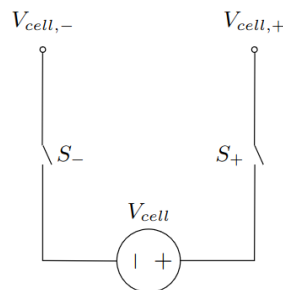
Figure 2-1: Canonical Switching Cell

All SCC battery balancers are essentially energy tanks interfacing with each switching cell such that the average voltage of the cells in aggregate is imparted as a steady state voltage constraint on all N cells: $\lim_{t\to\infty} V_{cell,n}(t) = \frac{V_{battery}}{N}$ (see Fig. 2-2) where $V_{cell,n}$ is the voltage of the nth cell and $V_{battery}$ is the battery voltage. One way to prove this equilibrium condition is through the principle of virtual work, as shown in Appendix C.1 [31].
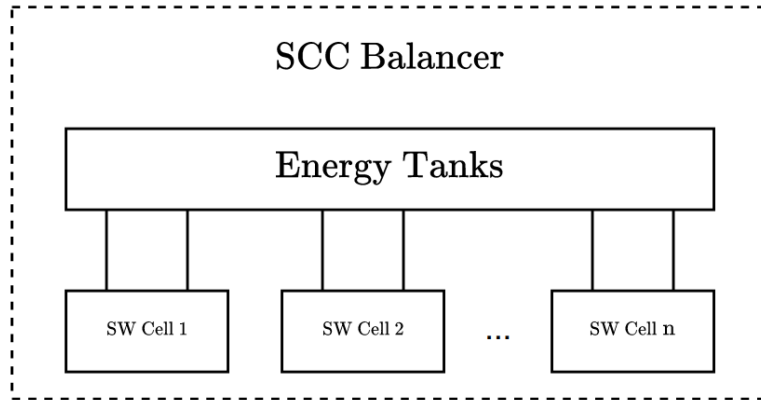
Figure 2-2: SCC Balancer Abstraction

We can use 2 canonical switching cells connected together by a capacitive energy tank to construct the simplest possible 2S SCC battery balancer (see Fig. 2-3). The
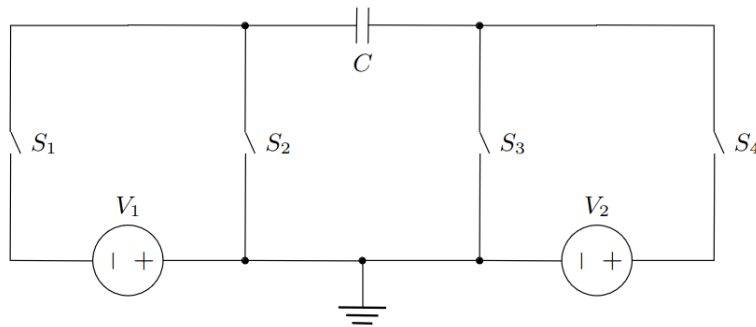
Figure 2-3: Canonical 2S SCC Battery Balancer

odd numbered switches share the same state and are complementary to the even numbered switches. This means that in a given switching state, one of the cells (V_1 or V_2) will be connected in parallel with the flying capacitor energy tank C (see Fig. 2-4). The resistor R is the combination of capacitor series resistance (ESR) and the resistance of the switches. The switches are controlled via pulse width modulation

(PWM) with duty cycle D and switching frequency f_s. From the point of view of the
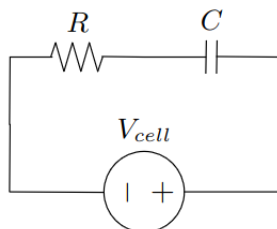
Figure 2-4: Switching State of 2S SCC Balancer

flying capacitor, it will see a pulse wave input oscillating between V_1 and V_2 with a DC average of $DV_1 + (1 - D)V_2$ and AC peak-to-peak amplitude[1] of $\Delta V = V_1 - V_2$. These SCC circuits typically operate with $D = 0.5$ to minimize impedance [15]. Thus, the average flying capacitor voltage $\langle V_c \rangle = \frac{V_1 + V_2}{2}$ (refer to Fig. 2-5). We also know from periodic steady state (PSS) analysis that $\langle i_c \rangle = 0$ [4].
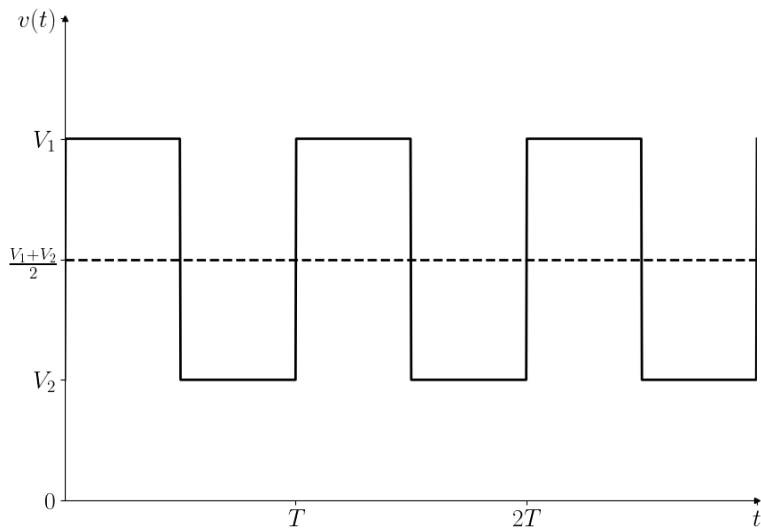
Figure 2-5: Square Wave Input to Flying Capacitor

2.1.1   Static Analysis

We can initially model the battery cells as ideal voltage sources to gain intuition on the static operation of the circuit and then relax this constraint later to perform a dynamic analysis. We can model the average behavior of the circuit by defining an

---

[1]This assumes that $V_1 > V_2$.

equivalent impedance R_{eq} that connects the unbalanced battery cells and carries out the charge transfer (see Fig. 2-6) [5, 10]. The cell voltage differential and equivalent
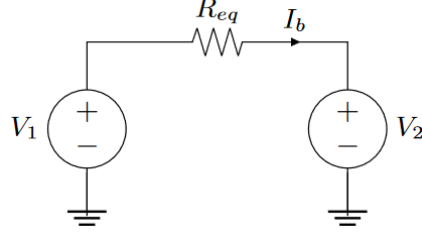
Figure 2-6: Equivalent Circuit Model of 2S SCC Balancer

impedance determine the balance current $I_b = \frac{\Delta V}{R_{eq}}$. By inspection of Fig. 2-6, one can see that $\langle i_1 \rangle = -\langle i_2 \rangle = -I_b$, where i_1 and i_2 are the battery cell currents. It is worth noting that in most practical designs, there will be some difference in the magnitude of $\langle i_1 \rangle$ and $\langle i_2 \rangle$ due to resistive mismatches in the circuit. It is thus better to define the balance current as

$$I_b = \frac{|\langle i_1 \rangle| + |\langle i_2 \rangle|}{2} \tag{2.1}$$

The power loss through the flying capacitor will be determined by its root mean square (RMS) current, which can be expressed as $i_{RMS} = \sqrt{i_{DC}^2 + i_{RMS,AC}^2}$. Since $i_{DC} = \langle i_c \rangle = 0$, then $i_{RMS} = i_{RMS,AC}$. From Fourier analysis, it can be shown that $i_{RMS,total} = \sqrt{\sum_{k=1}^{N} i_{k,RMS}^2}$ if the set of i_k form an orthogonal basis [4]. With this in mind, we can express the capacitor RMS current as

$$i_{c,RMS} = \sqrt{i_{1,RMS}^2 + i_{2,RMS}^2} \tag{2.2}$$

Assuming resistive symmetry, $i_{1,RMS} \approx i_{2,RMS}$ and therefore $i_{c,RMS} \approx \sqrt{2} \cdot i_{1,RMS}$. The average power loss in the flying capacitor is thus

$$\langle P_{c,loss} \rangle = i_{c,RMS} \cdot V_{c,RMS} \approx \sqrt{2} \cdot i_{1,RMS} \cdot \frac{V_1 + V_2}{2} \tag{2.3}$$

Note that $V_{c,RMS} \approx \frac{V_1+V_2}{2}$ if the capacitor voltage ripple is sufficiently small, as is in the case if the equivalent impedance is dominated by the circuit series resistances. It is crucial to understand why and how R_{eq} changes as a function of both switching frequency and duty cycle [15, 16].

2.1.2   Equivalent Impedance

We can define the circuit time constant $\tau = RC$ (see Fig. 2-4) and compare its magnitude to the switching period T_s. From here, we can distinguish between 3 different regions for R_{eq} as the switching frequency is varied. If $\tau \ll T_s$, then the capacitor fully charges and discharges within each switch period. This implies that R_{eq} will behave as a capacitive impedance (see leftmost region of Fig. 2-7). If $\tau \gg T_s$, the capacitor voltage ripple is approximately linear since the charge interchange is very small. This causes R_{eq} to behave as a resistive impedance (see rightmost region of Fig. 2-7). Finally, if $\tau \approx T_s$, there is partial charge interchange from the capacitor to the cells. This will cause R_{eq} to behave as an intermediate impedance between the two main regions (refer to the curved section of impedance curve in Fig. 2-7). This characterizes the transition from the capacitive region to the resistive region. The total impedance formula is commonly approximated as

$$R_{eq,total} \approx \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{2.4}$$

where R_{SSL} is the impedance in the capacitive region (slow switching limit) and R_{FSL} is the impedance in the resistive region (fast switching limit) [15]. The 2S canonical SCC balancer has $R_{SSL} = \frac{1}{f_s C}$ and $R_{FSL} = \frac{R}{D(1-D)}$. However, it is worth noting that in practice, there is an additional region to R_{eq}.

A practical R_{eq} curve is shown in Fig. 2-8. There will always be some stray (or intentional) inductance present in any practical circuit and as such will affect the equivalent impedance. This third region is commonly referred to as the inductive switching limit (ISL) [12]. The transition to ISL will depend upon the circuit's quality factor Q. For an RLC circuit whose impedances depend on duty cycle, the quality
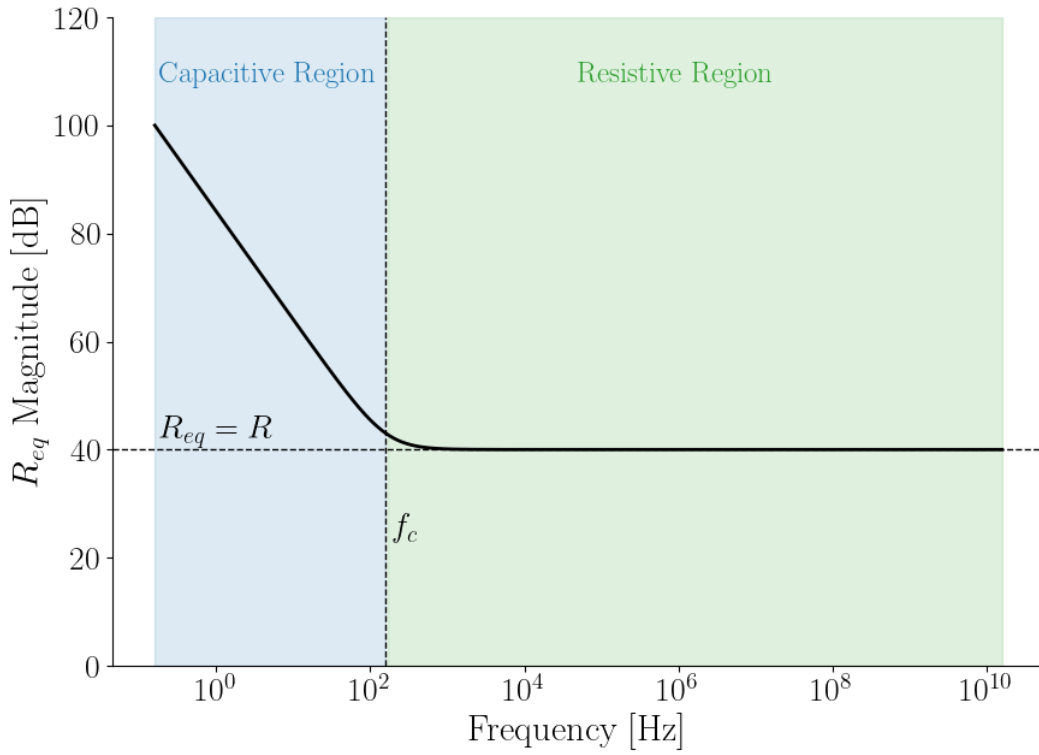
Figure 2-7: Ideal Equivalent Impedance vs Frequency
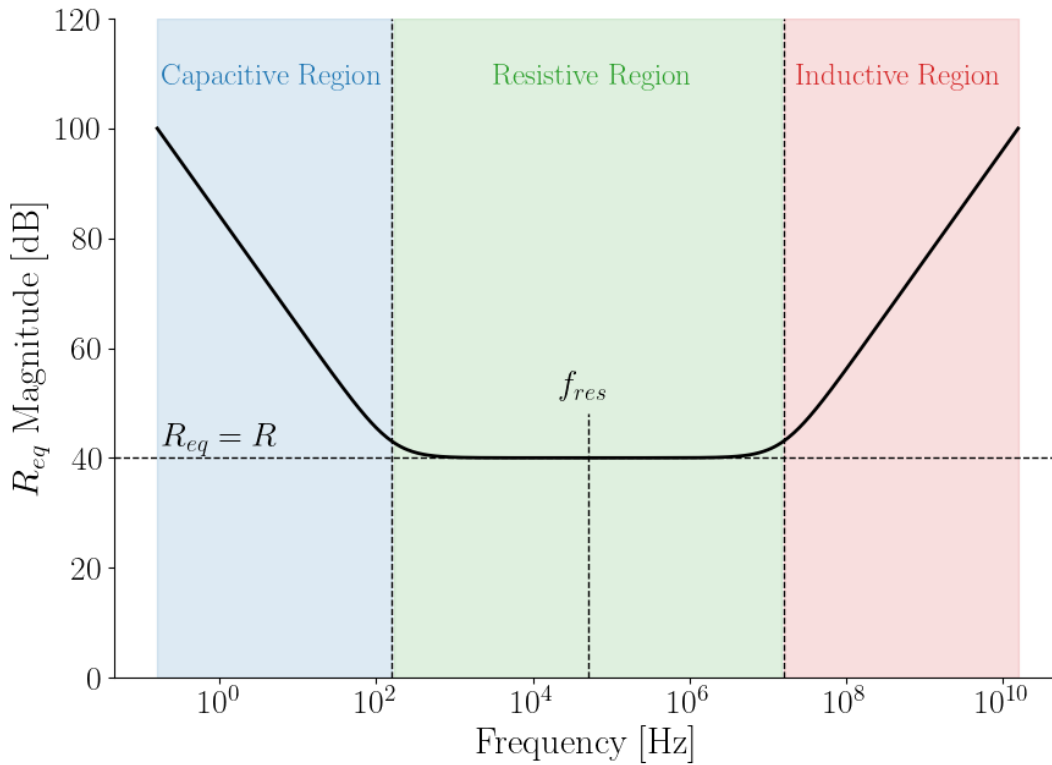
Figure 2-8: Practical Equivalent Impedance vs Frequency

factor is

$$Q = \frac{2\pi f_{res} L}{R} \tag{2.5}$$

where $f_{res} = \frac{D}{\pi\sqrt{LC}}$. The Q factor will approach zero as L becomes smaller. This will cause the transition from the resistive region to the inductive region to occur at an arbitrarily large frequency and the practical RLC impedance curve will look more like the ideal RC impedance curve. It is recommended to operate the circuit near resonance for high Q factors, which can also occur if R or D is low with L fixed. Additionally, variations in duty cycle will change the magnitude and frequency cutoffs of R_{eq} throughout the various regions in Fig. 2-7 and 2-8. For a detailed discussion on the trade-offs involved with intentionally augmenting the flying capacitor's impedance with a series inductor, please refer to [12, 34].

2.1.3 Dynamic Analysis

To approximate the 2S canonical SCC balancer's dynamic behavior, we can replace the ideal voltage sources with a simple battery cell model in the form of a very large capacitor. This will approximate a real battery cell's behavior in its linear region of operation. This opens up the opportunity for meaningful analytical solutions and thus provides a reasonable estimate on balancer performance. One can utilize more complicated cell models to predict battery cell performance beyond the linear region, but we will utilize this large capacitor model for the remainder of this thesis [28].
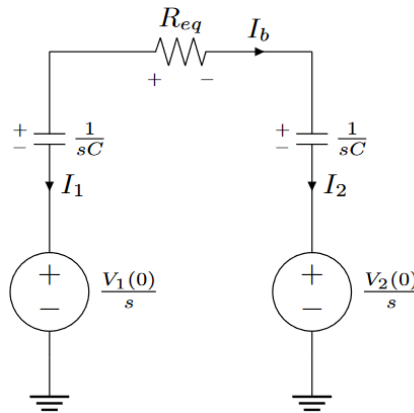
Figure 2-9: Equivalent Circuit Model of Dynamic 2S SCC Balancer

We will begin by replacing V_1 and V_2 with capacitors C_1 and C_2 (see Fig. 2-9). Each capacitor is initialized to the respective voltage of its original ideal voltage source. Furthermore, let $C_1 = C_2 = C$. We now can take the Laplace transform of each circuit element to construct its s-domain analog. The equations of motion for this circuit (KVL and KCL) are

$$V_1(s) - I_b R_{eq} - V_2(s) = 0 \tag{2.6}$$

$$V_1(s) - \frac{V_1(0)}{s} - \frac{I_1}{sC} = 0 \tag{2.7}$$

$$V_2(s) - \frac{V_2(0)}{s} - \frac{I_2}{sC} = 0 \tag{2.8}$$

$$I_1 + I_2 = 0 \tag{2.9}$$

$$I_b - I_2 = 0 \tag{2.10}$$

This is just a first-order linear system of ordinary differential equations (ODEs). Solving this system yields the following voltage equations

$$V_1(t) = \left\{ t \geq 0 : \frac{V_{batt}}{2} + \frac{\Delta V_{12}}{2} e^{\frac{-2t}{RC}} \right\} \tag{2.11}$$

$$V_2(t) = \left\{ t \geq 0 : \frac{V_{batt}}{2} - \frac{\Delta V_{12}}{2} e^{\frac{-2t}{RC}} \right\} \tag{2.12}$$

where $V_{batt}(t) = V_1(0) + V_2(0) = V_1(t) + V_2(t)$ since we shall assume that $\frac{d}{dt} V_{batt} = 0$. Additionally, we express the initial voltage differential as $\Delta V_{12} = V_1(0) - V_2(0)$. This system is comprised of two poles (or eigenvalues) at locations $\lambda_k = [0, -\frac{2}{RC}]$, which characterize system stability and settling time. Since $\Re(\lambda_k) \leq 0$, the system is stable [26]. The balance time τ_b can be expressed as

$$\tau_b = \frac{RC}{2} \ln \left(\frac{|\Delta V_{12}|}{\Delta v_b} \right) \tag{2.13}$$

The balanced voltage differential Δv_b is chosen arbitrarily by the circuit designer. We will use $\Delta v_b = 10$ mV for numerical characterization of the balance time in later

sections of this thesis. The average efficiency of the balance process is

$$\eta_b(t) = \frac{P_{out}}{P_{in}} = \frac{\min\left(|i_1 V_1|, |i_2 V_2|\right)}{\max\left(|i_1 V_1|, |i_2 V_2|\right)} \tag{2.14}$$

If we assume that $V_1 \geq V_2$ and utilize Eq. (2.9), then $\eta_b(t) = \frac{V_2(t)}{V_1(t)}$. Thus, the average balance process efficiency is purely determined by the distance between battery cell voltages. If the linear region of the cell voltages is constrained to be within the range $[3.0, 3.4]$, as is generally the case with LiFePO4 battery cells, then the minimum average balance efficiency is $\eta_{min} = \frac{3}{3.4} = 0.882$ [14].

2.2 Canonical Balancer Generalization

The 2-cell canonical balancer model can be generalized for higher-order balancing topologies. In our investigation, we will focus exclusively on balancing topologies that utilize the minimum number of required switches per cell (two). We place a heavy emphasis on this since the addition of more switches will typically bring more gate drivers along with them. Thus, designers have the freedom to choose the number of energy tanks to connect between the switching nodes (n of them) created by the $2n$ switches, where n is the number of cells to be balanced.

2.2.1 Multi-Tier Topology

There has been a tremendous amount of work done on enumerating SCC balancing topologies and characterizing their behavior [1, 7, 9, 30, 32, 33]. However, in the author's opinion, there is room for additional theoretical insight into the behavior of these topologies and exploration of interesting circuit structures that may be hidden in plain sight. A key insight from the aforementioned papers is the idea of adding charge paths to facilitate both direct and indirect energy transfer between cells. If one generalizes this idea to a particular set of SCC balancer topologies, then a Grand Canonical Balancer may be found for that topological family. We can apply this idea to the set of SCC battery balancer topologies with the minimum switch count.
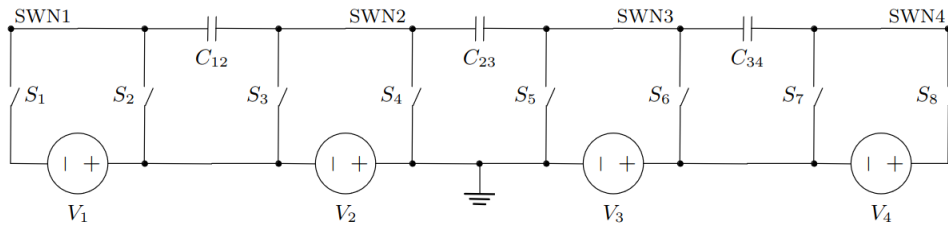
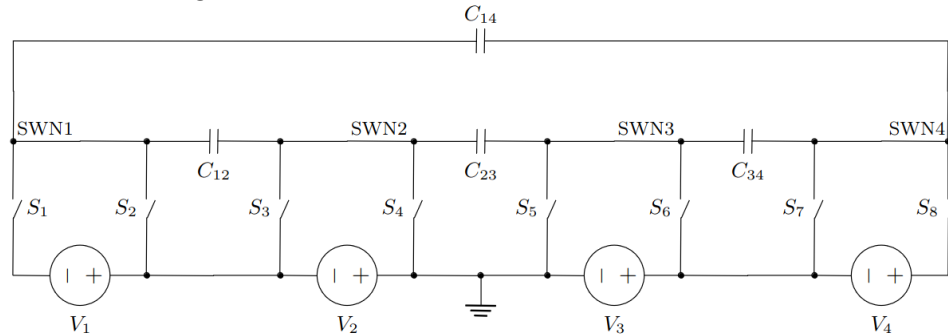Figure 2-10: Conventional or Flat 4S Balancer
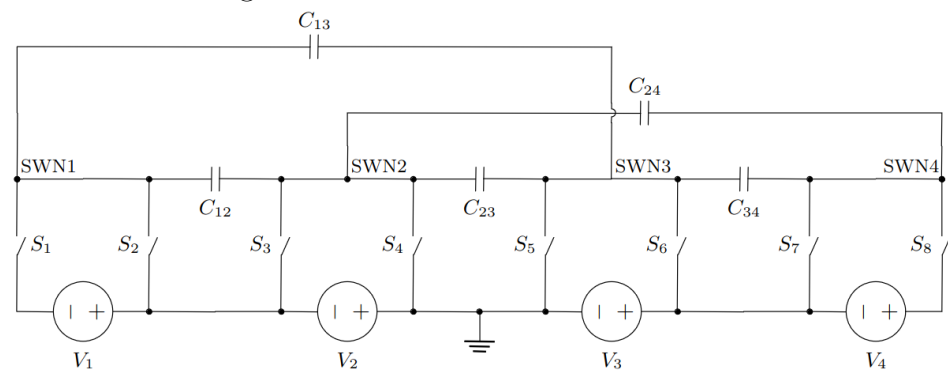

Figure 2-11: Double-Tier 1 4S Balancer

Figure 2-12: Double-Tier 2 4S Balancer
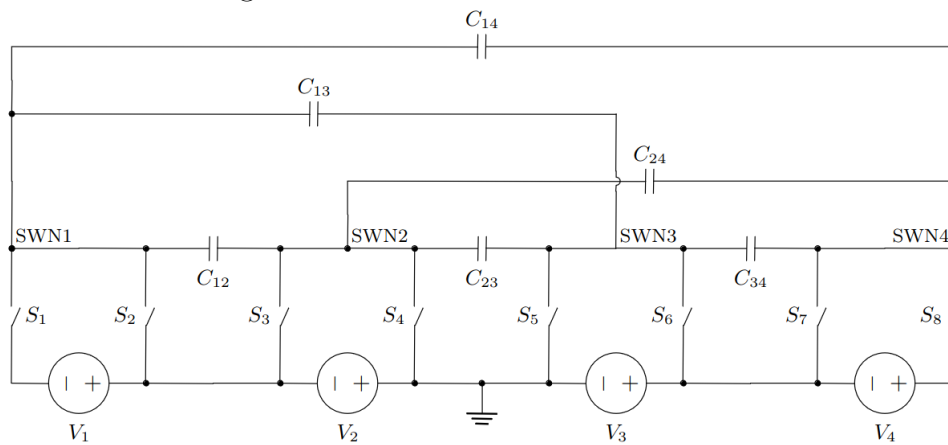
Figure 2-13: Multi-Tier 4S Balancer

Let us examine a few 4S implementations of circuits within this family. In Fig. 2-10, the Conventional or Flat topology within the minimum switch family is shown. To improve the balance time performance of this circuit, consider adding an additional capacitor between the furthest switching nodes. This yields a topology with an additional capacitor tier, that we will label: Double-Tier 1 (see Fig. 2-11). We can also consider adding two additional capacitors to the Flat topology by connecting them between every odd and even pair of switching nodes. We will refer to this topology as Double-Tier 2 (see Fig. 2-12).

Finally, we can extend the idea of facilitating charge paths to its limit and obtain the Multi-Tier topology (shown in Fig. 2-13). Observe that each switching node is connected to every other switching node via a capacitor. Thus, in the simplest terms, to construct the Multi-Tier balancer for any number of battery cells, connect each switching node to every other switching node via a capacitor (or more generally an appropriate energy tank). This is the Grand Canonical Balancer for the set of SCC balancers with the minimum number of switches and the maximum number of unique capacitors connecting pairs of switch nodes.

To the best of the author's knowledge, the Multi-Tier is a novel balancing topology that has been overlooked until now[2]. The number of capacitors required to construct this topology for arbitrary n is $\binom{n}{2} = \frac{n(n-1)}{2}$. This grows asymptotically as $\frac{n^2}{2}$, which is impractical as the number of battery cells grows. However, the topology may be advantageous for a low number of cells (probably $n \leq 9$). The author believes that the topology can primarily be used to study the set of SCC balancers with minimum switch count, as all other topologies in the family exist within the Multi-Tier. One can make certain resistances infinite to map the Multi-Tier structure to any other within the set. In the following sections, we explore some of this topology's behavior by analyzing its 3S and 4S average circuit models.

---

[2]However, it is important to note that the idea of connecting all switching node pairs together in switched-capacitor circuits is not new (see Fig. 11 in [29]).

2.2.2 3S Multi-Tier Analysis

The 3S Multi-Tier balancer is shown in Fig. 2-14 and its average circuit model in Fig. 2-15. To aid with the analysis, we will assume that all capacitances are equal i.e. $C_1 = C_2 = C_3 = C$, and the resistances scale such that $R_{12} = R$, $R_{23} = \beta R$, and $R_{13} = \alpha R$ where $\{\alpha, \beta \in \mathbb{R} \mid \alpha, \beta > 0\}$. The equations of motion for the 3S Multi-Tier balancer can be found in Appendix C.2.1. Solving these equations with this level of generality leads to a rather complicated set of analytical solutions, as shown in Eq. (2.15).

$$V_1(t) = \left\{ t \geq 0 : \frac{V_{batt}}{3} + \frac{1}{3}e^{-\sigma_3 t}\left(\cosh\left(\sigma_1 t\right) - \sigma_4 \sinh\left(\sigma_1 t\right)\right)\left(\Delta V_{1,2} + \Delta V_{1,3}\right)\right\}$$

where

$$
\begin{aligned}
\sigma_1 &= \frac{\sigma_2}{RC\alpha\beta} \\
\sigma_2 &= \sqrt{\alpha^2\beta^2 - \alpha^2\beta + \alpha^2 - \alpha\beta^2 - \alpha\beta + \beta^2} \\
\sigma_3 &= \frac{\alpha + \beta + \alpha\beta}{RC\alpha\beta} \\
\sigma_4 &= \frac{\alpha\beta\left(\Delta V_{1,2} - \Delta V_{2,3}\right) + \beta\left(\Delta V_{1,3} + \Delta V_{2,3}\right) - \alpha\left(\Delta V_{1,2} + \Delta V_{1,3}\right)}{\sigma_2\left(\Delta V_{1,2} + \Delta V_{1,3}\right)}
\end{aligned}
\tag{2.15}
$$

We can eliminate one of the free parameters by setting $\beta = 1$. This implies that all equivalent impedances at the lower (flat) level share the same value, which in practice should be approximately true. As a result, (2.15) simplifies to the following battery cell voltage equations

$$V_1(t) = \left\{ t \geq 0 : \frac{V_{batt}}{3} + \frac{\Delta V_{12} - \Delta V_{23}}{6}e^{\frac{-3t}{RC}} + \frac{\Delta V_{13}}{2}e^{\frac{-t}{RC}\left(1+\frac{2}{a}\right)}\right\} \tag{2.16}$$

$$V_2(t) = \left\{ t \geq 0 : \frac{V_{batt}}{3} - \frac{\Delta V_{12} - \Delta V_{23}}{3}e^{\frac{-3t}{RC}}\right\} \tag{2.17}$$

$$V_3(t) = \left\{ t \geq 0 : \frac{V_{batt}}{3} + \frac{\Delta V_{12} - \Delta V_{23}}{6}e^{\frac{-3t}{RC}} - \frac{\Delta V_{13}}{2}e^{\frac{-t}{RC}\left(1+\frac{2}{a}\right)}\right\} \tag{2.18}$$

The system has three poles at locations $\lambda_k = [0, -\frac{3}{RC}, -\frac{1+\frac{2}{\alpha}}{RC}]$. Using the method of
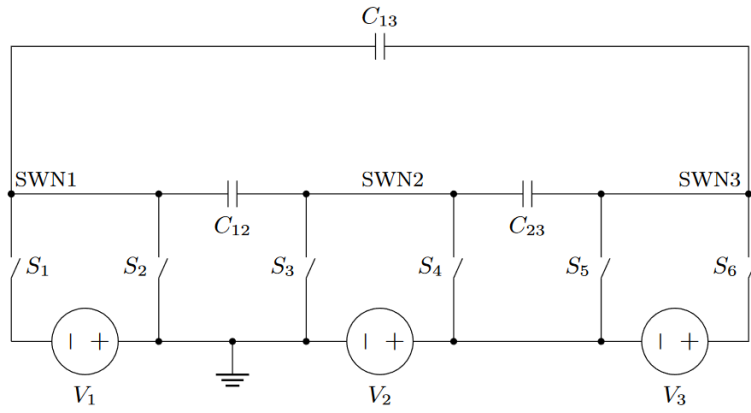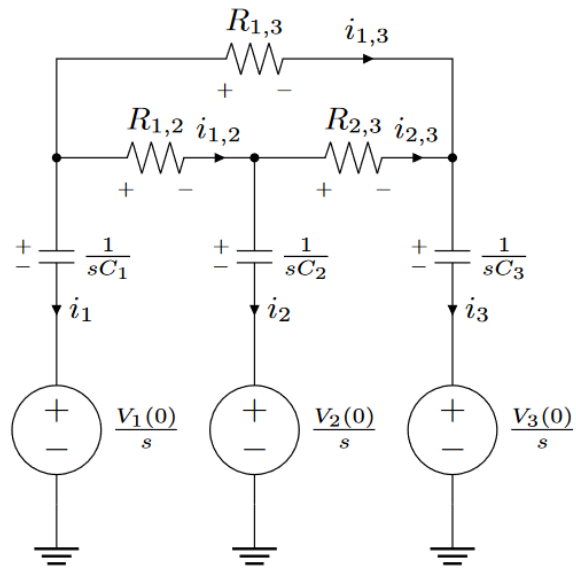
Figure 2-14: 3S Multi-Tier Balancer

Figure 2-15: Average Model for 3S Multi-Tier

37

dominant time constant, we can determine which of the non-zero poles will bottleneck the balance time [29]. The dominant time constant is expressed as λ_1 such that $0 > \lambda_1 \geq \ldots \geq \lambda_{n-1}$. Thus, the balance time can be approximated as

$$\tau_b \approx \max\left(\frac{RC}{3}\ln\left(\frac{\max\left(|\Delta V_{12}|, |\Delta V_{23}|\right)}{\Delta v_b}\right), \frac{RC}{1+\frac{2}{\alpha}}\ln\left(\frac{|\Delta V_{13}|}{\Delta v_b}\right)\right) \tag{2.19}$$

We can determine for what range of α does $-\frac{3}{RC}$ become the dominant time constant. If $-\frac{3}{RC} \geq -\frac{1+\frac{2}{\alpha}}{RC}$, then $\alpha \leq 1$. One might be quick to assume that the effect of the top-tier capacitor is negligible, however that is not necessarily true because $\lim\limits_{\alpha \to \infty} -\frac{1+\frac{2}{\alpha}}{RC} = -\frac{1}{RC} > -\frac{3}{RC}$. Therefore, while having $\alpha > 1$ causes its respective pole to be the dominant pole, the associated time constant is still lower than if α were infinite. Observe that when $-\frac{1}{RC} \geq -\frac{1+\frac{2}{\alpha}}{RC}$ implies that $\alpha \leq \alpha + 2$, which is true for all practical values of α. This can also be shown by taking the ratio of the balance time for $\alpha \geq 1$ over the balance time for the case where $\alpha \to \infty$:

$$\frac{\tau_{b,\alpha}}{\tau_{b,flat}} = \frac{1}{1+\frac{2}{\alpha}} \tag{2.20}$$

Note that at $\alpha = 2$, the balance time is half of what it would be without the top-tier capacitor.

2.2.3 4S Multi-Tier Analysis

The 4S Multi-Tier balancer is shown in Fig. 2-16 and its average circuit model in Fig. 2-17. To aid with the analysis, we assume that $C_1 = C_2 = C_3 = C_4 = C$, $R_{12} = R_{23} = R_{34} = R$, $R_{13} = R_{24} = \alpha R$, and $R_{14} = \phi R$ such that $\{\alpha, \phi \in \mathbb{R} \mid \alpha, \phi > 0\}$. The equations of motion can be found in Appendix C.2.2. Solving these equations with this level of generality leads to a rather complicated set of analytical solutions, as such we will analyze two sets of solutions by setting one of the free parameters to unity and letting the other vary.

We first consider the case where $\phi = 1$ and α is allowed to vary, such as in a design where much emphasis is placed on matching the lower and higher-tier equivalent
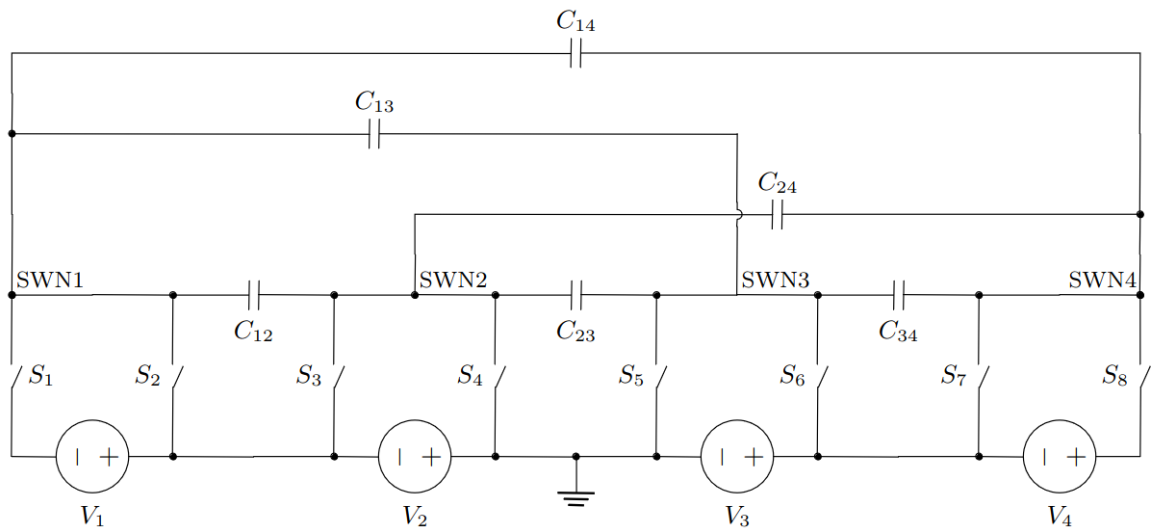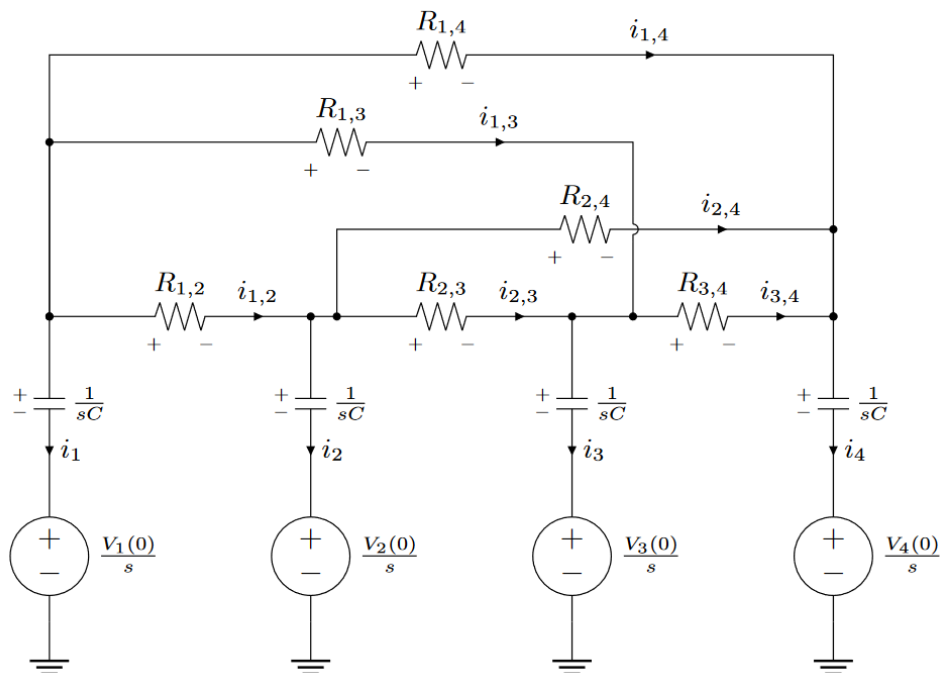
Figure 2-16: 4S Multi-Tier Balancer

Figure 2-17: Average Model for 4S Multi-Tier

impedances while allowing flexibility at the middle-tier. As a result, solutions are much neater and understandable. The battery cell voltages can be expressed as

$$V_{1,\alpha}(t) = \left\{ t \geq 0 : \frac{V_{batt}}{4} + \frac{\Delta V_{14} - \Delta V_{23}}{4} e^{\frac{-4t}{RC}} + \frac{\Delta V_{13}}{2} e^{\frac{-t}{RC}\left(2 + \frac{2}{a}\right)} \right\} \qquad (2.21)$$

$$V_{2,\alpha}(t) = \left\{ t \geq 0 : \frac{V_{batt}}{4} - \frac{\Delta V_{12} + \Delta V_{34}}{4} e^{\frac{-4t}{RC}} + \frac{\Delta V_{24}}{2} e^{\frac{-t}{RC}\left(2 + \frac{2}{a}\right)} \right\} \qquad (2.22)$$

$$V_{3,\alpha}(t) = \left\{ t \geq 0 : \frac{V_{batt}}{4} + \frac{\Delta V_{12} + \Delta V_{34}}{4} e^{\frac{-4t}{RC}} - \frac{\Delta V_{13}}{2} e^{\frac{-t}{RC}\left(2 + \frac{2}{a}\right)} \right\} \qquad (2.23)$$

$$V_{4,\alpha}(t) = \left\{ t \geq 0 : \frac{V_{batt}}{4} - \frac{\Delta V_{14} - \Delta V_{23}}{4} e^{\frac{-4t}{RC}} - \frac{\Delta V_{24}}{2} e^{\frac{-t}{RC}\left(2 + \frac{2}{a}\right)} \right\} \qquad (2.24)$$

The system has three poles at locations $\lambda_k = [0, -\frac{4}{RC}, -\frac{2+\frac{2}{\alpha}}{RC}]$. It is important to note that more poles are possible in the general case with two free resistor parameters. As before, we may utilize the method of dominant time constant to determine the balance time

$$\tau_b \approx \max \left(\frac{RC}{4} \ln \left(\frac{\max\left(|\Delta V_{12}|, |\Delta V_{14}|, |\Delta V_{23}|, |\Delta V_{34}|\right)}{\Delta v_b} \right), \frac{RC}{2+\frac{2}{\alpha}} \ln \left(\frac{\max(|\Delta V_{13}|, |\Delta V_{24}|)}{\Delta v_b} \right) \right) \quad (2.25)$$

We can also assess the effect of variations in α by taking the ratio of the balance time for $\alpha \geq 1$ over the balance time for the case where $\alpha \to \infty$

$$\frac{\tau_{b,\alpha}}{\tau_{b,\alpha \to \infty}} = \frac{1}{1 + \frac{1}{\alpha}} \qquad (2.26)$$

Note that at $\alpha = 2$, the balance time is two-thirds of what it would be without the middle-tier equivalent impedances. The reduction in balance time is less than that of Eq. (2.20) for a given α. This is likely due to the top-tier capacitor's ability to provide an alternative charge path to that of the middle-tier capacitors.

Now we will consider the case where $\alpha = 1$ and ϕ is allowed to vary, for example in a design where significant emphasis is placed on matching the lower and middle-tier equivalent impedances while allowing flexibility at the high-tier. These solutions are

also clean and simple. The battery cell voltages can be expressed as

$$V_{1,\phi}(t) = \left\{ t \geq 0 : \frac{V_{batt}}{4} + \frac{\Delta V_{12} - \Delta V_{34}}{4} e^{\frac{-4t}{RC}} + \frac{\Delta V_{14}}{2} e^{\frac{-t}{RC}\left(2+\frac{2}{\phi}\right)} \right\} \tag{2.27}$$

$$V_{2,\phi}(t) = \left\{ t \geq 0 : \frac{V_{batt}}{4} - \frac{\Delta V_{12} - \Delta V_{23} - \Delta V_{24}}{4} e^{\frac{-4t}{RC}} \right\} \tag{2.28}$$

$$V_{3,\phi}(t) = \left\{ t \geq 0 : \frac{V_{batt}}{4} - \frac{\Delta V_{13} + \Delta V_{23} - \Delta V_{34}}{4} e^{\frac{-4t}{RC}} \right\} \tag{2.29}$$

$$V_{4,\phi}(t) = \left\{ t \geq 0 : \frac{V_{batt}}{4} + \frac{\Delta V_{13} - \Delta V_{24}}{4} e^{\frac{-4t}{RC}} - \frac{\Delta V_{14}}{2} e^{\frac{-t}{RC}\left(2+\frac{2}{\phi}\right)} \right\} \tag{2.30}$$

The system has three poles at locations $\lambda_k = [0, -\frac{4}{RC}, -\frac{2+\frac{2}{\phi}}{RC}]$. As before, we may utilize the method of dominant time constant to determine the balance time

$$\tau_b \approx \max\left(\frac{RC}{4} \ln\left(\frac{\max\left(|\Delta V_{12}|, |\Delta V_{13}|, |\Delta V_{23}|, |\Delta V_{24}|, |\Delta V_{34}|\right)}{\Delta v_b} \right), \frac{RC}{2+\frac{2}{\phi}} \ln\left(\frac{|\Delta V_{14}|}{\Delta v_b} \right) \right) \tag{2.31}$$

We can also assess the effect of variations in ϕ by taking the ratio of the balance time for $\phi \geq 1$ over the balance time for the case where $\phi \to \infty$

$$\frac{\tau_{b,\phi}}{\tau_{b,\phi\to\infty}} = \frac{1}{1 + \frac{1}{\phi}} \tag{2.32}$$

Note that this result is identical to that of Eq. (2.26), except now in terms of ϕ. This is likely due to the middle-tier capacitors' ability to provide an alternative charge path to that of the higher-tier capacitor.

2.2.4 NS Multi-Tier Analysis

From these results, we can predict what may happen in the general case of an NS Multi-Tier balancer. We can represent the solution of an arbitrary cell voltage V_k as

$$V_k(t) = \left\{ t \geq 0 : \frac{V_{batt}}{N} + \sum_{m=1}^{N-1} \alpha_{mk} e^{\lambda_m t} \right\} \text{ where}$$

$$\alpha_{mk} = f\left(R_{12}, R_{13}, \ldots, R_{ij}, C, \Delta V_{12}, \Delta V_{13}, \ldots, \Delta V_{ij}\right) \text{ for } i < j \qquad (2.33)$$

$$\lambda_m = m^{\text{th}} \text{ non-zero eigenvalue or pole of system}$$

In general, the most challenging portions of the solution to obtain are the poles λ_m and coefficients α_{mk}. These can and will be very complicated functions of the circuit resistances, capacitances, and initial conditions [29]. Although this may seem daunting, for considerations of balance time, one needs to just find the dominant pole. There are various matrix algorithms to accomplish this task, but it may also be possible to find an elegant analytical solution utilizing the approaches in [6, 17, 18, 19]. The maximum possible balance time for an NS Multi-Tier balancer can be

$$\tau_b \approx \frac{1}{\max(\lambda_1, \lambda_2, \ldots, \lambda_{N-1})} \ln\left(\frac{\Delta v_b}{\max\left(|\Delta V_{12}|, |\Delta V_{13}|, \ldots, |\Delta V_{mn}|\right)}\right) \qquad (2.34)$$

Chapter 3

Comparing Switched Capacitor Balancing Topologies

We present and compare four different SCC battery balancing topologies. Average circuit models for each are shown at the 4S level. We also compare their balance time performances through simulation.

3.1   Topologies

We compare the balance time, component selection, and capacitor stress of the Flat, Double-Tier, and Multi-Tier topologies (these topologies are initially introduced in Section 2.2.1). Table 3.1 compares the component selection and capacitor stress of these topologies. Fig. 3-1, 3-2, 3-3, and 3-4 depict their equivalent circuit models.

Topology	Number of Capacitors	Number of Switches	Capacitor Stress
Flat SC	$n-1$	$2n$	$V_{cell,max}$
Double-tier SC 1	n	$2n$	$(n-1)V_{cell,max}$
Double-tier SC 2	$2n-3$	$2n$	$2V_{cell,max}$
Multi-tier SC	$\frac{n^2-n}{2}$	$2n$	$(n-1)V_{cell,max}$

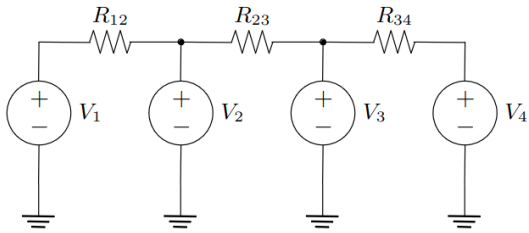Table 3.1: Comparison on Capacitor Number, Switch Number, and Capacitor Stress

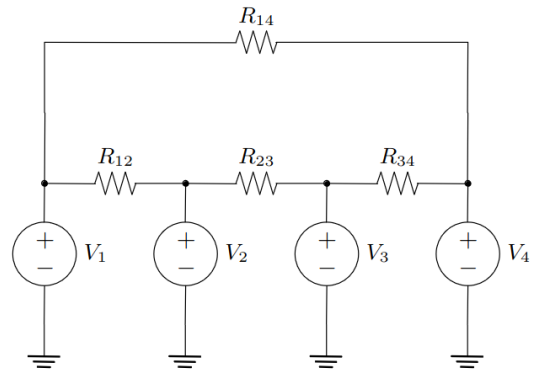Figure 3-1: 4S Flat Average Model

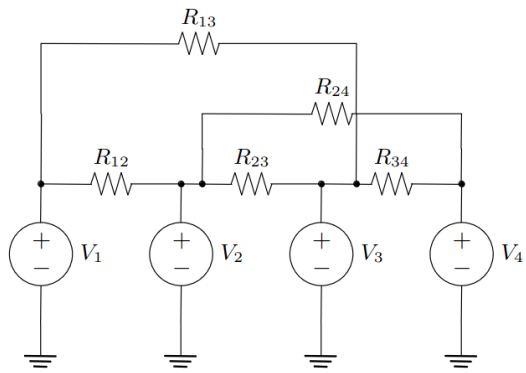Figure 3-2: 4S Double-Tier 1 Average Model
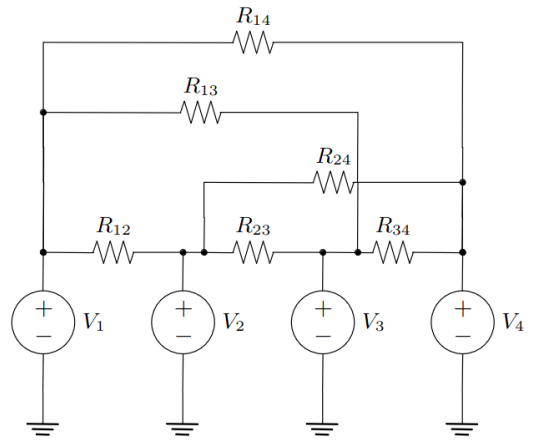

Figure 3-3: 4S Double-Tier 2 Average Model

Figure 3-4: 4S Multi-Tier Average Model

3.2 Balance Speed Comparison

We define the balance time (τ_b) as the time it takes for the maximum difference between cell voltages to be smaller than 10 mV. We simulate five different SPICE simulations, each with varying initial condition, for the average model for each topology. The simulation parameters are listed in Table 3.2 and the initial conditions (ICs) are shown in Table 3.3. Table 3.4 presents the resulting balance times for all initial conditions and shows that the Multi-Tier topology performs most consistently across these initial conditions. We highlight the cell voltage waveforms for initial condition 5 in Fig. 3-5, 3-6, 3-7, and 3-8. These curves validate the addition of higher-tier capacitors across switching nodes to significantly improve the balance time. Table 3.5 presents the average balance time for each SCC balancer topology over all ICs .

Parameter	Value
Battery cell capacitance [kF]	9
R_{12}, R_{23}, R_{34} [mΩ]	100
R_{13}, R_{24} [mΩ]	150
R_{14} [mΩ]	200

Table 3.2: Balance Time Comparison Simulation Parameters

Initial Condition Number	V_1 [V]	V_2 [V]	V_3 [V]	V_4 [V]
(1)	3	3.4	3	3.4
(2)	3	3	3.4	3.4
(3)	3	3.2	3.2	3.4
(4)	3	3.1	3.3	3.4
(5)	3	3.3	3.1	3.4

Table 3.3: Battery Cell Voltages for Different Initial Conditions

Topology	Balance Time for IC1 [min]	Balance Time for IC2 [min]	Balance Time for IC3 [min]	Balance Time for IC4 [min]	Balance Time for IC5 [min]
Multi-Tier	19.818	23.143	21.771	22.747	20.631
Flat	77.435	100.593	91.525	96.431	85.108
Double-Tier 1	26.816	42.627	37.558	40.302	33.489
Double-Tier 2	33.210	36.256	35.001	35.698	33.978

Table 3.4: Comparison of Balance Times for Different Initial Conditions (ICs)
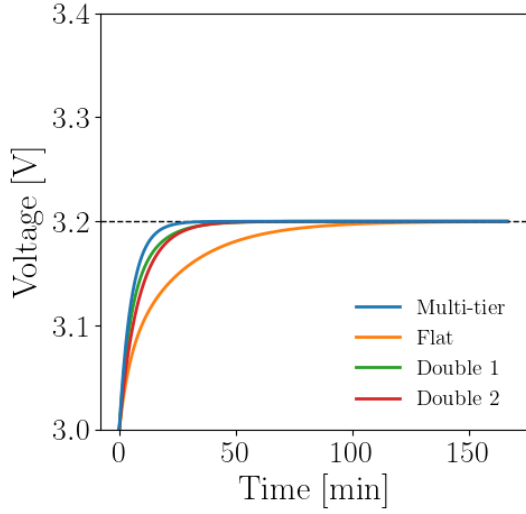
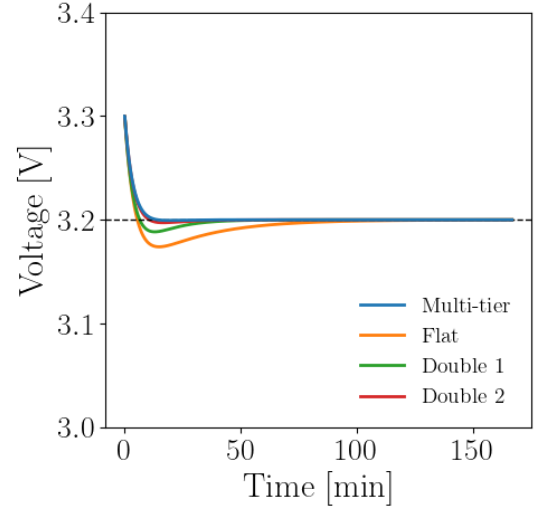Figure 3-5: V_1 Simulated Waveform for Initial Condition 5

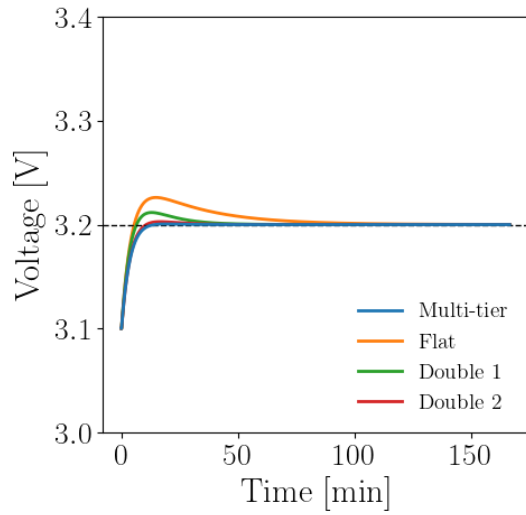Figure 3-6: V_2 Simulated Waveform for Initial Condition 5

Figure 3-7: V_3 Simulated Waveform for Initial Condition 5

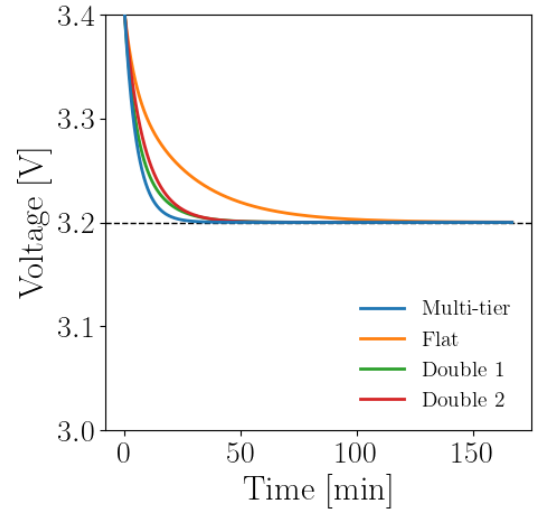Figure 3-8: V_4 Simulated Waveform for Initial Condition 5

Topology	Average Balance Time [min]
Multi-Tier	21
Flat	90
Double-Tier 1	36
Double-Tier 2	34

Table 3.5: Battery Cell Voltages for Different Initial Conditions

Chapter 4

Implementation of SCC Balancer

We design and validate three practical SCC balancers on printed circuit boards (PCBs). Two of these are 2S balancers, one utilizes only N-channel (NCH) switches while the other uses a combination of NCH and P-channel (PCH). Building upon these designs, a 4S NCH+PCH balancer is developed and tested. The 4S balancer is a practical implementation of the new Multi-Tier topology from Chapters 2 and 3. Component selection, schematics, and PCB layout are provided for each design. We perform frequency sweeps, battery cell voltage differential sweeps, and dynamic balance experiments. All tests are performed at 50% duty cycle. Table A.4 lists the lab equipment utilized for testing. Battery cell emulation parameters can be found in Table A.5.

4.1   2S NCH Design

The schematic for the 2S NCH design is in Fig. B-4. We utilize a resonant SCC 2S balancer [8, 12]. An LTSpice simulation of the circuit is created to verify the design before PCB layout (see Fig. B-1). Top and bottom 3D views of the PCB layout are shown in Fig. B-7 and B-8. The populated PCB is shown in Fig. B-9 and B-10. A complete component list can be found in Table A.1.

4.1.1 LC Tank

The LC tank is comprised of 10x22 μF parallel ceramic capacitors in series with a 100 nH inductor, yielding a nominal resonant frequency of 34 kHz. Including many capacitors in parallel helps reduce ESR and mitigate DC bias effects. GMK325BJ226MM-P is the chosen capacitor component with a voltage rating of 35 V. We choose the inductor based on the guidelines provided in [34], which suggests choosing an L with a DC resistance on the order of the switch resistance. Thus, we choose PA5189.101HLT as the inductor component with $R_{DC} = 0.39$ mΩ (around half the NCH switch resistance). Its inductance value is also selected to keep the resonant frequency somewhere between 30-100 kHz. The LC tank needs to operate near this frequency band to minimize switching loss and capacitor ESR.

4.1.2 Input Bypass Capacitors

As described in [10], input bypass capacitors are required to mitigate poor battery cell current waveforms, in the form of impulses. The addition of bypass capacitors smooths the cell current waveforms by attenuating its AC component. The larger the bypass capacitors, the more the cell current resembles that of a buck converter output: triangular with small AC ripple and minimal high frequency content. This also reduces the associated RMS current loss across the cells, assuming that $Z_{bypass} \leq \alpha Z_{cell}$, where $\{\alpha \in \mathbb{R} \mid 0 < \alpha < 10\}$. Additionally, if Z_{input}[1] $\gtrapprox R_{eq} - Z_{input}$, then the average cell current will notably increase by including the bypass capacitor (see Fig. 4-1).

A practical way of achieving high capacitance and low resistance across the cell terminals is following an approach similar to the flying capacitors, utilizing several capacitors in parallel. Our design uses a 0603 0.1 μF, 0805 1 μF, and 1210 10 μF ceramic capacitors in parallel for general noise rejection in addition to 1210 3x22 μF parallel ceramic capacitors for larger bulk capacitance. One should also be aware that most of the current will flow through the larger capacitors via capacitor charge

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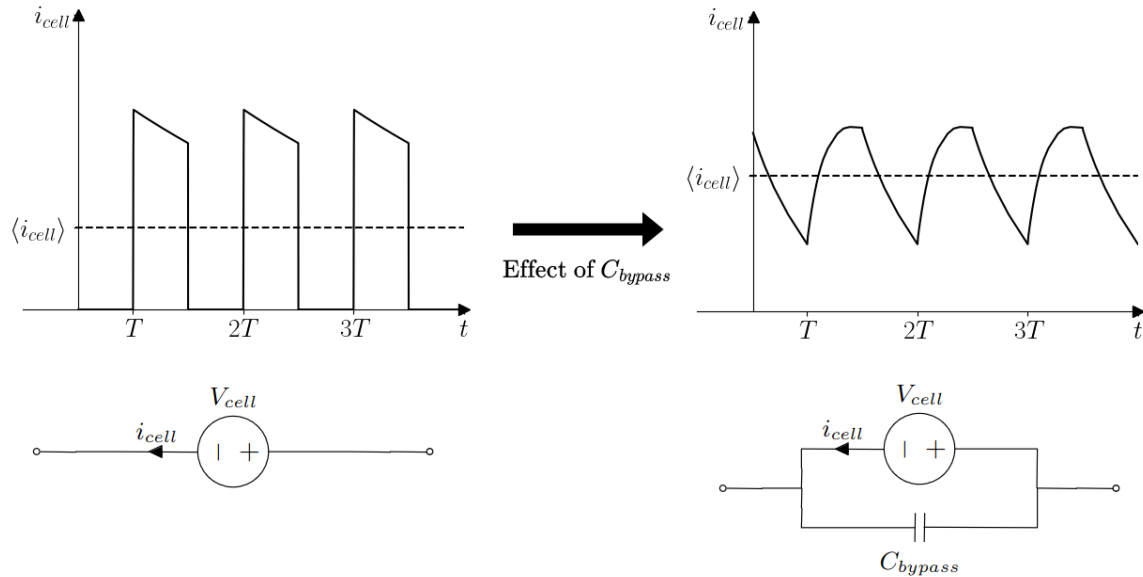[1]$Z_{input} = Z_{cell} \parallel Z_{bypass}$

Figure 4-1: Effect of Bypass Capacitors on Cell Current

sharing. The voltage rating of these components should be at least twice the cell voltage to have a comfortable safety margin. This design uses 6.3 V rated capacitors.

4.1.3 Switches and Bootstrap

The NCH switches are chosen such that their threshold voltages could be reached within a 2S battey voltage swing while minimizing $R_{DS,on}$. Our design utilizes the Infineon IAUC120N04S6L008ATMA1 with $R_{DS,on}$ of 0.8 mΩ and a $V_{GS,th}$ of 2 V. These switches are capable of blocking up to 40 V (well above anything produced in the circuit) and handling 120 A at room temperature. We choose gate resistors with resistance value 10 Ω to help with noise and ringing in the gate drive path. The resistor is also specified such that its power rating was sufficient to handle the average power loss as the gate driver pushes current through it. Furthermore, a turn-off diode in parallel with the resistor is necessary to have the switches reach their off-state as quickly as possible to mitigate shoot-through and switching loss. We use a Schottky diode (CUS10S30,H3F) for its low forward-biased voltage (V_D) that can also handle the gate driver's peak sinking current. A bootstrap circuit is needed for this implementation because the circuit is powered completely off the cell voltages.

We design a quasi-synchronous bootstrap to generate nearly identical V_{GS} signals for each switch (see Fig. 4-2). The bootstrap circuit is essentially another SCC that connects a bootstrap capacitor to the entire battery in state 1, and then connects the capacitor to the gate driver power rails in state 2. The main advantage of this circuit is that it avoids adding extra components by utilizing the switches that are already in the power circuit. However, this bootstrap does add to the switch stress since the existing switches have to perform more functions. This issue can be mitigated with appropriately rated components. Additionally, we use low-power PCH devices to provide quasi-synchronous bootstrap that can run off the same gate signals as the NCH devices in the power circuit. One of the diodes (D7 in Fig. B-4) cannot be easily replaced with a PCH switch since the existing gate signals are not compatible with it and can cause shoot-through. Similar to the NCH devices, the PCH gates are equipped with 10 Ω gate resistors and Schottky diodes in parallel for quick turn-off[2].
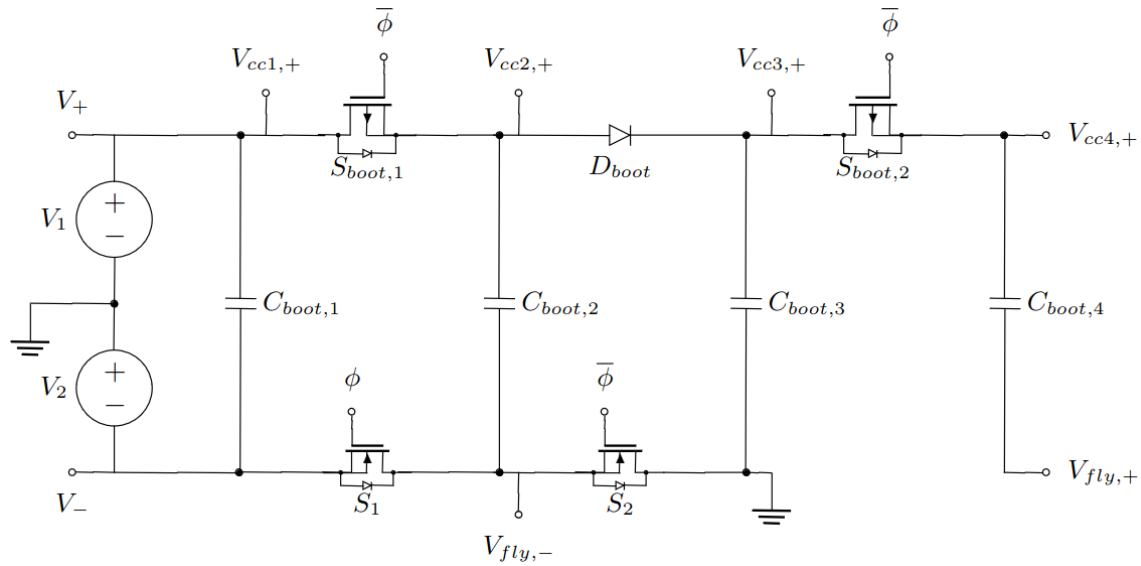

Figure 4-2: Bootstrap Circuit for 2S NCH Balancer

[2]For quick PCH turn-off, the turn-off diode must point towards the gate (opposite to that of the NCH switch).

4.1.4 Gate Drive

As shown in the power circuit on Fig. B-4, the majority of sources on the NCH switches are referenced to non-zero voltages or switching nodes. Thus, we decide to use opto-isolated gate drivers (IS480P). Four gate drivers are required in the 2S NCH design due to the nature of controlling four NCH switches (later we reduce the number of gate drivers by utilizing CMOS technology). Although the circuit can be operated using an on-board square wave generator, as is the case in v1.0.0 of the design (refer to the op-amp multivibrator in Fig. B-1), in the final revision (v1.1.0), we use an off-board square wave generator (Juntek JDS-2900-60M) to streamline the experimental testing and PCB population.

To prevent shoot-through from occurring between the NCH devices, a dead-time circuit is designed using an op-amp integrator topology. The input to the integrator is a square wave. The output is a clipped triangle wave with a much smaller slope between the waveform's transition points than that of the input square wave. The output is then fed into two pairs of anti-parallel gate driver inputs. Dead-time occurs and therefore no switches conduct when the clipped triangle waveform's voltage is between $\pm V_D$, where V_D is the forward voltage of the gate driver input diode.

4.1.5 Testing

In the experimental testing, the resonant frequency is 53 kHz with a maximum average balance current of 4.9 A, as shown in Fig. 4-3. A plot of the equivalent impedance is also shown in Fig. 4-4. The measured minimum impedance is 81.7 mΩ. We define the balance time ($\tau_{b,meas}$) to be the time when the difference between cell voltages is constrained such that $\Delta V < 10$ mV. This 2S NCH design achieves $\tau_{b,meas} = 25.2$ min (see Fig. 4-5). The battery cell emulation parameters can be found in Table A.5. One cell is initialized to 3.4 V (100% SOC) and the other to 3 V (0% SOC).

We determine that the bypass capacitors are the main resistive bottleneck for this practical implementation by running a high cell differential thermal test (nearly identical to Fig. B-30). The quasi-synchronous bootstrap also operates as intended as

shown in Fig. B-24. Each channel shows the V_{GS} waveform for each of the switches. Note that the their amplitudes are nearly identical.
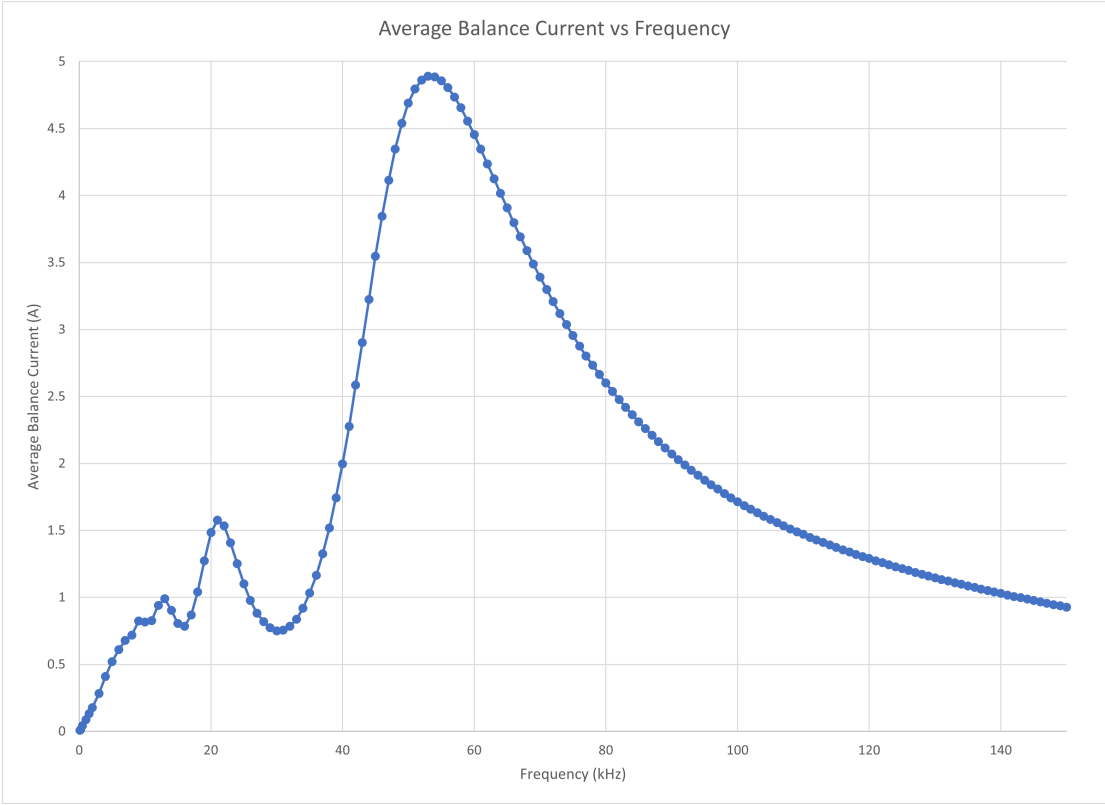
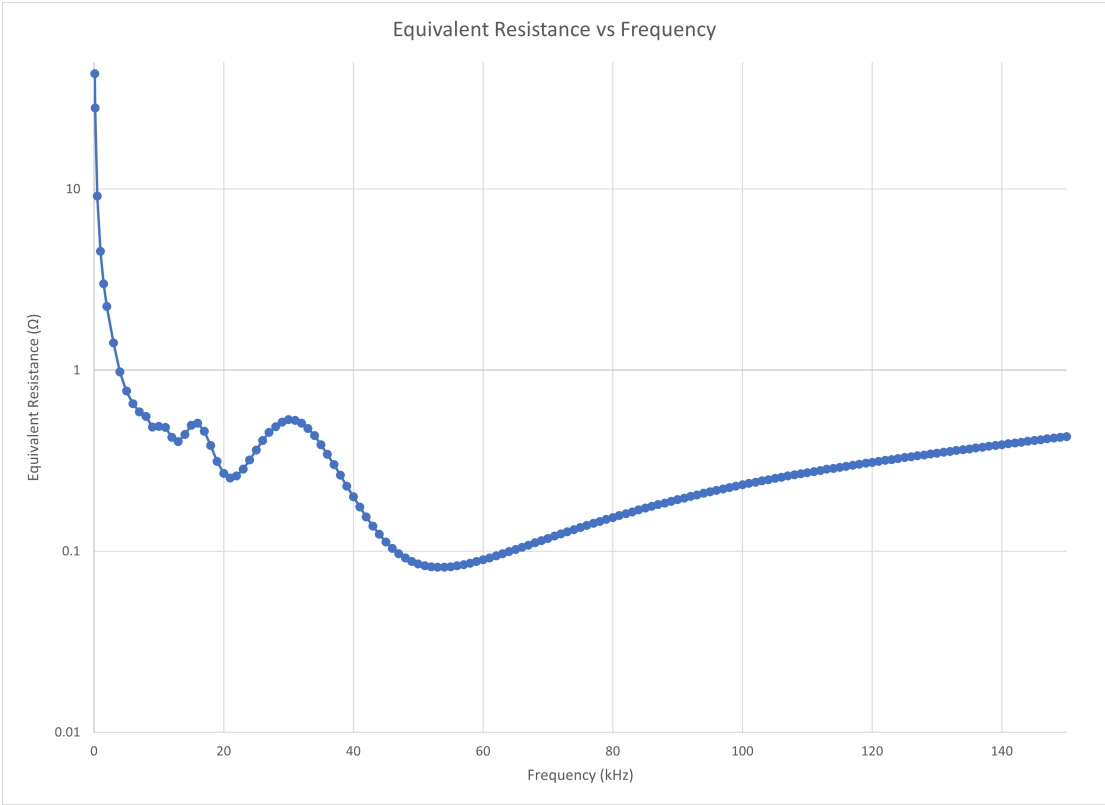Figure 4-3: 2S NCH Average Balance Current vs Frequency
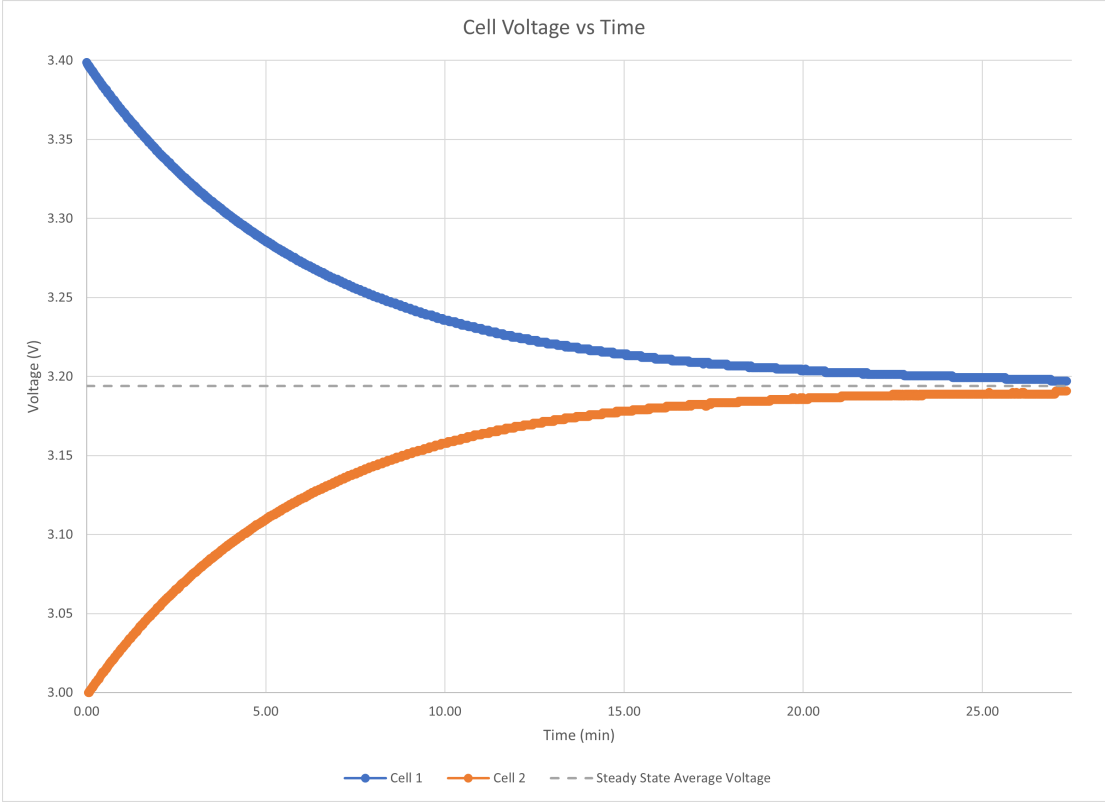

Figure 4-4: 2S NCH R_{eq}

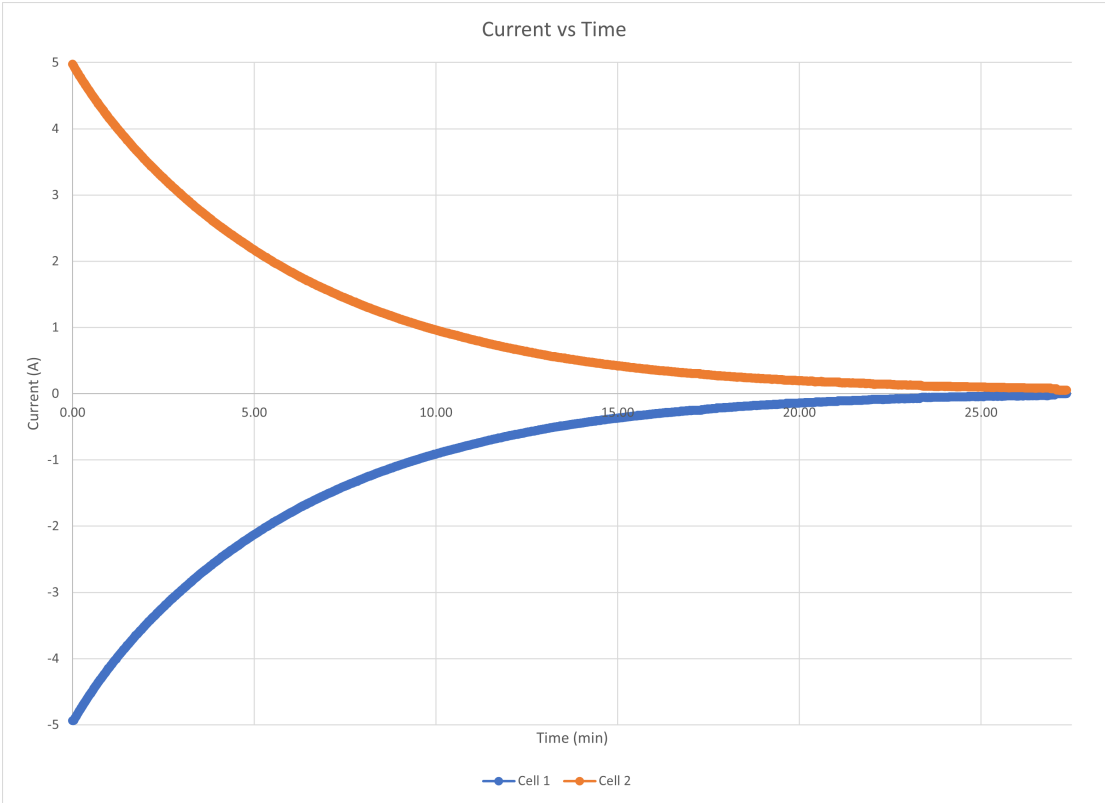Figure 4-5: 2S NCH Dynamic Cell Voltages

Figure 4-6: 2S NCH Dynamic Cell Currents

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4.2   2S NCH+PCH Design

While PCH devices have limited use in the power electronics community, they can be more advantageous than NCH technology in some designs [10, 20, 21]. The schematic for the 2S NCH+PCH design is in Fig. B-5. We utilize a resonant SCC 2S balancer. To verify the design before PCB layout, we simulate the circuit in LTSpice (see Fig. B-2). Fig. B-11 and B-12 show the top and bottom 3D views of the PCB layout. The populated PCB is displayed in Fig. B-13 and B-14. Table A.2 presents a complete component list for this design.

4.2.1   LC Tank

Same component selection and reasoning as Section 4.1.1.

4.2.2   Input Bypass Capacitors

Same component selection and reasoning as Section 4.1.2.

4.2.3   Switches and Bootstrap

The NCH and PCH switches are selected such that they reach their threshold voltages within a 2S battery voltage swing while minimizing $R_{DS,on}$. This design uses the Nexperia PH2925U,115 for the NCH switches with an $R_{DS,on}$ of 3 mΩ and a $V_{GS,th}$ of 1 V. We also use the Vishay Siliconix SQJ123ELP-T1_GE3 for the PCH switches with an $R_{DS,on}$ of 4 mΩ and a $V_{GS,th}$ of 1.5 V. Both of these switches are capable of blocking the highest voltages produced in this circuit. We also include gate resistors for both NCH and PCH switches (with sufficient power ratings) to reduce the noise and ringing in the gate drive path. The gate resistance for the NCH and PCH switches are 10 Ω and 1 Ω respectively. Furthermore, we connect a turn-off Schottky diode (CUS10S30,H3F) diode in parallel with each gate resistor to have the switches transition to their off-state as quickly as possible to mitigate shoot-through and switching loss.

We also design a bootstrap to generate about the same V_{GS} signals for each switch (see Fig. 4-7). The bootstrap circuit works by connecting a bootstrap capacitor in parallel to battery cell 1 in state 1, which charges the capacitor to roughly the cell voltage. Then, another capacitor is connected in parallel to battery cell 1 in state 2, which also charges this second capacitor to roughly the cell voltage. These capacitors are connected in series between the gate driver power rails. This provides $V_{cc} \approx V_{batt}$. The circuit is repeated for battery cell 2.
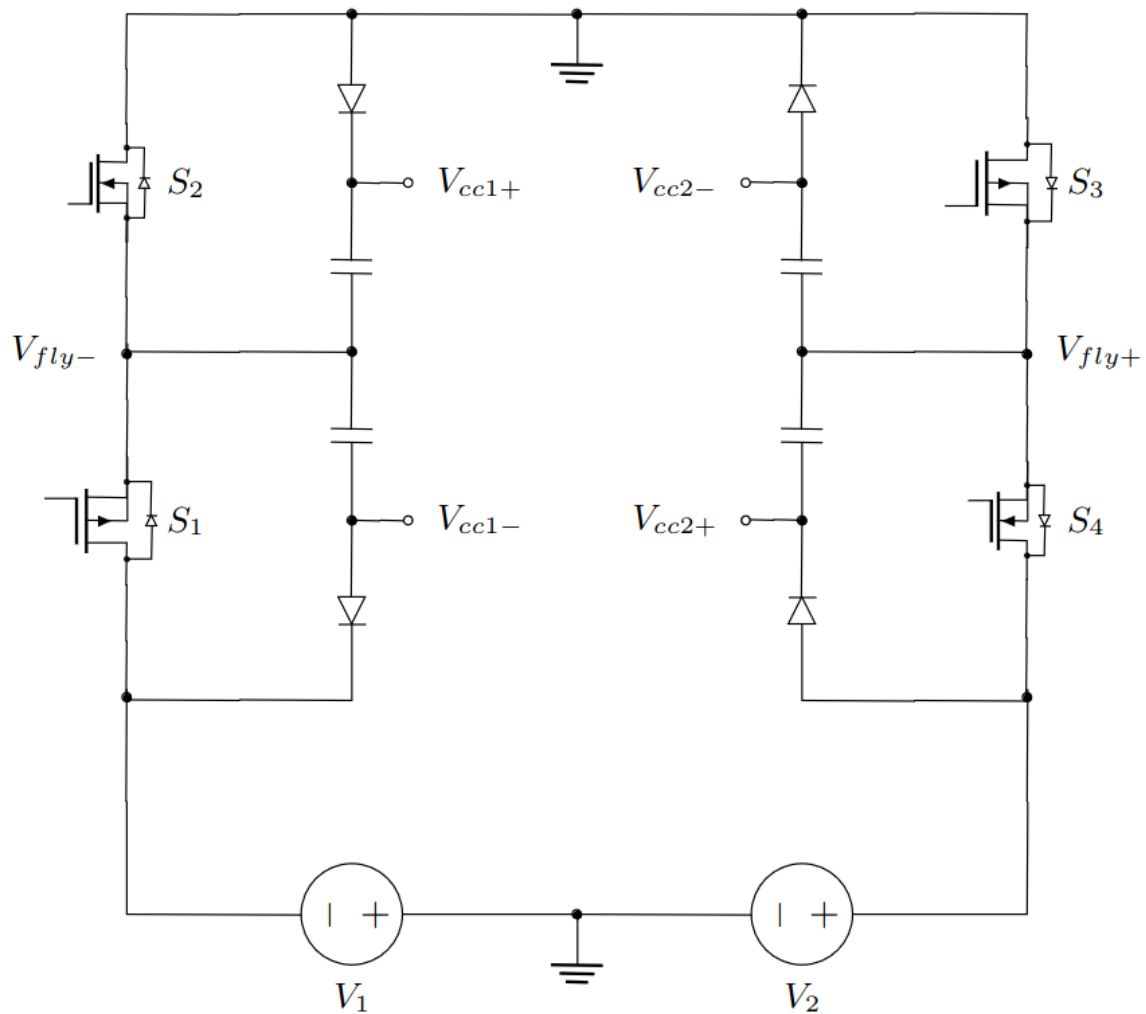
Figure 4-7: Bootstrap Circuit for 2S NCH+PCH Balancer

4.2.4 Gate Drive

As shown in the power circuit on Fig. B-5, the NCH and PCH sources are referenced to switching nodes. Thus, we decide to use opto-isolated gate drivers (IS480P). Two gate drivers are required in this design due to the nature of controlling two CMOS switch pairs. The circuit can similarly operate with an on-board square wave generator, as is the case in v1.0.0 of the design (refer to the op-amp multivibrator in Fig. B-2), but for the final revision in v1.1.0, we use an off-board square wave generator to streamline the experimental testing and PCB population.

4.2.5 Testing

In our experimental testing, the resonant frequency is 57 kHz with a maximum average balance current of 4.24 A, as shown in Fig. 4-8. Fig. 4-9 presents a plot of the equivalent impedance. The measured minimum impedance is 94.4 mΩ. The difference between this impedance and that of the NCH design is due to the increase in switch resistance: $\Delta R_{eq} = R_{eq,2} - R_{eq,1} = \Delta R_{SW} \approx 12$ mΩ. Similarly, the bypass capacitors are the main resistive bottleneck for this practical implementation, determined through a high cell differential thermal test, as shown in Fig. B-30.

Using the same definition for the balance time ($\tau_{b,meas}$) defined in Section 4.1.5, this NCH+PCH design achieves a $\tau_{b,meas} = 31.4$ min (see Fig. 4-10). The battery cell emulation parameters can once again be found in Table A.5. One cell is also initialized to 3.4 V (100% SOC) and the other to 3 V (0% SOC).
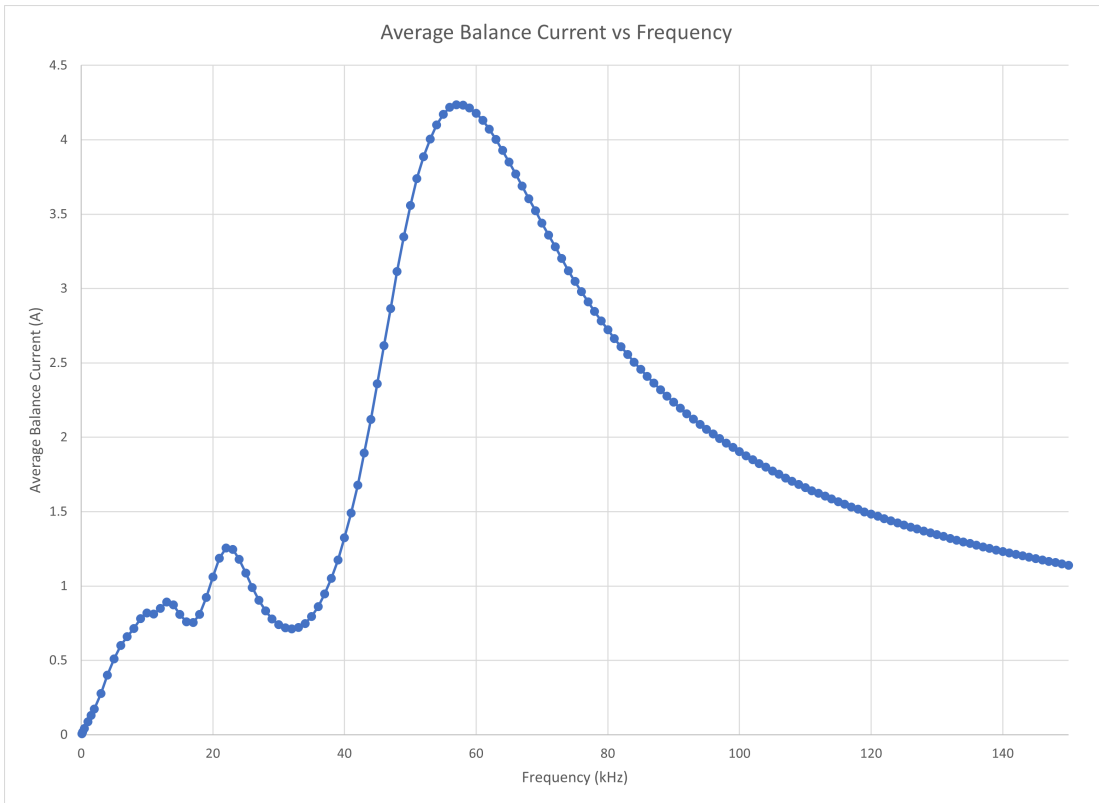
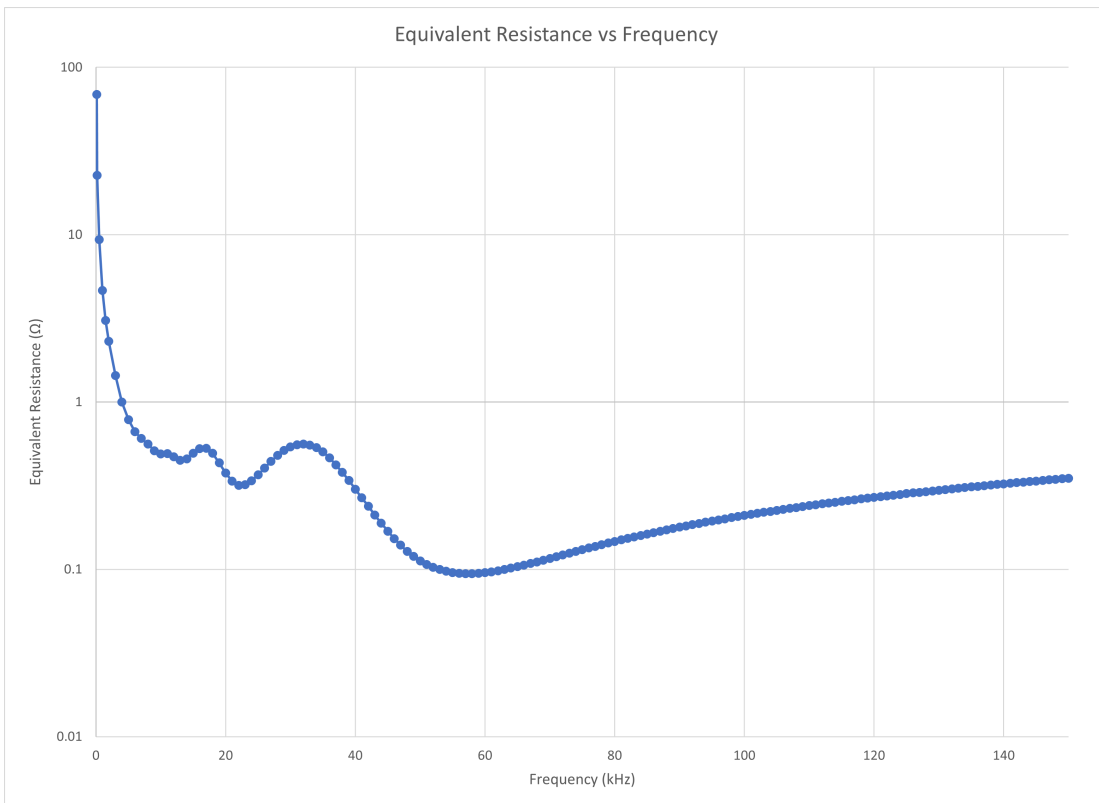Figure 4-8: 2S NCH+PCH Average Balance Current vs Frequency
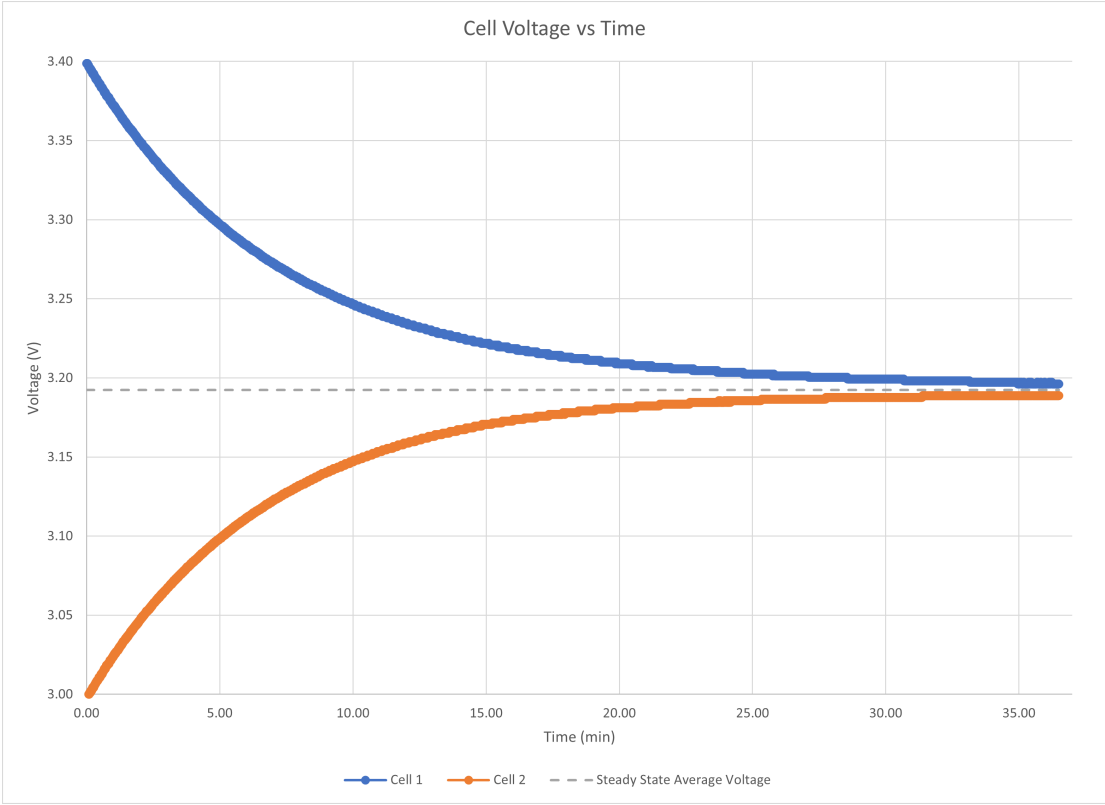

Figure 4-9: 2S NCH+PCH R_{eq}
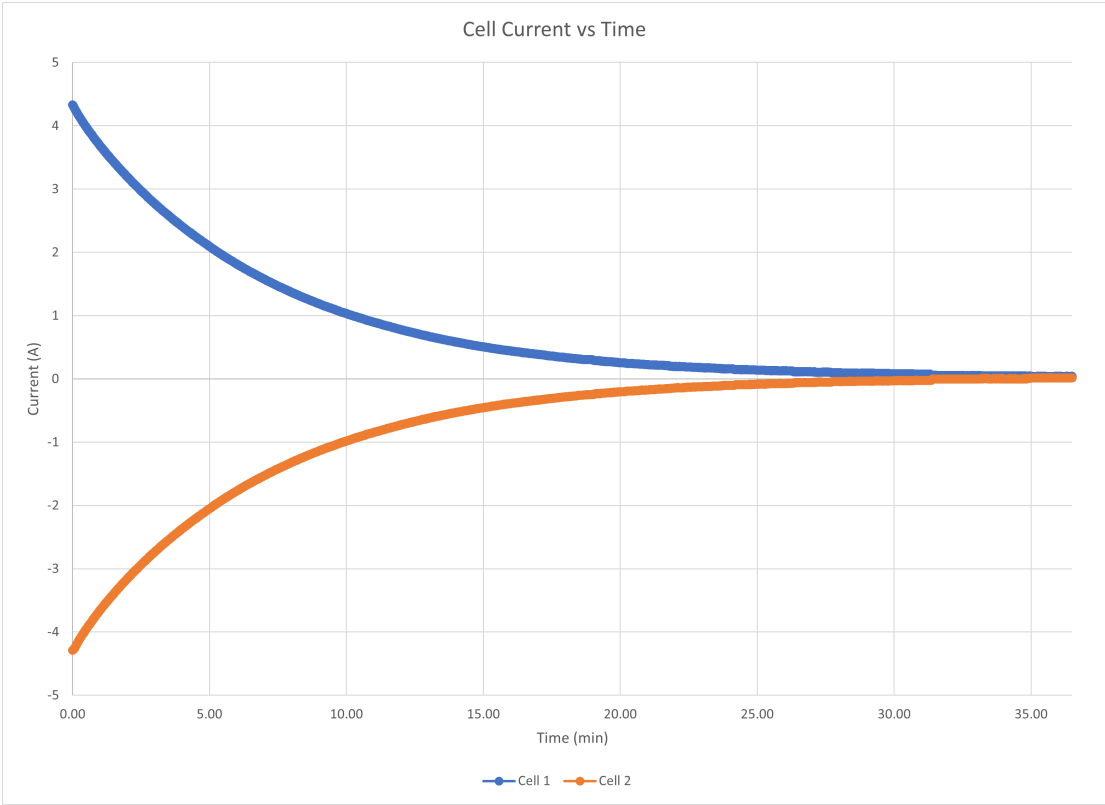
Figure 4-10: 2S NCH+PCH Dynamic Cell Voltages

Figure 4-11: 2S NCH+PCH Dynamic Cell Currents

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4.3 Comparing Practical 2S Designs

4.3.1 Balance Time

As expected, the 2S NCH design is slightly faster than the 2S NCH+PCH design since $R_{eq,1} < R_{eq,2}$ (see Table 4.1). This due to the switches in the latter design having higher resistance. Otherwise, the power circuits are identical.

Design	Balance Time [min]
2S NCH	25.2
2S NCH+PCH	31.4

Table 4.1: Measured Balance Times for 2S Balancers

4.3.2 Volume and Cost

While the board outline is the same for both PCBs, the 2S NCH+PCH design uses less volume and is cheaper to fabricate. The 2S NCH+PCH design does not need an op-amp and its associated passives, and requires two gate drivers instead of four [10, 20, 21]. The reduction in volume and simplification of the PCB layout starts to become more significant as the balancer is generalized for more cells. However, this improvement in cost, volume, and PCB layout comes with a trade-off of slower balance time. Any engineer developing these circuits should weigh relevant performance metrics accordingly and make informed design choices tailored for the application at hand. Table A.1 and A.2 show complete component lists for the 2S NCH and 2S NCH+PCH designs respectively.

4.4 4S Design

We build a 4S Multi-Tier balancer by extending the work in Sections 4.1, 4.2, and 4.3. The 2S NCH+PCH Balancer is chosen as the fundamental building block to minimize cost, component count, and simplify PCB layout. Fig. B-6 shows the schematic for the 4S NCH+PCH design, which utilizes a resonant SCC 4S balancer. To verify the

design before PCB layout, we simulate this circuit using LTSpice (refer to Fig. B-3).
Top and bottom 3D views of the PCB layout are shown in Fig. B-15 and B-16. The
populated PCB is presented in Fig. B-17 and B-18. Table A.3 shows a complete
component list.

4.4.1 LC Tank

Same component selection and reasoning as Section 4.1.1 for LC tanks at the bottom
tier of the balancer hierarchy: L_{12} and C_{12}, L_{23} and C_{23}, L_{34} and C_{34}. However, for
the middle and top tier, we add additional capacitors to mitigate increased DC bias
effects due to the higher average voltage. For C_{13} and C_{24}, five additional capacitors
(of the same component) were added. For C_{14}, ten additional capacitors were added
(of the same component).

4.4.2 Input Bypass Capacitors

Same component selection and reasoning as Section 4.1.2. Additionally, we add 4x47
μF capacitors (TMK325ABJ476MM-T) to provide further benefits in circuit perfor-
mance. This capacitor is rated for 25 V and has a 1210 package.

4.4.3 Switches and Bootstrap

Same component selection and reasoning as Section 4.2.3. However, we now have
eight switches due to the increase in number of battery cells. The bootstrap circuit
is identical but the associated component count is doubled.

4.4.4 Gate Drive

Same component selection and reasoning as Section 4.2.4. However, we now have
four gate drivers due to the increase in number of battery cells. We also place unity
gain buffers before each pair of gate driver inputs to prevent current overloading of
the external signal generator serving as the square wave input.

4.4.5 Testing

In experimental testing, the resonant frequency is 46 kHz with a maximum average balance current of 4.31 A, as shown in Fig. 4-12. This frequency sweep is performed with $[V_1, V_2, V_3, V_4] = [3, 3.4, 3.4, 3]$. Like the other designs, the main resistive bottleneck for this practical implementation is the bypass capacitors, determined through a high cell differential thermal test, as shown in Fig. 4-13. We conducted six different dynamic balancing tests (see Table 4.2). The balance time ($\tau_{b,meas}$) is still the time when $|\Delta V_{i,j}| < 10$ mV for every combination of battery cells i and j. We also use the same battery cell emulation parameters found in Table A.5.

We highlight the waveforms for initial condition 3 (see Fig. 4-14 and 4-15). Note that the curves of cells 2 and cells 3 move away and then back to each other due to resistive mismatches between LC tanks, which can cause the outer cells to "pull" the inner cells towards them during the balancing process. This phenomenon is avoided if all the resistances of the LC tanks are perfectly matched, but this is rarely the case in practical designs. The remaining curves for all other initial conditions can be found in Appendix B (starting with Fig. B-31). Table A.6 compares the performances of the 4S NCH+PCH and a commercial balancer.

Initial Condition	V_1 [V]	V_2 [V]	V_3 [V]	V_4 [V]	Balance Time [min]
(1)	3	3.4	3	3.4	49.17
(2)	3	3	3.4	3.4	67.9
(3)	3	3.2	3.2	3.4	61.3
(4)	3	3.1	3.3	3.4	64.95
(5)	3	3.3	3.1	3.4	57.45
(6)	3	3.4	3.4	3	25.8

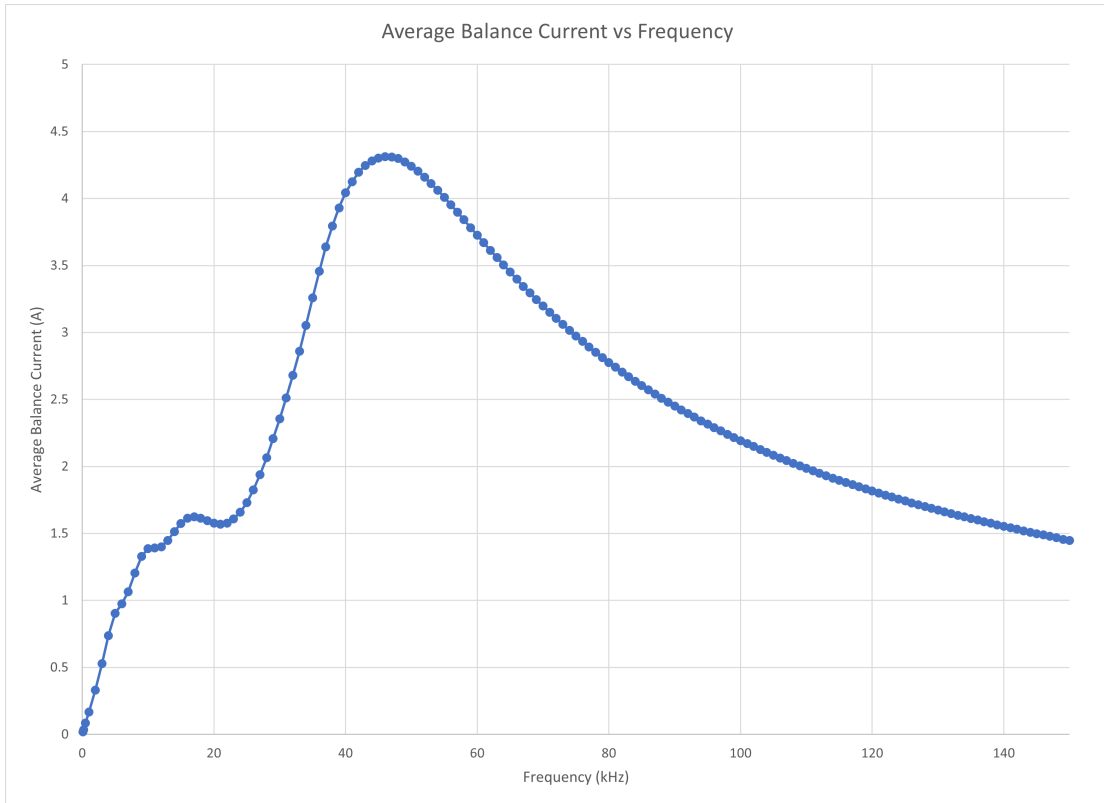Table 4.2: Measured Balance Times for 4S Balancer

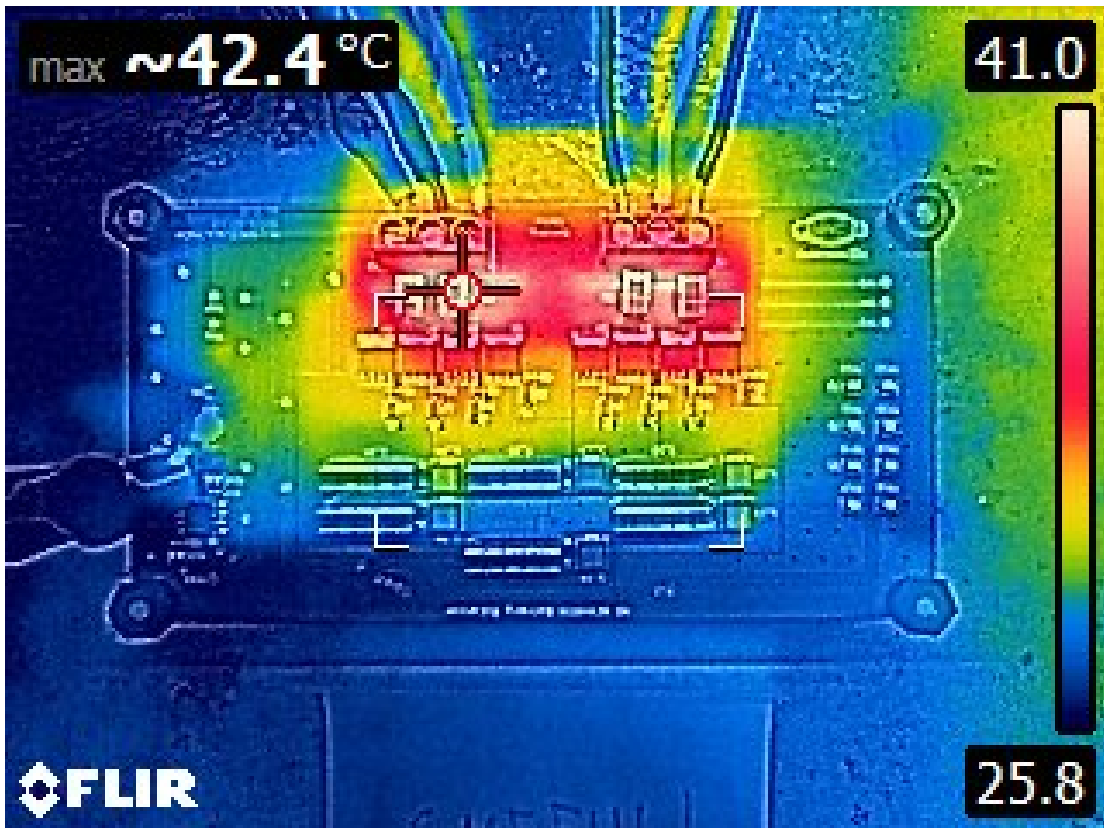Figure 4-12: 4S Average Balance Current vs Frequency
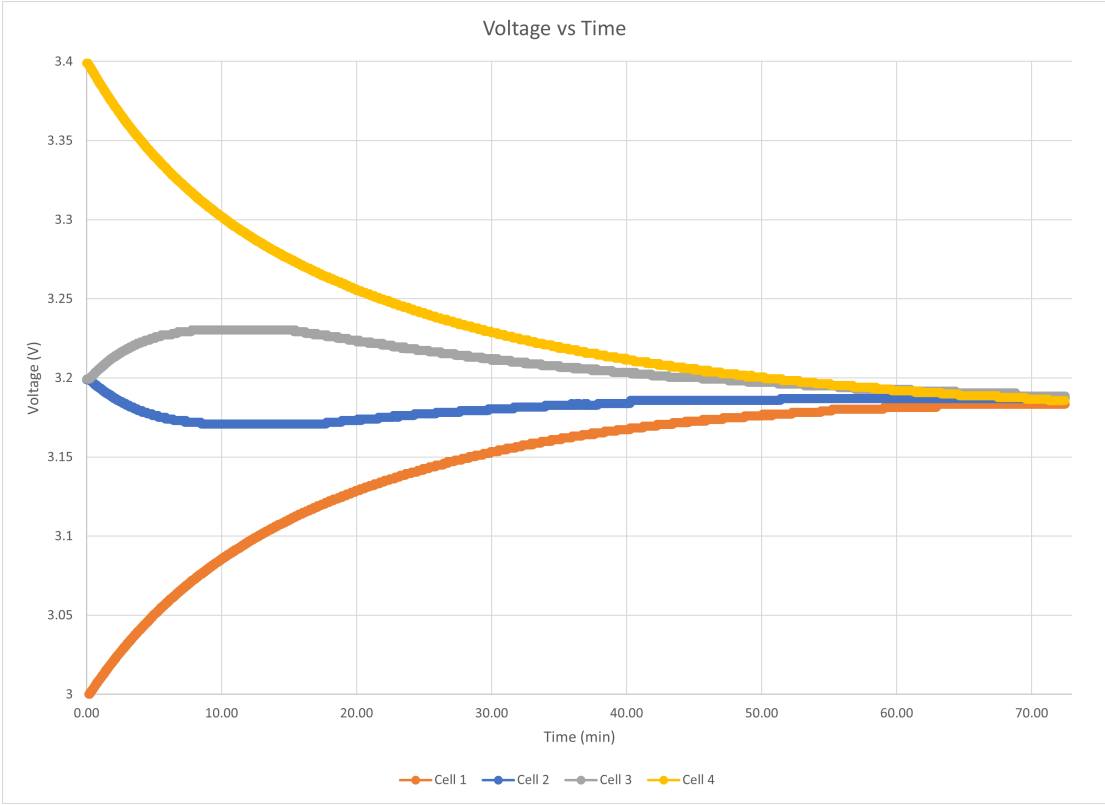

Figure 4-13: 4S Thermal Test

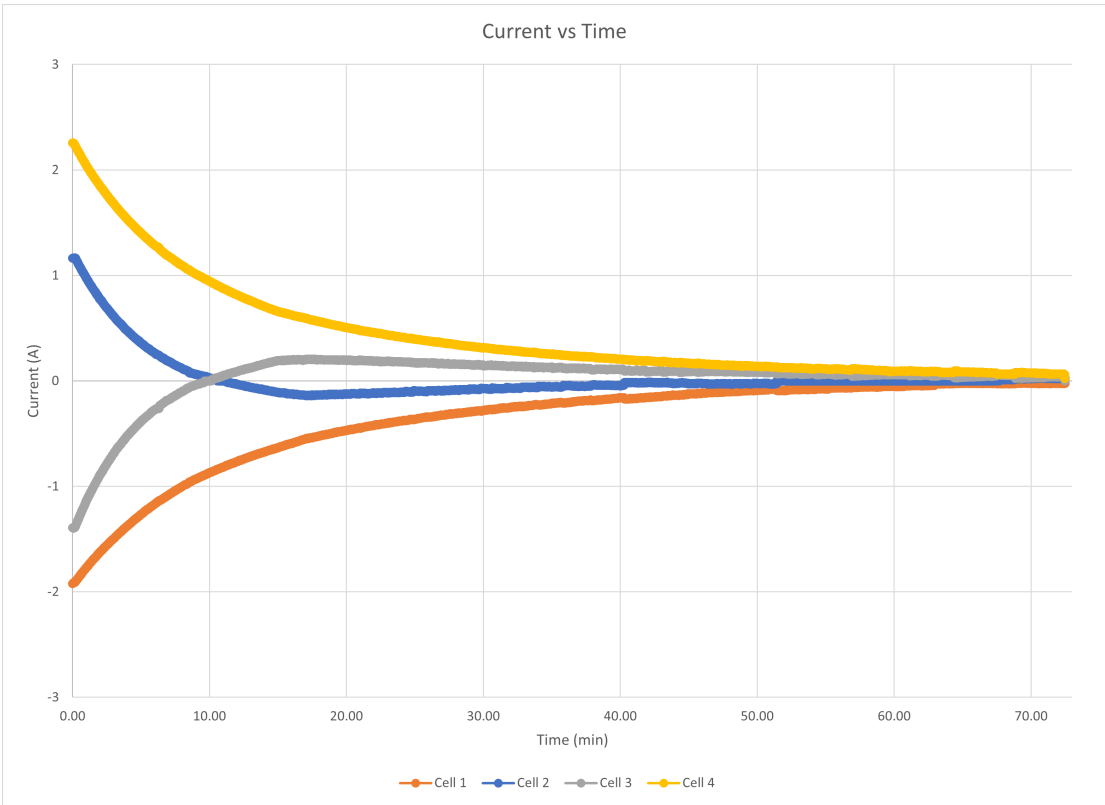Figure 4-14: 4S Dynamic Balance Test 3 Cell Voltages

Figure 4-15: 4S Dynamic Balance Test 3 Cell Currents

Chapter 5

Conclusions

This thesis has addressed and made progress towards some of the gaps in the present state of SCC battery balancers. We have presented a novel balancer topology called the Multi-Tier and derived an analytical solution (at the 3S and 4S level) through an average circuit model. A potential pathway towards low-entropy solutions for higher order balancers was shown (Chapter 2). We compared the new topology with a few others and demonstrated its potential through circuit simulations (Chapter 3). A practical implementation of the 4S Multi-Tier topology was built and its validity demonstrated (Chapter 4).

5.1   Modeling and Analysis

In Chapter 2, we began our modeling of SCC battery balancers by focusing on the fundamental building block for various topologies: the canonical 2S balancer. We showed how one can model its average behavior through an impedance based approach. A static and dynamic analysis was performed. We then presented a novel balancer topology, the Multi-Tier, and derived an analytical solution at the 3S and 4S level through simplifying assumptions. Theoretical balance time improvement was demonstrated with the addition of higher-tier capacitors. A pathway to low-entropy analysis of higher order balancers was discussed. Additionally, it was shown how analytical solutions of several other balancer topologies could be extracted from the

Multi-Tier. In Chapter 3, we ran simulations to compare the balance time of the new topology with similar ones.

5.2 Design

In Chapter 4, we built three practical SCC battery balancers. We designed two 2S canonical balancers and validated their functionality. One balancer utilized an all NCH power circuit while the other used NCH+PCH. Component selection, schematics, PCB layout, and experimental results were shown. Performance between designs was compared. This led to a practical 4S Multi-Tier Balancer. The 2S NCH+PCH design was chosen as the fundamental building block due to its reduced component selection and simplified PCB layout. Components, schematics, PCB layout, and experimental results were given for the 4S balancer.

5.3 Future Work

There is much analysis work needed for various higher order SCC balancing topologies. The author believes that meaningful analytical solutions using clever impedance approaches, such as the N Extra Element Theorem or Generalized Time-and Transfer-Constants, can yield fruitful theoretical insight. It could be worth starting from first principles and thinking of new creative approaches. There are also several other SCC battery balancing topologies that can be compared with the ones presented in this thesis.

On the practical side, there are plenty of experiments beyond those conducted for the 4S Multi-Tier balancer in this thesis. One can remove some of the energy tanks in the circuit to turn the Multi-Tier into a Double-Tier or Flat topology, and then perform the same experiments described in Chapter 4. Future work can also be design and testing of an 8S or higher order balancer implementation. Tests may also be ran with actual battery cells instead of supplies emulating them.

Appendix A

Tables

Component Type	Designator	Part Number	Manufacturer	Value
Decoupling Capacitor	C1, C8, C15, C18	CL21B105KPFNNNE	Samsung Electro-Mechanics	1 μF
Bypass Capacitor*	C14, C19	CL32B106KAJNNNE GMK325BJ226MM-P	Samsung Electro-Mechanics Taiyo Yuden	10 μF 3×(22 μF)
Decoupling Capacitor	C2, C4, C6, C9, C10, C12, C16, C17	CL10B104KO8NFNC	Samsung Electro-Mechanics	0.1 μF
Deadtime Capacitor	C3	885012006029	Würth Elektronik	1 nF
Bootstrap Capacitor	C5, C7, C11, C13	CL32B106KAJNNNE	Samsung Electro-Mechanics	10 μF
Flying Capacitor	C_{fly}	GMK325BJ226MM-P	Taiyo Yuden	10×(22 μF)
Schottky Diode	D1, D2, D3, D4, D5, D6, D7	CUS10S30,H3F	Toshiba Semiconductor and Storage	
LED	D8	XZMDKVG55W-4	SunLED	
Terminal Block	H1	OSTTC032162	On Shore Technology Inc.	
Flying Inductor	L_{fly}	PA5189.101HLT	Pulse Electronics	100 nH
Gate Driver	O1, O2, O3, O4	IS480P	Isocom Components 2004 LTD	
NCH Switch	Q1, Q2, Q3, Q4	IAUC120N04S6L008ATMA1	Infineon Technologies	
Bootstrap Switch	Q5, Q6	SSM3J340R,LF	Toshiba Semiconductor and Storage	
NCH Gate Resistor	R1, R2, R3, R4 R11, R12	WR06X100 JTL	Walsin Technology Corporation	10 Ω
LED Resistor	R5	RMCF0603JT100R	Stackpole Electronics Inc.	100 Ω
Deadtime Resistor	R7, R8	RMCF0603JT100R	Stackpole Electronics Inc.	100 Ω
DC Gain Resistor	R6	RC0603FR-071M6L	YAGEO	1.6 MΩ
Gate Driver Resistor	R9, R10	RC0603FR-07499RL	YAGEO	499 Ω
Test Point	TP1, TP2, TP6, TP7, TP8, TP13, TP14, TP15, TP16 TP17, TP18, TP19, TP20	5196TR	Keystone Electronics	
Op-amp	U1	OPA2197ID	Texas Instruments	

* C14, C19 are each the parallel combination of the two listed values.

Table A.1: Components of 2S NCH Balancer v1.1.0

Component Type	Designator	Part Number	Manufacturer	Value
Bootstrap Capacitor	C1, C3, C4, C5, C7, C8	CL32B106KAJNNNE	Samsung Electro-Mechanics	10 μF
Decoupling Capacitor	C10, C13	CL21B105KPFNNNE	Samsung Electro-Mechanics	1 μF
Decoupling Capacitor	C2, C6, C11, C12	CL10B104KO8NFNC	Samsung Electro-Mechanics	0.1 μF
Bypass Capacitor*	C9, C14	CL32B106KAJNNNE GMK325BJ226MM-P	Samsung Electro-Mechanics Taiyo Yuden	10 μF $3\times(22\ \mu\text{F})$
Flying Capacitor	C_{fly}	GMK325BJ226MM-P	Taiyo Yuden	$10\times(22\ \mu\text{F})$
Schottky Diode	D1, D2, D3, D4, D5, D6, D7, D8	CUS10S30,H3F	Toshiba Semiconductor and Storage	
LED	D9	XZMDKVG55W-4	SunLED	
Terminal Block	H1	OSTTC032162	On Shore Technology Inc.	
Flying Inductor	L_{fly}	PA5189.101HLT	Pulse Electronics	100 nH
Gate Driver	O1, O2	IS480P	Isocom Components 2004 LTD	
PCH Switch	Q1, Q3	SQJ123ELP-T1_GE3	Vishay Siliconix	
NCH Switch	Q2, Q4	PH2925U,115	Nexperia USA Inc.	
PCH Gate Resistor	R1, R3	RK73B1JTTD1R0J	KOA Speer Electronics, Inc.	1 Ω
Gate Driver Resistor	R5, R6	RC0603FR-07499RL	YAGEO	499 Ω
NCH Gate Resistor	R2, R4	WR06X100 JTL	Walsin Technology Corporation	10 Ω
LED Resistor	R7	RMCF0603JT100R	Stackpole Electronics Inc.	100 Ω
Test Point	TP1, TP2, TP6, TP7, TP8, TP13, TP14, TP15, TP16	5196TR	Keystone Electronics	

* C9, C14 are each the parallel combination of the two listed values.

Table A.2: Components of 2S NCH+PCH Balancer v1.1.0

Component Type	Designator	Part Number	Manufacturer	Value
Flying Capacitor*	C_{12}, C_{13}, C_{14}, C_{23}, C_{24}, C_{34}	GMK325BJ226MM-P	Taiyo Yuden	$10\times(22\ \mu F)$
Bootstrap Capacitor	C1, C3, C4, C5, C7, C8 C9, C13, C14, C15, C19, C20	CL32B106KAJNNNE	Samsung Electro-Mechanics	$10\ \mu F$
Decoupling Capacitor	C10, C16, C22, C25, C28, C31	CL21B105KPFNNNE	Samsung Electro-Mechanics	$1\ \mu F$
Decoupling Capacitor	C2, C6, C11, C12, C17, C18, C23, C24, C29, C30	CL10B104KO8NFNC	Samsung Electro-Mechanics	$0.1\ \mu F$
Bypass Capacitor†	C21, C26, C27, C32	CL32B106KAJNNNE GMK325BJ226MM-P TMK325ABJ476MM-T	Samsung Electro-Mechanics Taiyo Yuden Taiyo Yuden	$10\ \mu F$ $3\times(22\ \mu F)$ $4\times(47\ \mu F)$
Schottky Diode	D1, D2, D3, D4, D5, D6, D7, D8, D10, D11, D12, D13, D14, D15, D16, D17	CUS10S30,H3F	Toshiba Semiconductor and Storage	
LED	D9	XZMDKVG55W-4	SunLED	
Terminal Block	H1, H2	OSTTC032162	On Shore Technology Inc.	
Flying Inductor	L_{12}, L_{13}, L_{14}, L_{23}, L_{24}, L_{34}	PA5189.101HLT	Pulse Electronics	100 nH
Gate Driver	O1, O2, O3, O4	IS480P	Isocom Components 2004 LTD	
PCH Switch	Q1, Q3, Q5, Q7	SQJ123ELP-T1_GE3	Vishay Siliconix	
NCH Switch	Q2, Q4, Q6, Q8	PH2925U,115	Nexperia USA Inc.	
PCH Gate Resistor	R1, R3, R5, R7	RK73B1JTTD1R0J	KOA Speer Electronics, Inc.	$1\ \Omega$
Gate Driver Resistor	R10, R11, R12, R13	RC0603FR-07499RL	YAGEO	$499\ \Omega$
NCH Gate Resistor	R2, R4, R6, R8	WR06X100 JTL	Walsin Technology Corporation	$10\ \Omega$
LED Resistor	R9	RMCF0603JT100R	Stackpole Electronics Inc.	$100\ \Omega$
Test Point	TP1, TP2, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23	5196TR	Keystone Electronics	
Op-amp	U1	OPA2197ID	Texas Instruments	

* C_{12}, C_{23}, C_{34} are each $10\times(22\ \mu F)$. C_{13}, C_{24} are each $15\times(22\ \mu F)$. C_{14} is $20\times(22\ \mu F)$.
† C21, C26, C27, C32 are each the parallel combination of the three listed values.

Table A.3: Components of 4S NCH+PCH Balancer v1.0.0

Equipment Name	Function
Juntek JDS-2900-60M	Signal Generator
Itech IT-M3432	Battery Cell Emulation
Tektronix DP04034	Oscilloscope
LPKF Protoflow S4	Reflow Oven

Table A.4: Lab Equipment

Parameter	Value
Full Voltage	3.4 V
Empty Voltage	3 V
Capacity	1 Ah
Cell Resistance	0 mΩ

Table A.5: Battery Cell Emulation Parameters

Initial Condition	V_1 [V]	V_2 [V]	V_3 [V]	V_4 [V]	Commercial Balancer Experimental τ_b [min]	4S NCH+PCH Multi-Tier Balancer Experimental τ_b [min]
(1)	3	3.4	3	3.4	76.22	41.5
(2)	3	3	3.4	3.4	56.23	57.8
(3)	3	3.2	3.2	3.4	48.48	52.8
(4)	3	3.1	3.3	3.4	47.13	57.1
(5)	3	3.3	3.1	3.4	58.98	48.9

These balance time values use $\Delta v_b = 20$ mV

Table A.6: Balance Time Comparison Between Commercial Balancer and 4S NCH+PCH Multi-Tier Balancer

Appendix B

Figures
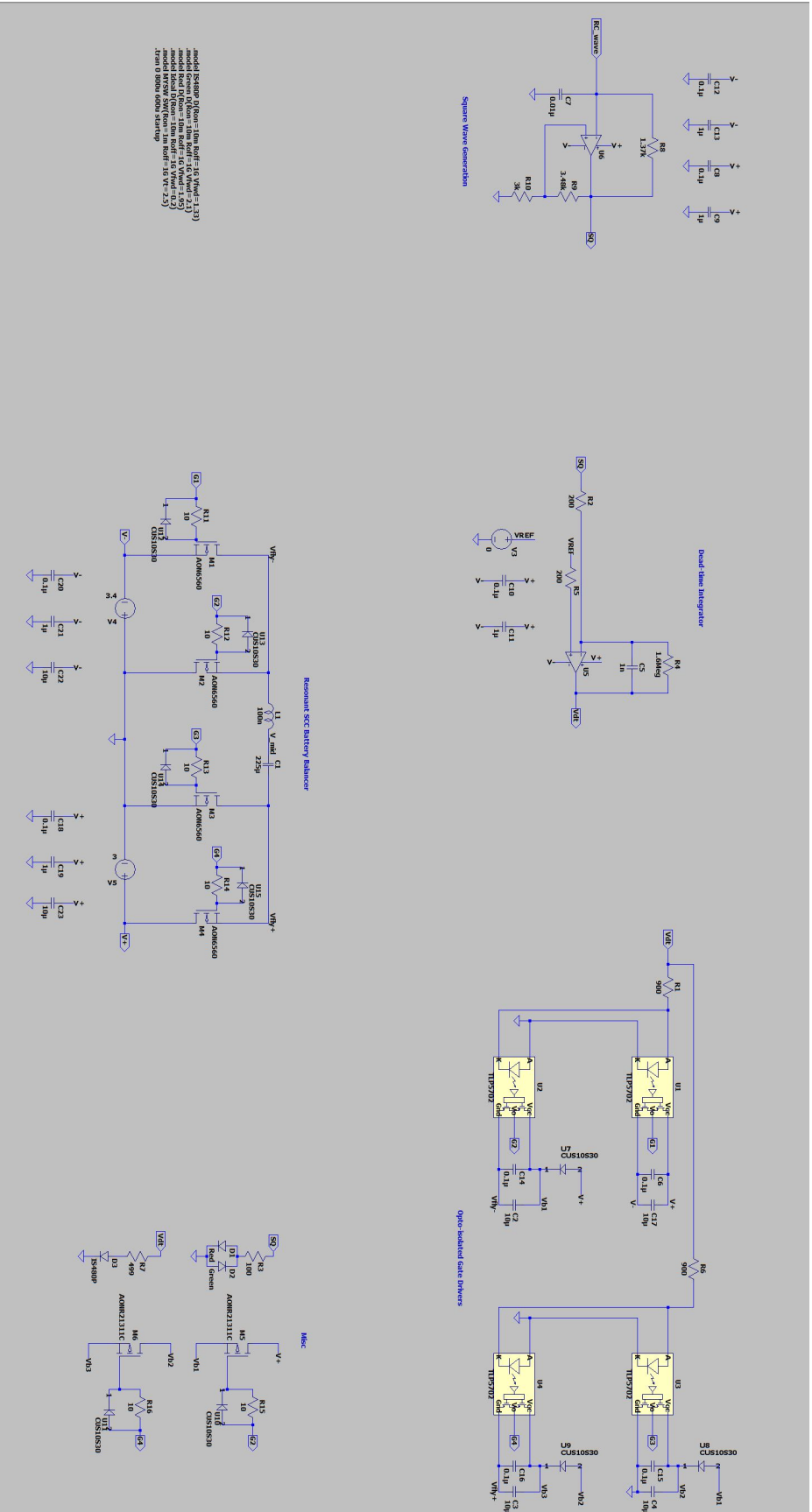
Figure B-1: LTSpice Simulation for 2S NCH Design
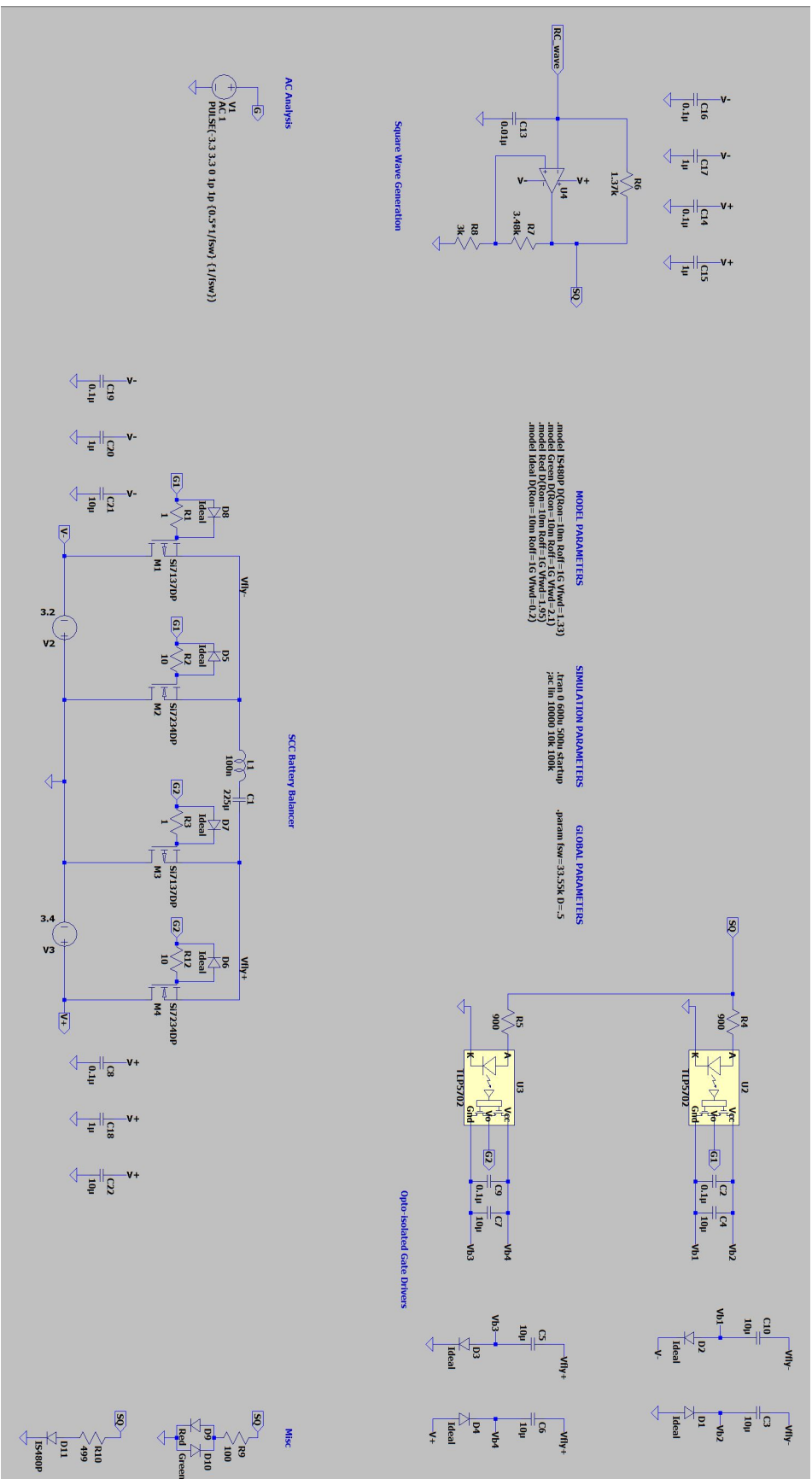
Figure B-2: LTSpice Simulation for 2S NCH+PCH Design
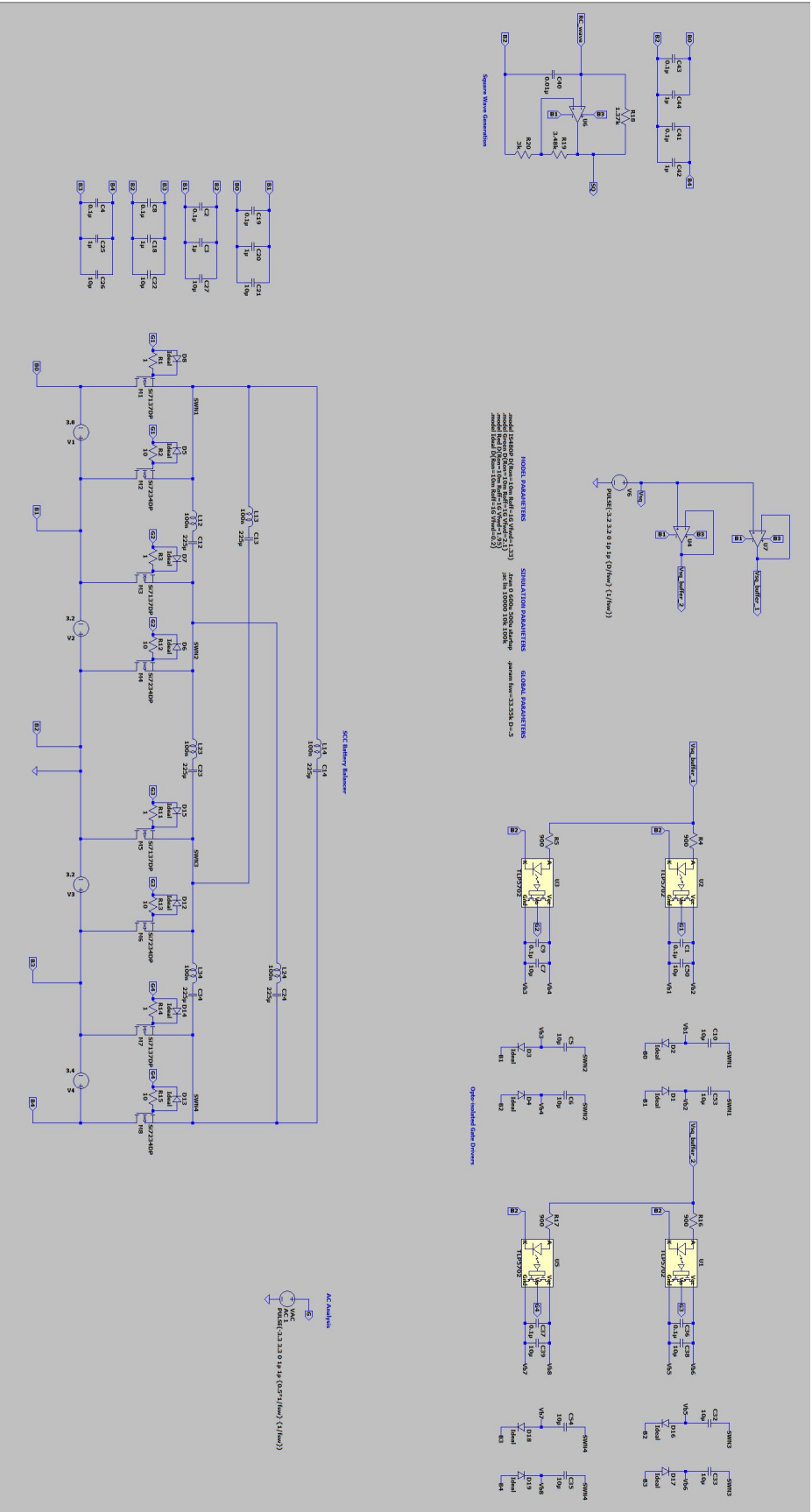
Figure B-3: LTSpice Simulation for 4S NCH+PCH Design
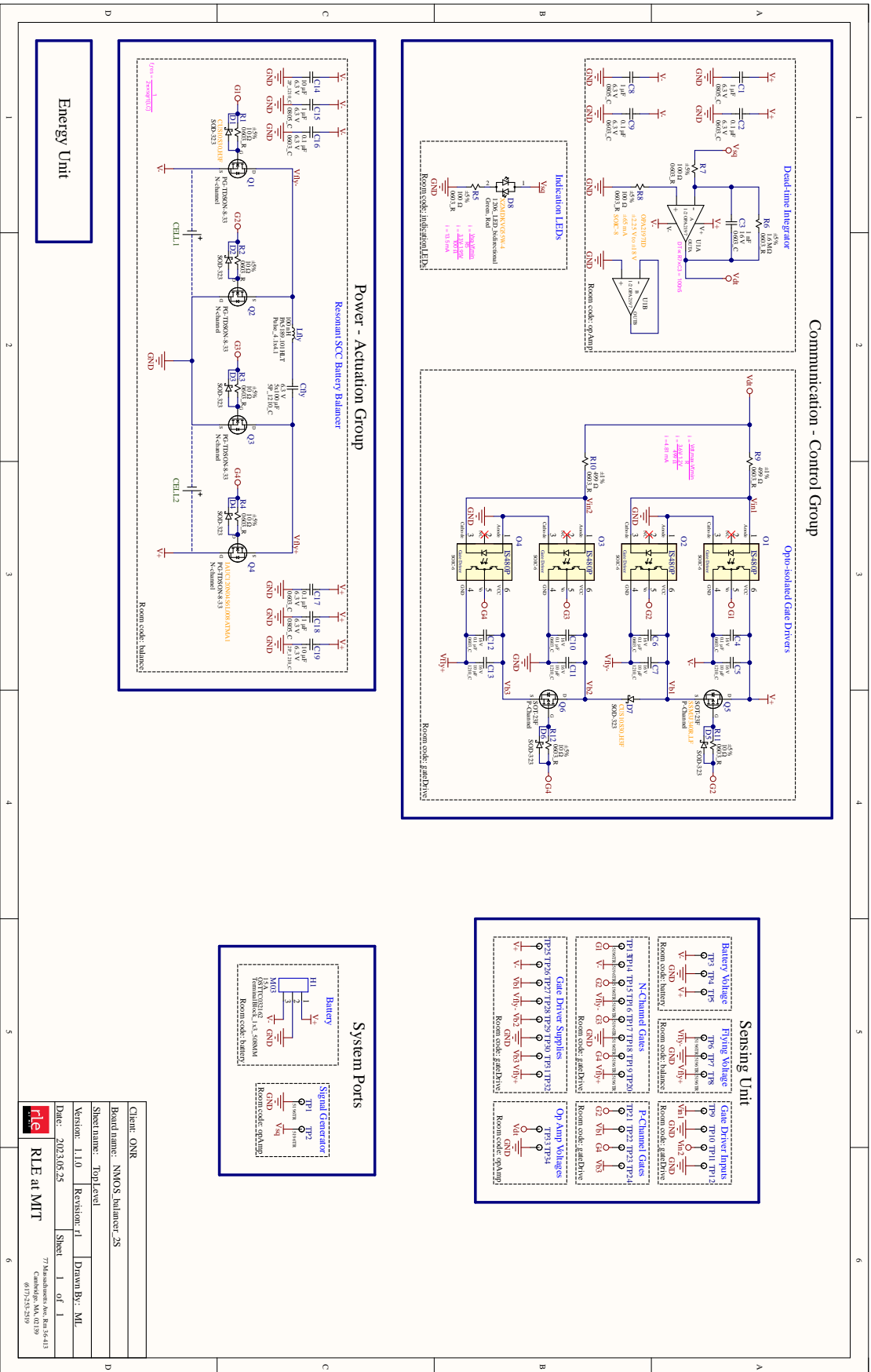
Figure B-4: 2S NCH Balancer Schematic
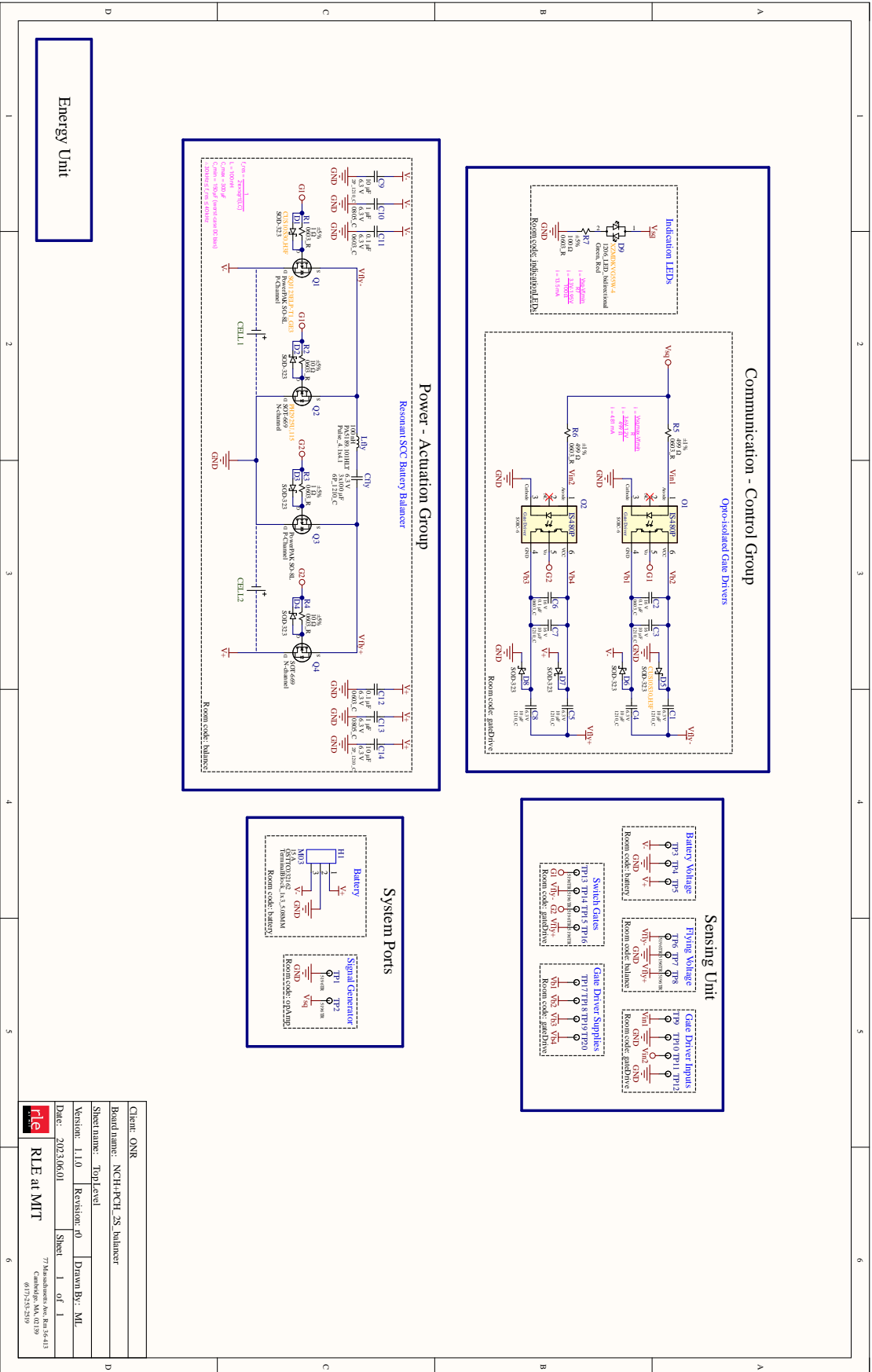
Figure B-5: 2S NCH+PCH Balancer Schematic
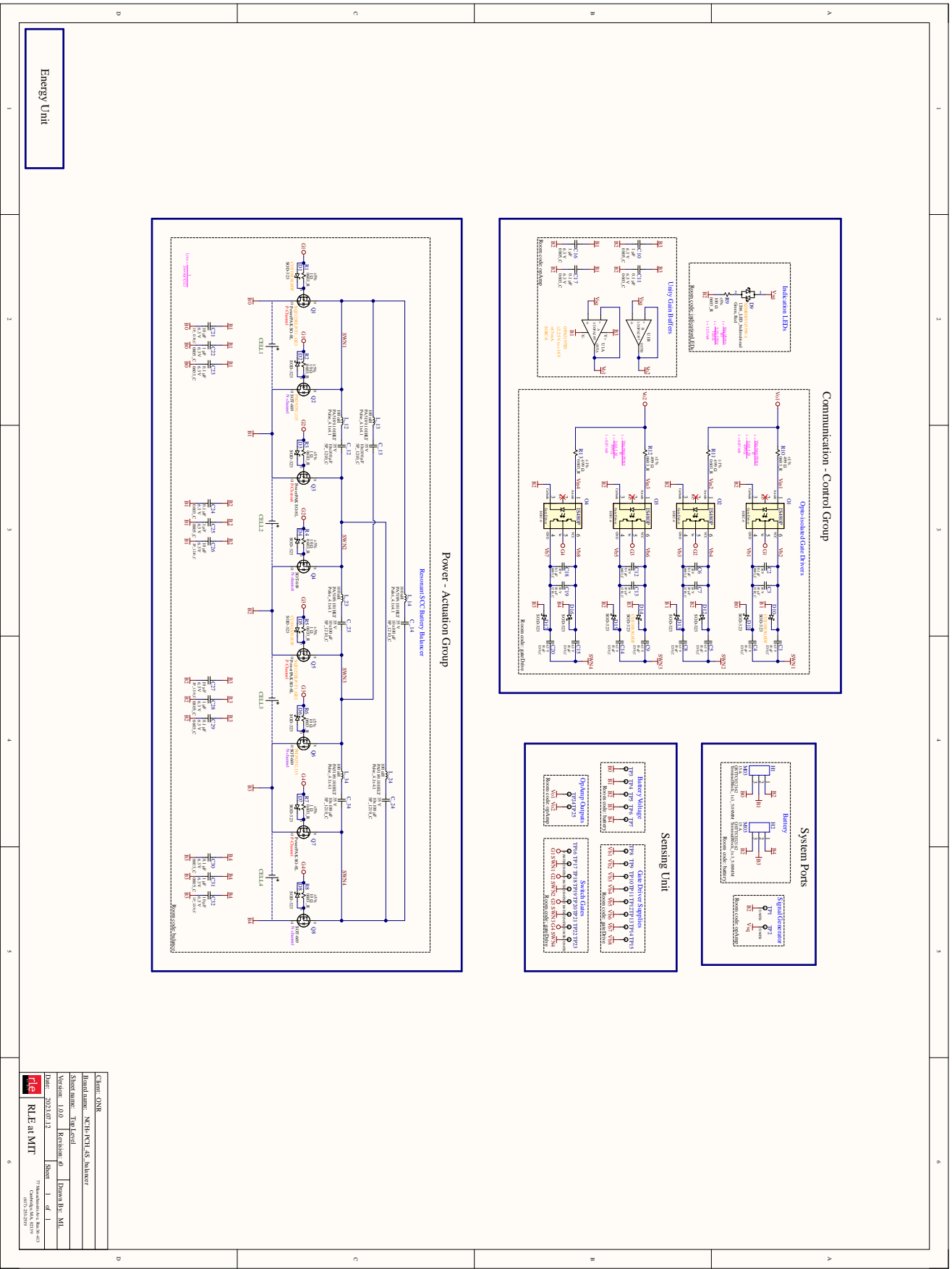
Figure B-6: 4S NCH+PCH Balancer Schematic
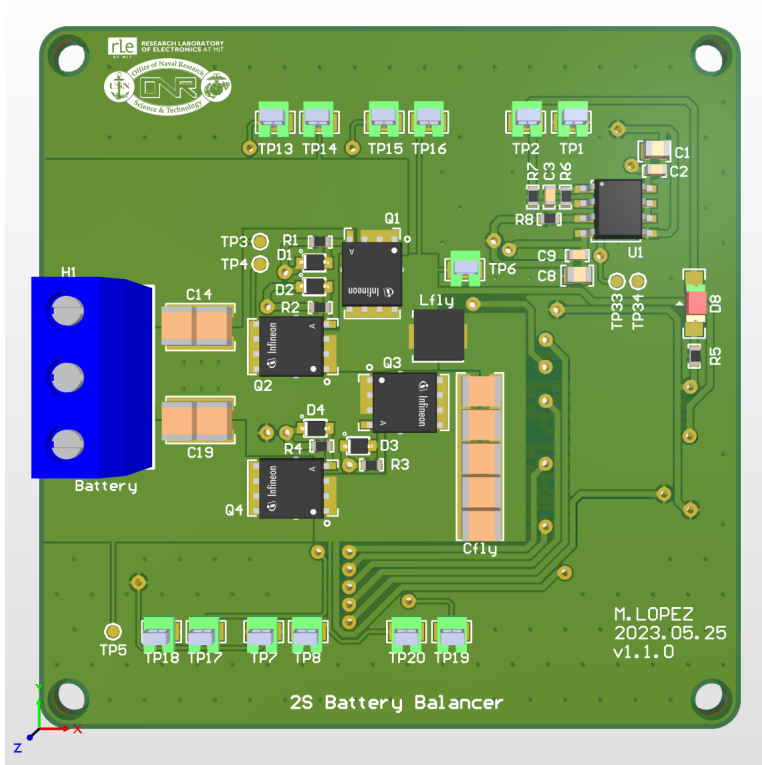
Figure B-7: 2S NCH Balancer Top Layout
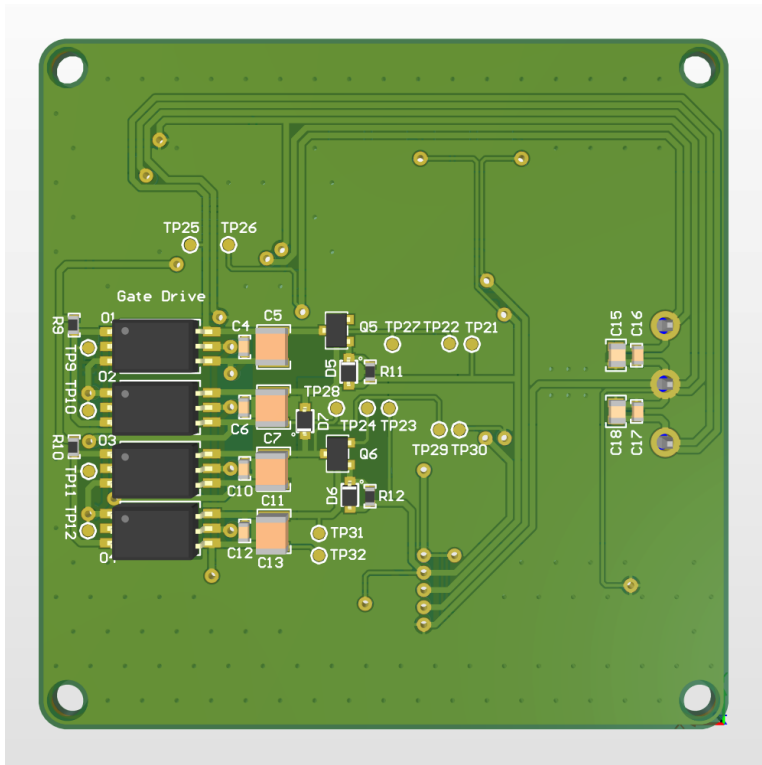
Figure B-8: 2S NCH Balancer Bottom Layout
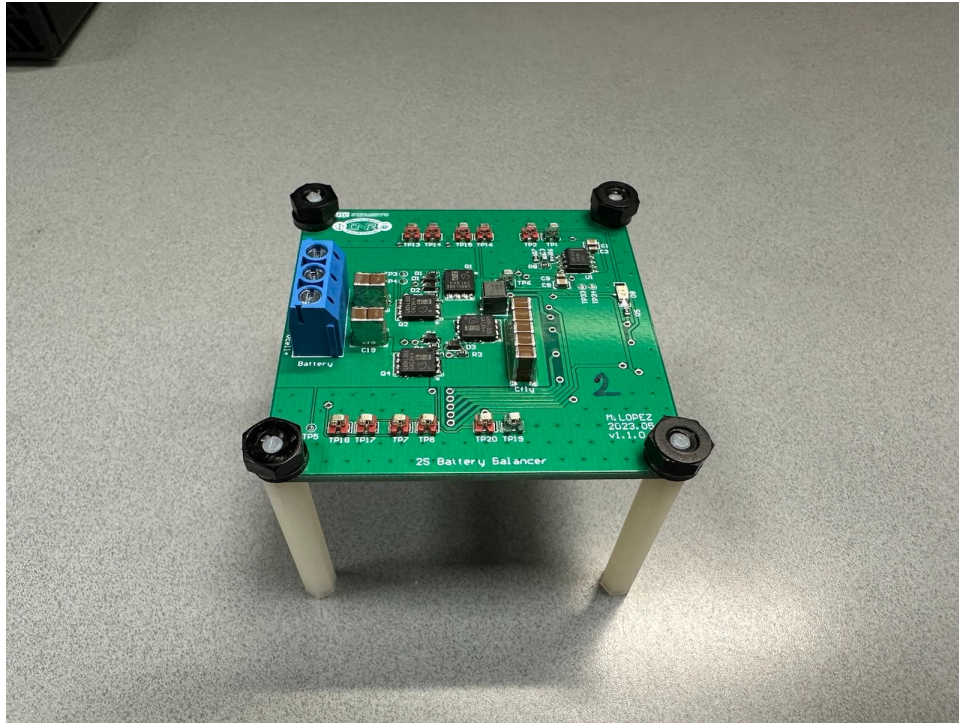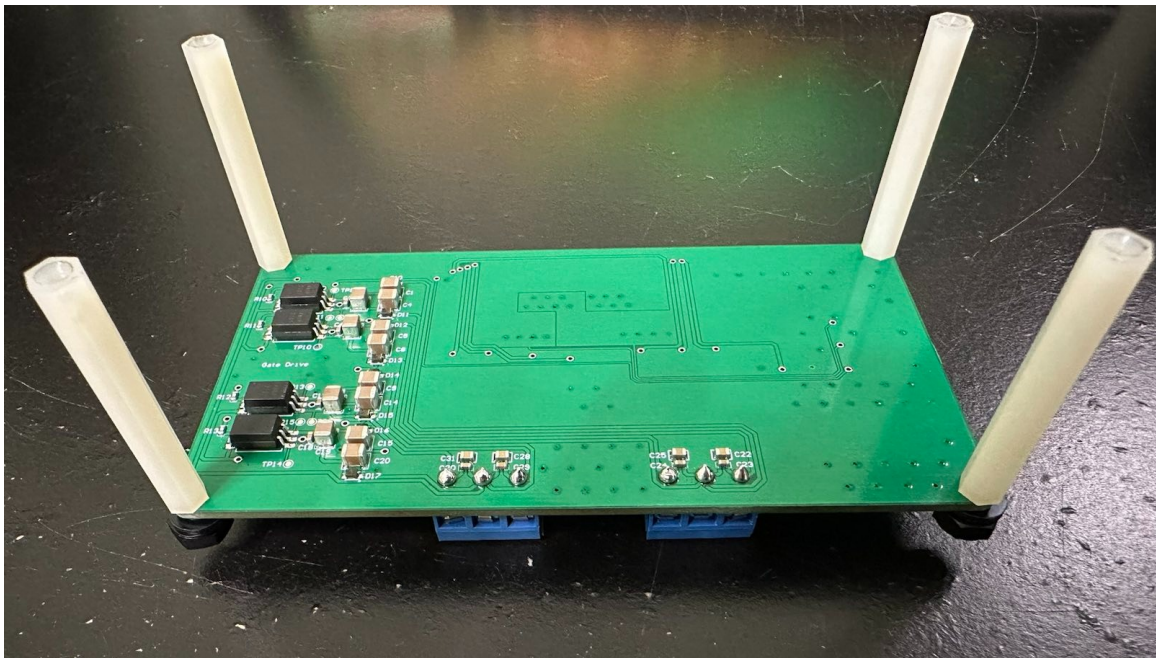
Figure B-9: 2S NCH Balancer PCB Top View
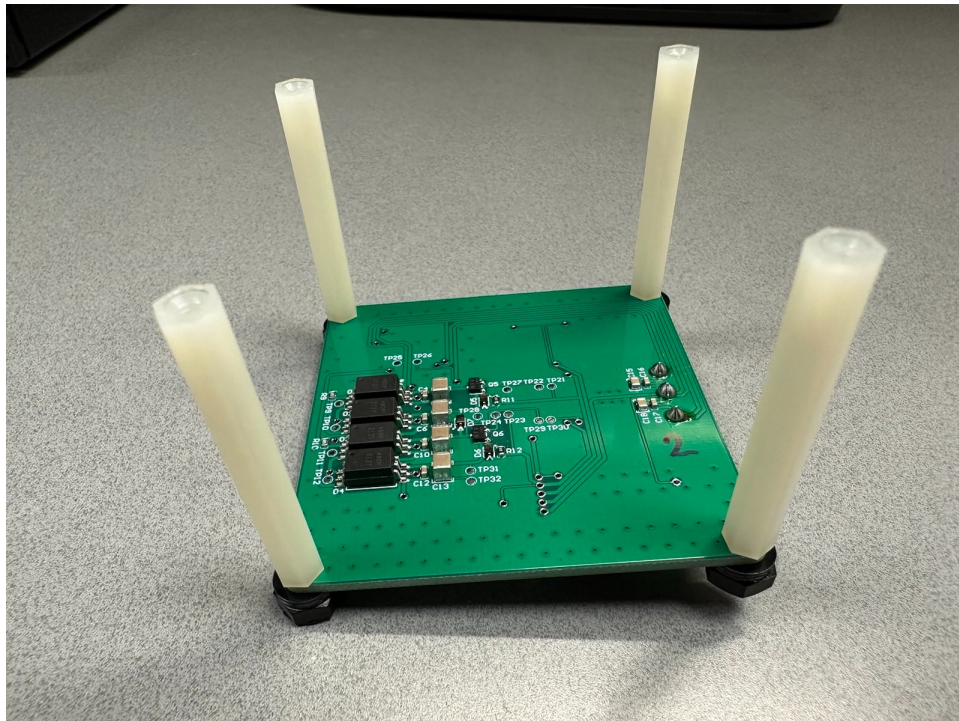

Figure B-10: 2S NCH Balancer PCB Bottom View
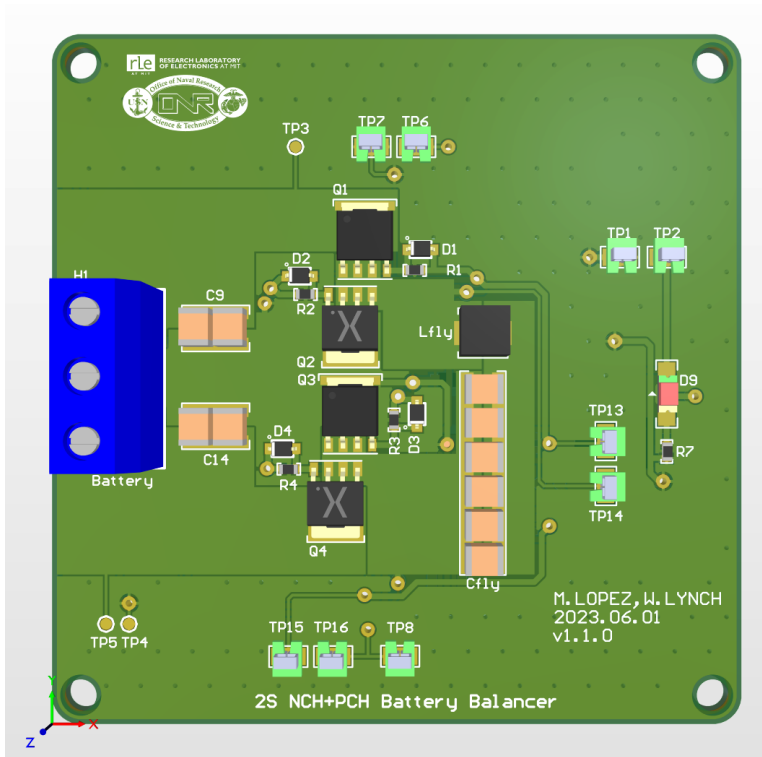
Figure B-11: 2S NCH+PCH Balancer Top Layout
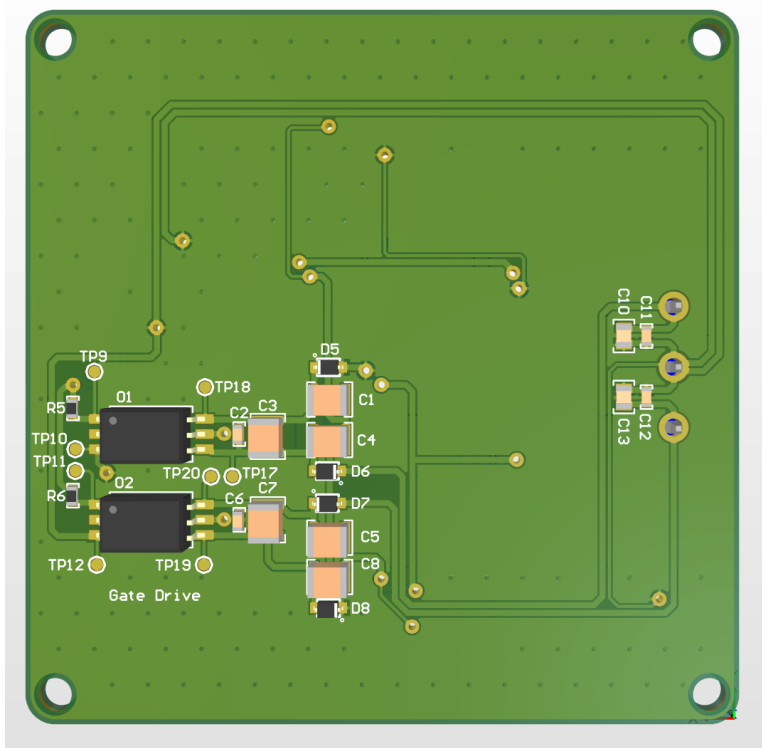
Figure B-12: 2S NCH+PCH Balancer Bottom Layout
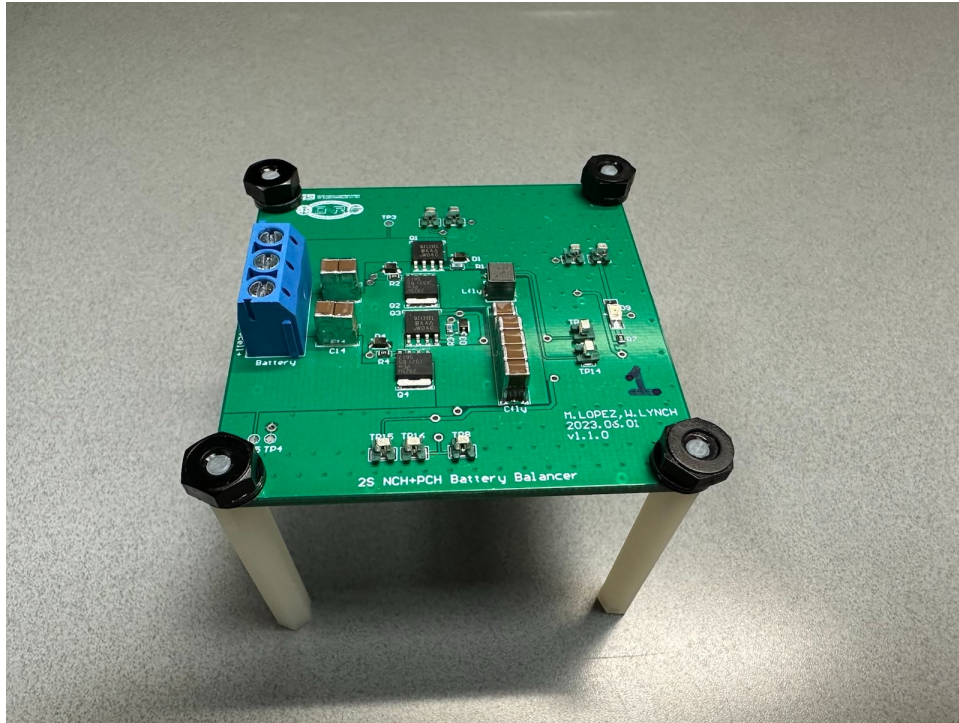
Figure B-13: 2S NCH+PCH Balancer PCB Top View
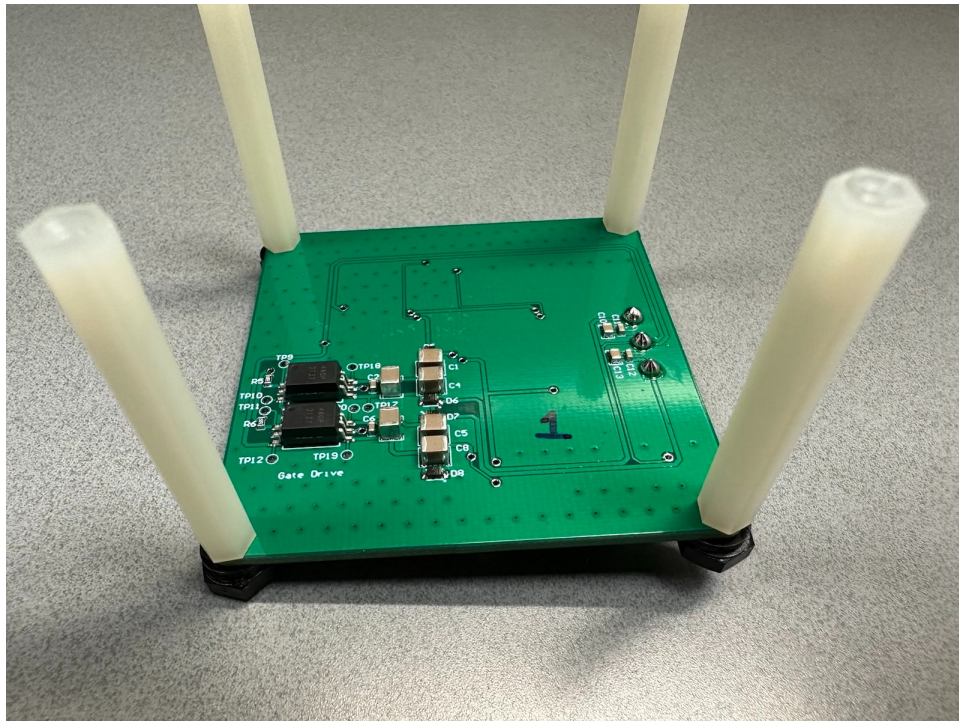
Figure B-14: 2S NCH+PCH Balancer PCB Bottom View
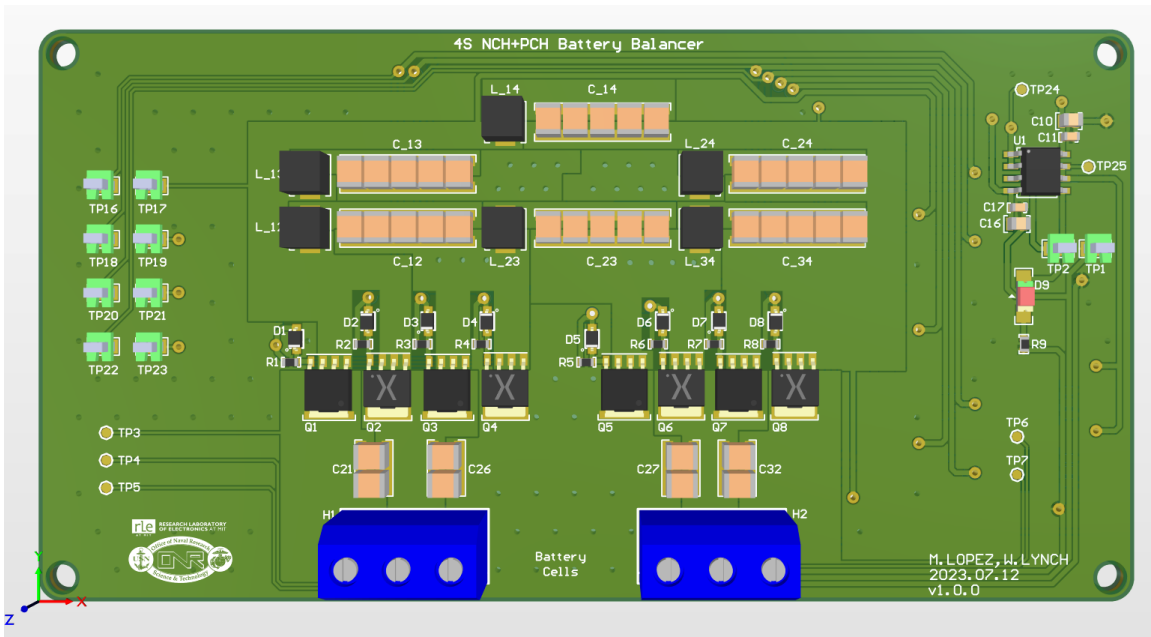
Figure B-15: 4S NCH+PCH Balancer Top Layout
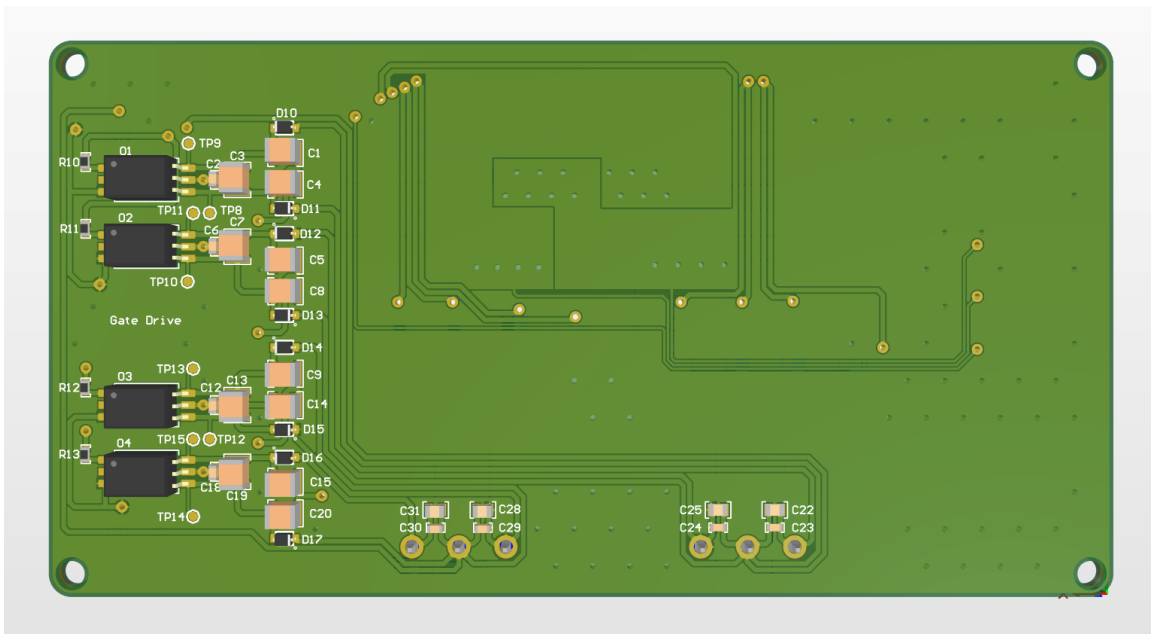
Figure B-16: 4S NCH+PCH Balancer Bottom Layout
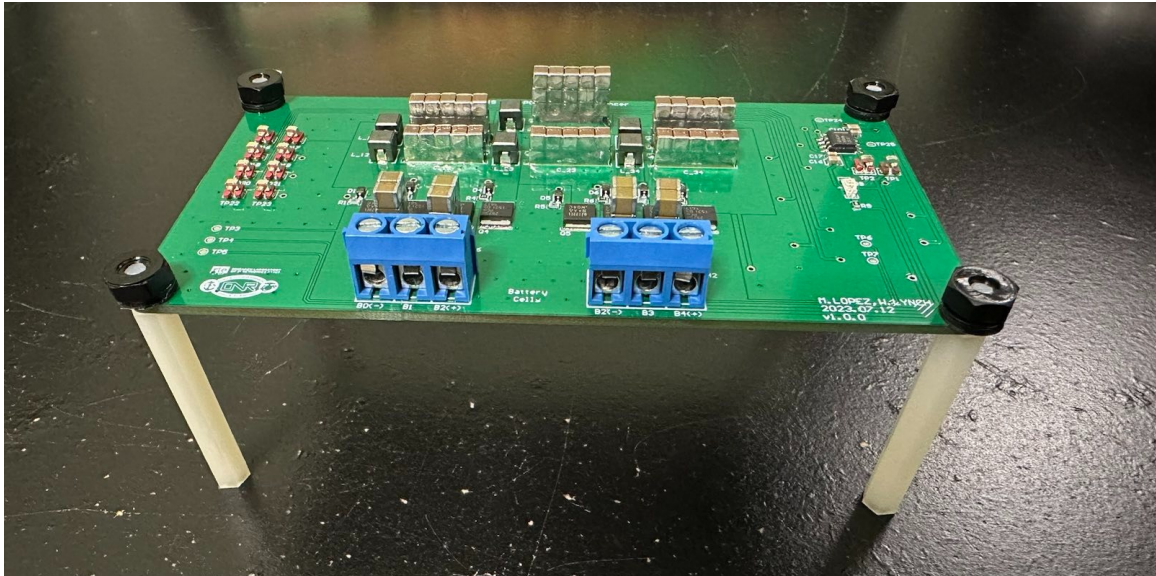
Figure B-17: 4S NCH+PCH Balancer PCB Top View

Figure B-18: 4S NCH+PCH Balancer PCB Bottom View
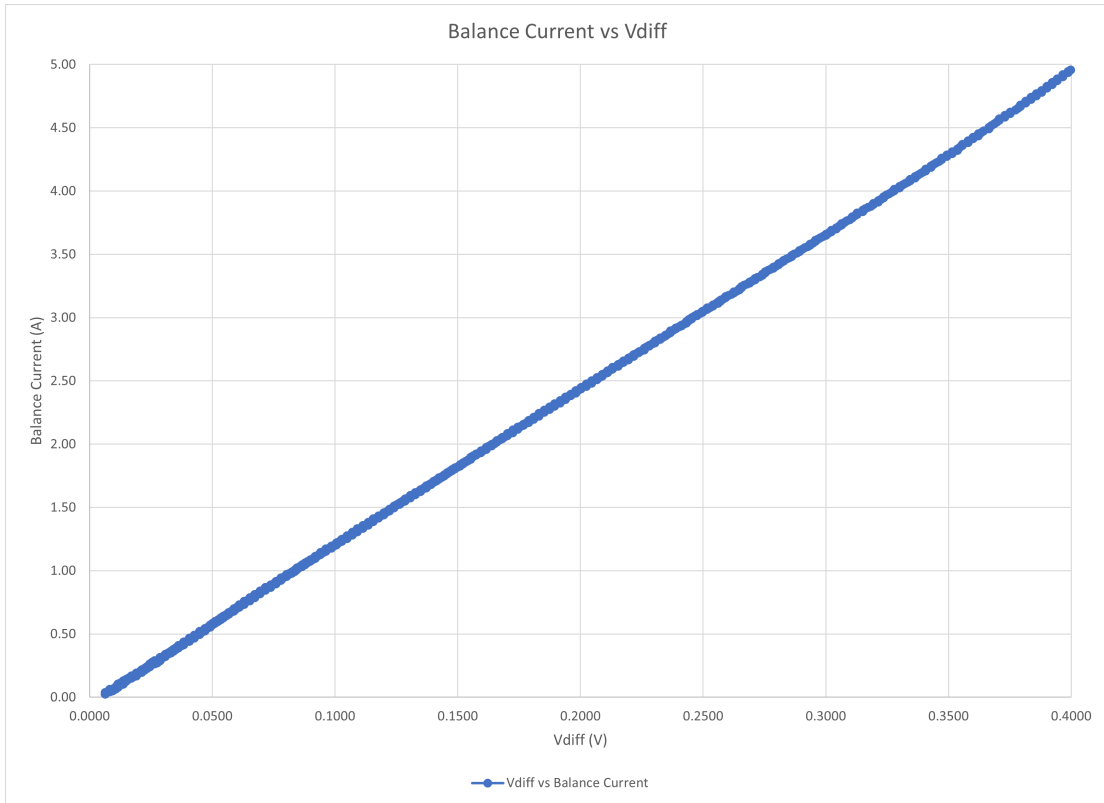
Figure B-19: 2S NCH Dynamic Balance Current vs ΔV
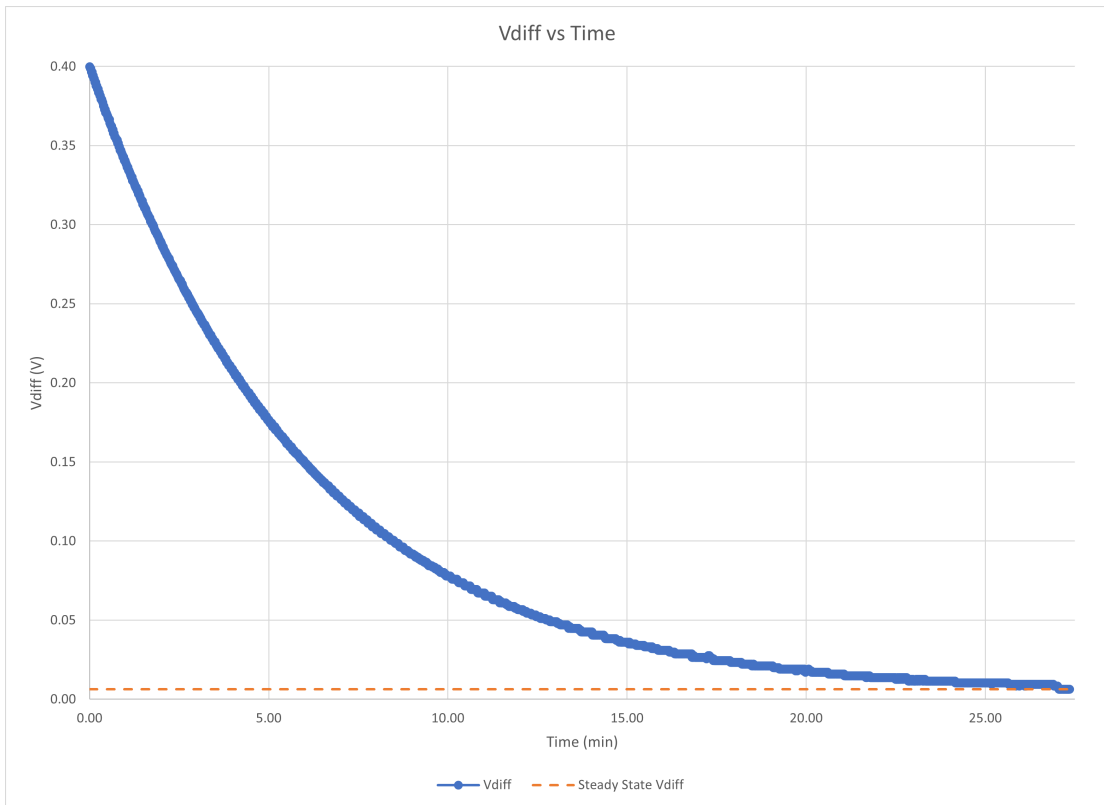
Figure B-20: 2S NCH Dynamic ΔV

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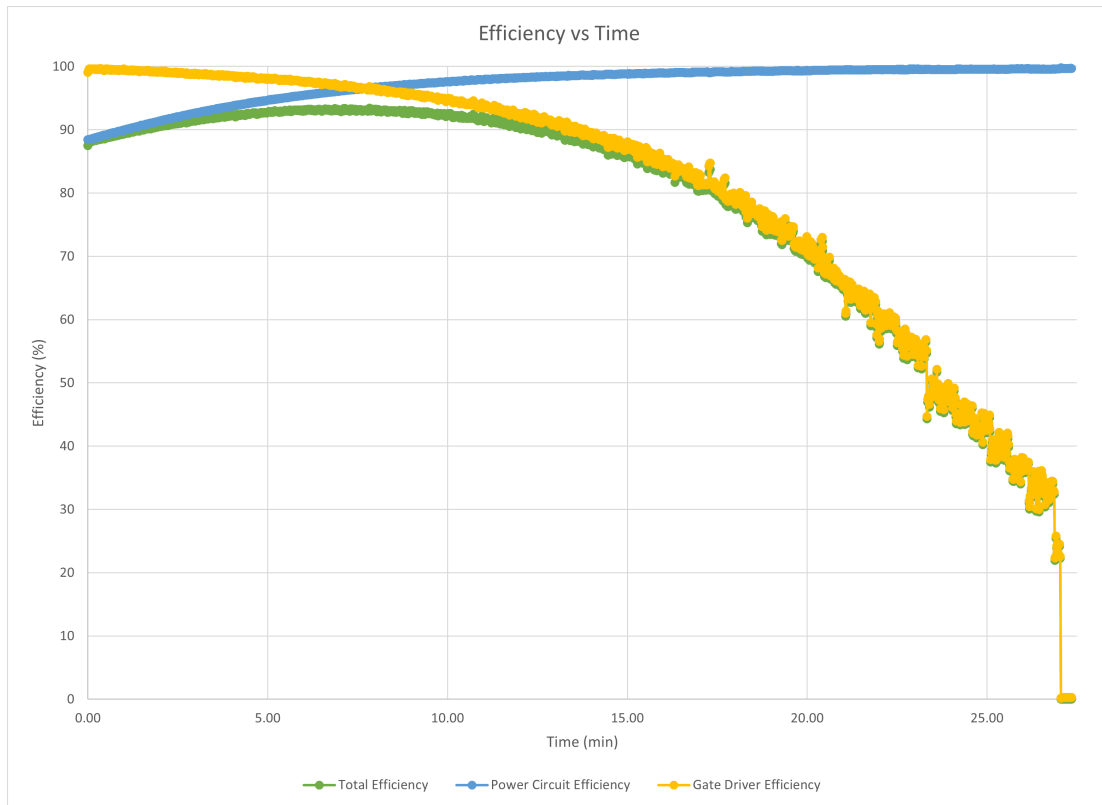
Figure B-21: 2S NCH Dynamic Efficiency
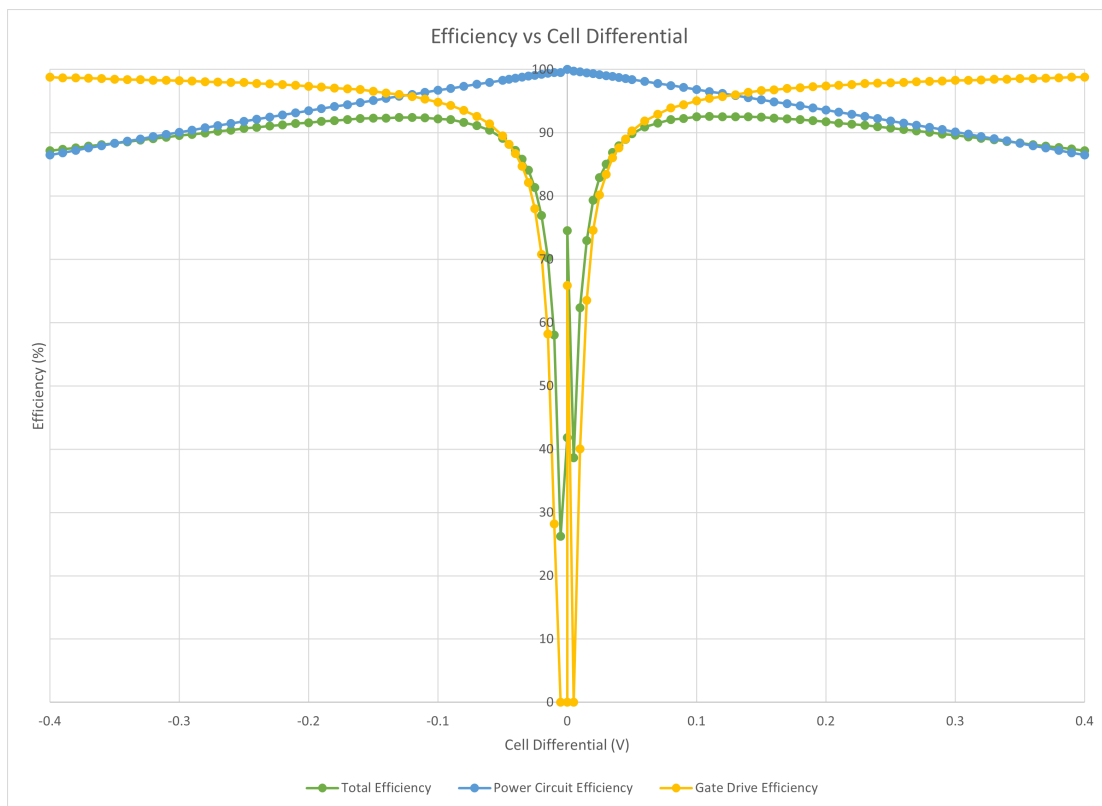
Figure B-22: 2S NCH Efficiency vs ΔV

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Figure B-23: 2S NCH Balancer Deadtime Verification

Figure B-24: 2S NCH Balancer Quasi-Synchronous Bootstrap Verification (V_{GS} shown for each switch)
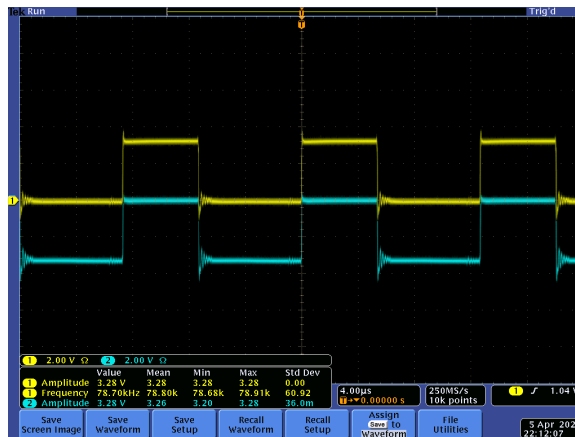
Figure B-25: 2S NCH Balancer Switching Node Voltages
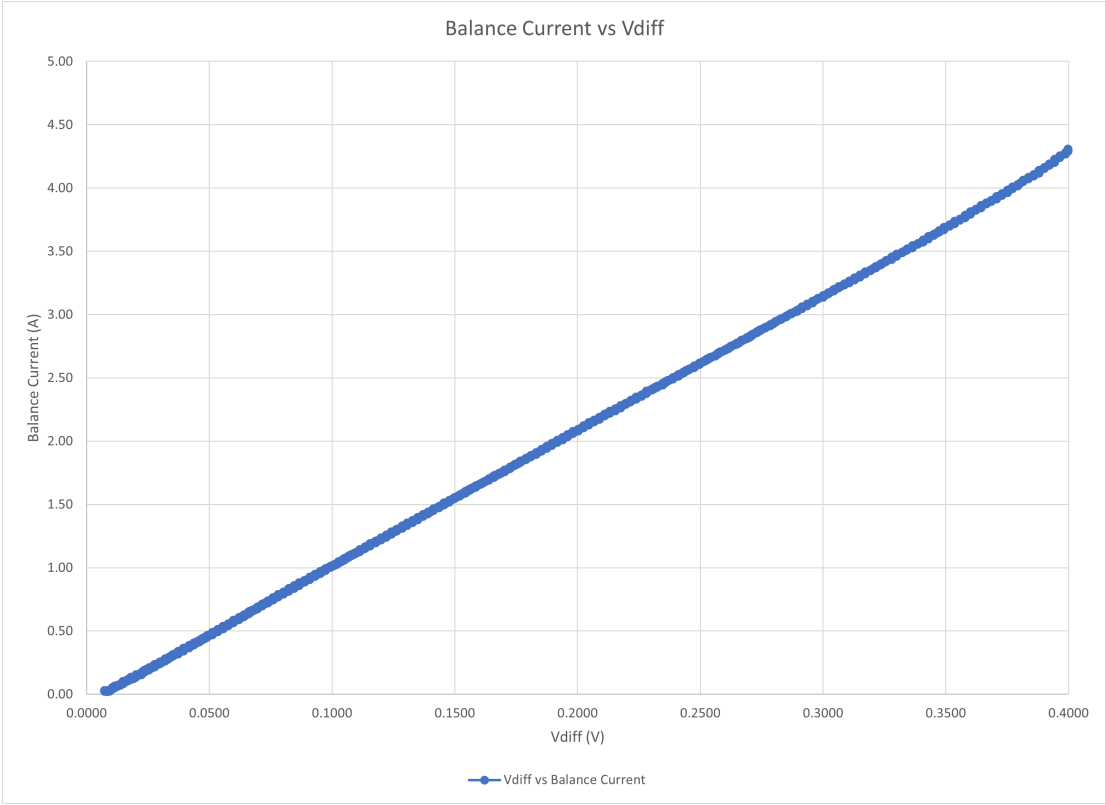
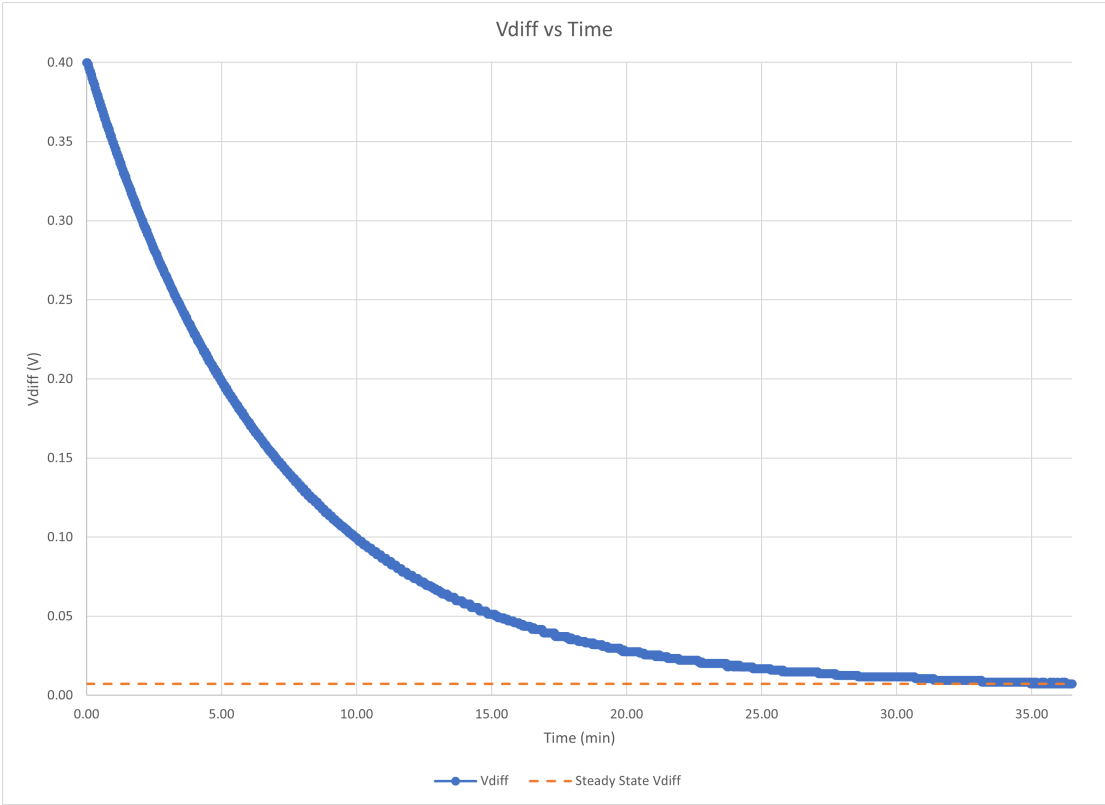Figure B-26: 2S N+P Dynamic Balance Current vs ΔV
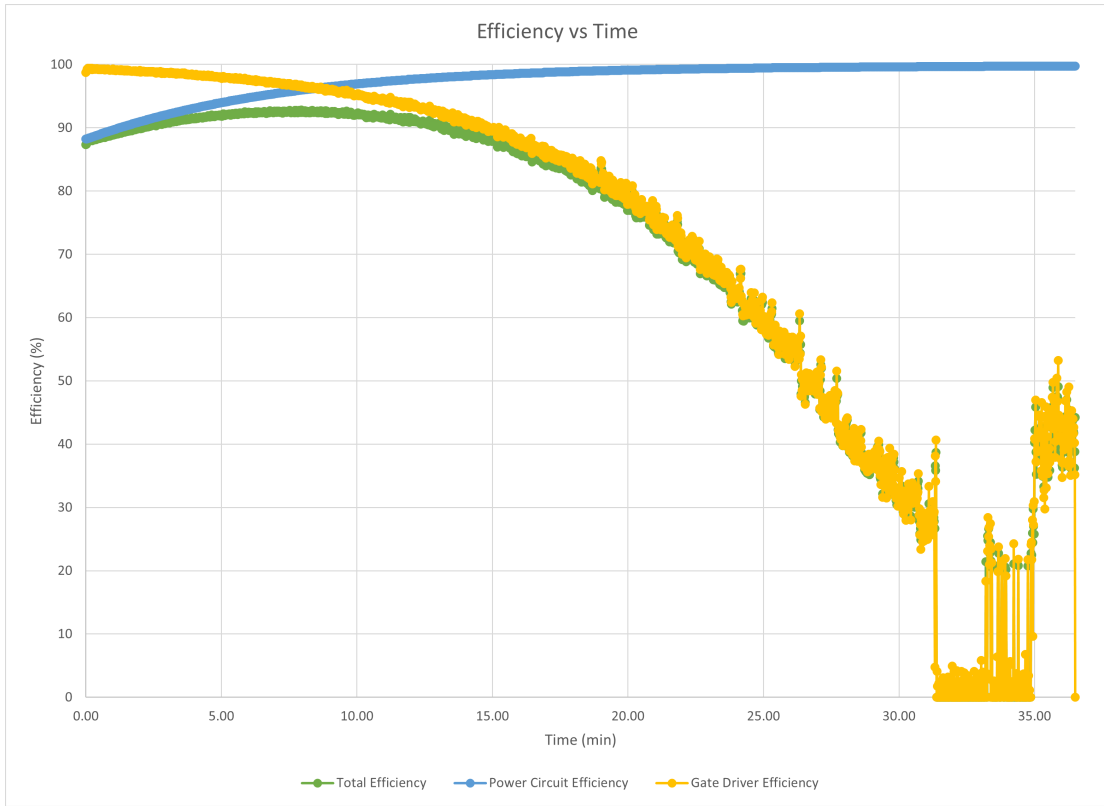

Figure B-27: 2S N+P Dynamic ΔV

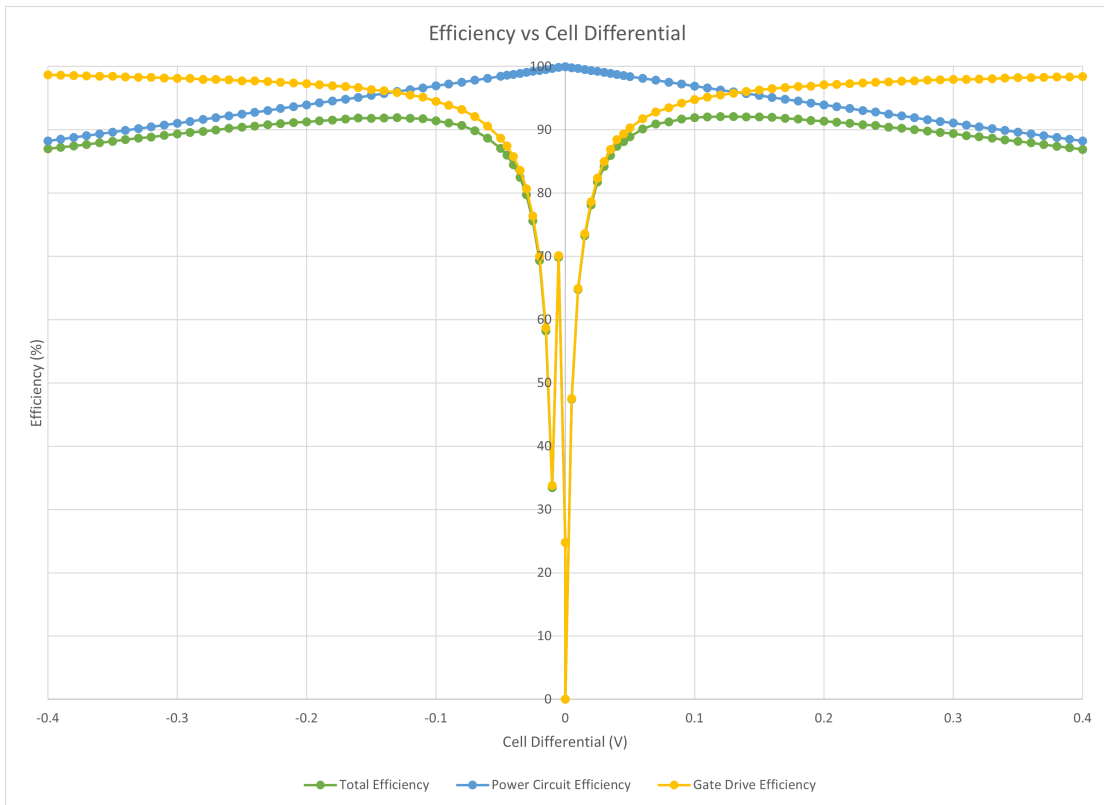Figure B-28: 2S N+P Dynamic Efficiency

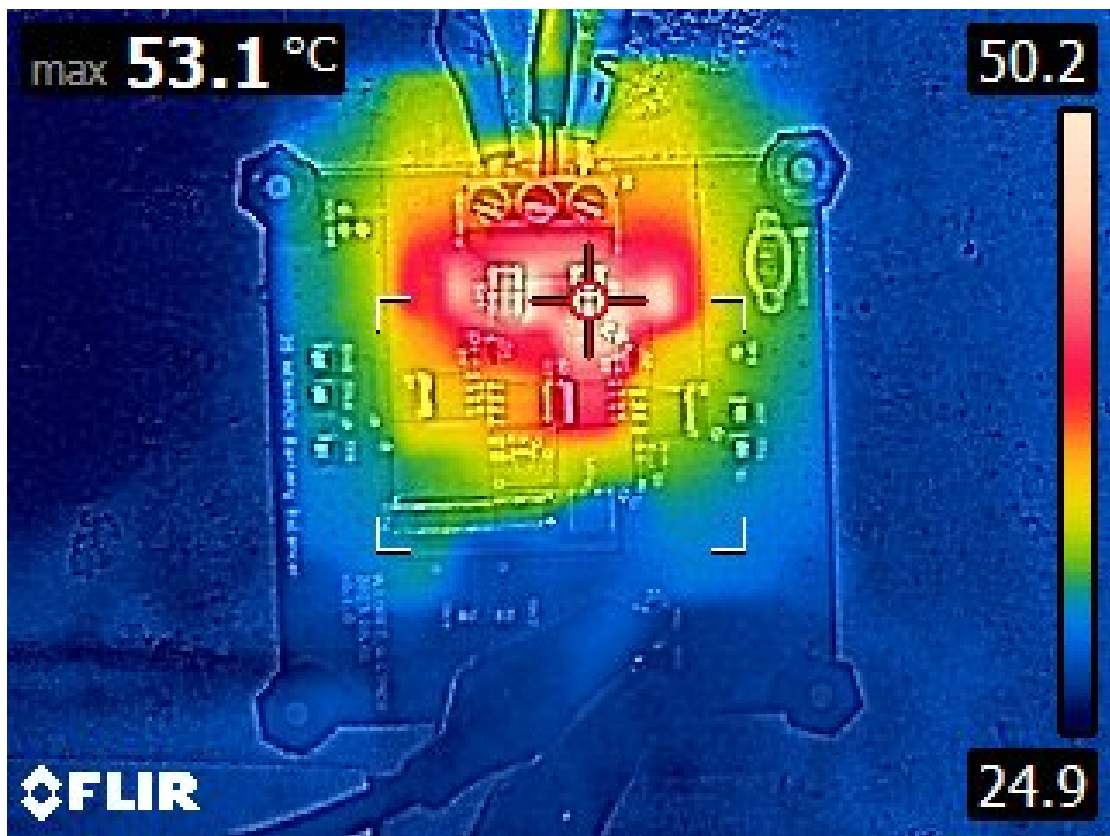Figure B-29: 2S N+P Efficiency vs ΔV

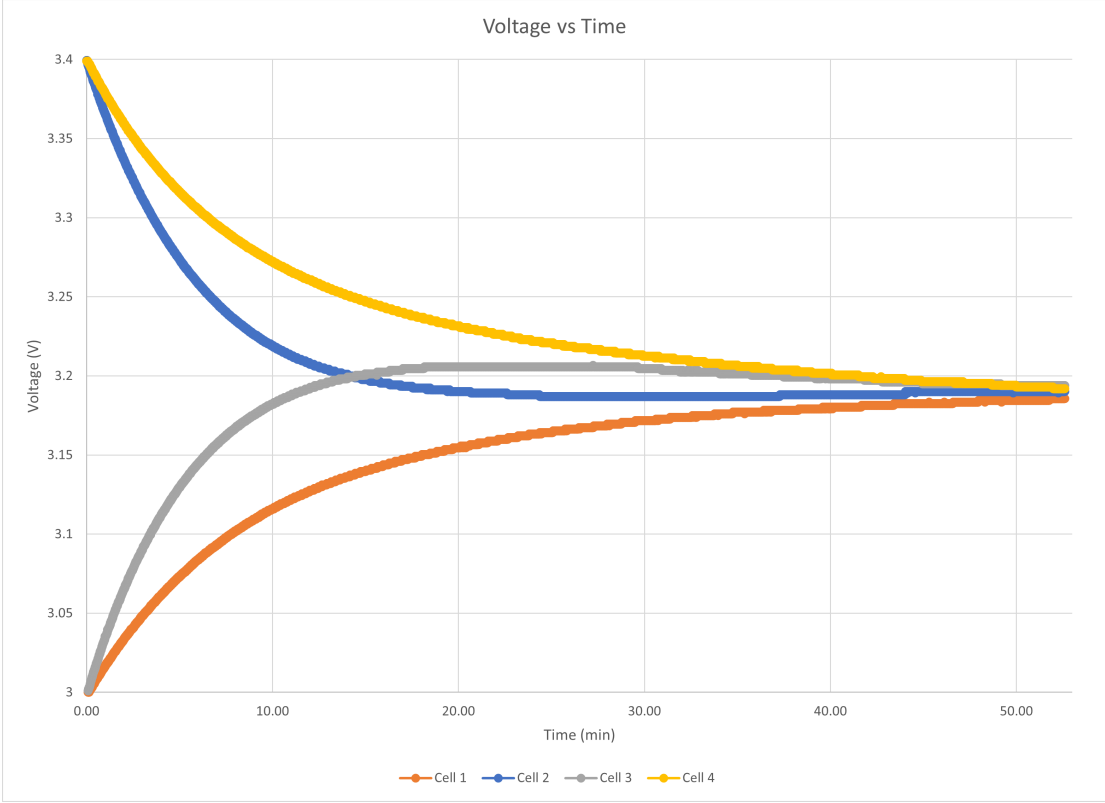Figure B-30: 2S N+P Thermal Test at $\Delta V = 0.6$ V

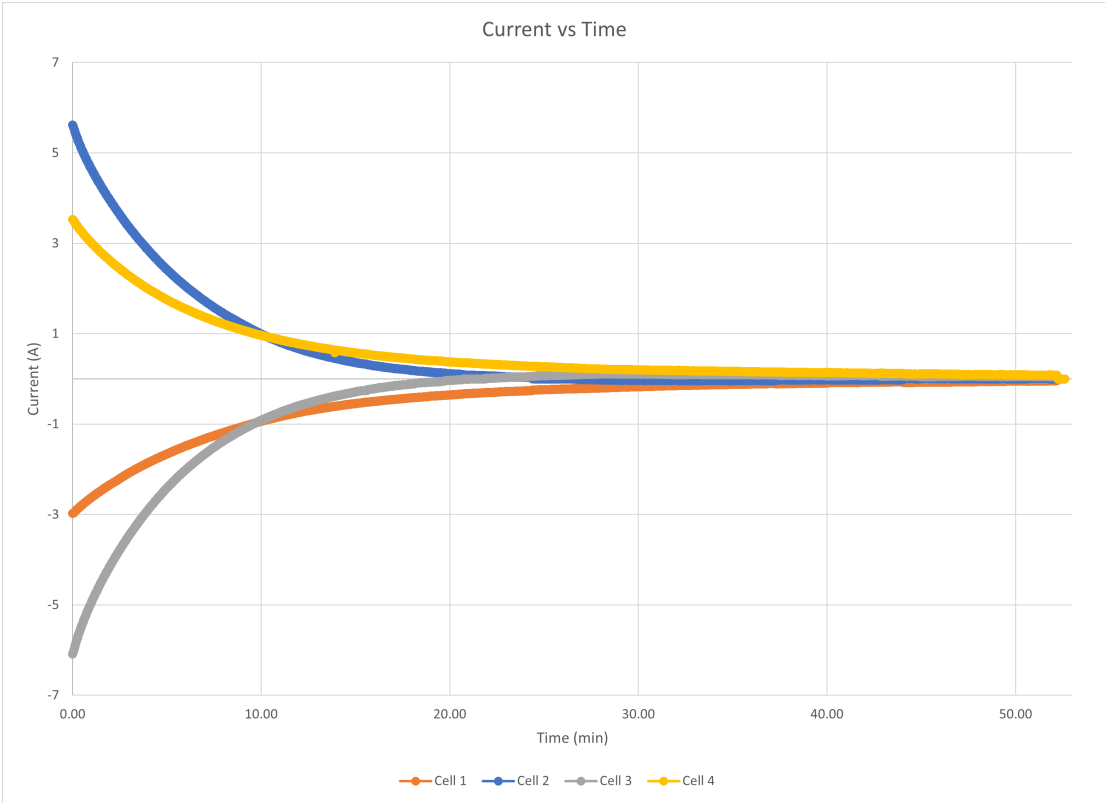Figure B-31: 4S Dynamic Balance Test 1 Cell Voltages

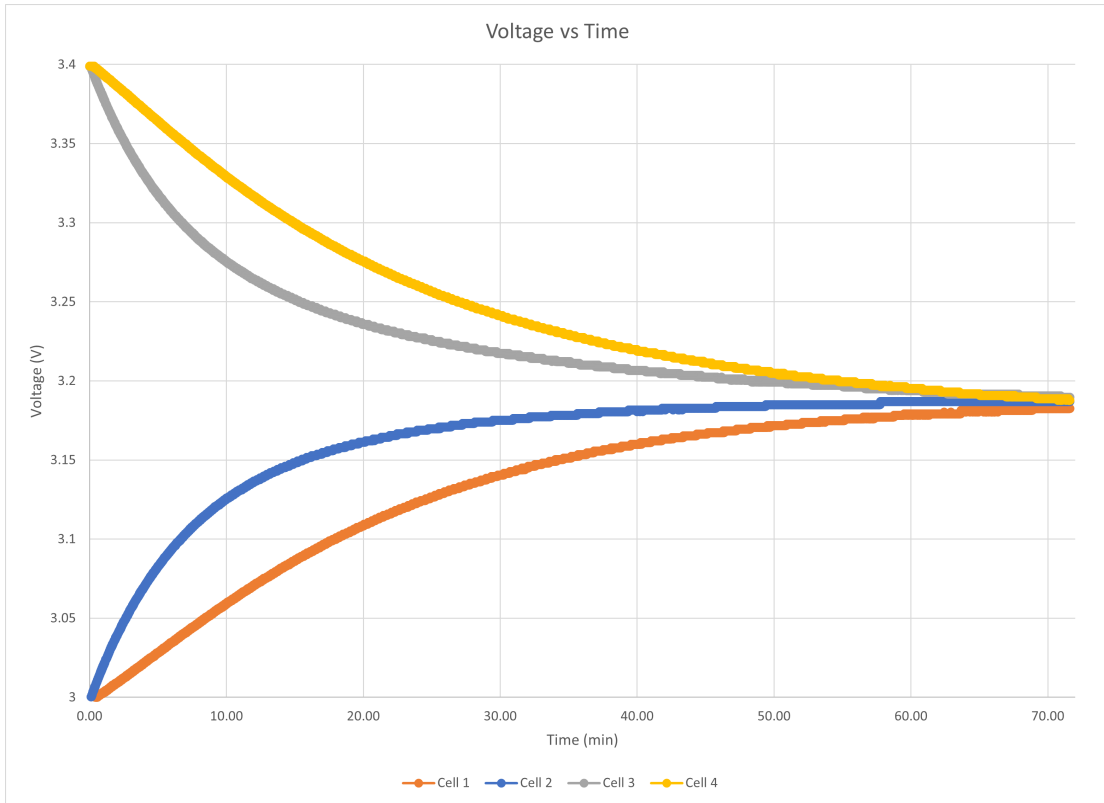Figure B-32: 4S Dynamic Balance Test 1 Cell Currents

Figure B-33: 4S Dynamic Balance Test 2 Cell Voltages
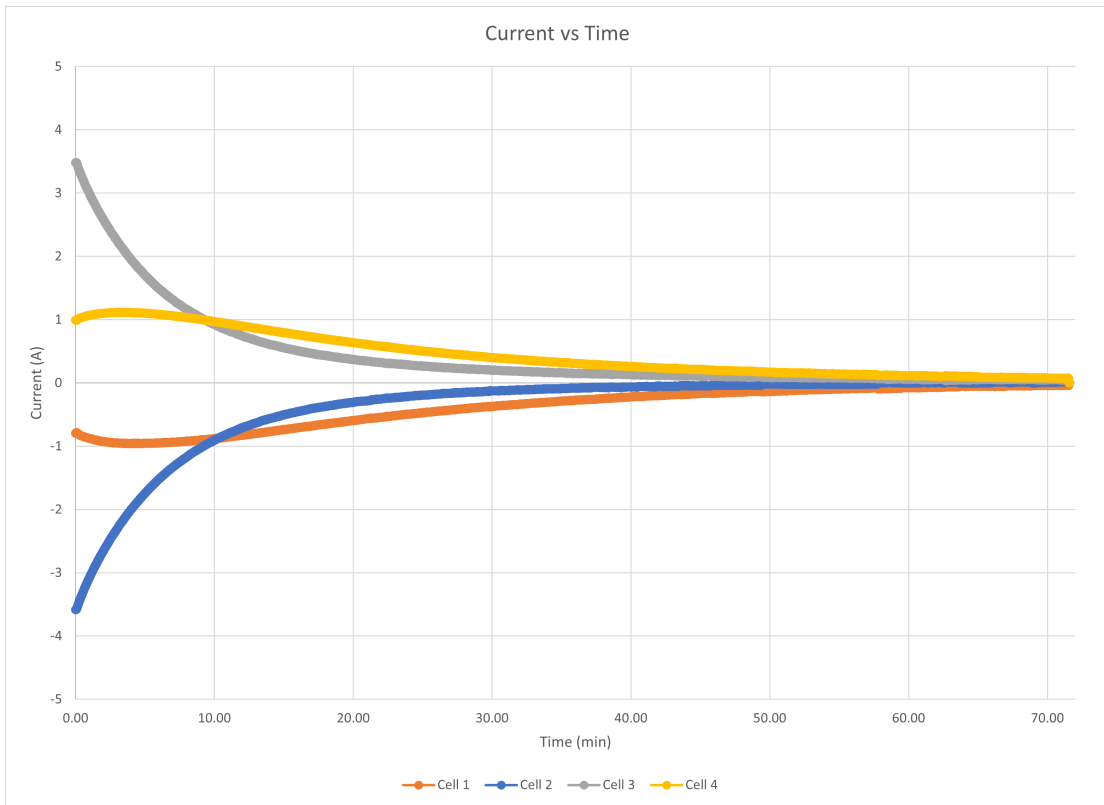

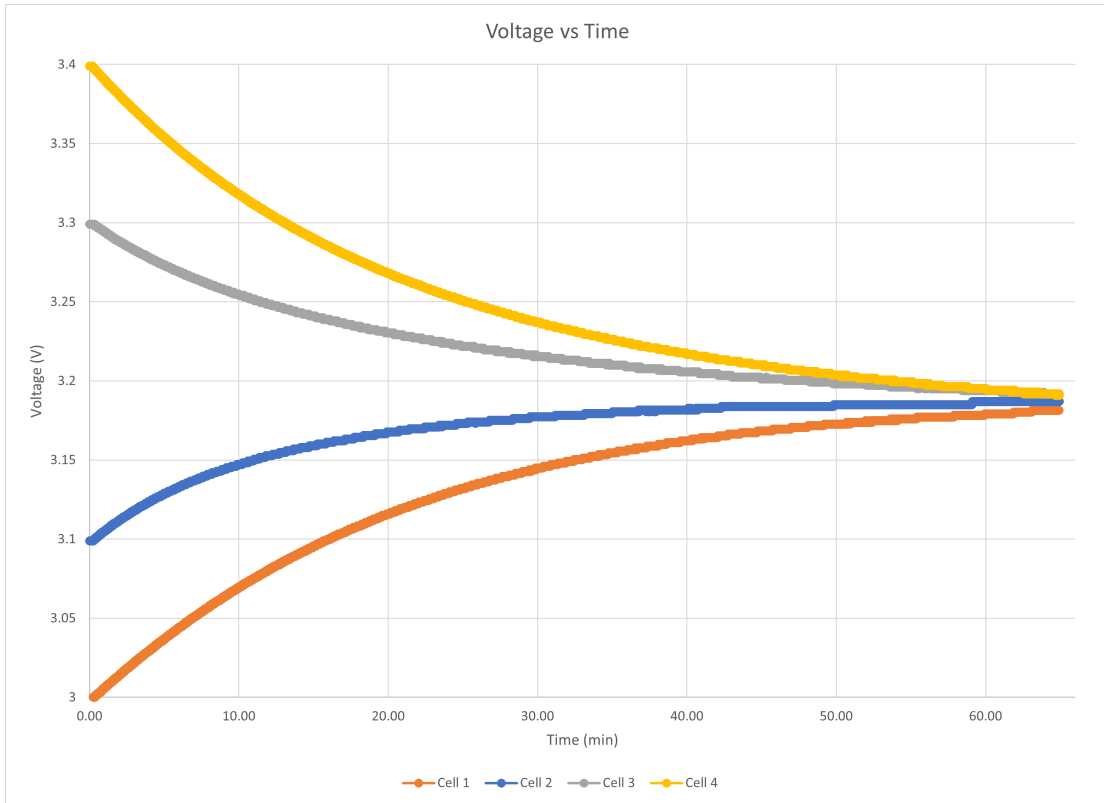Figure B-34: 4S Dynamic Balance Test 2 Cell Currents

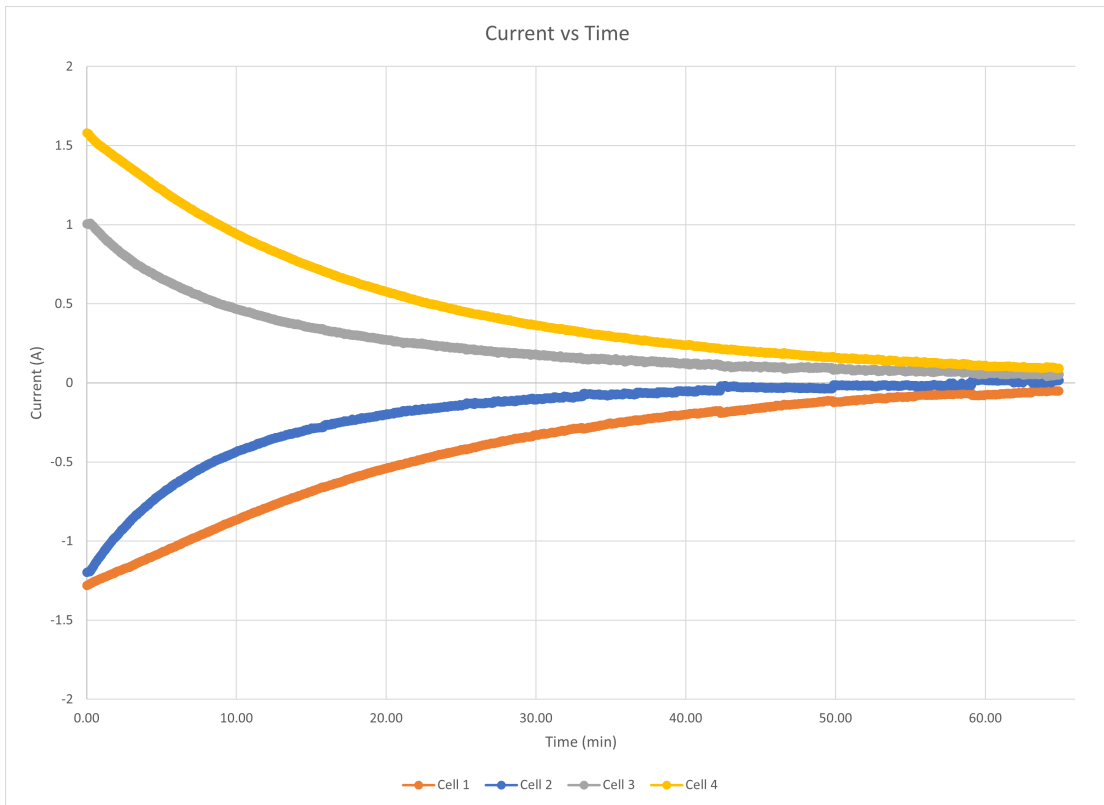Figure B-35: 4S Dynamic Balance Test 4 Cell Voltages

Figure B-36: 4S Dynamic Balance Test 4 Cell Currents
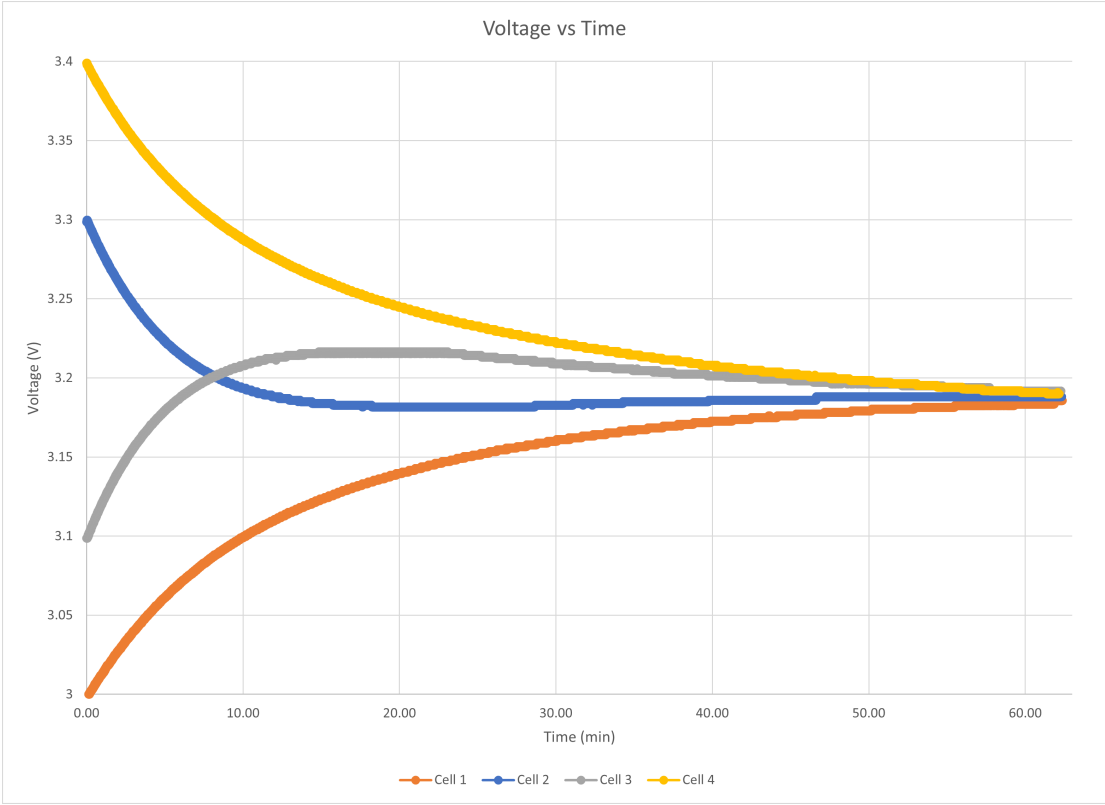
Figure B-37: 4S Dynamic Balance Test 5 Cell Voltages
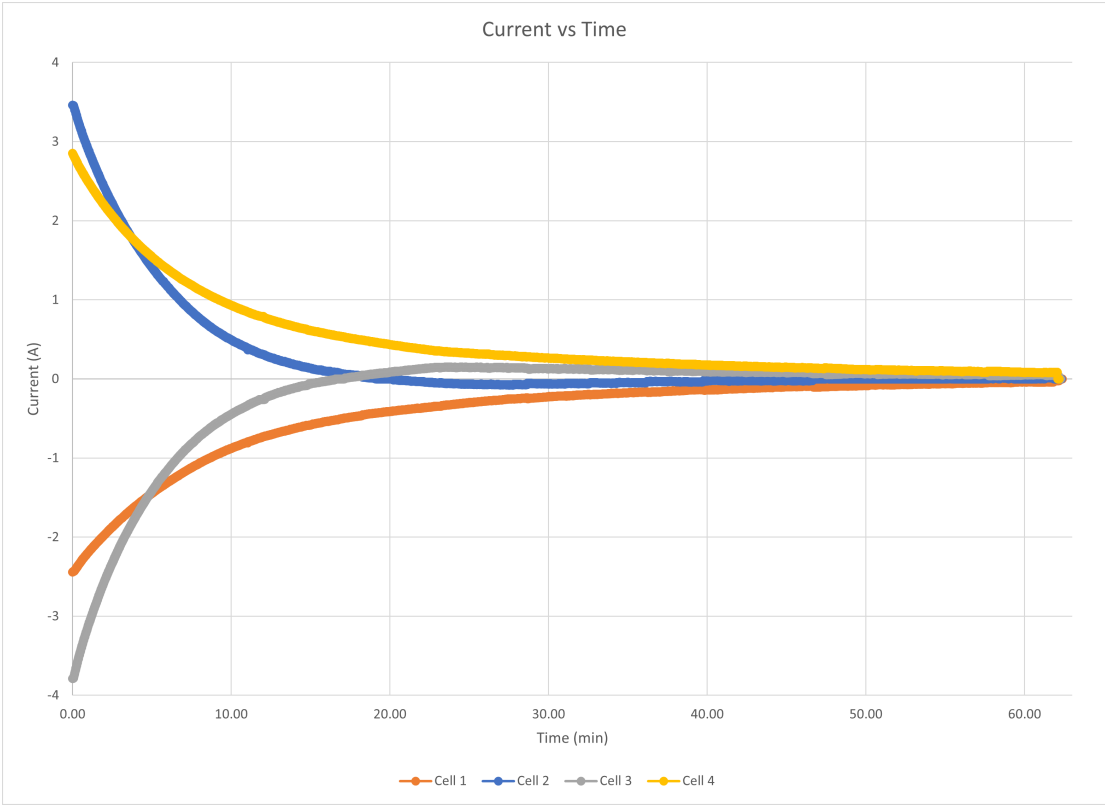
Figure B-38: 4S Dynamic Balance Test 5 Cell Currents

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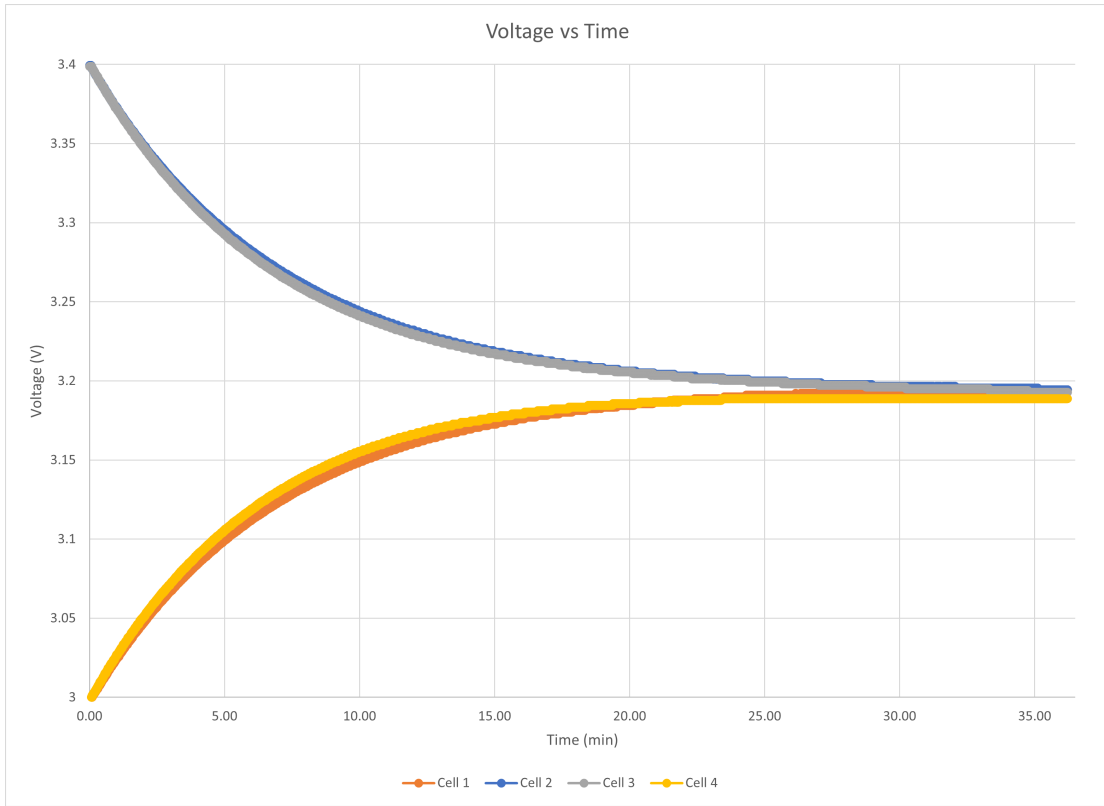
Figure B-39: 4S Dynamic Balance Test 6 Cell Voltages
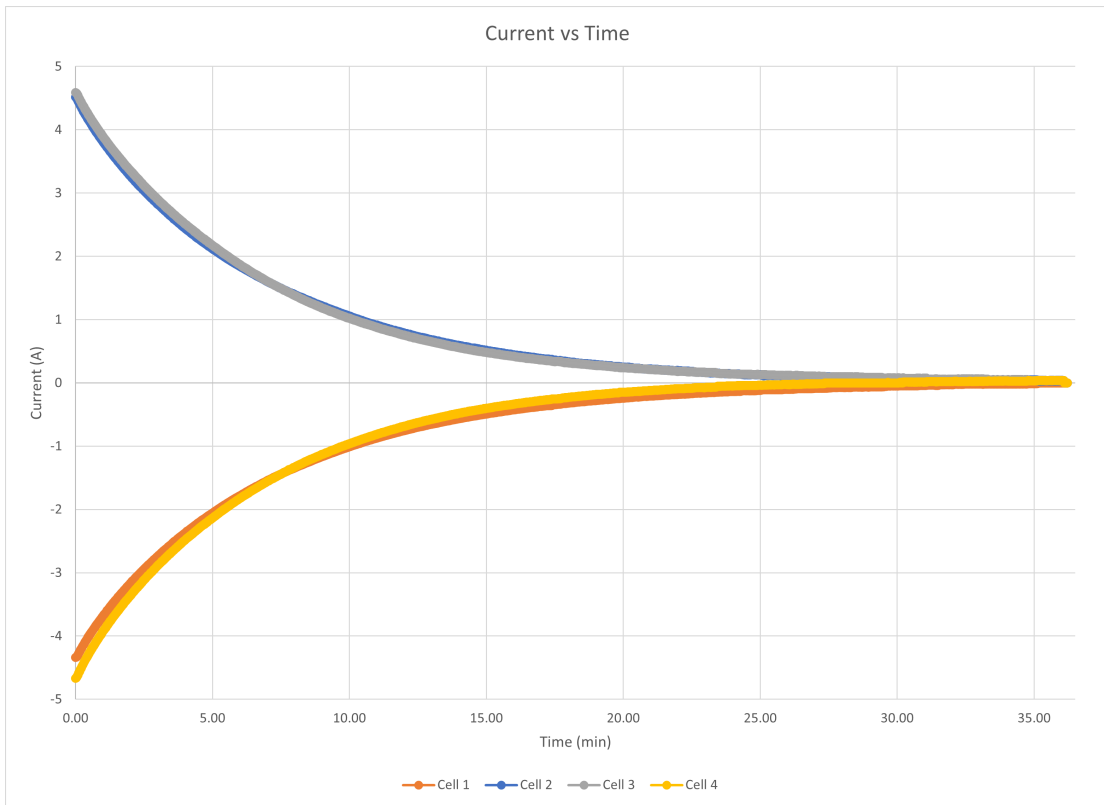
Figure B-40: 4S Dynamic Balance Test 6 Cell Currents

Appendix C

Equations

C.1   Principle of Virtual Work

Let V_k be the final state voltage of cell k. We define δq_k as the virtual charge displacement, Q_k as the generalized electromotive force associated with this displacement, N as the number of battery cells, and δW as the virtual work such that

$$\delta W = \sum_{k=1}^{N-1} Q_k \delta q_k = 0 \tag{C.1}$$

where $Q_k = V_k - i_{kj} R_{kj} - V_j$ for $j = k+1$. Assume the system of cells is in electrostatic equilibrium i.e. $i_{kj} = 0$ (no current flow). Thus,

$$Q_k = 0, \ \forall k \in \{1, 2, \ldots, N-1\} \tag{C.2}$$

Therefore, in equilibrium

$$V_1 = V_2 = \ldots = V_N \tag{C.3}$$

V_k is also constrained by

$$\sum_{k=1}^{N} V_k = V_{batt} \tag{C.4}$$

By (C.3) and (C.4), the end state for all cell voltages is given by

$$V_k = \frac{V_{batt}}{N} \qquad (C.5)$$

C.2 Equations of Motion

C.2.1 3S Equations of Motion

$$V_1(s) - i_{1,2}R - V_2(s) = 0 \qquad (C.6)$$

$$V_1(s) - i_{1,3}\alpha R - V_3(s) = 0 \qquad (C.7)$$

$$V_2(s) - i_{2,3}\beta R - V_3(s) = 0 \qquad (C.8)$$

$$V_1(s) - \frac{V_1(0)}{s} - \frac{I_1}{sC} = 0 \qquad (C.9)$$

$$V_2(s) - \frac{V_2(0)}{s} - \frac{I_2}{sC} = 0 \qquad (C.10)$$

$$V_3(s) - \frac{V_3(0)}{s} - \frac{I_3}{sC} = 0 \qquad (C.11)$$

$$i_1 + i_{1,2} + i_{1,3} = 0 \qquad (C.12)$$

$$i_2 - i_{1,2} + i_{2,3} = 0 \qquad (C.13)$$

$$i_3 - i_{2,3} - i_{1,3} = 0 \qquad (C.14)$$

C.2.2 4S Equations of Motion

$$V_1(s) - i_{1,2}R - V_2(s) = 0 \qquad (C.15)$$

$$V_1(s) - i_{1,3}\alpha R - V_3(s) = 0 \qquad (C.16)$$

$$V_1(s) - i_{1,4}\phi R - V_4(s) = 0 \qquad (C.17)$$

$$V_2(s) - i_{2,3}R - V_3(s) = 0 \qquad (C.18)$$

$$V_2(s) - i_{2,4}\alpha R - V_4(s) = 0 \qquad (C.19)$$

$$V_3(s) - i_{3,4}R - V_4(s) = 0 \tag{C.20}$$

$$V_1(s) - \frac{V_1(0)}{s} - \frac{I_1}{sC} = 0 \tag{C.21}$$

$$V_2(s) - \frac{V_2(0)}{s} - \frac{I_2}{sC} = 0 \tag{C.22}$$

$$V_3(s) - \frac{V_3(0)}{s} - \frac{I_3}{sC} = 0 \tag{C.23}$$

$$V_4(s) - \frac{V_4(0)}{s} - \frac{I_4}{sC} = 0 \tag{C.24}$$

$$i_1 + i_{1,2} + i_{1,3} + i_{1,4} = 0 \tag{C.25}$$

$$i_2 - i_{1,2} + i_{2,3} + i_{2,4} = 0 \tag{C.26}$$

$$i_3 - i_{1,3} - i_{2,3} + i_{3,4} = 0 \tag{C.27}$$

$$i_4 - i_{1,4} - i_{2,4} - i_{3,4} = 0 \tag{C.28}$$

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