Vacuum Transistors Based on III-Nitrides Field Emitter Arrays with Self-Aligned Gate

by

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B.S., Electrical Engineering, National Taiwan University (2015)
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Abstract

Vacuum electronics are promising future high-frequency and harsh-environment devices thanks to their scattering-free and radiation-robust vacuum channels. Field-emission vacuum transistors based on silicon and metals have been demonstrated over past 30 years, however the power consumption and long-term device stability are still issues. To further improve the field emission device performance and stability, III-Nitride semiconductors are attracting significant attention recently thanks to their engineerable electron affinities and high bonding energies. Ideally, the degenerately-doped n-type semiconductors with low electron affinities can have low work functions, leading to small electron Fowler-Nordheim tunneling barriers and thus low operating voltage and reduced power consumption. Moreover, materials with large bonding energies are expected to be more robust towards ion-bombardment-induced degradation. In spite of the great potential of III-Nitride vacuum transistors, there are still very limited transistor-level demonstrations with performance comparable to Si and metal-based field emitters.

This thesis aims to identify the key challenges of III-Nitride vacuum transistors and demonstrate new approaches to tackle these issues. First, GaN field emission diodes are studied to understand the basic device operation and the long-term stability of GaN emitter tips. Second, self-aligned-gate structures are developed on GaN field emitter arrays to demonstrate vacuum transistors with reduced operating voltages. The device performance is further improved by sharpening the field emission tips and optimizing device geometries. Third, N-polar GaN and AlGaN self-aligned-gate field emitter arrays are also fabricated and their material properties for field emission applications are investigated. Finally, a new technology to demonstrate fully-integrated III-Nitride vacuum transistors is discussed. This thesis work serves as a foundation for future high-frequency (above-100 GHz) and high-power III-Nitride vacuum electronics.

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Chapter 1

Introduction

1.1 Vacuum electronics

Semiconductor industry has been a driving force for tremendous amount of modern technologies and applications in nowadays daily life since the transistors were invented 75 years ago. Thanks to Moore's law in CMOS technology, personal computing, smart mobile devices, machine learning, artificial intelligence, and many other technologies have been made possible and accessible. However, Si-based CMOS technologies still have drawbacks in some specific applications, such as high-power and high-frequency electronics and harsh-environment applications.

On the other hand, though the vacuum electronics are already replaced by their solid-state counterparts in most systems, they are in principle better choices for high-power, high-frequency, and harsh-environment electronics [1–9]. In this chapter, a brief history of vacuum electronics and the basic operation mechanisms of field emission devices are firstly introduced. The motivation of using III-Nitride semiconductors as field emission devices is then discussed, and the structure of this thesis will be described in the end of this chapter.

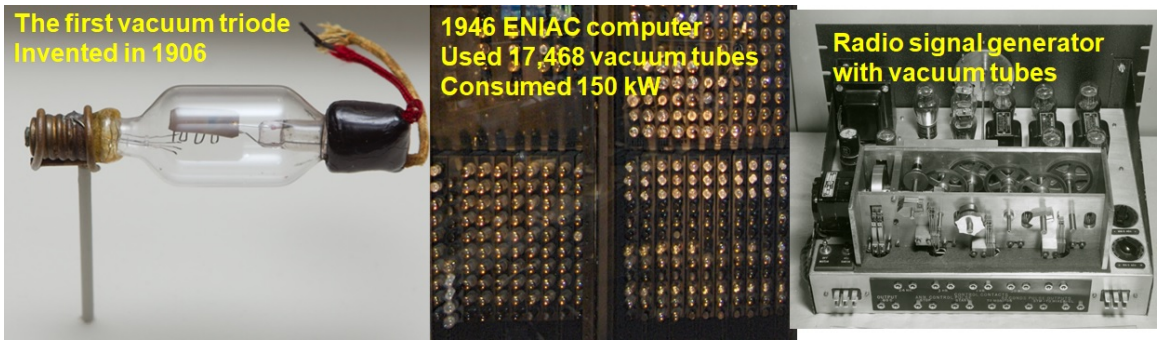


Figure 1-1: The three-terminal triode, early-stage computer (ENIAC), and radio signal generator based on vacuum tubes [1].

1.1.1 History of vacuum electronics

Before the solid-state electronics are invented, the logic switches were based on vacuum tubes (Fig 1-1), which are bulky and power-consuming. Because of these device properties, computers built in 1940s and 1950s were huge and consumed a lot of power (like a well-known ENIAC computer in Fig. 1-1). Besides the computation, vacuum tubes were also used for RF applications such as radio signal generator and amplifiers (Fig. 1-1) [1].

As the solid-state electronics are invented and developed over past 70 years, the vacuum tubes in logic switches and computers are firstly replaced by solid-state devices, such as NMOS and CMOS logic. The integrated circuits, combined with semiconductor foundries and fabrication technologies, made CMOS eventually the dominant technologies for most digital circuit systems. After the digital devices and circuits, many RF and power devices are also developed based on different semiconductors and vacuum tubes are gradually removed from those commercial fields. Nowadays, vacuum electronics mostly exist only in military, space, and some narrow fields of applications.

1.1.2 Advantages of vacuum electronics

While the solid-state electronics have been used in most applications, vacuum electronics have some intrinsic benefits over their solid-state counterparts. For example, the carriers transporting in the semiconductor channel can experience many kinds of

scattering (Fig. 1-2(a)). The phonon scattering due to the lattice vibrations at above-0 K temperature will always exist in solid-state channels, and the surface roughness, dangling bonds, and impurity in materials can cause additional coulomb scatterings. All these scatterings affect the overall carrier mobility or saturation velocity in a semiconductor channel.

On the other hand, the electron transportation in vacuum can be regarded almost like a scattering-free mechanism (Fig. 1-2(b)). If the electric field in vacuum channel is strong enough, the electron transportation can be modeled by simple equations:

$$d = \frac{1}{2}a\tau^2 + v_i\tau \tag{1.1}$$

$$a = \frac{qE}{m_e} \tag{1.2}$$

$$E = \frac{V_{Bias}}{d} \tag{1.3}$$

$$v = \sqrt{v_i^2 + 2\frac{q}{m_e}V_{Bias}} \tag{1.4}$$

where the d is transport distance, a is the electron acceleration velocity due to electric field (E), v_i is the initial electron velocity, q is electron charge, m_e is electron mass, and v is final electron velocity, assuming the velocity is not too high to break the Newtonian limit. Thus, the electron velocity in the vacuum channel can be much higher than the saturation velocities in semiconductor channels, which are usually at the order of 10^7 cm/s.

Besides the high electron velocity, the breakdown field in the vacuum channel in the high vacuum environments can also be higher than most semiconductors [10–12]. Therefore, based on these great properties and some assumptions, researchers have estimated the performance limits of different channel materials for power and high-frequency applications (Fig. 1-2(c)) [13]. It is proposed that the vacuum channel can surpass most semiconductors in high-power or high-frequency applications.

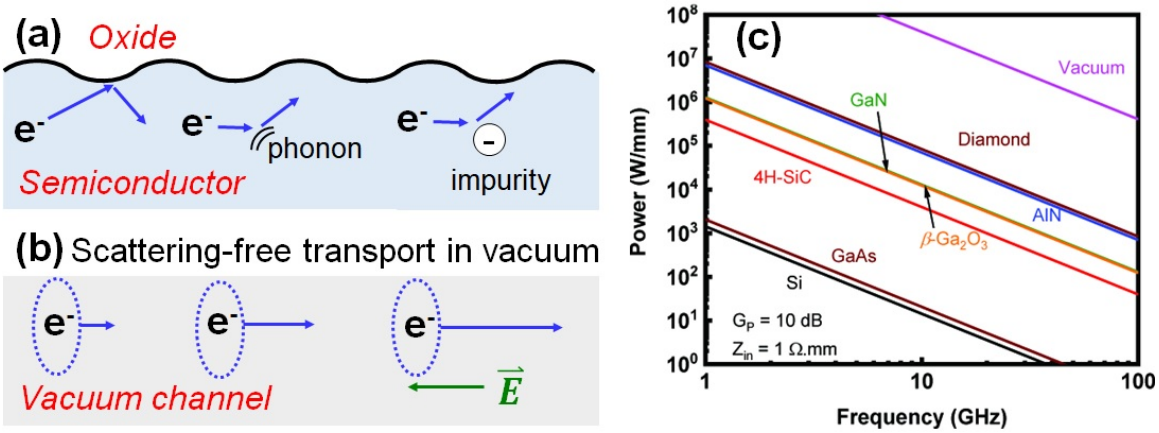


Figure 1-2: (a) Scatttering-affecting electron transport in the solid-state channel, (b) scattering-free electron transport in vacuum, and (c) the calculated power versus frequency based on Johnson's figure of merit (JFOM) of different materials [13] showing a significant gap in theoretical limits of performance between vacuum and semiconductor channels, reprinted with permission © 2020 IEEE. Copyright statement for (c) is in Appendix H.

1.1.3 Potential applications

As shown in Fig. 1-2(c), the vacuum electronics can be good candidates for above-100 GHz communication and power amplifiers. In fact, the traveling-wave tubes (TWTs), utilizing the interaction between a focused electron beam and RF signals, are used for above-100 GHz power amplification [3, 6, 7], which is an good example for high-frequency vacuum electronics. If the vacuum electronics can be integrated and fabricated in the semiconductor industry, they can be great devices for future high-frequency communications (Fig. 1-3(a)).

Moreover, as there is no materials or lattice atoms in the vacuum channel, many degradation or failure mechanisms happening in semiconductor devices in harsh environments can be reduced or avoided. For example, the radiation in space is a big concern for solid-state electronics used in space crafts and space stations. Different radiations, neutrons, and ions bombardment can degrade and break the semiconductor devices [14, 15]. On the other hand, the vacuum channels are expected more robust or immune to these damages, which makes them great future space electronics (Fig. 1-3(c)).

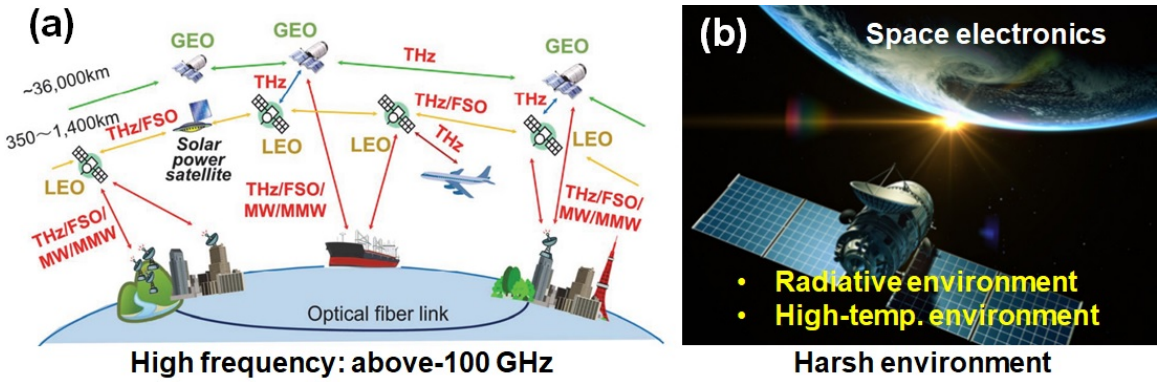


Figure 1-3: (a) Above-100 GHz and THz communication in the space [16] and (b) outer space electronics requiring radiation robustness and wide-range temperature stability [17]. Vacuum electronics are more robust toward radiation and high temperature degradation than conventional solid-state electronics.

1.2 Operation mechanism of vacuum transistors

In this section, the operation of the vacuum transistors will be reviewed to provide the general idea of the main operation mechanisms in the vacuum transistors: electron emission and transport in vacuum. Both electron emission and electron transportation in vacuum will be discussed.

1.2.1 Electron emission

The electron emission can be done through different mechanisms, such as thermionic emission, field emission, hot electron emission, and ferroelectric electron emission (Fig. 1-4(a)) [18–26].

Thermionic emission is the main electron emission mechanism for most of vacuum tubes since they are invented. In the thermionic emission, the electron source materials (emitters) are heated up to make some high-energy electrons have equal or higher energy than the work function of the materials, and these electrons can surmount the work function barrier and inject into vacuum (green arrow in Fig. 1-4(b)). The thermionic emitters can provide stable and high emission current when the device is ON. However, as the heating is necessary, the power consumption on heating reduces the energy efficiency and the thermal insulation required between emitters and other

(a)	Thermionic emitter	Field emitter	MIM tunnel emitter	Cesium-coated emitter	Ferroelectric cathode
Pros.	• High current • Stable (when ON)	• Scalable • power efficient	• Simple structure	• High current	• Simple structure
Cons.	• Bulky • Power waste	• Stability	• Low efficiency	• Stability • UHV requirement	• Scalability?

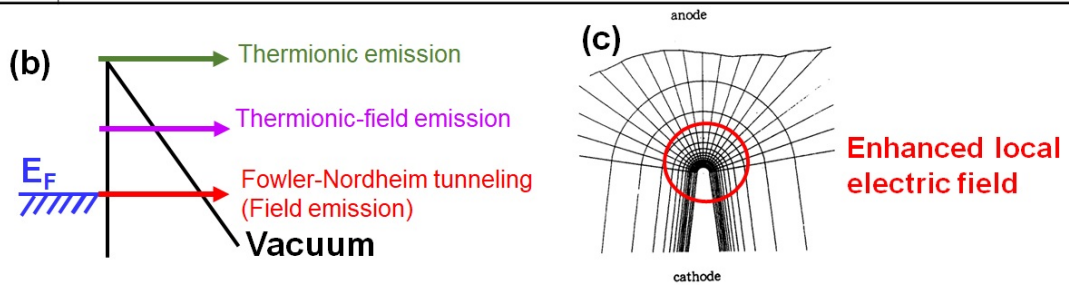


Figure 1-4: (a) Comparison of some electron emission devices, (b) energy band diagram showing different electron emission processes, and (c) locally enhanced electric field on a sharp nanostructure, which is suitable as field emitter tip [19]. Figure (c) is reprinted with permission © 1991 IEEE (Appendix H). The positions of different arrows in (b) indicate different energy levels of emitting electrons.

parts makes these devices bulky and hard to integrate for large-circuit implementation (as ENIAC computer in Fig. 1-1).

Besides thermionic emission, there are different mechanisms for electron emission (Fig. 1-4(a)). Compared to the thermionic emission, other mechanisms do not require heating on the emitters, thus regarded as "cold emission." The field emitters use strong electric field to reduce the tunneling distance from the solid materials to the vacuum level (Fig. 1-4(b)). With nanostructures such as nanowires or nanopyramids, the local electric field can be enhanced on the sharp region to induce strong enough electric field and thus relax the requirement of high bias voltage (Fig. 1-4(c)) [19]. The field emitters are theoretically able to provide current densities comparable with or higher than the thermionic emitters. Furthermore, since the thermal insulation is not a requirement in field emitters, these devices can be scalable and more energy efficient. However, issues, such as self-heating-induced thermal runaway and ion bombardments, are still potential challenges and the stability is still a general concern for these field emitters [27, 28].

The hot-electron emission such as metal-insulator-metal (MIM) tunnel emitters is also demonstrated for electron emission. In MIM tunnel emitters, the top metal

terminal is positively biased to make electrons tunnel from the bottom metal through the insulator and some electrons can inject into the vacuum level of the top metal before they lose kinetic energies. There are different demonstrations on this type of devices, such as graphene-oxide-semiconductor emitters [22–24]. While the device structures of MIM tunnel emitters are usually simpler than field emitters, the power efficiency of MIM tunnel emitters is usually lower as electrons can lose energies in both insulator and top metal layers and then flow into the top metal layers as a leakage current (Fig. 1-4(a)).

As the electron emission is a mechanism happening on the material surface, the modified surfaces can provide additional advantages for electron emission devices. For example, Cesium (Cs)-coated surface can form a dipole at the surface of the material, which lowers the surface barrier for electron emission into vacuum [29, 30]. The surface energy barrier can be reduced to 1 eV in some reports [31]. However, highly-reactive cesium can still react with gases in the environment and loses the surface-dipole property for work-function lowering. Furthermore, if the fields at the surface are large, the electromigration can happen on these cesium atoms to cause the lose of Cs-coated surface. Therefore, though Cs-coated emitters can provide high current and efficiency, the stability and ultra-high vacuum (UHV) requirements are main issues for these devices (Fig. 1-4(a)).

Another electron emitter type is the ferroelectric emitter. Different from other cold emission mechanisms mentioned above, this type of emitters uses the spontaneous dipoles in the ferroelectric materials. By applying the alternating fields on the ferroelectric materials, the dipoles can be flipped and the electrons at the surface due to the spontaneous polarization can then be repelled by the flipped dipoles and emit into the vacuum [25]. The structures of these ferroelectric emitters are simple, but they are mostly demonstrated on the bulky ferroelectric ceramics, and thus their scalability as electronics is still a main challenge (Fig. 1-4(a)).

Besides the electron emitters mentioned above, there are still different emitters in literature, such as negative-electron-affinity (NEA) emitters based on hydrogen-terminated diamonds [32, 33]. In this thesis work, we focus on field emission de-

vices combined with the III-Nitride semiconductors to demonstrate high-performance state-of-the-art GaN and AlGaN field emitters as vacuum transistors. Therefore, the operation mechanisms of field emission and electron transport in the vacuum will be discussed in more details.

Field emission

As briefly described above, the field emission requires strong enough electric field to reduce the tunneling distance for electron to tunnel from the fermi level (E_F) of the materials into vacuum level without the need of heating process. The field emission process was firstly modeled using the Fowler-Nordheim (F-N) equation with an approximation on image-force-induced barrier lowering:

$$I_{FN} = cE^2\ exp(\frac{-d}{E}) \tag{1.5}$$

$$c \cong \frac{\alpha A}{1.1\phi} exp(\frac{B(1.44\times10^{-7})}{\phi^{0.5}}) \tag{1.6}$$

$$d \cong 0.95B\phi^{1.5} \tag{1.7}$$

where I_{FN} is the field emission current, E is the electric field at the emission surface (unit: V/cm), α is the emitting area, ϕ is the work function, and A & B are constants (A $\cong 1.54\times10^{-6}$ and B $\cong 6.83\times10^{7}$) [34]. In the gated field emitters, if the electric field at the emitter tip surface is dominantly controlled by the gate-emitter voltage (V_{GE}), then the equations (1.5) - (1.7) can be expressed as:

$$I_{FN} = a_{FN}V_{GE}^2\ exp(\frac{-b_{FN}}{V_{GE}}) \tag{1.8}$$

$$a_{FN} = \frac{\alpha A\beta^2}{1.1\phi}\ exp(\frac{B(1.44\times10^{-7})}{\phi^{0.5}}) \tag{1.9}$$

$$b_{FN} = \frac{0.95B\phi^{1.5}}{\beta} \tag{1.10}$$

where the electric field (E) in equation (1.5) can be expressed as $\beta \times V_{GE}$. The β is the gate-emitter field factor (unit: cm^{-1}). In gated field emitters (like one in Fig. 1-5(b)), experimentalists usually use the equation (1.8) or the similar form to analysis

the device behavior. For example, based on equation (1.8), we can get

$$ln(\frac{I_{FN}}{V_{GE}^2}) \quad = \quad ln(a_{FN}) - \frac{b_{FN}}{V_{GE}} \tag{1.11}$$

and a plot of $ln(\frac{I}{V_{GE}^2})$ versus $\frac{1}{V_{GE}}$, which is called Fowler-Nordheim (F-N) plot. If a negative-slope straight line is observed in the F-N plot, the device operation in this region is believed to be dominated by field emission. However, these equations are based on an approximation of an image-force-induced barrier lowering with a suitable approximation range. This approximation only works in the region of $0 <$ y < 1, where y $= 3.79 \times 10^{-4} \ \frac{E^{0.5}}{\phi}$. Therefore, if the electric field is too high or the work function is too low, this approximation will fail [34]. On the other hand, if the image charges are not taken into consideration, the emitting area will usually be overestimated for more than 1 order of magnitude [35].

Since the last two decades, there have been discussion and arguments from theorists to use better models, such as different Murphy-Good approximation models, to interpret the experimental results [36–40]. Recently, a paper combining the experimental study of a tungsten field emission tip with different approximation models reports that the image charge correction is necessary and an additional caution should be made for reported low-work function field emitters [35]. As there are in fact three variables, field factor β, emitting area α, and work function ϕ, in equation (1.8), it is not possible to get precise numbers for all of them from a transfer characteristics I-V measurement only. Researchers proposed different approaches and models to interpret the experimental results, while the models are either too complex to analyze the experimental data or they do not match with the experimental results well [35]. Therefore, in practice, the field factor or the work function is usually assumed a fixed value based on the electrostatic simulation or the measured material properties, and the other two parameters are then calculated accordingly. Though there are issues, such as tip-shape changing or the surface absorption/desorption during operation, can affect the values of β and ϕ [35], it is still a dominant approach among the experimentalists.

There are some ways to help reduce the uncertainty or clarify the communication between different experimental results, such as the study of the multiple I-V sweeps of a field emitter to confirm if the tip-shape changing or work function modification happens. As results, when analyzing the experimental data, the assumption on field factor or work function should be made carefully. For instance, if the field emitters are made of semiconductors, the electric field penetration into the semiconductor surface should be taken into consideration when simulating for the field factor (β). Since this thesis work aims to experimentally demonstrate III-Nitride field-emitter-based vacuum transistors, the I-V characteristics data are mostly interpreted by a F-N tunneling model with an image-force-barrier-lowering approximation (equation (1.8)) [34]. Though the field factors or work functions are not pre-known values, the assumption is made based on electrostatic simulation generated from the device cross-sectional scanning electron microscope (SEM) images or based on measured values reported in literature.

1.2.2 Transport in vacuum

In the vacuum electronics, electron emission is the first part of the carrier transportation. To make an analogy, the electron emission in the vacuum transistors is like the carrier injection from the source to the channel in MOSFETs. Therefore, after the electron emission, the electron transport in vacuum is another important part for the current conduction (as shown in Fig. 1-5(a)).

When the electrons emit from solid materials into vacuum, they can form an electron cloud with negative charges when transporting in vacuum. While the external electric field can accelerate the electrons moving away from the emission sites, the electron cloud would provide the repel force for newly-emitted electrons back to the emission sites (Fig. 1-5(a)). If the external electric field is not strong enough, the amount of electron current will be limited by the electron cloud exists in vacuum. This phenomenon is called as space-charge limit [41, 42].

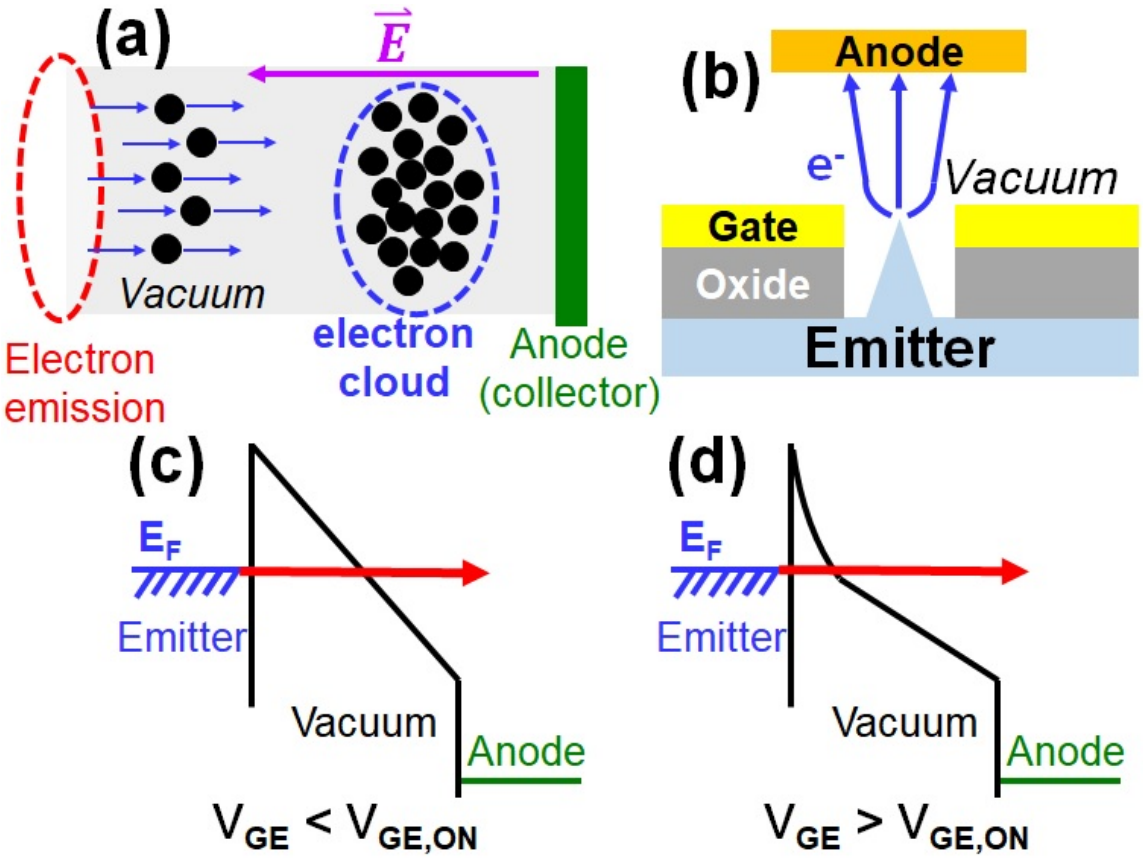


Figure 1-5: (a) The electron transport in vacuum after emission, (b) a geometry of a gated field emitter device, and the energy band diagrams from the emitter to the anode (c) at OFF state and (d) at ON state. The electron cloud in the vacuum shown in (a) can block more electrons from approaching anode when it reaches the space-charge limit in vacuum.

Space-charge limit

The space charge limit of electron conduction in vacuum is first investigated in thermionic vacuum tubes, which is known as Child's law, proposed by Clement D. Child. The space-charge-limited current flowing in a diode, which is composed of two parallel planar electrode and the vacuum in between, can be expressed as:

$$J = \frac{4\epsilon_0}{9}\sqrt{\frac{2e}{m_e}}\frac{V^{1.5}}{d^2} \tag{1.12}$$

where ϵ_0 is the dielectric constant of vacuum, e is the electron charge, m_e is the electron mass, V is the bias voltage between two parallel planar electrodes, and d

is the distance between these two electrodes [42, 43]. However, in the case of field emitters, the emitted electrons can have non-zero velocity when they transport into the vacuum channel with space charge; therefore, a modification on space-charge-limted current is necessary. In late 20th century, the space-charge-limited current with a non-zero initial carrier velocity is proposed:

$$I = \frac{2\epsilon_0 m_e}{9e}\left(\frac{v_i^{\frac{3}{2}} - (v_i^2 + \frac{2eV}{m_e})^{\frac{3}{4}}}{d}\right)^2 \tag{1.13}$$

where the v_i is the electron initial velocity [44].

In the transfer characteristics measurement of gated field emitters, the anode-emitter bias (V_{AE}) is kept high enough to prevent the electron current from hitting the space charge limit. In this case, the energy band diagrams of the field-emitter-based vacuum transistors can be drawn for both OFF state (Fig. 1-5(c)) and ON state (Fig. 1-5(d)). As long as the electron current in vacuum does not reach the space-charge limit, the emission current can be expressed by equation (1.8) to extract parameters such as the field factor and emitting area.

On the other hand, when the output characteristics of gated field emitters are measured, the electron emission is still mostly controlled by the gate-emitter voltage (V_{GE}), but the anode current (collector current) (I_A) can be limited by the space charge if V_{AE} is low. When the space-charge limit is reached, the additional amount of emitted electrons will be repelled to the gate by the electron cloud in vacuum and become the gate leakage. Therefore, in the output characteristics, the operation is separated into two regions: space-charge-limited region and field-emission-limited region. The field emission current has been studied and modelled, while the space-charge-limited region of the field-emitter-based vacuum transistors is still an ongoing task for device modelling. For example, basic space-charge-limited current is proposed based on the two-parallel electrodes structure, while the field emitters usually have more complex 3D structures. The electric field in the 3D space of vacuum can be more complicated, leading to difficulty in modelling space-charge limit in gated field emitters.

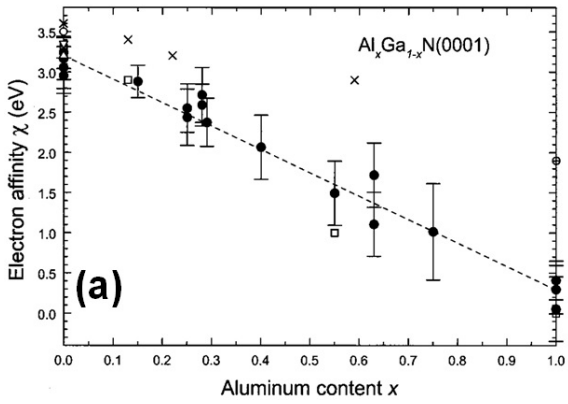
1.3 III-Nitride semiconductors for field emission

There have been many materials used as field emitters in past decades since the semiconductor industry became mature in fabrication technologies. For example, Si gated field emitters have been demonstrated since 1990s thanks to the capability of oxidization process of Si tips for nanometer-level sharpness and mature Si process [45]. As mentioned in section 1.2.1 and in Fig. 1-4(c), the local electric field can be enhanced based on the geometry of the emitter tip. Besides Si gated field emitters [13, 46–49], metal field emitters, such as Mo Spindt-type gated field emitter arrays, were also demonstrated [34, 50–53]. Additionally, carbon-based field emitters such as carbon-nanotube (CNT) field emitters and diamond gated field emitters were reported, too [54–56].

Different materials' field emitters have their own pros. and cons. Mo Spindt-type gated field emitters have the simplest fabrication process, but the stability can be an issue for metal field emitters due to low bonding energy. Si gated field emitters are demonstrated with mature technologies in Si industry, but the fabrication is more complex than metal field emitters and the performance is not better than metal counterparts. CNT devices theoretically have high aspect-ratio and thus reduced operation voltages, while the experimental results do not show clear better performance than Si and metal field emitters. Diamond gated field emitters have good thermal conductivity for heat dissipation and can potentially provide the negative-electron-affinity (NEA) surface for field emission, but the fabrication of diamond devices can be more difficult.

1.3.1 Advantages of III-Nitride material properties

Since late 20th century, III-Nitride semiconductors, such as GaN and AlGaN, have been developed and demonstrated for broad fields of electronics and optoelectronics, such as power electronics, high-frequency amplifiers, and high-efficient light emitter diodes (LEDs). In past two decades, researchers start looking into the potential applications of III-Nitrides on field emission devices. Compared to metal and Si field



(b)	Electron affinity (eV)	Bond energy (eV/atom)
Si	4.05	4.63
GaAs	4.07	6.5
SiC	3.6 (4H) 4.0 (6H)	6.29
GaN	3.8 (Ga-polar) 3.3 (N-polar)	8.9

Figure 1-6: (a) The relation between the electron affinity and the Al composition in the metal-polar (0001) AlGaN alloy, reprinted from [57], with the permission of AIP Publishing (Appendix H), and (b) the electron affinities and bond energies of different semiconductors [58–62]. The low-electron-affinity semiconductors can potentially build field emitters with low electron emission barrier, leading to low operating voltage or high emission current.

emission devices, III-Nitride semiconductors possess some good material properties for field-emitter-based vacuum transistors.

Engineerable electron affinities

First of all, the electron affinities of III-Nitride semiconductors are reported related to the Al composition of the AlGaN alloy (Fig. 1-6(a)) or the lattice orientation (Fig. 1-6(b)) [57,58]. The electron affinity of (0001) c-plane GaN is reported between 3 and 4.5 eV, and the (0001) c-plane AlN surface is reported to have electron affinity around or below 1 eV [63]. It should be noted that the experimental values of electron affinity on reactive AlN surfaces vary between 0 and 2 eV since the surface is vulnerable to oxidization and is affected by other surface properties [57, 63–66]. Moreover, an experimental work also reports that the electron affinity of N-polar (000-1) GaN surface is lower than the one of Ga-polar (0001) GaN surface (Fig. 1-6(b)) [58]. Some work also reported that the electron affinity of the N-polar AlN is lower than the one of Al-polar AlN [67]. Ideally, if the n-type semiconductor is degeneratedly doped, the work function can be close to the electron affinity of the material since the Fermi level (E_F) is close to the conduction band (E_C). Therefore, the low-electron-affinity

III-Nitride semiconductors can potentially have low work function for field emission to provide high emission current or low operation voltages.

Additionally, the polarization properties and large piezoelectric constants in III-Nitride semiconductors provide additional room for improvement such as polarization-induced doping and polarization-induced-electric-field engineering. With proper design on epitaxial structures, work with low effective electron affinity was demonstrated on InGaN/GaN field emitter pyramids [26].

High bonding energies

Secondly, the strong ionic bonding between group-III atom (such as Ga and Al) and the nitrogen atom provides a strong bond energy in III-Nitride semiconductors. As shown in Fig. 1-6(b), the bond energy of GaN is clearly higher than many conventional semiconductors [60–62]. Since there is strong electric field on the emitter tip surface during operation, ion bombardment due to the ionization of residual gases in the vacuum chamber is usually regarded as potential degradation and failure mechanisms for field emitters [68, 69]. If the ion bombardment is a concern of device stability, the high-bond-energy materials can be more stable under potential physical ion bombardment than the materials with low bond energies.

1.3.2 Prior work in literature

There have been great amount of work on III-Nitride materials for field emission devices. Many efforts have been especially spent on the growth of GaN nanostructures as field emitters [70–77]. These growth experiments and study are "bottom-up approaches," whose focuses are growing high-aspect-ratio GaN nanostructures for enhanced electric fields for field emission. Though many different approaches such as metal-organic chemical vapor deposition (MOCVD), chemical vapor deposition (CVD), and molecular beam epitaxy (MBE) demonstrated for two-terminal GaN field emission diodes, most of those nanostructures are hard to be integrated with gate structures because of the random growth directions or non-uniform nanostruc-

tures [72–77]. There are some work demonstrating orderly well-controlled nanostructure growths, while there is limited demonstration on gated field emission devices [71], and most efforts were still only spent for two-terminal diode structures [70]. In order to demonstrate high-performance GaN and AlGaN field emitters as vacuum transistors, the self-aligned-gate structures and the well-controlled process for III-Nitride nanostructure formation are both critical. Although the bottom-up approach can provide additional room for improvement by properly designing the epitaxial structures [26, 71, 78, 79], we focus on different approach, "top-down approach," to demonstrate the generally missing part, self-aligned-gate structures for three-terminal III-Nitride vacuum transistor demonstration.

1.3.3 Challenges of III-Nitride vacuum transistors

To demonstrate III-Nitride field-emitter-based vacuum transistors, there are two main challenges to be tackled: the self-aligned-gate structure and the well-controlled process of III-Nitride nanostructure formation.

First of all, the self-aligned-gate structures have been demonstrated for Si, diamond, Mo, and Spindt-type gated field emitter arrays. The main advantages of self-aligned-gate structures are the relaxation of difficult lithography alignment and the reduction of bias voltage requirement between gate and emitter. Compared to the bottom-up approach, the top-down one can form orderly nanostructures, which can be easier for the process development and integration for the self-aligned-gate structures. Furthermore, the GaN vertical FinFETs for power applications [80, 81] have been demonstrated, which can be a reference for the initial process development.

Secondly, the process for III-Nitirde nanostructure formation is also critical. There are works demonstrating different etching process on GaN and AlGaN, such as photoelectrochemical (PEC) etching on GaN, wet-etching on GaN and AlGaN, and dry etching on GaN and AlGaN [82–87]. However, most of the work demonstrated structures with above-100-nm dimensions. As mentioned in section 1.2.1, the electric field can be enhanced on nanometer-sharp tips. Therefore, the way to reproducibly fabricate uniform sub-50 nm III-Nitride vertical nanostructures is necessary for the success

of the high-performance III-Nitride field-emitter-based vacuum transistors.

1.4 Structure of this thesis

The contents of this thesis are separated into 5 chapters, conclusion and future work, and a few appendices.

Chapter 2 focuses on the demonstration of two-terminal GaN field emitter diodes with a top-down approach. Prior work on GaN field emitters with different approaches are firstly discussed. Our own approach is then discussed and reported. With the top-down approach, the orderly uniform field emitter arrays are demonstrated and the basic field emission behavior is confirmed. As the two-terminal structures do not consist any gate stacks or other materials than emitters, these simple structures are great candidates to study long-term stability of GaN field emitters.

Chapter 3 demonstrates the self-aligned-gate structures on GaN vertical nanowires (NWs). The reproducible process is developed and demonstrated in the first generation of our GaN self-aligned-gate field emitter arrays (SAGFEAs). The drive current density is comparable to the values of two-terminal GaN field emitter diodes reported in literature, the operating voltage is significantly reduced, and the gate-modulation of current conduction is achieved thanks to the self-aligned-gate structures.

Chapter 4 focuses on improving the GaN SAGFEAs' performance by investigating the issues and failure of the prior generations of devices. The uniformity and reproducibility of vertical nanostructures are improved by changing field emitter shapes from NWs to nanopyramids. The wet-based digital etching (DE) is then developed to improve the nanopyramid-based GaN SAGFEAs. The emitter pyramid tip width can be shrunk from 40 nm to below 20 nm by this wet-based DE process. The further improvements are made by the modification of the device geometry. The most recent GaN SAGFEAs show state-of-the-art performance for both operating voltage and drive current density. The best GaN SAGFEA has higher current density than the state-of-the-art Si SAGFEAs in literature at the same bias voltage.

Chapter 5 demonstrates SAGFEAs based on other III-Nitride semiconductors,

such as N-polar GaN and different AlGaN materials. Theoretically, N-polar n^+ GaN and high-Al n^+ AlGaN semiconductors have lower electron affinities than the one of Ga-polar GaN, and the performance improvement is thus expected. However, since the process flow was not optimized for N-polar GaN and high-Al AlGaN semiconductors, some issues during fabrication are observed and the device performance is also affected. Moreover, the measured work functions of AlGaN materials are much higher than theoretical values of electron affinity. Therefore, more work needs to be done in the future to further improve these III-Nitride SAGFEAs.

Chapter 6 discusses different topic for the vacuum transistors. In order to demonstrate integrated circuits or applications based on field-emitter-based vacuum transistors, the integration of anode terminal is necessary. The anode terminals in the field emitters are like drain terminals in the MOSFETs. Therefore, in chapter 6, the efforts to integrate anode structures for fully-integrated vacuum transistors are discussed. The preliminary study is also conducted to understand the effect of integrated anode structures on the device performance.

Chapter 7 includes both conclusion and the discussion of future work that can be done to further improve the vacuum transistor performance and to demonstrate real applications in high-frequency, high-power, or harsh-environment fields.

Appendices contain developed process flows, different critical etching steps and their experiments, the measurement procedure of these SAGFEAs, and other work during the PhD research which does not fit in this thesis contents.

Chapter 2

Two-terminal GaN field emission diodes

2.1 Prior work in literature

As mentioned in section 1.3.2, there have been demonstrations of III-Nitride semiconductors field emission devices since the last decade in the 20th century. The experimental results of a few GaN field emission devices are summarized in Fig. 2-1 [70–79, 88–105]. A lot of GaN field emitters were formed by the "bottom-up approach" for high-aspect-ratio nanostructures. These GaN field emission devices are mostly two-terminal diodes because of difficulties in gate-integration process for these non-uniform nanostructures. Therefore, the operating voltages of these GaN field emitters are mostly in the range from 200 V to above 1000 V. Although the limitation of two-terminal device scheme and the high operating voltages are main challenges for the practical applications using III-Nitride field emission devices, the analysis on two-terminal diodes is much less complex, and this scheme is thus mostly applied in material-growth and material-characterization work.

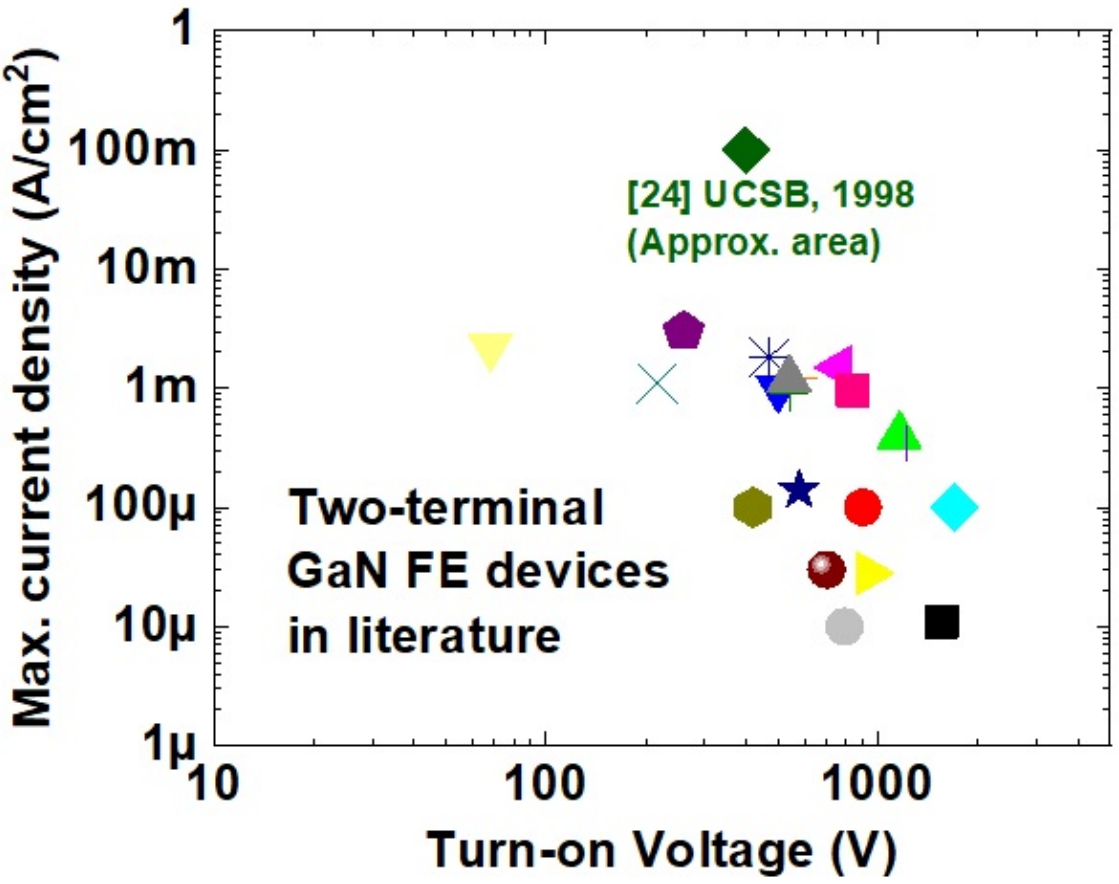


Figure 2-1: Prior work of GaN field emission devices in literature [70, 72–79, 88–105]. Most of them are two-terminal devices and have high turn-on voltages ($>$ 100 V).

2.2 Field emission diodes fabricated by a top-down approach

Though many efforts have been made on the "bottom-up approach" for GaN field emitters, in order to make useful vacuum transistors, the integrated-gate structures on GaN field emitters are necessary. The bottom-up approach is suitable for growth technologies to develop high-aspect-ratio nanostrucutres, but the uniformity and orientations of nanostructures are usually hard to be controlled. On the other hand, the "top-down approach" combining both lithography and etching steps can be more flexible on complex device structure designs and can produce uniform nanostructures [87]. As a result, to study the basic operation and stability of the electron field emission

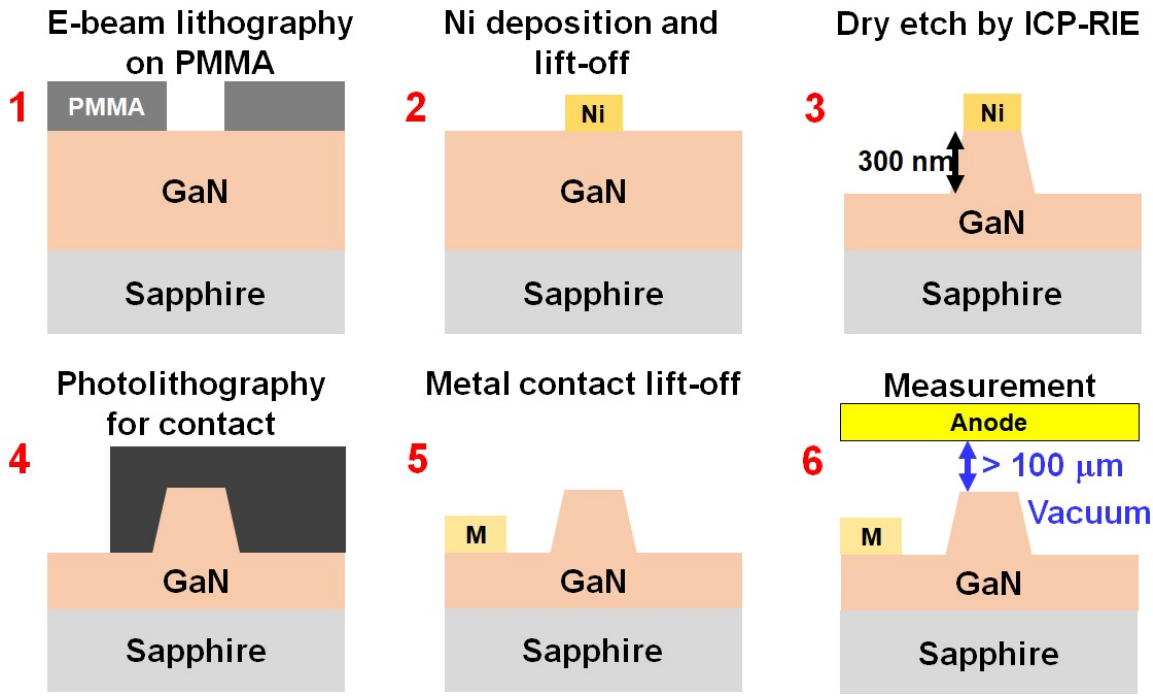


Figure 2-2: Process flow of the GaN field emitter (FE) diodes for I-V characteristics and long-term stability study.

from GaN nanostructures, the GaN field emission diodes are fabricated by a top-down approach and are characterized in this chapter.

The process flow of the GaN field emission diodes is shown in Fig. 2-2. The GaN-on-sapphire coupons are used in this work to develop and test the whole process flow. The samples are firstly cleaned by piranha for 10 min, and then (1) the e-beam lithography defines patterns on PMMA (950 A4) with cold develop (1 MIBK + 3 IPA, @ -10 $\sim$ -13^{o}C for 80 - 90 sec). Then (2) a Ni hard mask is deposited by an e-beam evaporator and the samples are soaked in acetone or N-Methyl-2-pyrrolidone (NMP) for lift-off. After lift-off, the samples are cleaned by organic solvents and a short oxygen plasma ashing, and (3) the GaN pyramids are formed by inductively coupled plasma-reactive ion etching (ICP-RIE) with Ni hard mask. The Ni mask is then removed by wet etching (piranha or Ni etchant). Following that, the (4) metal contact regions is defined and (5) contact metal lift-off is the last step of the fabrication. After the fabrication, the GaN field emitter pyramids are checked by the scanning electron microscope (SEM) for both top-view image (Fig. 2-3(a)) and cross-

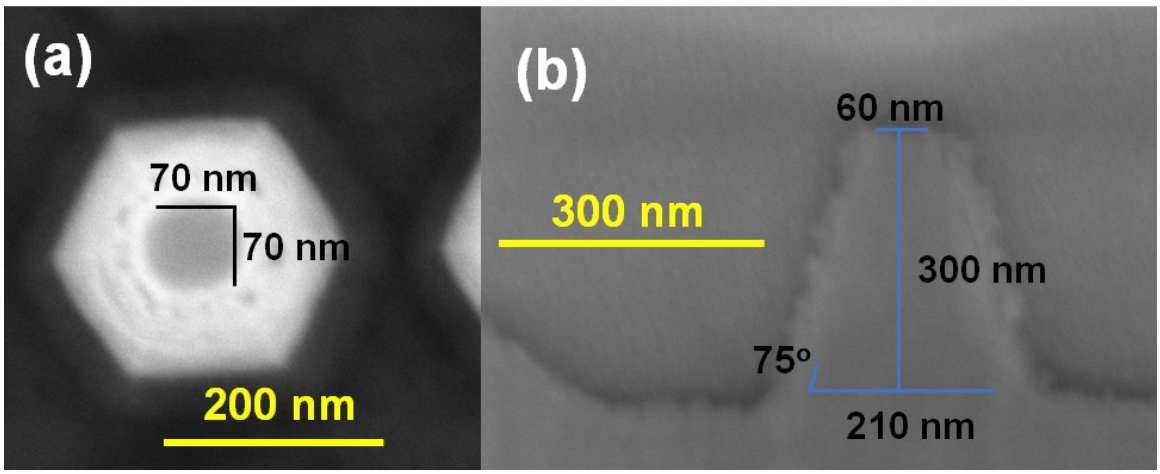


Figure 2-3: (a) Top-down and (b) cross-sectional scanning electron microscopy (SEM) images of fabricated GaN field emitter pyramid. The GaN pyramids are formed by the inductively coupled plasma-reactive ion etching (ICP-RIE).

sectional image (Fig. 2-3(b)). The Cross-sectional image is obtained by the focused ion beam-scanning electron microscope (FIB-SEM) dual beam system. Specific semi-polar planes of GaN appears on these GaN pyramids, and the sidewall slope is around 75 degree. The field-emitter pyramid tip width is about 60-70 nm. As mentioned in section 1.2.1, the sharp field emitter tip is desired to enhance the electric field on the emission surface, and there is still room of improvement for these GaN pyramid tips.

Finally, (6) the GaN coupons are loaded into the ultrahigh vacuum (UHV) chamber for the device characterization. The anode is a suspending tungsten metal ball with a diameter of 0.5 mm. The anode is moved by micro-manipulators to be on top of the GaN field emitter array (FEA) with a distance longer than 100 μm. It should be noted that, during this study, the distance between anode and GaN FEAs is not properly calibrated, so the turn-on voltages of these GaN FEAs are not transferable to the turn-on electric field. However, the distance is kept the same when measuring a GaN FEA, so the performance variation among different I-V sweeps and the long-term device stability are still meaningful.

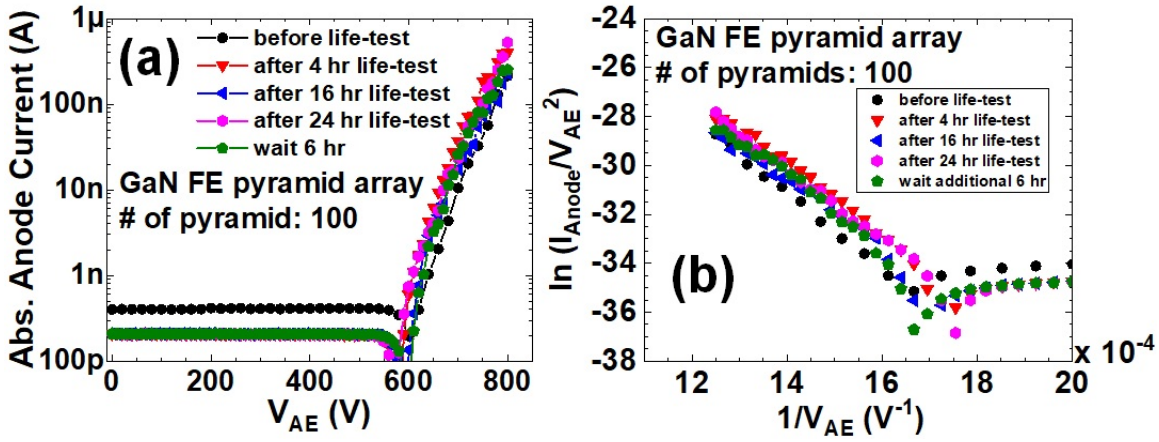


Figure 2-4: (a) I-V characteristics and (b) corresponding Folwer-Nordheim (F-N) plot of a two-terminal GaN field emitter pyramid array diode. This field emitter array consists of 100 GaN pyramids. The F-N plot indicates that this field emission diode is stable even after 24 hours of DC operation.

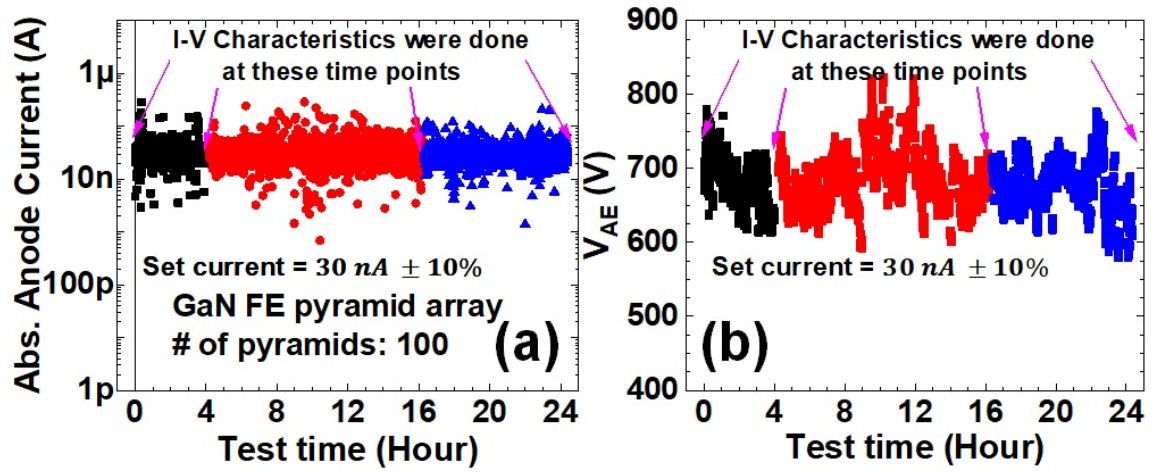


Figure 2-5: (a) Current and (b) anode-emitter voltage (V_{AE}) versus time of the long-term stability test. The test is set to control the V_{AE} to keep the anode current at a constant level of 30 nA ± 10%. There is some variation in current and bias voltage during this long-term stability test, while the overall behavior remains unaltered, which is confirmed by F-N plot in Fig. 2-4(b).

2.3 Device characterization

The GaN field emission diodes are measured in the UHV chamber. The I-V curves and the corresponding Folwer-Nordheim (F-N) plot of a GaN FEA diode are shown in Fig. 2-4. This GaN FEA consists of 10 × 10 pyramids with ∼ 60-nm tip width and ∼ 360-nm pitch. The maximum anode current is about 500 nA at V_{AE} (anode-emitter

voltage) = 800 V, where the maximum emission current density is estimated about 4 A/cm^2 based on the array area. The I-V curves are measured before, during, and after the lifetime test (Fig. 2-5). Based on I-V curves and F-N plot, the GaN FEA is found very stable across a long (24-hr) DC operation.

The DC lifetime test is conducted by varying V_{AE} to keep the anode current at 30 nA $\pm$ 10%, which is estimated as 150 mA/cm^2 in emission current density (Fig. 2-5). The large noise in the anode current can be resulted from micro-vibration of the suspending anode terminal, the noise in the measurement system at the high bias ($>$ 500 V) condition, and the adsoprtion/desoprtion of residual gases on the emitter tips during operation [35]. Though the current seems noisy (Fig. 2-5(a)), the V_{AE} stays in the same region (600 - 800 V) during the whole DC lifetime test.

Based on the I-V curve, the initial F-N slope (-b_{FN}) (before the lifetime test) is -15,700, and the -b_{FN} after 24-hr lifetime test is -14,070. After waiting for another 6 hours, the -b_{FN} is back to -15,030. The standard errors of b_{FN} extraction in fitting lines of F-N plot is 300 $\sim$ 500, which equal to about 2-3% of the extracted b_{FN} values. The Seppen-Katamuki (S-K) plot of this GaN FEA diode for all I-V sweeps before, during, and after the DC lifetime test is shown in Fig. 2-6. The results of S-K plot show that the performance changes after the long DC operation, but the device is not permanently altered. After the device rests for 6 hours after 24-hour-long DC operation, the extracted F-N intercept (ln(a_{FN})) and F-N slope (-b_{FN}) are very close to the values before the DC lifetime test. Therefore, the change in F-N intercept and F-N slope during the DC lifetime test might indicate the adsorption/desorption happening on the emitter surface to change the surface emission properties. Though the precise field enhancement factor is hard to be estimated since the distance between anode and the GaN FEA is not calibrated, the GaN FEA is believed stable based on the measurement results [35]. Furthermore, the GaN field emission pyramids are checked before and after the lifetime test by SEM (Fig. 2-7), and no clear deformation nor damage is observed.

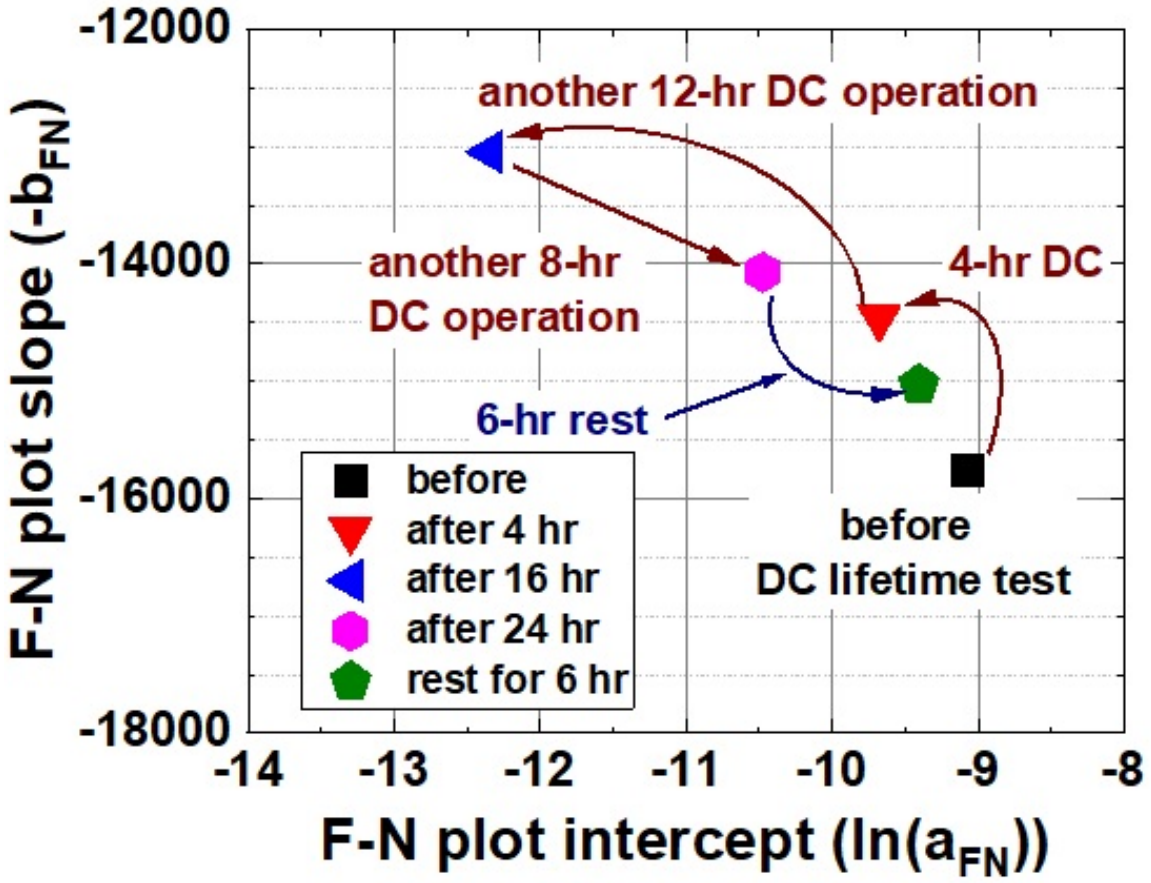


Figure 2-6: Seppen-Katamuki (S-K) plot of the GaN FEA diode before, during, and after the DC operation lifetime test. There is change during the long-term stability test, which can potentially be explained by the surface adsorption and desorption to affect the effective tip radius and work function [106]. However, the change is mostly temporary since the behavior goes back to near initial condition after 6-hour rest.

2.4 Device failure during operation

Another GaN FEA is also measured (Fig. 2-8(a)). It should be noted that the anode metal is moved to be on top of the measured GaN FEA, but the distance between the FEA and anode might be different from the measurement in Fig. 2-4. Thus, the operating voltage can be significantly different between two devices (Fig. 2-4 and Fig. 2-8(a)) due to the lack of proper calibration on the distance between anode and the sample.

The device breakdown is observed during the 3rd I-V sweep of this GaN FEA and the pressure jumps up over two orders of magnitude (from below 10^{-8} Torr to above

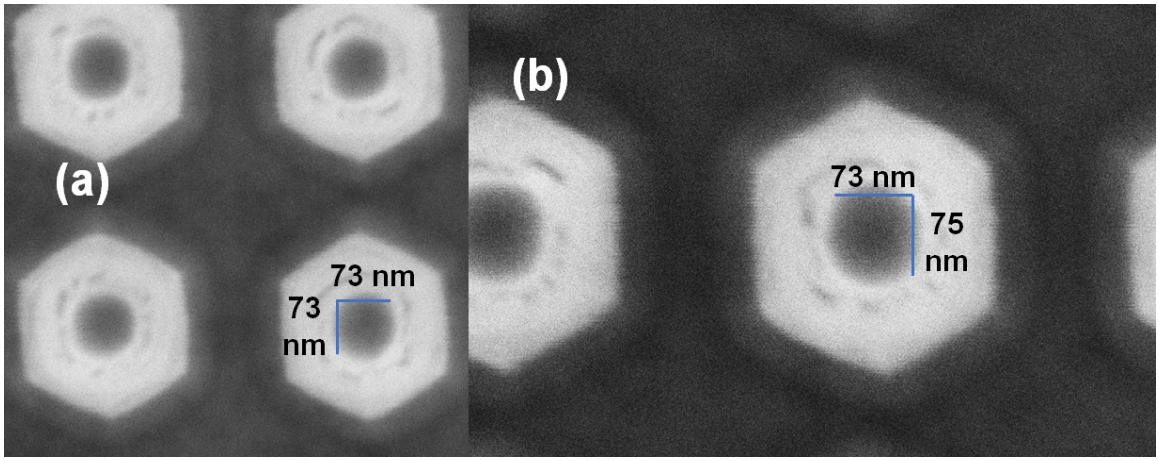


Figure 2-7: Top-down SEM images of a GaN pyramid array (a) before and (b) after the 24-hour long-term stability test. There is no clear difference before and after the stability test.

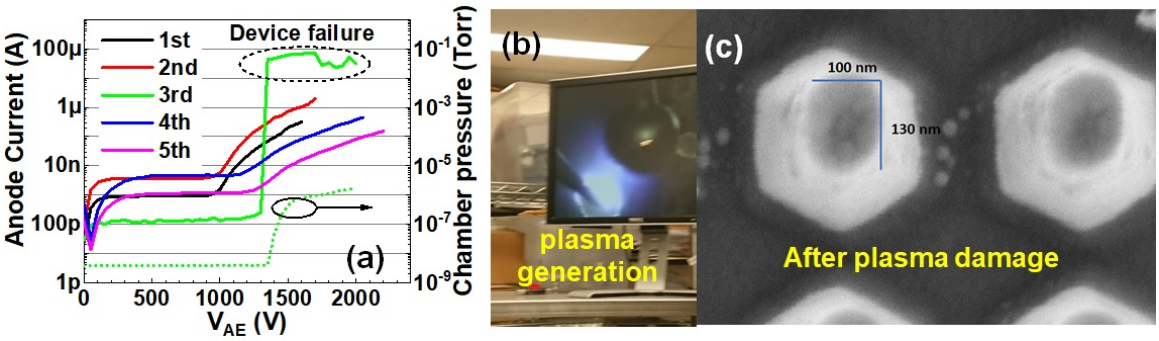


Figure 2-8: (a) I-V characteristics and pressure changes when the device failure happens, (b) photo took when the device failure happens, and (c) SEM image of the failed GaN FE pyramid after device failure. The device failure are probably resulted from the plasma generation between the emitter and the anode metal ball (as shown in (b)).

10^{-6} Torr). Additionally, the anode current jumps to the pre-set maximum value of ~ 100 μA, which means the additional conduction path forms during this breakdown. When the device breakdown happens, the arcing (or plasma) is also observed (Fig. 2-8(b)). Though the mechanism that causes this failure is not clear, there are few possibilities. For example, if the anode metal is not clean, the emitted electrons' kinetic energy ($\sim eV_{AE}$) can be transferred to and heat up the anode metal, leading to the degassing from the anode. Furthermore, the electron conduction in the field emitter tips can also cause self-heating of the tips, leading to the degassing from the

emitters and even thermal runaway. The gas can be also ionized by the electric field between metal terminals and emitters, which can then cause ion current conduction and arcing [107–109]. The energy dissipated in the vacuum arcing path can cause physical sputtering on the material surface, which kicks out more atoms and the pressure of the chamber increases (Fig. 2-8(a)). At this point, the high-current conduction path in the vacuum formed and the anode current reaches the pre-set maximum value in the measurement setup. The GaN FEA is checked by SEM after the device breakdown, and the deformation is clearly observed on the GaN pyramids (Fig. 2-8 (c)), which is another evidence that the physical damage happened when the device breakdown is observed during the I-V measurement.

2.5 Summary of the chapter

The top-down approach of GaN nanopyramid formation via ICP-RIE process is developed for GaN FEA diodes. The maximum emission current density of a 10 $\times$ 10 GaN pyramid FEA can be about 4 A/cm^2 when considering the whole area of the array (Fig. 2-5 (a)), which is already higher than most of the reported current densities in literature (Fig. 2-1). Though the field enhancement on this GaN FEA is hard to estimate since the distance between the anode metal and the GaN FEA is not properly calibrated, the field emission current of the GaN pyramid FEA diode is found stable for at least 24-hr DC operation at $\sim$ 150 mA/cm^2 (Fig. 2-7) without clear degradation after the lifetime test.

Another GaN FEA diode is also measured, and the device failure is observed with clear jumps in both anode current and chamber pressure (Fig. 2-8(a)). While the mechanism of this device failure is not clear, the reduction of the anode voltage can be a way to mitigate the anode degassing. To reduce the operating voltage of anode, the gate terminal is necessary to effectively control the emission current. Furthermore, the self-aligned-gate structure is much preferred than the external gate structure since the distance between the gate and the emitter directly affects the minimum operating voltage required for the effective gate control. Therefore, the main focus

in the next chapter is to develop the self-aligned-gate structure for GaN gated FEAs with a reduced operating voltage and effective gate control as a vacuum transistor.

Chapter 3

GaN nanowire self-aligned-gated field emitter arrays

The materials in this chapter are partially based on the following conference paper: Pao-Chuan Shih et al., "GaN Nanowire Field Emitters with a Self-Aligned Gate Process," 2020 Device Research Conference, DOI: 10.1109/*DRC*50226.2020.9135161 *[110], with permission, © 2020 IEEE [111].*

The two-terminal GaN FEA diodes are fabricated with a top-down approach and are characterized for both I-V characteristics and DC operation stability in chapter 2. Except for the catastrophic breakdown and arcing (Fig. 2-8), the GaN FEA is very stable and the device does not permanently degrade (Figs. 2-6 and 2-7) after a long DC operation. However, the high operating voltage (>500 V) and the lack of gate-modulating operation are still main issues to use those GaN FEAs as vacuum transistors. There are two aspects to reduce the operating voltage and bring the gate-modulating operation: (1) high-aspect-ratio nanostructure emission tips, and (2) the self-aligned-gate structure. The high-aspect-ratio nanostructures can locally enhance the electric field on the emitter tips, and the vertical nanowires (NWs) with vertical sidewalls can provide the highest aspect ratio [19]. The GaN vertical structures with vertical m-plane sidewalls have been demonstrated by combining the plasma dry etching and wet etching for vertical FinFETs [80, 81]. On the other

hand, the self-aligned-gate structure can reduce the gate-emitter distance without difficult lithography alignment step, and it can provide good gate control on electron emission. Since the general process flow of this NW self-aligned-gate field emitter arrays (SAGFEAs) is relatively similar to the GaN vertical FinFETs, in this chapter, our first generation of GaN SAGFEAs are developed based on the prior veritcal FinFET work [80, 81].

The process flow and each key step are described, and the experimental results of our first demonstration of GaN NW SAGFEA are reported in this chapter. The operating voltage (V_{GE}) as a field-emitter-based vacuum transistor is below 70 V, which is an order of magnitude lower than the applied voltage in the two-terminal GaN FEA diodes in chapter 2. The transistor-like transfer and output characteristics are observed. However, the maximum current density ($J_{A,max}$) is about 12 mA/cm^2, which is two orders of magnitude lower than the one of two-terminal GaN FEA diodes. Furthermore, the gate leakage increases significantly in about 10 mins of the DC lifetime test. These results indicate that our first-generation GaN NW SAGFEAs do not have good enough performance and are not stable enough to be useful vacuum transistors. The further improvement on device performance based on modifications of device structures and process flow will be reported in the next chapter.

3.1 Advantages of self-aligned-gate structure

To demonstrate field-emitters with a gate-modulating operation for x-ray tubes and electron sources, there have been work on carbon-nanotube (CNT) gated field emitters, which clearly shows significant advantages of self-aligned-gate structures compared to the remote-gate structures. The operating voltage on the gate can be much reduced (from $>$ 500 V to below 50 V) and the device sizes can be reduced by many orders of magnitudes by using the self-aligned-gate structure instead of the remote-gate structures [112–114]. The remote-gate structures are useful for x-ray tubes since the voltages of anode to generate x-ray are already at the level of 10 kV, thus the gate voltage of a few hundred volts is not the big concern. Furthermore, the integration of

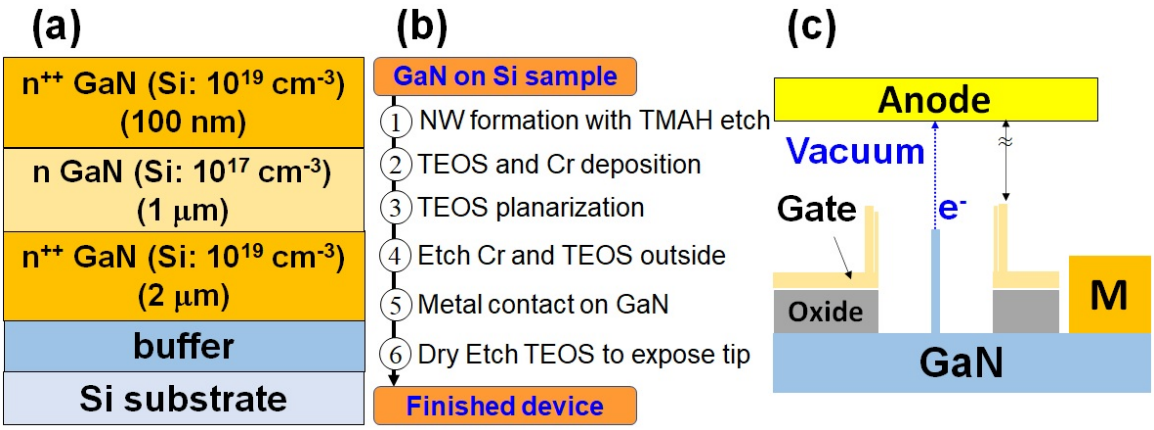


Figure 3-1: (a) GaN-on-Si epitaxial structure used for the self-aligned-gate process development, (b) the brief process flow for GaN nanowire (NW) self-aligned-gate field emitter arrays (SAGFEAs) consists of key fabrication steps, and (c) illustration showing the measurement setup of the GaN NW SAGFEA. The anode is a suspended metal ball positioned by micro-manipulators.

many devices is not useful for x-ray tubes, so the device size in the range of a few mm to cm is not an issue [112, 113]. On the other hand, for field-emitter-based vacuum transistors, the low operating voltages, electron emission efficiency, and the capability of future device integration are critical, and thus the self-aligned-gate structures are chosen and developed for the III-Nitirde FEAs in this thesis research.

3.2 Device fabrication

In this chapter, the GaN self-aligned-gated field emitter arrays (SAGFEAs) are fabricated on pieces cut from a 6-inch GaN-on-Si wafer grown by Enkris, Inc via MOCVD. The epitaxial structure of this GaN-on-Si wafer is as follows: 100 nm n^{++}-GaN ([Si] = 1×10^{19} cm^{-3}), 1 μm n^{-}-GaN ([Si] = 1×10^{17} cm^{-3}), 2 μm n^{++}-GaN ([Si] = 1×10^{19} cm^{-3}), and buffer layers on the (111) Si substrate (Fig. 3-1(a)). Though this epitaxial structure was originally designed for GaN vertical FinFETs, which is not optimal for GaN FEAs, these pieces are still useful to develop the 1st generation of the GaN SAGFEAs. The key steps of the device fabrication are summarized in Fig. 3-1(b), and the cross-sectional device diagram of the finished GaN SAGFEAs is shown in Fig. 3-1(c). The details of process steps and issues during the process

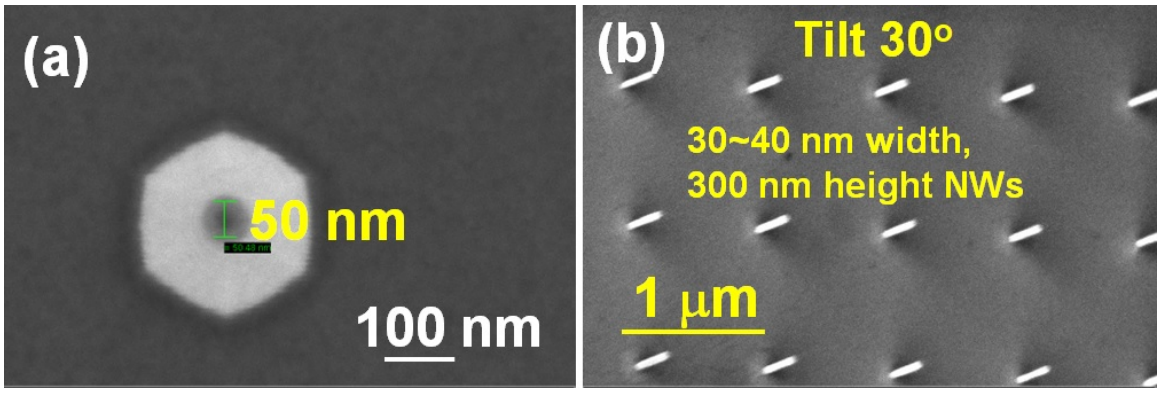


Figure 3-2: The SEM images of (a) a GaN pyramid with Ni hard mask formed by ICP-RIE dry etching and (b) GaN NW array fabricated by the following TMAH etching.

development are summarized in Appendix A. Devices will be measured in the UHV chamber, and the anode metal, as mentioned in chapter 2, is a suspending tungsten 0.5-mm-diameter ball which can be moved by the micro-manipulators.

3.2.1 GaN nanowire fabrication

The GaN-on-Si pieces are firstly cleaned by piranha (3 H_2SO_4 + 1 30% H_2O_2) for 10 mins. After the cleaning, the first key process step is the formation of GaN verital nanowire (NW) arrays (step (1) in Fig. 3-1(b)). The Ni hard mask is defined by e-beam lithography on PMMA with the metal lift-off. The GaN vertical pyramids are then defined by Cl_2/BCl_3-based ICP-RIE with Ni hard mask (Fig. 3-2(a)). The pyramids with tip width of $\sim$ 50 nm are fabricated. After that, the GaN sidewalls are etched by heated Tetramethylammonium Hydroxide (TMAH), and the Ni mask is then removed by piranha in this experiment. The TMAH and KOH are well-known chemicals for orientation-dependent wet etching on GaN. A 50 $\times$ 50 array of GaN NWs with about 40-nm width and about 300-nm height can be achieved by this process (Fig. 3-2(c)). The etching rate on non-polar m-planes ($\{1\bar{1}00\}$) of GaN is much slower than the ones on different semi-polar planes (like the sidewalls on the GaN pyramid (Fig. 3-2(a)) [80,85,86,115]. However, the etching rate on non-polar a-planes ($\{11\bar{2}0\}$) is still higher than the one on m-planes, so the fabrication of uniform

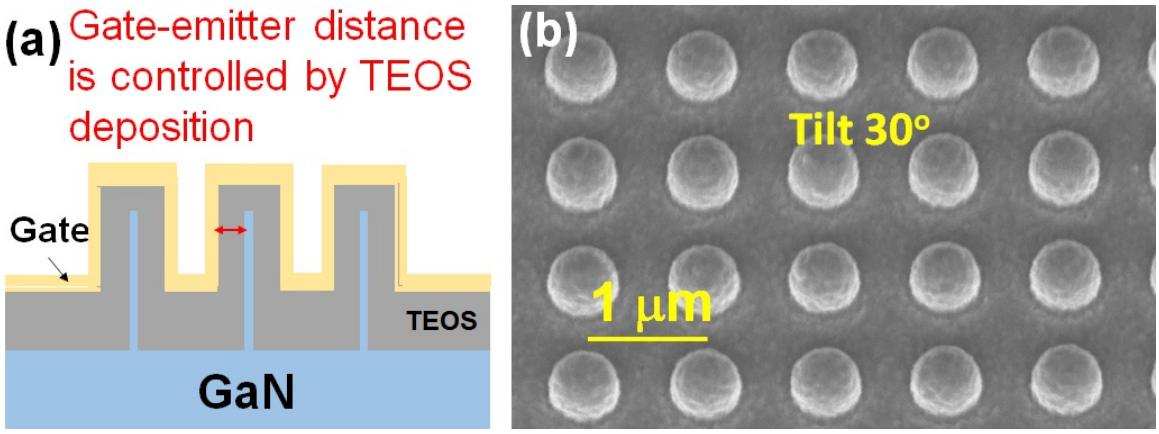


Figure 3-3: (a) The cross-sectional diagram and (b) SEM image of the device after step (2): tetraethyl orthosilicate (TEOS) and Cr deposition.

sub-30-nm-width GaN vertical NWs is still challenging.

3.2.2 Self-aligned-gate structure formation

After the GaN NW arrays are formed, the 2nd step is the gate stack deposition (step (2) in Fig. 3-1(b)). The ∼ 200-nm-thick TEOS as gate insulator is deposited by plasma enhanced chemical vapor deposition (PECVD), and the ∼ 50-nm-thick Cr is then deposited by sputtering as gate metal (Fig. 3-3(a)). The TEOS is chosen instead of conventional Silane-based SiO_2 because of better sidewall coverage of TEOS film. For the better sidewall coverage, the sputtering is also chosen instead of e-beam evaporation for the gate metal. The uniform domes of Cr/TEOS/GaN stack are fabricated and confirmed by SEM (Fig. 3-3(b)). It should be noted that the gate-emitter distance (d_{GE}) is mainly controlled by the TEOS deposition. Ideally, the sidewall coverage should be good but not as thick as the planar film deposition, in order to get both good gate-emitter isolation and a relatively smaller d_{GE} for better gate control on field emission regions.

Following the gate stack deposition, the planarziation on FEA regions is then performed (step (3) in Fig. 3-1(b)). A ∼ 1-μm-thick TEOS layer is firstly deposited by PECVD, and the blank CF_4-based dry etching is then conducted to etch the TEOS layer (Fig. 3-4). The CF_4-based dry etching step is critical and is timed to make sure

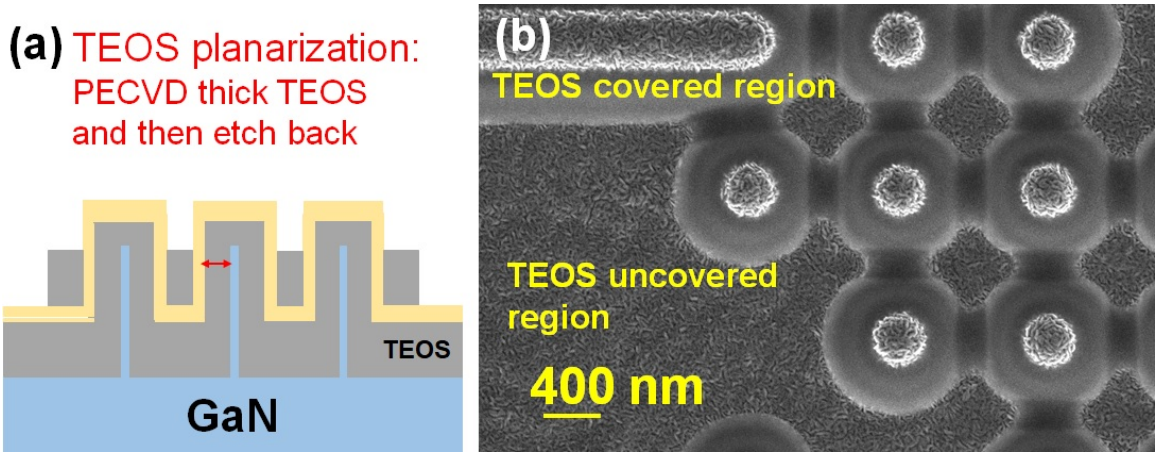


Figure 3-4: (a) The cross-sectional diagram and (b) SEM image of the device after step (3): TEOS planarization. The gate metal on top of the tips is exposed, and the gate metal surrounding the tips is still protected by TEOS.

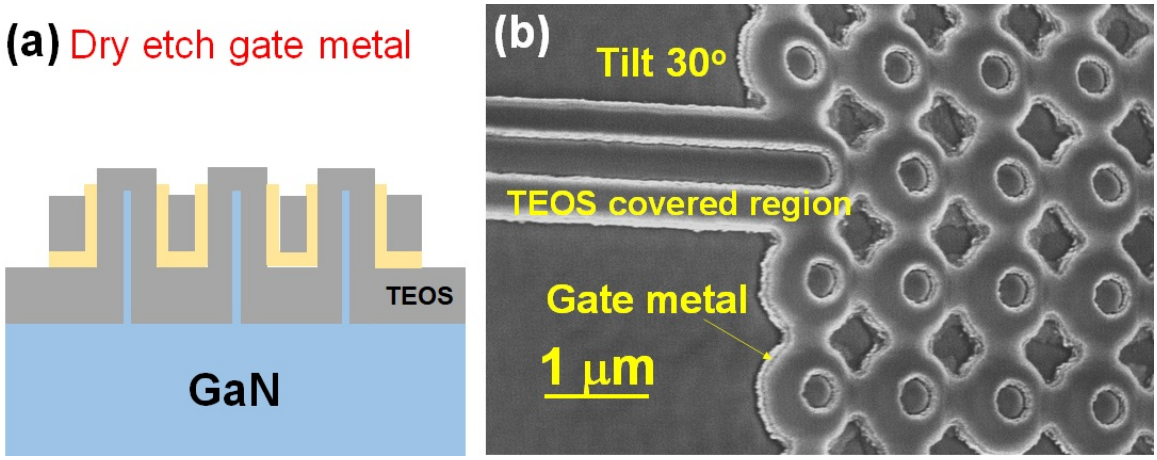


Figure 3-5: (a) The cross-sectional diagram and (b) SEM image of the device after step (4): Cr dry etching.

the Cr metal top surface is exposed but the sidewalls of the Cr/TEOS/GaN domes are still protected by TEOS (Fig. 3-4(b)). The TEOS layer is used since the PECVD silane-based SiO_2 will have voids in the film between the vertical structures, leading to a problem in the following gate metal etching step. On the other hand, the TEOS film is continuous across the array, so the gate metal will still be continuous after the following etching step.

The gate metal (Cr) is then etched by Cl_2/O_2-based ICP-RIE (step (4) in Fig. 3-1(b)). As the sidewalls and the connections between gate metal on each NW are

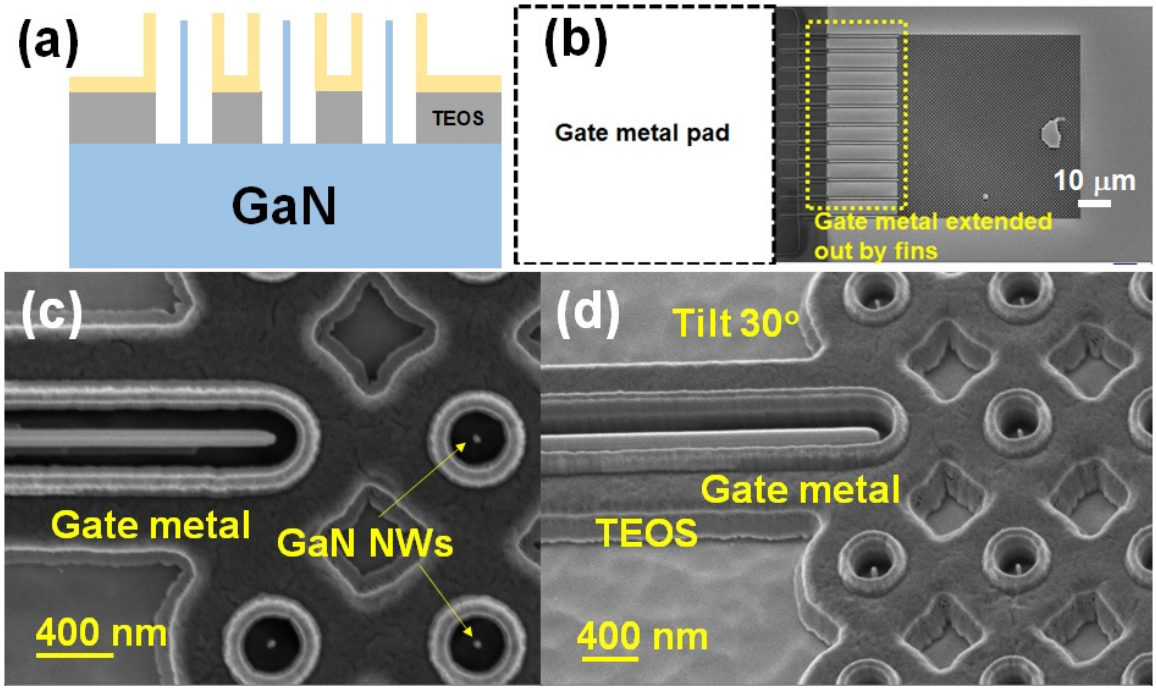


Figure 3-6: (a) The cross-sectional diagram and (b) (c) (d) SEM images of the finished GaN NW SAGFEA. The fins adjoint to NWs are used to extend the gate metal out from the FEA region to the gate pad region for probing (as shown in (b)).

protected by TEOS, the gate metal is still continuous after the top regions of the gate metal is etched away (Fig. 3-5). By carefully controlling all the deposition and etching steps (steps ② - ④ in Fig. 3-1(a), Figs. 3-3, 3-4, and 3-5), the well-defined self-aligned device structure can be fabricated without the need of lithography alignment. After the gate metal etching, the TEOS outside the FEA regions is then wet etched by buffer oxide etchant (BOE) to expose the GaN surface for metal contact formation. The metal contact is then deposited on GaN surface (step ⑤ in Fig.3-1(b)).

The last step of the device fabrication is the etching process to expose the GaN NW emitters (step ⑥ in Fig. 3-1(b)). The TEOS layer covering the GaN NW emitters is etched by CF_4-based RIE (Fig. 3-6(a)). After the dry etching, the device is checked by SEM to confirm that the GaN NW emitters are exposed (Fig. 3-6(c) and 3-6(d)). The fins connecting to the FEA are used to extend the gate metal out from the FEA region to the gate metal pad region for probing in the following I-V characteristics measurement (Fig. 3-6(b)).

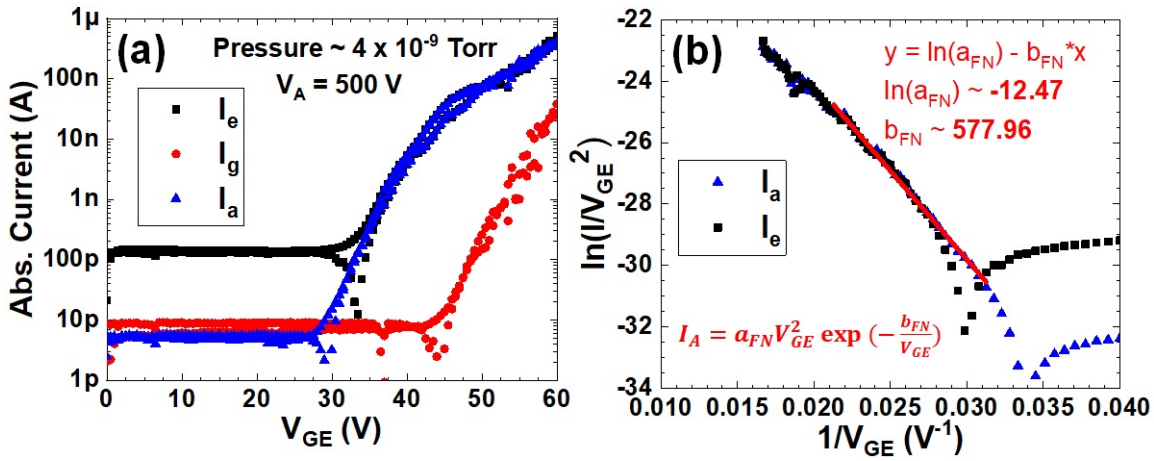


Figure 3-7: (a) Transfer characteristics and (b) the corresponding Fowler-Nordheim (F-N) plot of the GaN NW SAGFEA. This GaN NW SAGFEA consists of 50 × 50 NWs. This device turns on at V_{GE} = 29 V (@ I_A = 10 pA) and the max I_A = 415 nA ($J_A \approx 14\ mA/cm^2$). The self-aligned-gate structure gives good emission current control, while the total emission current is not as high as we expected.

3.3 Device characterization and discussion

After the device fabrication and the SEM characterization, the sample piece is then loaded into the UHV chamber for the I-V characteristics measurement. The measurement setup is illustrated in Fig. 3-1(c)). The anode-emitter distance (d_{AE}) is kept about few mm in all measurement in this chapter.

3.3.1 DC I-V characteristics

The transfer characteristics and the corresponding Fowler-Nordheim (F-N) plot of a GaN NW SAGFEA with a 50 × 50 NW emitter tips are shown in Fig. 3-7. The NW tip width is about 30-40 nm, the NW height is about 300 nm, the d_{GE} is about 160 nm, and the pitch between NW tip is about 1.2 μm. The anode voltage (V_A) is fixed at 500 V in the transfer characteristics. The anode current (I_A) starts increasing from the noise level at gate-emitter voltage (V_{GE}) of ~ 29 V. The max I_A is about 420 nA at V_{GE} = 60 V, and the max anode current density ($J_{A,max}$) is about 12 mA/cm^2 based on the FEA area of 60 μm × 60 μm. The gate leakage (I_G) is always at least 1 or 2 orders of magnitude lower than I_A.

Based on the equation:

$$I_A = a_{FN} V_{GE}^2 exp(-\frac{b_{FN}}{V_{GE}}) \tag{3.1}$$

we can get:

$$ln(\frac{I_A}{V_{GE}^2}) = ln(a_{FN}) - \frac{b_{FN}}{V_{GE}} \tag{3.2}$$

where we can plot a curve of $ln(\frac{I}{V_{GE}^2})$ versus $\frac{1}{V_{GE}}$ (F-N plot in Fig. 3-8(b)). If a negative-slope straight line is observed, the operation of this straight line region is dominated by the field emission. In this GaN NW SAGFEA, the slope of F-N plot ($-b_{FN}$) is $\sim$ -577.96, and the intercept of F-N plot ($\ln(a_{FN})$) is $\sim$ -12.47. The slight change in slope in the F-N plot at small $\frac{1}{V_{GE}}$ (i.e. large V_{GE}) might indicate that the electron emission current is approaching the electron-supply limitation. In equation 3.1, the field emission current is calculated based on the assumption that there are more than enough electron supply at the emitter surface and thus the current is only represented by the field emission mechanism. If electron supply is also considered, the emission current can thus be represented as:

$$j(\overrightarrow{E}) = e \cdot \int N(W) \cdot D(W, \overrightarrow{E}) dW \tag{3.3}$$

where $\overrightarrow{E}$ is the electric field at the emitter surface, W is the energy of electron, N(W) is the supply function describing electron flux to the emitter surface, and $D(W, \overrightarrow{E})$ is the probability of an electron with energy W to tunnel from emitter to vacuum. The electron supply function N(W) can be expressed:

$$N(W) = \frac{4\pi mkT}{h^3} ln(1 + e^{-\frac{W - E_F}{kT}}) \tag{3.4}$$

in the original field emission theory based on a flat metal plane [116]. The E_F is the fermi level. In our GaN NW SAGFEAs, the electron supply will be limited by both quantization of the density of states and the surface depletion from NW sidewalls. For the quantization on the density of states, the electron emission equation from the

low-dimensional systems can be described by summing over all electronic states **Q**:

$$J(\overrightarrow{E}) = e\frac{2}{\Sigma_0}\sum_{Q} f_{FD}(E_Q, T)\int\int D_Q(\overrightarrow{E}, s)[j_Q(s)\cdot\hat{n}]d\Sigma \tag{3.5}$$

which is the equation (2.41) in reference [116]. E_Q is the total energy of state **Q**, Σ_0 is the emitter surface area, $f_{FD}(E_Q, T)$ is the Fermi-Dirac distribution, $D_Q(\overrightarrow{E}, s)$ is the tunneling probability of electron emission, T is the temperature, s is the set of points of the emitter surface, and $j_Q(s)\cdot\hat{n}$ is the electron flux density normal to the tunneling barrier. The probability electron flux density can be expressed:

$$j_Q(r) = \frac{\hbar}{2m_0 i}[\Psi_Q^*(r)\boldsymbol{\nabla}\Psi_Q(r) - \Psi_Q(r)\boldsymbol{\nabla}\Psi_Q^*(r)] \tag{3.6}$$

However, the surface depletion of the n^--GaN layer in the NW is another mechanism affecting the electron supply. Since the field emission theory and detailed physics in the NW structure are not the focus of this thesis research, the detailed discussion and calculation on low-dimensional electron emission can be referred to the section 2.5 in the reference [116].

The operating voltage is reduced from a few hundred volts (Fig. 2-4(a)) to below 70 V (Fig. 3-7(a)) by using the self-aligned-gate device structure, but the maximum current density is about two orders of magnitude lower than the emission current density in the GaN vertical pyramid FEA diode reported in chapter 2. There are few possible reasons of the low emission current density. First of all, The low current density can be the results from the high series resistance in the GaN NWs in the n^--GaN layer. The sidewall depletion on GaN NWs will deplete the electrons in the NW [117], and thus further increases the series resistance. Additionally, the non-uniformity in GaN NW dimensions can also degrade the FEA performance from the expected performance, which will be discussed in chapter 4. Moreover, during the process of CF_4-based RIE to expose GaN tips, the F^- ions on the GaN surface can potentially deplete the electrons from the GaN surface [118], and the plasma can potentially damage the GaN NW tip surface (Appendix C). All these effects can

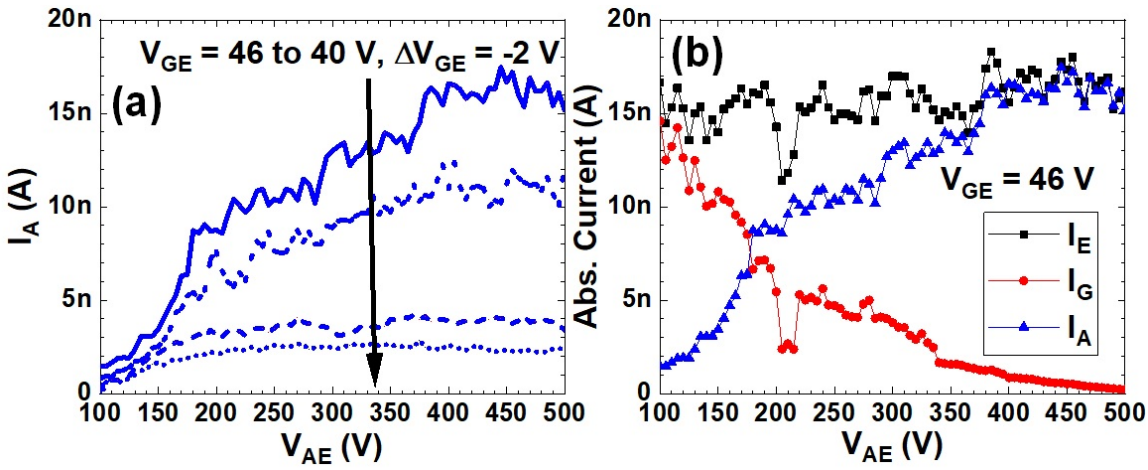


Figure 3-8: The output characteristics of (a) anode current at different V_{GE} and (b) absolute current flowing through 3 terminals at a fixed $V_{GE} = 46\ V$. The current is very noisy since the current is small and additional noise could be generated from vibrations on the suspending anode metal. Despite the noisy data, the overall emission current keeps constant in the whole V_{AE} bias range, indicating the emission current is mostly only controlled by the gate-emitter voltage (V_{GE}).

degrade the GaN NW SAGFEA performance and lead to the low emission current density.

After the transfer characteristics measurement, the output characteristics of this GaN NW SAGFEA are also measured (Fig. 3-8). The output characteristics of V_{GE} = 40, 42, 44, and 46 V are measured from V_{AE} = 100 V to V_{AE} = 500 V. The output characteristics with a slight saturation are observed, but the I_A is very noisy across the whole range. The large noise can be resulted from the micro-vibration on the suspeneded anode or from the measurement noise in the source-measure unit (SMU) due to the high V_{AE} bias and low emission current (10 - 20 nA). The emission current (I_E), gate current (I_G), and anode current (I_A) are all measured simultaneously (Fig. 3-8(b)). Though the measured current is very noisy, the emission current is approximately a constant under the fixed V_{GE} bias condition, which confirms that the electron emission from the emitter tips is mostly controlled by the gate and is not affected by the electric field from the anode. When the V_{AE} is low, the electric field from the anode is too weak and the electron transportation in the vacuum is limited by the space-charge transportation (section 1.2.2) and the surplus emitted electrons

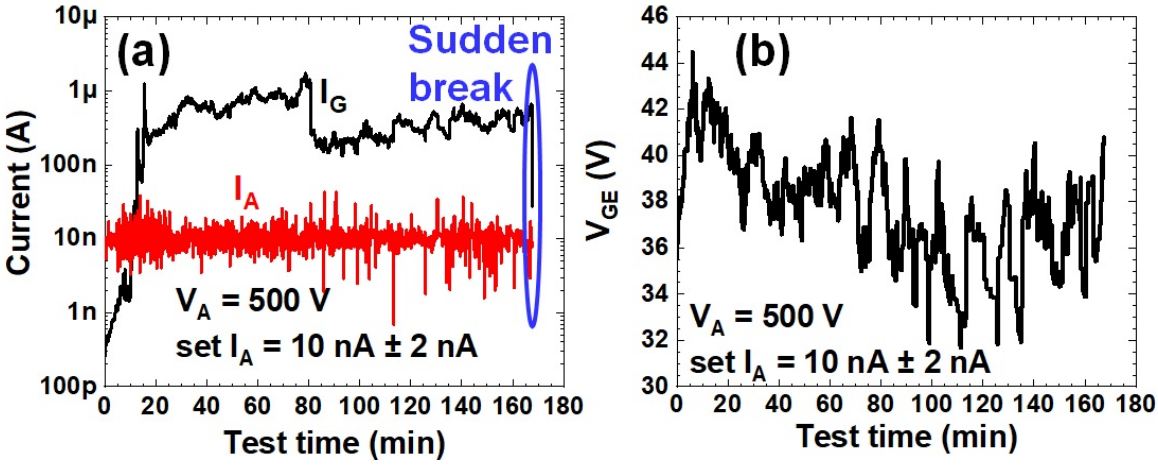


Figure 3-9: (a) The anode current (I_A) and gate leakage (I_G) and (b) the gate-emiter voltage (V_{GE}) of the device DC lifetime test. In this test, the V_{GE} is varied to keep the I_A at a fixed level of 10 nA. The V_A is fixed at 500 V. The gate leakage sharply increases during the first 10-20 mins of DC lifetime test, indicating some issues in device structure or fabrication.

are repelled by the electron cloud to the gate (@ low V_{AE} region in Fig. 3-8(b)). As the V_{AE} increases, the electric field eventually become strong enough that the emitted electrons are not limited by space-charge and most of the emitted electrons can transport to the anode (@ high V_{AE} region in Fig. 3-8(b)).

3.3.2 Device lifetime test

The DC operation stability of this GaN NW SAGFEA is also characterized after the transfer and output characteristics (Fig. 3-9). Since this is a 3-terminal device structure whose emission current is controlled by the gate, the measurement is conducted by varying the V_{GE} to keep the anode current (I_A) at the constant level (10 nA ± 2 nA). The anode voltage (V_A) is fixed at 500 V during the whole DC operation stability measurement. The device breaks after about 170 mins of the DC operation, and before the failure, the V_{GE} mostly varies between 33 V and 43 V. Additionally, after about first 10 mins of the DC stability test, the gate leakge (I_G) sharply increases from few nA to few hundred nA, which is more than 10× higher than the I_A. Though the causes of these issues are not fully understood, they indicate that the device structure and the process flow require more optimizations in the following

Figure 3-10: The SEM images of the device (a) before and (b) (c) after the DC lifetime test. After the DC lifetime test, the GaN NW and surrounding gate region do not show failure or deformation (as shown in (b)), while the damage is clearly observed in the extended fin region (in (c)).

generations of GaN SAGFEAs.

After all measurement, this measured GaN NW SAGFEA is unloaded from the UHV chamber and is then checked by SEM again (Fig. 3-10). There is no observable distortion nor damage in the gated FEA region (Fig. 3-10(b)), while clear damages are observed around the extended gate region (Fig. 3-10(c)). The gate metal in the extended gate region seems to be sputtered or damaged by the arcing during the measurement and cause electrical short between gate and emitter. The sidewall roughness on these fins might be the additional electron emission sites and can be the weak points of the arcing generation and breakdown. To improve the device stability, this potential arcing mechanism should be reduced and eventually eliminated.

3.3.3 Discussion

In this chapter, the self-aligned-gate structures on GaN vertical NWs are developed and fabricated for the demonstration of transistor-like GaN SAGFEAs. The device performance is compared with GaN field emission devices reported in literature (Fig. 3-11) [70, 72–79, 88–105]. Thanks to the close-packed gate structure, the operating voltage (V_{GE}) to control the electron emission is reduced from a few hundred volts to below 70 V. However, the maximum anode current density ($J_{A,max}$) of 12 mA/cm^2 at V_{GE} = 60 V is only at the same level of current densities of GaN FEA diodes reported in the literature, and it is lower than the maximum emission current density

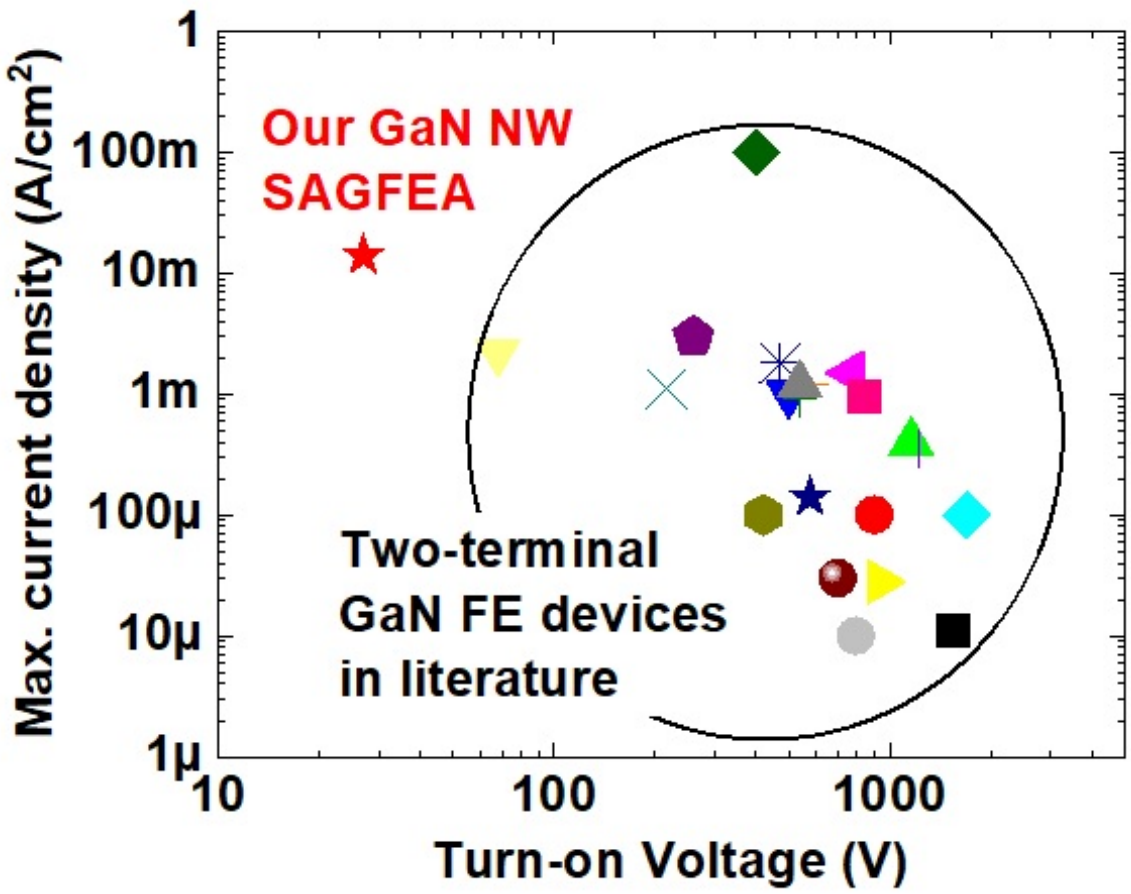


Figure 3-11: The benchmark plot comparing our GaN NW SAGFEA with the two-terminal GaN FE devices in literature [70, 72–79, 88–105]. By developing and integrating the self-aligned-gate structure onto field emitter arrays, the turn-on voltage is successfully reduced from $>$ 100 V to below 50 V, and the transistor-like behavior is demonstrated.

($\sim$ 4 A/cm^2) of the GaN FEA diode reported in chapter 2.

There have been different failures and corresponding modifications during the process development. The encountered issues during the process development and the corresponding modifications on process flow and on device structures are summarized in Appendix A. For example, different from the TEOS planarization process (Fig. 3-4), the photoresist (PR) planarization reported in GaN vertical FinFET fabrication was also tested [80, 119], but there are some issues during the process development and integration. Additionally, the last plasma etching step on TEOS to expose unprotected GaN NW tips can cause additional physical damages and surface depletion

due to the F^- ions [118]. These issues should be avoided or eliminated in the following batches of GaN SAGFEAs to further improve the device performance.

To improve the device performance, there are a few things can be engineered or modified. First, the epitaxial structure can be re-designed and optimized for the field emission devices. Secondly, the device structures, such as emitter tip shapes and the surrounding structures should be modified to improve the uniformity and reproducibility in device fabrication. Especially, the emitter tip size uniformity is critical to provide better performance and stable operation in the field-emisison-based vacuum transistors. Finally, a reproducible way to well-contorlled etching process for sub-20-nm dimension for emission tips is necessary to enhance the electric field for the electron field emission. All these topics will be discussed and dealt with in the next chapter.

Chapter 4

Optimization of GaN self-aligned-gated field emitter arrays

The materials in this chapter are partially based on the following journal and conference papers:
(1) Pao-Chuan Shih et al., "Self-Align-Gated GaN Field Emitter Arrays Sharpened by a Digital Etching Process," IEEE EDL, DOI: 10.1109/LED.2021.3052715 *[120].*
(2) Pao-Chuan Shih et al., "Wet-based digital etching on GaN and AlGaN," APL, DOI: 10.1063/5.0074443 *[121].*
(3) Pao-Chuan Shih et al., "GaN Field Emitter Arrays with J_A of 10 A/cm^2 at V_{GE} = 50 V for Power Applications," 2022 IEDM, DOI: 10.1109/$IEDM$45625.2022.10019399 *[122].*

The GaN NW SAGFEAs, which are fabricated by a top-down approach, have been developed and discussed in chapter 3. In this chapter, the additional modifications on both device structures and fabrication are discussed and conducted to further improve the performance of GaN field-emitter-based vacuum transistors. The current density (J_A) at the same bias condition is improved by $\sim 1000\times$ from the GaN NW SAGFEAs reported in chapter 3 to the state-of-the-art GaN SAGFEAs (from < 0.01 A/cm^2 to

10 A/cm^2 at V_{OV} = 30 V, where V_{OV} = V_{GE} - $V_{GE,ON}$).

First of all, the yield and uniformity of FEAs and their effects on device performance are discussed. The pyramid-shape FEAs are chosen over NW-shape FEAs for better fabrication yield and uniformity. Following that, a digital etching technology to sharpen field emitter tips to further improve the electric field enhancement is developed. The 2nd-generation GaN SAGFEAs are then fabricated based on pyramid-shape tips, which are sharpened by digital etching. The 2nd-generation device has a slightly lower $V_{GE,ON}$ and 10× higher maximum current density ($J_{A,max}$) than the GaN NW SAGFEAs reported in chapter 3.

In the 3rd-generation GaN SAGFEAs, the device structure and fabrication flow are further modified based the failure and device breakdown observed in the 2nd-generation devices. The structure and thickness of the insulator layer under the gate pad region are modified to prevent early breakdown observed in the 2nd-generation devices, which happens at $V_{GE} \sim 50$ V. The maximum operating gate-emitter voltage (V_{GE}) can then be increased to above 60 V and the maximum current density ($J_{A,max}$) can be increased by another 10× from the 2nd-generation devices (from 0.15 A/cm^2 to above 1 A/cm^2).

In the last-generation GaN SAGFEAs, the device structure is further optimized to improve the device stability. The potential weak points in the 3rd-generation devices are identified based on Silvaco TCAD simulation, and the device structure design is modified accordingly. As the device structure is further optimized and the process flow becomes mature, the state-of-the-art (4th-generation) GaN SAGFEAs are demonstrated. Compared to the state-of-the-art Si SAGFEAs, these GaN SAGFEAs have comparable turn-on voltages ($V_{GE,ON}$) and higher current density at the same bias condition (J_A = 10 A/cm^2 at V_{OV} = 30 V). With the capability of high current density at low bias condition, these latest results show the potential of GaN field-emitter-based vacuum transistors for future power and high-frequency vacuum electronics.

Finally, possible further improvement on GaN SAGFEAs in the future are briefly discussed. For example, the chemical physical polishing (CMP) process can be devel-

oped if the technology is transferred from pieces to 6-inch wafer-scale fabrication in the future. On the other hand, the e-beam lithography alignment combined with the integrated anode can potentially further reduce the operating voltage and improve the device stability. Our efforts on integrating anode onto the GaN SAGFEAs will be discussed in more details in chapter 6.

4.1 Choice of emitter shapes

As mentioned in Fig. 1-4(c), the sharp nanostructures can enhance the local electric field for electron emission. The trade-off between electric field enhancement and thermal dissipation of different-shape field emitter tips are discussed in Ref [19]. Amoung different vertical nanostructures, nanowire-shape field emitter tips can have the strongest electric field enhancement, but the thermal dissipation through conduction is the worst. In contrary to the nanowire-shape tips, the pyramid-shape field emitter tips can have better thermal dissipation and mechanical stability, but their electric field enhancement is worse than the nanowire-shape ones'. In this section, the issues of NW field emitters in chapter 3 are firstly discussed, and the pyramid-shape tips are then studied by Silvaco TCAD and are compared with the nanowire-shape tips. The new digital etching (DE) process is then developed to help improve the electric field enhancement on the pyramid-shape field emitters.

4.1.1 Nanowire-shape GaN emitter tips

The tilted SEM image of the GaN NW SAGFEA reported in chapter 3 is shown in Fig. 4-1(a), and the device geometry is then drawn in the Silvaco TCAD for electrostatic simulation based on the SEM image (Fig. 4-1(b)). The structure is drawn under the cylindrical symmetry along the symmetry axis, which is in the middle of GaN nanowire emitter (x = 0). The unit in both x and y directions is μm. The yellow regions are emitter contact and gate metal. The anode metal is set 1 μm above the emitter tip with a fixed bias (V_A = 1 V) for the whole electrostatic simulation. In this simplified simulation, the emitter contact is assumed perfectly ohmic, the gate

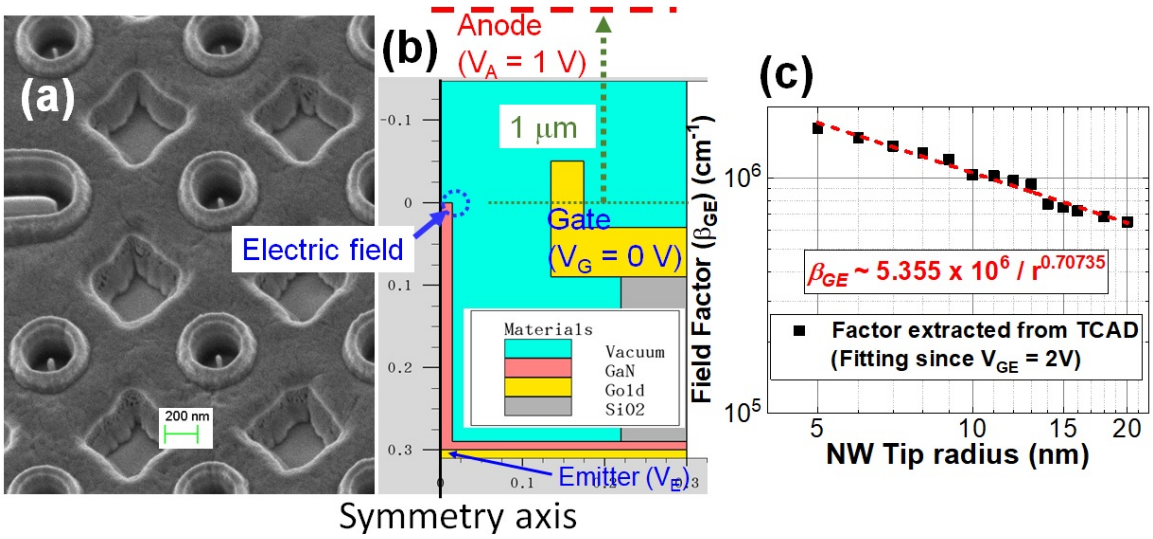


Figure 4-1: (a) The SEM image of the GaN NW SAGFEA, (b) the device structure based on this GaN NW SAGFEA in the Silvaco TCAD simulation, and (c) the extracted gate-emtter field factor (β_{GE}) as a function of NW field emission tip radius. The metal terminals are set up as gold when building the mesh and device structure, while the work functions of different terminals are set separately when doing electrostatic simulation (Emitter: 3.8 eV, Gate and Anode: 4.5 eV). High gate-emitter field factor is desired since it means that high electric field on tips can be achieved at low V_{GE} bias.

metal is set with work function of 4.5 eV (for Cr), the anode metal is also set with work function of 4.5 eV (for W), and the electron affinity of GaN is set 3.8 eV [58]. In the electrostatic simulation, the gate voltage (V_G) is fixed at 0 V and the emitter voltage (V_E) is swept to negative values. The electric field at the corner of the emitter tip (blue dashed circle in Fig. 4-1(b)) is recorded for the whole gate-emitter voltage (V_{GE}) sweep. The doping concentration in the GaN layer is set at 1×10^{19} cm^{-3} and the dopants are set fully ionized. The effects of n$^-$ GaN layer and the sidewall depletion in the nanowire is not considered in this simulation. By sweeping the V_{GE}, the gate-emitter field factor (β_{GE}) can be extracted. In the simulated results,

$$\beta_{GE} = \frac{d\vec{E}}{dV_{GE}} \tag{4.1}$$

where the $\vec{E}$ is the electric field at the emitter tip corner (unit: V/cm). Therefore, the unit of β_{GE} is cm^{-1}. The β_{GE} is not directly extracted from the value of $\frac{\vec{E}}{V_{GE}}$

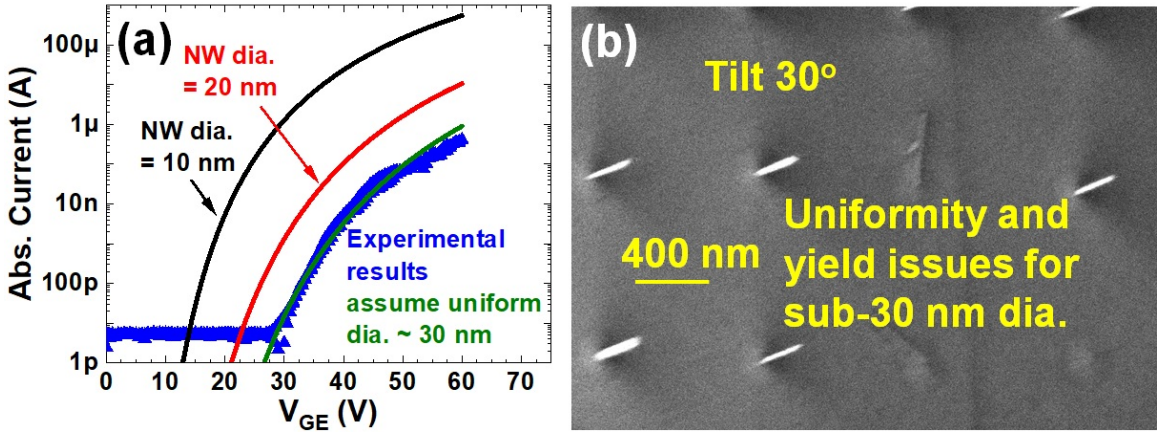


Figure 4-2: (a) Transfer characteristics of the estimated emission current with different NW tip radius based on TCAD-simulated field factor (Fig. 4-1(c)) and (b) the SEM image of the GaN NW array with uniformity and yield issues. Though the narrow NWs with small diameter can provide better performance, the fabrication faces challenges in maintaining reasonable uniformity and yield.

since there is work function difference between the GaN tip (3.8 eV) and gate metal (set to be 4.5 eV for Cr) and thus the electric field on the tip is zero at $V_{GE} \sim 0.7$ V but not at $V_{GE} = 0$ V. By varying NW tip radius in the simulation, the β_{GE} versus tip radius (r) can be summarized (Fig. 4-1(c)). Based on the data points extracted from simulation, a red dashed fitting line for the value of β_{GE} can be approximated by a fitting equation:

$$\beta_{GE} \sim \frac{5.355 \times 10^6}{r^{0.70735}} \tag{4.2}$$

where r is in the unit of nm, and the β_{GE} is in the unit of cm^{-1}. For example, when the NW tip radius is about 10 nm, the gate-emitter field factor (β_{GE}) is about 1.05 $\times$ 10^6 cm^{-1}. High β_{GE} indicates strong electric field enhancement.

Once the relation between β_{GE} and tip radius is obtained, the measured transfer characteristics (Fig. 3-7) and equations (1.8) - (1.10) can be used to extracted the gate-emitter field factor (β_{GE}) and emitter area (α) by assuming the work function of 3.8 eV. The extracted β_{GE} is about 8.316×10^5 cm^{-1} and α is about 9.705 nm^2 for this 50 $\times$ 50 NW tip array. Based on the extracted β_{GE} and the equation (4.2), the NW tip radius can then be estimated, which is about 14 nm (diameter = 28 nm). When assuming the emitting area remains constant, the transfer characteristics of

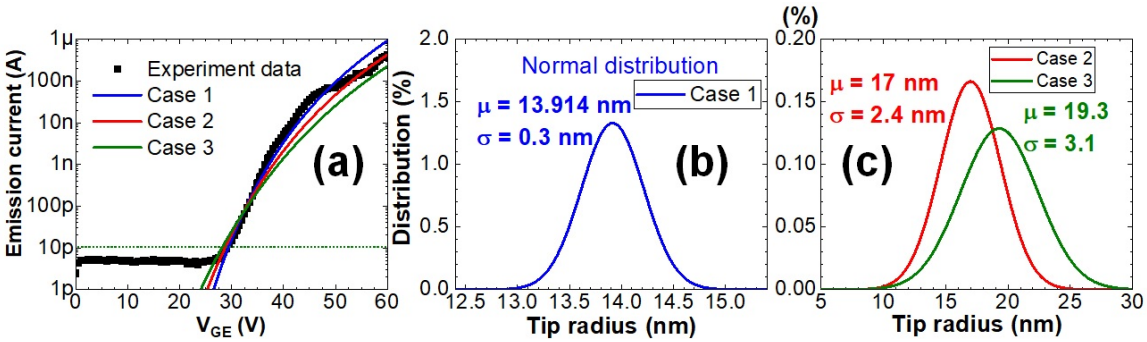


Figure 4-3: (a) Transfer characteristics compares experimental data with estimated curves with three different NW-radius-variation cases. The NW-radius distributions are assumed as normal distributions with (b) 0.3-nm standard deviation (σ) and (c) 2.4-nm and 3.1-nm standard deviations. All three cases have similar turn-on voltage and overall I-V trend, but the maximum current densities are affected by the level of uniformity of electron emission in the array.

estimated emission current can be calculated for different NW tip radius (Fig. 4-2(a)). The estimated I-V curve of GaN NW SAGFEA with 30-nm-diameter NW tips has a good agreement with the experimental results (blue triangles in Fig. 4-2(a)). However, based on the SEM image shown in Fig. 3-10(b), the measured device has some NWs with diameter of about 55 nm. When considering the emitting area (α), it is noted that the average emitting area per tip will be only 3.88×10^{-3} nm^2. Therefore, it is very likely that the tip-diameter variation exists in the field emitter array, and only the sharpest tips in the array are effectively emitting the electrons. The effect of tip-size variation in these field emitter arrays is well known and has been studied on Si SAGFEAs before [124–126]. Though the tip-diameter variation is observed, by combining the equation (4.2) and the equations (1.8) - (1.10), we can still estimate the I-V curves of GaN NW SAGFEAs with 20-nm-diameter and 10-nm-diameter NW tips (red and black curves in Fig. 4-2(a)). The NW tips with narrower diameter are expected to further improve the performance of GaN NW SAGFEAs. However, the issues of bad uniformity and low yield for GaN NW arrays become much more severe when the NW diameter is reduced to below 30 nm (Fig. 4-2(b)).

As the non-uniform tip radius of fabricated GaN vertical NW arrays is observed, the effects of uniformity issue of tip radius in the FEA on device performance should be discussed. Three different sets of NW tip radius distributions are used, and the

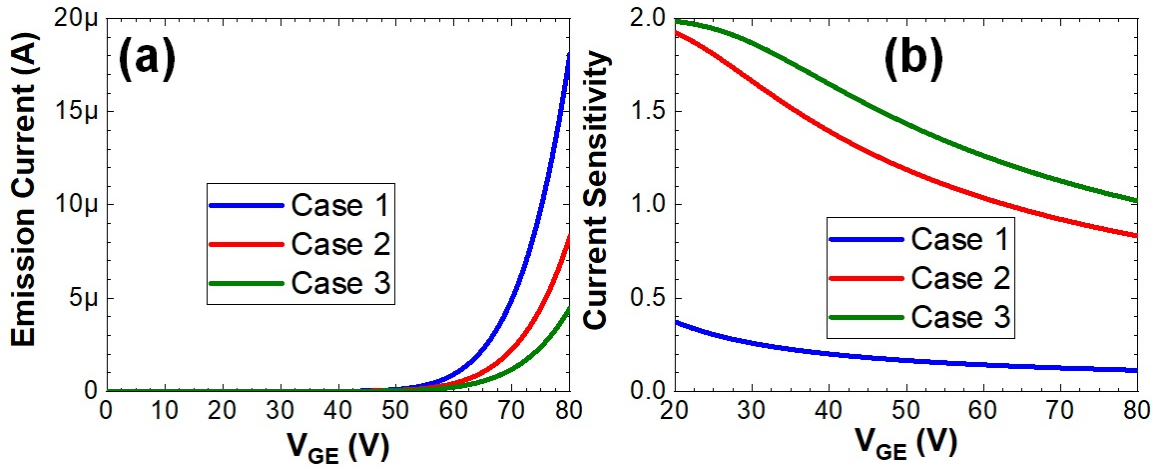


Figure 4-4: (a) The estimated transfer characteristics in linear scale and (b) current sensitivity of three different NW-radius-variation cases. The high current sensitivity means high variation in current through each tip and thus means high probability of the tip burnout [49]. Therefore, uniform tips are critical to obtain high-performance and stable field emitter arrays.

estimated I-V curves from all three NW tip radius distributions are plotted with the experimental data in Fig. 4-3(a). All three cases are based on normal distributions with different means and variations. The case 1 has the most uniform NW tip radius with a mean radius (μ) of 13.914 nm and radius variation (σ) of 0.3 nm (Fig. 4-3(b)). The case 2 and 3 have NW tip radius distributions with mean radius of 17 nm and 19.3 nm, and with radius variation of 2.4 nm and 3.1 nm, respectively (Fig. 4-3(c)). It should be noted that, since we assume the emitting area (α) is a constant and it is very small (average emitting area per tip is only $\sim 3.88 \times 10^{-3}$ nm^2), the simulation here is only considering the sharpest portion of the NW tips in the array, which only represent the very small amount of tips. Based on these calculated results, it is possible that most of NW tips with much wider tip radius, for example, a NW with $\sim$ 55-nm NW diameter in Fig. 3-10(b), do not effectively contribute to the electron emission current in this device. However, since we do not have statistical data of NW dimension in the FEA, it is hard to know if the tip diameter distribution in the whole FEA follows the normal distribution or log-normal distribution [124].

The estimated transfer characteristics with higher V_{GE} of three cases are plotted in Fig. 4-4(a). Though the turn-on voltages have good fits for all three cases in Fig.

4-3(a), the maximum emission current can be 3× different between different cases of tip radius distribution. Furthermore, the tip variation in the FEAs can be the cause of tip burnout and device failure , and a parameter, current sensitivity (S), is used to quantify the probability of these burnout and failure in FEAs [127]. The current sensitivity S is defined as:

$$S = \frac{\Delta I_E}{\bar{I_E}} \tag{4.3}$$

where the $\bar{I_E}$ is the average emission current and the ΔI_E is the emission current variation:

$$\Delta I_E = \int_0^\infty |I_E(r) - \bar{I_E}| f(r) dr \tag{4.4}$$

where the $I_E(r)$ is the emission current from a emitter tip with tip radius r, and $f(r)$ is the probability density function describing the tip radius distribution [49]. The $\bar{I_E}$ can be calculated by:

$$\bar{I_E} = \int_0^\infty I_E(r) f(r) dr \tag{4.5}$$

The current sensitivity of different tip radius distributions across the range of gate-emitter voltage (V_{GE}) can then be calculated (Fig. 4-4(b)). If the current sensitivity is high, the tip burnout will more likely happen since the high sensitivity S indicates that most emission current is only flowing through a small portion of sharpest emitter tips in an FEA [49, 127]. As a result, based on calculated results in Figs. 4-3 and 4-4, the uniform sharp field emitter tips are critical to make high-performance and stable field-emitter-based vacuum transistors. GaN vertical nanowires fabricated by the combination of ICP-RIE and heated TMAH wet etching are not good enough because of uniformity issue on tip radius in these NW FEAs.

4.1.2 Pyramid-shape GaN emitter tips

In contrary to the nanowire-shape emitter tips, the pyramid-shape emitter tips can potentially have better tip-radius uniformity since only one-step ICP-RIE process is required. The pyramid-shape tips are more mechanically stable and can have better fabrication yield and uniformity. Therefore, the same electrostatic TCAD simulation

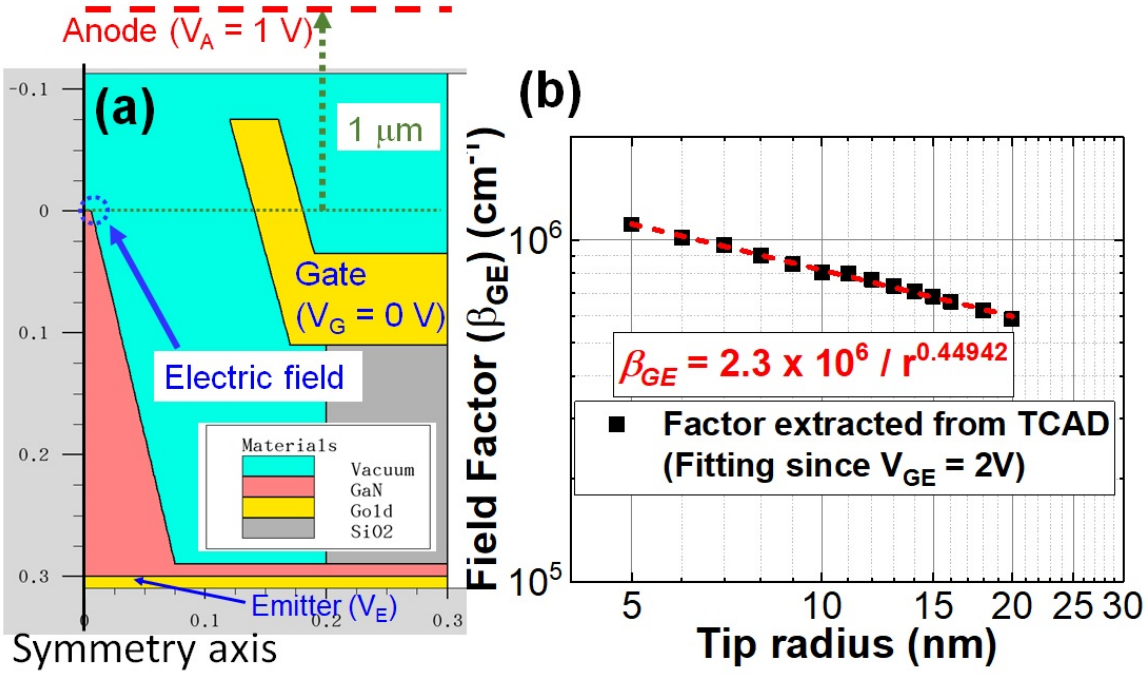


Figure 4-5: (a) The TCAD simulation setup of GaN SAGFEA with pyramid-shape emitters and (b) the extracted gate-emitter field factor (β_{GE}) as a function of tip radius, which has similar trend as Fig. 4-1(c), but the value of β_{GE} at the same tip radius is lower than the one of NW field emitter.

is set up for the pyramid-shape GaN SAGFEA to study its gate-emitter field factor (β_{GE}) (Fig. 4-5). The sidewall slope of GaN pyramid is set $\sim 77^o$ in TCAD simulation (Fig. 4-5(a)), which is close to the estimated sidewall slope in cross-sectional SEM images of etched GaN pyramids. Other simulation settings are similar to the one in NW-shape emitter tip simulation. The extracted β_{GE} can be fitted:

$$\beta_{GE} \sim \frac{2.3 \times 10^6}{r^{0.44942}} \tag{4.6}$$

as a function of pyramid tip radius (r) (Fig. 4-5(b)). Comparing between equation (4.2) and equation (4.6), when the tip radii are identical, the pyramid-shape emitter tip has smaller gate-emitter field factor (β_{GE}) than the one of NW-shape emitter tip. The low β_{GE} means the high V_{GE} is required to induce the strong electric field for field emission. Therefore, though the tip radius is more uniform in the pyramid-shape FEA and the yield of fabrication is higher, the performance of pyramid-shape

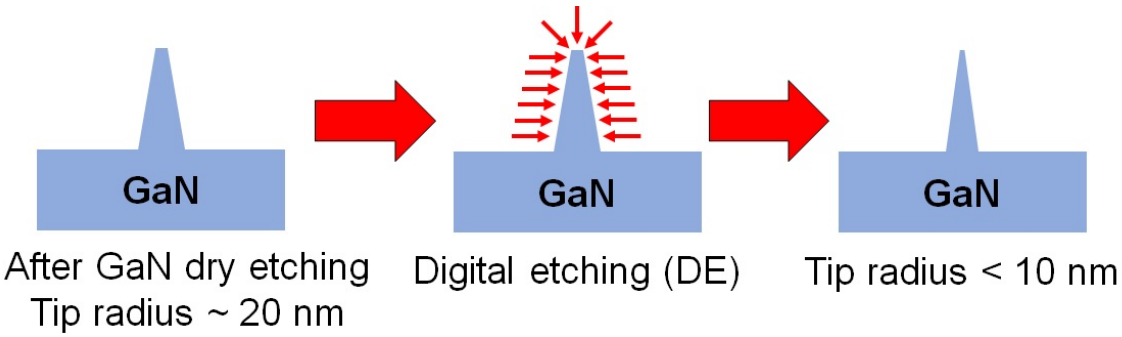


Figure 4-6: The illustration showing the proposed digital etching (DE) process for sharpening the GaN pyramid tip to improve the electric field enhancement on the pyramid tip.

FEAs might not be better than NW-shape ones. The process technology to finely sharpen the pyramid emitter tips is necessary to make better GaN SAGFEAs based on pyramid-shape tips.

4.1.3 Sharpened GaN pyramids by chemical digital etching

There have been many work demonstrating digital etching (DE) and atomic layer etching (ALE) on c-plane III-Nitrides for high electron mobility transistors (HEMTs) [128–137], while there is only very limited study on etching along other directions for vertical structure sharpening (as shown in Fig. 4-6). One common DE or ALE process on III-Nitrides is to first oxidize the surface by O_2 or N_2O plasma, followed by Dilute HCl to remove surface oxide [128, 129]. Additionally, DE process based on O_2 and BCl_3 plasma has also been studied for its etching properties on c-plane surface [130, 131]. Besides oxygen-based plasma for surface oxidization, thermal oxidization followed by KOH wet etching is also demonstrated on c-plane AlGaN surface [134, 135]. However, there is only very few work investigating on the combined oxidization and wet etching process for etching on the sidewalls of III-Nitride vertical structures [138]. Furthermore, the oxidization of III-Nitrides could introduce additional surface roughness [139, 140]. Other types of DE or ALE technologies also mostly feature the use of an anisotropic plasma, so they are not directly applicable for sharpening vertical nanostructures [132, 133]. A thermal ALE on (0001) GaN and AlN surfaces

using XeF_2 and BCl_3 has been reported [136, 137]. This plasma-free ALE process is promising for sharpening the vertical nanostructures, but it requires a custom-made system that is not easily available in most laboratories.

Table 4.1: Process steps of 1 cycle of digital etching (DE).

Step no.	Chemicals	Time	Purpose
1	1 H_2SO_4 + 1 (30%)H_2O_2	4 min	Oxidize surface
2	DI water	30 sec, then DI water rinse	Remove chemicals
3	1 (37%)HCl + 3 H_2O	2 min	Etch oxidized layer
4	DI water	30 sec, then DI water rinse	Remove chemicals

Since the thermal ALE on III-Nitrides is not a widely available technology yet and the anisotropic-plasma-based DE and ALE is not suitable for vertial nanostructure sharpening, we develop a wet-based DE for GaN and AlGaN in this thesis research. The wet-based DE developed in this thesis research consists of two main steps, surface oxidization and removal of surface oxide, and a DI-water cleaning step after each main step (Table 4.1). The GaN pyramid surface is first oxidized by the mixture of H_2SO_4 and H_2O_2 (step 1), and then the chemicals remaining on the surface is removed by DI water cleaning (step 2). After the cleaning, the surface oxide layer on the GaN pyramid surface is then etched away by dilute HCl (step 3), and the sample is cleaned again by DI water (step 4). One cycle of DE consists of these 4 steps. Since the H_2O_2 will decompose and the temperature of mixture of H_2SO_4 and H_2O_2 will decrease over time, all chemicals and DI water are renewed after 3 cycles of DE, i.e., renewed every $\sim$ 20-25 mins, to maintain the stable etching rate of DE. Besides the chemicals mentioned here, different chemicals such as (30%)H_2O_2 and BOE are also tested for surface oxidization and oxide removal steps, respectively. The details of these experiments are summarized in Appendix B.

The DE process is tested on the GaN vertical pyramids fabricated by a top-down approach. The process flow is shown in Fig. 4-7(a), and the tip shrinking (sidewall etching) versus numbers of DE cycle is summarized in Fig. 4-7(b). The Ni hard mask is first defined by e-beam lithography (EBL) on PMMA with lift-off process, and

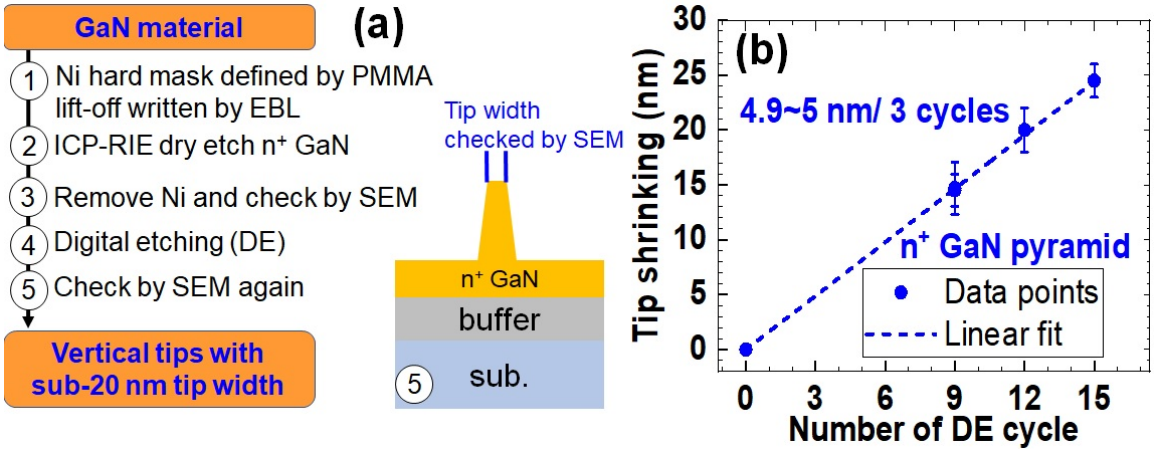


Figure 4-7: (a) The process flow of the DE experiments on the GaN pyramid tip and (b) the GaN tip shrinking results as a function of number of DE cycles.

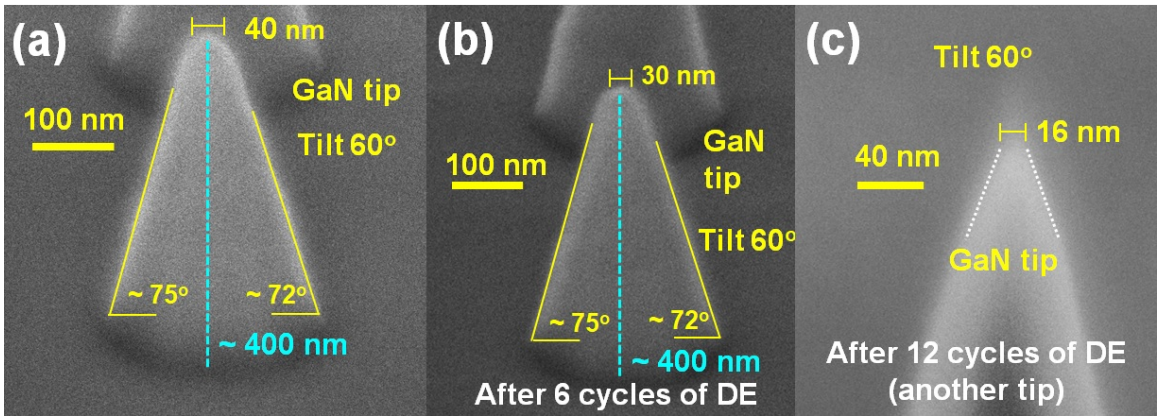


Figure 4-8: Tilted SEM images of the GaN pyramid tip (a) after ICP-RIE dry etching and Ni-mask removal and (b) after subsequent 6 cycles of DE, and (c) another GaN pyramid tip with sub-20-nm tip diameter after 12 cycles of DE.

the GaN pyramids are formed by Cl_2/BCl_3 ICP-RIE with Ni hard mask. After dry etching, the Ni mask is removed and the GaN pyramids are checked by SEM (Fig. 4-8(a)). Following that, a few cycles of DE are applied on the sample and the GaN pyramids are checked by SEM again to estimate the etching rate on sidewalls of GaN pyramids.

The same GaN pyramid before DE (Fig. 4-8(a)) and after 6 cycles of DE (Fig. 4-8(b)) is characterized by SEM, and the tip shrinking rate of these GaN pyramids is about 4.9-5 nm/3 cycles (Fig. 4-7(b)). After multiple cycles of DE, the GaN pyramid with sub-20-nm tip width, i.e., sub-10-nm tip radius, can be reproducibly fabricated

with high yield and uniformity (Fig. 4-8(c)). With this wet-based DE technology, GaN SAGFEAs with sharp pyarmid-shape tips can be fabricated with both better fabrication yield and uniformity than the GaN NW SAGFEAs reported in chapter 3.

4.2 2nd generation of GaN gated field emitter arrays

Based on the wet-based DE process we developed, the GaN pyramid-shape emitter tip with sub-10 nm tip radius can be fabricated (Fig. 4-8(c)), whose gate-emitter field factor (β_{GE}) can be comparable or better than the GaN NW-shape emitter tip fabricated in chapter 3. Additionally, the new epitaxial structure is used in this and following generations of GaN SAGFEAs in this chapter. This new epitaxial structure is composed of a 1.4 μm n^{++}-GaN ([Si] $\sim 1 \times 10^{19}$ cm^{-3}) and a buffer layer on the (111) Si substrate. The n^{-}-GaN layer is removed to reduce the series resistance of GaN vertical nanostructures. The structure is grown on 6-inch Si wafer by Enkris, Inc via MOCVD. This wafer is cut into pieces for the different experiments and different generations of GaN SAGFEAs in this chapter.

4.2.1 Device fabrication

The process flow is modified slightly for the GaN SAGFEAs with pyramid-shape tips sharpened by DE (Fig. 4-9(a)). The GaN pyramid-shape emitter tips are fabricated by Cl_2/BCl_3-based ICP-RIE without the following TMAH wet etching. The pyramid tips are then sharpened by multiple cycles of DE until the tip radius is expected to be lower than 10 nm (based on the etching rate estimated in Fig. 4-7(b)). After that, a $\sim$ 30-nm Al layer is sputtered to protect the tips from the following dry etching steps (step (2) in Fig. 4-9). The protecting layer is necessary since the emitter tips can be damaged by physical bombardment during plasma dry etching due to the locally enhanced electric field on the tips (Appendix C). After that, similar process are applied to the following steps: gate stack (TEOS and Cr) deposition, TEOS planarization, gate metal (Cr) etching, and the metal stack (Ti/Au) as both contact on n^{++}-GaN and gate pad. The GaN SAGFEA after TEOS planarization is checked

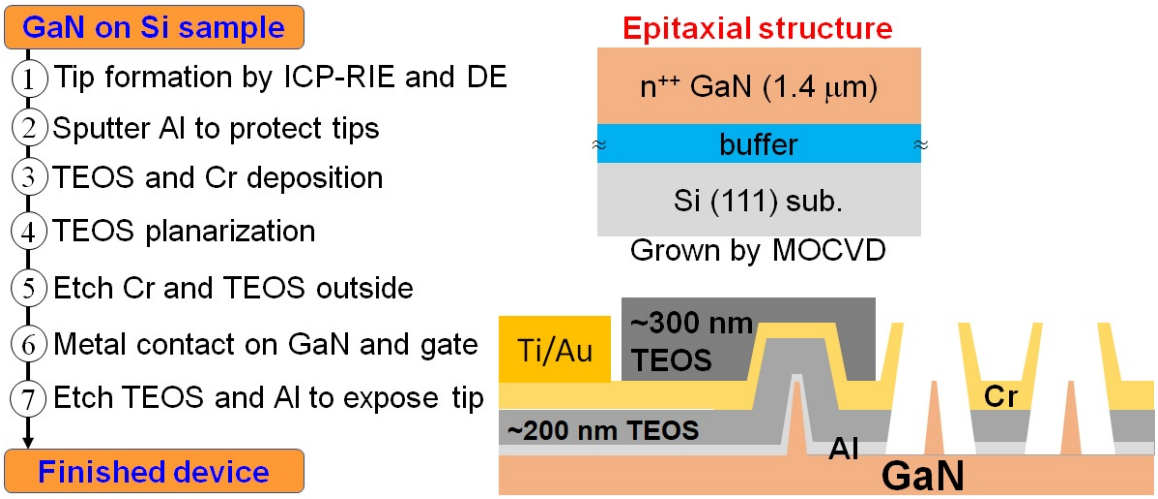


Figure 4-9: The process flow, epitaxial structure, and the finished device geometry of the GaN pyramid SAGFEA (2nd-generation GaN FEA). The 6-inch GaN-on-Si wafer is grown by metal-organic chemical vapor deposition (MOCVD) provided through the courtesy of Enkris, Inc. The following generations of GaN SAGFEAs are all fabricated on coupons cut from the same 6-inch GaN-on-Si wafer.

by SEM to make sure the gate metal is exposed and the sidewalls of gate metal are still protected by TEOS (Fig. 4-10(a)). The TEOS is then used as hard mask when dry etching Cr using Cl_2/O_2-based ICP-RIE. Finally, the carefully-timed CF_4-based dry etching is used to etch TEOS to expose the top surface of GaN pyramid tips. The residual TEOS on GaN pyramid sidewalls and Al are then removed by quick BOE and TMAH-based developer. A tilted SEM image of the finished GaN SAGFEA is shown in Fig. 4-10(b). The detailed process flow and relevant experiments are summarized in Appendix B, C, and D.

One of the 2nd-generation GaN SAGFEAs after I-V characteristics measurement (section 4.2.2) is investigated by the cross-sectional SEM and high-resolution transmission electron microscope (TEM) (Fig. 4-11). Both cross-sectional SEM and TEM images are obtained and provided through the courtesy of Prof. Bruce Gnade group at SMU. Based on cross-sectional SEM image, the pyramid shape, sidewall slope of 77^o, and the shape of gate metal are confirmed. The TCAD simulation in section 4.1.2 is based on this image (Figs. 4-11(a) and 4-5(a)). Additionally, based on the TEM image, the tip radius of this sharp pyramid emitter is about 5-6 nm, i.e., tip width is

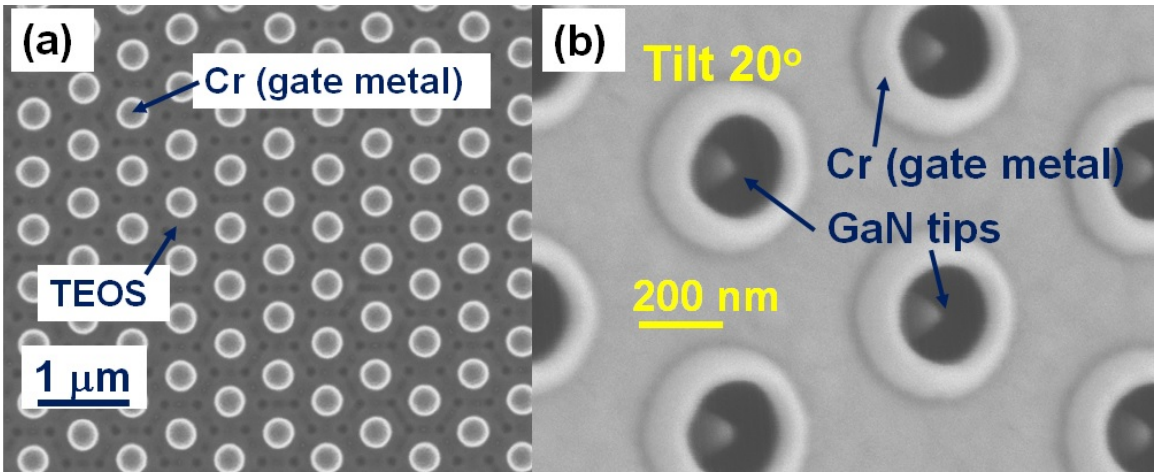


Figure 4-10: The SEM images of (a) after TEOS planarization step and (b) finished GaN pyramid SAGFEA.

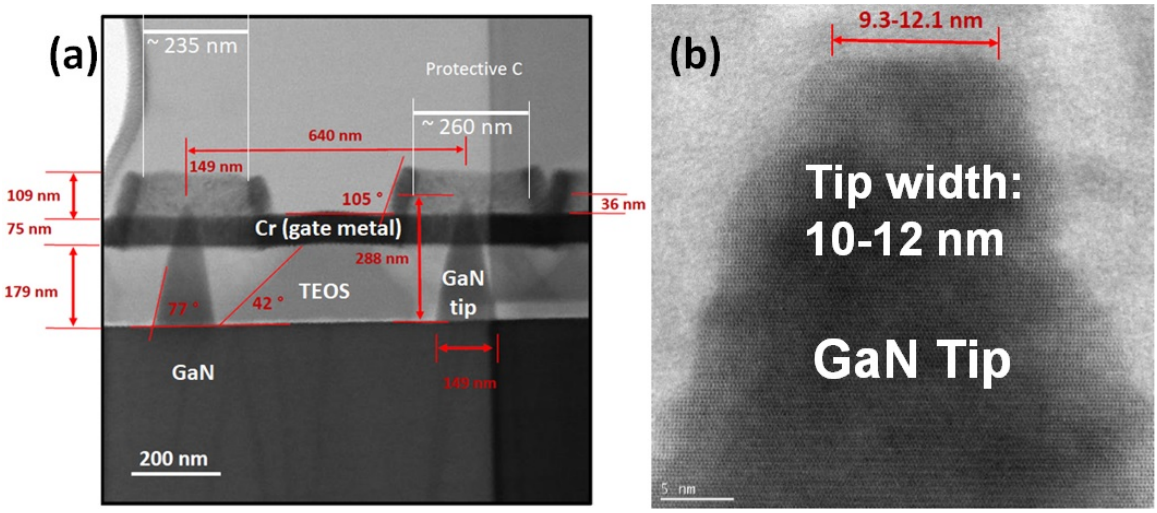


Figure 4-11: (a) The cross-sectional SEM and (b) high-resolution transmission electron microscopy (TEM) images of this 2nd-generation GaN pyramid SAGFEA. The GaN tip width is about 10-12 nm. These images are obtained and provided by the courtesy of Prof. Bruce Gnade group at Southern Methodist University (SMU).

about 10-12 nm (Fig. 4-11(b)). Since the tip width defined by e-beam lithography is about 30-40 nm, this TEM image is a direct evidence that the developed wet-based DE successfully sharpens the GaN pyramid tips.

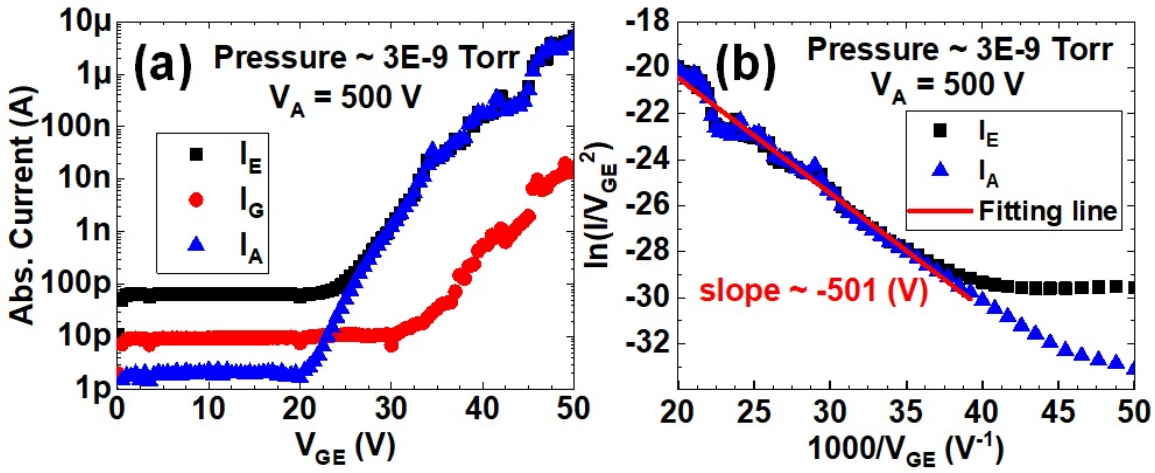


Figure 4-12: (a) Transfer characteristics and (b) the corresponding F-N plot of this 2nd-generation GaN pyramid SAGFEA with 100 × 100 sub-10-nm-tip-radius tips. This device turns on at V_{GE} = 23 V (@ $I_A = 10\ pA$) and the max $I_A = 5\ \mu A$ (max $J_A \approx 150\ mA/cm^2$).

4.2.2 Characterization and discussion

After the SEM inspection (Fig. 4-10(b)), the sample is quickly loaded to the UHV measurement chamber. The UHV chamber base pressure is about 3 × 10^{-9} Torr. The anode is a 0.5-mm-diameter tungsten metal ball which can be moved by micro-manipulators in all x, y, and z directions. The height distance between anode and device is about 1 mm.

The anode voltage (V_A) is fixed 500 V in the transfer characteristics measurement (Fig. 4-12(a)). After the multiple I-V sweeps as conditioning, a GaN SAGFEA, which consists of 100 × 100 pyramid tips with sub-10-nm tip radius, turns on at $V_{GE} \sim 23$ V. The conditioning procedure used in this thesis work is summarized in Appendix E. The turn-on voltage ($V_{GE,ON}$) is determined as the V_{GE} when I_A increases from the noise level and reaches a certain level (10 pA in this work). The maximum I_A reaches about 5 μA at $V_{GE} = 50$ V, whose current density (J_A) is equal to about 150 mA/cm^2 when considering the FEA area of 63 μm × 53.5 μm. The gate leakage (I_G) is always about 2 orders of magnitude lower than I_A in the region where $V_{GE} > 30$ V. The F-N plot of transfer characteristics is also plotted (Fig. 4-12(b)). A negative-slope straight fitting line can be drawn with slope ($-b_{FN}$) of -501 V. Assuming the work functions

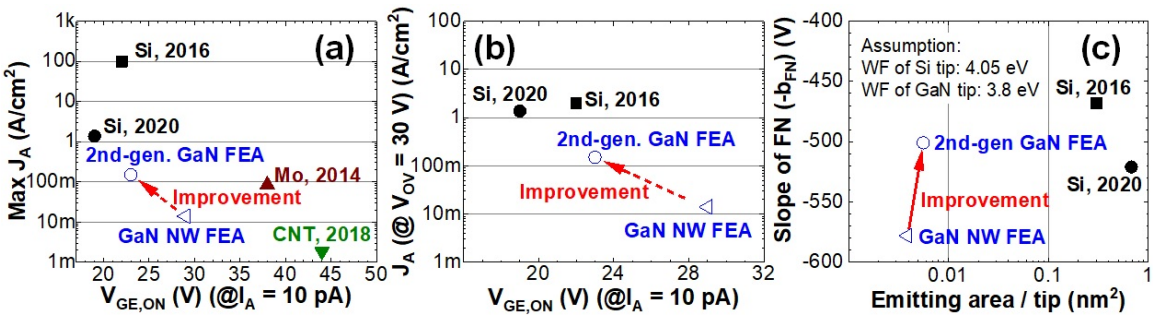


Figure 4-13: The benchmark plots of (a) max J_A and (b) J_A at $V_{OV} = 30$ V, and (c) The estimated emitting area per tip of different Si and GaN SAGFEAs [48–50, 55]. The V_{OV} is defined as $V_{GE} - V_{GE,ON}$ in (b).

are identical, the smaller value of $|b_{FN}|$ indicates stronger gate-emitter field factor (equation (1.10)). The smaller $|b_{FN}|$ and the higher J_A at the same bias condition show that the 2nd-generation GaN SAGFEAs with pyramid-shape tips are better than the GaN NW SAGFEAs reported in chapter 3. It should be noted that the data points in the high V_{GE} bias region are noisy, indicating that more conditioning sweeps might be necessary. However, the device suddenly breaks in the following measurement and the gate is shorted to the emitter. The failure of this device and other devices fabricated on the same sample piece will be discussed in the next section (sec. 4.2.3).

Though the device stability is still an issue of this GaN SAGFEA, the maximum current density ($J_{A,max}$) and J_A at the same bias condition (@ $V_{OV} = 30$ V) has been increased by 10× from the GaN NW SAGFEA reported in chapter 3 (Fig. 4-13(a) and (b)). While the performance is still not as good as state-of-the-art Si SAGFEAs [48,49], it is already better than Mo and CNT SAGFEAs reported in literature [50,55]. Furthermore, based on equations (1.9) and (1.10), the average emitting area per tip in FEAs can be calculated by assuming the work functions (Si: 4.05 eV, GaN: 3.8 eV) (Fig. 4-13(c)). The average emitting area per tip of this 2nd-generation GaN SAGFEA is not clearly higher than the one of GaN NW SAGFEA, and it is about 1-2 orders of magnitudes lower than the ones of Si SAGFEAs. Therefore, more optimization and study is still necessary to further improve these GaN SAGFEAs.

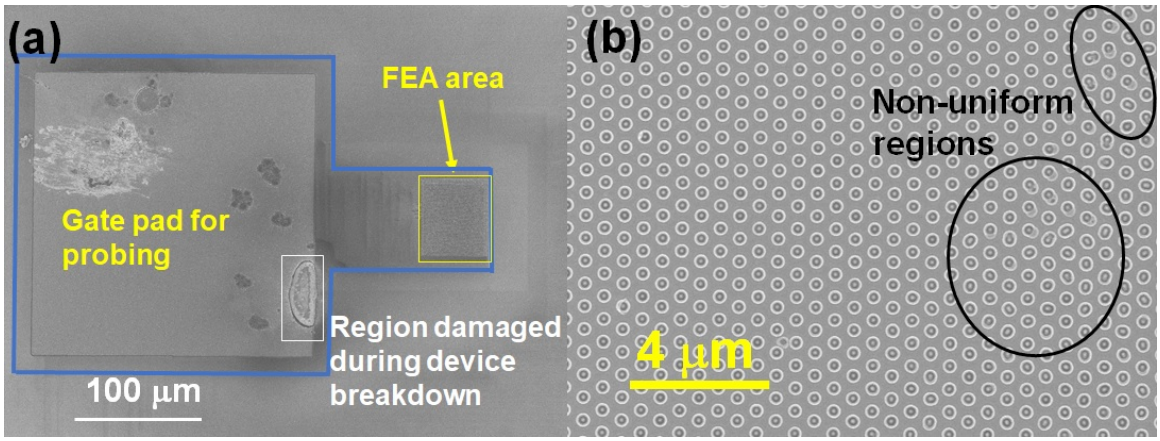


Figure 4-14: The SEM images of the 2nd-generation GaN pyramid SAGFEA after measurement. (a) The device failure is most likely due to the damage at the gate pad region. (b) There is no observable damage or failure in gated FEA region, while the tip non-uniformity is observed. Therefore, there is still room for improvement on both device structure and fabrication steps.

4.2.3 Device failure analysis

The measured GaN SAGFEA (Fig. 4-12) is checked by SEM again after it breaks to investigate the failure (Fig. 4-14). Damages can be directly observed at the gate pad region by SEM (Fig. 4-14(a)). Based on the SEM image, the breakdown seems to only happen at the gate pad region in this device. While there is no observable damage or breakdown in the FEA region (yellow rectangle region in Fig. 4-14(a)), the non-uniformity in GaN pyramid tips is observed in the FEA region (Black circles in Fig. 4-14(b)). The non-uniform tip shapes could be the cause of low avearge emitting area per tip calculated in Fig. 4-13(c). The emission current will be mostly only flowing through the sharpest tips, which is only a small portion of tips, in the non-uniform FEA, and thus the average emitting area per tip is low. This issue requires further optimization on process steps, such as improving e-beam lithography to have uniform tip arrays and carefully cleaning samples before dry etching to prevent micro-masking from residuals. On the other hand, the early breakdown in the gate pad region can be reduced or eliminated by increasing the insulator thickness in this region. This requires some modifications on process flow and lithography pattern design, which are conducted in the 3rd-generation GaN SAGFEAs (section 4.3).

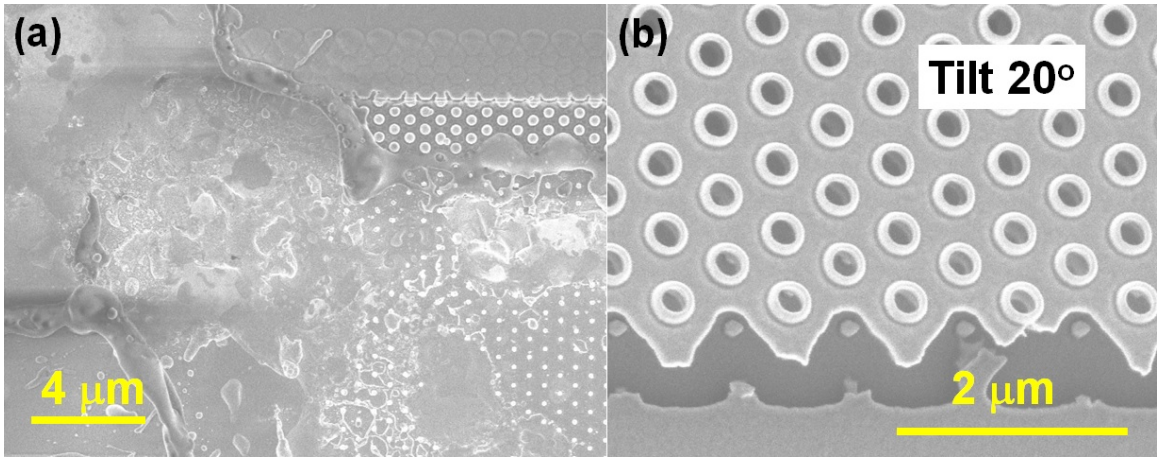


Figure 4-15: The SEM images of other device failures, such as (a) gate explosion and (b) gate metal breaks and lifts up. Therefore, in the next generation of devices, the lithography patterns are changed to have an additional overlap to prevent the issue in (b) happens again.

Other GaN SAGFEAs on the same sample are also characterized. However, the overall yield of the fabricated devices are low, and many of them failed either during the conditioning procedure for the I-V characteristics or due to the lack of emission current even at $V_{GE} > 50$ V. Some of the devices fail since the gate-emitter short suddenly happened, and one of these failed device is checked by SEM afterward (Fig. 4-15(a)). The failure of this device is likely due to the arcing between gate and emitter in the FEA region, which causes catastrophic physical damages. Besides these catastrophic breakdown, some devices show a failure of discontinuous gate metal (Fig. 4-15(b)), leading to the lack of gate control and emission current at high V_{GE}. This discontinuity can be resulted from the undercut of the BOE etching in the last step of tip exposure (step (7) in Fig. 4-9). The broken gate metal becomes a screening plate with a floating voltage and can not control the field emission from the emitter tips. Additionally, if the gate metal is suspending on the FEA region without a proper support layer underneath, like a SiO_2 pillar between tips shown in Fig. 4-11(a), the gate can be attacted to the underneath GaN layer when V_{GE} bias is applied. When the gate suddenly touches the GaN layer, it can cause a sudden electrical discharge between the gate and GaN layer, leading to a catastrophic breakdown. Some of these failures are summarized in Appendix C. In the 3rd-generation GaN SAGFEAs (sec.

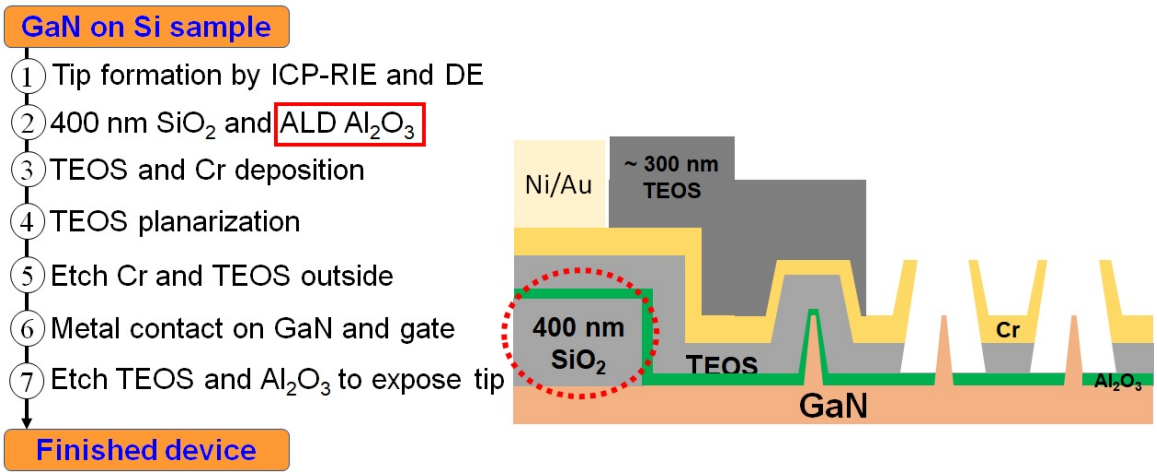


Figure 4-16: The process flow and the finished device geometry of the 3rd-generation GaN SAGFEAs with modified steps (highlighted by red color). The 400 nm SiO_2 under the gate pad is added to prevent the early breakdown of oxide under the gate pad, and the tip-protection layer is changed from a sputtered Al layer to an ALD Al_2O_3 layer.

4.3), modifications on device structures, process flow, and lithography patterns are conducted to deal with some of these issues.

4.3 3rd generation of GaN gated field emitter arrays

4.3.1 Modification of the device structure

Based on the issues observed in the 2nd-generation GaN SAGFEAs, the process flow and device structures are modified to improve the device fabrication yield and overall yield rate of working devices (Fig. 4-16). First, an additional 400-nm-thick PECVD SiO_2 is deposited and defined under the gate pad region to increase the insulator thickness and to prevent the early breakdown happened in the prior device (red dashed circle in Fig. 4-16). The protecting layer is also changed from sputtered Al to 10-nm-thick thermal atomic layer deposition (ALD) Al_2O_3 (step (2) in Fig. 4-16). The sputtered film can trap gas in the layer, and these gas can potentially release from the film in UHV environment when under device measurement. Additionally, the electric field surrounding the FEA tips is very strong ($>$ 10 MV/cm) when doing

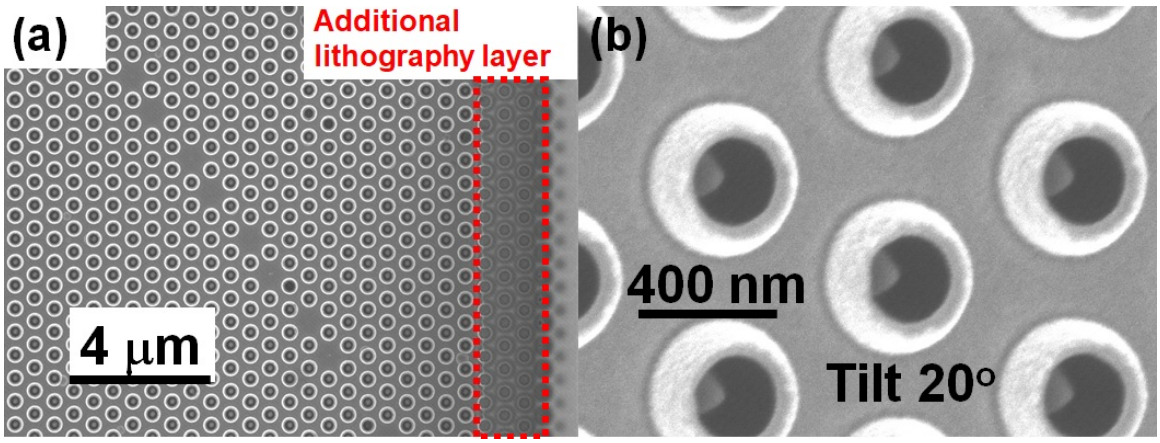


Figure 4-17: SEM images of the finished 3rd-generation GaN pyramid SAGFEAs. (a) The additional lithography step is added to prevent gate from breaking and lifting-up (as shown in Fig. 4-16(b)).

measurement, the residual gas can be ionized and cause ion bombardment and local energy discharge. In contrast to the sputtered film, thermal ALD Al_2O_3 is also robust to protect the underneath GaN tips from plasma-etching damages, but the gas trapping issue is not a concern. Furthermore, since the increase of insulator thickness under the gate pad region is proposed to improve device stability, the non-metal insulating protection layer is required. Besides the dielectric layers, the device arrangement is changed that the extending fin structures near the FEA (as one shown in Figs. 3-6 and 3-10) are removed to prevent arcing from the sidewalls of these extended fins.

Besides the device structure modification, there are some other changes in different fabrication steps in this 3rd-generation GaN SAGFEAs. For example, to improve the uniformity of emitter tips in FEAs, the water-based discharge layer is coated on the PMMA to help reduce the electron charging when defining tip arrays during the e-beam lithography step.

Moreover, an additional lithography step is added in the middle of TEOS planarization step (step (4) in Fig. 4-16) to have protection on the peripheries of FEAs (Fig. 4-17(a)). With this additional lithography step, the gate breaking issue observed in the prior generation devices (Fig. 4-15(b)) can be eliminated. It should be noted that there are some empty spots in the FEA, which might be resulted from the

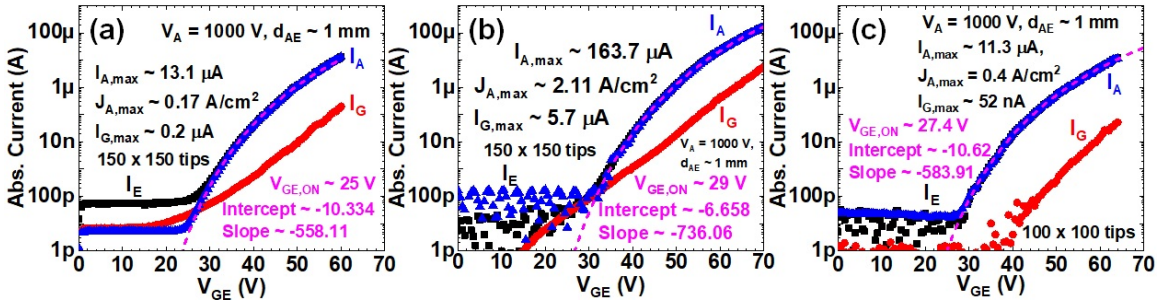


Figure 4-18: Transfer charactersitics of 3 different 3rd-generation GaN SAGFEAs on a GaN-on-Si piece. the 3rd-generation GaN SAGFEAs can endure higher V_{GE} than the 2nd-generation device, and the max J_A can reach 2 A/cm^2.

issue of lift-off process after the e-beam lithography process for tip arrays.

Additionally, the metal stacks on GaN and gate are changed to use different metal layers. The metal contact stack on n^{++}-GaN layer is Ti/Al/Ti/Au, and the metal stack on gate (sputtered Cr) as a gate probing pad is Ni/Au. Finally, the finished 3rd-generation GaN SAGFEAs after tip exposure steps are checked by SEM to confirm the finish of fabrication (Fig. 4-17(b)). The details of this modified process flow is summarized in Appendix C.

4.3.2 Device characterization and discussion

After the SEM characterization (Fig. 4-17(b)) of the finished GaN SAGFEAs, the sample is quickly loaded into the UHV chamber. After multiple IV sweeps for device conditioning, the transfer characteristics of three different 3rd-generation GaN SAGFEAs are shown in Fig. 4-18. The anode voltage (V_A) is kept 1000 V, and the anode-emitter distance (d_{AE}) is kept about 1 mm. The first and second devices consist of 150 × 150 tips in the array (Fig. 4-18(a) and (b)), and the 3rd device has 100 × 100 tips in the array (Fig. 4-18(c)). The relation between the anode current (I_A) and gate-emitter voltage (V_{GE}) can be expressed as: $I_A = a_{FN} V_{GE}^2 \, exp(-\frac{b_{FN}}{V_{GE}})$ (equation (1.8)), and the ln(a_{FN}) (intercept) and b_{FN} (|slope|) can be extracted by fitting on F-N plot (equation (1.11)). The extracted values are noted in each figure. The turn-on voltage (V_{GE}) of each device is the V_{GE} when I_A reaches 10 pA from the noise level (Fig. 4-18(a)) or when the extrapolated I_A curve (purple dashed line)

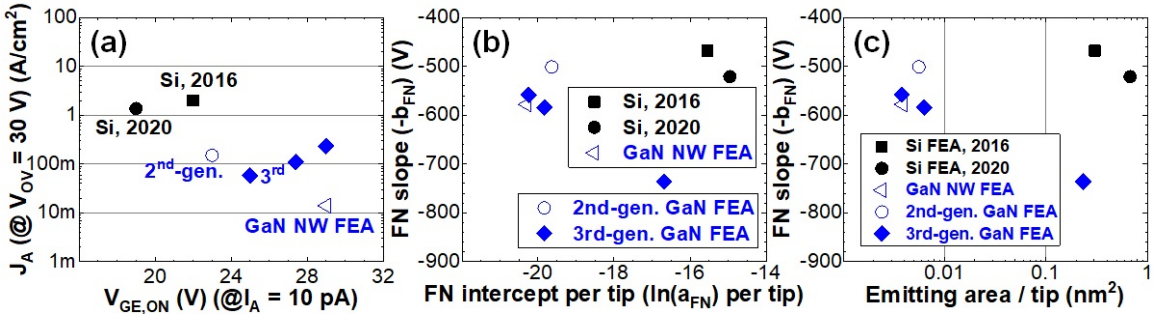


Figure 4-19: (a) The benchmark plot of the $V_{GE,ON}$ versus J_A (@ V_{OV} = 30 V), (b) Seppen–Katamuki (S-K) plot, and (c) emitting area per tip versus F-N slope of different Si and GaN SAGFEAs [48, 49, 110, 120]. Though the device becomes more stable, the performance is slightly worse than our 2nd-generation device (Fig. 4-12), indicating more optimization is necessary as structure and process flow are changed.

reach 10 pA (Fig. 4-18(b) and (c)). The device performance is summarized in the Table 4.2. With the modification on process flow and device structures mentioned in section 4.3.1, the devices are more stable, the maximum applicable V_{GE} can be increased from 50 V to above 60 V, and the maximum current density is thus increased from 0.15 A/cm^2 to above 2 A/cm^2 (Fig. 4-18(b)). Furthermore, the gate leakage (I_G) is still at least 1-2 orders of magnitude lower than the drive current, I_A. However, the turn-on voltage is slightly higher than the 2nd-generation GaN SAGFEAs.

Table 4.2: Summary of the device performance of 3rd-generation GaN SAGFEAs (Fig. 4-18). The V_{OV} is defined as V_{GE} - $V_{GE,ON}$.

Device	FEA size (number of tips)	$V_{GE,ON}$	$I_{A,max}$ (@ V_{OV})	$J_{A,max}$
(a)	150 × 150	25 V	13.1 μA (35 V)	0.17 A/cm^2
(b)	150 × 150	29 V	163.7 μA (41 V)	2.11 A/cm^2
(c)	100 × 100	27.4 V	11.3 μA (36.6 V)	0.4 A/cm^2

These devices are benchmarked with the piror GaN SAGFEAs and state-of-the-art Si SAGFEAs (Fig. 4-19) [48, 49, 110, 120]. Though the maximum current density ($J_{A,max}$) can reach 2 A/cm^2 at high V_{GE}, the current density at the same bias condition (V_{OV} = 30 V) is not better than the prior GaN SAGFEA [120]. Additionally, the current densities of these GaN SAGFEAs are still about an order of magnitude lower than state-of-the-art Si SAGFEAs [48, 49]. The Seppen-Katamuki (S-K) plot and the estimated emitting area per tip also show that the performance is not as good

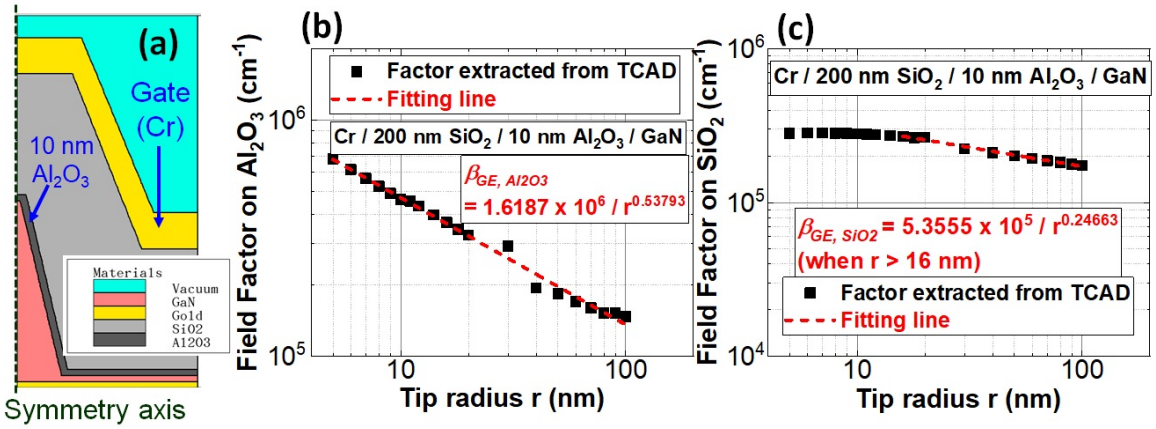


Figure 4-20: (a) The MOS structure of the oxide-covered tip and peak electric field (b) in the Al_2O_3 layer and (c) in the SiO_2 layer vs. tip radius simulated by Silvaco TCAD. The field factor of $3 \times 10^5\ cm^{-1}$ means that the peak electric field will be about 15 MV/cm at $V_{GE} = 50$ V, which can cause stability problems such as PBTI.

as Si devices (Fig. 4-19(b) and (c)). Two blue-diamond data points in the left-upper region of Fig. 4-19(c) indicate that the emitter tips are still not uniform and only the sharpest tips in the array emit electrons. Another blue-diamond data point means that this device (Fig. 4-18(b)) has a more uniform tip array, but their tip radius is larger because the higher $|b_{FN}|$ extracted from the F-N plot fitting, assuming the work functions are identical for all emitter tips of GaN SAGFEAs (equation (1.11)).

4.3.3 Weak points of devices

As shown in Fig. 4-17(a), there are regions with unexposed tips in the fabricated GaN SAGFEAs. These surrounding regions are necessary to extend out gate metal from the FEA region to the gate probing pad region. However, since these unexposed tips are also as sharp as the exposed tips in FEAs, the electric field in the dielectric layers between gate metal (Cr) and GaN tip can be very strong, which could be the weak points of these 3rd-generation devices. Therefore, the Silvaco TCAD electrostatic simulation is conducted to check the unexposed-tip region (Fig. 4-20(a)). The field factors for the peak electric fields in 10-nm ALD Al_2O_3 and in 200-nm PECVD SiO_2 are extracted from the simulation (Fig. 4-20(b) and (c)). As there is work function difference between the gate (Cr: 4.5 eV) and emitter (GaN: 3.8 eV), the flat-band

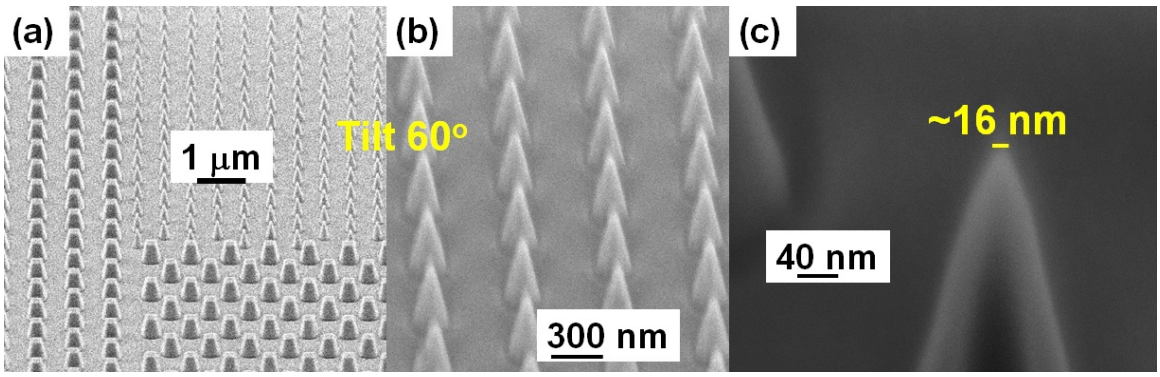


Figure 4-21: Tilted SEM images of (a) a GaN FEA with sacrificial blunt tips and uniform vertical GaN tips with sub-10 nm tip radius under (b) medium magnification and (c) high magnification. After multiple generations and batches of fabrication, process steps are finally optimized to get sharp and uniform field emitter arrays.

voltage is not at 0 V. Therefore, to precisely understand the peak electric field in the dielectric layers at ON state, the field factor is defined as $\frac{d\vec{E}}{dV_{GE}}$, and the large field factor indicates a strong peak electric field. For example, if the tip radius r is 10 nm, the peak electric fields in 10-nm ALD Al_2O_3 and 200-nm PECVD SiO_2 could both be above 10 MV/cm at $V_{GE} = 40$ V, leading to potential stability issues on dielectric such as breakdown and positive bias temperature instability (PBTI). Therefore, the device structures require more optimizations on these surrounding regions to either reduce the peak electric field in dielectric layers or remove the use of unexposed tip regions to extend out the gate metal.

4.4 State-of-the-art GaN gated field emitter arrays

4.4.1 Device structure optimization

Based on the TCAD simulation of electric fields in the dielectric layers on the unexposed tip (Fig. 4-20), the high peak electric field can potentially cause stability issues. The key steps of fabrication for the latest generation of GaN SAGFEAs are the same as the ones in Fig. 4-16, but the device arrangement is modified. The surrounding regions with wide tips ($\sim$ 200 nm width) are added at the periphery of the FEA (Fig. 4-21(a)). Since these GaN SAGFEAs are fabricated on small pieces,

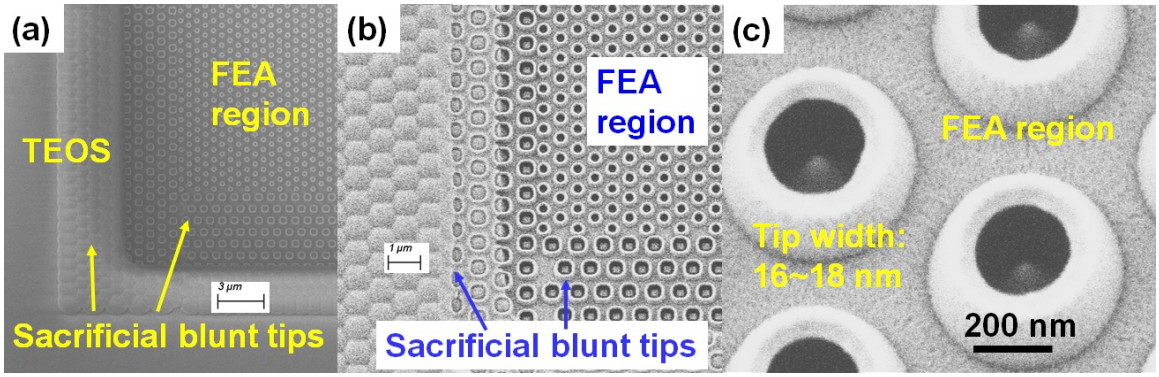


Figure 4-22: SEM images of (a) a GaN FEA after TEOS planarization and (b) a finished GaN FEA. (c) A zoom-in SEM image of the FEA region of this finished GaN FEA. The overlap regions only contain sacrificial blunt tips (as shown in (b)), so the peak electric fields in dielectrics can be reduced to improve device stability.

the planarization process by CMP process which is used for Si SAGFEAs is hard to apply [48, 49]. Therefore, to extend the gate metal from the FEA region to the probing pad region, there will always be some unexposed-tip regions to accommodate the misalignment of photolithography, which is practically at least about few hundred nm. Instead of identical sharp tips across the whole FEA region in the 3rd-generation GaN SAGFEAs, the additionally wide tips surrounding the FEA region can help extend out the gate metal and at the same time reduce peak electric fields in dielectric layers (Fig. 4-20).

Though the device arrangement is modified, the uniform sharp emitter tips with sub-10-nm tip radius of the FEA can still be fabricated (Fig. 4-21(b) and (c)) by the combination of the Cl_2/BCl_3-based ICP-RIE and wet-based DE (section 4.1.3). While the sidewalls of wide tips in the surrounding regions are also etched by DE, these wide tips are still about 180-nm wide and the peak electric fields in the dielectric layers deposited in the following steps can be still lower than the case of 3rd-generation GaN SAGFEAs.

After the GaN tip formation, $\sim$ 435-nm thick SiO_2 layer is deposited by PECVD and defined for the thick insulator layer under the gate pad. A 10-nm Al_2O_3 layer is then deposited by thermal ALD to protect GaN tips from the plasma etching damage in the following step (as step (2) in Fig. 4-16). The gate stack of $\sim$ 220 nm TEOS

and $\sim$ 100 nm Cr layers are then deposited by PECVD and sputter, respectively (as step (3) in Fig. 4-16).

The TEOS planarization is then conducted (as step (4) in Fig. 4-16) (Fig. 4-22(a)). A $\sim$ 1100-nm-thick TEOS layer is deposited by PECVD, and this TEOS layer is then timed etched by CF_4/Ar-based ICP-RIE until its remaining thickness is expected $\sim$ 300 nm. A lithography step is then conducted to define the region covering partial area of the wide tips regions surrounding the FEA, which are noted as sacrificial blunt tips in Fig. 4-22(a)). And the remaining $\sim$ 300-nm TEOS is then etched by CF_4/H_2-based ICP-RIE. The SEM image in Fig. 4-22(a) shows a device after the photoresist is removed after dry etching.

The gate metal (Cr) is then dry etched by Cl_2/O_2-based ICP-RIE using TEOS as hard mask, and the TEOS outside the device regions is removed by BOE for the following metal contact formation on n^{++}-GaN (as step (5) in Fig. 4-16).

The metal contacts on GaN and gate are then defined by lift-off process (as step (6) in Fig. 4-16). First, the lithography is conducted to define the contact regions for n^{++}-GaN, followed by the Dilute HCl (1 (37%) HCl + 3 H_2O for 1 min), Ti/Al/Ti/Au stack deposition by e-beam evaporator, and lift-off process. The gate pad metal is then defined by another lithography step, Ni/Au stack deposited by e-beam evaporator, and lift-off process.

After the metal contacts formation, the last step is the tip exposure (as step (7) in Fig. 4-16). The last lithography step is conducted to define the region for exposing the FEA tips, and the 220-nm TEOS layer is timed etching by CF_4/H_2-based ICP-RIE with a $\sim$ 10% overetch, and the quick BOE wet etching for $\sim$ 15 sec is used to remove remaining TEOS on the tips and the 10-nm Al_2O_3. It is important to keep this BOE wet etching step short since undercut etching on TEOS layer can potentially remove all TEOS under the gate metal (Cr) layer and cause device failure (Appendix C). After the quick BOE etching, the photoresist mask is then removed by soaking in the N-Methyl-2-pyrrolidone (NMP) overnight and a following short ultrasonic cleaning in NMP. The finished devices are then checked by SEM (Fig. 4-22(b) and (c)). There are three regions observed in the sacrificial blunt tip area. The left and middle regions

are separated during the lithography step in the TEOS planarization process, and the middle and right regions are separated during the lithography step in the tip exposure process. Though the lithography misalignment makes additional area cost surrounding the sharp-tip FEA, the fabrication yield has been increased significantly since the problems shown in Fig. 3-10(c) and Fig. 4-15(b) are eliminated in these latest generation of GaN SAGFEAs. After the SEM inspection, the sample is then quickly loaded into the UHV measurement chamber for device characterization.

4.4.2 Experiment results and discussion

The illustration of the measurement on the GaN SAGFEA is shown in Fig. 4-23(a). The anode metal ball is moved to make anode-emitter distance (d_{AE}) about 2 mm for all measurement in this section. In the transfer characteristics, the anode voltage (V_A) is fixed at 500 V and the gate-emitter voltage (V_{GE}) is swept. The device is first conditioned by multiple I-V sweeps until the stable and nearly identical multiple consecutive I-V curves are observed. The I-V characteristics of one GaN SAGFEA during the conditioning procedure are summarized in Appendix E. There are different conditioning procedures such as baking in the UHV chamber and UV light exposure [141]. The conditioning procedure is mostly applied to remove the water vapor and other possible gas adsorbates on the emitter surfaces since these adsorbates can affect the surface work function and make device unstable. The conditioned device is then measured for its transfer characteristics.

The transfer characteristics and the corresponding F-N plot of the best GaN SAGFEA are plotted in Fig. 4-23(b) and (c)). This GaN SAGFEA consists of 150 $\times$ 150 sharp emitter tips. The high noise levels of emitter and anode current ($\sim$ 1 nA at the range from V_{GE} = 0V to $V_{GE} = \sim$ 20 V) is resulted from the measurement setup and the source-measurement units (SMUs) used in the measurement. The noise levels are around 10 pA when the maximum current during measurement is below 100 μA, and the noise levels increase when the measured maximum current becomes higher than 100 μA. However, to make a fair comparison with other GaN SAGFEAs, the F-N parameters, such as slope (-b_{FN}) and intercept ($\ln(a_{FN})$) of the

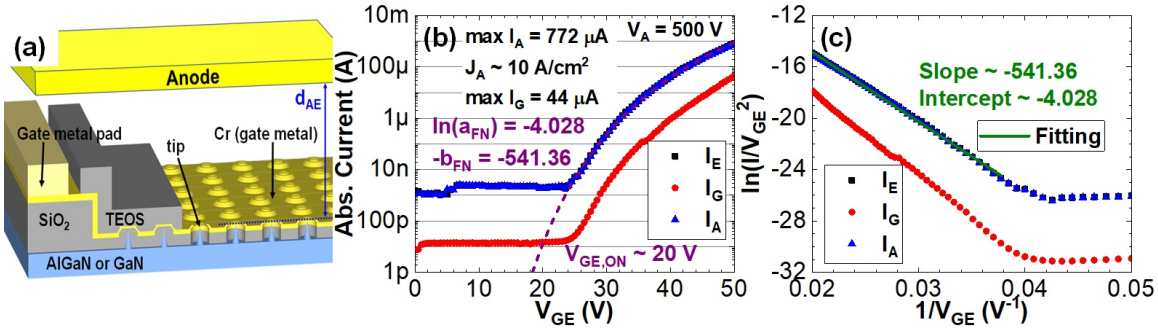


Figure 4-23: (a) 3D illustration of a FEA with a suspended anode, (b) transfer characteristics, and (c) corresponding Fowler-Nordheim (F-N) plot of a GaN FEA with 150 × 150 sharp tips. The anode-emitter distance (d_{AE}) is fixed at about 2 mm in all measurements in this section. The FEA area is about 81 × 96 μm^2. This FEA has max J_A of 10 A/cm^2 at V_{GE} = 50 V. To have a fair comparison with other devices, the turn-on voltage ($V_{GE,ON}$) of 20 V is extrapolated at I_A = 10 pA based on intercept ($ln(a_{FN})$) and slope ($-b_{FN}$) in (c).

F-N plot (Fig. 4-23(c)), are used to draw the fitting curve of anode current (purple dashed line) in transfer characteristics plot (Fig. 4-23(b)). The extrapolated turn-on voltage ($V_{GE,ON}$) at I_A = 10 pA is about 20 V, and the I_A at V_{OV} = 30 V is 772 μA, which is equal to about current density (J_A) of 10 A/cm^2. The V_{OV} is defined as V_{GE} - $V_{GE,ON}$. Furthermore, the gate leakage (I_G) is always at least one order of magnitude lower than the anode current. This device provides highest current density among III-Nitride SAGFEAs and its performance is also better than state-of-the-art Si SAGFEAs at the same bias condition [48, 49]. The current density of this GaN SAGFEA is higher than the ones of Si devices at V_{OV} = 30 V, and the high gate leakage observed in the Si device, which is at the same order as its anode current, is not observed here [48].

The I-V curves of another conditioned device are plotted in Fig. 4-24. This device also consists of 150 × 150 sharp emitter tips and has the same device structure design as the one shown in Fig. 4-23. The fitted F-N parameters (b_{FN} and $ln(a_{FN})$) are very similar in two devices, indicating that the device variation is small. Based on the transfer characteristics and the fitted anode current (purple dashed curve) of this device, the $V_{GE,ON}$ is approximately 20.5 V, and the I_A at V_{OV} = 29.5 V is 545 μA, which is equal to about 7 A/cm^2 for anode current density (J_A). This device

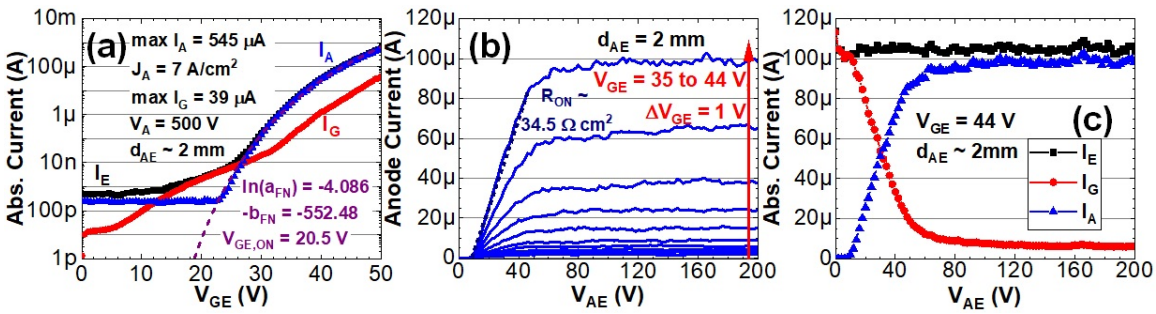


Figure 4-24: (a) Transfer characteristics and (b) (c) output characteristics of another GaN FEA with 150 × 150 sharp tips (with sub-10 nm tip radius). Saturation in the output characteristics is clearly observed. I_A of 100 μA is equal to J_A of about 1.3 A/cm^2. R_{ON} is about 34.5 Ω cm^2 for V_{GE} = 44 V at d_{AE} = 2 mm. Good saturation and constant emitter current are observed, while the long d_{AE} becomes the main issue causing high R_{ON}.

has a slightly higher gate leakage (I_G) in the range from V_{GE} = 10 V to V_{GE} = 30 V, while the I_G is still about one order of magnitude lower than I_A at ON state. The output characteristics of this GaN SAGFEA are also measured (Fig. 4-24(b)). The V_{GE} is varied from 35 V to 44 V, and the V_{AE} is swept from 0 to 200 V, with the sweep step of 2 V. Clear saturation regions are observed at V_{AE} > 60 V, while the on resistance (R_{ON}) is very high ($\sim$ 34.5 $\Omega \cdot cm^2$) due to the very long vacuum channel length ($d_{AE} \approx$ 2 mm). The I-V curves (I_E, I_G, and I_A) at V_{GE} = 44 V are plotted in Fig. 4-24(c). The emitter current (I_E) is almost constant when the V_{GE} bias is fixed, and the gate leakage (I_G) at ON state in transfer characteristics (Fig. 4-24(a)) is one order of magnitude lower than anode current (I_A); therefore, the emission current is mainly controlled by V_{GE}. The I_A remains at noise level from V_{AE} = 0 V to V_{AE} = 6 V, and starts increasing from noise level since V_{AE} > 6 V. These offset of a few volts for the turn-on of I_A is resulted from the work function of anode, since the electrons transport in the vacuum will see the energy barrier near the anode terminal if V_{AE} < the work function of anode [142]. As the V_{AE} increases, the amount of electron flow in the vacuum transports to the anode is now determined by the space-charge limit, as mentioned in section 1.2.2. Once the V_{AE} is high enough, for example, when V_{AE} > 60 V in this measurement, total emitted electron current from emitter (I_E) is less than the space-charge limit, and the anode current is now

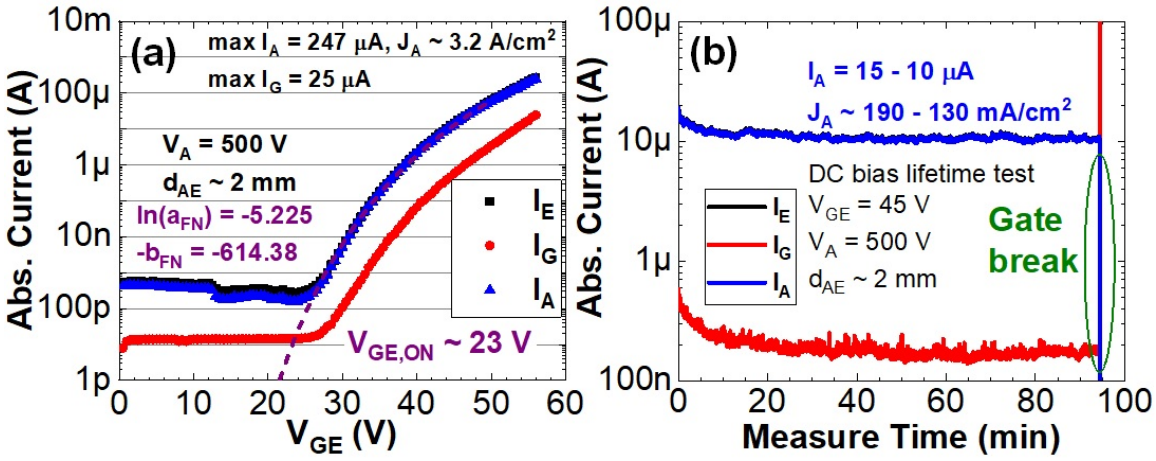


Figure 4-25: (a) Transfer characteristics and (b) DC lifetime test of another GaN FEA with 150 × 150 sharp tips (with sub-10 nm tip radius). The device is very stable during the DC lifetime test until the sudden breakdown. A over-100-hr stable operation of our fabricated GaN SAGFEAs with wire bondings are also observed by our collaborator, Prof. Bruce Gnade group at SMU.

determined by I_E. Therefore, the output characteristics of the vacuum transistors based on SAGFEAs consist of two different regions: space-charge-limit region at low V_{AE} bias and emission-dominant region at high V_{AE} bias. The electric field from the V_{AE} can potentially increase the electric field at the tip surface and thus increase the emission current, but the very long channel length (d_{AE}) and the screening from the gate metal, which is resulted from the fact that the gate metal is higher than tip (Fig. 4-11(a) and Fig. 4-22(c)), make I_A almost a constant at high V_{AE} bias in our device. It should be noted that the space-charge-limit current equations in section 1.2.2 (equations (1.12) and (1.13)) do not fit the experimental data very well. Those equations are based on the one-dimensional electron transport between two parallel metal plates, while our device is an array of emitter sites (tips) toward a large anode metal ball, which is larger than the FEA size of our device. The electron transport in the vacuum is thus a 3-dimensional problem and will require more detailed study and modeling in the future.

Another GaN SAGFEA with 150 × 150 tips is also measured for its transfer characteristics after conditioning (Fig. 4-25(a)). This device is designed to have tips which are about 5 nm wider than the ones shown in Figs. 4-23 and 4-24. Therefore,

the field factor of this device is expected to be slightly smaller, leading to a slightly higher b_{FN} value. Based on the fitted curve (purple dashed curve) plotted using extracted F-N parameters ($\ln(a_{FN})$ and $-b_{FN}$), the turn-on voltage ($V_{GE,ON}$) is $\sim$ 23 V, and the max I_A of 247 μA at V_{OV} = 33 V, which is equal to about 3.2 A/cm^2 in current density (J_A). The DC bias lifetime test is then conducted by fixing V_{GE} = 45 V and V_A = 500 V (Fig. 4-25(b)). Both anode current and gate leakage are very stable during the lifetime test until the sudden breakdown happens after about 95 mins. The gate leakage is always 1-2 orders of magnitude lower than the anode current before the sudden breakdown, which is better than the prior devices (Fig. 3-9(a)). The DC lifetime test shows a fairly stable operation of our latest GaN SAGFEA, while the breakdown observed at $\sim$ 95 min requires more study in the future. There are some possible reasons causing this breakdown, such as the oxide breakdown due to PBTI on the unexposed blunt sacrificial tips or the arcing randomly happens on the device. Though the peak electric fields in dielectric layers on blunt tips are already lower than the ones on sharp tips (Fig. 4-20), they can still be as high as $\sim$ 6 and 7.7 MV/cm in 10-nm ALD Al_2O_3 and 200-nm PECVD SiO_2 at V_{GE} = 45 V. Therefore, the PBTI can still be a potential issue for long-term stability of these GaN SAGFEAs. On the other hand, since the device is connected by probes without wire bonding, the vibration from the environment can potentially cause noise and even glitch during the measurement. If the probe suddenly loses its contact on the sample, the instant transition in current conduction might cause device failure. In fact, some of our GaN SAGFEAs are wire-bonded and are characterized for over 100-hr stable DC operation without breakdown, reported from our collaborators, Prof. Bruce Gnade group at Southern Methodist University (SMU). Therefore, the ways to further reduce peak electric fields in dielectric layers and to package the devices by wire bonding would be necessary in the future to further improve and characterize the long-term stability of our GaN SAGFEAs.

4.5 Summary and further improvement

4.5.1 Summary of Ga-polar GaN SAGFEAs

When considering the b_{FN} = 541.36 V (Fig. 4-23) and the tip-radius-dependent gate-emitter factor (β_{GE}) (Fig. 4-5(b)), we can estimate the tip radius based on the I-V characteristics and TCAD simulation with the SEM observation. Based on equation (1.10), assuming the work function (ϕ) is 3.8 eV, the β_{GE} extracted from experimental data (Fig. 4-23) is about 8.88 $\times$ 10^5 cm^{-1}. By applying the equation shown in Fig. 4-5(b), the estimated tip radius based on TCAD simulation is about 8.3 nm, corresponding to the tip width of 16.6 nm, which is very close to the observation in the SEM (Figs. 4-21 and 4-22). Furthermore, the fitted b_{FN} of 614.38 V in Fig. 4-25 corresponds to the estimated tip radius of 11 nm, which is 22 nm in tip width. The tip-width difference extracted from measurement data (16.6 nm for Fig. 4-23 and 22 nm for Fig. 4-25) well matches our initial designed tip-width difference defined by device fabrication (Fig. 4-26(a)). These results might as well indirectly indicate that the assumed work function (ϕ) of 3.8 eV is a reasonable value for our GaN SAGFEAs. Though the more precise tip size variation in the array should be investigated by TEM or high-resolution STEM, the extracted values here seem to suggest that our latest generation of GaN SAGFEAs has much uniform tips than the prior generations. As the technology has become mature, the expected performance of GaN SAGFEAs with even sharper tips can be estimated assuming the emitting area (α) is kept constant (Fig. 4-26(b)). As expected, when the tip radius is decreased to sub-5 nm range, the device performance can be further improved, which has been shown in Si devices [126].

All Ga-polar GaN SAGFEAs demonstrated in this thesis research are compared with state-of-the-art SAGFEAs in benchmark plots (Figs. 4-27 and 4-28, and Table 4.3) [48–50, 126, 143–152]. During this thesis research, the process flows of GaN SAGFEAs are developed and modified, and the devices are improved over different generations. Our best GaN SAGFEA has $V_{GE,ON}$ of 20 V and J_A of 10 A/cm^2 at V_{OV} = 30 V, which has been the state-of-the-art III-Nitride vertical field emission devices. Furthermore, this GaN SAGFEA has higher current density than the state-of-the-art

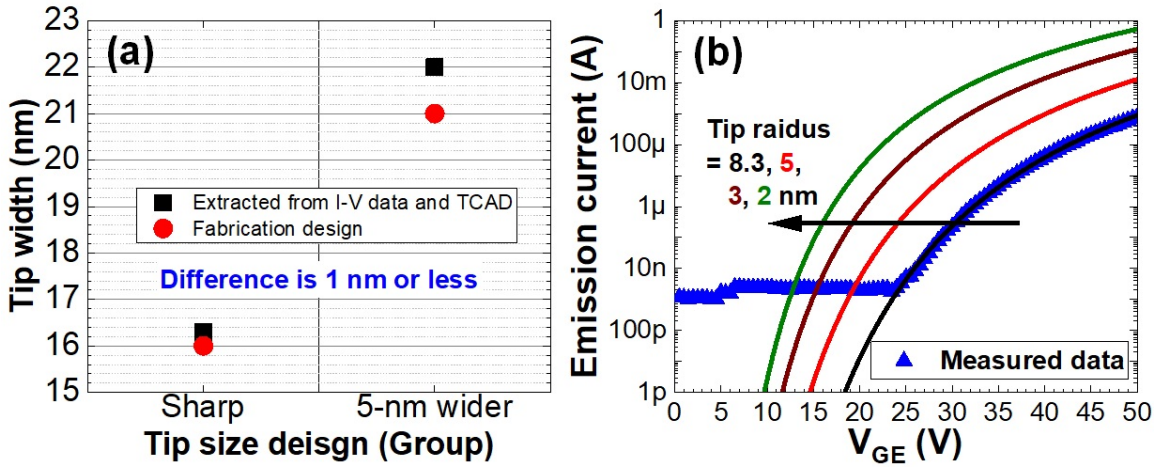


Figure 4-26: (a) The extracted tip width and the designed tip width, and (b) the estimated emission current with different tip-radius GaN SAGFEAs. Sharp tips and 5-nm wider tips are devices shown in Figs. 4-23 and 4-25, respectively. The extracted tip width (based on equation (1.10) and Fig. 4-5(b)) is very close to the fabrication-designed value, indicating the mature technology and uniform tips in the FEA.

Si SAGFEAs at the same bias condition (Figs. 4-27(a) and 4-28(d)). The S-K plot of different devices is shown in Fig. 4-27(b), and the average emitting area per tip can be estimated assuming the work functions of emitter tips (Si: 4.05 eV, GaN: 3.8 eV) (Fig. 4-27(c)). The average emitting area per tip in our last generation of GaN SAGFEAs is improved and comparable with the state-of-the-art Si SAGFEAs. The much uniform electron emission across the array leads to the highest anode current density at the same bias condition (V_{GE} = 50 V). In the past 4 years, the current density (J_A) of GaN SAGFEAs increases from 0.01 A/cm^2 to 10 A/cm^2. which is about 1000× improvement.

The benchmark plot of turn-on voltage ($V_{GE,ON}$) and |FN slope ($-b_{FN}$)| of different technologies is shown in Fig. 4-28(a). Since the transfer characteristics of different work are not all shown in the same way, to make fair comparison, the anode current level for extracting the $V_{GE,ON}$ of different devices is also noted in the plot. The trend of low b_{FN} value with the low $V_{GE,ON}$ voltage is observed. Since the field emission current has a exponential term , $exp(\frac{-b_{FN}}{V_{GE}})$, devices with low b_{FN} values can thus have low turn-on voltage [124]. Our GaN SAGFEAs have comparable turn-on voltages (20 - 30 V) with Si and CNT devices in literature [48,49,126,143–150,152]. It is noted that

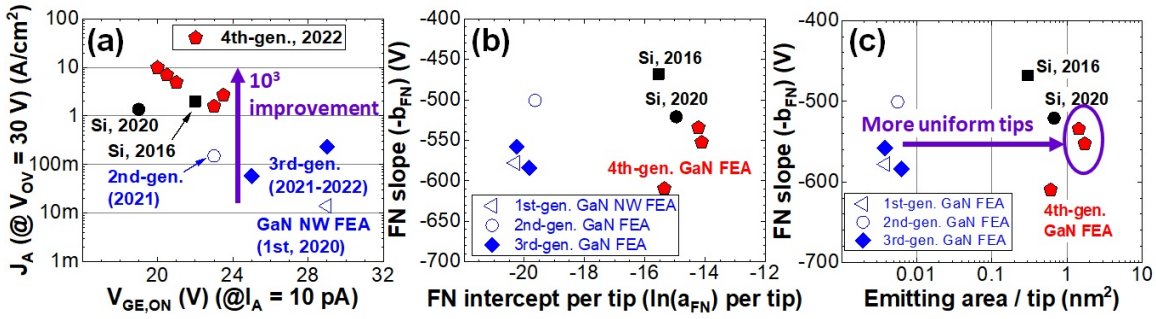


Figure 4-27: (a) The benchmark plot of the $V_{GE,ON}$ versus J_A (@ V_{OV} = 30 V), (b) Seppen-Katamuki (S-K) plot, and (c) emitting area per tip versus F-N slope of different Si and GaN SAGFEAs [48, 49]. After multiple generations of improvement, the state-of-the-art GaN SAGFEAs have outperformed the state-of-the-art Si SAGFEAs in terms of current densities and emitting area per tip.

the maximum anode current of our best GaN device is only about 770 μA, which is one-order-of-magnitude lower than the highest anode current of Si devices ($\sim$ 10 mA) (Fig. 4-28(b)). Nonetheless, when the applied V_{GE} for the maximum anode current per tip (Fig. 4-28(c)) and maximum anode current density (J_A) (Fig. 4-28(d)) is considered, our best GaN device has high anode current per tip (34.5 nA per tip) and the highest anode current density (10 A/cm^2) at V_{GE} = 50 V. One HfC-coated Si SAGFEA and another Si SAGFEA have emission current of about 500 and 100 nA per tip at V_{GE} = 50 V, while their current densities at 50 V are lower than our best device [48, 147]. A more complete list for comparison between different devices is shown in Table 4.3 [48–50, 126, 143–153].

Besides the comparison in Figs. 4-27 and 4-28, different state-of-the-art devices are also compared in S-K plot (Fig. 4-29) [48,49,146]. Theoretically, the upper-left region indicates smaller tip apex, and the upper-right region indicates smaller effective work function [106]. This interpretation matches with Si and HfC-coated Si devices. When considering our GaN SAGFEAs with 8.3-nm tip radius with the drawn brown-dashed line from the Si devices, our GaN devices might have a slightly lower work function than the Si devices. However, when comparing our GaN devices with different tip radius, relative locations of the data points do not match the theoretical trend [106]. More investigation is necessary in the future to understand this discrepancy.

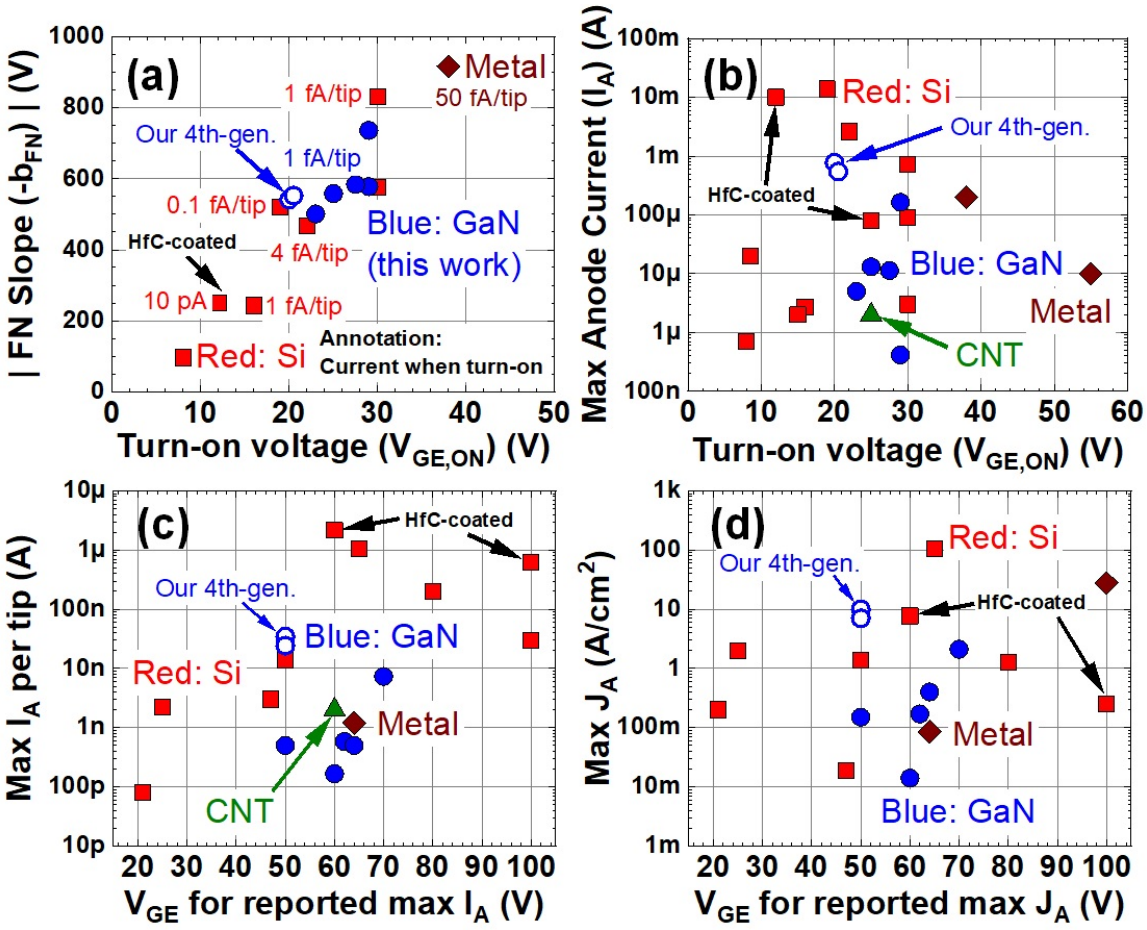


Figure 4-28: The performance benchmark of different materials' SAGFEAs [48–50, 126, 143–153]. To make fair comparison between different technologies, the turn-on voltage ($V_{GE,ON}$) shown in (a) and (b) is defined as a gate-emitter voltage (V_{GE}) when the anode current per tip reaches a certain level. Since the transfer characteristics of different work are not all shown in the same way, the anode current level of turn-on voltage for each data point is noted in (a). As some work does not mention the emitter device area or the number of tips in the array, some work does not have data points in different plots. The more complete comparison is shown in Table 4.3. Our GaN SAGFEAs have the comparable turn-on voltage, relatively high max current per tip at V_{GE} = 50 V, and high current density (J_A) = 10 A/cm^2 at V_{GE} = 50 V.

While the performance of GaN SAGFEAs has been enhanced over the past few years during this thesis research, the device geometry and process flow can still be improved further in the future. For example, the gate aperture size, tip radius, or the aspect-ratio of the GaN emitter tips can be improved further to reduce the operating voltage, which is beneficial to long-term stability on dielectric layers. For example, the smaller gate apertures in Si devices (Table 4.3) provides smaller turn-on voltage,

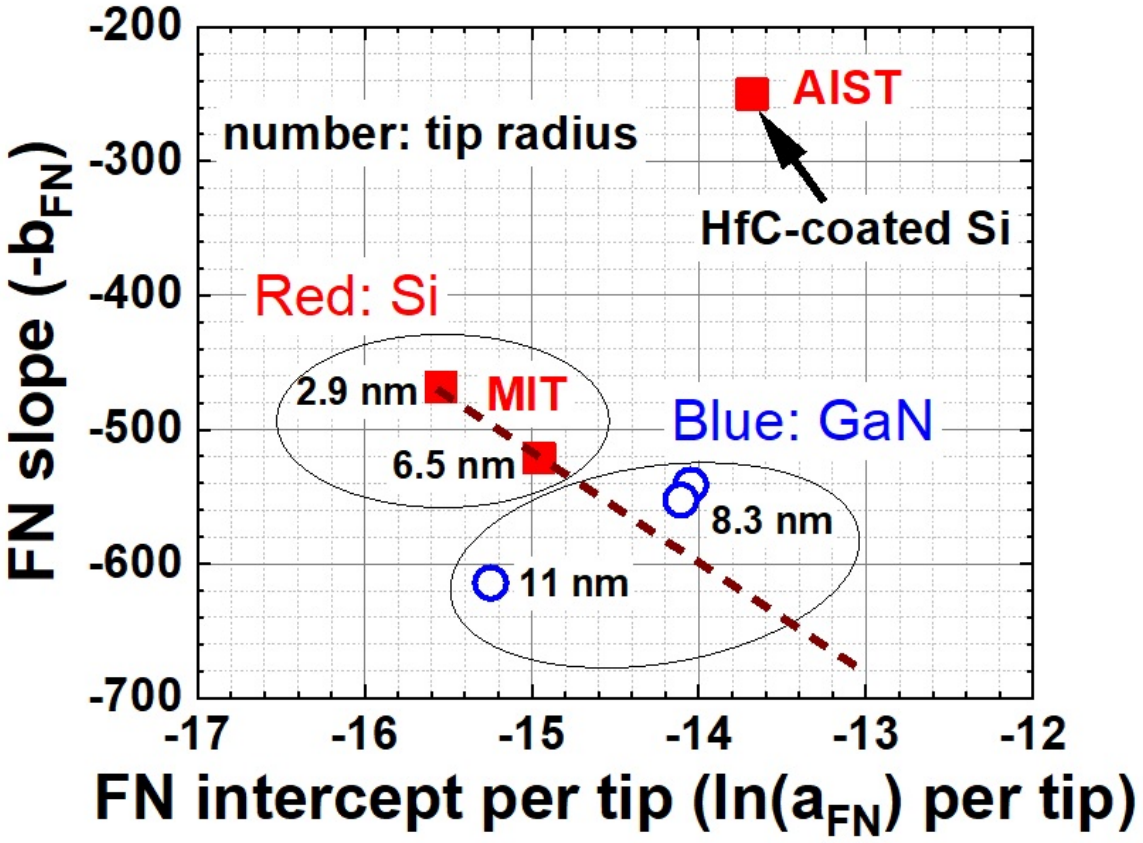


Figure 4-29: The S-K plot of few state-of-the-art devices [48, 49, 146]. GaN devices are our 4th-generation SAGFEAs. The circles in the plot indicate the same or similar fabrication technologies. The brown-dashed line is drawn to help compare devices. Theoretically, the upper-left region indicates smaller tip apex, and the upper-right region indicates smaller effective work function [106]. However, our devices with different tip width show different trend and requires further investigation in the future.

and the emission current is expected to be enhanced with sharper tips (Fig. 4-26(b)). The average maximum emission current per tip in our best GaN SAGFEA is still only $\sim$ 35 nA, while the maximum emission current per tip in state-of-the-art Si SAGFEA can be $\sim$ 1 μA [48, 146, 147] at a higher V_{GE}. Since the thermal conductivity and bonding energy of GaN are comparable with or better than Si, GaN emitter tips should be capable of conducting the similar amount of current. By improving the gate oxide quality and by modifying the device geometry, the long-tetm stability of dielectric layers can help achieve higher bias voltage conditions. Some potential future modifications will be discussed in the following section.

Table 4.3: The complete list of different SAGFEAs compared in Figs. 4-27 and 4-28 [48–50, 126, 143–152].

FEA	Researchers from	Gate aperture (nm)	Turn on Voltage (V)	FN slope ($-b_{FN}$) (V)	Max Current (at V_{GE})	Max J_A (A/cm^2)	Max I_A per tip
Si	AIST, Japan	600	8?	-96.1	**700 nA** (30 V)	?	?
Si	AIST, Japan	1600	30?	-575.6	**90 μA** (70 V)	?	?
a-Si	AIST, Japan	1800	30?	?	**3 μA** (100 V) (100 tips)	?	30 nA
Si	Seoul National University, Korea	550	?	?	**670 μA** (58 V) (2500 tips)	?	260 nA
HfC-Si	AIST, Japan	?	12 (10 pA)	-250	**10 mA** (100 V) (16,000 tips)	0.25	625 nA
HfC-Si	AIST, Japan	600	25 (3 pA/tip)	?	**80 μA** (60 V) (37 tips)	7.7	2.16 μA
Si	MIT, USA	1000	30 (1 fA/tip)	-830.28	**720 μA** (80 V) (60 * 60 tips)	1.25	200 nA
Si	MIT, USA	1000	16 (1 fA/tip)	-243	**2.7 μA** (47 V) (900 tips)	0.0188	3 nA
Si	MIT, USA	160	15 (10 pA)	?	**2 μA** (25 V) (900 tips)	2	2.2 nA
Si	MIT, USA	70	8.5 (40 aA/tip)	?	**20 μA** (21 V) (500*500 tips)	0.2	80 pA
Si	MIT, USA	360	22 (40 fA / tip)	-468	**2.6 mA** (65 V) (50 * 50 tips)	104	1.04 μA
Si	MIT, USA	360	19 (100 aA / tip)	-521	**13.8 mA** (50 V) (1000 * 1000 tips)	1.37	13.7 nA
Metal	Paul Scherrer Institute, Switzerland	1500	55 (100 pA)	?	**10 μA** (100 V)	27.78	?
Mo	Paul Scherrer Institute, Switzerland	350	38 (50 fA/tip)	-917	**200 μA** (64 V) (165,000 tips)	0.085	1.2 nA
CNT	MIT, USA	1300	25 (10 fA / tip)	?	**2 μA** (60 V) (32 * 32 tips)	?	2 nA
GaN	Our 1st gen.	350	29 (4 fA / tip)	-577.96	**415 nA** (60 V) (50 * 50 tips)	0.014	166 pA
GaN	Our 2nd gen.	280	23 (1 fA / tip)	-501	**5 μA** (50 V) (100 * 100 tips)	0.15	500 pA
GaN	Our 3rd gen.	400	25 (1 fA / tip)	-558.11	**13.1 μA** (62 V) (150 * 150 tips)	0.17	582 pA
GaN	Our 3rd gen.	400	29 (1 fA / tip)	-736.06	**164 μA** (70 V) (150 * 150 tips)	2.11	7.3 nA
GaN	Our 3rd gen.	400	27.5 (1 fA / tip)	-583.91	**11.3 μA** (64 V) (150 * 150 tips)	0.4	500 pA
GaN	Our 4th gen.	300	20 (1 fA / tip)	-541.36	**772 μA** (50 V) (150 * 150 tips)	10	34.5 nA
GaN	Our 4th gen.	300	20.5 (1 fA / tip)	-552.48	**545 μA** (50 V) (150 * 150 tips)	7	24.2 nA

4.5.2 Further improvement: uniform GaN NW emitters

The first-generation GaN SAGFEAs are based on GaN vertical NWs fabricated by two-step etching process combining Cl_2/BCl_3-based ICP-RIE and heated TMAH wet etching (Fig. 3-2), but the uniformilty and fabrication yield of sub-30-nm GaN NWs are issues to keep improving the field-emission-based vacuum transistors (section

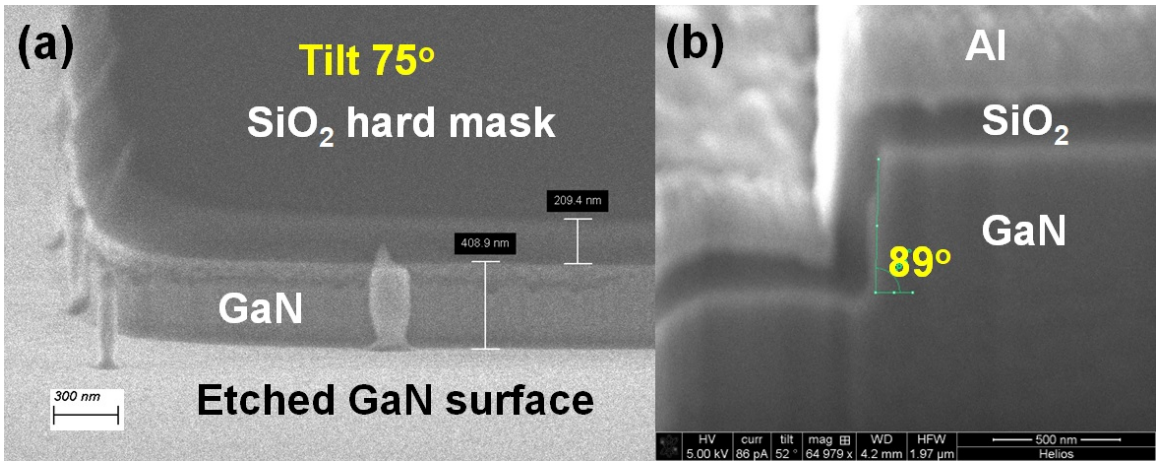


Figure 4-30: (a) The tilted and (b) cross-sectional SEM images of the GaN mesa formed by the Cl_2/Ar-based ICP-RIE with SiO_2 hard mask. The (b) cross-sectional SEM image is obtained from the focus ion beam-scanning electron microscope (FIB-SEM) system at MIT MRSEC. Before the FIB, the SiO_2 mask is removed by BOE, and the new SiO_2 layer and Al layer are deposited by PECVD and by sputtering, respectively, to protect GaN sidewalls and to reduce the charging effect from the Ga-ion beam during the FIB cutting process.

4.1.1). While these issues are avoided by changing the tip shape from NW to pyramid, the electric field enhancement on pyramid-shape tips is weaker than the one on NW-shape tips (Fig. 4-1(c) and Fig. 4-5(b)). Therefore, the better top-down approach to form uniform vertical GaN NWs with sub-30-nm width is still important. Based on the reported Cl_2/Ar-based ICP-RIE for GaN vertical sidewalls [154], the new approach of one-step dry etching for GaN vertical NWs are developed and the uniform GaN vertical NW arrays can be fabricated through this approach.

In the first experiment, the similar Ti/Ni hard mask, which we used for pyramid-shape tips formation, is used as hard mask for Cl_2/Ar-based ICP-RIE. However, the Ni hard mask is observed deformed after the dry etching. Though it is not clear the reason of the deformation of Ni mask, the hard mask for GaN dry etching is changed from Ni to PECVD SiO_2 in the following experiments. The $\sim$ 220-nm-thick SiO_2 is deposited by PECVD and is then defined by CF_4/Ar-based ICP-RIE (recipe name: SiO_2 default) using photoresist mask. The resist is then removed and the SiO_2 layer is used as the mask for the initial test of Cl_2/Ar-based ICP-RIE dry etching on GaN. After varying the pressure and ICP and Bias power for a few test, the recipe for

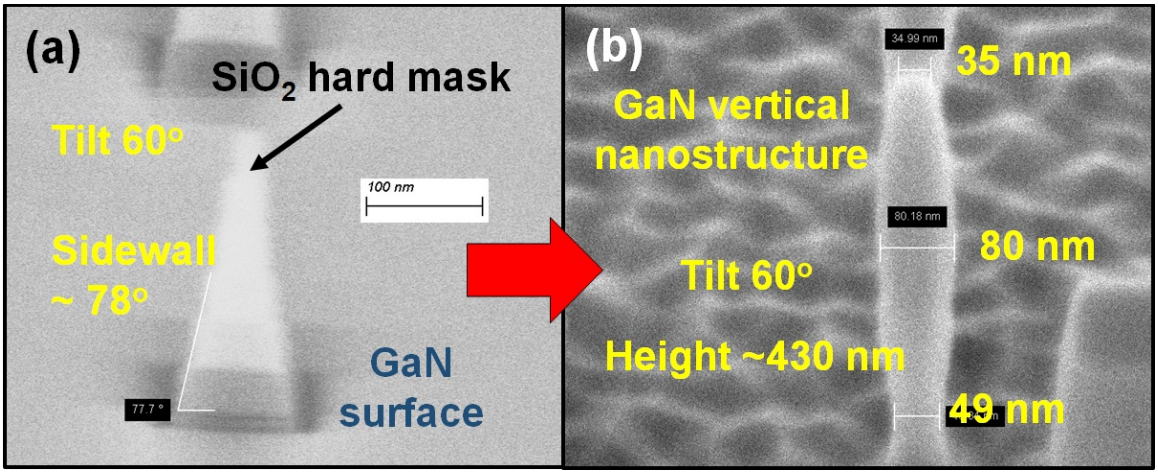


Figure 4-31: The tilted SEM images of (a) SiO_2 hard mask defined by default SiO_2 etching recipe in our ICP-RIE tool and (b) GaN vertical nanostructure formed by Cl_2/Ar-based ICP-RIE. The Ti/Ni metal stack is defined by lift-off process using PMMA and e-beam lithography and is used as the hard mask for SiO_2 dry etching. The Ti/Ni mask is then removed and the SiO_2 is used as the hard mask for GaN dry etching. The sidewall shape of SiO_2 mask affects the sidewall profile of GaN nanostructures formed by dry etching.

etching GaN with vertical sidewalls is identified, and the tilted and cross-sectional SEM images of this etching results are shown in Fig. 4-30. The estimated GaN sidewall slope is $\sim 89^o$ based on the cross-sectional SEM image (Fig. 4-30(b)).

After the recipe for GaN dry etching with vertical sidewalls is confirmed in our ICP-RIE system, the NW-formation experiments are then conducted. The Ti/Ni mask defined by e-beam lithography with PMMA lift-off is used for SiO_2 dry etching. The Ti/Ni mask is then removed by Ni etchant TFB and piranha clean. The default CF_4/Ar-based ICP-RIE gives SiO_2 sidewalls with a slope of $\sim$ 78 degree (Fig. 4-31(a)). The GaN layer is then dry etched by Cl_2/Ar-based dry etching (recipe name: GaN vertical), and the SiO_2 mask is then removed by BOE. The spindle-like GaN vertical nanostructure is formed (Fig. 4-31(b)). The overall sidewall slope of these GaN vertical structures is close to 90 degree, but the spindle shape is not desired, and it is likely resulted from the non-vertical sidewalls of SiO_2 mask (Fig. 4-31(a)).

As the hard mask for the dry etching can play an important role in the etching profile, such as sidewall slopes and shapes, the additional experiments have been conducted to obtained the etched SiO_2 layer with vertical sidewalls (Fig. 4-32(a)). Un-

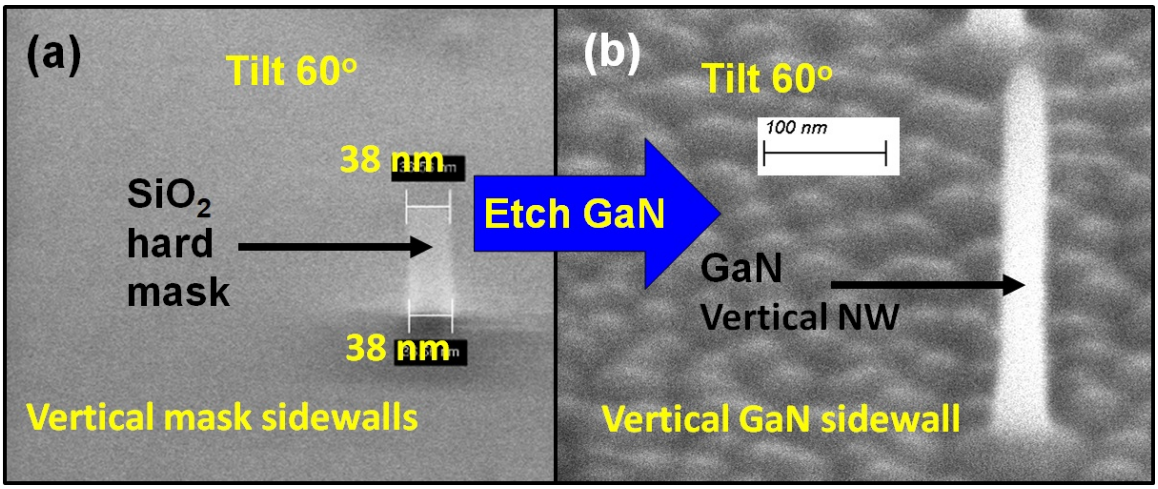


Figure 4-32: The tilted SEM images of (a) SiO_2 hard mask with vertical sidewalls defined by optimized CF_4/H_2-based ICP-RIE process and (b) a GaN vertical NW formed by the same Cl_2/Ar-bassed ICP-RIE with the vertical-sidewall SiO_2 hard mask. Both SEM images are taken after the hard masks are removed.

like the SiO_2 default recipe, the CF_4/H_2-based etching recipe is used in the ICP-RIE (recipe name: SiO_2 optimized). The e-beam lithography patterns can be successfully transferred from Ti/Ni mask to SiO_2 mask with vertical sidewalls (Fig. 4-32(a)). With this SiO_2 mask, the GaN vertical NW with vertical sidewalls are fabricated by Cl_2/Ar-based ICP-RIE (recipe: GaN vertical) (Fig. 4-32(b)). It is noted that the etched GaN surfaces in these experiments (Fig. 4-31(b) and Fig. 4-32(b)) are much rougher than the one in the prior experiment (Fig. 4-30(a)), and this requires further investigation in the future.

A uniform GaN vertical NW array can be fabricated through the fabrication demonstrated here (as shown in Fig. 4-32). After the GaN dry etching and the removal of SiO_2 mask, the GaN NWs can be shrunk by the wet-based DE (Table 4.1). After multiple cylces of DE, uniform GaN NW arrays with sub-30-nm NW width are formed with high yield (Fig. 4-33). The GaN vertical NW with $\sim$ 24-nm width and a $\sim$ 12:1 height-to-width aspect ratio can be reproducibly fabricated (Fig. 4-33(b)). It is possible to apply more cycles of DE to further shrink the GaN NW diameter to below 20 nm, but the surface tension of water (or solvent) can make NW break during sample drying [138]. All different ICP-RIE recipes used and developed in these exper-

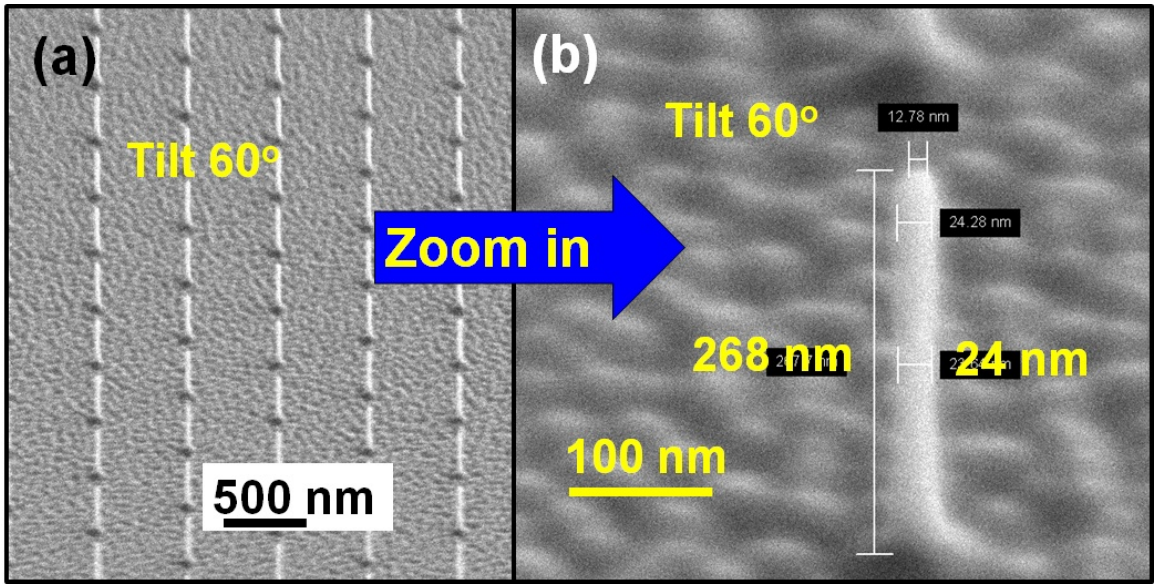


Figure 4-33: (a) The tilted and (b) high-magnification SEM images of GaN vertical NW array with sub-30 nm NW width and a $\sim$ 1:12 width-height aspect ratio after multiple cycles of wet-based DE on NWs formed in Fig. 4-32(b).

iments are summarized in Table 4.4. All dry etching steps presented in this section are conducted in a SAMCO 230iP system (local tool name: RIE-Mixed-SAMCO-230iP) on the quartz carrier for pieces.

With these developed technologies, the uniformity and yield issues of GaN NW fabrication encountered in the first-generation GaN SAGFEAs (section 4.1.1) are solved. The high-aspect-ratio GaN NW emitter tips can then be a great candidate to further improve the local electric field enhancement on the tips for the higher emission current and to further reduce the operating voltage (V_{GE}) in the future GaN NW SAGFEAs.

4.5.3 Further improvement: Reduction of peak electric fields in dielectric layers

Besides the emitter-shape formation and optimization to reduce the operating voltage (V_{GE}) and increase emission current, the device stability also requires work to optimize the overall device geometry and the corresponding process flow. After the failure of device during the measurement, for example, the breakdown observed in

Table 4.4: Summary of dry etching process for GaN vertical NW formation. The etching rates of (1) SiO_2 default, (2) SiO_2 optimized, (3) GaN default, and (4) GaN vertical are (1) $\sim$ 130 nm/min, (2) $\sim$ 110 nm/min, (3) $\sim$ 3.6 nm/sec, and (4) $\sim$ 240 nm for 10 sec BT + 1 min Etch. All etching recipes here are conducted in RIE-Mixed-SAMCO-230iP with quartz carrier and chamber temperature of 20^{o}C. The etching recipe of (2) SiO_2 optimized can potentially have undercuts due to the heating up of sample surface during etching. Instead of the quartz carrier, the Si wafer carrier with heat-transfer oil, such as Santovac, should be used for deep SiO_2 etching to reduce undercuts.

Etch recipe	Hard mask	Gas (sccm)	Pressure	ICP/Bias Power (W)	Sidewall slope
SiO_2 default	Ni	30 CF_4 + 60 Ar	1 Pa	400/100	~ 78^o
SiO_2 optimized		50 CF_4 + 10 H_2	0.45 Pa	600/50	~ 90^o
GaN default	Ni or SiO_2	15 Cl_2 + 5 BCl_3	0.6 Pa	150/75	~ 78^o
GaN vertical	SiO_2	• BT: 20 BCl_3 + 5 Ar	0.5 Pa	500/50	~ 90^o
		• Etch: 20 Cl_2 + 20 Ar	4 Pa	600/75	

Fig. 4-25(b), the device is then investigated by SEM again to identify the potential breakdown points of the current device geometry (Fig. 4-34(a)). Other broken devices are also checked by SEM, and most of their failures are observed at the corner or the edge of the FEA, that is, the sacrificial unexposed blunt-tip regions. As discussed in the discussion of Fig. 4-25, the peak electric fields in dielectric layers on the unexposed wide tips can still be as high as $\sim$ 6 and 7.7 MV/cm in 10-nm ALD Al_2O_3 and 200-nm PECVD SiO_2, respectively. The physical damages observed in these unexposed-tip regions (Fig. 4-34(a)) further confirm that these regions are still weak points for the long-term stability of our GaN SAGFEAs.

There are few possible approaches to further reduce the peak electric fields in these dielectric layers or to fully eliminate this issue: (1) Using the wider mesa with $\sim$ 500-nm or 1-μm width for these sacrificial regions, (2) Redesigning process flow and using e-beam lithography for better lithography alignment, and (3) Using CMP planarization instead of TEOS planarization.

First of all, the peak electric fields in dielectric layers can be further reduced by

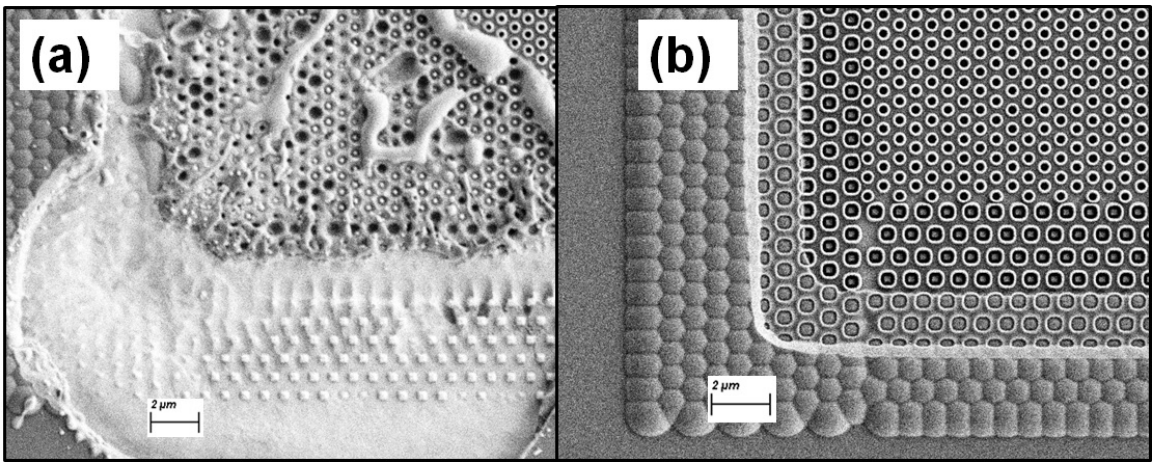


Figure 4-34: The SEM images of (a) the failure region of a failed GaN SAGFEA and (b) the same region of another pristine GaN SAGFEA. The failed GaN SAGFEA is the one reported in Fig. 4-25. Most failed devices have failure spots at the edges or corners of FEAs, which might indicate that peak electric field requires better management or structure design.

using wider tips in these unexposed regions, which is the easiest and trivial approach to improve the device stability. However, these regions are the area cost and do not really provide any advantage on device performance. Therefore, this approach can be an intermediate step during the device and process development, while the strong peak electric fields still exist in dielectric layers, leading to the concerns of PBTI issue.

Secondly, the e-beam lithography can be used for the definition of etching mask for TEOS planarization. The photolithography in the university-level cleanroom setting can get lithography misalignment in few hundred nm or 1 μm, but the device structure, for example the GaN pyramid, has around 100-200 nm width. Additionally, to achieve the best results of the lithography, the process parameters, such as resist, dose, and development need to be optimized if the sample is not a simple Si substrate. Therefore, using a single photolithography step to get the perfect alignment with patterns with right sizes can be challenging. On the other hand, the e-beam lithography can get alignment error below 100 nm and the errors of pattern sizes can be easily below 100 nm. Therefore, use the e-beam lithography for alignment and mask definition of the TEOS planarization step can potentially remove the sacrificial regions and thus the device instability due to the peak electric fields in dielectric layers can

be eliminated. However, the PMMA e-beam resist is not a good dry etching mask, so the metal mask lift-off on PMMA patterns or the use of different e-beam resist might be necessary. The preliminary experiments of using e-beam lithography alignment for Ni hard mask for following SiO_2 dry etching will be reported and discussed in Chapter 6, but more experiments and optimizations are still necessary to make this approach feasible and reproducible.

Thirdly, the planarization step can be changed from the dry etching of TEOS layer to the conventional CMP process. The process developed in this thesis research is mainly applied to the small pieces cut from the 6-inch GaN-on-Si wafer, and the CMP process on pieces can be difficult. If the process flow is transferred from small pieces to 6-inch or 8-inch wafers in the future, the CMP can be the good option to do the vertical structure planarization, like the process demonstrated in Si SAGFEAs [48,49]. There will be additional optimizations necessary for typical GaN-on-Si wafers due to their large wafer bows from the stress and thermal expansion mismatch, but the CMP process can potentially be a more uniform and high-yield planarization step. The unexposed-tip regions used in TEOS planarization can also be removed and the instability issues due to the peak electric fields in dielectric layers can be eliminated (Fig. 4-35).

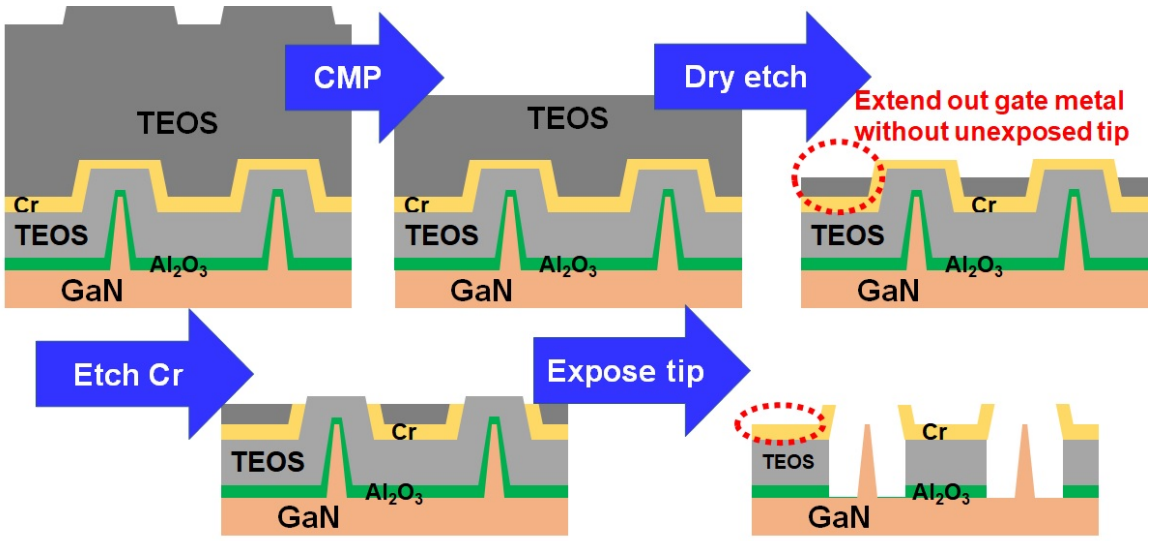


Figure 4-35: The proposed process flow of GaN SAGFEAs with a CMP planarization process. After the gate stack deposition, the thick TEOS layer is deposited by PECVD, and the CMP process is applied to planarize the TEOS surface. After that, the timed dry etching on TEOS is conducted until the top gate metal (Cr) is exposed. The gate metal is then etched with TEOS mask, and the tips are finally exposed. The red dashed circles indicate the region which can extend out the gate metal without the need of overlapping and unexposed tip regions.

Chapter 5

Other III-Nitrides field emitter arrays

The materials in this chapter are partially based on the following journal papers:
(1) Pao-Chuan Shih et al., "Wet-based digital etching on GaN and AlGaN," APL, DOI: 10.1063/5.0074443 *[121].*
(2) Pao-Chuan Shih et al., "Stable and High Performance AlGaN Self-Aligned-Gate Field Emitter Arrays," IEEE EDL, DOI: 10.1109/LED.2022.3184996 *[155].*
The published materials in publication mentioned above are reused with permission, AIP Publishing [123], and © 2022 IEEE, respectively [111].

5.1 Motivation of using other III-Nitrides

The Ga-polar GaN SAGFEAs are developed and improved in chapter 3 and chapter 4. Though the performance of our latest Ga-polar GaN SAGFEAs has been improved and becomes comparable with the state-of-the-art Si SAGFEAs (Figs. 4-27 and 4-28 and Table 4.3), the performance of III-Nitride field-emitter-based vacuum transistors can be improved further by using different III-Nitride materials to reduce the electron emission energy barrier, as discussed in section 1.3.1. Ideally, the work function of n^{++}-semiconductor is close to its electron affinity (Fig. 5-1(a)), and the semiconductors with lower electron affinities can thus have lower work functions. Based on the equations (1.8)-(1.10) and the experimental data of the state-of-the-art GaN SAGFEA (Fig. 4-23), the emitting area (α) and gate-emitter field factor (β_{GE}) can

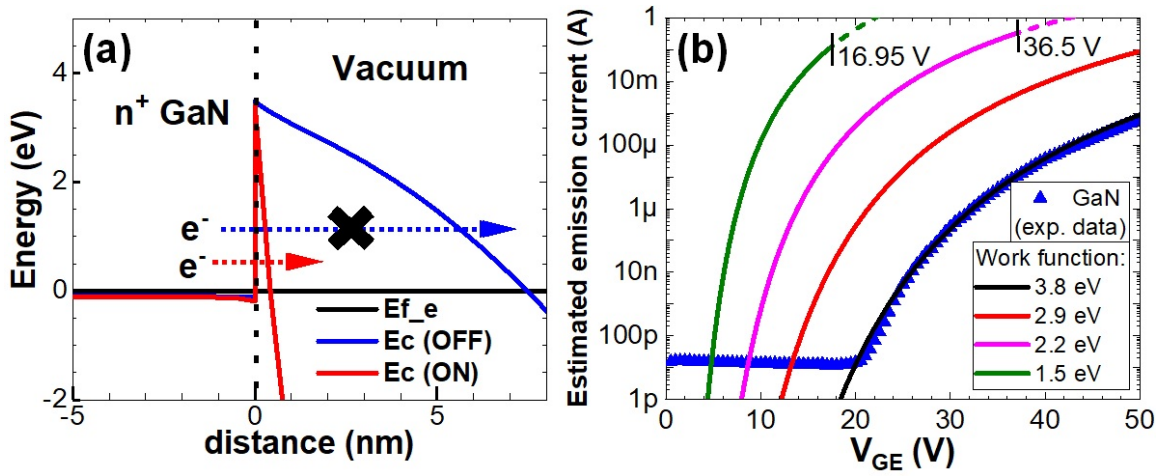


Figure 5-1: (a) Energy band diagram of OFF and ON states of a field emitter, and (b) estimated emission current of the field emitter arrays with different work functions. The experimental data of GaN SAGFEA is the same as the one in Fig. 4-23. Theoretically, low-work-function emitters can build vacuum transistors with low operating voltage and high current density.

be extracted with the assumption that the work function of Ga-polar n^{++}-GaN is 3.8 eV. If both emitting area and gate-emitter field facor are assumed constants, the field emission current from emitter tips of materials with different work functions can be calculated (Fig. 5-1(b)) [34]. The more sophisticated models and analyses on field emission physics can be found in Reference [156]. Based on the prior work of electron affinities of different AlGaN alloy compositions and different polarization (Fig. 1-6) [57, 58], the work functions can be theoretically reduced to around 2 eV or below for high-Al AlGaN field emitter tips. These high-Al AlGaN SAGFEAs with low work functions are expected to have superior performance to the one of Ga-polar GaN SAGFEAs. For example, the AlGaN SAGFEA with work function of 1.5 eV can have $V_{GE,ON} \sim 5$ V (@ $I_A = 10$ pA) and the estimated emission current can reach ~ 10 mA at $V_{GE} = 12$ V, which is equal to about 125 A/cm^2 of current density. The estimated emission current is calculated based on the approximation of image-force-induced barrier lowering. The approximation is valid only when

$$0 < y < 1 \tag{5.1}$$

$$y = 3.79 \times 10^{-4} \times \frac{E^{0.5}}{\phi} \tag{5.2}$$

where E is the electric field in the unit of V/cm, and ϕ is the work function of material and is in the unit of eV. The electric field E $\approx \beta_{GE}V_{GE}$. Therefore, if the work function is low, y can be larger than 1 if the electric field E is strong enough, and the approximation will then fail [34]. The regions where the approximation fails in the estimated emission current are drawn with dashed lines, and the solid lines are the regions where the approximation still works (Fig. 5-1(b)). Though the assumption of constant emitting area (α) and gate-emitter field factor (β_{GE}) may not be fully correct, for example, the emitting area will also depend on the electric field strength on the emitter surface [156, 157], the estimation provides the general idea of using III-Nitrides with low electron affinities for potentially-low-work-function field emitter tips.

5.2 N-polar GaN self-aligned-gate field emitter arrays

As mentioned above, one way to further improve the device performance is to use the low-electron-affinity n^+ semiconductors for potentially low-work-function emission surface (Fig. 5-1). A work of material characterizations on both Ga-polar and N-polar GaN surfaces reports that the electron affinity of N-polar surface is lower than the one of Ga-polar surface (Fig. 1-6) [58]. Therefore, the N-polar n^+ GaN SAGFEAs are also fabricated, aiming to provide better performance than Ga-polar GaN SAGFEAs.

5.2.1 Device fabrication and observed issues

The N-polar n^+ GaN was grown and provided by the collaborator, Dr. Raju Ramesh at Aalto University by MOCVD. The epitaxial structures, Hall measurement results, and the microscope image of the grown N-polar GaN surface are shown in Fig. 5-2. The epitaxial structure is grown on the c-plane sapphire substrate with 2-degree miscut toward a-plane, which is purchased from Kyocera Coporation. The sheet electron concentration measured by Hall measurement is about 6.35 - 6.4 $\times$ 10^{14}

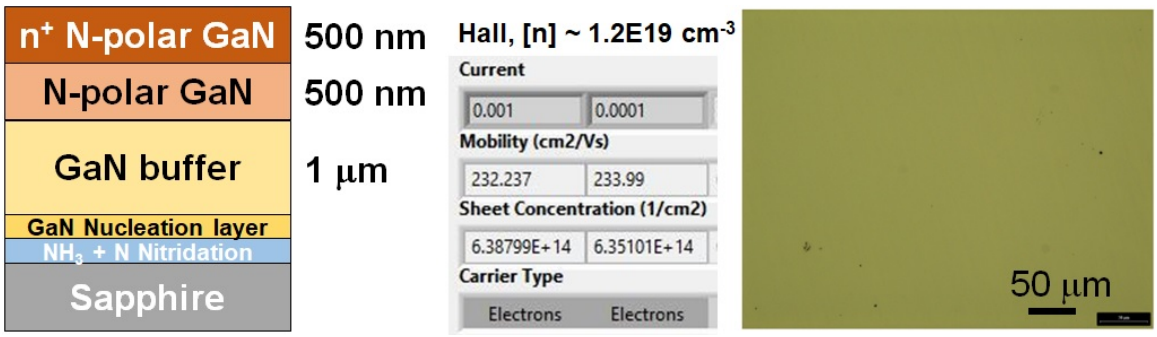


Figure 5-2: The epitaxial structure, hall measurement results, and the surface under microscope of the n^+ N-polar GaN grown on a miscut sapphire substrate. The Hall electron concentration is estimated about 1.2×10^{19} cm^{-3}. There is no significant crack or huge pit defects observed on this heavily-n-doped N-polar GaN sample. The N-polar GaN sample is grown by MOCVD and is provided by Dr. Raju Ramesh at Aalto University, Finland.

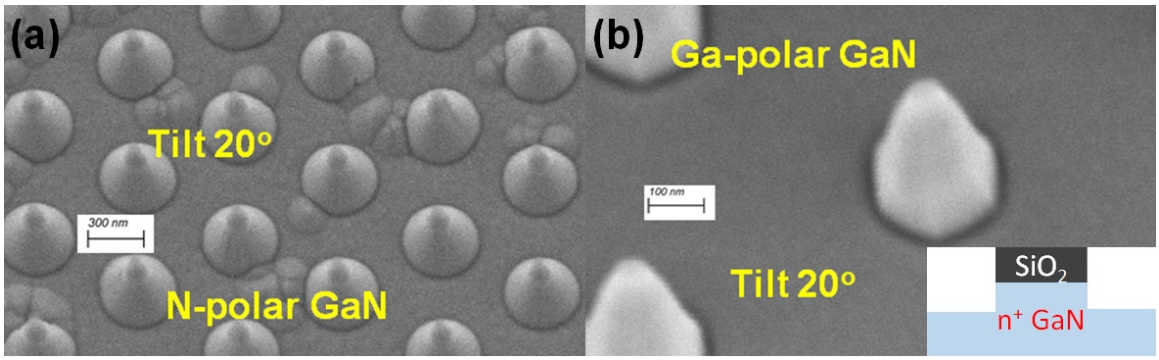


Figure 5-3: (a) N-polar and (b) Ga-polar GaN pyramids after ICP-RIE dry etching with SiO_2 hard mask. Unlike the Ga-polar GaN, the N-polar GaN does not show specific lattice planes after dry etching.

cm^{-2}. Assuming that most electrons exist in the top n^+ GaN layer, the electron concentration (n) in this n^+ N-polar GaN layer is approximately 1.2 - 1.3 $\times$ 10^{19} cm^{-3}. Though the top layer has a high doping concentration, the pristine grown surface is still smooth.

The process flow of N-polar GaN SAGFEAs is similar to the one of Ga-polar GaN SAGFEAs (Fig. 4-16). The device fabrication of N-polar GaN SAGFEAs is conducted simultaneously with the Ga-polar GaN SAGFEAs reported in section 4.4. First of all, the 100-nm SiO_2 is deposited by PECVD and the Ti/Ni mask is defined by e-beam lithography and lift-off process on SiO_2. The SiO_2 is then etched by ICP-

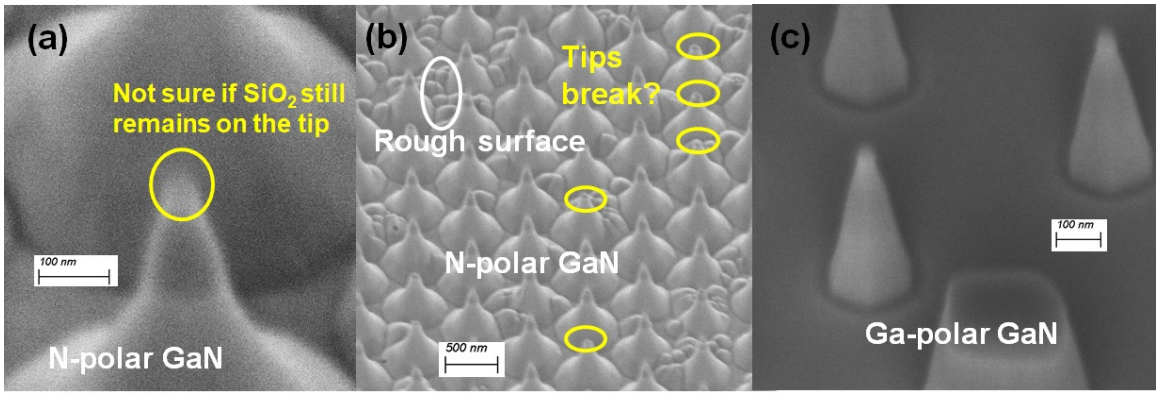


Figure 5-4: The SEM images of N-polar GaN pyramids after 6 cycles of digital etching (DE) (same procedure as listed in Table 4.1) under (a) high magnification and (b) medium magnification. Unlike (c) Ga-polar GaN, the N-polar GaN after DE shows rough surface and break of tips (shown in (b)). Different-color regions are observed in N-polar GaN, which might indicate dopant (Si) segregation on the surface.

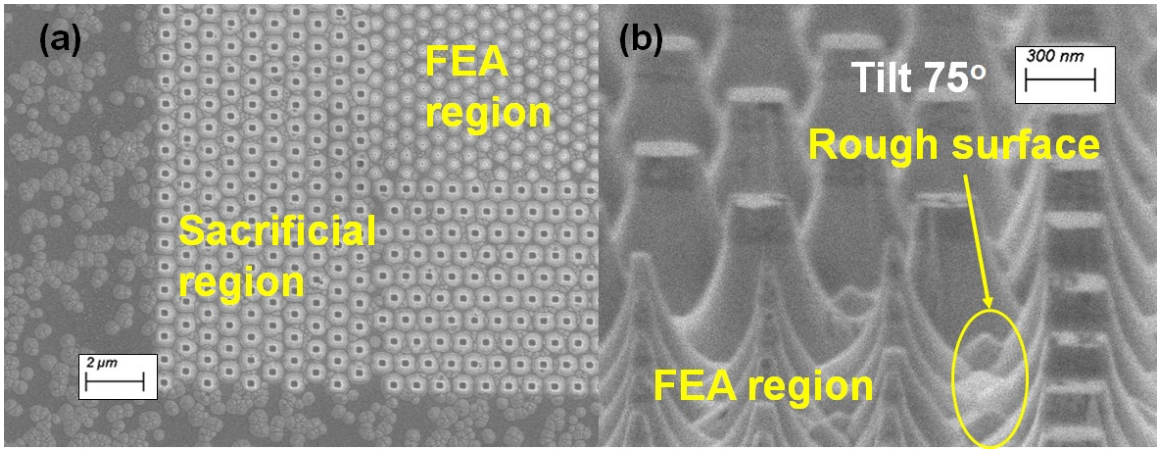


Figure 5-5: The SEM images of N-polar GaN FEA after SiO_2 mask is removed by BOE. The surface outside device region has a lot of pyramids, which cause rough surface (as shown in (a)).

RIE with Ti/Ni hard mask, and the metal mask is then removed by chemical etching (Ni etchant TFB and piranha clean). After that, the SiO_2 is used as hard mask for Cl_2/BCl_3-based ICP-RIE on GaN to form vertical pyramids. Unlike the Ga-polar GaN pyramids, the N-polar GaN pyramids do not show clear certain lattice planes on sidewalls (Fig. 5-3). The N-polar GaN vertical structures formed by dry etching look like cones (Fig. 5-3(a)).

After dry etching the GaN to form emitter tips, the wet-based DE is then applied

to sharpen the emitter tips (Table 4.1). Since the HCl is known to attack N-polar GaN [158], the SiO_2 mask is kept during the DE to provide additional protection on N-polar GaN emitter tips. After the same DE process, the shape of N-polar GaN tips is different from the shape of Ga-polar ones (Fig. 5-4). The N-polar GaN tips are also sharpened by the DE (Fig. 5-4(a)); while the N-polar surface becomes rough and some tips are broken or gone (Fig. 5-4(b)). The tip size variations could significantly affect the performance of SAGFEAs (Fig. 4-4). The N-polar GaN is known chemically unstable, for example, both HCl and TMAH-based developer attack N-polar GaN surface and generate a rough surface [158–160], so more study and experiments are necessary in the future to optimize the DE for N-polar GaN tips.

Since there are issues, such as tip size variation, broken tips, and rough surface, observed on N-polar GaN FEAs after 6 cycles of DE, the further DE process is thus avoided on this N-polar GaN sample. The SiO_2 mask on N-polar GaN tips is then removed and the devices are checked by SEM again (Fig. 5-5). The overall design of FEAs is kept, but the N-polar GaN surface becomes very rough with many small pyramids, which is probably formed during the dilute HCl step of the DE process (Fig. 5-5(a)). The tip size variation and the rough surface between tips are also observed in a FEA (Fig. 5-5(b)).

Besides the tip-size variation and rough surface, the SEM signal-strength difference in different regions of the N-polar GaN vertical pyramids is observed, while this is not observed in Ga-polar GaN (Fig. 5-4). The darker regions in the SEM image might indicate the higher n-type doping. In this case, Si is used as the donor for n-type doping, and prior work proposed and discovered that the heavily Si-doped GaN grown by MOCVD under the N-rich condition can form Si-segregated layer on the surface [161, 162]. High V/III ratio in MOCVD growth is a known approach to improve the N-polar GaN layer quality [163, 164], and it is applied in this sample growth. Therefore, though further investigation is still necessary in the future to understand this SEM signal-strength difference, one hypothesis is that Si segregation happens on the surface during the growth of the top n^+ N-polar GaN layer.

The 400-nm TEOS is then deposited and defined for the region at the gate pad,

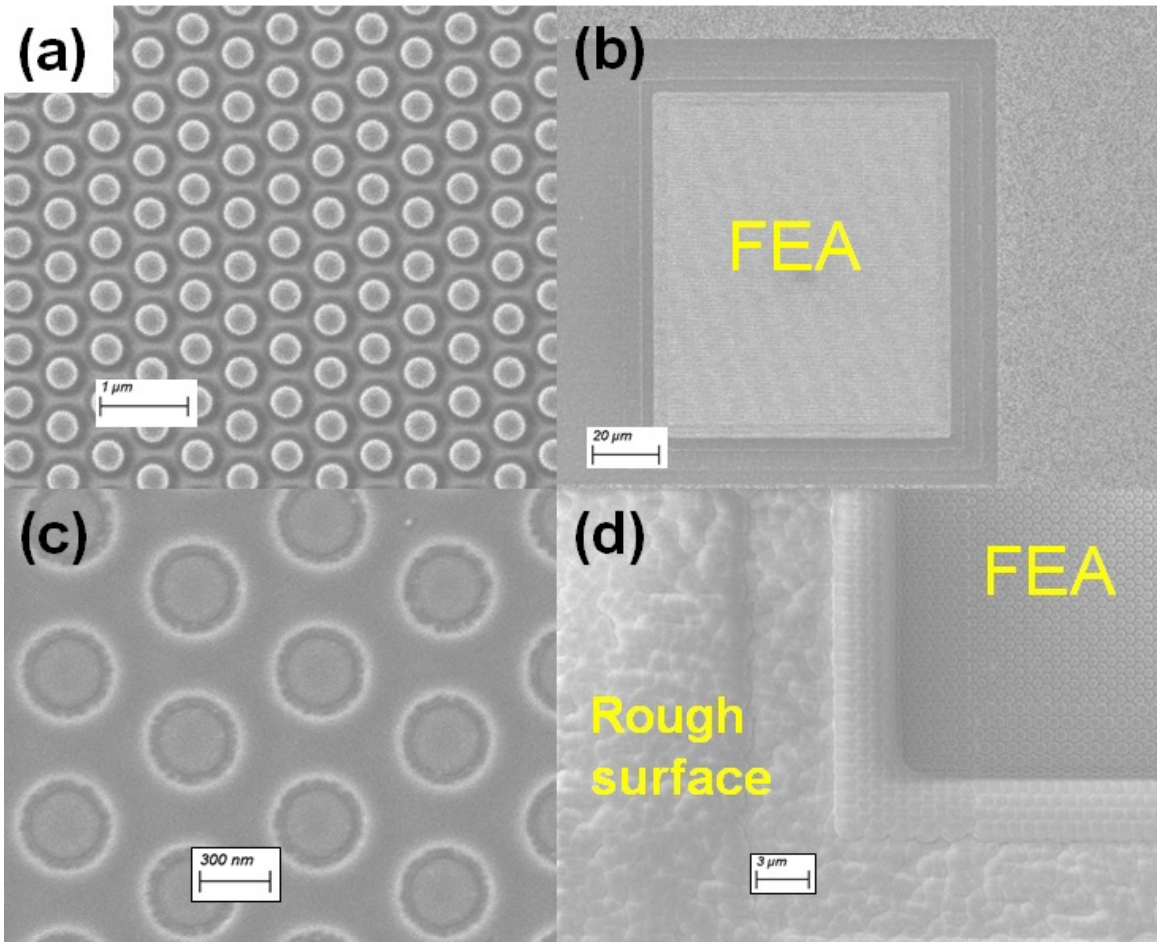


Figure 5-6: The SEM images of (a) (b) a N-polar GaN FEA after TEOS planarization and (c) (d) after gate metal (Cr) dry etching.

and the protecting layer of 10-nm Al_2O_3 is then deposited by ALD to protect tips from dry etching plasma in the later step. The gate stack of insulator (TEOS) and gate metal (Cr) is then deposited by PECVD and sputter, respectively. The TEOS planarization process is then used to planarize the device surface (Fig. 5-6(a) and (b)). The top surface of the gate metal is exposed and the sidewalls are still protected by TEOS (Fig. 5-6(a)), and the surrounding regions to extend out gate metal are also protected (Fig. 5-6(b)). The gate metal (Cr) is then etched by Cl_2/O_2-based ICP-RIE with TEOS protecting sidewalls (Fig. 5-6(c)). The rough surface outside the device region is still observed (Fig. 5-6(d)), and these defects under the gate stack can potentially become weak points and cause huge gate leakage during device operation.

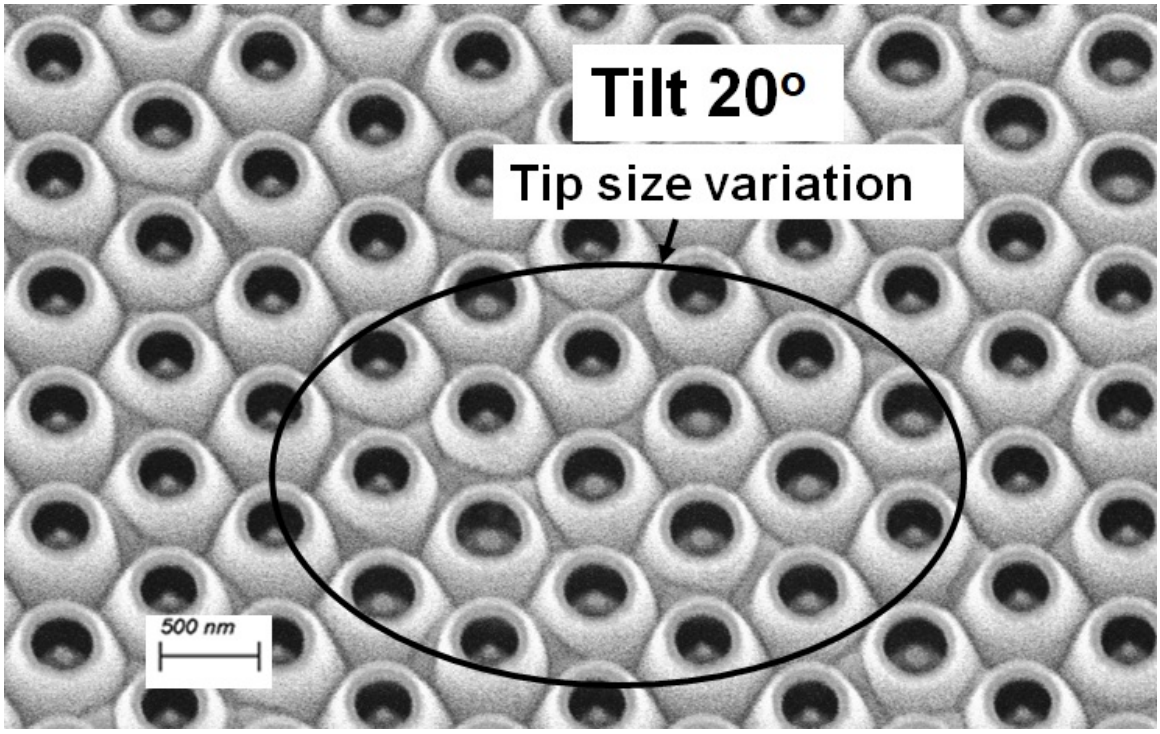


Figure 5-7: The SEM image of a finished N-polar GaN SAGFEA. The tip size variation is clearly observed.

After dry etching the gate metal, the ohmic contact on N-polar GaN is formed with a Ti/Al/Ti/Au metal stack. The N-polar GaN surface for ohmic contact is treated with dilute HCl to remove surface oxide right before the metal stack deposition. The gate metal pad (Ni/Au) is then deposited on the gate metal (Cr). Since the rough surface is observed outside the device region, the gate of different devices seems to connect together through the remaining gate metal on the non-uniform surface. Additional process step is added to wet etch the remaining gate metal to isolate each device (not shown here). Then the tip is finally exposed by a two-step etching process combining timed dry etching and the following short BOE etch for $20 \sim 25$ secs to remove both remaining TEOS and 10-nm Al_2O_3 protection layer. The finished devicce is checked by SEM, and the variation of tip sizes in a FEA is clearly observed (Fig. 5-7).

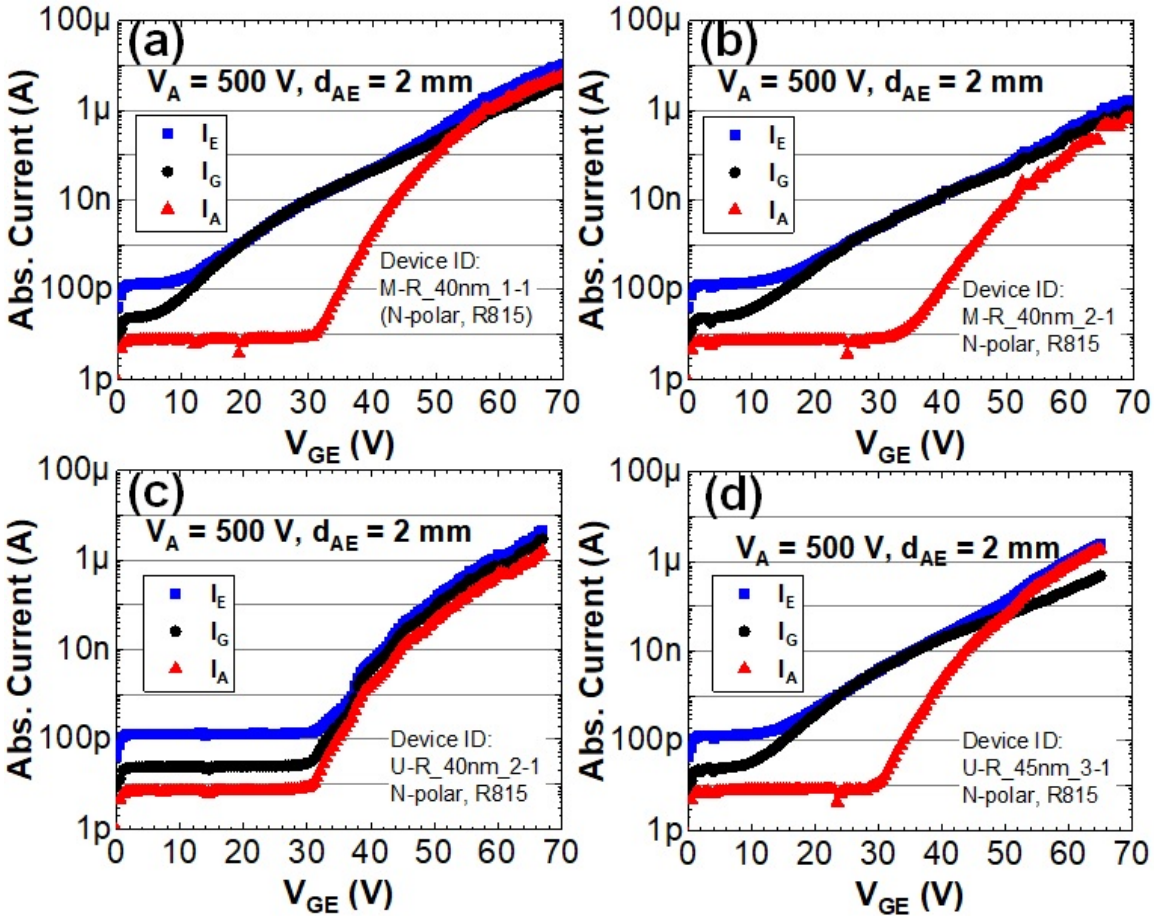


Figure 5-8: The transfer characteristics of 4 different N-polar GaN SAGFEAs on this N-polar GaN sample. Due to the rough surface and non-uniform emitter tips, the performance of these N-polar GaN SAGFEAs is not as good as Ga-polar GaN SAGFEAs reported in Chapter 4. The results are summarized in Table 5.1

5.2.2 Device performance and discussion

The sample is loaded into the UHV chamber for device measurement right after the SEM inspection. Transfer characteristics of four different N-polar GaN SAGFEAs after conditioning procedure (Appendix E) are plotted in Fig. 5-8. The measurement settings are the same as the one for Ga-polar GaN SAGFEA (Fig. 4-23). The anode voltage (V_A) is fixed at 500 V and the anode-emitter distance (d_{AE}) is about 2 mm. The gate leakage (I_G) of all measured devices is high, compared to the I_G of Ga-polar GaN SAGFEAs reported in chapter 4. The high gate leakage is probably resulted from the rough surface of N-polar GaN (Fig. 5-5 and Fig. 5-6(d)). The high gate leakage makes these N-polar GaN SAGFEAs not attractive for applications with

energy-efficiency requirements, and thus additional experiments and optimizations for DE on N-polar GaN are needed. For example, the process to remove surface oxide layer which still keeps the quality and roughness of N-polar GaN surface, will be critical. As both TMAH-based developer and HCl can attack the N-polar GaN surface, the plasma-type process might be necessary.

Besides the gate leakage of transfer characteristics, the anode current (I_A) of these N-polar GaN SAGFEAs is summarized in Table 5.1. All four devices have 150 $\times$ 150 emitter tips. The tip sizes of devices, shown in FIg. 5-8(a), (b), and (c), are designed to be similar, and thus their turn-on voltages ($V_{GE,ON}$) are similar. However, the anode current of these devices are very different, and the F-N parameters ($\ln(a_{FN})$ and -b_{FN}) are not similar. The best device has I_A of 6.2 μA at V_{GE} = 70 V, which is equal to about 80 mA/cm^2 in current density (J_A). To the best of author's knowledge, there is only limited work demonstrating N-polar GaN field emitters in literature [165]. The KOH is used to produce sharp N-polar GaN tips, whose tip diameter is reported to be below 20 nm [84,165]. However, the pyramid formation by KOH wet etching is not controlled by lithography or other patterning technologies, leading to the difficulty of integrating the self-aligned-gate structures on those N-polar GaN pyramids. Therefore, though the performance of our N-polar GaN devices is not as good as the performance of our Ga-polar GaN devices, these N-polar GaN SAGFEAs are likely to be the first demonstration of transistor-like N-polar FEAs with gate voltage below 100 V in the world. With further optimizations on process technologies on N-polar GaN, the device performance is expected to be improved and can potentially have better performance than Ga-polar GaN devices because of the lower electron affinity of N-polar surface [58].

Table 5.1: Summary of transfer characteristics of N-polar GaN SAGFEAs shown in Fig. 5-8. All N-polar GaN SAGFEAs summarized here have arrays consisting of 150 × 150 tips. Based on F-N parameters ($ln(a_{FN})$ and b_{FN}), there is variation in tip sizes in these field emitter arrays.

Device	$V_{GE,ON}$	I_A (@ V_{OV} = 30 V)	Max I_A (@ V_{OV})	$ln(a_{FN})$	$-b_{FN}$
(a)	31 V	1.65 μA	6.21 μA (39 V)	-10.403	-679.55
(b)	33 V	215 nA	651 nA (37 V)	-12.310	-713.87
(c)	31 V	507 nA	1.61 μA (36 V)	-13.089	-585.91
(d)	29.5 V	742 nA	1.9 μA (35.5 V)	-11.989	-614.31

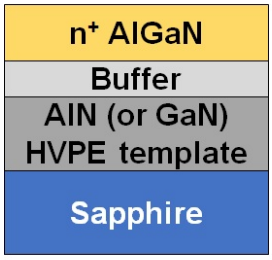
5.3 AlGaN self-aligned-gate field emitter arrays

In addition to the N-polar GaN, the AlGaN alloys with different Al composition are also fabricated as field-emission-based vacuum transistors. The electron affinities of AlGaN alloys are reported to be related to the Al composition ratio. The higher the Al composition in AlGaN is, the lower the electron affinity is [57].

The n^+ AlGaN materials are grown by Prof. William Alan Doolittle group at Georgia Institute of Technology by molecular beam epitaxy (MBE) on 10 mm × 10 mm AlN or GaN templates. The AlN or GaN templates are grown on sapphire substrate by hydride vapour phase epitaxy (HVPE). The information of three grown n^+ AlGaN coupons is summarized in Fig. 5-9. The Al compositions are 43.6%, 37.6%, and 65.7%, respectively, which are measured by x-ray diffraction (XRD). The electron concentrations, n^+ AlGaN film resistivity, and surface roughness are also measured by Prof. William Alan Doolittle group right after the MBE growth via hall measurement and atomic force microscope (AFM). Based on the measured electron concentrations, these three n^+ AlGaN materials are degeneratedly doped and their fermi levels are theoretically close to their conduction bands (E_C), which is ideal as field emitters.

5.3.1 Device fabrication and nuances from GaN devices

The process flow of AlGaN SAGFEAs is shown in Fig. 5-10, which is like the one in Fig. 4-16 with a small modification. An additional 40-nm Al layer is deposited on the surface by sputttering after the AlGaN emitter tip formation. This additional Al layer is used as a parallel conduction path for electrons flowing from the source



Sample ID	R641	R646	R647
AlGaN Al%	43.6%	37.6%	65.7%
AlGaN thickness	650 nm	420 nm	420 nm
Hall [n] (cm^{-3})	8.9×10^{19}	3.9×10^{19}	1.9×10^{19}
Resistivity	1.396 mΩ-cm	3.456 mΩ-cm	65.68 mΩ-cm
Grown on	GaN template	AlN template	AlN template
Surface roughness	0.643 nm	4.19 nm	2.4 nm

Figure 5-9: The n^+ AlGaN materials grown by molecular beam epitaxy (MBE) and their hall electron concentration and resistivity. These materials are provided through the courtesy of Prof. William Alan Doolittle group at Georgia Institute of Technology.

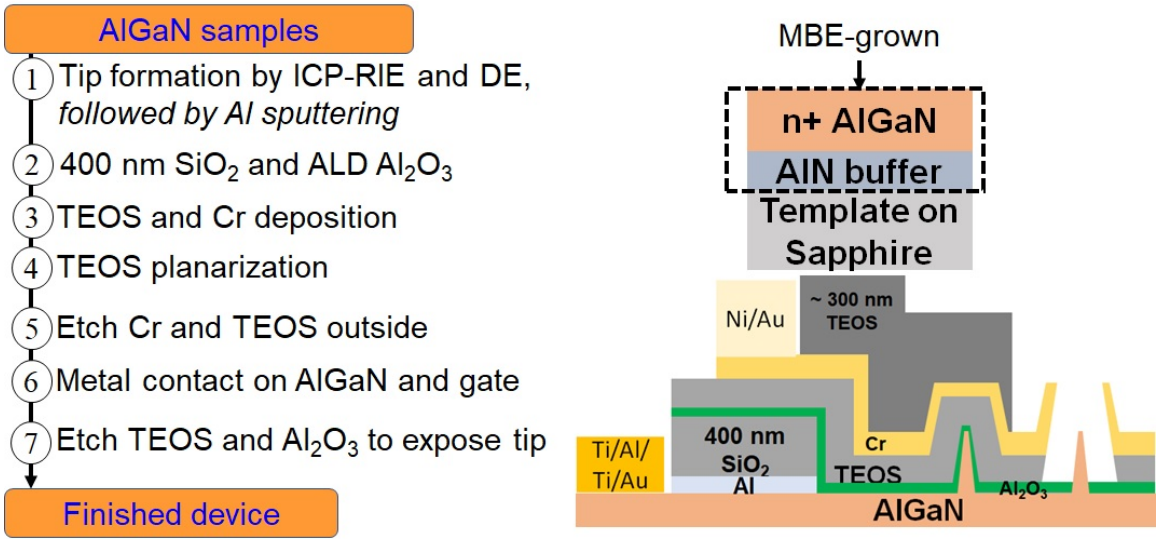


Figure 5-10: The process flow, epitaixial structure, and the cross-sectional diagram of finished device of the AlGaN SAGFEA. The process flow is similar to the one of 3rd-generation of GaN SAGFEAs, and the AlGaN devices' performance will be compared with 3rd-generation GaN devicecs. The Al sputtering in the 1st step after digital etching (DE) is to used to help electron conduction from contacts to FEA regions.

contact (Ti/Al/Ti/Au stack shown in Fig. 5-10) since the thickness of remaining n^+ AlGaN layer for this lateral electron conduction is only about 100 nm for both sample R646 and R647 (Fig. 5-9).

The first step is the tip formation. Similar to the GaN tips, the AlGaN emitter tips are first formed by Cl_2/BCl_3-based ICP-RIE with Ti/Ni hard mask defined by e-beam lithography with PMMA lift-off. The etching results of each sample is summarized as follows:

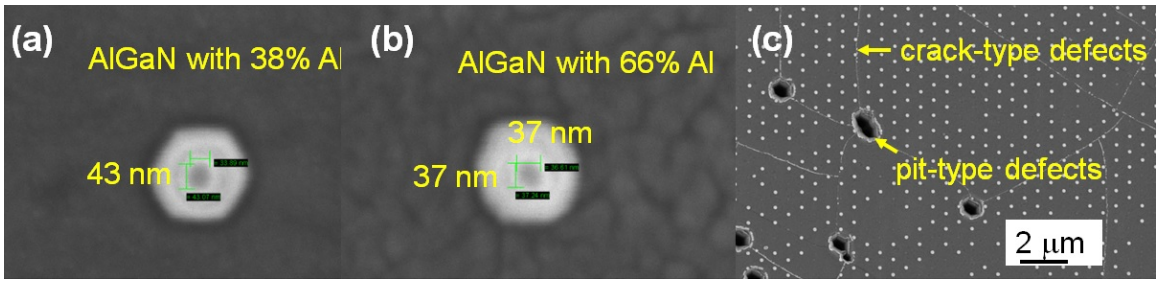


Figure 5-11: The SEM images of (a) 37.6%-Al and (b) (c) 65.7%-Al AlGaN after tip formation by ICP-RIE. The crack-type and pit-type defects are observed in AlGaN materials after dry etching, which can be resulted from growth or from the template underneath the AlGaN epitaxial layer (Fig. 5-9).

Sample ID	Dry etch recipe	Etch time	Estimated tip height
R641 (43.6% Al)	GaN-Fast (Cl-SAMCO)	85 sec	230 - 260 nm
R646 (37.6% Al)	GaN-Fast (Cl-SAMCO)	85 sec	270 - 300 nm
R647 (65.7% Al)	GaN-Fast (Cl-SAMCO)	92 sec	250 - 300 nm

where the tip height is estimated based on the meas height measured by surface profiler. The surface of sample R647 becomes rough after dry etching, and thus the estimated height has a large variation range. The dry etching recipe is summarized in Appendix D. The AlGaN emitter tips formed by dry etching are checked by SEM (Fig. 5-11). It is noticed that the etched sidewall surface of 65.7%-Al AlGaN (Fig. 5-11(b)) is a bit rougher than the one of 37.6%-Al AlGaN (Fig. 5-11(a)). Additionally, the crack-type defects are observed on all three samples, while the pit-type defects are only observed on 65.7%-Al AlGaN (Sample R647) (Fig. 5-11(c)). The crcak-type defects might be resulted from the lattice mismatch between the template and AlGaN layer, and the pit-type defects are likely resulted from the defects in the template, based on the discussion with Prof. William Alan Doolittle group.

The AlGaN emitter tips are then sharpened by the wet-based DE process. The tip shrinking rates of metal-polar AlGaN tips and GaN tips are summarized in Fig. 5-12(a). The sidewall etching rate of high-Al AlGaN is higher than the ones of low-Al AlGaN and GaN. Furthermore, the sidewalls of AlGaN pyramids after DE are rough, especially for the high-Al (65.7%) AlGaN (Fig. 5-12(b) and (c)). Though the reasons of these differences are not clear yet, there are some possible explanations. First of all, the Al_2O_3 and Al can be etched by piranha [166], so the piranha step

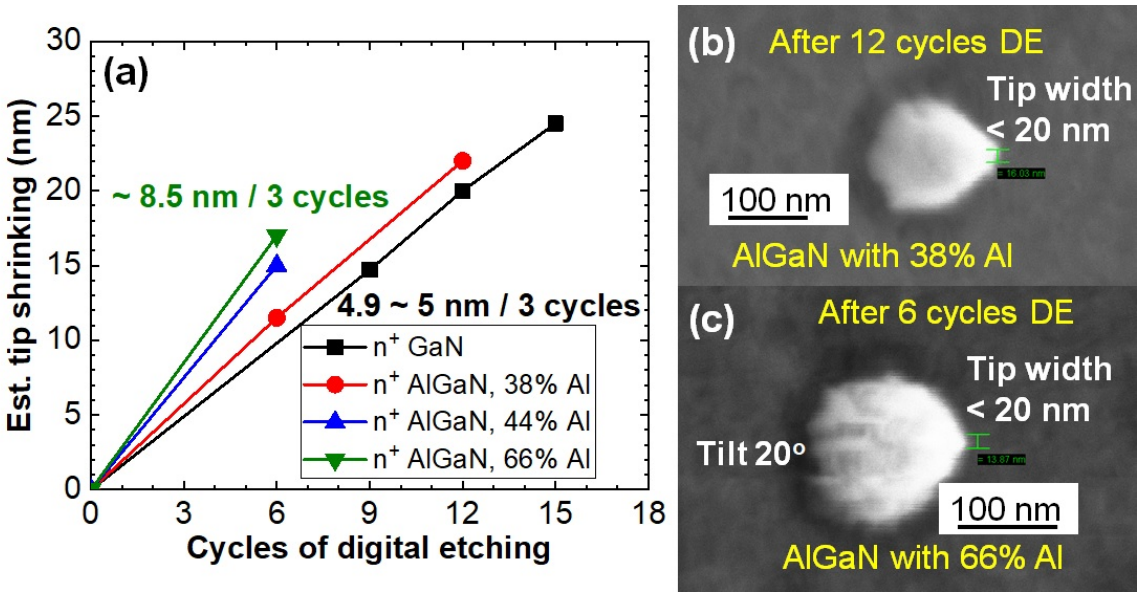


Figure 5-12: The digital etching (DE) results on different III-Nitride pyramids. (a) The tip shrinking rate of high-Al AlGaN pyramid is higher than the ones of low-Al AlGaN and GaN pyramids. The SEM images of (b) 37.6%-Al and (c) 65.7%-Al AlGaN pyramids after DE show rough sidewalls. Piranha might not only oxidize the surface but also etch Al and AlO_x existing on AlGaN pyramids.

in the DE might not only oxidize the surface but also directly etch Al_2O_3 formed on the AlGaN. Secondly, the The III-N semi-polar sidewalls can be more chemical reactive than the metal-polar c-plane surface [167], and thus the rough sidewalls from AlGaN pyramids might be resulted from the microfaceting due to the orientation-dependent etching rates [168, 169]. Thirdly, the rough sidewalls might be related to the probable segregation in AlGaN alloys during growth [170, 171]. Investigation of these hypotheses requires more study in the future.

After the tip formation and the sharpening by DE, the 40-nm Al is deposited by sputter, and the 400-nm SiO_2 is deposited by PECVD to increase the insulator thickness under the gate pad region (As shown in Fig. 5-10). After defining the area of this thick SiO_2 layer by lithography and BOE wet etching, the 10-nm Al_2O_3 is then deposited by ALD to protect the AlGaN emitter tips. After that, the following steps are similar to the ones of Ga-polar GaN SAGFFEAs. The devices after TEOS planarization are checked by SEM (Fig. 5-13). And after the metal contact formation on n^+ AlGaN and on gate metal (Cr), the emitter tips are finally exposed by timed

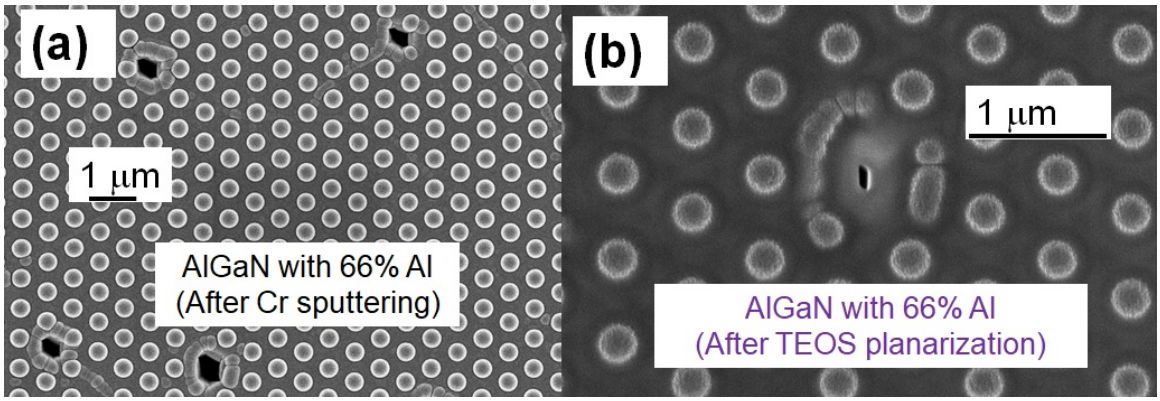


Figure 5-13: SEM images of 65.7%-Al AlGaN SAGFEA (a) after gate metal (Cr) sputtering and (b) after TEOS planarization. The pit-type defects are still observed, while they do not affect the process significantly.

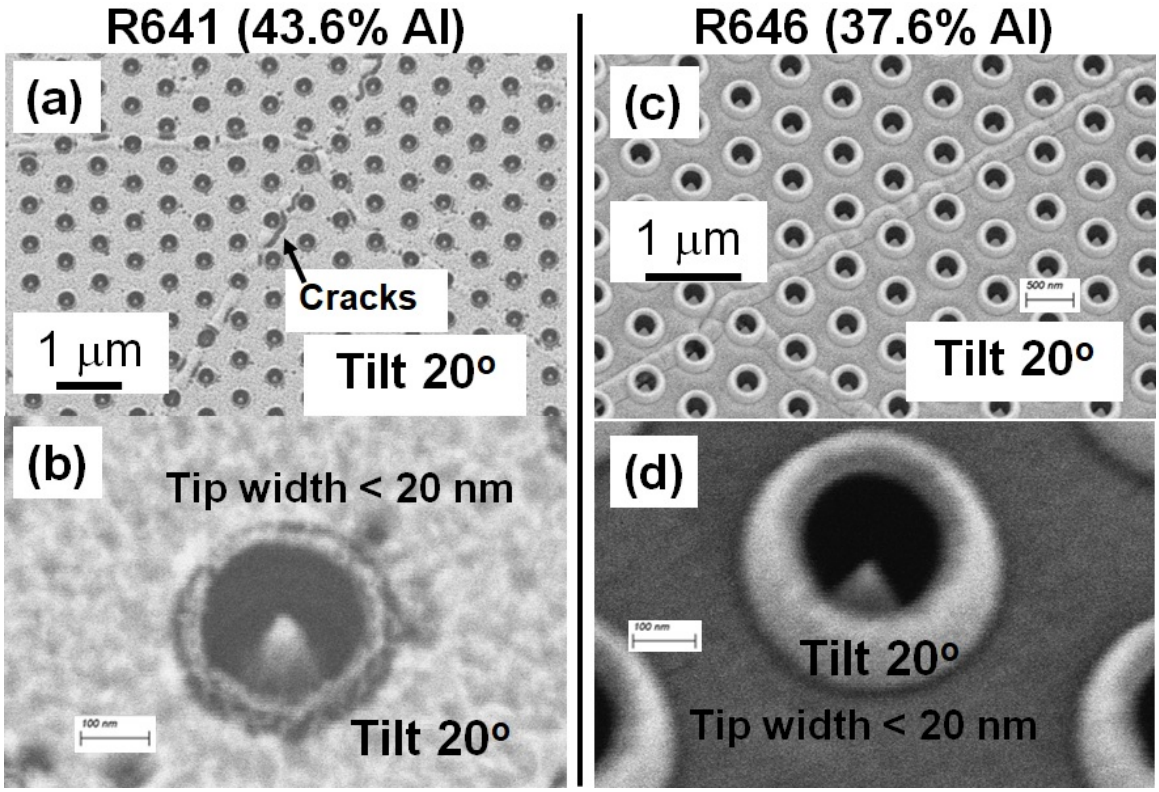


Figure 5-14: SEM images of finished (a) (b) 43.6%-Al and (c) (d) 37.6%-Al AlGaN SAGFEAs. The cleaning steps are different in two samples, leading to different surface morphology. The R641 sample is cleaned by oxygen plasma in an asher (Asher-Chuck-ESI). The oxygen plasma seems too aggressive and the gate metal surface is roughened and gate layer cracks. The other sample (R646) is thus only cleaned by NMP. The Oxygen plasma recipe is 2000 sccm O_2 and 100 sccm N_2 at 1.2 Torr, 250^{o}C, and RF 900 W for 45 sec.

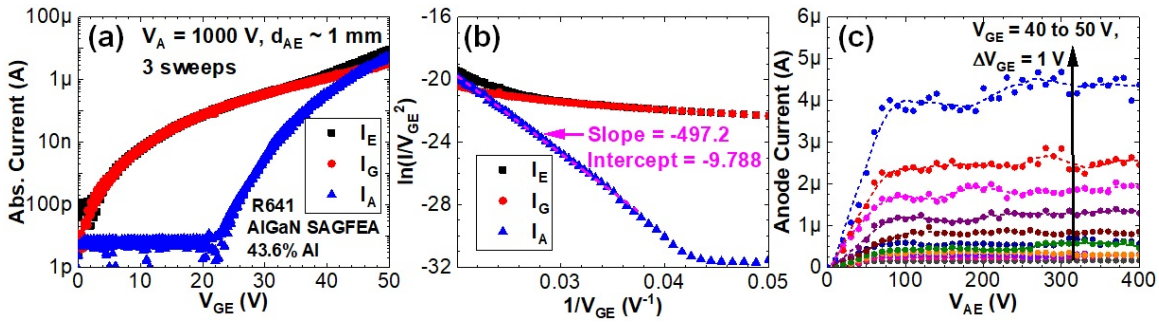


Figure 5-15: (a) Transfer characteristics, (b) corresponding F-N plot, and (c) output chracteristics of a 43.6%-Al AlGaN SAGFEA. As the gate is damaged by oxygen plasma, the gate leakage (I_G) is clearly much higher than the anode current (I_A).

slow dry etching followed by a short BOE wet etching. After that, two samples go through different resist cleaning steps. The sample R641 (43.6% Al) was cleaned by the new asher with oxygen plasma at 250^{o}C. However, after the asher process, the gate metal (Cr) seems to be damaged since the rough surface and cracks are observed by SEM (Fig. 5-14(a) and (b)). Therefore, another samples are only cleaned by N-Methyl-2-pyrrolidone (NMP) to remove the resist. The devices cleaned by NMP are not damaged (Fig. 5-14(c) and (d)). The samples are quickly loaded into the UHV chamber for measurement after the SEM.

5.3.2 Device performance and discussion

AlGaN SAGFEAs with three different Al composition are characterized. Since the fabrication is not finished at the same time, they are measured separately.

First, the transfer charactreristics and the corresponding F-N plot of a 43.6%-Al AlGaN SAGFEA (sample R641, damaged by asher process) are plotted in Fig. 5-15(a) and (b). The anode voltage (V_A) is kept 1000 V and the anode-emitter distance (d_{AE}) is kept $\sim$ 1 mm. The gate leakage is significantly high at OFF state, which can be resulted from the damages induced by asher process. Though the leakage is high, the anode current still shows stable field emission current after conditioning (Appendix E). The overall performance, other than the gate leakage, seems comparable with the performance of 2nd-generation GaN SAGFEAs (Fig. 4-12). After the stable transfer characteristics are observed, the output characteristics are measured (Fig. 5-15(c)).

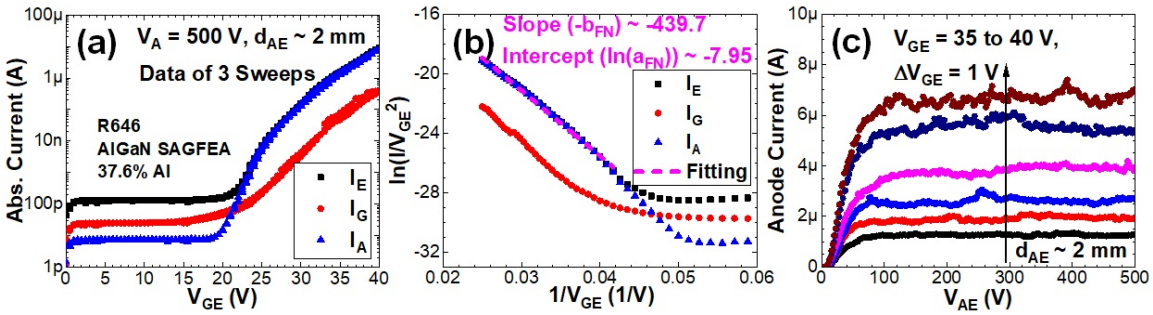


Figure 5-16: (a) Transfer characteristics, (b) corresponding F-N plot, and (c) output characteristics of a 37.6%-Al AlGaN SAGFEA. Without oxygen plasma damage, the device has good performance and low gate leakage.

Though the high V_{AE} is required ($\sim$ 100 V) to reach the saturation regime due to the long d_{AE}, the device still has a transistor-like behavior with good saturation. However, to prevent the failure of this device, the output characteristics at higher V_{GE} bias condition (above 50 V) are not measured since some AlGaN devices break when the V_{GE} is applied above 50 V.

Different from the devices damaged by the asher process, the 37.6%-Al AlGaN SAGFEAs cleaned by NMP do not have significant gate leakage (Fig. 5-16(a) and Fig. 5-17(a)). The transfer characteristics, corresponding F-N plot, and output characteristics of one of the best 37.6%-Al AlGaN SAGFEAs are shown in Fig. 5-16. The V_A is kept at 500 V for transfer characteristics, and the d_{AE} is kept $\sim$ 2 mm for all measurement on this device. In transfer characteristics, the turn-on voltage ($V_{GE,ON}$) at I_A = 10 pA is about 20 V, and the maximum I_A is about 8 μA at V_{GE} = 40 V ($V_{OV} = V_{GE}$ - $V_{GE,ON}$ = 20 V), which corresponds to a current density (J_A) of $\sim$ 100 mA/cm^2. The gate leakage is always about 1-2 orders of magnitude lower than I_A when V_{GE} is above 25 V. The magnitude of F-N slope (b_{FN}) is $\sim$ 439.7 V. The device also has clear saturation in output characteristics (Fig. 5-16(c)).

Since these 37.6%-Al AlGaN SAGFEAs are not damaged by asher process, the device yield is higher than the devices damaged by the asher. Therefore, the long-term stability can be measured on some AlGaN SAGFEAs. After conditioning, the device transfer characteristics are measured (dots in Fig. 5-17(a)). The DC device stability test (lifetime test) is then conducted with a fixed bias condition (V_{GE} = 37 V and V_A

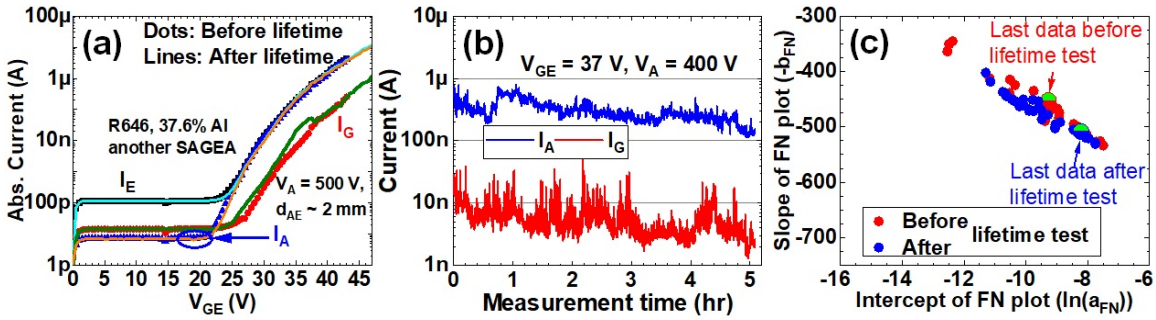


Figure 5-17: (a) Transfer characteristics, (b) DC device stability test, and (c) S-K plot of another 37.6%-Al AlGaN SAGFEA. The DC stability test is conducted by monitoring current flowing through all three terminals with a fixed bias condition (V_A = 400 V and V_{GE} = 37 V). The change between different I-V sweeps in the S-K plot might indicate that the temporary surface modification happens and the effective emitting tip apex changes [106]. Nevertheless, the transfer characteristics and the data-point distribution in the S-K plot show that this AlGaN SAGFEA is very stable without clear degradation after 5-hour DC stress.

= 400 V). Both anode and gate current are recorded during this stability test (Fig. 5-17(b)). Though the data are noisy, the anode current is found always more than an order of magnitude higher than the gate leakage. The noise in measurement might be resulted from the residual gas adsorption and desorption or other surface mechanisms happen during the measurement [35]. After about 5 hours of DC stability test, the anode current seems to be less than half of the initial value when the stability test starts, so the test stops. The transfer characteristics are then measured again after the stability test (lines in Fig. 5-17(a)), and there is no significant discrepancy between the curves before and after the 5-hr DC stability test. Furthermore, the extracted F-N parameters of all stable transfer characteristics of this device are plotted in the S-K plot (Fig. 5-17(c)). There is no clear change after the lifetime test, indicating that this is a stable field-emission vacuum transistor.

The transfer characteristics of two high-Al (65.7%-Al) AlGaN SAGFEAs are measured (Fig. 5-18). The V_A is fixed at 1000 V and d_{AE} is kept $\sim$ 1 mm. As some of these high-Al AlGaN SAGFEAs are found easily broken during the measurement and the gate shorts to the emitter, to try reducing the possibility of device breakdown, the curves in Fig. 5-18(a) are obtained using the slow-pulse setting of the Keithley SMUs (model: Keithley 237 High Voltage Source Measurement Unit) for V_{GE} sweep,

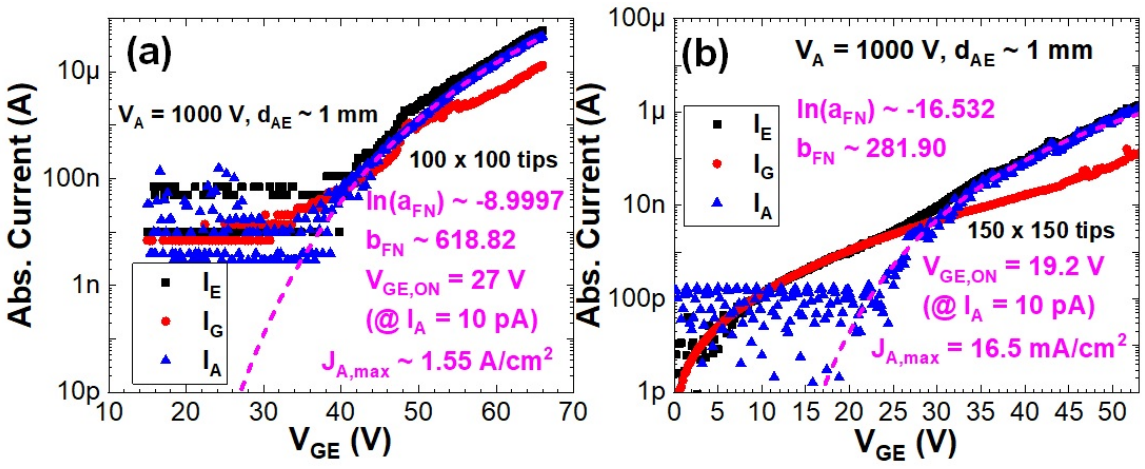


Figure 5-18: Transfer characteristics of 65.7%-Al AlGaN SAGFEAs (a) with 100 × 100 tips and (b) with 150 × 150 tips. The defects and rough sidewalls (Fig. 5-12(c)) on these 65.7%-Al AlGaN SAGFEAs can be the cause of high gate leakage, while the detailed study is still necessary in the future.

whose pulse width is in the order of ms. The V_{GE} is at 0 V when the pulse is OFF, and is pulsed to the bias voltage when ON. The ON time of the pulse (T_{ON}) is 20 ms and the OFF time (T_{OFF}) is 200 ms. The pulse setting has a higher noise level in measurement (∼ few nA level), so the extrapolation of the anode current is used to estimate the turn-on voltage ($V_{GE,ON}$) at I_A = 10 pA. The $V_{GE,ON}$ is 27 V, and the maximum anode current is about 45.4 μA at V_{GE} = 66 V, which corresponds to the current density (J_A) of about 1.55 A/cm^2. The gate leakage is as high as the anode current in this device.

Another 65.7%-Al AlGaN SAGFEA with 150 × 150 tips is also measured (Fig. 5-18(b)). The measurement was conducted by the same Keithley SMUs, but it is done in DC sweep mode, and thus the noise levels are lower. This device has a lower $V_{GE,ON}$ of ∼ 19.2 V, but the maximum anode current is only about 1.3 μA at V_{GE} = 53 V before the device fails. There is still noise in the anode current in this log-scale transfer characteristics, indicating the device conditioning is not fully finished yet (Appendix E).

The high gate leakage and device failure of these high-Al (65.7%-Al) AlGaN SAGFEAs are probably resulted from the rough sidewalls of emitter pyramids, rough surface, and the defects observed on the etched surface (Fig. 5-11(b) and (c) and Fig.

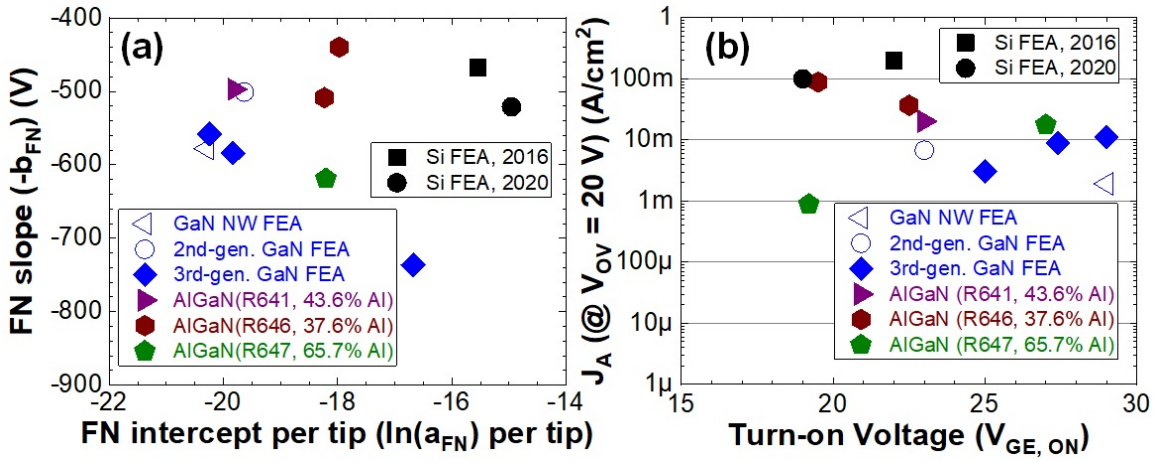


Figure 5-19: The (a) S-K plot of Si SAGFEAs, different GaN SAGFEAs (1st, 2nd, and 3rd generations), and different AlGaN SAGFEAs. (b) The turn-on voltage ($V_{GE,ON}$) versus anode current density (J_A) at the same bias condition of different SAGFEAs [48, 49]. As the fabrication and critical process steps are not optimized for AlGaN materials (like rough sidewalls shown in Fig. 5-12(b) and (c)), the performance of AlGaN SAGFEAs do not show clear trend of improvement when the Al composition is increased. The $V_{GE,ON}$ is defined as V_{GE} at I_A = 10 pA, and $V_{OV} = V_{GE}$ - $V_{GE,ON}$.

5-12(c)). Further optimization on etching steps, such as dry etching and following DE process, are necessary in the future to improve the performance and stability of these high-Al AlGaN SAGFEAs.

The S-K plot and performance benchmarks of different devices are summarized in Fig. 5-19. Since the AlGaN SAGFEAs are fabricated using the same pattern design as the 3rd-generation GaN SAGFEAs, the performance is compared between our AlGaN SAGFEAs, 1st-3rd generations of Ga-polar GaN SAGFEAs, and the state-of-the-art Si SAGFEAs in literature [48,49]. Based on the S-K plot, the 37.6%-Al AlGaN SAGFEAs are slightly better than our 1st, 2nd, and 3rd generations of GaN SAGFEAs since they have a slightly lower $|b_{FN}|$ (Fig. 5-19(a)). It could indicate that the effective work functions of these 37.6%-Al AlGaN SAGFEAs are slightly lower than the ones of GaN SAGFEAs [106]. However, there is no clear trend between SAGFEAs with different Al compositions, which can be resulted from the non-optimized process steps or other issues such as, surface-states-induced band bending [172]. The performance of 37.6%-Al AlGaN SAGFEAs is close to the state-of-the-art Si SAGFEAs at the same bias condition (V_{OV} = 20 V) (Fig. 5-19(b)), and it is believed that AlGaN

SAGFEAs can provide better performance than Si SAGFEAs once the process steps are optimized.

5.3.3 Material property characterization

The AlGaN SAGFEAs with different Al compositions are fabricated and characterized, and 37.6%-Al AlGaN SAGFEAs seem to have a slightly lower work function than Ga-polar GaN SAGFEAs (Fig. 5-19(a)) [106]. However, based on the reported electron affinities of different AlGaN alloys (Fig. 1-6(a)), the work function of the n^+ 65.7%-Al AlGaN alloy is expected to be 2 eV or below, and thus the AlGaN SAGFEAs should theoretically have much better performance than GaN devices (Fig. 5-1(b)). Nonetheless, the experimental data do not agree with the original expectation, which can be resulted from the issues of un-optimized process steps or the unsatisfactory properties of the AlGaN surface [172]. Before the optimization of process steps, the fundamental properties of III-Nitrides' surface for field emission should be also studied.

As the band diagram shown in Fig. 5-1(a), the field emission properties of a material is highly determined by its surface work function. Ideally, the work function of degeneratedly doped n-type semiconductor should be close to its electron affinity, but the surface states on III-Nitrides surface are known to induce surface band bending and can affect the field emission properties [172–175]. Therefore, the surface work functions of III-Nitride semiconductors are characterized by ultraviolet photoelectron spectroscopy (UPS), which is helped by Dr. Tyson Back at Air Force Research Laboratory (AFRL) (Table 5.2). The raw data of UPS measurement are shown in Fig. 5-20.

The n^+ GaN on Si grown by Enkris, Inc via MOCVD, the n^+ AlGaN grown by Prof. William Alan Doolittle group at Georgia Institute of Technology via MBE, and the AlGaN template provided by DOWA corporation are measured. The doping concentration of n^+ GaN is $\sim 10^{19}$ cm^{-3}, and the hall carrier concentrations of different AlGaN materials are 6×10^{19} cm^{-3}, 3.5×10^{19} cm^{-3}, and 8.3×10^{18} cm^{-3}, for MBE-grown 50%-Al and 70%-Al n^+ AlGaN, and 70%-Al n-type AlGaN

template, respectively. Since the doping concentration ([Si] in n^+ GaN) and the electron concentrations of AlGaN alloys are higher than their effective densities of states in the conduction band (N_C), these semiconductors are degeneratedly doped. The work function (WF) of n^+ GaN measured by UPS is about 3.3 eV, which is in the range of electron affinities of GaN [57, 58]. However, the measured work functions of all three AlGaN materials are significantly higher than their electron affinities (Fig. 1-6(a)) [57]. The high work functions of these AlGaN materials could be caused by the surface oxidization or the surface states; therefore, the additional UPS measurement after the dilute HCl treatment to remove surface oxide is then conducted for all samples, which is also helped by Dr. Tyson Back at AFRL. However, the work functions of n^+ GaN and MBE-grown n^+ AlGaN materials after the dilute HCl treatment have similar or slightly higher values than the ones before HCl treatment. The work function of n-type 70%-Al AlGaN template is the only one that decreases after the HCl treatment, while the value is still much higher than the expected electron affinity of 70%-Al AlGaN, which is below 2 eV (Fig. 1-6(a)). Though the surface oxide formation cannot be fully ruled out since the HCl treatment is an ex-situ treatment in this study, the high work functions of n^+ high-Al AlGaN materials are more likely due to the surface band bending induced by the surface states [172, 173]. The surface band bending can potentially be estimated by carefully-designed UPS and x-ray photoluminescence spectroscopy (XPS) experiments, as reported in prior work done on H-terminated phosphorus-doped n-type diamond [176]. It is clearly shown that even the electron affinity can be negative on the H-terminated diamond surface, the work function is still positive because of the surface band bending. The relative positions between surface fermi level and surface conduction band can be estimated, and thus the surface band bending can be estimated by assuming the fermi-level position in the bulk semiconductor based on dopant activation energy and fermi-dirac distribution [177]. The different surface structures and surface bondings are also shown to affect the electron emission and device behavior in diamond field emitters [178, 179]. The approaches to prepare the AlGaN emitter surface, such as removing the adsorbed water vapor on the surface and surface passivation for surface states, and their effects

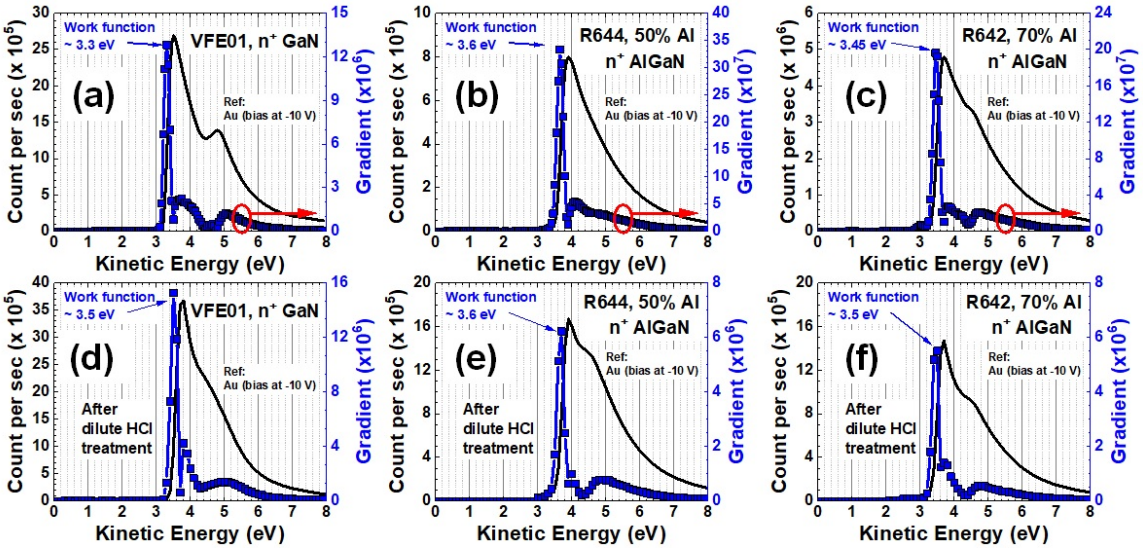


Figure 5-20: The UPS measurement results of (a) (d) GaN, (b) (e) 50%-Al AlGaN, and (c) (f) 70%-Al AlGaN for work function extraction. The measurements are conducted (a) (b) (c) before and (d) (e) (f) after the dilute HCl treatment. The raw data are provided by Dr. Tyson Back at AFRL.

on surface band bending could be important to enable the high-performance AlGaN field-emission-based vacuum transistors in the future [180].

Table 5.2: Summary of surface work function (WF) of different III-Nitride semiconductors. The work function measurement is helped by Dr. Tyson Back at Air Force Research Laboratory (AFRL) by ultraviolet photoelectron spectroscopy (UPS). The work function is measured before and after the dilute HCl treatment. It should be noted that the samples are exposed to the ambient air before the UPS measurement, so the measured surface might not be identical to the ones of fabricated devices. Furthermore, the different lattice orientations on our III-Nitride filed emitter tips might have different work functions, but only c-plane (0001) surface is measured here.

	n^+ GaN on Si	n^+ AlGaN	n^+ AlGaN	n AlGaN
Growth	MOCVD	MBE	MBE	MOCVD
Grower	Enkris	Georgia Institute of Technology		DOWA
Al comp. (x)	0%	50%	70%	70%
[n] (cm^{-3})	[Si] $\sim 10^{19}$	6×10^{19}	3.5×10^{19}	8.3×10^{18}
N_C (cm^{-3})	2×10^{18}	4.2×10^{18}	5×10^{18}	5×10^{18}
WF before HCl	$\sim$ 3.3 eV	$\sim$ 3.6 eV	$\sim$ 3.45 eV	$\sim$ 4.3 eV
WF after HCl	$\sim$ 3.5 eV	$\sim$ 3.6 eV	$\sim$ 3.5 eV	$\sim$ 3.8 eV

5.4 Conclusion and future work

To further improve the performance of III-Nitride field emitters, the SAGFEAs based on N-polar GaN and AlGaN with different Al compositions are developed and demonstrated in this chapter. Most of the work on N-polar GaN or high-Al AlGaN field emitters in literature is two-terminal devices because of the complex and difficulty of the self-aligned-gate structures and the corresponding process integration. To author's best knowledge, the N-polar GaN and high-Al AlGaN SAGFEAs reported in this chapter are likely the first demonstration of vacuum transistors with sub-100-V gate operating voltage using these materials.

The electron concentrations of N-polar n^+ GaN grown by MOCVD and metal-polar n^+ AlGaN materials are confirmed to be higher than their effective conduction band densities of states. However, since the process steps are not optimized for N-polar GaN nor for the AlGaN, there are issues observed during the device fabrication. For example, the dilute HCl step in the DE process probably causes the problems of rough surface and broken tips on N-polar GaN devices (Figs. 5-4 and 5-5). These issues cause the high gate leakage and the worse performance of the N-polar GaN SAGFEAs. The low F-N intercepts ($\ln(a_{FN})$) of measured N-polar SAGFEAs indicate the nonuniform tip size distribution in the FEA (Table 5.1). More experiments and study on optimizing critical process steps for N-polar GaN devices are still necessary.

Besides the N-polar GaN, the AlGaN SAGFEAs with 37.6%-Al composition show slight performance improvement from the Ga-polar GaN SAGFEAs with the same structure design, which is the 3rd-generation device design in chapter 4. However, there is no performance improvement when the Al composition in AlGaN devices increases from 37.6% to 65.7%. Furthermore, the measured surface work function of high-Al n^+ AlGaN is not lower than the work function of n^+ GaN (Table 5.2). There are two possible hypotheses for this discrepancy between the expected performance improvement from low electron affinity and the experimental data: (1) the non-ideal sidewall roughness and non-optimized process steps for AlGaN, and (2) the surface-state-induced band bending. The rough sidewalls of high-Al AlGaN emitter pyramids

observed after DE process can provide additional undesirable emitting spots on the sidewalls and induce more gate leakage between the gate and emitter. The crack and pit-type defects observed on the film might also indicate that the materials are not at their highest quality yet. On the other hand, the surface states can cause surface fermi-level pinning, and thus the surface work function is much higher than the electron affinity of the material. More study on surface properties, treatment, and passivation for surface states is necessary to improve the AlGaN field-emission-based vacuum transistors and push them to the expected high performance regime.

Other than the optimization of process flow and the understanding of the surface properties of high-Al AlGaN, there are other aspects can be studied in the future. For example, the polarization engineering of III-Nitrides' surface has been demonstrated to reduce electron emission barriers in field emitters [26]. The regrowth of InGaN on top of GaN pyramid tips to reduce the surface electron emission barrier can be a promising approach since the developed process flow for self-aligned-gate structures can still be used to build compact vacuum transistors with polarization-engineered emitter surface. Additionally, the N-polar high-Al AlGaN materials are expected to be better than N-polar GaN and metal-polar AlGaN materials, while the growth of N-polar high-Al n^+ AlGaN could be more challenging and the process integration might be more difficult due to the chemical instability of N-polar surface. The proper passivation of surface states will also be critical for these highly reactive surfaces.

Though the performance of N-polar and high-Al AlGaN devices does not show significant improvement from the Ga-polar GaN devices, the developed process flows are demonstrated for the fabrication of different III-Nitride SAGFEAs. With further optimizations and study in the future, these III-Nitride SAGFEAs are expected to provide better performance than the state-of-the-art GaN SAGFEAs.

Chapter 6

Development of fully-integrated vacuum transistors

GaN and AlGaN SAGFEAs are demonstrated in this PhD thesis research and the performance of GaN devices has been improved with a 3-order-of-magnitude enhancement in current density (Chapter 4). However, one of the metal terminals, anode, is still not integrated into the devices. The long vacuum channel leads to the high voltage requirement for the anode terminal to conquer the space-charge limit. Additionally, the missing of integrated anode terminal is one main issue when building the circuit-level prototypes/products based on these vacuum transistors. Different approaches had been demonstrated to integrate the anode [181–184], while there is limited work on three-terminal transistor-like or triode-like devices. Therefore, to build the fully-integrated field-emission-based vacuum transistors, two different approaches are proposed and tested with preliminary experiments in this chapter.

6.1 Motivation of integrated-anode structures

The GaN and AlGaN SAGFEAs fabricated and characterized in the prior chapters are not stand-alone vacuum transistors since the anode terminal is a suspended metal ball in the UHV measurement system. The vacuum channel length is at the order of mm in all measurement in chapters 3, 4, and 5, leading to a high anode voltage required to

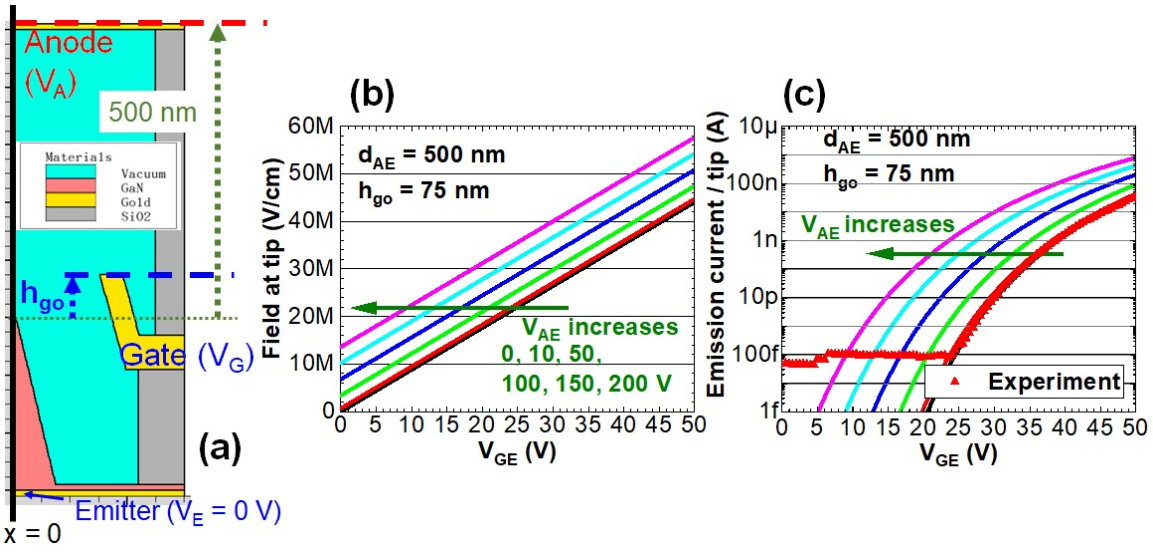


Figure 6-1: (a) The structures and (b) the peak electric field versus bias voltages simulated by Silvaco TCAD, and (c) the estimated emission current per tip based on the simulated peak electric field and equations in literature [34]. A self-aligned-gated GaN field emitter tip is simulated in a cylindrical symmetry along x = 0 (shown in (a)). A minor short channel effect is observed while the device can still be properly controlled by the gate.

approach the saturation regime in output characteristics (> 80 V in Figs. 4-24(b) and 5-16(c)). Without the integrated anode, these field-emission-based vacuum transistors are not capable of circuit-level applications due to scale-up difficulty. Therefore, the anode integration is necessary. However, with a short vacuum channel length with a μm or sub-μm length, the non-ideal behavior for the voltage-controlled current sources is observed in simulation (Fig. 6-1(c)) as the electric field from anode-emitter bias voltage (V_{AE}) can now affect the electric field on the tip surface ($\overrightarrow{E}$) (Fig. 6-1 (a) and (b)), which can be represented:

$$\overrightarrow{E} = \beta_{GE} * V_{GE} + \beta_{AE} * V_{AE} \tag{6.1}$$

where the anode-emitter field factor (β_{AE}) indicates the electric field induced by anode-emitter bias voltage (V_{AE}). Based on simulated electric field (Fig. 6-1(a)), the β_{AE} is about 6.8 $\times$ 10^4 cm^{-1}, which is about 10 % of the gate-emitter field factor, β_{GE}, which is about 8.8 $\times$ 10^5 cm^{-1}. Though β_{AE} is smaller than β_{GE} in this designed

structure, this phenomenon can be regarded as a short channel effect in these vacuum transistors, and careful study in device structure design is necessary. For example, the height difference between the gate metal and GaN emitter tip (h_{go} in Fig. 6-1(a)) is a critical parameter. If the gate is lower than the emitter tip, that is, h_{go} is a negative value, the gate can not properly screen out the electric field from the anode and the gate control can significantly degrade [184]. On the other hand, when the gate is higher than the tip ($h_{go} > 0$), the electric field from the anode is largely screened by the gate, but it can still slightly increase the peak electric field (Fig. 6-1(b)) and the estimated transfer characteristics show a reduction of operating voltage (V_{GE}) with a high V_{AE} (Fig. 6-1(c)). Therefore, a careful design on device geometry is necessary to mitigate this short channel effect.

In the following sections, two different approaches are proposed, tested, and discussed: (1) metal membrane process, and (2) e-beam lithography (EBL) alignment combined with tilted metal evaporation.

6.2 Approach I: Metal membrane process

The first approach for integrated anode is the metal membrane fabrication. This type of suspended film through the semiconductor fabrication is known as "surface micromachining" in microelectromechanical systems (MEMS) society. For example, one type of the nano-relays has the suspended metal beam as a channel and actuation electrodes as a gate to control the connection between the metal beam and the electrode for current conduction [185]. When the electric field is applied between the actuation electrodes, the suspended metal beam will be pull down and the beam can touch the conduction terminal to form a current conduction path if the structure is designed properly. Besides the nano-relays, the metal beams are also fabricated for different applications [186–188]. Moreover, some prior work has utilized these fabrication technologies to demonstrate the anode terminal integrated on the Si FEAs with a sealed vacuum cavity; while they are only two-terminal geometries (without gate) and there are no reports on I-V characteristics of Si FEAs in those sealed vacuum cavi-

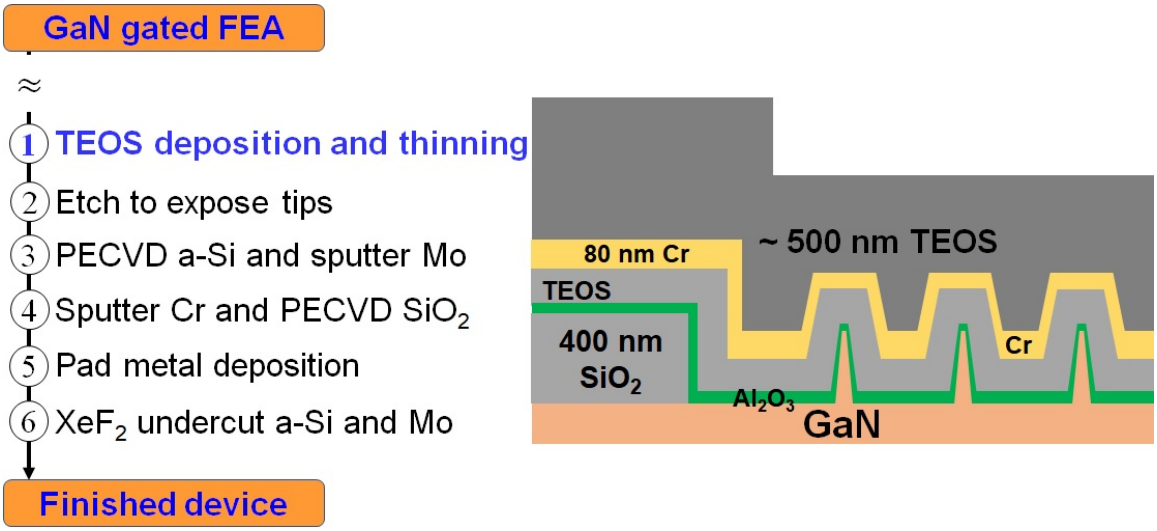


Figure 6-2: The process flow of the suspending anode metal membrane and the cross-sectional device diagram after TEOS deposition and thinning by dry etching.

ties [182,183]. Therefore, the similar idea is applied here to form the integrated anode on our III-Nitride SAGFEAs, aiming to demonstrate the fully-integrated III-Nitride field-emission-based vacuum transistors.

6.2.1 Designed process flow

The designed process flow is shown in Fig. 6-2, and cross-sectional structure diagrams after different steps are shown in Figs. 6-2 to 6-6. As the GaN emitter tip formation and gate stack deposition are similar to the process reported in chapter 4, the description of those steps can be found there.

After the gate stack deposition, a thick ($\sim 1\ \mu$m) TEOS is deposited by PECVD and is then thinned down to about 500-nm thickness by dry etching (Fig. 6-2). This 500-nm TEOS on top of the gate layer will be the insulator between the anode and gate in the finished devices. A Ni layer is then defined by lift-off process and is used as a hard mask for following 500-nm TEOS dry etching, Cr dry etching, and tip exposure. The expected finished structure is shown in Fig. 6-3.

A 500-nm amorphous Si (a-Si) is then deposited by PECVD at $\sim 150^{o}$C, and 50 nm Mo is deposited by sputtering right after the a-Si deposition to protect the a-Si layer from oxidization. Both Mo and a-Si layers are then patterned by dry etching

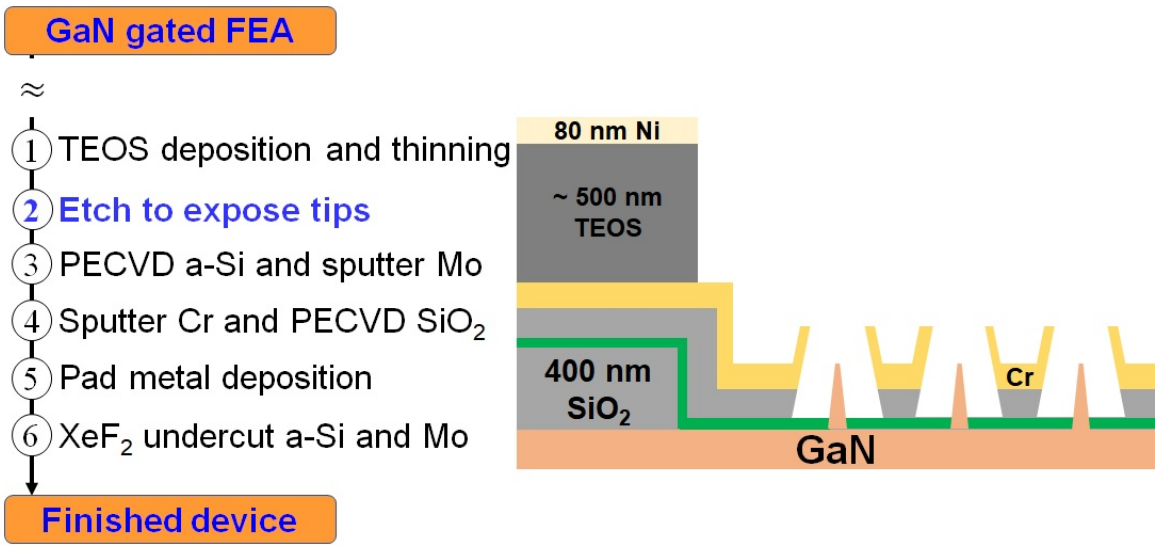


Figure 6-3: The etching step to etch gate metal (Cr) and insulator layers to expose emitter tips. During the etching process, the Ni layer is used to protect the supporting 500-nm TEOS layer, which will be the insulator between gate metal and anode in the finished devices.

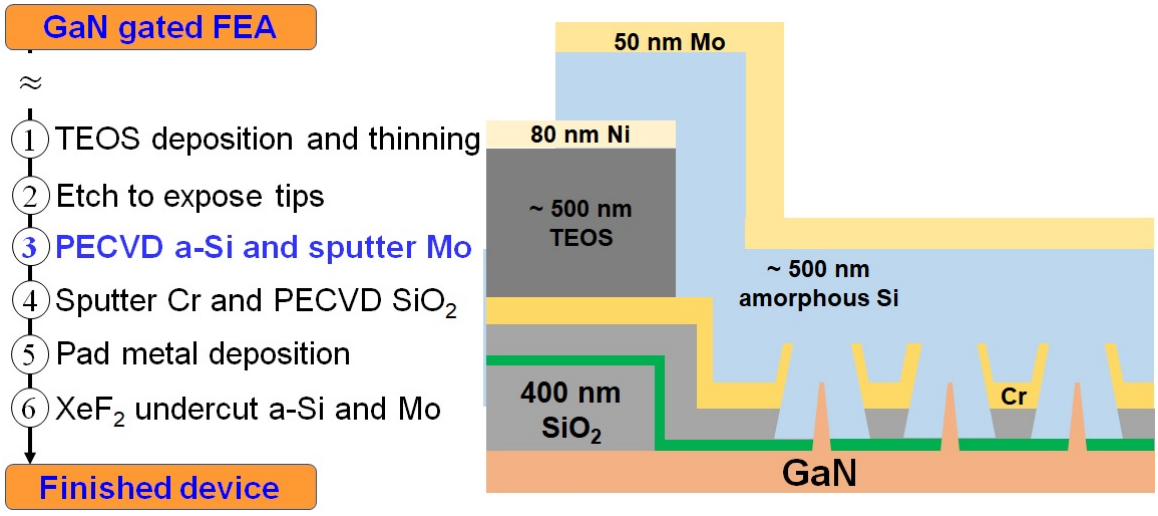


Figure 6-4: PECVD amorphous Si (a-Si) and sputter Mo and dry etching for patterning the region for suspending metal regions. The Mo is sputtered right after the a-Si deposition to protect a-Si layer from oxidization.

(Fig. 6-4). These two layers are sacrificial layers which will be etched away to form the cavity in the last step.

The 100-nm Cr is then sputtered, which will be the anode terminal afterwards. A 500-nm TEOS is then deposited by PECVD on top of the Cr layer (Fig. 6-5), which is used as a etching mask for Cr and a supporting layer for Cr after the removal of

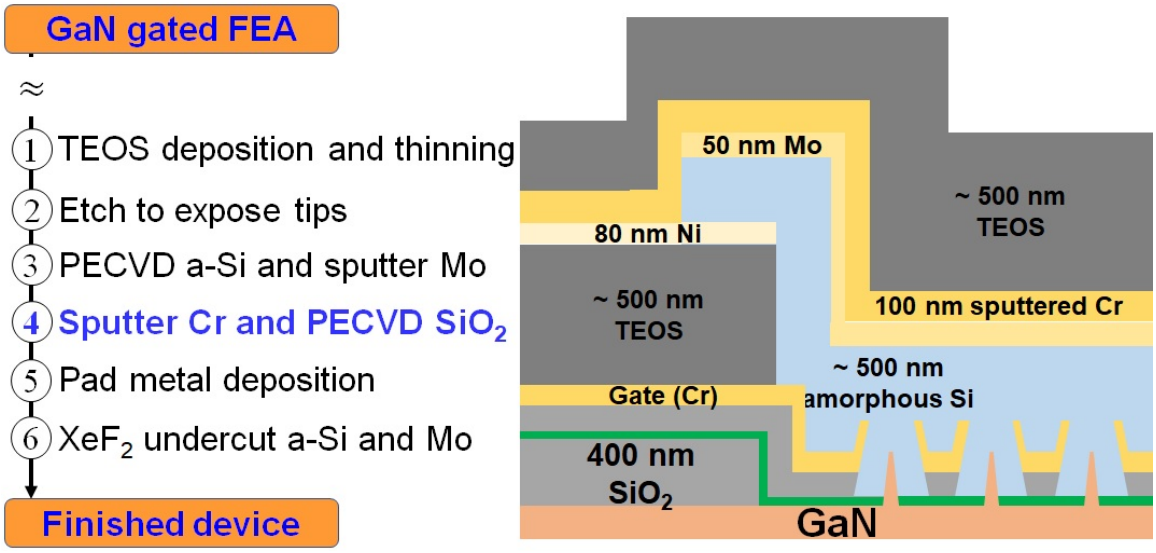


Figure 6-5: The deposition of the suspending anode metal membrane. The 100-nm Cr is firstly deposited by sputtering, followed by PECVD 500-nm TEOS. The 500-nm TEOS is used to help support the Cr metal membrane after a-Si and Mo are removed.

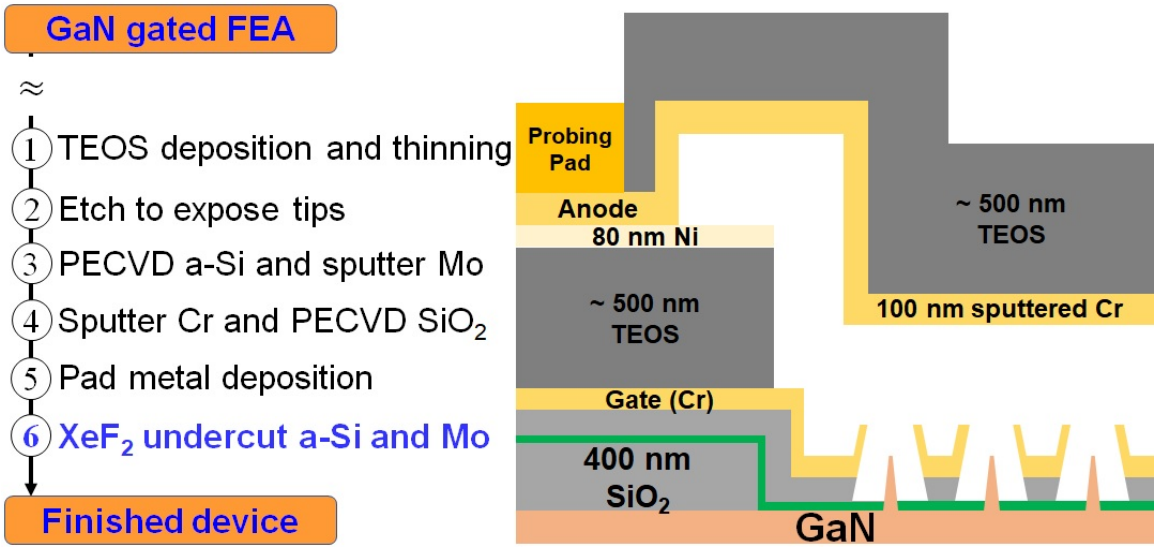


Figure 6-6: The undercut etching of a-Si and Mo to form the suspending anode metal membrane (Cr).

sacrificial layers.

The metal pads on gate and anode terminals, and the metal contact on GaN are deposited. After that, the last step is XeF_2 etching to remove the a-Si and Mo (Fig. 6-6). The XeF_2 etching is a known dry etching process which uses the chemical reaction between XeF_2 (gas) and different materials. It is known that the Si and Mo

will be etched by XeF_2, while XeF_2 cannot etch Cr, SiO_2, and GaN. Additionally, this is a pure dry process, so the common issues during membrane release process, such as pulling force due to the surface tension of water during drying step, can be avoided. This XeF_2 step is the main motivation of applying the metal membrane fabrication to form the integrated anodes on our GaN SAGFEAs.

6.2.2 Experimental results

As the full process of both GaN SAGFEAs and following anode integration will be very complex, to simplify and test the critical steps in the metal membrane process, the Si pieces without any field emitter tips are used to preliminary test the proposed process flow and structures.

The 500-nm TEOS is firstly deposited by PECVD on Si substrate as a protection layer for Si substrate from XeF_2 etching. After that, to mimic the anode shape of the proposed structure (Fig. 6-6), a 500-nm TEOS, which is the insulator between anode and gate in the proposed device structure (Fig. 6-6), is deposited and is dry etched with Ni/Al mask. This 500-nm TEOS insulator is necessary since the non-flat surface for anode metal membrane is one main potential issue of this proposed metal membrane structure and requires testing. The 500-nm a-Si and 50-nm Mo are then deposited by PECVD and sputtering, respectively, and they are dry etched to define the regions of these sacrificial layers.

The anode metal (Cr) and the supporting SiO_2 layer are then deposited by sputtering and PECVD, respectively. The anode membrane and the probing region are then defined by photolithography, as shown in Fig. 6-7(a) and (c). The supporting SiO_2 layer is then dry etched with photoresist mask, which is removed after the etching. The anode metal, Cr, is then dry etched by Cl_2/O_2-based ICP-RIE with SiO_2 mask (Fig. 6-7(b) and (d)).

The sacrificial a-Si and Mo layers are exposed after the Cr dry etching, and they are etched by XeF_2 dry etching to release the suspending Cr anode metal. The finished test structures are then checked by SEM and FIB-SEM (Fig. 6-8 and Fig. 6-9). It is confirmed that the anode metal membrane (arm in Fig. 6-8(a)) still exists

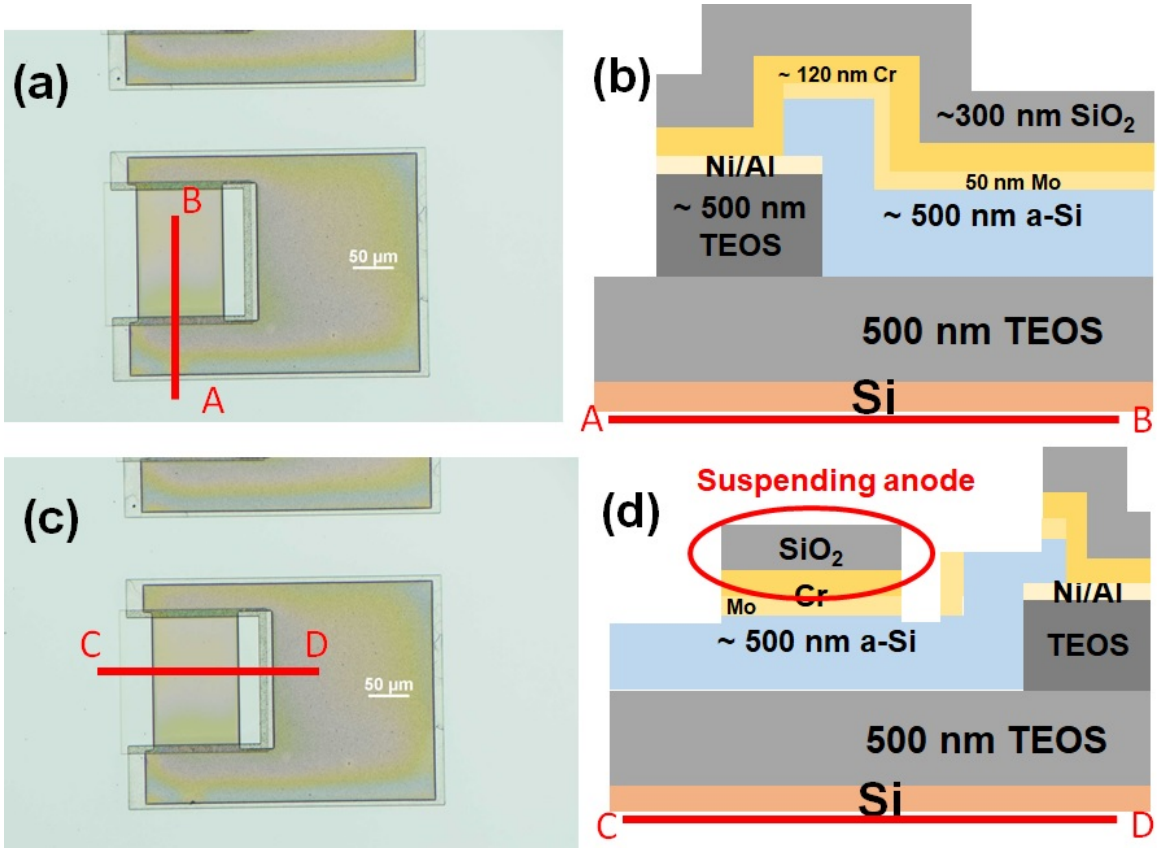


Figure 6-7: The test structures after SiO_2 and Cr dry etching. The patterned regions in (a) and (c) are the photoresist mask for SiO_2 dry etching. The resist is removed afterwards. The cross-sectional diagrams of expected device structures are shown in (b) and (d).

after the XeF_2 undercut etching. However, since the gap between the anode metal membrane and underneath TEOS protection layer (< 1 μm) is much smaller than the width and length of metal membrane (> 100 μm), it is hard to know whether the sacrificial a-Si and Mo layers are fully removed or not by SEM directly (Fig. 6-8(b)). Therefore, the FIB-SEM is then used to check the cross sections of the test structure.

The cross-sectional SEM images obtained by the FIB-SEM system and the corresponding cross-sectional structure diagram are shown in Fig. 6-9. The red and blue circles in Fig. 6-9(a) and (b) represent the corresponding locations in the test structure. There are issues identified by the zoom-in SEM image for the blue-circled region (Fig. 6-9(c)). For example, the residual materials, which are likely Mo and a-Si, are observed in the gap region, and a crack is observed in the Cr metal film.

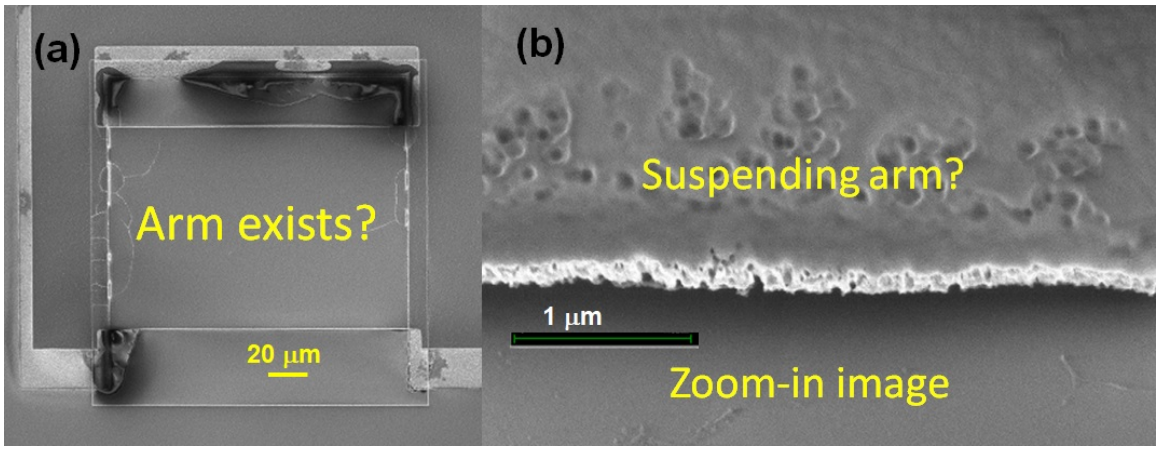


Figure 6-8: The SEM images of test structures after Mo and a-Si undercut etching by XeF_2. The metal membrane still exists, but it is hard to confirm if the a-Si and Mo are fully etched away by SEM only because of the narrow gap ($<$ 600 nm) and the wide arm (width $>$ 100 μm).

Additionally, a significant break in the anode metal (Cr) is observed at the edge of the anode metal membrane on the non-flat surface (Fig. 6-9(d)). This preliminary experiment suggests that the proposed structure and process flow might not work for the anode integration on our GaN SAGFEAs. The modifications on both structures and process flow are still necessary.

6.2.3 Discussion and following directions

The preliminary experiments show that the originally proposed structure does not work due to multiple issues such as residual sacrificial materials and the discontinuity in the anode metal (Cr) film. Hence, the modifications on structures are necessary.

The residual sacrificial materials observed in FIB-SEM are probably resulted from the high width-gap ratio, which is at the level of 100:1 (100 μm : sub-1 μm). The XeF_2 gas is hard to reach the remaining sacrificial a-Si and Mo layers under the anode metal film in the middle area. Furthermore, the reaction of XeF_2 and Si [189],

$$2XeF_2(g) + Si(s) \rightarrow 2Xe(g) + SiF_4(g) \tag{6.2}$$

will increase the pressure during the etching. Since the width-gap ratio is high in the

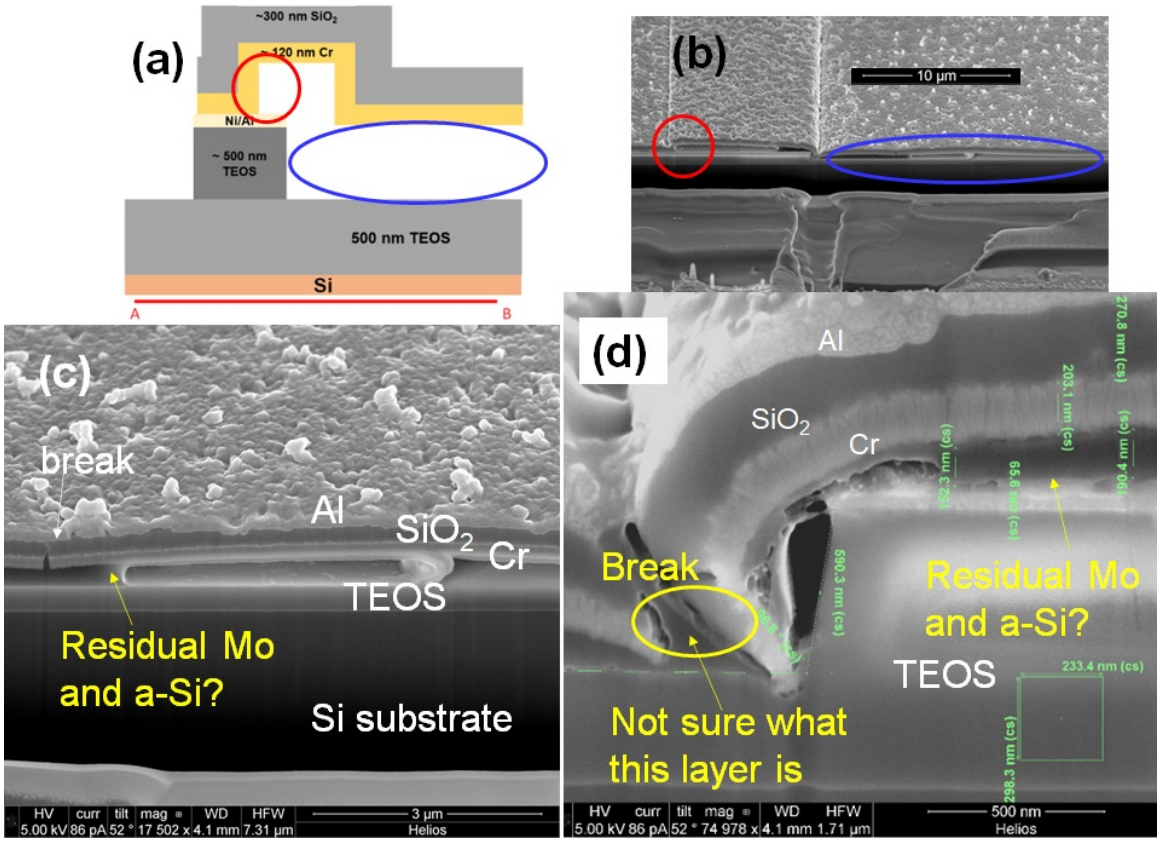


Figure 6-9: The cross-sectional images of test structures are obtained by FIB-SEM. (a) The structure diagram and (b) cross-sectional SEM image of the test structure. The SEM images of (c) suspending metal membrane region and (d) supporting region. The red and blue circles in (a) and (b) indicate the similar regions in diagram and SEM image. There are residual Mo and a-Si, and the crack in the Cr layer, observed in the suspending metal membrane region (shown in (c)). Additionally, the supporting region shows clear discontinuity in the Cr layer (shown in (d)).

proposed structure, the local pressure where the etching happens could increase and induce additional force to break the anode metal film before the gas dissipates away (Fig. 6-9(c)). The change of design, for example, replace the one wide metal arm by multiple metal arms with gap between them, might be able to solve this potential issue.

On the other hand, the non-flat surface with multiple height-changing edges causes additional challenge for supporting the suspending metal beam. The sub-1 μm gap is also hard to keep along the long distance (> 100 μm) with the a thin anode metal and SiO_2 ($\sim$ 120 nm Cr and $\sim$ 500 nm SiO_2) [190]. To support the suspending arm

with long distance and a narrow gap, the thickness of the arm should be significantly increased ($> 10\ \mu$m). Additionally, the electrostatic pull-down due to the bias voltages applied during the device operation can potentially pull the anode metal down to touch the device and cause failure during the operation of these vacuum transistors [190]. As a results, the increase of gap size between the anode metal arm and the underneath device might be necessary.

An anode metal formed by the combination of photoresist and thick metal layer has been demonstrated for two-terminal III-Nitride field emission devices [26]. Therefore, the modified device structure and corresponding process flow is proposed based on those prior demonstrations (Fig. 6-10). Since the photoresist residual can remain on GaN and gate metal surface, leading to contamination issues and performance degradation, the a-Si and sputtered Mo layers are still used on top of the GaN SAGFEAs. After defining these sacrificial layers by dry etching, a thick resist is then patterned by photolithography (Fig. 6-10(a) and (b)). The thick photoresist can increase the gap size without a time-consuming thick a-Si deposition, and it can also help planarize the non-flat surface (Fig. 6-10(b)). A thing Cr layer is then sputtered, and a thick metal is deposited and defined by the lift-off process. In literature, the thickness of this anode metal bridge is at the order of μm, so the electroplating process or thick metal evaporation might be necessary. After that, the sputtered Cr is etched away to disconnect the anode metal from gate and source terminals, and to expose the thick resist underneath the anode metal (Fig. 6-10(c) and (d)). The thick resist can then be removed by organic and dried by a critical point dryer. The sacrificial a-Si and Mo layers can then be etched away by XeF_2 to finish the device (Fig. 6-10(e) and(f)). Since now there is plenty space for gas expansion during the XeF_2 etching, the concern about the increase of pressure, which can push and break the anode metal membrane, can be relieved. However, this new proposed structure requires thick metal bridge, the gap size between anode and GaN SAGFEA will be at least few μm, and the vacuum sealing will require additional process after the XeF_2 etching. These modified proposed process flow and structures are not experimentally tested yet, and there is still work to be done in the future.

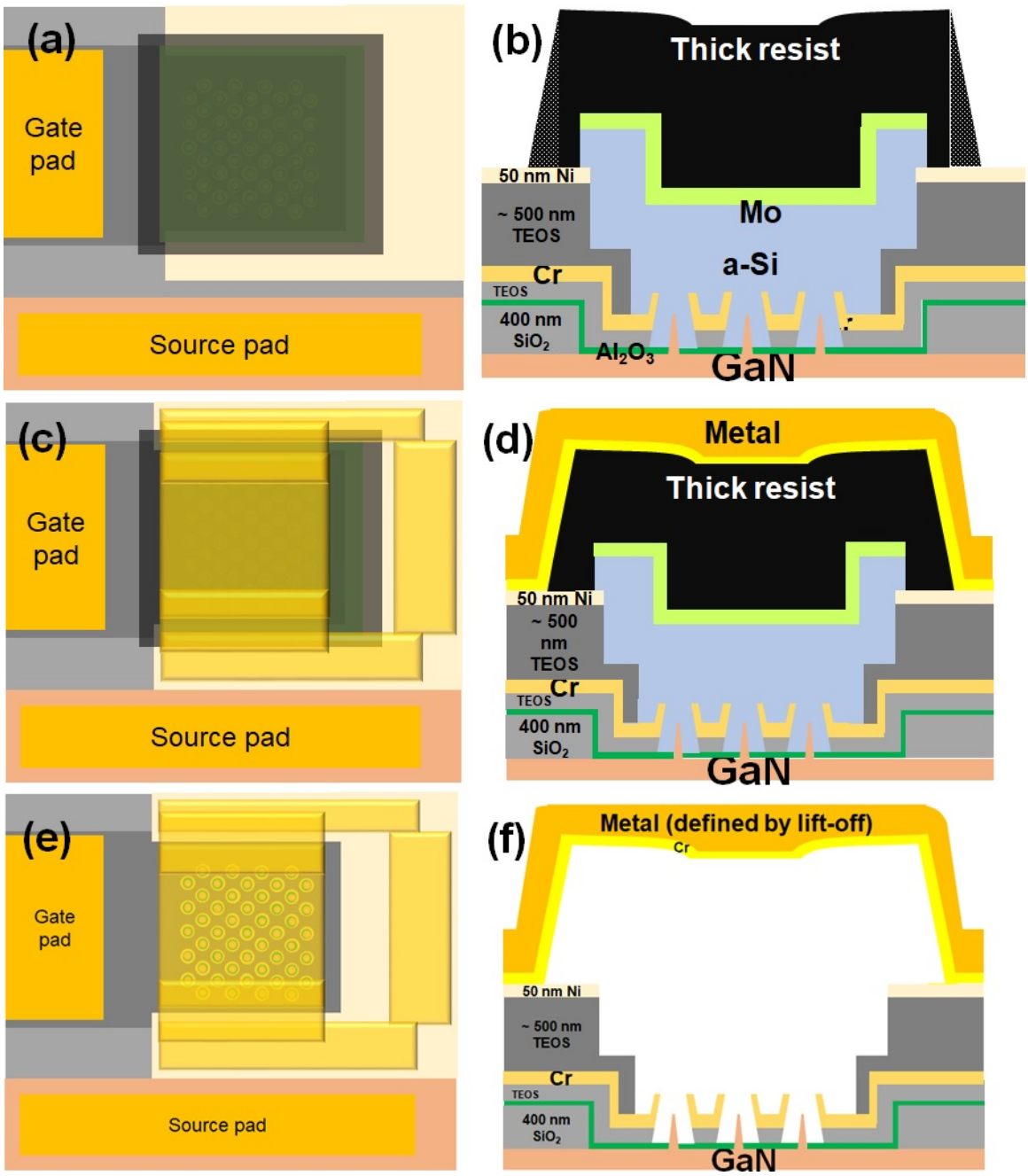


Figure 6-10: The proposed modified structures for suspending metal membrane with thick resist. (a) (c) (e) The top-view illustration and (b) (d) (f) the corresponding cross-sectional structure diagrams after different process steps. (a) (b) the thick resist (> 5 μm) is patterned on sacrificial Mo and a-Si layers. (c) (d) The thick anode metal is then deposited on thick resist. (e) (f) The thick resist is removed by acetone and the critical-point dryer, and the sacrificial Mo and a-Si are etched away by XeF_2.

6.3 Approach II: EBL alignment and tilted metal evaporation

As the metal membrane approach requires a thick metal beam and a larger gap because of the long distance of suspended anode metal, adding supporting dielectric pillars is a reasonable solution to help support the anode metal membrane. However, if the same approach of metal membrane is still used, the device structure requires redesign and the density of the field emitter tips is expected to be reduced to provide additional area for supporting dielectric pillars. On the other hand, if the better lithography alignment can be achieved, for example, sub-100-nm misalignment, the formation of local dielectric pillars is possible. Therefore, the 2nd approach, which combines the e-beam lithography (EBL) alignment with the tilted metal deposition process is proposed and tested.

6.3.1 Designed process flow

The process flow of this EBL alignment and tilted metal deposition approach is shown in Fig. 6-11, and the cross-sectional structure diagrams after different steps are shown in Figs. 6-11 to 6-14. The detailed process flow and the lithography patterns are summarized in Appendix G.

The GaN field emitter tips are formed and the gate stack (Cr and TEOS) is deposited. After that, the thick TEOS ($\sim$ 1000 nm) is deposited by PECVD, and the Ni hard mask is defined by EBL with PMMA lift-off (Fig. 6-11). This EBL requires an alignment to make sure that the Ni mask lines are on top of the middle region of the adjacent emitter tips. The misalignment below 100 nm is critical and is practical for the EBL tool. The pitch and space of these Ni metal lines are designed corresponding to the design of the FEAs.

After the lift-off process, the TEOS is firstly dry etched by CF_4/H_2-based ICP-RIE (Recipe: SiO2-PC in Mixed-SAMCO) for about 800 nm with vertical sidewalls, and the remaining $\sim$ 300-nm TEOS is then dry etched with a slow etching recipe

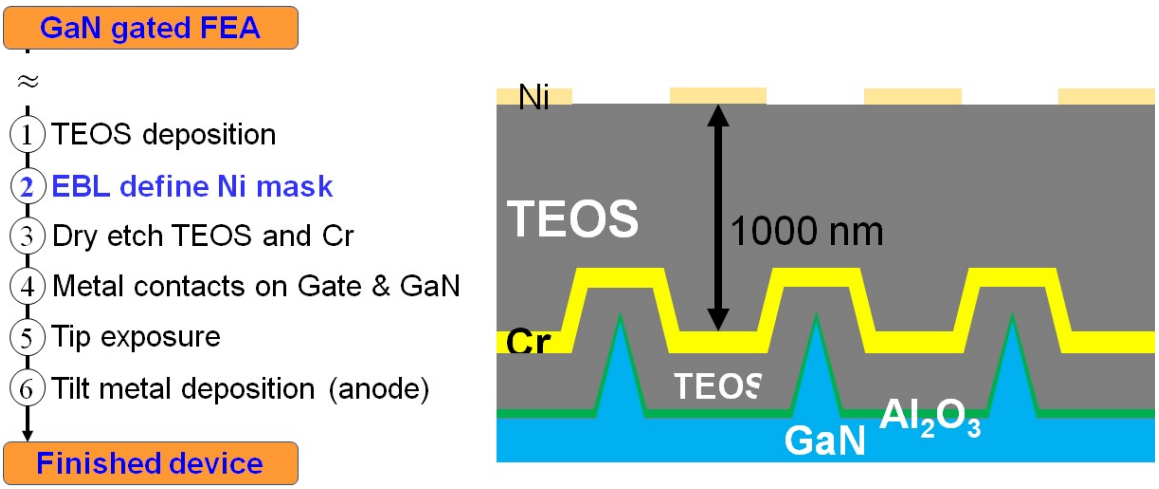


Figure 6-11: The process flow of the e-beam lithography (EBL) and tilted metal deposition and the cross-sectional device diagram after Ni mask defined by EBL with PMMA lift-off. The EBL with sub-50-nm misalignment is necessary.

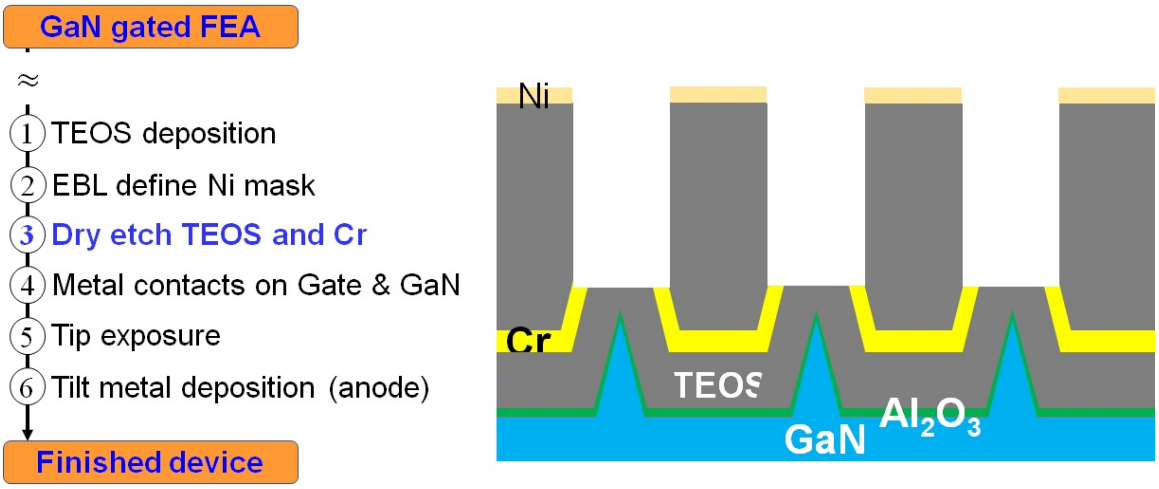


Figure 6-12: The TEOS and Cr are dry etched with Ni hard mask. The TEOS pillars formed by dry etching will be the supporting dielectric between anode and gate, and will also be the shadow masks for adjacent TEOS pillars during the tilted anode metal evaporation.

(Recipe: SiO2-SEL in Mixed-SAMCO) (Appendix D). The Cr is then dry etched by Cl_2/O_2 ICP-RIE, and the expected structure after these etching steps is shown in Fig. 6-12.

The metal contacts on gate and GaN are then deposited respectively, and the thick resist is used to protect all these metal layers. The TEOS layer on the GaN emitter tips are then dry etched, and the 10-nm Al_2O_3 is then etched away by the

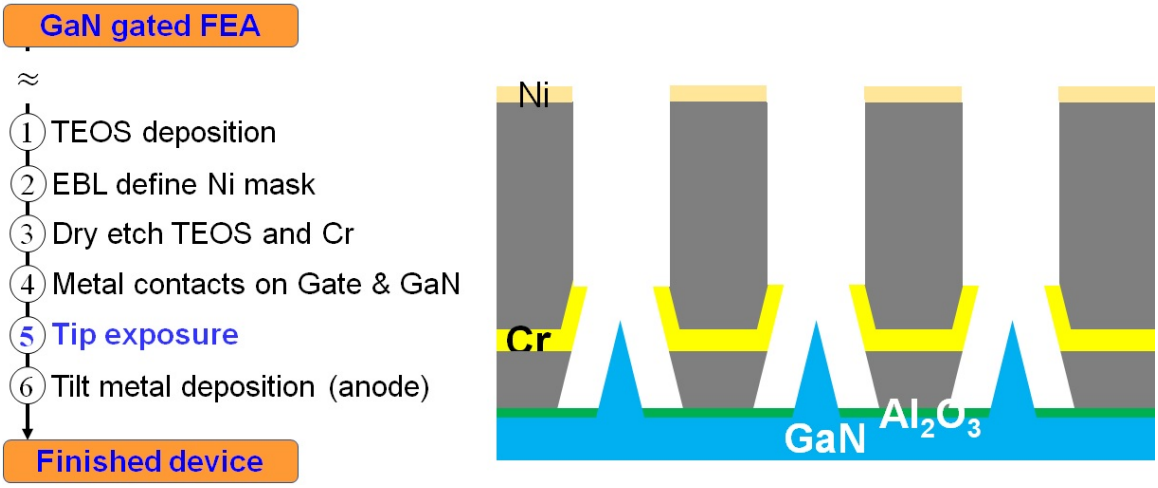


Figure 6-13: The GaN emitter tips are exposed by dry etching gate insulator (TEOS) and by wet etching Al_2O_3.

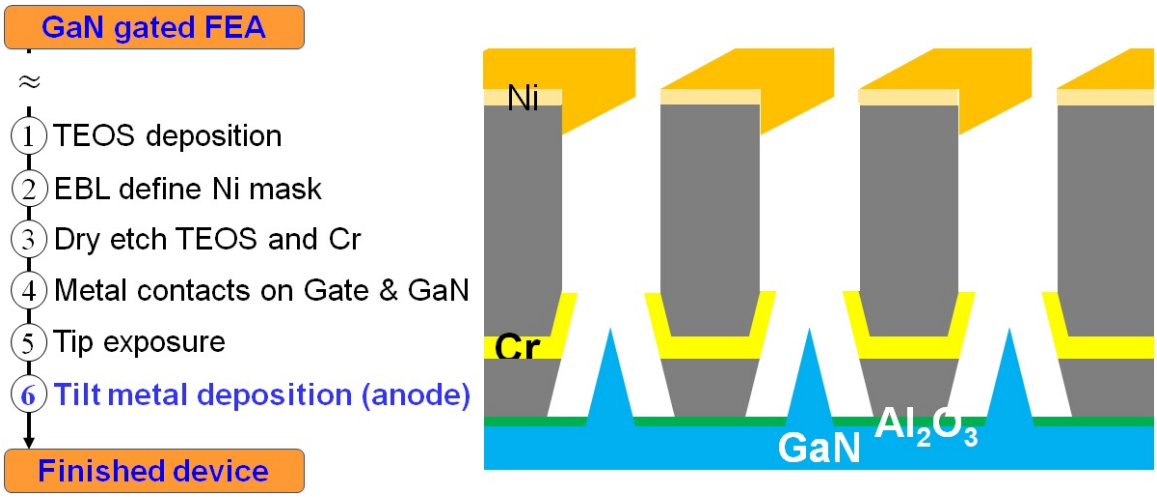


Figure 6-14: The anode metal is deposited with a tilted angle by e-beam evaporation. If the deposited metal is thick enough, the vacuum cavity between anode metal and GaN tips can potentially be in-situ packaged during the e-beam evaporation.

TMAH-based developer (Fig. 6-13). At this point, the TEOS pillars under the Ni mask are the supporting dielectrics for the anode metal, which will be deposited in the following step.

After the tip exposure step, the thick resist is not removed, and the anode metal evaporation is conducted with a tilting angle. For example, the orange regions shown in Fig. 6-14 are the anode metal deposited with a 70-degree tilt angle. The high TEOS pillars are both supporting the anode metal and used as shadow masks for the

metal deposition. The evaporated metal thickness, tilt angle, and the space between of Ni mask defined by EBL will determine whether the vacuum cavity is fully sealed during the metal evaporation. If the evaporated metal is thick enough, the vacuum cavity between the emitter tip and the anode metal can be directly closed during the anode metal deposition, so the vacuum channel can be packaged at high vacuum or even ultra high vacuum (UHV) conditions.

After the anode metal deposition, the thick resist is then removed by organics and the unwanted metal films on the thick resist are lifted off at the same time. After this, the GaN field-emission-based vacuum transistors with integrated anodes are fabricated (Fig. 6-14). The vacuum channel length can be engineered by multiple parameters, such as TEOS pillar height, Ni hard mask pattern, and the tilt angle of anode metal deposition. In principle, the sub-μm vacuum channel length can be obtained, and the device structure is believed to be very stable compared to the structure formed by the metal membrane approach (section 6.2). The tilted metal deposition step is a well-known technique for the fabrication of some devices, such as Spindt-type Mo FEAs [34]. The initial idea of this tilted-metal deposition approach is generated and finalized during and after the discussion with Joshua Perozek in Tomás Palacios group.

6.3.2 Experimental results

Since the proposed process flow of the fully-integrated vacuum transistors requires many process steps, a simplified structure is tested in the preliminary experiments to check the critical steps of this EBL alignment and tilted metal deposition approach.

A sample with GaN tips and the protecting 10-nm Al_2O_3 is prepared for this preliminary experiment. As the tool for TEOS deposition had been not available for a while during this experiment development, instead of TEOS, the $\sim$ 1060-nm silane-based SiO_2 is deposited by another PECVD system. The Ti/Ni lines are then defined by EBL with PMMA lift-off with sub-100-nm misalignment (Fig. 6-15(a)-(c)). The trenches existing in the SiO_2 layer are in the middle region of adjacent emitter tips and are observed in SEM. The bumps on the emitter tips are also observed, while the

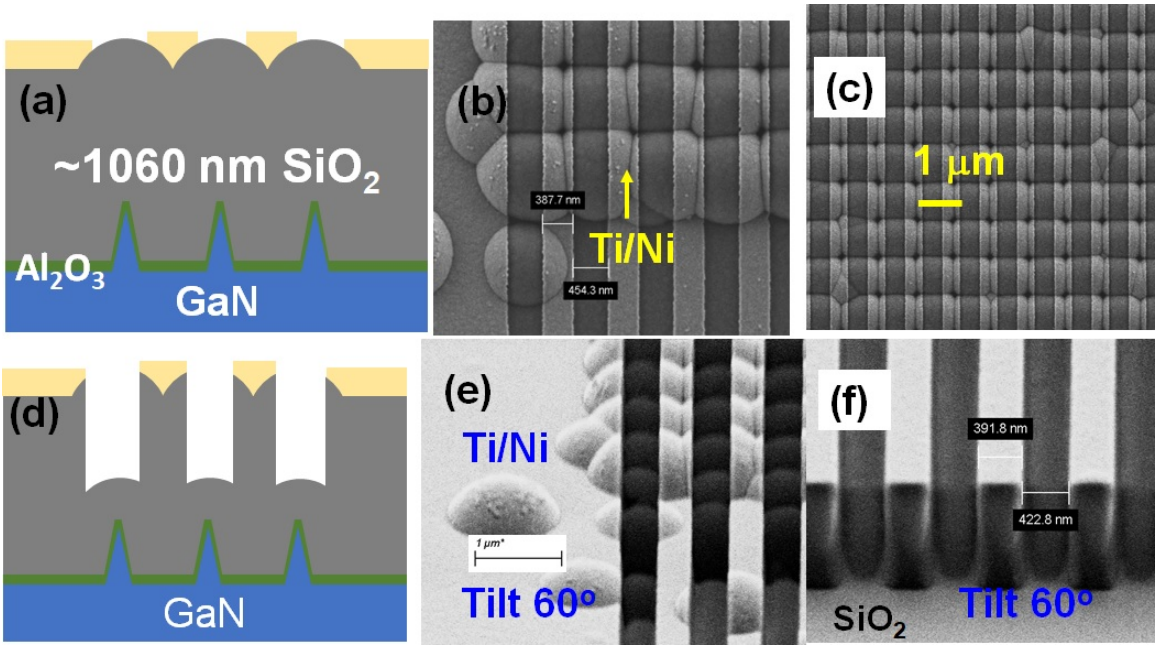


Figure 6-15: The test structures of EBL and tilted metal deposition process (a) (b) (c) after Ni hard mask lift-off defined by EBL on PMMA and (d) (e) (f) after $\sim$ 730 nm SiO_2 dry etching. The structure diagrams are shown in (a) and (d). The Ti/Ni lines defined by EBL are aligned in the middle of the adjacent tips. The (e) (f) tilted SEM images of the structure after SiO_2 dry etching show that the vertical sidewalls of SiO_2 pillars are obtained. Since the etching depth of SiO_2 is only about 730 nm, the GaN tips are not exposed yet (as shown in (e)).

Ti/Ni metal lines are still successfully formed after PMMA lift-off (Fig. 6-15(b) and (c)). It should be noted that the alignment marks for this EBL step are the crosses of GaN mesa with $\sim$ 300-nm height difference, which were defined during the prior EBL step for GaN FEA definition.

After the Ti/Ni mask formation, SiO_2 dry etching for $\sim$ 730-nm etching depth is conducted (recipe: SiO2-PC in Mixed SAMCO, Appendix D) (Fig. 6-15(d)-(f)). This etching step is conducted on a 6-inch Si wafer carrier with a vacuum oil, Santovac, for improved thermal conduction between the backside cooling and the sample. The etching results are confirmed by the SEM, and the vertical sidewalls are observed (Fig. 6-15(e) and (f)). The SiO_2 bumps still exist in the trenches since the 730-nm etching depth does not fully remove SiO_2 layer on GaN tips.

The thick resist (AZ-10xT 520cP) is then patterned to define the region for tilted anode metal deposition, and another SiO_2 dry etching for $\sim$ 390-nm depth is con-

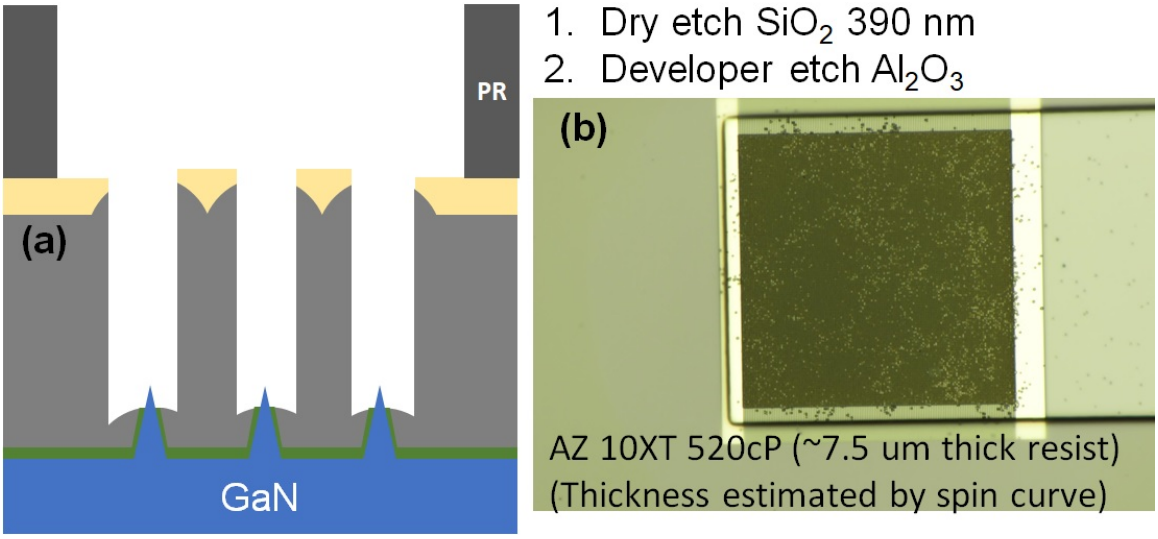


Figure 6-16: The thick resist ($\sim$ 7.5 μm thickness) is patterned by lithography and used as a etching masks for following 390-nm SiO_2 dry etching and wet etching Al_2O_3 by a TMAH-based developer. The dry etching step here uses a recipe with a slower etching rate and lower plasma power to reduce the potential damages on GaN tips. The optical microscope image of a device is shown in (b).

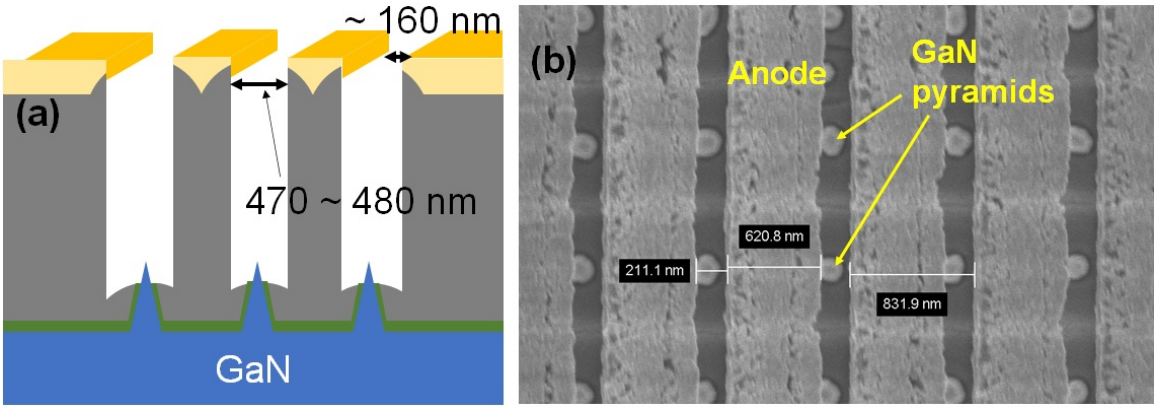


Figure 6-17: The finished structure after the tilted metal deposition. The metal stack (20 nm Ti/200 nm Al/20 nm Ti/100 nm Au) is deposited with a 70-degree tilting angle. (b) The SEM image of a finished structure shows that the anode metal deposited by tilted deposition can close the gaps between SiO_2 pillars.

ducted (recipe: SiO2-SEL in Mixed-SAMCO). After that, the TMAH-based developer is then used to etch the Al_2O_3 to expose GaN tips (Fig. 6-16(a)). The FEA regions are exposed and the surrounding area is protected by the thick resist (Fig. 6-16(b)).

A thick anode metal is then deposited by 70-degree-tilted e-beam metal evaporation. The metal stack of 20 nm Ti / 200 nm Al / 20 nm Ti / 100 nm Au is

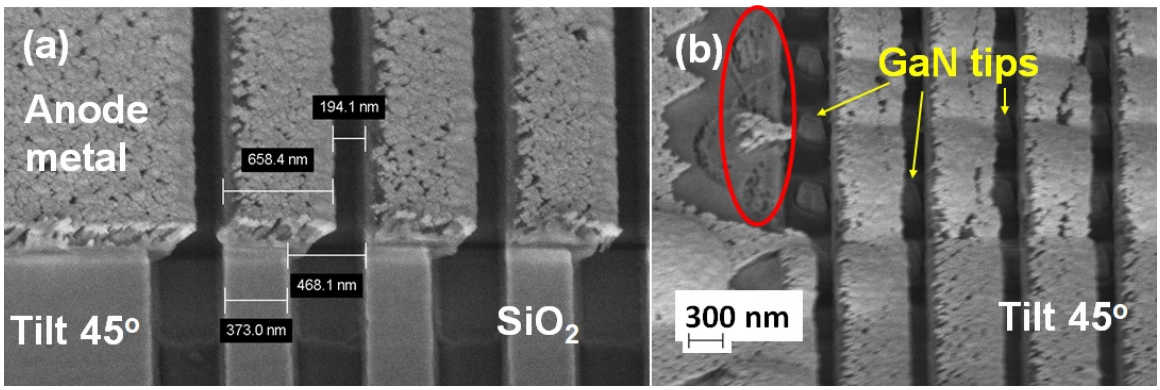


Figure 6-18: The 45-degree tilted SEM images of (a) the structure without GaN tips underneath and (b) the structure with GaN tips. Bumps in SiO_2 pillars due to the non-flat underneath GaN surface are observed in (b). Therefore, the planarized dielectric surface, such as planar surface by TEOS deposition, will still be better than the surface formed by PECVD Silane-based SiO_2.

deposited, and the lift-off process is done with n-methyl-2-pyrrolidone (NMP) with a few-minute ultrasonic bath. The expected cross-sectional diagram of the finished structure is shown in Fig. 6-17(a). To be able to check the test structure after tilted metal deposition by SEM, the thickness of evaporated metal stack is chosen to keep a gap between adjacent anode metal lines. The test structure is then characterized by SEM (Figs. 6-17(b), 6-18 and 6-19). The top-down SEM image of the test structure shows that the GaN emitter pyramids are not covered by the anode metal (Fig. 6-17(b)).

The 45-degree tilted SEM images of the test structures without and with GaN emitter tips are shown in Fig. 6-18. The surface of SiO_2 pillars of the structure without GaN emitter tips are very flat and uniform since there is no height difference (Fig. 6-18(a)), and this test structure confirms that the proposed structure works if the SiO_2 pillars' surface is planarized. On the other hand, bumps are observed on SiO_2 pillars in the region with GaN emitter tips due to the non-flat surface before the SiO_2 deposition (Fig. 6-18(b)). Most of the anode metal lines are still formed successfully, while the bumps and height difference can cause local shadowing during the tilted metal deposition, as shown in the red-circled region in Fig. 6-18(b). Therefore, though the silane-based SiO_2 can still be used as the supporting pillars in this process, the

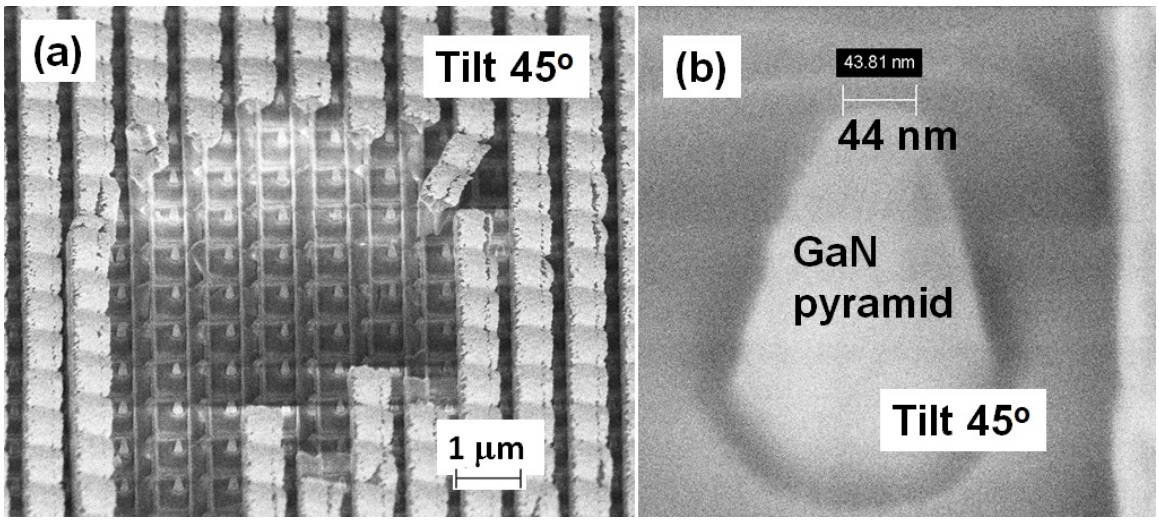


Figure 6-19: The tilted SEM images of (a) a failed region and (b) a GaN emitter pyramid in this failed region. As the tips are not coated with metal, the damage on SiO_2 pillars is most likely generated during the cleaning procedure after tilted metal deposition. The GaN emitter pyramids are designed to have tip width of 40 - 45 nm, so the GaN tips are still pristine after a long process flow with different steps.

TEOS with planarized surface might still be better than SiO_2 since the potential issues of these bumps due to non-flat emitter tip surface can be mitigated.

Different regions of the test sample are also checked, and some failures are observed (Fig. 6-19(a)). As the ultrasonic bath is used to help lift-off the anode metal after tilted metal deposition, some regions of the SiO_2 pillars seem broken and the GaN emitter tips in those regions can be observed by SEM. This failure most likely happens during the lift-off process, since the GaN emitter tips in those failed regions are not coated with anode metal. Additionally, there is a misplaced SiO2 pillar with the anode metal on it (right region in Fig. 6-19(a)). This failure might be resulted from the trenches or voids existing in the SiO_2 film, which leads to the weaker mechanical strength in these SiO_2 pillars. Though this failure indicates that the lift-off step requires additional carefulness, these failed regions also provide good spots to confirm if the GaN emitter tips are exposed and are not damaged by the tip exposure step (Fig. 6-19(b)). The GaN pyramids are designed to have tip width of 40-45 nm, and they are not sharpened by DE process in this test sample. Therefore, the tip exposure process combined with the SiO_2 pillars still works and does not damage the

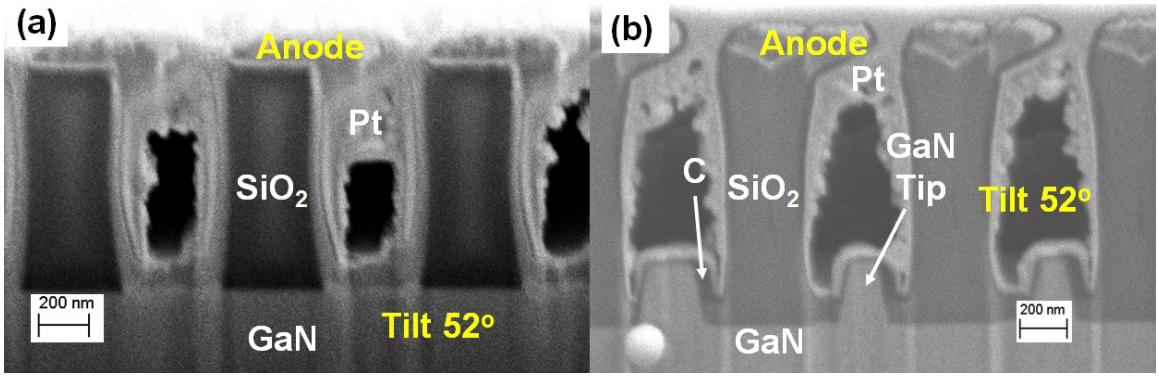


Figure 6-20: Cross-sectional SEM images of the test structures (a) without GaN emitter tips and (b) with GaN emitter tips. The cross sections are obtained by a FIB system using Ga ion beam. The Pt is deposited in (a), and the C and Pt are deposited in (b) before the FIB cutting, respectively, to protect structures.

GaN emitter tips.

The cross sections of test structures are prepared by FIB cutting using the Ga ion beam and are checked by the SEM (Fig. 6-20). The carbon (C) and Pt are deposited in the FIB-SEM system before the FIB cutting to protect the structures during the Ga ion-beam milling. The shape of anode metal formed by tilted metal deposition is similar to the design (Fig. 6-17(a)). Since the anode close more than the half of the gap between SiO_2 pillars, the C and Pt cannot easily fill the whole cavity between anode and GaN emitter tips (Fig. 6-20(b)). The tip size observed in (b) might not be correct since the FIB cutting is very likely not right at the emitter tips' position. When comparing the anode metal in both Fig. 6-20(a) and (b), the non-flat surface of SiO_2 pillars also shows a potential issue of discontinued anode metal (Fig. 6-20(b)). Planarized dielectric pillars using PECVD TEOS in the future might be able to eliminate this potential issue.

After the preliminary test, the anode integration process is then conducted on GaN SAGFEAs to form fully-integrated vacuum transistors (Fig. 6-21). The SEM images of different critical steps confirm that the proposed approach works. With thick TEOS layer ($\sim 1\ \mu m$), the oxide pillars have more flat and smooth surface, and thus the following anode metal deposition has much better coverage and the gap is almost closed by 400-nm-thick metal deposition. The TEOS layer is deposited by

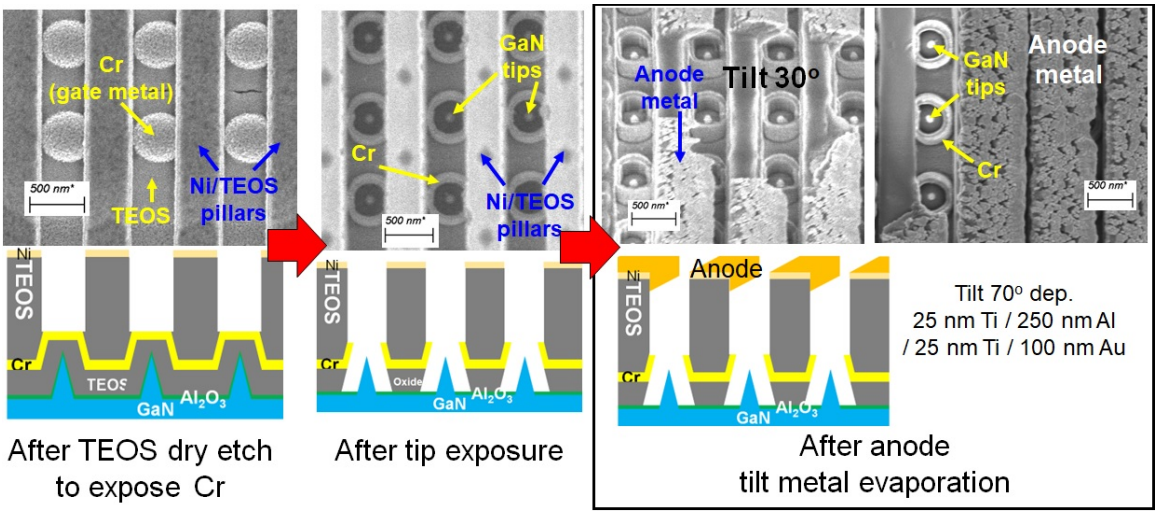


Figure 6-21: The experiments to fabricate fully-integrated GaN field-emission vacuum transistors. The proposed process flow is demonstrated and confirmed by the SEM images of different critical steps. There are some regions with broken anode after anode metal evaporation and lift-off process, which needs further optimization on process steps.

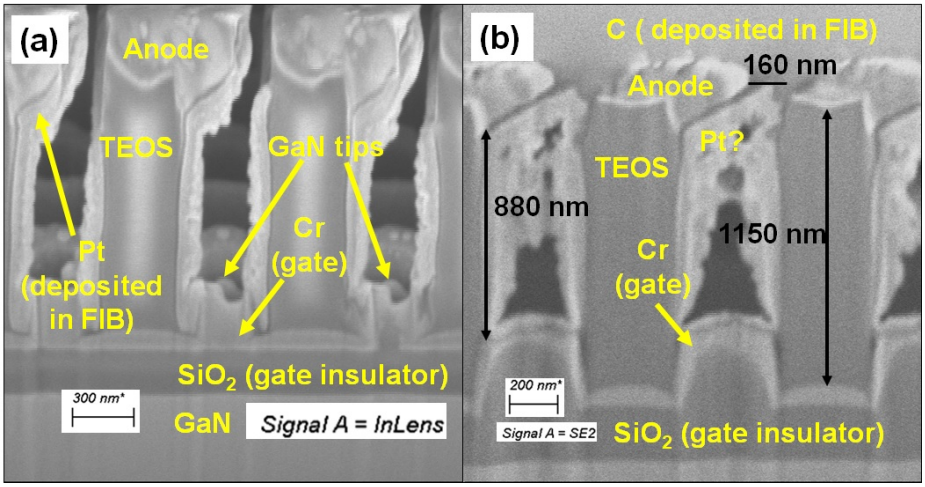


Figure 6-22: Cross-sectional SEM images of fabricated fully-integrated GaN field-emission-based vacuum transistors. These cross sections are obtained by a Ga focus ion beam (FIB) system. The (a) Pt and (b) carbon (C) are deposited by FIB before the milling to protect the structure. The Pt on the sidewalls is likely to be sputtered from the cut region during the FIB milling. The cross sections prove that the preliminary proposed process and structure work as expected.

PECVD through the help from Applied Materials (AMAT).

The cross-sectional SEM images confirm that the proposed process flow and designed structure work as expected (Fig. 6-22). Additional metal on the sidewalls of

TEOS pillars is likely the metal which is sputtered by Ga ions and redeposits on the sidewalls during the FIB milling process. Despite the artifacts of these metal-coated sidewalls, the C-protected structure shown in Fig. 6-22(b) confirms that the overall cross-sectional structure matches our design.

6.3.3 Preliminary device measurement results

After the device structure of these preliminary experiments is confirmed by cross-sectional SEM images, the sample is loaded into the UHV measurement chamber to characterize these devices. Since the gaps between anode and gate are not fully sealed by the anode metal in this preliminary experiment (Figs. 6-21 and 6-22), the sample is still loaded into the UHV system to ensure the vacuum level in the devices.

The transfer characteristics of an anode-integrated GaN SAGFEA are plotted in Fig. 6-23. It is observed that the emitted electrons from emitters will all go to the gate if the anode voltage is lower than the gate voltage, that is, $V_{AG} < 0$ V. Therefore, in these measurements, instead of anode voltage, the anode-gate voltage (V_{AG}) is fixed at a constant voltage. As mentioned in Appendix E, we use multiple I-V sweeps to condition the device. The anode current starts increasing from the noise level when V_{GE} increases above 50 V (Fig. 6-23(a)), but the anode-gate leakage path suddenly forms and the transistor operation fails (Fig. 6-23(b)). The chamber pressure, which is monitored by an ion gauge, does not increase when this leakage-path formation happens. More investigation on this leakage path formation is still necessary.

Though the anode-gate leakage path formation causes the device failure, we can still characterize the device behavior before this failure happens. The transfer characteristics and corresponding F-N plot before the anode-gate leakage happens are plotted in Fig. 6-24. Before the leakage path generation, both the gate current (I_G) and anode current (I_A) are positive, and $|I_E| = |I_G| + |I_A|$ when the current is above the noise level. The gate current is still one-order-of-magnitude lower than the anode current at high V_{GE}. Moreover, the anode current in the F-N plot shows a negative-slope straight line region (Fig. 6-24(b)), indicating that the field emission is the main current conduction mechanism before the anode-gate leakage path formation. The

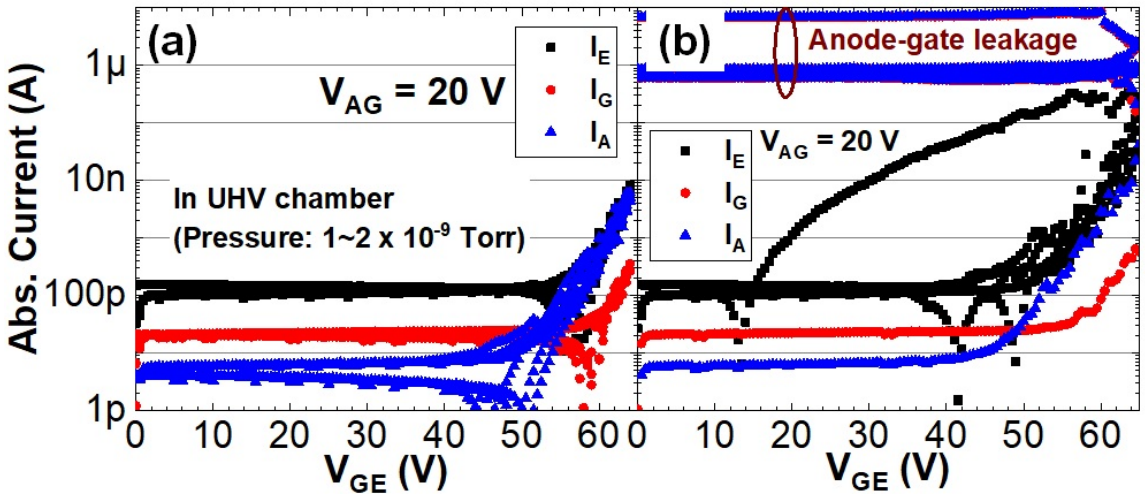


Figure 6-23: The transfer characteristics of a fully-integrated GaN field-emission vacuum transistors (with 150 × 150 tips) during the I-V sweep conditioning step (as described in Appendix E). The anode-gate voltage (V_{AG}) is fixed at 20 V to make sure most emitted electrons are collected by anode. During the I-V sweep, the anode-gate leakage path suddenly forms and leads to failure of the transistor operation.

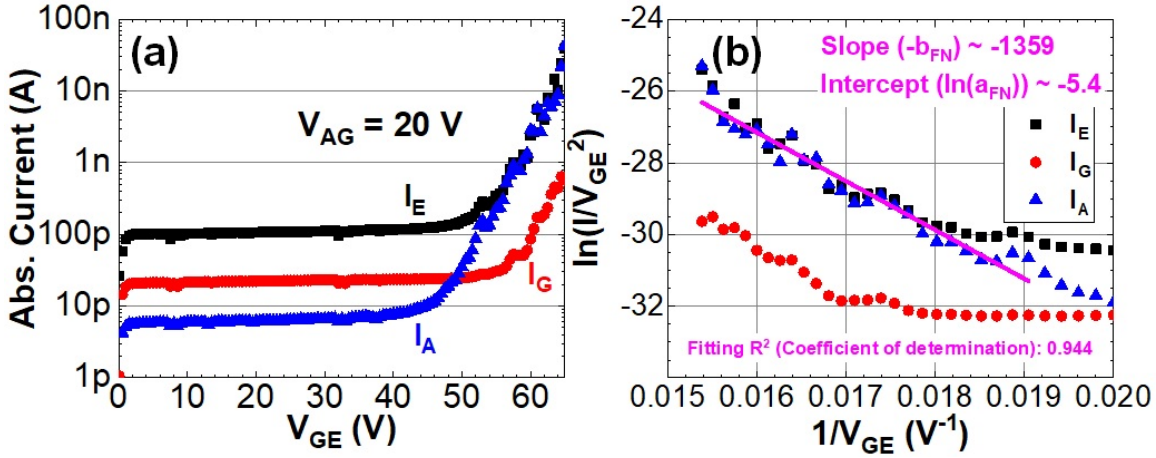


Figure 6-24: The (a) transfer characteristics and (b) corresponding F-N plot of the measured device right before the formation of anode-gate leakage path (Fig. 6-23(b)). The F-N plot shows that the anode current is still dominated by field emission, which is mainly controlled by V_{GE}. However, the large b_{FN} indicates that the device might not be fully conditioned yet and the tip surface might still have some absorbates or a thin surface oxide layer.

anode current data is found still noisy in F-N plot, and the F-N slope ($-b_{FN}$) is about -1359 V, which is much steeper than the GaN SAGFEAs we showed in Chapter 3 and Chapter 4. Therefore, it is very likely that there are still absorbates or thin oxide layer

on the emitter tip surface that affect the electron emission property. More work to be done in the future to understand the conditioning mechanism of these III-Nitride field emission devices.

As the anode-gate leakage path formation is one big issue of these preliminary devices, another measurement is conducted on another device to monitor the occurrence of this leakage path. The bias voltages are fixed (V_{GE} = 60 V and V_{AG} = 10 V), and the current and chamber pressure are measured with a period of 1 sec in this measurement (Fig. 6-25). The 10 min DC operation measurement shows that the chamber pressure is stable, while there are a few jumps in current of different terminals (Fig. 6-25(a)). Furthermore, an abrupt sign change of the gate current is observed at the 2nd current jump, which is zoomed in and shown in Fig. 6-25(b). When the anode current jumps to 10s or 100 nA, the gate current then flips the sign from positive to negative, and the anode-gate leakage path forms. As there is no pressure change and the device is not fully broken, this anode-gate leakage might not be resulted from the arcing, which could be more catastrophic to the device. On the other hand, the leakage path might generate from the re-deposition of the materials which desorb from the emitter surface during the measurement, or from the additional leakage path through the dielectric layer between the anode and gate metal. However, more investigation is needed in the future to draw any meaningful conclusion on this leakage issue.

After the 10-min DC operation test (Fig. 6-25), the device is further characterized by a long DC test ($\sim$ 8000 secs) at a fixed bias condition (V_{GE} = 62 V and V_{AG} = 30 V) (Fig. 6-26). As the V_{AG} bias is high, the anode-gate leakage is at 10s to 100 μA level (Fig. 6-26(a)). This leakage current increases in the first half hour and then stabilizes at about 130 μA, and there is no jump in chamber pressure. The emitter current is negative with the magnitude of 1-2 μA (Fig. 6-26(b)).

After the DC operation test, the transfer characteristics of this device are measured again (Fig. 6-27). As the anode-gate leakage path formed, the V_{AG} is set to be only 0.2 V to reduce the leakage current and to check if the emission current can still be observed in anode current. The anode current starts increasing from the anode-gate

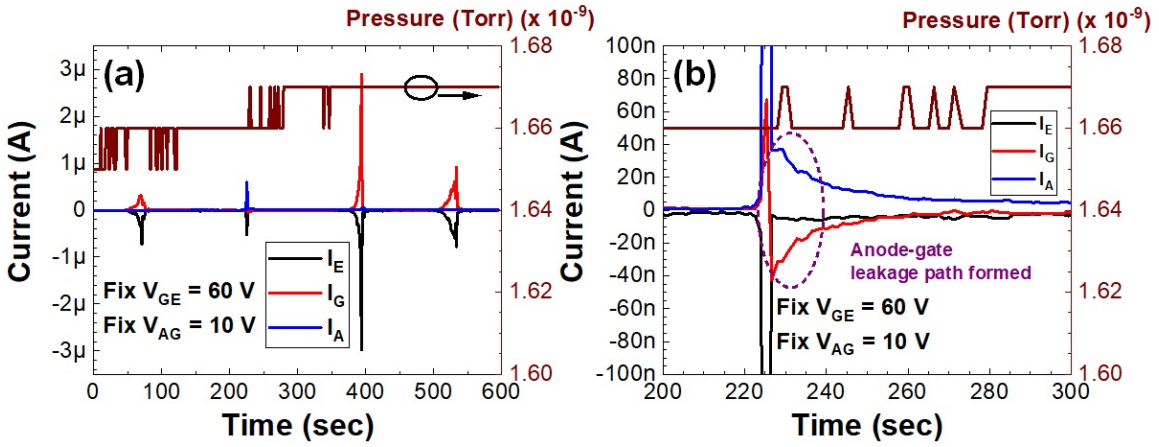


Figure 6-25: The DC operation test of another fully-integrated GaN field-emission-based vacuum transistors. The plot (b) is the zoom-in for the measurement during 200 sec to 300 sec. A sudden sign change of gate current and anode-gate leakage formation happens right after a small jump in emission current. However, the chamber pressure does not change during this time period. This anode-gate leakage path formation requires more investigation in the future.

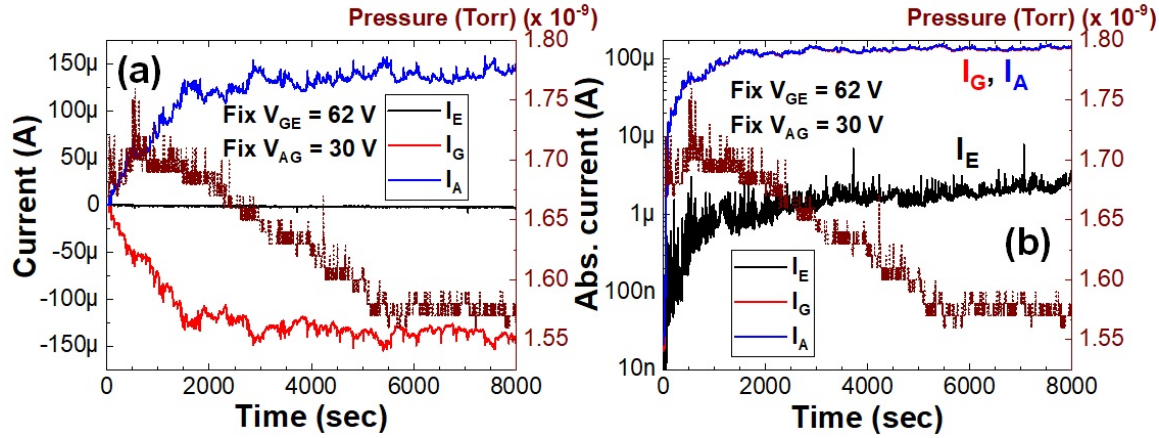


Figure 6-26: The subsequent DC operation test after the test shown in Fig. 6-25. The current is plotted in (a) linear scale and (b) log scale. The emitter current (I_E) is relatively stable but the anode-emitter leakage path has about 100× higher current than the emitter current at a fixed V_{AG} of 30 V.

leakage current level ($\sim$ 20 nA) at $V_{GE} > 50$ V. The increase of anode current is confirmed to be field-emission-dominated current with F-N slope ($-b_{FN}$ = -625.05 V) and F-N intercept ($\ln(a_{FN})$ = -13.72) (Fig. 6-27(b)). If assuming that (1) the tip-radius-dependent gate-emitter factor (β_{GE}) is the same as the one shown in Fig. 4-5(b), (2) the electric field on the emitter tip is only controlled by the gate-emitter

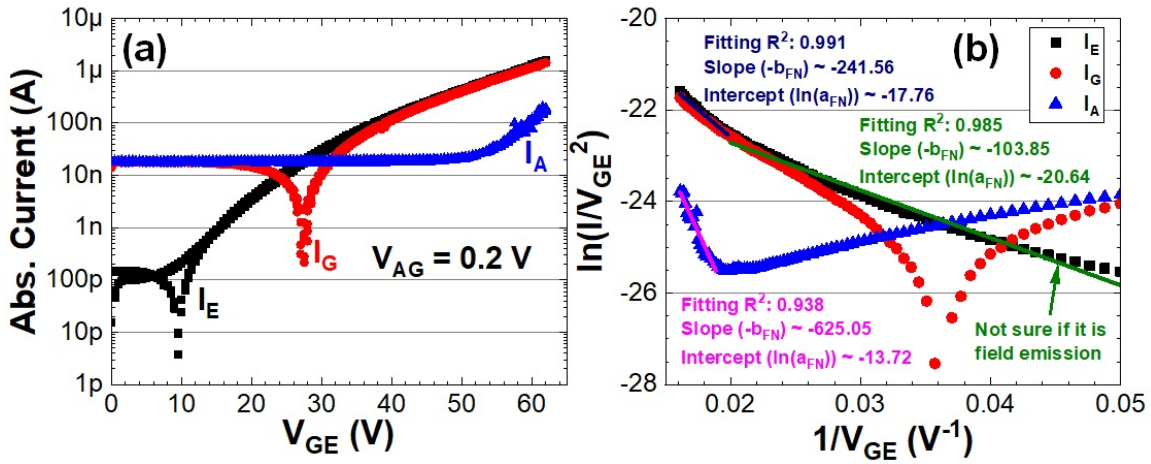


Figure 6-27: The (a) transfer characteristics and (b) F-N plot of the device after DC operation test (Figs. 6-25 and 6-26) at $V_{AG} = 0.2$ V. The V_{AG} is reduced to 0.2 V to reduce the leakage current between the anode and gate. The emitter and gate current is not like field emission current, while the anode current seems to agree with the field emission mechanism at $V_{GE} > 50$ V. The gate current changes sign from negative to positive at $\sim V_{GE} = 30$ V. The gate current at $V_{GE} < 30$ V is anode-gate leakage, and the gate-emitter current starts dominating at $V_{GE} > 30$ V.

voltage (V_{GE}), and (3) the work function of emitter tip is 3.8 eV, the extracted β_{GE} is about 7.7×10^5 cm^{-1} and the estimated emission tip radius is about 11.5 nm, which is much wider than the expected tip radius based on device design and fabrication (about 8-9 nm). On the other hand, if we assume the tip radius to be 9 nm, the β_{GE} will be about 8.6×10^5 cm^{-1} (based on Fig. 4-5(b)), and the estimated work function of emission tip will be about 4.08 eV. These results indicate that the TCAD simulation requires additional modifications on simulated structures or the device is not fully conditioned yet. It should be noted that we use two assumptions here: (1) the increase of anode current is due to the electron emission from the emitter tips, and (2) this electron emission is only controlled by the V_{GE}. In fact, the V_{AE} is also not a constant in this measurement setup, so the electric field on the emitter tips is in fact affected by both V_{GE} and V_{AE} (equation (6.1)).

Furthermore, in these fabricated preliminary devices, since the TEOS pillars are important for anode terminal formation, BOE or HF-based acid cannot be used to remove the ALD Al_2O_3 layer on the GaN tips, and this AL_2O_3 layer is instead etched by TMAH-based developer (AZ 300 MIF for 5 mins) in this experiment. However, it

is not clear whether there is still some remaining Al_2O_3 layer on the tips and whether the GaN tips are affected by the TMAH-based developer. The precise tip radius, and the confirmation of residual Al_2O_3 layer and tip shapes should be investigated by high-resolution TEM in the future.

Besides the anode current, the emitter current (I_E) and gate current (I_G) are also recorded (Fig. 6-27(a)). The gate current at $V_{GE} < 30$ V is at a constant -20 nA (anode-gate leakage), and it changes the sign and starts increasing at $V_{GE} > 30$ V. The gate-emitter conduction dominates both I_E and I_G at $V_{GE} > 30$ V. However, when I_E is analyzed in the F-N plot (Fig. 6-27(b)), it is noted that the I_E does not fully match with the field emission mechanism across the whole bias range. Given that the current flowing through the emitter tips is small (average < 1 nA / tip), the joule-heat-induced tip shape reconfiguration might be less likely to happen. As shown in Fig. 6-23(b), the increase of I_E at low V_{GE} happens after the anode-gate leakage path formation, the increased I_E and gate-emitter conduction might be also resulted from the re-deposition of materials which desorb from the emitter tips. However, this hypothesis requires more study and investigation, such as cross-sectional SEM images, to confirm whether this hypothesis is correct or not.

The measured devices are then checked by SEM again (Fig. 6-28). The overall SEM image of the measured device (Fig. 6-27) does not show any clear degradation or damage at the oxide or the device region (Fig. 6-28(a)). The zoom-in top-view SEM image of the FEA region also does not show any noticeable damage or degradation (Fig. 6-28(b)). On the other hand, the zoom-in SEM image of the probed anode region show clear scratches and potentially some damages (Fig. 6-28(c)).

It is hard to confirm where the gate-emitter leakage path exists by top-view SEM images (Fig. 6-28). Therefore, the cross-sectional SEM images of both FEA region and probed anode metal region might be necessary (Figs. 6-29 and 6-30) to identify the leakage path and potential weak points in the device structure or induced by the certain process steps. By checking the cross-sectional structures obtained by the FIB, the dimensions of the fabricated anode-integrated GaN SAGFEAs (Fig. 6-30(a)) seem to match our designed structure; while the SiO_2 is only etched down for

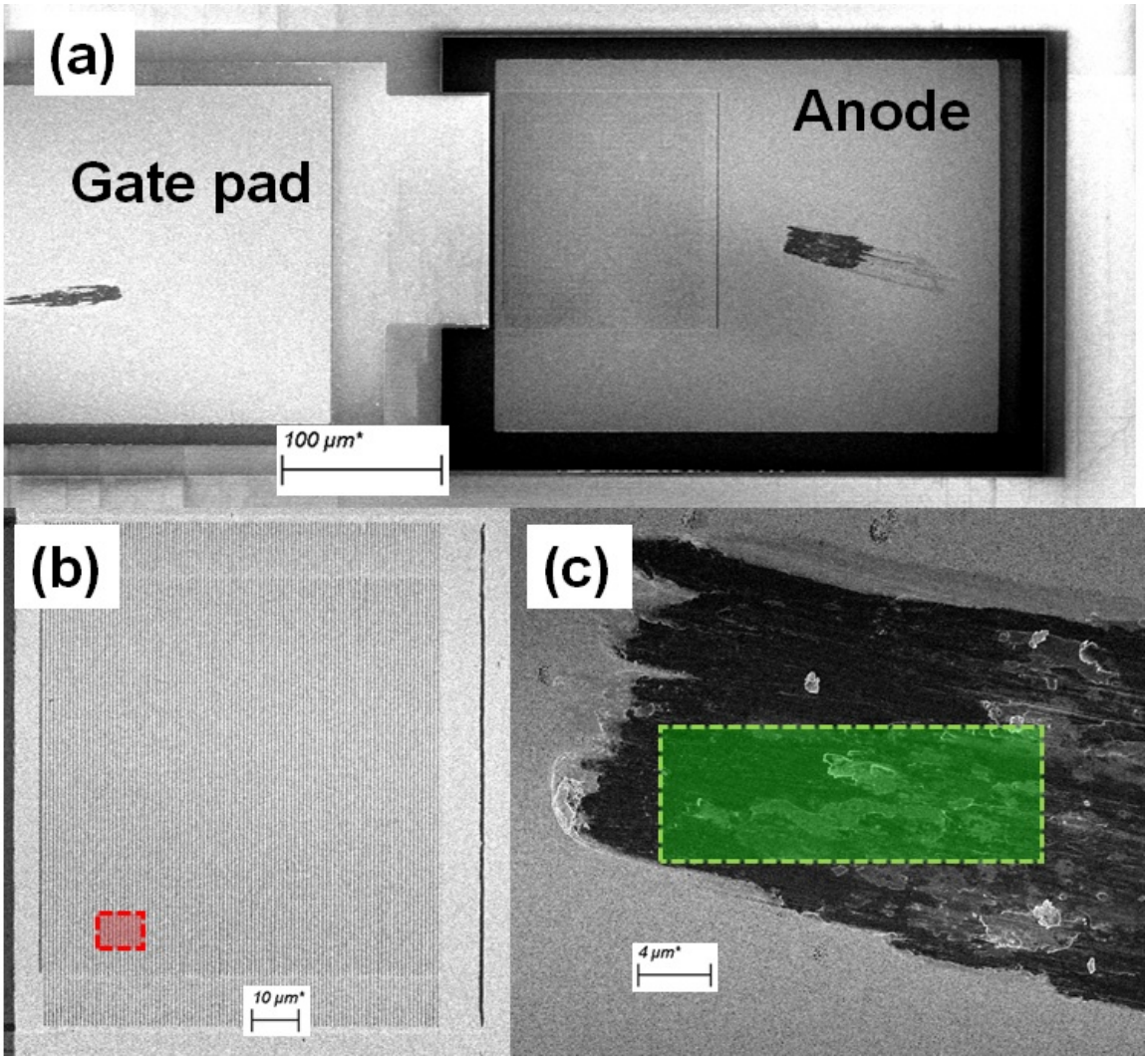


Figure 6-28: The top-view SEM images of (a) one overall device area, (b) FEA area, and (c) probed anode metal region after measurement (Figs. 6-27). Though the significant anode-gate leakage forms and is observed in I-V characteristics measurement (Fig. 6-27), there is no SEM-detectable damage or degradation in the FEA area (Fig. (b)). On the other hand, the probed anode region seems to have some damages (Fig. (c)); while it requires further investigation to confirm whether the anode-gate leakage forms in these probed regions. The red and green rectangle regions represent the locations which are cut by FIB to check the cross-sectional structures in Fig. 6-30.

about 190 nm (when comparing the Cr gate height and the etched SiO_2 regions). More optimizations on the etching of this tip-exposure step are still necessary. It should be noted that the FIB-cut cross section is not right on the tip apex region, and thus the GaN pyramids shown in Fig. 6-30(a) do not contain the sharpest top regions because of this FIB-cutting misalignment. When checking the cross-sectional

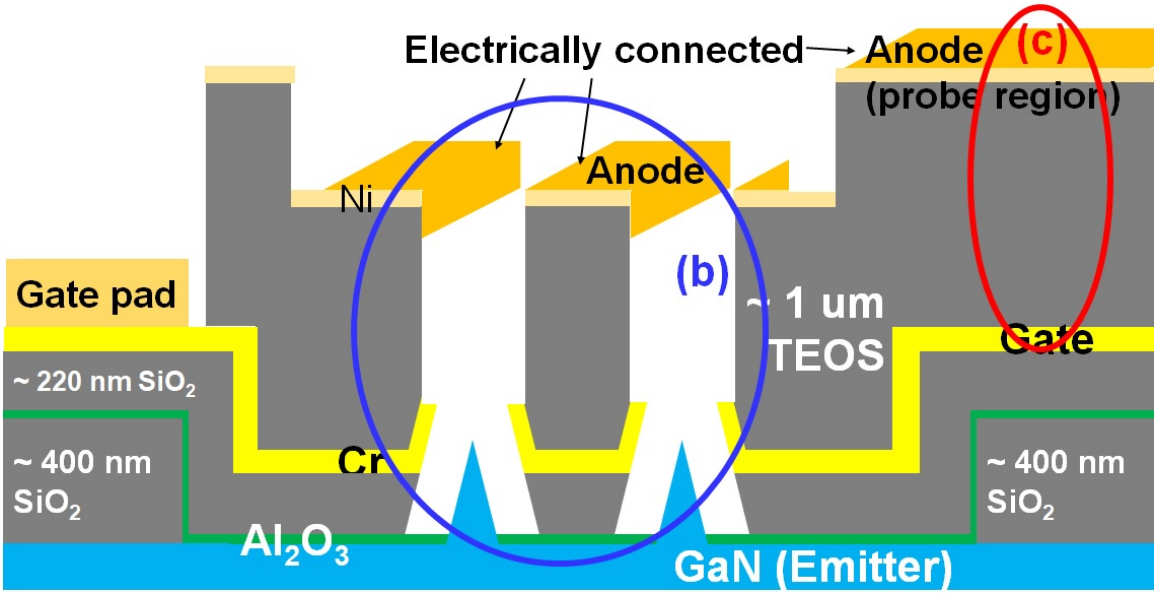


Figure 6-29: The full deivce geometry of an anode-integrated GaN field-emission-based vacuum transistor. The blue and red circles represent the FEA region (Fig. 6-28(b)) and probed anode region (Fig. 6-28(c)). Since the gate metal (Cr) is deposited by Ar-plasma-based sputtering, there might be Ar trapped in the gate metal film. As there is no observable damage in FEA region (Fig. 6-28(b)), one hypothesis is that the leakage paths form between the anode and gate (red circle); however, it should be checked by cross-sectional SEM images (Fig. 6-30).

structures, other than those re-deposited materials on TEOS pillar sidewalls, there is no observable damage nor leakage path. The re-deposited materials are most likely to be materials sputtered away by Ga ions during the ion milling step, and these materials then re-deposited on the nearby regions and empty cavities between the anode and FEA.

Since the cross-sectional SEM images (Fig. 6-30) do not show clear leakage paths or damages, the cause of this conditioning-induced anode-gate leakage requires more study in the future. Though it is possible that there are leakage paths or damages existing in regions which are not cut by FIB and checked by SEM, there are also few other possible issues that potentially cause this problem. For example, the sputtered gate film (Cr) might degas during the measurement. Furthermore, the non-conditioned GaN emitter tips might also have additional adsorbates released during the measurement and affect the device behavior and stability. Therefore, the change

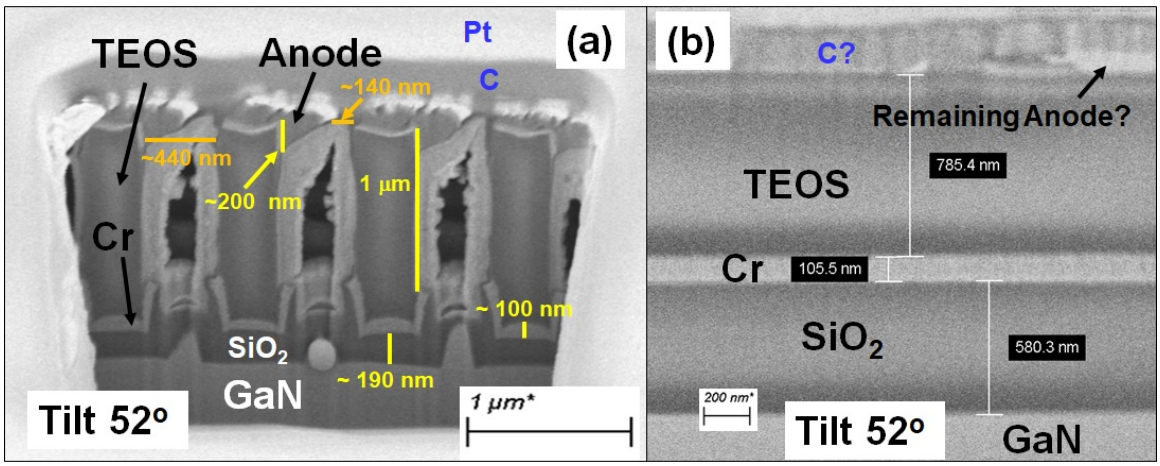


Figure 6-30: The cross-sectional SEM images of (a) field emitter array region and (b) probed anode pad region. Region (a) is the red rectangle region in Fig. 6-28(b) and blue-circled region in Fig. 6-29, and region (b) is the green rectangle region in Fig. 6-28(c) and red-circled region in Fig. 6-29. The Carbon (C) and Pt are deposited by electron beam and Ga ion beam to protect structures during the Ga ion milling step in the FIB. Other than the re-deposited materials on the TEOS sidewalls shown in (a), there is no observable damage nor leakage path in the cut regions.

of gate metal deposition from sputtering to e-beam evaporation might be critical, and the proper approach to condition or prepare the GaN emitter tips, such as UV-light treatment or baking, right before or during the anode metal deposition will be necessary and critical to prevent the requirement of conditioning step during the device measurement. This proper conditioning is also critical for future compact III-Nitride field-emission-based vacuum transistors in circuit-level integration.

6.3.4 Discussion

The approach consists of EBL alignment and the tilted metal deposition is tested and is shown promising as a reproducible way to fabricate fully integrated GaN field-emission-based vertical vacuum transistors. The vacuum transistors with 1 μm or sub-1 μm channel length can be fabricated and the anode metal is mechanically stable, compared to the suspended metal membrane proposed in section 6.2. However, the measured preliminary devices show issues such as anode-gate leakage path formation during the measurement, and the still-required conditioning procedure for these

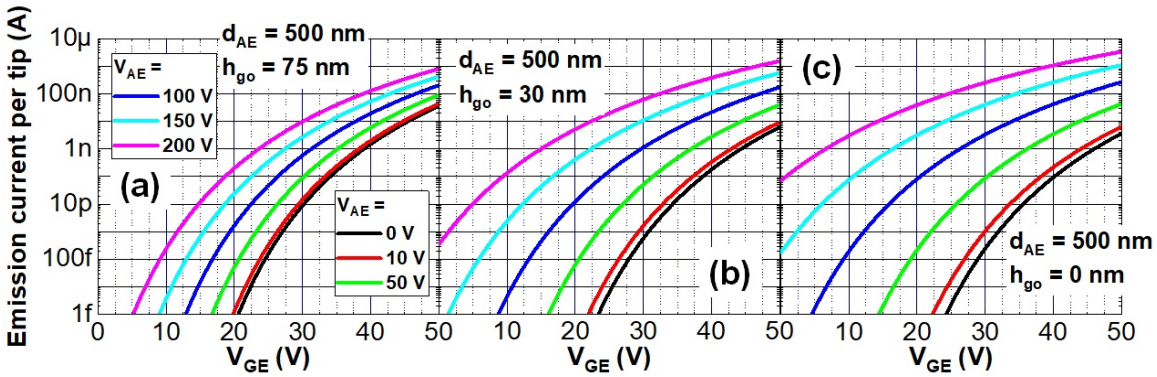


Figure 6-31: The estimated emission current per tip of the fully-integrated GaN field-emission-based vacuum transistors based on the Silvaco TCAD simulation and equations in literature [34]. The simulated structure is similar to the one shown in Fig. 6-1, and devices with three different height difference between gate and tip (h_{go}) are simulated. To mitigate the short channel effects, the gate works better to screen the electric field from the anode when it is higher than the emitter tip.

devices. The conditioning procedure potentially indicates that there is residual gas adsorbing on the emitter tip surface.

The possibility of potential residual gas desorption during the device operation is still an issue with more uncertainty, such as the amount of residual gases, local pressure change, and their effects on device operation. The water vapor has been discussed as one main adsorbate on Si FEAs affecting the device performance [191], but the residual gas analysis on GaN FEAs is still an ongoing study topic. If the water vapor is also the main affecting adsorbate for GaN FEAs, the in-situ heating of the e-beam evaporator before the anode metal evaporation might be helpful, but the elevated temperatures are usually used for this purpose, for example, annealing at 250^{o}C or higher temperature [174, 180]. This is a general issue for all field-emission-based vacuum transistors when the vacuum cavity is packaged. If the residual gas or the diffusion of gas into the vacuum cavity is still a concern of the sealed integrated vacuum transistors, the getter, such as Ti getter, can be designed and be integrated with the device to help maintain the vacuum cavity condition [183]. However, the device structure and fabrication will be more complex and require additional investigation in the future.

Besides the issues observed during the I-V characteristics measurement, the device

geometry can also affects the device behavior. The device performance with different geometries is thus simulated and estimated by Silvaco TCAD and the equations in literature [34]. As discussed in section 6.1, the gate can screen out some portion of the electric field from anode if the gate is higher than the tip surface with this specific gate shape (Fig. 6-31). If compare the transfer characteristics of V_{AE} = 0 V and 50 V, when the emission current per tip is fixed at 1 pA, we can have a preliminary quantified short channel effect:

$$AIBL = \frac{V_{GE}(V_{AE}=0V) - V_{GE}(V_{AE}=50V)}{50-0}|_{I=1\ pA} \tag{6.3}$$

where the anode-induced-barrier-lowering (AIBL) is an analogy to the drain-induced-barrier-lowering (DIBL) used in MOSFETs. It should be noted that this is a preliminary definition since the DIBL in MOSFETs is defined based on threshold voltage shift due to different drain-source bias voltage (V_{DS}), while there is no similar definition of the threshold voltage in the FEAs. We can thus compare the short channel effects existing in three different structures (Table 6.1). Therefore, though the reduced anode-emitter distance induces short channel effects, this issue can be mitigated by modifying the device structure. Furthermore, the increase of anode-emitter distance, for example, increasing from sub-1 μm to 2 or 3 μm channel length, can also reduce the short channel effect.

Table 6.1: The extracted anode-induced-barrier-lowering (AIBL) of different device geometry simulated by Silvaco TCAD.

Data from	Fig. 6-31(a)	Fig. 6-31(b)	Fig. 6-31(c)
AIBL	78 mV/V	146 mV/V	197 mV/V

In addition to understanding the effects of gate position on device performance, the peak electric field on this proposed device structure is also investigated by a simplified Silvaco TCAD simulation (Fig. 6-32). At OFF state, the peak electric field will exist at gate surface or tip surface; however, these peak electric fields in vacuum are still much lower than 2 V/nm, so the leakage is not a big concern. On the other hand, there is also a peak-electric-field region at the anode-oxide-vacuum

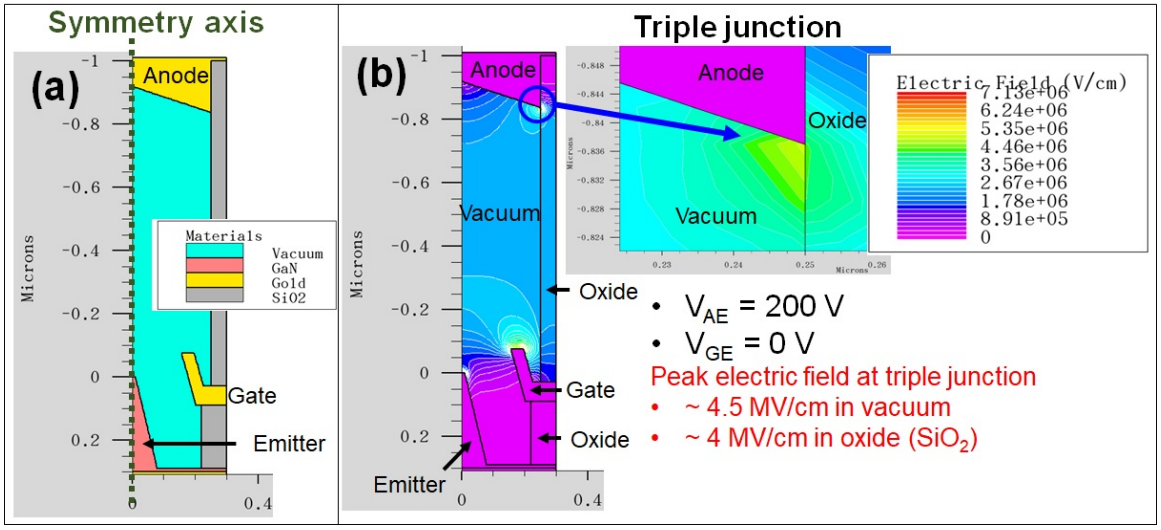


Figure 6-32: The electric field distribution of a fully-integrated vacuum transistor simulated by Silvaco TCAD. (a) The structure is based on cylindrical symmetry to simplify simulation complexity, and (b) the electric field distribution at V_{AE} = 200 V and V_{GE} = 0 V. The peak electric field is at gate surface and is about 7 MV/cm, and the peak electric fields at the anode-oxide-vacuum triple junction are 4.5 and 4 MV/cm in vacuum and oxide, respectively. If the anode voltage is kept below 100 V, the peak electric field at the triple junction should not be a significant issue.

triple junction. Based on these simplified simulation results, as long as the anode voltage is kept at or below 100 V, the peak electric field at this triple junction should not be a big issue for device long-term stability.

Though there are still necessary experiments to confirm and debug the issues mentioned above, this approach is promising to build the vacuum transistors with locally packaged vacuum channels. Moreover, compared to the process requiring CMP for a flat surface, this approach is more flexible and can be potentially applied to different materials' field emission devices, no matter whether the devices are fabricated on small pieces or wafers.

6.4 Comparison between two approaches

Two different approaches to form integrated anode on the GaN field-emission-based vertical vacuum transistors are proposed and tested with preliminary experiments. Both approaches are compared and their pros and cons are listed in Table 6.2.

Table 6.2: Comparison of two different approaches for anode integration.

Approach	Metal membrane	EBL and tilted metal dep.
Vacuum channel length	5 – 10 μm and above	500 nm – 2 μm
Pros.	• No charging issue on oxide • Have been demonstrated in MEMS devices	• Tolerance for non-planar surface • Vacuum cavity can be in-situ packaged during metal dep.
Cons.	• Non-planar surface can cause problem • Thick metal are needed	• Need e-beam lithography alignment • Electrons might accumulate on SiO_2 sidewall and cause breakdown

Generally, if the vacuum channel length can be above 10 μm, the bonding process might be an easier way, especially for wafer-scale fabrication. However, if the vacuum channel length needs scaling, the metal membrane (for vacuum channel length of few μm) or the EBL with tilted metal deposition (for vacuum channel length of sub 2 μm) might be better than the conventional bonding process. If the charging on oxide from emitted electrons causes device stability issues and failure, the metal membrane approach might be better. On the other hand, the EBL alignment with tilted metal deposition is more flexible and the vacuum channel can be in-situ sealed during the fabrication; though an additional gas diffusion layer, such as Al_2O_3, might be necessary to prevent the gas from diffusion and degrading the vacuum cavity [192]. The vacuum environment might not be required during the packaging and wire bonding since the vacuum channels are isolated from the external environment. Therefore, while the metal membrane approach is more mature as the MEMS society has been working on this type of structures for decades, the 2nd approach, EBL alignment with tilted metal deposition, might be a better way in this specific application for fully integrated vacuum transistors.

Chapter 7

Conclusion and future work

7.1 Conclusion

In this thesis research, III-Nitride vertical field emitter arrays with self-aligned gates are developed. GaN SAGFEAs are demonstrated and their performance has been improved over 3 orders of magnitude in anode current density over 4 generations of devices. The N-polar GaN and AlGaN SAGFEAs are also demonstrated in preliminary experiments. However, the performance of N-polar GaN and high-Al AlGaN SAGFEAs is not better than Ga-polar GaN SAGFEAs, requiring more study in the future.

Besides the demonstration of III-Nitride SAGFEAs, another critical aspect of fully-integrated vacuum transistors, the development of an integrated anode, is also discussed in this thesis. Two different approaches, (1) metal membrane, and (2) EBL alignment with tilted metal deposition, are proposed and tested by preliminary experiments. While there are still some parts requiring more study and experiments, the 2nd approach seems to be a better way to form the fully integrated III-Nitride field-emission-based vacuum transistors.

Though there are still topics requiring more study, the results reported in this thesis serve as a foundation for future development of the useful III-Nitride field-emission-based vacuum transistors for high power, high-frequency, or harsh-environment applications.

7.1.1 GaN vacuum transistors

This thesis has significantly advanced the understanding of GaN field emission devices. Two-terminal GaN field emitter arrays are first fabricated with a top-down approach and characterized. The field emission current is stable over 24-hour DC operation and the maximum current density is estimated ~ 4 A/cm^2 based on the FEA area. The basic and stable electron field emission is confirmed in this two-terminal diode study, and the top-down technology is proven to make well defined field emitters based on arrays of GaN vertical nanostructures.

After the experiments on two-terminal GaN FEAs, the self-aligned-gate structure is then developed and integrated onto GaN FEAs to make a three-terminal vacuum transistors with a gate control capability. Thanks to the use of self-aligned-gate structures, the operating gate voltage can be reduced from a few hundred volts, when remote gate grids are used, to sub-100 V thanks to the reduced distance between gate and emitter tip. The devices have been improved over 4 generations of technology advances. The following different generations of GaN SAGFEAs are fabricated on pieces cut from one 6-inch GaN-on-Si wafer, which is grown by MOCVD and provided by Dr. Kai Cheng at Enkris, Inc.

In the first generation of GaN SAGFEAs, the emitter tips are based on the GaN vertical NWs formed by two-step etching combining dry etching and heated TMAH wet etching. These NWs are not stable and are prone to break if the NW diameter is below 30 nm. Furthermore, the variation in NW diameter is also observed, and this variation makes these NW SAGFEAs less favorable since the main portion of the emission current will only conduct through sharpest tips and can cause device instability, thermal runaway, or other issues.

In the more advanced generations of GaN SAGFEAs, the emitter tips are changed from NW shape to pyramid shape. The pyramid-shape emitter tips are more mechanically stable and the size variation can be reduced since the TMAH etching is avoided. However, the electric field enhancement on pyramid tips is generally lower than the one on NW tips; therefore, a feasible way to sharpen these pyramid tips is neces-

sary to keep and improve the device performance. A wet-based digital etching (DE) process is then developed for this purpose, and the GaN pyramid tips with sub-10 nm tip radius can be obtained by sharpening these vertical structures via this DE process. The device structures are furthter modified in the 3rd and 4th generations of GaN SAGFEAs, and the most recent devices have state-of-the-art performance in all III-Nitride FEAs with $V_{GE,ON}$ of 20 V (@ I_A = 1 fA/tip) and J_A of 10 A/cm^2 at V_{GE} = 50 V. The extracted tip radius from measured I-V curves and TCAD simulation matches the SEM observation very well, and the average emitting area per tip is now comparable to the state-of-the-art Si devices (at least to the ones with available data for estimation) in literature. The maximum emission current per tip (I_A per tip) is about 35 nA/tip at V_{GE} = 50 V, which is close to the best Si devices in literature (100 - 500 nA/tip at V_{GE} = 50 V), and the current density of this best device is higher than the state-of-the-art Si SAGFEAs at V_{GE} =50 V reported in literature.

7.1.2 Other III-Nitride vacuum transistors

One motivation for using III-Nitride as field emitters in vacuum transistors is the engineerable electron affinities of III-Nitride semiconductors. The N-polar GaN has a lower electron affinity then the Ga-polar GaN, and it is also reported that the electron affinity of high-Al AlGaN is lower than the one of low-Al AlGaN. Semiconductors with degenerated n-type doping and low electron affinity can be a good electron emission source since the tunneling barrier, work function, will be low.

Both N-polar GaN and metal-polar AlGaN semiconductors with different Al compositions are used in this thesis work to demonstrate field-emission-based vacuum transistors. The N-polar GaN are grown by MOCVD and provided by Dr. Raju Ramesh at Aalto University, Finland. The metal-polar AlGaN with different Al compositions are grown by MBE and provided by Prof. William Alan Doolittle group at Georgia Institute of Technology.

The process flow of N-polar GaN and AlGaN SAGFEAs is similar to the one of Ga-polar GaN SAGFEAs with some minor modifications. However, since critical steps, such as dry etching and digital etching on emitter tips, are only optimized for

the Ga-polar GaN emitters, there are different issues observed during the fabrication of N-polar GaN and AlGaN devices. For example, the dilute HCl used in DE can attack and roughen the N-polar GaN surface, leading to the high gate leakage in N-polar GaN SAGFEAs. The piranha step in DE is also found to roughen the sidewalls of high-Al AlGaN pyramids. Therefore, though the process flow is applicable to different III-Nitride semiconductors, the critical steps still require material-dependent optimizations. The fabricated N-polar GaN and AlGaN SAGFEAs were characterized; however, the performance of these devices is not better than Ga-polar GaN SAGFEAs because of the non-optimized process steps. Furthermore, the work function of the high-Al AlGaN surface was not found to be lower than the one of low-Al AlGaN or Ga-polar GaN surface. The work function measurement is conducted by UPS and is helped by Dr. Tyson Back at AFRL. The UPS results indicate that additional surface effects, such as surface-states-induced band bending, might exist and influence the surface properties. More study is necessary to make low-work-function III-Nitride emitter tips in the future.

7.1.3 Fully-integrated vacuum transistors

Besides III-Nitride SAGFEAs, another important aspect of vacuum transistors, the formation of the anode terminal is also critical for fully integrated devices. The device characterization in this thesis research is done in a UHV system with a suspending tungsten metal ball as the anode terminal. The device fabrication can thus be easier since the vacuum channel is defined by the measurement setup in the UHV chamber. However, to apply these SAGFEAs as vacuum transistors for circuit-level and practical applications, the separated integrated anode for each vacuum transistor is necessary. Therefore, two different approaches are proposed and tested with preliminary experiments in this thesis research.

The first approach is the suspended metal membrane as the anode terminal. a-Si and Mo are used as sacrificial layers under the anode metal (Cr) deposited by sputtering. XeF_2 gas, widely used for MEMS fabrication, can react and remove both Si and Mo and it will not etch Cr and SiO_2. The XeF_2 etching is shown to be able to

undercut the a-Si in preliminary experiments, but the suspended Cr metal membrane breaks after the etching. There are multiple issues in this test structure: narrow gap (sub μm) and long length ($>$ 100 μm), thin metal membrane ($\sim$ 120 nm), and non-flat surface. Additionally, the electrostatic force induced by electric field during the device operation can pull down the anode metal and break it or make a electrical short. Moreover, local supporting dielectric pillars might be necessary to make this metal membrane more stable. All these issues require more study in structure design, such as mechanical stress simulation. Although this approach might be good for vacuum transistors with $>$ 5 μm vacuum channel length, it is challenging for devices with sub-1 μm vacuum channel length and non-flat surface.

The second approach is the EBL alignment followed by tilted metal deposition. The EBL alignment with sub-50-nm resolution is used to define SiO_2 pillars that will act as the supporting dielectrics and the insulator layer between the anode and gate. The anode metal is then deposited by tilted metal deposition. There are a few advantages of this approach, such as well-defined and changeable vacuum channel length, mechanically stable anode metal, and the potential of in-situ vacuum cavity package during the metal deposition. The preliminary experiment results show that this approach is also more robust on the non-flat surface than the metal membrane approach. Though there are still issues and uncertainties requiring more optimizations, this approach is believed to be a better way to fabricate fully integrated vacuum transistors.

7.2 Future work

7.2.1 Optimizations on AlGaN composition and fabrication

The AlGaN SAGFEAs are expected to provide better performance than Ga-polar GaN SAGFEAs because of their low electron affinities. However, the measured work function of n^{++} AlGaN materials is not lower than the one of n^{++} Ga-polar GaN, which might be the result from the surface-state-induced band bending. Therefore,

a detailed study on n^{++} AlGaN (0001) surface with different Al compositions is necessary to understand the difference between electron affinities and measured surface work function. The effects of surface states in III-Nitride field emission devices are discussed in literature recently [172], but there is still more work to be done.

Furthermore, the process flow developed in this thesis research is based on Ga-polar GaN emitter tips, and the critical etching steps require material-dependent optimization. For example, the dry etching recipe used for Ga-polar GaN produce different shapes of AlGaN etched structures, and the wet-based DE is not optimized for high-Al AlGaN emitter tips since the piranha etch is observed to directly etch and roughen AlGaN sidewall surface.

7.2.2 RF and power characteristics of vacuum transistors

The GaN and AlGaN SAGFEAs demonstrated in this thesis research are mostly characterized as discrete transistors with basic transfer and output characteristics. However, the performance and behavior characterizations of these III-Nitride field-emission-based vacuum devices in RF and power applications require the development of an integrated anode. Once the integrated anode technology is fully in place with reproducible fabrication, the practical RF and power device measurement, such as power gain and power add efficiency (PAE) in different frequency and bias conditions can be characterized, which are important metrics for future applications.

7.2.3 Radiation and high-temperature characterization

As the vacuum electronics are believed to be more robust under radiative and high-temperature environments than solid-state electronics, the degradation and stability study of these field-emission-based vacuum transistors in harsh environments is both beneficial and necessary to the practical applications of vacuum transistors. The integrated anode structure is not a necessary structure in this type of study, but the study of the impact of radiation and high temperature on devices under bias can provide more information than the approach of just comparing devices before and after

radiation or high temperature treatment. The in-situ device characterization under radiation or at high temperature will require fully integrated vacuum transistors. These advanced experiments can confirm whether vacuum transistors are robust under harsh environments and the best applications for them.

Appendices

Appendix A

Process flow and development of GaN NW SAGFEAs

GaN NW SAGFEAs with TEOS Planarization

This process flow was developed in 2019 and was performed in the old cleanroom at MTL. Most of the tools are not available anymore or are moved to the new cleanroom at MIT.nano with a new tool name since 2021.

Process and Number	Process Step	Tool
1. Wafer Cleaning	10 min Piranha Clean	Acid-Hood
2. Alignment Mark Formation *(Optional)*	Spin coat PMMA-950 A4	Coater
	Bake for 7 min at 180°C	Hot Plate
	EBL to open pattern for metal mask lift-off	elionix
	Evaporate 15 nm Cr/ 50 nm Au	ebeamFP
	Place in acetone (or NMP) for lift-off	Photo-wet-Au
3. EBL for Fin Formation	Spin coat PMMA-950 A4	Coater
	Bake for 7 min at 180°C	Hot Plate
	EBL to write pattern for metal mask lift-off (device pitch ~ 1 um)	elionix
	Evaporate 40 nm Ni (Zero rotation)	ebeamFP
	Place in acetone for lift-off (no ultrasonic)	Photo-wet-Au
	Use SEM to check EBL pattern	semZeiss
4. Fin/NW Etch	Etch roughly 300 nm GaN with Recipe #45 GaN-High (~1'30") Or Recipe #46 GaN-Low (~5'30")	SAMCO
	Use AFM to check surface roughness of etched region	AFM
	Use profilometer to check etch depth	dektak
5. Wafer Clean	Remove residual PR with acetone	Photo-wet-r
	Optional: improve sidewall roughness with 10 min in TMAH at 80°C (170~175 °F) or 30 min in TMAH at 70°C	Acid-Hood
	Remove Ni by piranha 10 min	Acid-hood
6. Thick TEOS near device	1000 nm TEOS deposition (TEOS_350C_Zerostress_Noclean) (Deposit ~ 40 nm/min)	Oxford-100
	HMDS 1 min program	HMDS-oven
	Spin coat SPR-700 (750 rpm 6" -> 3500 rpm 60" -> 90°C 6 min)	Coater

	Define etch region (375 nm, dose: 130) (or 405 nm, dose: 170)	MLA-150
	Post bake 115°C 1 min	hotplate
	Develop: CD-26 75" -> DI water rinse	Photo-wet-r
	BOE etch TEOS	Acid hood
	Remove resist	Asher and photo-wet-r
7. Gate deposition	300 nm TEOS deposition	Oxford-100
	Cr/Al/Mo/Cr deposition (Sputtering) (10 nm/ 70 nm/ 30 nm/ 10 nm)	AJA-TRL
8. TEOS planarization	1000 nm TEOS deposition (thickness ≥ device pitch)	Oxford-100
9. Define gate pad	HMDS 1 min program	HMDS-oven
	Spin coat SPR-700 (750 rpm 6" -> 3500 rpm 60" -> 90°C 6 min)	Coater
	Define gate pad region (375 nm, dose: 130) (or 405 nm, dose: 170)	MLA-150
	Post bake 115°C 1 min	Hotplate
	Develop: CD-26 75" -> DI water rinse	Photo-wet-r
10. Etch gate region	Dry etch TEOS (1050 ~ 1100 nm)	Plasmaquest or Oxford-100
	Dry etch Cr/Al/Mo/Cr	Plasmaquest
	Dry etch TEOS (~ 700 nm) (GaN etched + 300 nm TEOS + overetch)	Plasmaquest or Oxford-100
	Remove resist	Asher and photo-wet-r
11. Source Definition	HMDS 1 min program	HMDS-oven
	Spin coat PMGI SF5 (750 rpm 10"-> 3500 rpm 60")	Coater
	Bake 235°C 6 min	hotplate
	SPR-700 (750 rpm 6" -> 3500 rpm 60" -> 90°C 6 min)	Coater
	Lithography: MLA **170 mJ/cm²**, 0 defocus, 375 nm	MLA-150
	Descum 800 W 5 min	Asher
12. Source pad	Surface clean DI water dip 1 min	Acid-Hood
	HCl:DI water = 1:3 dip for 1 min	Acid-Hood
	DI water dip 1 min	Acid-Hood
	Ti/Al/Au deposition (10 nm/ 50 nm/ 50 nm)	ebeamFP
	Use NMP for lift-off	Photo-wet-r

	Optional: Remove residual by Asher	Asher
13. Expose emitter tips	HMDS 1 min program	HMDS-oven
	SPR-700 (750 rpm 6" -> 3500 rpm 60" -> 90°C 6 min)	Coater
	Lithography: MLA **170 mJ/cm^2**, 0 defocus, 375 nm	MLA-150
	Dry etch TEOS	Plasmaquest or Oxford-100
	Remove resist	Asher and photo-wet-r
14. clean	Organic	Photo-wet-r
	DI water rinse	Photo-wet-r
	Bake 130°C 5 min	hotplate

GaN NW SAGFEAs with Resist Planarization

This process flow was developed in 2019 and was performed in the old cleanroom at MTL. Most of the tools are not available anymore or are moved to the new cleanroom at MIT.nano with a new tool name since 2021.
This process was not used after the first few experiments in 2019-2020. All new GaN SAGFEAs since 2021 are fabricated with TEOS planarization process.

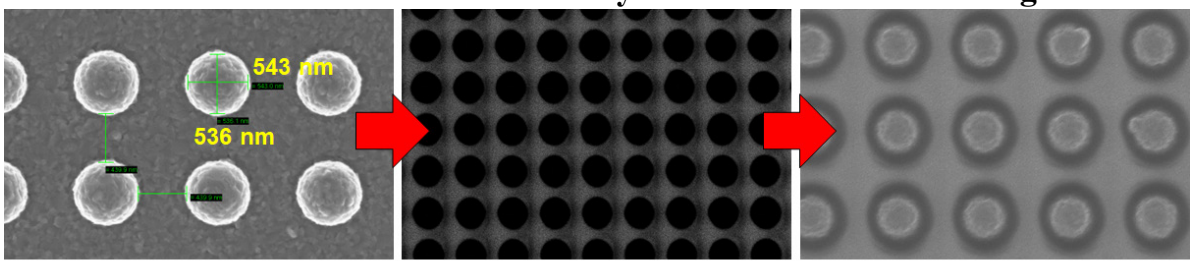
Process and Number	**Process Step**	**Tool**
1. Wafer Cleaning	10 min Piranha Clean	Acid-Hood
2. Alignment Mark Formation *(Optional)*	Spin coat PMMA-950 A4	Coater
	Bake for 7 min at 180°C	Hot Plate
	EBL to open pattern for metal mask lift-off	elionix
	Evaporate 15 nm Cr/ 50 nm Au	ebeamFP
	Place in acetone (or NMP) for lift-off	Photo-wet-Au
3. EBL for Fin Formation	Spin coat PMMA-950 A4	Coater
	Bake for 7 min at 180°C	Hot Plate
	EBL to write pattern for metal mask lift-off (device pitch ~ 1 um)	elionix
	Evaporate 40 nm Ni (Zero rotation)	ebeamFP
	Place in acetone for lift-off (no ultrasonic)	Photo-wet-Au
	Use SEM to check EBL pattern	semZeiss
4. Fin/NW Etch	Etch roughly 300 nm GaN with Recipe #45 GaN-High (~1'30")	SAMCO
	Use AFM to check surface roughness of etched region	AFM
	Use profilometer to check etch depth	dektak
5. Wafer Clean	Remove residual PR with acetone	Photo-wet-r
	Optional: improve sidewall roughness with 10 min in TMAH at 80°C (170~175 °F)	Acid-Hood
	Remove Ni by piranha 10 min	Acid-hood
6. Mesa etch	500 nm TEOS deposition	Oxford-100
	HMDS 1 min program	HMDS-oven
	Spin coat SPR-700 (750 rpm 6" -> 3500 rpm 60" -> 90°C 6 min)	Coater
	Define mesa etch region (375 nm, dose: 130)	MLA-150
	Post bake 115°C 1 min	hotplate

		Develop: CD-26 75” -> DI water rinse	Photo-wet-r
		Dry etch TEOS 550 nm (over etch 50 nm)	Oxford-100
		Remove resist step 1: nanostrip 10 min	Acid-hood
		Remove resist step 2: Ashing 1000 W 20 min	Asher
		Dry etch GaN 1 um (recipe #45, ~ 5’00”)	SAMCO
		Remove TEOS by BOE	Acid-hood
7.	Source define	HMDS 1 min program	HMDS-oven
		Spin coat PMGI SF5 (750 rpm 10”-> 3500 rpm 60”)	Coater
		Bake 235^{O}C 6 min	hotplate
		SPR-700 (750 rpm 6” -> 3500 rpm 60” -> 90^{o}C 6 min)	Coater
		Lithography: MLA **170 mJ/cm^{2}**, 0 defocus, 375 nm	MLA-150
		Post bake 115^{o}C 1 min	Hotplate
		Develop: CD-26 75” -> DI water rinse	Photo-wet-r
		Descum 800 W 5 min	Asher
8.	Source pad	Surface clean DI water dip 1 min	Acid-Hood
		HCl:DI water = 1:3 dip for 1 min	Acid-Hood
		DI water dip 1 min	Acid-Hood
		Metal deposition Ti(200 Å)/Al(1000 Å)/Ni(250 Å)/Au(500 Å)	ebeamAu or ebeam FP
		Lift off in NMP	photo-wet-r
		Acetone -> Methanol -> IPA	photo-wet-r
9.	Remove residual resist	Ashing 1000 W 10 min	Asher
10.	RTA	GAN800-direct, 800 ^{O}C 30 sec	RTA-pieces
11.	Wafer clean	Acetone -> Methanol -> IPA	photo-wet-r
12.	Gate deposition	200 nm TEOS deposition	Oxford-100
		100 nm Cr sputtering	AJA-TRL
		50 nm TEOS deposition	**Oxford-100**
13.	PR planarization for self-align gate	HMDS 1 min program	HMDS-oven
		Spin coat SPR-700 (750 rpm 6” -> 3500 rpm 60” -> 90^{o}C 6 min)	Coater
		Define gate (375 nm, dose: 130)	MLA-150
		Post bake 115^{o}C 1 min	hotplate
		Develop: CD-26 75” -> DI water rinse	Photo-wet-r
		Check resist thickness	dektak

	O_2 Plasma anisotropic etching resist (Recipe: O2_BL, ~ 40 nm/min?) **(Target: remaining thickness ~ 200 nm)** **(100 nm thinner than Fin height)**	Plasmaquest
	Check resist thickness	Dektak
	Check gate exposure	semZeiss
14. Self-align gate	**Dry etch TEOS 70 nm** **(over etch 20 nm)**	**Oxford-100**
	Dry etch Cr 120 nm (over etch 20 nm) (Cr etch, Cl_2/O_2-based plasma)	Plasmaquest
	Dry etch TEOS 350 nm (over etch 50 nm than Fin height)	Oxford-100
15. Remove PR and clean	Asher 1000 W 20 min	Asher
	Acetone -> Methanol -> IPA -> DI water	photo-wet-r
	Bake 130°C 5 min	hotplate

The highlighted steps are added since the resist is not a good mask for Cr dry etching, which uses Cl_2 + O_2 plasma. The failure due to the micromasking from resist is shown in the following pages.

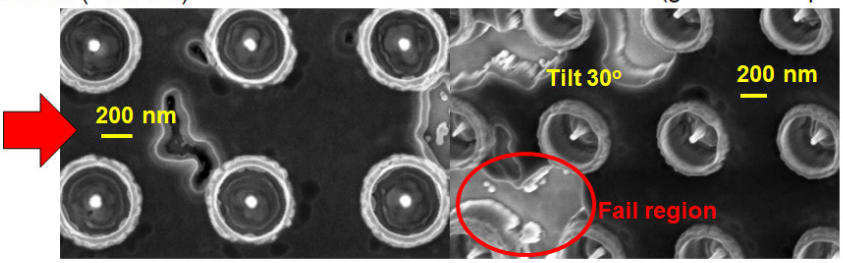
Resist Planarization without a TEOS layer between the resist and gate metal



PECVD TEOS (~325 nm) and Sputter gate metal (~100 nm)

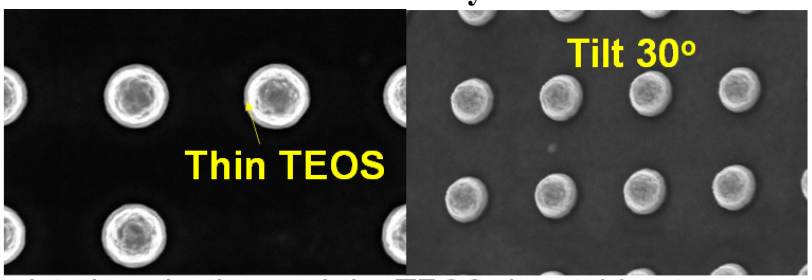
After SPR-700 coating and litho.

After oxygen plasma etching (gate metal exposed)

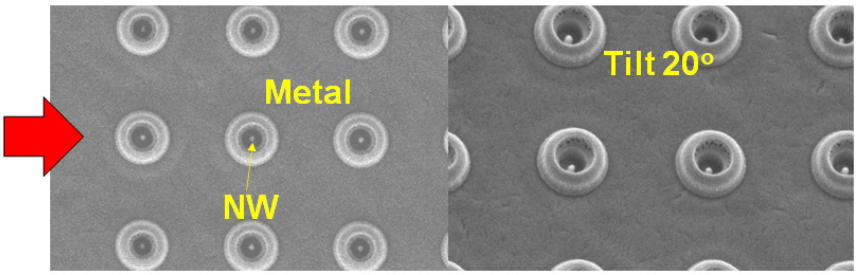


After metal and TEOS dry etching

Resist Planarization with a TEOS layer between the resist and gate metal

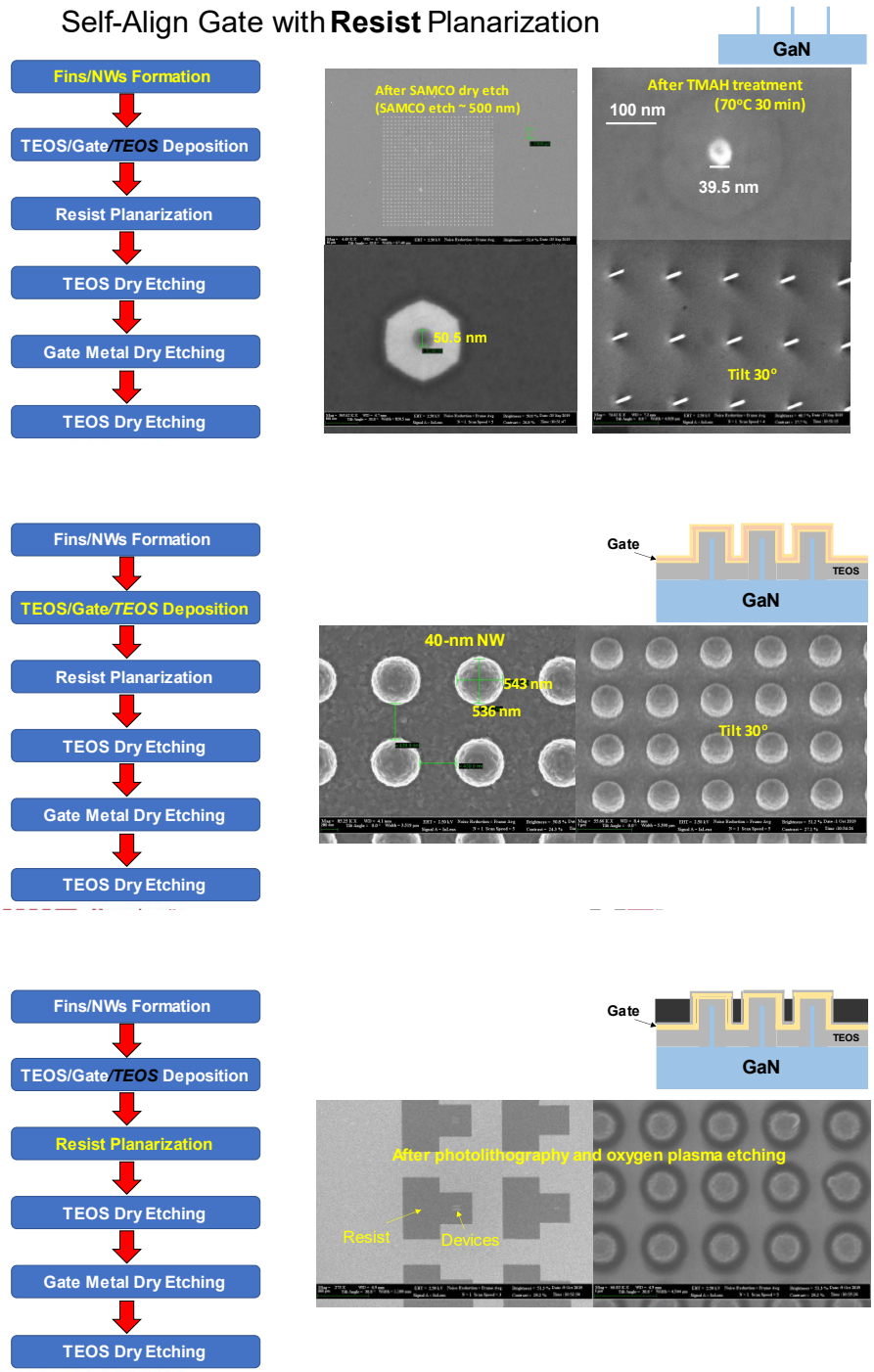


After resist planarization and the TEOS dry etching to expose the gate metal

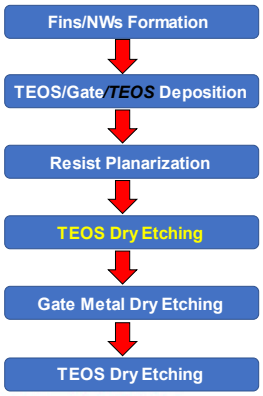


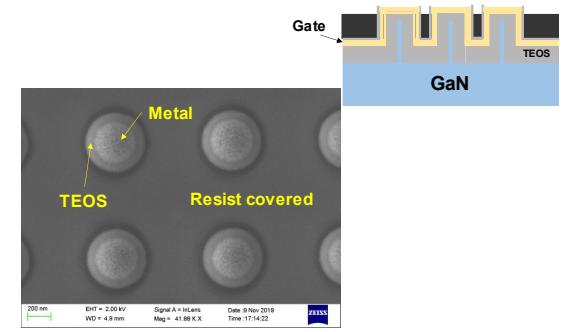
After GaN NW emitters are exposed by dry etching TEOS

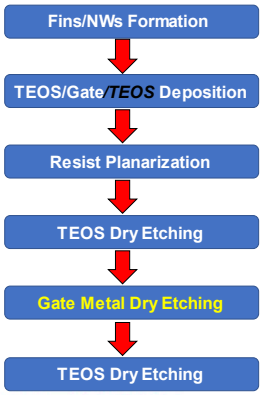
Process flow and SEM images of the resist planarization process

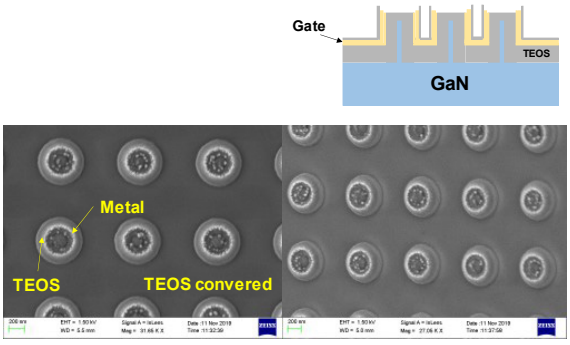


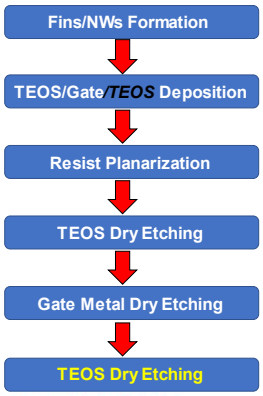
Appendix A: Process flow and development of GaN NW SAGFEAs

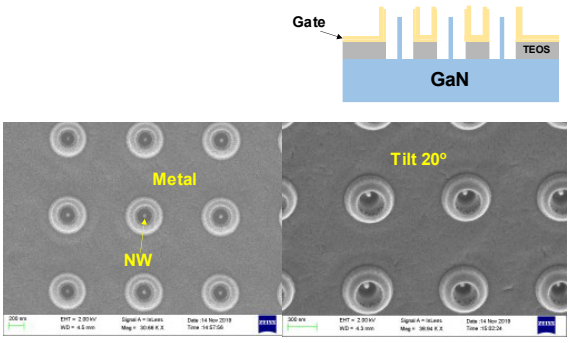












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Appendix B

Experiments of digital etching on GaN and AlGaN

Digital etching on GaN and AlGaN vertical sidewalls

Pao-Chuan Shih

This process flow was developed in 2020 and was performed in the old cleanroom at MTL. Most of the tools are not available anymore or are moved to the new cleanroom at MIT.nano with a new tool name since 2021. However, the wet-based digital etching has also been checked and works at MIT.nano since it is not a tool-dependent process.

Process and Number	Process Step	Tool
1. Wafer Cleaning	10 min Piranha Clean	Acid-Hood
2. Alignment Mark Formation *(Optional)*	Spin coat PMMA-950 A4	Coater
	Bake for 7 min at 180ºC	Hot Plate
	EBL to open pattern for metal mask lift-off	elionix
	Evaporate 15 nm Cr/ 50 nm Au	ebeamFP/ebeamAu
	Place in acetone (or NMP) for lift-off	Photo-wet-Au
3. EBL for Fin Formation	Spin coat PMMA-950 A4	Coater
	Bake for 7 min at 180ºC	Hot Plate
	EBL to write pattern for metal mask lift-off (device pitch ~ 600 nm)	elionix
	Evaporate 35 nm Ni (Zero rotation)	ebeamFP/ebeamAu
	Place in acetone for lift-off (no ultrasonic)	Photo-wet-Au
	Use SEM to check EBL pattern	semZeiss
	Remove residual PMMA by Ashing	Asher
4. Fin/NW Etch	Etch roughly 300 nm GaN with Recipe #45 GaN-High (~1'30") Or Recipe #46 GaN-Low (~5'30")	SAMCO
	Use profilometer to check etch depth	dektak
5. Wafer Clean	Organic clean	Photo-wet-r
	***Optional**:* improve sidewall roughness with 10 min in TMAH at 80ºC (170~175 ºF) or **30 min in TMAH at 70ºC**	Acid-Hood
	Remove Ni by piranha 10 min	Acid-hood
6. Digital Etching to shrink NW width	Check NWs by SEM	semZeiss
	Ozone plasma treatment	**UVozone-Au**
	Dilute HCl:H2O = 1:3, 1 min	Acid-hood

Doing above two steps several times		
	Check NWs by SEM	semZeiss

When doing in MIT.nano, Ni should be removed by Ni etchant TFB in the specific hood. So the cleaning procedure is changed to as follows:

(1) Ni etchant TFB to remove Ni mask
(2) Piranha to fully clean the sample

Additionally, the SiO_2 mask is also used when dry etching GaN. The advantage of SiO_2 mask is that some dry etching recipes do not work with Ni mask, but they work with SiO_2 mask. The etching recipes of SiO2 with Ni hard mask are discussed in section 4.5.2.

Experiments of digital etching on GaN and AlGaN sidewalls

Concepts of digital etching

- Most common way :
  1. Oxidization of GaN
  2. Then remove Ga_2O_3 or GaO_x
- What does "digital" etching mean ?
  - Self-limiting etching rate per run (oxidization more like a diffusive procedure)
  - Etching depth is linearly dependent on number of runs
- For oxidation :
  - Most common: Oxygen plasma , can be biased or unbiased
    Or N_2O plasma, ozone, etc
  - Self-limiting process , determined by power, pressure, etc
- For removing Ga_2O_3 or GaO_x:
  - Dilute HCl
  - BCl_3 plasma https://onlinelibrary.wiley.com/doi/epdf/10.1002/pssc.200983644

MTL

Directional or isotropic?

- Digital etching on GaN demonstrated in literature are mostly **directional** so far.
  - Biased oxygen plasma for oxidizing GaN along (0001) direction.
  - Most work focuses on vertical direction for AlGaN/GaN HEMT applications .
- Is it possible to do isotropically digital etching on GaN?
  - Since we can remove GaO_x by dilute HCl, the main question is:
    "Can we oxidize GaN isotropically?"
  - The answer should be yes.

Oxidation for digital etching of AlGaN/GaN

GaN/AlGaN	Oxygen/Ozone	Power	RF freq.	Pressure, flow	Time	Rate	Ref
AlGaN	O_2 plasma	50 W	30 kHz	300 mTorr O_2	30 s	6 A/cycle	[1], 2002_UCSB
GaN	**O_2 plasma**	50 W	30 kHz	300 mTorr O_2	60 s	**7 A/cycle**	[2], 2003_UCSB
	O_2 plasma	700 W	2.45 GHz	1 Torr O_2	10 min	~ 8 nm for 10 min	[3], 2003_IIT
	UV ozone	?	?	?	5 min	~ 3 nm/cycle (**plasma damaged surface**)	[4], 2000_UF
	Remote O_2 plasma	100 W	60 MHz	16.5 Pa, Ar: 30 sccm O_2: 20 sccm	5 min	**0.6 nm/cycle (saturated at RT)**	[5], 2018_NagoyaU
	UV ozone	?	?	?	9	?	[6], 2019_U-WM
	Remote O_2 plasma	100 W	60 MHz	16.5 Pa, Ar: 20 sccm O_2: 30 sccm	1 min	0.2 nm at RT 1 nm at 300°C 2.1 nm at 500°C	[7], 2019_NagoyaU
	UV ozone	**?**	**?**	**?**	**5 min**	**~ 1 nm/cycle, SAMCO UV-300 chamber**	[8], 2020_U-WM

These are unbiased condition
=> should be more isotropic.

MTL

Reference list of GaN oxidization for digital etching

1. D. Buttari *et al.*, *LEC 2002*, V-7 (UCSB)
2. D. Buttari *et al.*, *APL*, vol. 83, no. 23, pp. 4779 – 4781, 2003 (UCSB)
3. S. Pal *et al.*, *TSF*, vol. 425, pp. 20 - 23, 2003 (IIT)
4. A. P. Zhang *et al* 2000 *J. Electrochem. Soc.***147** 719 (U of Florida)
5. Taishi Yamamoto *et al* 2018 *Jpn. J. Appl. Phys.***57** 06JE01 (Nagoya Univ.)
6. Kwangeun Kim *et al.*, *EDL*, vol. 40, no. 11, pp. 1796 – 1799, 2019 (U of W-M)
7. Noriharu Takada *et al* 2019 *Jpn. J. Appl. Phys.***58** SEEC02 (Nagoya Univ.)
8. Kwangeun Kim *et al* 2020 *Jpn. J. Appl. Phys.***59** 030908 (U of W-M)

Other ways of digital etching on GaN

- Ar plasma + KOH wet etching
  - RIE Ar plasma to damage III-Nitride surface
    - The damaged depth is determined by power, bias, etc
  - Then KOH is used to remove damaged surface
  - **Directional**
- Journal of ELECTRONIC MATERIALS, pp. 771 -776, Vol. 35, No. 4, 2006
- https://link.springer.com/content/pdf/10.1007/s11664-006-0137-6.pdf

My experiment

- Focus on **how to oxidize surface of GaN vertical structures**
- Test by **oxidization and following dilute HCl treatment**
- Two ways
  1. Asher for oxygen plasma (TRL Asher, 1000 W 5 min)
     - **Doesn't work**, maybe the power density is too low for GaN oxidization.
     - It also takes time waiting for pumping down and venting.
  2. Chemical solvents for oxidization
     - **First try**: RT 30% H_2O_2 (available in TRL)
       - **Doesn't work**
     - **Second try**: Mix 1 H_2SO_4 + 1 (30%) H_2O_2 (as Piranha, increased solvent temperature)
       - Seems working
       - Estimated total etching thickness on sidewalls is ~ 15 nm / 9 runs for GaN (semipolar planes on GaN pyramids with (0001) orientation)

Note: BOE was also tested for GaN surface oxide removal, but it does not work.

digital etching tested

- Semi-piranha (1 H_2SO_4 + 1 H_2O_2) + Dilute HCl (1 HCl + 3 H_2O)
  - Piranha for oxidation with increased solvent temperature
  - Dilute HCl for removing oxide

Step no.	Solvent	Time
1	Piranha (1 H_2SO_4 : 1 H_2O_2)	4 min
2	DI water	30 sec, then rinse with DI water
3	Dilute HCl (1 HCl : 3 H_2O)	2 min
4	DI water	30 sec, then rinse with DI water

1 cycle of DE

- **1 run = from step 1 to 4**
- **after 3 cycles => renew the piranha (i.e. renew the piranha after about 25 mins)**
- **Do total 9 runs => rinse with DI water => IPA and blow dry**

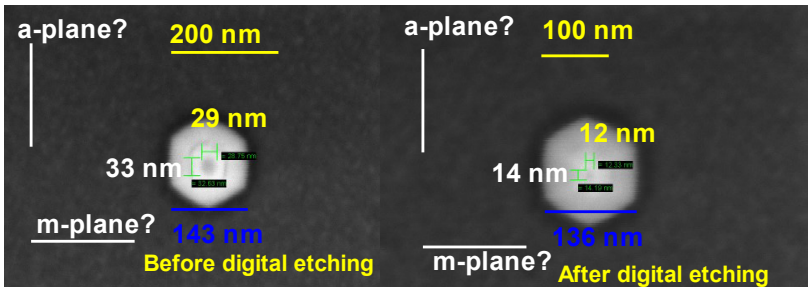
Note: the newest test changes the time of each step. The time duration of each step is changed to

(1) Piranha, 1 min
(2) DI water, 30 sec
(3) Dilute HCl, 1 min
(4) DI water, 30 sec

And the chemicals can be used for 6 cycles before renewal. I don't notice the difference on the etching rate per cycle.

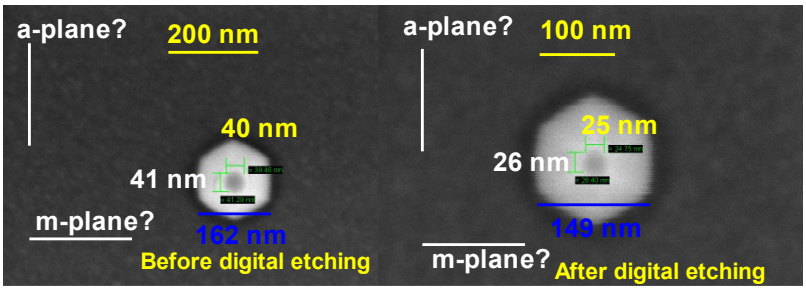
SEM images of digital etching test

• Piranha + Dilute HCl, 9 cycles

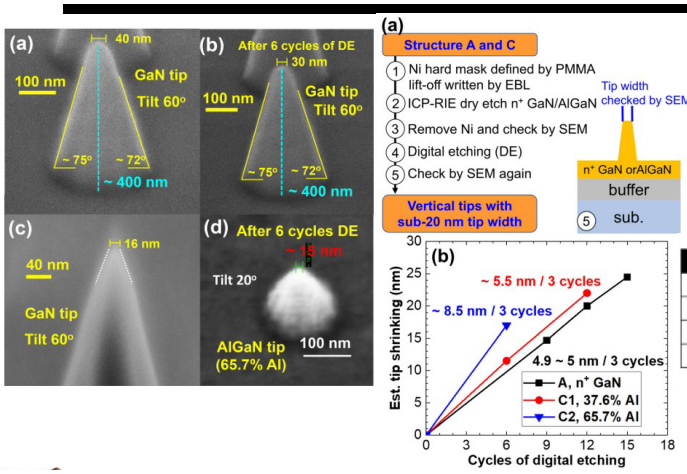


SEM images of digital etching test

• Piranha + Dilute HCl, 9 cycles



More test (in 2021)



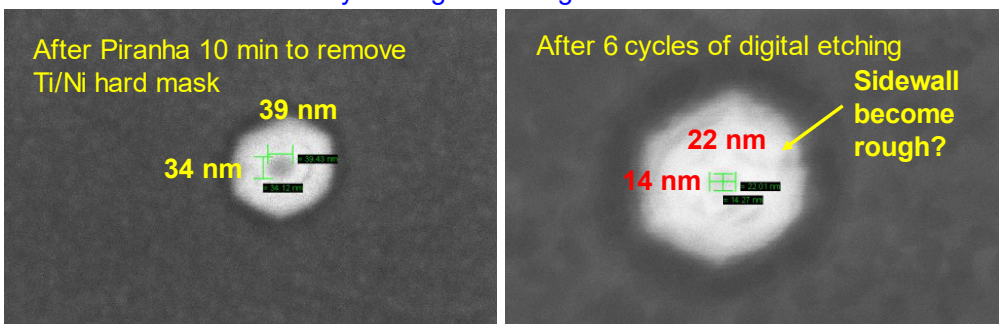
Our work
Pao-Chuan Shih ***et al***, Appl. Phys. Lett., vol. 120, no. 2, 2022, https://doi.org/10.1063/5.0074443

1 cycle of DE

Step no.	Solvent	Time
1	$1\ H_2SO_4 + 1\ 30\%\ H_2O_2$	4 min
2	DI water	30 sec, then DI water rinse
3	$1\ HCl + 3\ H_2O$	2 min
4	DI water	30 sec, then DI water rinse

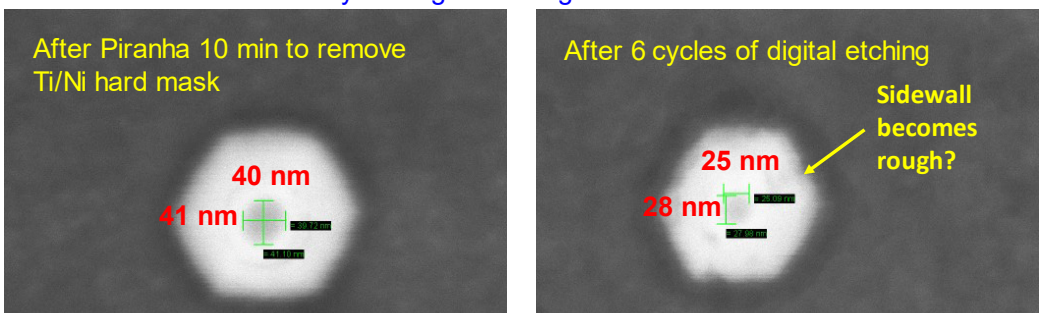
Digital etching on AlGaN pyramids

- R641, **AlGaN with 44 % Al**, on GaN template
- 45 nm design -> 35~40 nm after dry etching and hard mask removal
  -> 20~25 nm after 6 cycles digital etching



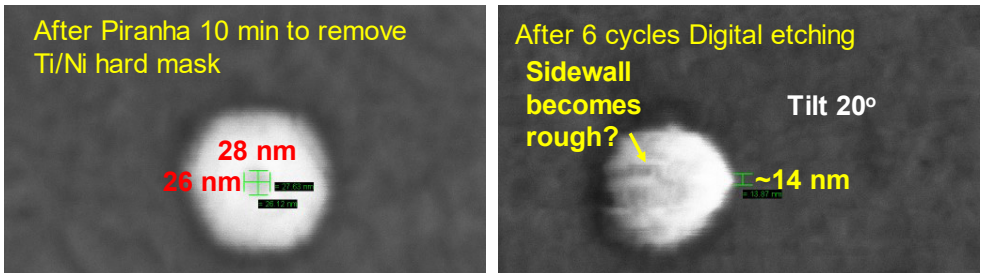
Digital etching on AlGaN pyramids

- R646, **AlGaN with 38 % Al**, on AlN template
- 45 nm design -> 38~40 nm after dry etching and hard mask removal
  -> 25~30 nm after 6 cycles digital etching



Digital etching on AlGaN pyramids

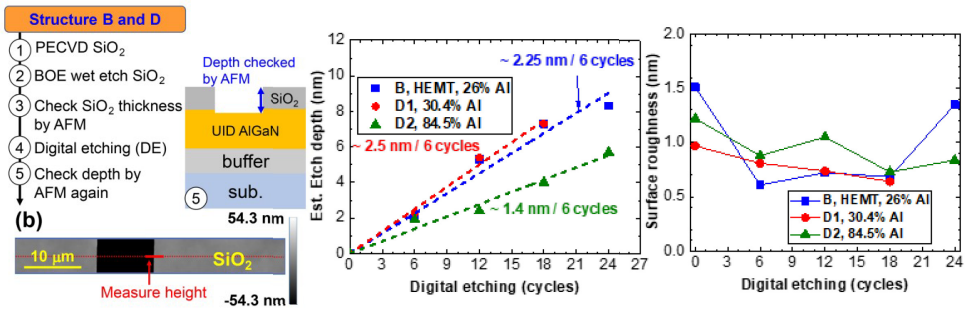
- R647, **AlGaN with 66 % Al**, on AlN template
- 45 nm design -> 26~31 nm after dry etching and hard mask removal
  -> ~15 nm? after 6 cycles digital etching



n^+ AlGaN materials are grown by MBE, provided by Prof. Alan Doolittle group at Georgia Institute of Technology

Experiments of DE on c-plane GaN and AlGaN

DE on c-plane AlGaN



Pao-Chuan Shih ***et al***, Appl. Phys. Lett., vol. 120, no. 2, 2022, https://doi.org/10.1063/5.0074443

UID AlGaN samples for DE experiments

Provided by Prof. Alan Doolittle group at Georgia Institute of Technology

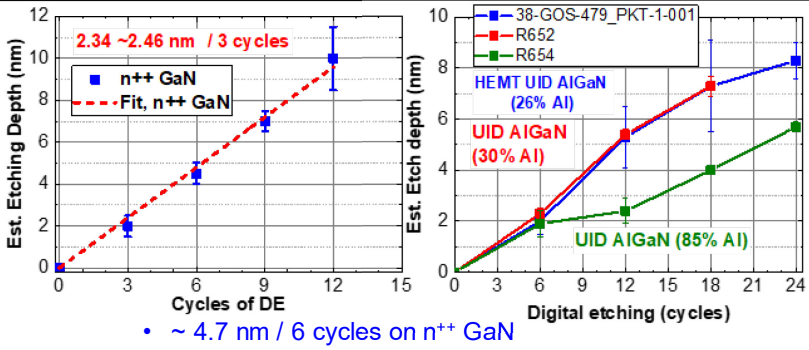
R652	
AlGaN (MME)	~100 nm
GaN (MME)	~200 nm
GaN (HVPE)	~4 microns
Sapphire	~430 microns

- Al% (XRD): 30.4 %
- AFM RMS Roughness: 0.631 nm

R654	
AlGaN (MME)	~100 nm
GaN (MME)	~200 nm
GaN (HVPE)	~4 microns
Sapphire	~430 microns

- Al% (XRD): 84.5 %
- AFM RMS Roughness: 0.731 nm

Etching rate on c-plane GaN and AlGaN



- ~ 4.7 nm / 6 cycles on n^{++} GaN
- ~ 2.5 nm / 6 cycles on UID $Al_{0.3}Ga_{0.7}N$
- ~ 1.4 nm / 6 cycles on UID $Al_{0.85}Ga_{0.15}N$

Experiments of ALE on GaN sidewalls

Concepts of Atomic Layer Etching (ALE)

- What is the difference between digital etching and ALE?

	Digital Etching	ALE
Self-limited etching	Yes	Yes
etching thickness	Linearly increased with number of runs	Linearly increased with number of runs
Etching thickness per run	**Varying**	**1 atomic layer**

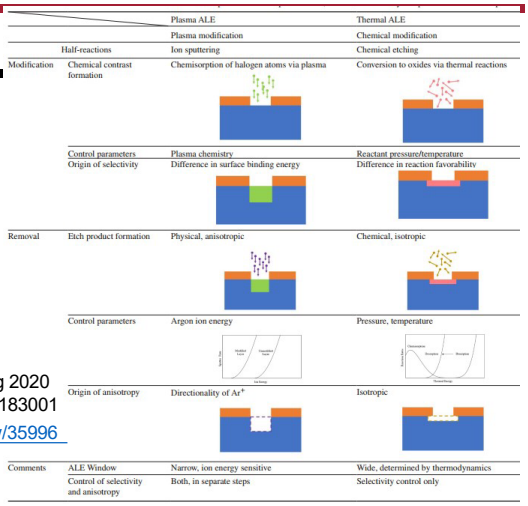
- Similar concepts in digital etching can be applied on ALE
  - Oxidization => oxide removal
  - Modified surface=> modified area removal

Types of ALE

- Two different approaches
- Plasma ALE (mostly anisotropic)
  - Lam
  - Oxford
  - Applied Materials
  - Hitachi High -Technologies
  - TEL
- Thermal ALE (isotropic)

Xia Sang and Jane P Chang 2020 *J. Phys. D: Appl. Phys.* **53** 183001

https://avssymposium.org/ALD2018/Sessions/Overview/35996

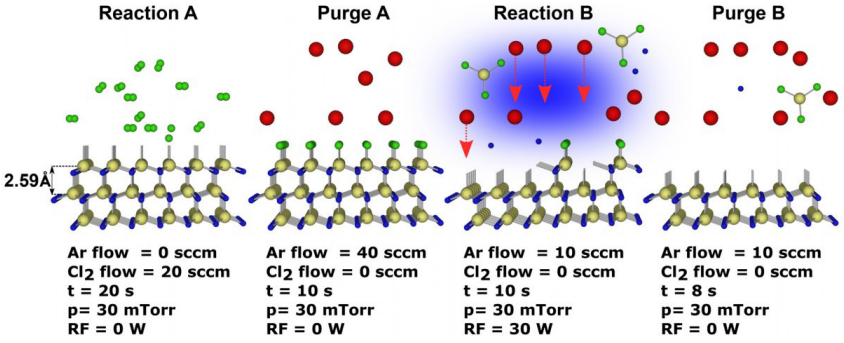


Plasma ALE on GaN

- Cl/Ar plasma based ALE (Conventional approach)
  - Cl plasma to modify surface
  - Ar plasma to remove modified region
    - The **bonding energy** between modified surface and pristine under layer is different.
- O_2/BCl_3 plasma based ALE (MIT Lincoln Lab)
  - O_2 plasma to oxidize surface
  - BCl_3 plasma to remove oxide
- Directional or isotropical?
  - Mostly directional in literature (similarly, for lateral HEMTs)
  - Isotropically etching should be possible

Plasma ALE on GaN (Cl/Ar)

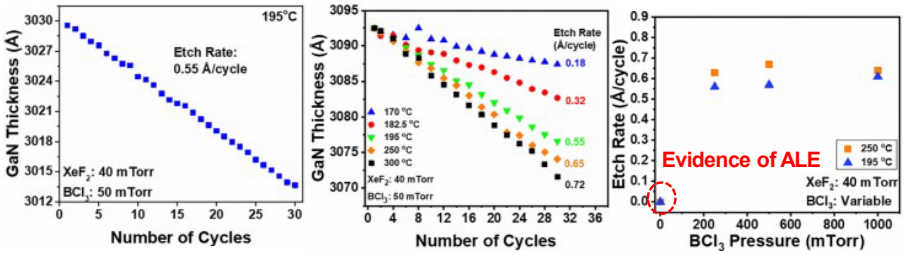
- Cl plasma reacts with GaN, then use Ar plasma to remove $GaCl_x$



Christoffer Kauppinen *et al*, *J. Vac. Sci. Technol. A* **35**, 060603 (2017)

Thermal ALE on GaN

- Only find one group published a thermal ALE on GaN in 2019 (& AlN in 2022)
  - Prof. Steven M. George, University of Colorado
  - XeF_2 reacts with GaN, then BCl_3 reacts with the GaF_x components
  - Fully thermal process, less-damage and more isotropic etching is expected



Nicholas R. Johnson *et al APL* **114** 243103 (2019) (U of Colorado)

ALE on different materials

Semi-conductors	Modification	Removal	Activation	Ref
Si	Cl_2	Ar	Plasma	[18]
Ge	Cl_2	Ar	Plasma	[19]
GaAs	Cl_2	Ar	Plasma	[20]
InP	Cl_2	Ne	Plasma	[10]
GaN	Cl_2	Ar	Plasma	[21] Aalto Univeristy
	XeF_2	BCl_3	Thermal	[16] University of Colorado
InGaAs	Cl_2	Ar	Plasma	[22]
	HF-pyridine	$AlCl(CH_3)_2$	Thermal	[17]
AlGaN	Cl_2	Ar	Plasma	[9]

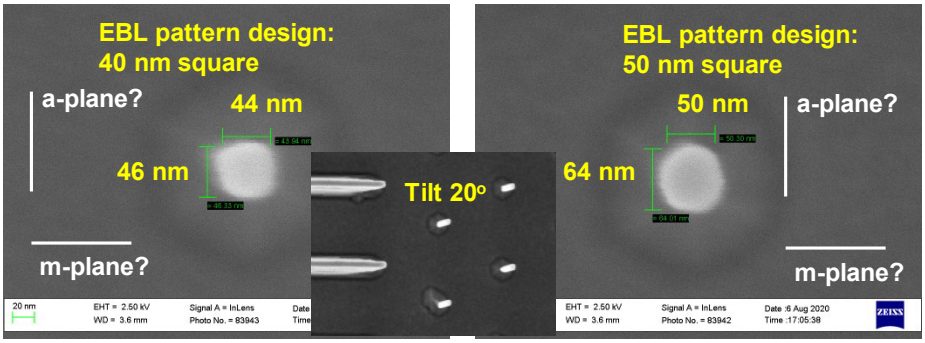
Xia Sang and Jane P Chang 2020
J. Phys. D: Appl. Phys. **53** 183001

ALE Test on GaN NWs (Lincoln Lab)

- ALE type of this test (info. from Jeff, Lincoln Lab)
  - **O_2 plasma** for oxidizing surface
  - **BCl_3 plasma** for removing oxide
  - **Plasma is generated by ICP , no biased power**
- Samples prepared
  - EBL with Ni lift -off
  - SAMCO Cl_2/BCl_3 dry etching, NW height about 280 nm
  - **Treated with RT 25% TMAH 20 min** after dry etching
  - Then Ni mask is removed by piranha

SEM of GaN NWs **before ALE test**

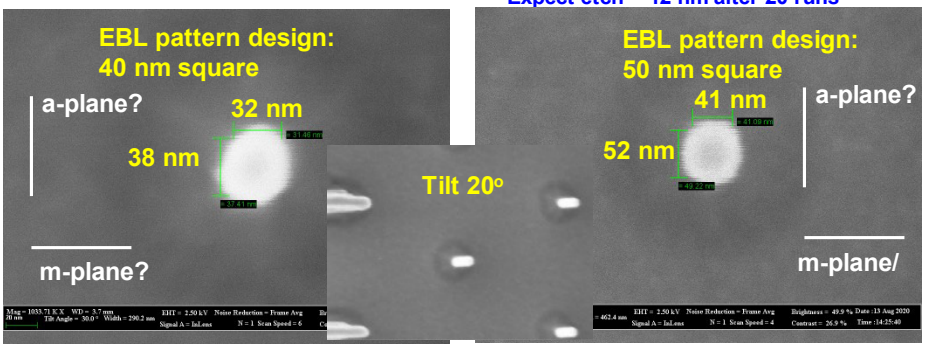
- With **RT** 25% TMAH 20 min



SEM of GaN NWs **after ALE test**

- 20 runs of ALE -> etch 8 ~ 14 nm.

In-plane lattice constant of GaN: 0.31 ~ 0.32 nm
Expect etch ~ 12 nm after 20 runs



Conclusion of ALE on GaN

- Mostly focus on vertical direction for AlGaN/GaN HEMTs
- Most ALE tools are based on plasma mechanism.
- Isotropically digital etching is possible

- Collaboration with MIT Lincoln Lab to test isotropic ALE
  - O_2/BCl_3 plamsa
  - It is possible since the plasma is not biased in this system

- Plasma or increased temperature is needed to provide enough energy for the process to happen.

The ALE experiments were helped by Dr. Jeff Daulton conducted at MIT Lincoln Lab.

This is the end of this appendix document.

Appendix C

Process flow and different failures of GaN SAGFEAs

Process flow and different failures of GaN SAGFEAs

Pao-Chuan Shih

This is the most updated version of process flow for the state-of-the-art GaN SAGFEAs reported in Chapter 4. This process flow was developed and approved in early 2022.

The Oxford-100 is no longer available, and the new PECVD tool for TEOS is not ready yet in 2023 Spring. The outsourcing to Lincoln Lab or Albany for TEOS deposition might be necessary.

The tool names here are mostly updated to the new name or to corresponding new tool in MIT.nano. This process flow serves as an example.

Process and Number	Process Step	Tool
1. Wafer Cleaning	10 min Piranha Clean	Acid-Etch-General-U10
2. EBL for Fin Formation	Spin coat PMMA-950 A4 750 rpm 6 sec -> 3,500 rpm 60 sec	Spinner-EBL
	Bake for 5 min at 180°C	Hot Plate
	EBL to write pattern for metal mask lift-off (device pitch ~ 600 nm)	elionix
	Evaporate 10 nm Ti / 30 nm Ni (Zero rotation)	Ebeam-Temescal-LL/ ebeamAu
	Place in acetone for lift-off (no ultrasonic)	Liftoff-L08
	Use SEM to check EBL pattern	SEM-Zeiss-Sigma300
	Remove residual PMMA by Ashing	Asher-Barrel-Thierry
3. Fin/NW Etch	Etch roughly 300 nm GaN with Recipe #45 GaN-High (~1'30") Or Recipe #46 GaN-Low (~5'30")	RIE-Cl2-SAMCO-200iP/ RIE-Mixed-SAMCO-230iP
	Use profilometer to check etch depth	Dektak-XT
4. Wafer Clean	Organic clean	Solvent-Clean-U06
	Remove Ni by Ni etchant TFB	Acid-Extended-U07
	10 min Piranha clean	Acid-Etch-General-U10
5. Digital Etching to shrink tip width	Check NWs by SEM	SEM-Zeiss-Sigma300
	Surface oxidization (1 H_2SO_4 + 1 30% H_2O_2, 4 min)	Acid-Etch-General-U10 (or L06)
	DI water soak 30 sec then rinse	Acid-Etch-General-U10
	37% HCl : H2O = 1:3, 2 min	Acid-Etch-General-U10
	DI water soak 30 sec then rinse	Acid-Etch-General-U10

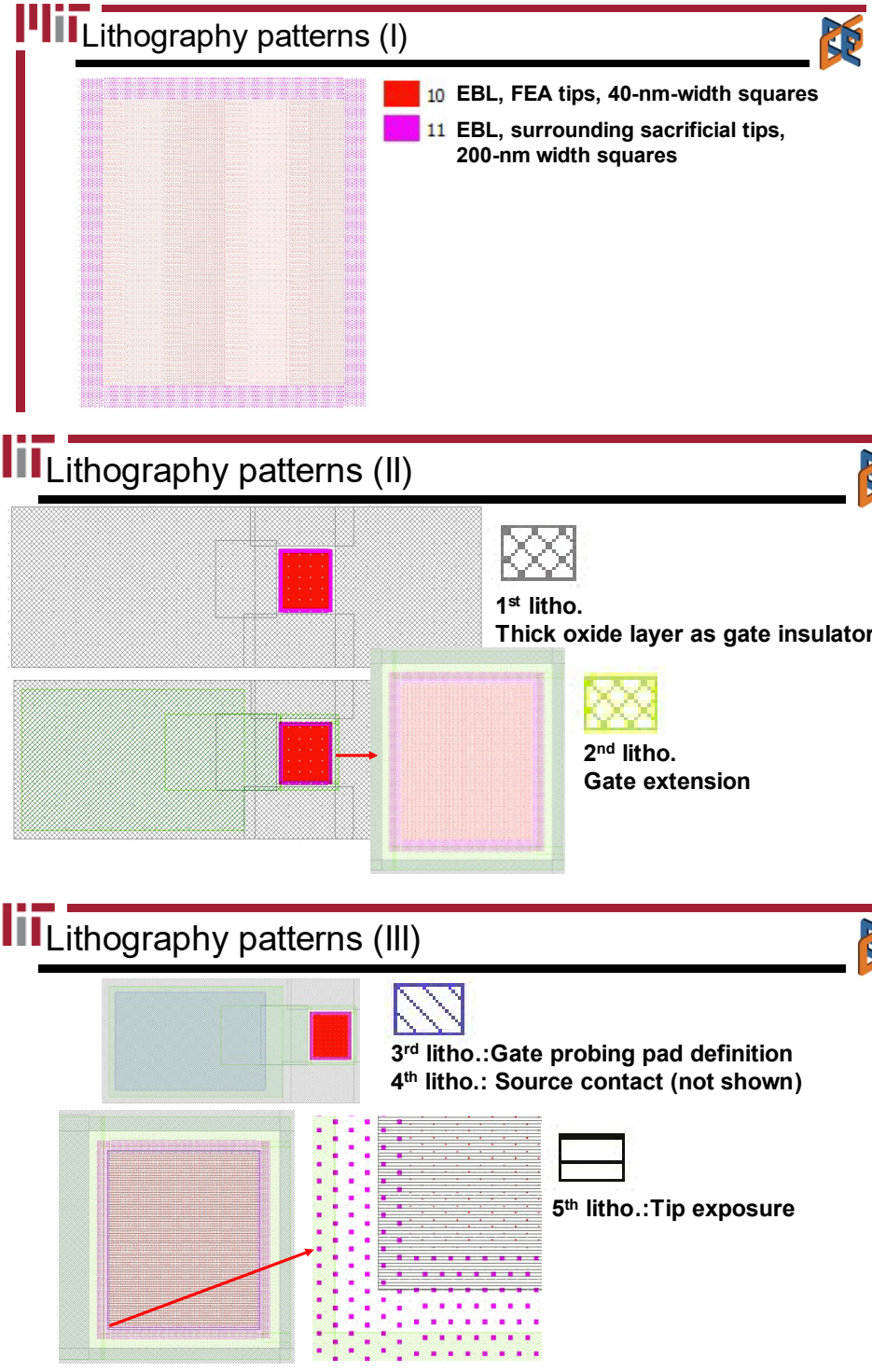
	Doing above four steps several times	
	Check NWs by SEM	SEM-Zeiss-Sigma300
6. Thick TEOS as gate insulator under pad region	400 nm TEOS deposition or SiO2 deposition	Oxford-100/ sts-CVD/ PECVD-SAMCO-PD220
	HMDS 1 min program	HMDS-YES-U10
	Spin coat AZ3312 (Default, 3,000 rpm 60 sec)	Spinner-Resist-U12
	Soft bake 100°C 1 min	Hotplate-Tower-U12
	Define etch region (375 nm laser) dose: 140 for Si sub. dose: 160 for sapphire sub.	DirectWrite-MLA-150-AirAF / DirectWrite-MLA-150-OptAF
	Post bake 110°C 1 min	Hotplate-Tower-U12
	Develop: AZ 300 MIF 80 sec -> DI water rinse	Develop-U12
	Hard bake 130°C 3 min	Hotplate-Tower-U12
	BOE etch TEOS (>130 nm/min)	Acid-Etch-General-U10
	Remove resist	Asher-Barrel-Thierry and Solvent-Clean-U06
7. Protection layer	2nd-gen. device: Sputter 35 nm Al Now: ALD 10 nm Al_2O_3 (100 cycle, 250°C)	Sputter-AJA-LL / ALD-Ozone
8. Gate stack deposition	200 nm TEOS deposition (or SiO2 deposition)	Oxford-100/ PECVD-STS-MMPLEX/ PECVD-SAMCO-P220
	Cr deposition (Sputtering) (100 nm)	Sputter-AJA-LL/ Sputter-AJA-ChamberLoad
9. TEOS planarization	1 μm TEOS deposition (thickness > device pitch)	Oxford-100
	Dry Etch TEOS down to ~ 300 nm (Etch ~ 700 nm) Recipe: SiO_2, ~ 125 nm /min, resist might be burnt; CF_4 + Ar are used	RIE-F-SAMCO-230iP/ RIE-Mixed-SAMCO-230iP
10. Define gate extension	HMDS 1 min program	HMDS-YES-U10
	Spin coat AZ3312 (Default, 3,000 rpm 60 sec)	Spinner-Resist-U12
	Soft bake 100°C 1 min	Hotplate-Tower-U12

	Define etch region (375 nm laser) dose: 140 for Si sub. dose: 160 for sapphire sub.	DirectWrite-MLA-150-AirAF / DirectWrite-MLA-150-OptAF
	Post bake 110°C 1 min	Hotplate-Tower-U12
	Develop: AZ 300 MIF 80 sec -> DI water rinse	Develop-U12
	Hard bake 130°C 4 min	Hotplate-Tower-U12
	Slowstrip-5 min	Asher-Barrel-Thierry
	Slow dry etch TEOS to expose Cr metal at top (Etch 350 ~ 400 nm) Recipe: SiO2-SEL (CHF_3 + CF_4) (RIE-F-SAMCO, rate 30~40 nm/min?) Recipe: SiO2-Sel (CF_4 + H_2) (RIE-Mixed-SAMCO, rate ~ 30 nm/min)	Oxford-100/ RIE-F-SAMCO-230iP/ RIE-Mixed-SAMCO-230iP
	Check by SEM	semZeiss/ SEM-Zeiss-Sigma300
	Remove resist by Organic solvent and ashing	Asher-Barrel-Thierry
11. Etch gate region	Dry etch Cr (Cl_2 + O_2-based chemistry) (SAMCO recipe, 75 ~ 85 nm/min on AJA-TRL Cr)	RIE-Mixed-SAMCO-230iP/ RIE-Cl2-SAMCO-200iP (as backup)
	Optional: Check by IV probe	***Waiting for new I-V probe station***
	Check by SEM	semZeiss/ SEM-Zeiss-Sigma300
12. Source Definition	HMDS 1 min program	HMDS-YES-U10
	Spin coat PMGI SF5 (750 rpm 10"-> 3500 rpm 60")	Spinner-PMGI-U12
	Bake 235°C 6 min	Hotplate-Tower-U12
	Spin coat AZ3312 (Default, 3,000 rpm 60 sec)	Spinner-Resist-U12
	Lithography: MLA **At least 180 mJ/cm^2**, 0 defocus, 375 nm	DirectWrite-MLA-150-AirAF / DirectWrite-MLA-150-OptAF
	Develop: AZ 300 MIF **90 sec** -> DI water rinse	Develop-U12
	Slowstrip-5 min	Asher-Barrel-Thierry

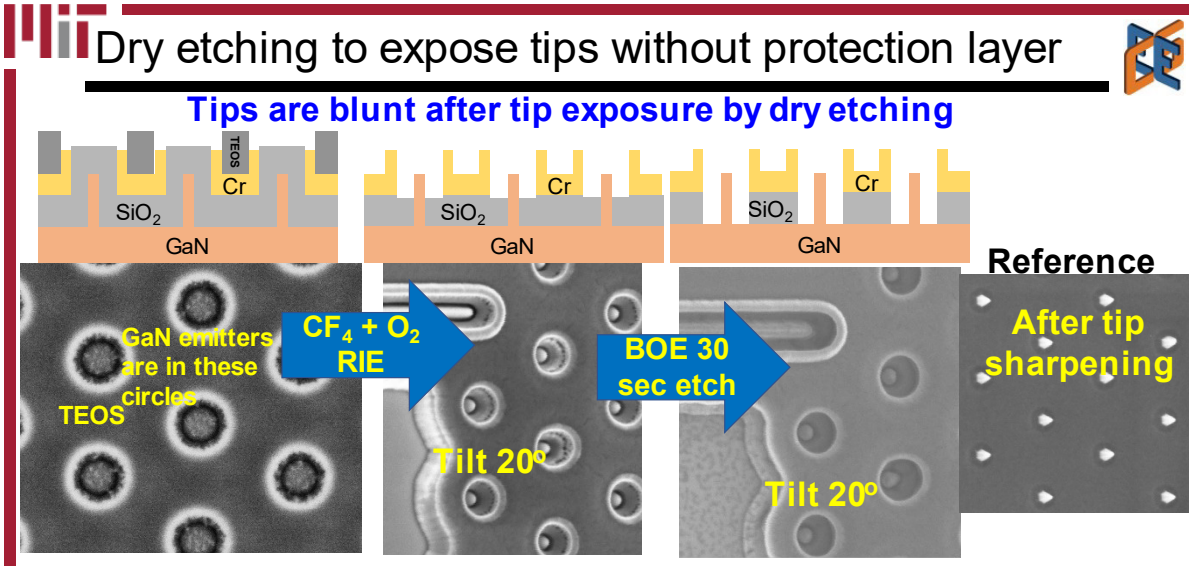
13. Source pad metal	BOE etch TEOS (~ 250 nm) to expose n+ layer surface for source contact (BOE etch TEOS ~ 200 nm/min)	Acid-Etch-General-U10
	Surface clean DI water dip 1 min	Acid-Etch-General-U10
	37% HCl : DI water = 1:3 dip for 1 min	Acid-Etch-General-U10
	DI water dip 1 min	Acid-Etch-General-U10
	Ti/Al/Ti/Au deposition (20 nm/ 100 nm/ 30 nm/ 50 nm)	Ebeam-Temescal-LL /ebeamAu/ebeamAJA
	Use NMP for lift-off	Liftoff-L08
	Remove residual by Ashing	Asher-Barrel-Thierry
14. Define gate pad	HMDS 1 min program	HMDS-YES-U10
	Spin coat PMGI SF5 (750 rpm 10"-> 3500 rpm 60")	Spinner-PMGI-U12
	Bake 235^{O}C 6 min	Hotplate-Tower-U12
	Spin coat AZ3312 (Default, 3,000 rpm 60 sec)	Spinner-Resist-U12
	Define gate pad region Lithography: MLA **At least 180 mJ/cm^2**, 0 defocus, 375 nm	DirectWrite-MLA-150-AirAF / DirectWrite-MLA-150-OptAF
	Develop: AZ 300 MIF **105 sec** -> DI water rinse	Develop-U12
	Slowstrip-5 min	Asher-Barrel-Thierry
15. Gate pad metal	BOE etch TEOS ~ 350 nm to expose Cr metal surface at pad area	Acid-Etch-General-U10
	Ni/Au deposition for gate pad (20 nm / 100 nm)	Ebeam-Temescal-LL /ebeamAu/ebeamAJA
	Use NMP for lift-off	Liftoff-L08
	Remove residual by Ashing	Asher-Barrel-Thierry
16. Expose GaN tips	HMDS 1 min program	HMDS-YES-U10
	Spin coat AZ3312 (Default, 3,000 rpm 60 sec)	Spinner-Resist-U12
	Soft bake 100^{o}C 1 min	Hotplate-Tower-U12
	Define device exposure region (375 nm laser) dose: 140 for Si sub. dose: 160 for sapphire sub.	DirectWrite-MLA-150-AirAF / DirectWrite-MLA-150-OptAF
	Post bake 110^{o}C 1 min	Hotplate-Tower-U12
	Develop: AZ 300 MIF 80 sec -> DI water rinse	Develop-U12

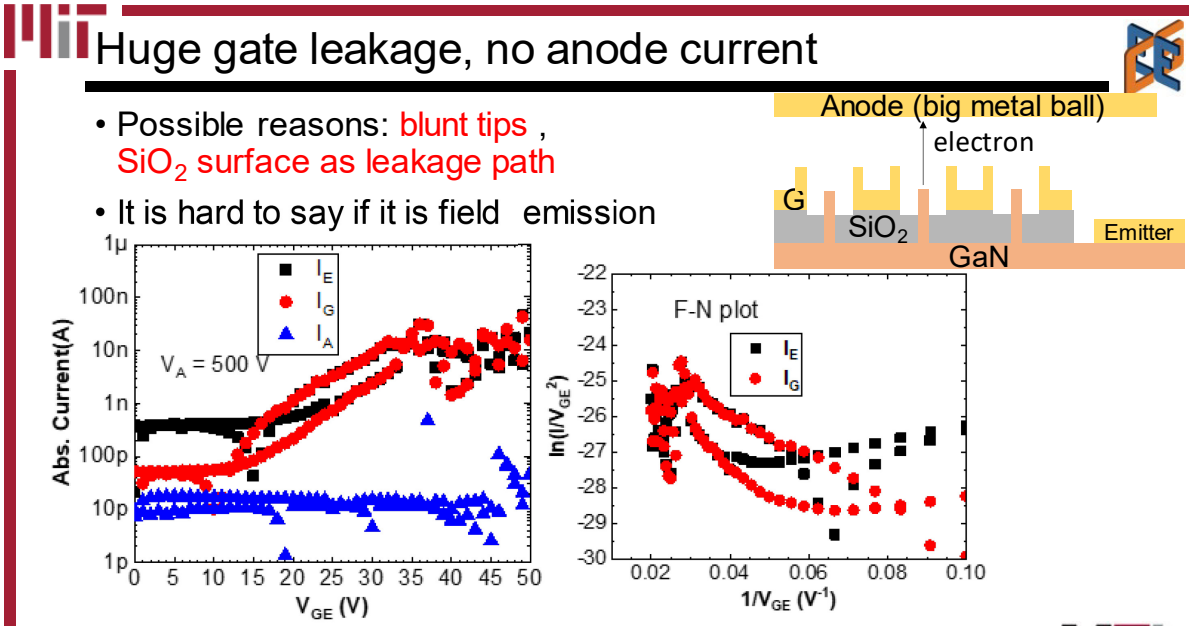
	Hard bake 130ºC 3 min	Hotplate-Tower-U12
	Slowstrip-5 min	Asher-Barrel-Thierry
	Dry etch TEOS ~ 200 nm (**Slow etch needed, no overetch, no high-power etch**) Recipe: SiO2-SEL (CHF_3 + CF_4) (RIE-F-SAMCO, rate 30~40 nm/min?) Recipe: SiO2-Sel (CF_4 + H_2) (RIE-Mixed-SAMCO, rate ~ 30 nm/min)	RIE-F-SAMCO-230iP/ RIE-Mixed-SAMCO-230iP
	Check by SEM	semZeiss/ SEM-Zeiss-Sigma300
	Quick BOE 15 ~ 20 sec, -> DI water soak -> DI water rinse -> IPA rinse -> blow dry	Acid-Etch-General-U10
	NMP clean with ultrasonic, then clean with DI water	Solvent-Clean-U06/ Asher-Barrel-Thierry
	Check by SEM	semZeiss/ SEM-Zeiss-Sigma300
	Optional: AZ300 MIF developer soak for etching residual Al_2O_3	Develop-U12
17. clean	DI water -> IPA -> blow dry	Solvent-Clean-U06
	Bake 130ºC 5 min	Hotplate-Tower-U12

Lithography patterns design of GaN SAGFEAs



GaN emitter tips without protection layer are damaged by plasma during tip exposure process

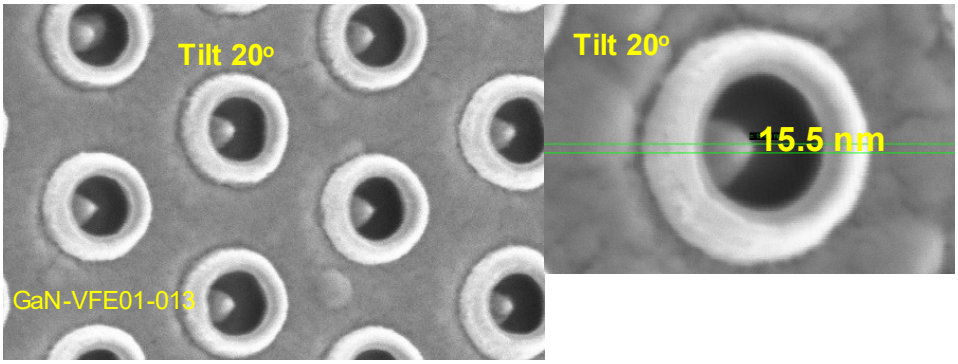




The failure of tip exposure with wet etching on GaN emitter tips without protection layer

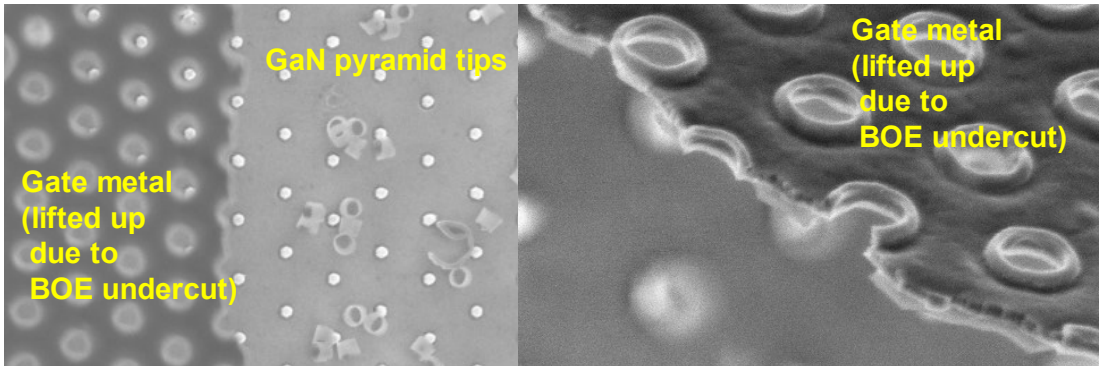
Long BOE (60 sec) to expose GaN tips

- RIE 5 min (etch 100 ~ 115 nm TEOS), then BOE 60 sec .
- GaN emitter tips are still sharp after tip exposure process.



Failure found after I-V measurement

- Most devices do not work.
- BOE undercuts TEOS too much. → Fully wet etching is problematic for this tip exposure step



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Appendix D

Summary of different processes used in this thesis work (by 2023/05/31)

Summary of different process used in this thesis work

Pao-Chuan Shih

A. Lithography

a. E-beam lithography (EBL)

PMMA with cold development for sub-50-nm patterns

- PMMA 950 A4:
  750 rpm 6 sec, => 4,000 rpm 60 sec
- Bake 180°C 4 min, cool down for few minutes
- Discharger4x:
  1,000 rpm 60 sec, => 3,000 rpm 10 sec

(1) Elionix (125 kV)

Writing:

- 2nA, base dose = 3,000 μC/cm^2 (for sub-200 nm)

Develop:

- DI water rinse 1 min (remove Discharger)
- 1 MIBK + 3 IPA, -10 ~ -12°C, 75 sec
- IPA rinse, blow dry

(2) HS-50 (50 kV)

Writing:

- 5nA, base dose = 2,000 μC/cm^2 (for sub-100 nm square)
- 100 nA, base dose = 1,600 μC/cm^2 (for above-um)
- 5 nA, base dose = 1,100 – 1,200 μC/cm^2
  (for dense lines, > 100 nm width)
- 5 nA, base dose = 1,300 μC/cm^2
  (for dense squares, >100 nm width)

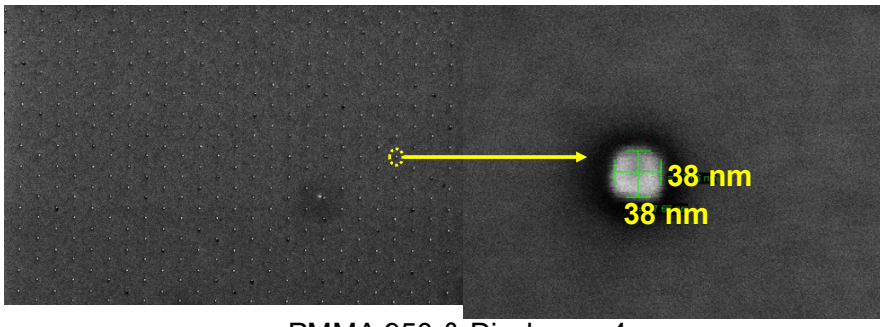
Develop:

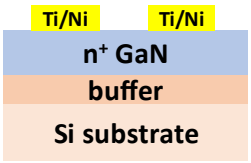
- DI water rinse 1 min (remove Discharger)
- 1 MIBK + 3 IPA, -10 ~ -12°C, 80 sec
- IPA rinse, blow dry

Note: All the dose for EBL mentioned here is the base dose. The real dose are corrected by Proximate Effect Correction (PEC) in beamer.

b. Photolithography: is summarized in the process flow.

Sub-50-nm square arrays defined by EBL





- PMMA 950 & Discharger4x

HS-50

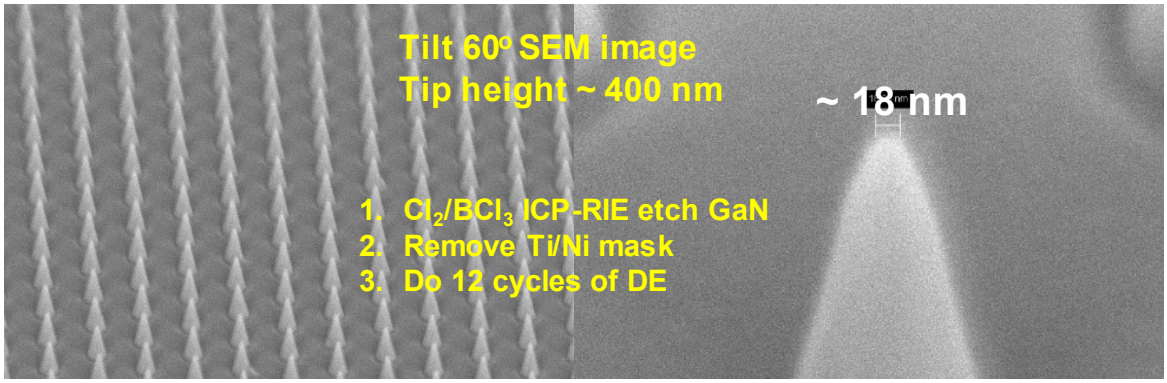
- 50 kV, 5 nA, **2,000 uC/cm² with PEC**

Metal lift-off

- 10 nm Ti/ 35 nm Ni, lift-off by NMP (soak over weekend)

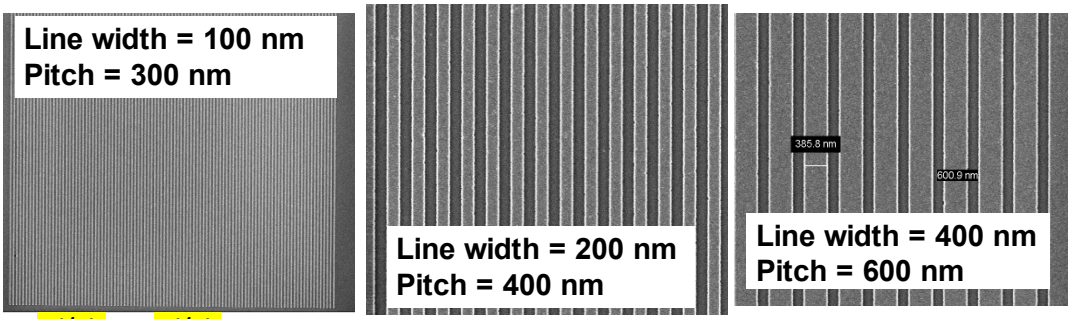
GaN FEA with sub-10-nm tip radius

- 150 x 150 tip arrays with sub -20 nm tip width (sub -10 nm tip radius)



Uniform FEAs with sub-10-nm tip radius can be reproducibly fabricated.

Dense patterns of Ti/Ni lines



- PMMA 950 & Discharger4x

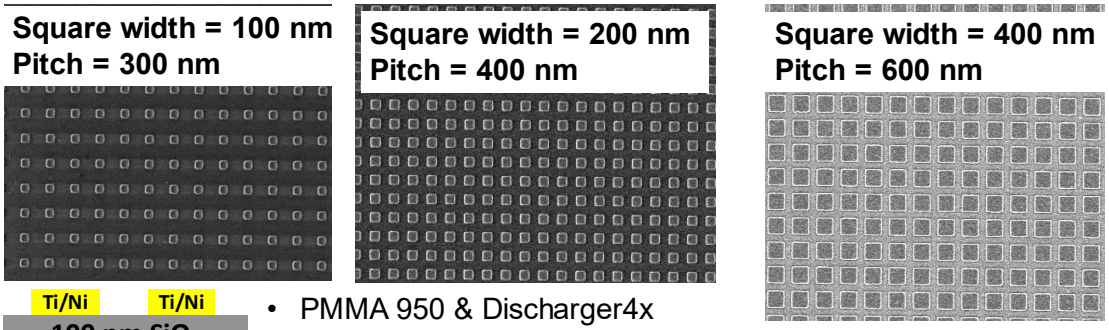
HS-50

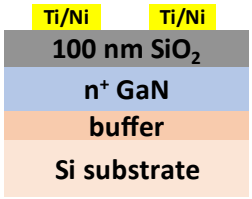
- 50 kV, 5 nA, **1100 uC/cm² with PEC**

Metal lift-off

- 10 nm Ti/ 35 nm Ni, lift-off by NMP (soak over weekend)

Dense patterns of Ti/Ni squares





- PMMA 950 & Discharger4x

HS-50

- 50 kV, 5 nA, **1300 uC/cm² with PEC**

Metal lift-off

- 10 nm Ti/ 35 nm Ni, lift-off by NMP (soak over weekend)

Note: Lift-off procedure:

1. Soak in NMP for over weekends
2. Use pipette to help remove most metal flakes
3. Transfer to new NMP
4. Low-power ultrasonic for ~ 1 min
5. Soak in DI water
6. DI water rinse
7. IPA rinse
8. Blow dry

B. Etch

a. Wet etching

Material	Etchant	Etch rate
PECVD SiO_2 or TEOS	BOE	≥ 150 nm / min
Sputtered Al	Al etchant type A	~ 50 nm / min
	AZ 300 MIF	> 20 nm / min
Ni	Ni etchant TFB	> 30 nm / min (not sure precise rate)
Cr	HCl, Cr etchant	Work, but not check rate
ALD Al_2O_3	AZ 300 MIF	~ 1 nm / min ?
	BOE	Work, but not check rate

b. Dry etching

- **RIE-Cl-SAMCO-200iP**

Recipe	Gas	Pressure	Power	Temp.	Etch rate
#45 (GaN-Fast)	15 Cl_2 + 5 BCl_3	0.6 Pa	ICP 150 W Bias 75 W	40°C	~ 200 nm / min (GaN)
#70 (Cr_low) (Backup)	20 Cl_2 + 3 O_2	1 Pa	ICP 400 W Bias 15 W	40°C	75-80 nm/min (Cr)
					~ 3 nm/min (SiO_2)
#46	15 Cl_2 + 5 BCl_3	0.6 Pa	ICP 150 W Bias 35 W	40°C	65-70 nm / min (GaN)

Note: Cr is prepared by sputtering.

Note: SiO_2 is deposited by PECVD.

TEOS has similar etching rate as SiO_2.

- **RIE-Mixed-SAMCO-200iP**

Recipe	Gas	Pressure	Power	Temp.	Etch rate
GaN-Fast	15 Cl_2 + 5 BCl_3	0.6 Pa	ICP 150 W Bias 75 W	20°C	~ 220 nm / min (GaN)
Cr_low	20 Cl_2 + 3 O_2	1 Pa	ICP 200 W Bias 25 W	20°C	> 55 nm/min (Cr)
Cr_fast	20 Cl_2 + 8 O_2	1 Pa	ICP 300 W Bias 100 W	20°C	> 100 nm/min (Cr)
SiO2	30 CF_4 + 60 Ar	1 Pa	ICP 400 W Bias 100 W	20°C	~ 130 nm / min (SiO_2)
SiO2-SEL	50 CF_4 + 10 H_2	2 Pa	ICP 100 W Bias 50 W	20°C	~ 30 nm / min (SiO_2)
SiO2-PC	50 CF_4 + 10 H_2	0.45 Pa	ICP 600 W Bias 50 W	20°C	~ 110 nm / min (SiO_2)
GaN-Vert (Mask: SiO_2)	20 Cl_2 + 20 Ar	4 Pa	ICP 600 W Bias 75 W	20°C	~380 nm / min? (GaN)
AlGaN (Mask: SiO_2)	20 BCl_3 + 5 Ar	0.5 Pa	ICP 500 W Bias 50 W	20°C	1st Step (BT): Breakthrough (10 sec for GaN) (1 min for high-Al AlGaN)
					~ 40 nm / min on SiO_2
	20 Cl_2 + 20 Ar	4 Pa	ICP 600 W Bias 75 W	20°C	2nd Step: Etch (330 nm/min for GaN?)
					~ 30 nm / min on SiO_2

Note: AlGaN recipe is still under development.

Note: GaN-Vert and AlGaN recipes cannot use Ni as etching mask since it deforms during the etching (on quartz carrier).

C. Deposition

a. PECVD

- **PECVD-SAMCO-PD220**

Recipe	Gas	Pressure	Power	Temp.	Dep. rate
HF SiO2	460 N_2 + 5 SiH_4	80 Pa	HF 100 W	350°C	53-55 nm / min
Low-stress SiN	200 N_2 + 5 NH_3 + 6 SiH_4	80 Pa	HF 120 W	350°C	31-33 nm / min
a-Si (150C)	8 SiH_4 + 92 Ar	60 Pa	HF 50 W	150°C	?

- **Oxford-100**

Recipe	Gas	Pressure	Power	Temp.	Dep. rate
TEOS-350C Zero Stress	300 O_2 + 50 TEOS/Ar	500 mTorr	HF 40 W (12 sec) LF 50 W (8 sec)	350°C	40-42 nm / min (< 10 mins)
					51-53 nm / min (> 15 mins)

Note: LF 50 W is used to compensate ~ 10 W reflection.
So the power of HF and LF is similar.
Note: Oxford-100 is no longer available.
But the new TEOS tool is not ready yet in Spring 2023.
So report Oxford-100 here only.

b. Sputter

- **Sputter-AJA-LL**

Recipe	Gas	Pressure	Power	Temp.	Dep. rate
Mo (Gun 2)	35 Ar	3 mTorr	100 or 150 W	RT	0.8 (100 W) 1.2 (150 W) Ang/sec
Cr (Gun 3)	35 Ar	3 mTorr	150 W	RT	1.2 Ang/sec
Al (Gun 4)	35 Ar	3 mTorr	RF 300 W	RT	1.4 Ang/sec

Note: Gun orientation is critical for dep. rate.
(Gun 2: ~12.45) (Gun 3: ~ 14.55)
Note: Gun 3 is changeable. Default is W.

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Appendix E

Conditioning procedure of III-Nitride SAGFEAs

Conditioning procedure of III-Nitride SAGFEAs

All the I-V measurements are conducted using Labview to control multiple Keithley source-measurement units (SMUs). The labview code was developed, provided, and helped by Dr. Girish Rughoobur in 2019-2021.

The conditioning procedure of III-Nitride SAGFEAs:

(1) Doing multiple I-V transfer characteristics sweeps. Start from the low bias condition and keep increasing the maximum voltage. The anode voltage is kept as constant. For example:

(i) V_{GE} = 0 V to 10 V, double sweep, 3 times
(ii) V_{GE} = 0 V to 15 V, double sweep, 3 times
(iii) V_{GE} = 0 V to 20 V, double sweep, 3 times
(iv) V_{GE} = 0 V to 25 V, double sweep, 3 times
…

Until the anode current turns on and starts becoming stable (i.e., the curves look similar in multiple sweeps).

(2) Doing reverse V_{GE} bias to check the gate leakage. Also start from the low reverse bias condition and keep increasing the maximum voltage. For example:

(i) V_{GE} = 0 V to -20 V, double sweep, 3 times
(ii) V_{GE} = 0 V to -25 V, double sweep, 3 times
(iii) V_{GE} = 0 V to -30 V, double sweep, 3 times
(iv) V_{GE} = 0 V to -35 V, double sweep, 3 times
(v) V_{GE} = 0 V to -40 V, double sweep, 3 times

If the gate leakage is low or only at noise level in these reverse bias conditions, the gate current observed in the transfer characteristics should be from the electron emission current from the emitter and is not from the leakage on or through the dielectric layer.

(3) Doing multiple I-V transfer characteristics sweeps again. The device is regarded conditioned if the I-V curves are stable and similar for multiple sweeps. For example:

(i) V_{GE} = 0 V to 40 V, double sweep, 3 times
(ii) V_{GE} = 0 V to 42 V, double sweep, 3 times
(iii) V_{GE} = 0 V to 44 V, double sweep, 3 times
(iv) V_{GE} = 0 V to 46 V, double sweep, 3 times
(v) V_{GE} = 0 V to 48 V, double sweep, 3 times
(vi) V_{GE} = 0 V to 50 V, double sweep, 3 times

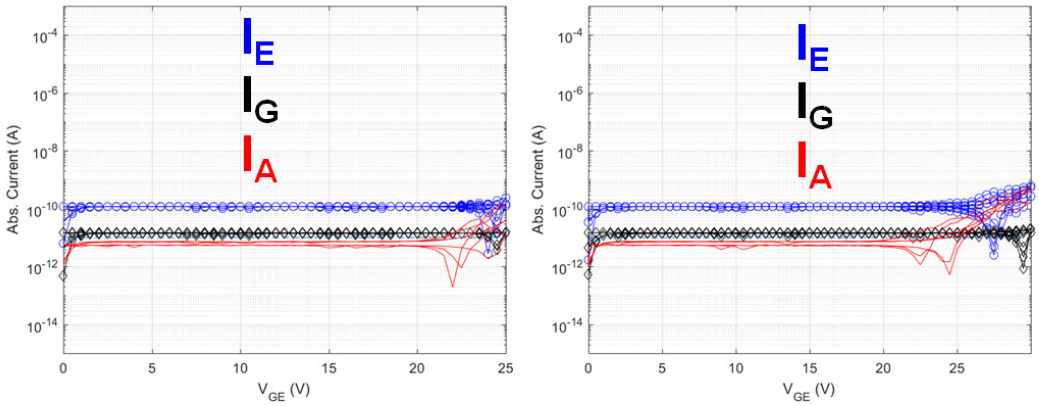
….

(4) If the device still works, do the output characteristics measurements.

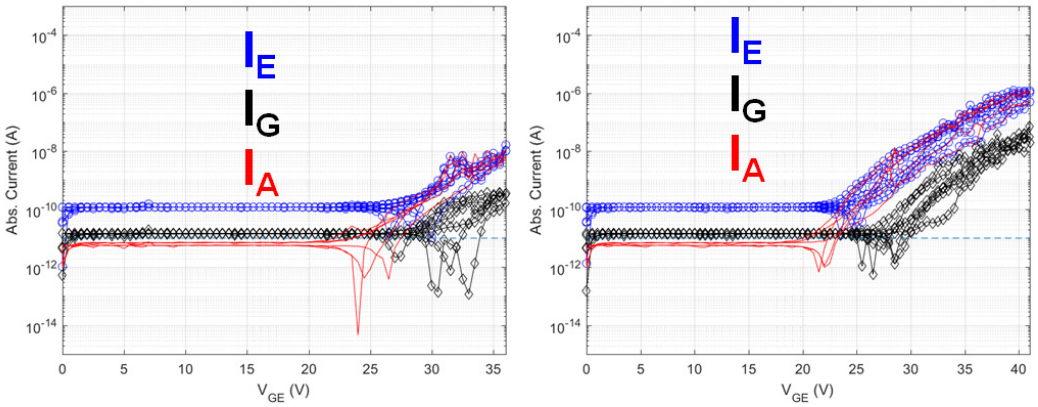
(5) Do the transfer characteristics again. Compare the results with (3) and (4).

The following is an example of a conditioning procedure of a GaN SAGFEA:

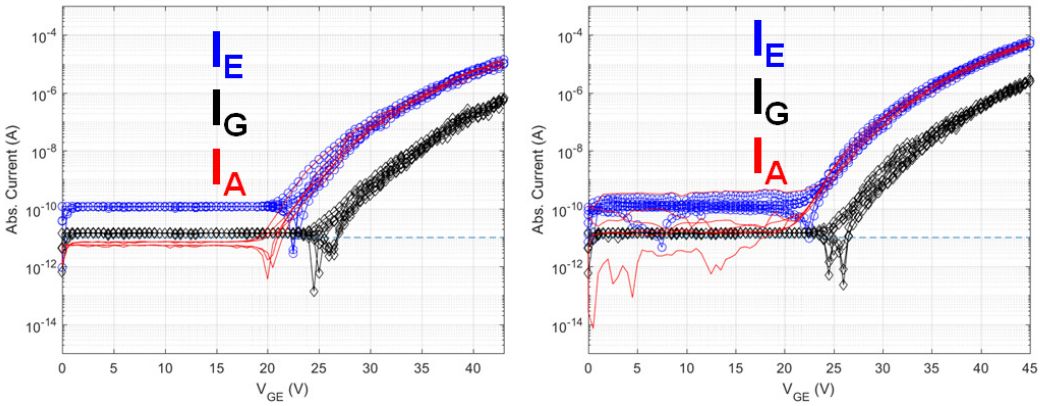
(1) Start conditioning, keep increasing the max bias voltage. Each plot has 3 I-V sweeps with double sweep directions.



Start seeing some current flowing through the anode.

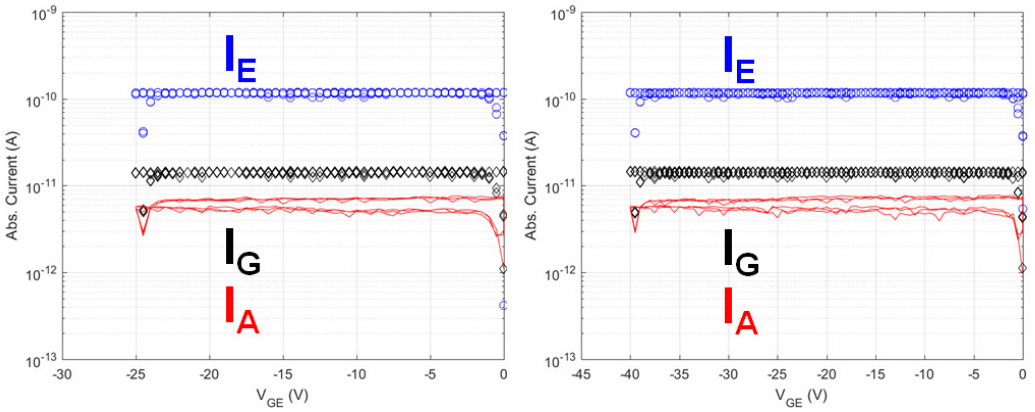


Currents are still noisy while the sweeps keep going on.



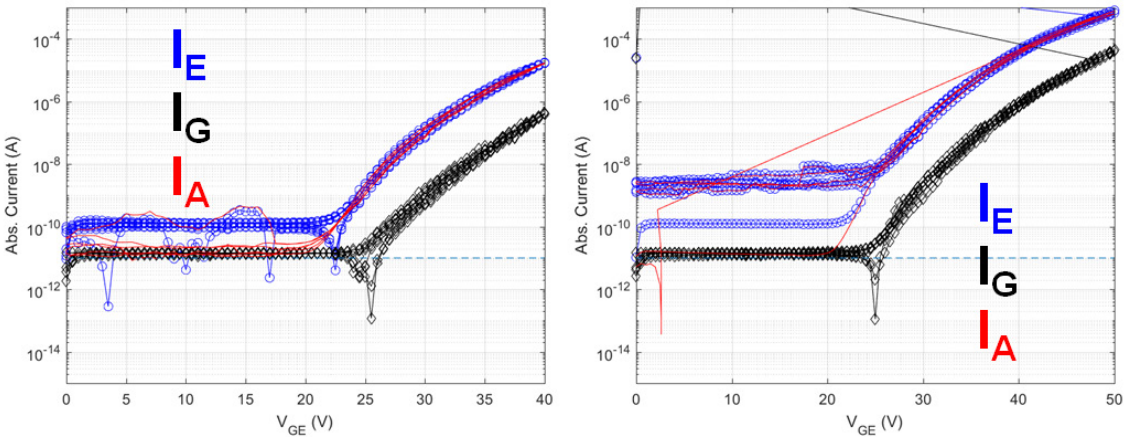
Currents become more stable and similar for multiple sweeps.

(2) Start reverse V_{GE} sweeping to check the gate leakage.



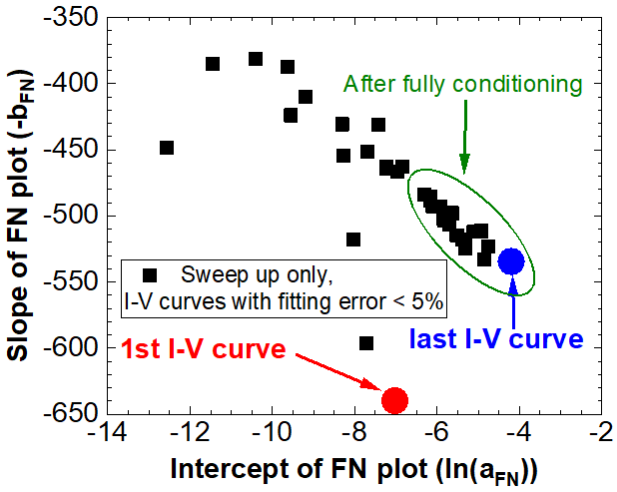
No gate leakage observed in reverse V_{GE} sweeps.

(3) Finish the conditioning.



Currents become more stable and similar for multiple sweeps.

Keep sweeping as needed until device breaks or enough experiments before the output characteristics or long-term stability test. This device suddenly breaks at the 3rd sweep of transfer characteristics when V_{GE} is swept down from 50 V to 0 V.



The Seppen-Katamuki (S-K) plot of different I-V sweeps during the conditioning procedure. It is clear that the F-N parameters converges to more stable values after the conditioning. The conditioning is important since the comparison between devices should be done based on the stable operation.

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Appendix F

Silvaco TCAD and Matlab codes used in this Thesis

Silvaco TCAD and Matlab codes used in this Thesis

(1) Silvaco code for generating SAGFEA structures (Generate a structure shown in Fig. 4.5(a))

```
# It is a 2D simulation with a cylindrical symmetry
# The symmetry axis is x = 0
#=== Define the simulation area ===#
set device_x1 = 0
set device_x2 = 0.3
set device_y1 = -0.51
set device_y2 = 0.31

#=== Define parameters for device structure ===#
#--- Set GaN region ---#
# GaN tip width = 20 nm (tip radius = 10 nm)
set GaN_tip_width = 0.02
# GaN tip height = 290 nm
set GaN_tip_height = 0.29
set GaN_tip_base = 0.138*$GaN_tip_height/0.29 + $GaN_tip_width

set GaN_tip_up_x1 = $device_x1
set GaN_tip_up_x2 = $GaN_tip_width/2
set GaN_tip_down_x1 = $device_x1
set GaN_tip_down_x2 = $GaN_tip_base/2
set GaN_planar_x1 = $device_x1
set GaN_planar_x2 = $device_x2
set GaN_tip_y1 = 0
set GaN_tip_y2 = $GaN_tip_y1 + $GaN_tip_height
set GaN_planar_y1 = $GaN_tip_y2
set GaN_planar_y2 = $device_y2

#--- Set Oxide region ---#
# Oxide thickness = 200 nm
set Oxide_thick = 0.2
# Oxide sidewall coverage = 150/180
set Oxide_sidewall_cover = 0.15/0.18
set Oxide_sidewall = $Oxide_thick * $Oxide_sidewall_cover
set Oxide_x1 = 0.22
set Oxide_x2 = $device_x2
set Oxide_y1 = $GaN_planar_y1 - $Oxide_thick
set Oxide_y2 = $GaN_planar_y1

#--- Set Gate metal region ---#
#Gate Metal part
set Gate_metal_overheight = 0.075
set Gate_metal_sidewall = 0.04
set Gate_metal_thick = 0.06
set Gate_ratio_x_to_y = 0.05/0.18
set Gate_metal_y0_location = $GaN_tip_up_x2 + $Oxide_sidewall
set Gate_metal_top_x1 = $Gate_metal_y0_location - $Gate_metal_overheight*$Gate_ratio_x_to_y
set Gate_metal_top_x2 = $Gate_metal_top_x1 + $Gate_Metal_sidewall
set Gate_metal_top_y = $GaN_tip_y1 - $Gate_metal_overheight
set Gate_metal_base_x1 = $Gate_metal_y0_location + ($Oxide_y1 - $GaN_tip_y1)*$Gate_ratio_x_to_y
```

```
set Gate_metal_base_x2 = $device_x2
set Gate_metal_base_y1 = $Oxide_y1 - $Gate_metal_thick
set Gate_metal_base_y2 = $Oxide_y1
set Gate_metal_base_middlex = $Gate_metal_top_x2 + ($Gate_metal_base_y1 -
$Gate_metal_top_y)*$Gate_ratio_x_to_y


#--- Set Anode region ---#
set electrode_thick = 0.01
set Anode_y1 = $device_y1
set Anode_y2 = $Anode_y1 + $electrode_thick
set Emitter_y1 = $device_y2 - $electrode_thick
set Emitter_y2 = $device_y2
set Anode_insulator_x1 = $Oxide_x1 + 0.03
set Anode_insulator_x2 = $Oxide_x2
set Anode_insulator_y1 = $Gate_metal_base_y1
set Anode_insulator_y2 = $Anode_y2
#=== Finish of defining parameters for device structure ===#

# Use devedit to define the structure and mesh #
go devedit
# Define whole device area
work.area x1=$device_x1 y1=$device_y1 x2=$device_x2 y2=$device_y2

# Define regions
region reg=1 mat=vacuum \
     polygon="$device_x1,$device_y1 $device_x2,$device_y1 $device_x2,$device_y2
$device_x1,$device_y2"
constr.mesh region=1 default

region reg=2 mat=GaN \
     polygon="$GaN_tip_up_x1,$GaN_tip_y1 $GaN_tip_up_x2,$GaN_tip_y1 \
               $GaN_tip_down_x2,$GaN_tip_y2 $GaN_planar_x2,$GaN_planar_y1 \
               $GaN_planar_x2,$GaN_planar_y2 $GaN_planar_x1,$GaN_planar_y2"
constr.mesh region=2 default

region reg=3 mat=Gold elec.id=1 name=gate \
     polygon="$Gate_metal_top_x1,$Gate_metal_top_y $Gate_metal_top_x2,$Gate_metal_top_y \
               $Gate_metal_base_middlex,$Gate_metal_base_y1 $Gate_metal_base_x2,$Gate_metal_base_y1 \
               $Gate_metal_base_x2,$Gate_metal_base_y2 $Gate_metal_base_x1,$Gate_metal_base_y2"
# Gate electrode
constr.mesh region=3 default

region reg=4 mat=oxide \
     polygon="$Oxide_x1,$Oxide_y1 $Oxide_x2,$Oxide_y1 $Oxide_x2,$Oxide_y2 $Oxide_x1,$Oxide_y2"
constr.mesh region=4 default

region reg=5 mat=oxide \
     polygon="$Anode_insulator_x1,$Anode_insulator_y1 $Anode_insulator_x2,$Anode_insulator_y1 \
               $Anode_insulator_x2,$Anode_insulator_y2 $Anode_insulator_x1,$Anode_insulator_y2"
constr.mesh region=5 default

region reg=6 mat=Gold elec.id=2 name=anode \
     polygon="$device_x1,$Anode_y1 $device_x2,$Anode_y1 $device_x2,$Anode_y2
$device_x1,$Anode_y2"
# Anode electrode
```

```
constr.mesh region=6 default

region reg=7 mat=Gold elec.id=3 name=emitter \
      polygon="$device_x1,$Emitter_y1 $device_x2,$Emitter_y1 $device_x2,$Emitter_y2
$device_x1,$Emitter_y2"
# Emitter electrode
constr.mesh region=7 default
# Finish define regions

# Define doping levels and doped regions
impurity id=1 reg=2 imp=Donors color=0xff0000 \
      peak.value=1e+19 ref.value=1000000000000 comb.func=Multiply
# Finish define doping

# Define Mesh
base.mesh height=0.01 width=0.01
#
bound.cond !apply max.slope=30 max.ratio=100 rnd.unit=0.001 line.straightening=1 align.points
when=automatic
#
imp.refine min.spacing=0.01
#
constr.mesh max.angle=90 max.ratio=300 max.height=1000 \
      max.width=1000 min.height=0.0001 min.width=0.0001
#
constr.mesh type=Semiconductor default
constr.mesh type=Insulator default
constr.mesh type=Metal default
constr.mesh type=Other default
constr.mesh region=1 default
constr.mesh region=2 default
constr.mesh region=3 default
constr.mesh region=4 default
constr.mesh region=5 default
constr.mesh region=6 default
Mesh Mode=MeshBuild
refine mode=both x1=0.0 y1=0.05 x2=0.05 y2=0.05
refine mode=both x1=0.0 y1=-0.025 x2=0.025 y2=0.025
refine mode=both x1=0.0 y1=-0.01 x2=0.01 y2=0.01
refine mode=both x1=$GaN_tip_up_x2*2/3 y1=$GaN_tip_y1-0.005 x2=$GaN_tip_up_x2*4/3
y2=$GaN_tip_y1+0.005
refine mode=both x1=$GaN_tip_up_x2*4/5 y1=$GaN_tip_y1-0.002 x2=$GaN_tip_up_x2*6/5
y2=$GaN_tip_y1+0.002
#
base.mesh height=0.01 width=0.01
# Finish define mesh

# Output the structures for later electronstatic simulation in atlas #
struct outfile="Tip_width_20nm_structure.str" master
# Finish
quit
```

(2) Silvaco code for electrostatic simulation of the SAGFEA structure (to extract the peak electric field on emitter tip)

```
# Set tip size = 20 nm for data saving
set Tip_size = 20
# Go to Atlas for electrostatic simulation
go atlas simflags="-P 20"
# Recall the structure file with a cylindrical symmetry
mesh infile="Tip_width_20nm_structure.str" cylindrical
# Set up metal contact condition
#gate = Cr, WF = 4.5 eV from wiki
contact name=gate workfun=4.5
#anode = W, WF = 4.32 ~ 5.32 eV from wiki, assume it as 4.5 eV
contact name=anode workfun=4.5
#emitter = ohmic contact on GaN, so assume WF = electron affinity of GaN = 3.8 eV
contact name=emitter workfun=3.8
# Recall models used in the simulation
models print srh numcarr=1 electrons temperature=300
# Did not simulate field-dependent mobility and saturation velocity here
#mobility material=gan albrct.n gansat.n
# Only change the electron affinity of GaN to 3.8 eV
material material=gan affinity=3.8
material material=vacuum affinity=0 permittivity=1.0 EG300=20.0
material material=oxide affinity=1.0 permittivity=3.9 EG300=10.0
# Determine what values will be outputted and can be plotted
output con.band val.band polar.charge band.par qss e.field charge e.mobility e.velocity
# Determine the method of convergence and only the electrons will be simulated (not consider holes)
method bicgst itlim=40 trap maxtrap=8 carriers=1 electrons
#=== Start simulating ===#
# Solve initial condition
solve init
save outf="Tip_$'Tip_size'nm_0V.str"
# Extract the electric field near the corner of GaN tip, which is the peak electric field in this structure
probe name=tip_field_x x=$Tip_size/2000+2e-5 y=-2e-5 Field Dir=0
probe name=tip_field_y x=$Tip_size/2000+2e-5 y=-2e-5 Field Dir=90
# Start sweeping voltages of different terminals with a loop function
loop steps = 17
solve init
#solve name=anode vfinal=$va vstep=5
assign name = va n.value=(5,10,15,20,25,30,35,40,45,50,60,70,100,125,150,175,200)
solve name=anode vfinal=$va vstep=5
save outf="Tip_$'Tip_size'nm_Vae=$'va'V_Vge=0V.str"
# Save the data of each simulated bias data point
log outfile="tip_field_Tip_$'Tip_size'nm_Vae=$'va'V.log"
solve name=gate vfinal=3 vstep=0.2
save outf="Tip_$'Tip_size'nm_Vae=$'va'V_Vge=$'vg'V.str"
solve name=gate vfinal=30 vstep=0.5
save outf="Tip_$'Tip_size'nm_Vae=$'va'V_Vge=30V.str"
log off
l.end
# Finish of the loop function
# Finish simulation
quit
```

Based on (1) and (2), the TCAD electrostatic simulation of a self-aligned-gated GaN emitter tip is simulated. Assuming all tips and surrounding structures are similar in the FEA, the device performance can then be estimated based on the simulation.

This is the end of Silvaco TCAD code

---

(3) Matlab code for estimating the field emission current of SAGFEAs with different work functions or tip sizes

```
% Estimate FEA current of varied work functions
clear all;
% Extracted from GaN FEA device results with assumption of 3.8 eV work
function
% values from GaN-VFE02-010, NW_DR_40nm_1-1 (the results in Fig. 4.23)
a_gan = exp(-4.028);
b_gan = 541.36;
% Constants of Field emission current from WKB approximation
A = 1.54E-6;
B = 6.83E+7;
work_function = 3.8;
% n++ GaN work function
beta = (0.95*B*(work_function)^(1.5))/b_gan;
% field factor, unit: cm^-1
alpha = (a_gan*1.1*3.8)/((A*(beta^2)))/exp((B*(1.44E-
7))/(work_function^0.5));
% emitting area, unit: cm^2
%=== Variables setting
phi = [3.8 2.9 2.2 1.5];
% work function array [GaN 20%ALGaN 40%AlGaN 60%AlGaN]
V_GE = 0.05:0.05:50; % Gate-Emitter voltage
% Calculation part
a = ((alpha * A * beta^2) ./ (1.1 .* phi)) .* exp((B * 1.44 * 10^-7) ./
(phi).^0.5);
b = 0.95 * B .* (phi).^1.5 / beta;
I = zeros(size(phi,2),size(V_GE,2)); % Set up Current array for each material
for m=1:size(I,1)
    for n=1:size(I,2)
        I(m,n) = a(m) * (V_GE(n))^2 * exp(-b(m) / V_GE(n));
    end
end
% I-V plot
semilogy(V_GE,I(1:4,:))
axis([0 50 1E-12 1])
grid on
xlabel('V_{GE} (V)')
ylabel('Emission Current (A)')
title('FEA Current Estimation')
```

```
% Estimate FEA current of varied tip radius
clear all;
% Extracted from GaN FEA device results with assumption of 3.8 eV work
function
% values from GaN-VFE02-010, NW_DR_40nm_1-1
a_gan = exp(-4.028);
b_gan = 541.36;
% Constants of Field emission current from WKB approximation
A = 1.54E-6;
B = 6.83E+7;
phi = 3.8;
% work function of n++ GaN
beta = (0.95*B*(phi)^(1.5))/b_gan;
% field factor, unit: cm^-1
alpha = (a_gan*1.1*phi)/((A*(beta^2)))/exp((B*(1.44E-7))/(phi^0.5));
% emitting area, unit: cm^2
tip_radius = (2.42E6 / beta)^(1/0.43934);
% Vavriables setting
tip_r = [tip_radius 6 5 4 3 2 1]; % tip radius array [8.9, 7, 6, 5, 4, 3 nm
radius]
beta_r = 2.42E6./(tip_r).^0.43934;
V_GE = 0.05:0.05:50; % Gate-Emitter voltage
% Calculation part
a = ((alpha * A .* beta_r.^2) ./ (1.1 .* phi)) .* exp((B * 1.44 * 10^-7) ./
(phi).^0.5);
b = 0.95 * B .* (phi).^1.5 ./ beta_r;
I = zeros(size(a,2),size(V_GE,2)); % Set up Current array for each material
for m=1:size(I,1)
    for n=1:size(I,2)
        I(m,n) = a(m) * (V_GE(n))^2 * exp(-b(m) / V_GE(n));
    end
end
% I-V plot
semilogy(V_GE,I(1:size(I,1),:))
axis([0 50 1E-12 1])
grid on
xlabel('V_{GE} (V)')
ylabel('Emission Current (A)')
title('FEA Current Estimation')
```

(4) Matlab code for plotting measured I-V data and Fowler-Nordheim (F-N) parameters extraction

The matlab codes here are developed with Dr. Girish Rughoobur's help, especially on the F-N parameters extraction part.

```
% Plot I-V data from measurement results
%(stored in .dat file output from labview)
clear;
% Read data from .dat file
d = dir('*.dat');
for i = 1:size(d,1)
 files{i} = d(i).name;
 A = importdata(files{i})';
% Extract separate values
 time = A(1,:);
 V_E = A(2,:);
 V_G = A(3,:);
 V_A = A(4,:);
 I_E = A(5,:);
 I_G = A(6,:);
 I_A = A(7,:);
 Pressure = A(8,:);
% Data preparation for plot
 V_GE = V_G - V_E;
 abs_I_E = abs(I_E);
 abs_I_G = abs(I_G);
 abs_I_A = abs(I_A);
% Plot data
 figure(i)
 semilogy(V_GE,abs_I_E,'bo-',V_GE,abs_I_G,'kd-',V_GE,abs_I_A,'r')
 hold on
 axis([0 max(V_GE) 1E-15 1E-3])
 grid on
 xlabel('V_{GE} (V)')
 ylabel('Abs. Current (A)')
 plot([0 max(V_GE)], [1E-11 1E-11],'--')
 files_name=strrep(char(files(i)),'.dat','');
 print(gcf,'-dtiff',strcat(files_name,'.tiff'));
end

% %For separating sweep up and down curves
% V_GE_up = [];
% V_GE_down = [];
% I_E_up = [];
% I_E_down = [];
% I_G_up = [];
% I_G_down = [];
% I_A_up = [];
% I_A_down = [];
%
% % extract out for sweep-up-only
% for n = 1:size(A,2)
%     if (n>=2 && n<size(A,2))
%         if (V_GE(n)>V_GE(n-1) && V_GE(n)>0)
```

```
%             V_GE_up = [V_GE_up V_GE(n)];
%             I_E_up = [I_E_up abs_I_E(n)];
%             I_G_up = [I_G_up abs_I_G(n)];
%             I_A_up = [I_A_up abs_I_A(n)];
%         elseif (V_GE(n)*V_GE(n-1) <= 0 && V_GE(n+1)>0)
%             V_GE_up = [V_GE_up 0 V_GE(n)];
%             I_E_up = [I_E_up 0 abs_I_E(n)];
%             I_G_up = [I_G_up 0 abs_I_G(n)];
%             I_A_up = [I_A_up 0 abs_I_A(n)];
%             V_GE_down = [V_GE_down 0 V_GE(n)];
%             I_E_down = [I_E_down 0 abs_I_E(n)];
%             I_G_down = [I_G_down 0 abs_I_G(n)];
%             I_A_down = [I_A_down 0 abs_I_A(n)];
%         else
%             V_GE_down = [V_GE_down V_GE(n)];
%             I_E_down = [I_E_down abs_I_E(n)];
%             I_G_down = [I_G_down abs_I_G(n)];
%             I_A_down = [I_A_down abs_I_A(n)];
%         end
%     else
%         V_GE_up = [V_GE_up V_GE(n)];
%         I_E_up = [I_E_up abs_I_E(n)];
%         I_G_up = [I_G_up abs_I_G(n)];
%         I_A_up = [I_A_up abs_I_A(n)];
%     end
% end
%semilogy(V_GE_up,I_E_up,'ro',V_GE_up,I_G_up,'bo',V_GE_up,I_A_up,'ko')
```

```
% Fowler-Nordheim parameters extraction
clear;
p = [];
c = [];
d = dir('*.dat');
z = [];
r2 = [];
i = 1;
sweep_time = 6;
% Fitmax is for F-N plot fitting, it is important to check this value
fitmax = 0.036;
% This is the value of the x-axis of the F-N plot
for i = 1:size(d,1)
for sweep =1:sweep_time
 files{i} = d(i).name;
% z= [z; dx.data(3)];
 data = importdata(files{i});
% ldata = data.data;
 vge = abs(data(:,3)-data(:,2));
 ia = abs(data(:,7));
 zeroin = find(vge<0.1);
 splice = 1:zeroin(3)/2;
 splice2 = splice(end):zeroin(2);
 spliceint = splice2(end):zeroin(4);
 splice3 = 1+spliceint(1:size(spliceint,2)/2);
 splice4 =  splice3(end):spliceint(end);
 spliceint2 = splice4(end):zeroin(6);
 splice5 = 1+spliceint2(1:size(spliceint2,2)/2);
```

```
 splice6 =  splice5(end):spliceint2(end);
 inits = [size(splice,2); size(splice2,2); size(splice3,2); size(splice4,2);
size(splice5,2); size(splice6,2)];
 inew = zeros(max(inits),6);
 inew(:) = NaN;
 inew(1:size(splice,2),1) = ia(splice);
 inew(1:size(splice2,2),2) = flipud(ia(splice2));
 inew(1:size(splice3,2),3) = ia(splice3);
 inew(1:size(splice4,2),4) = flipud(ia(splice4));
 inew(1:size(splice5,2),5) = ia(splice5);
 inew(1:size(splice6,2),6) = flipud(ia(splice6));

 %imean = mean([inew(:,1) inew(:,3) inew(:,5)],2,'omitnan');
 %imean = mean([inew(:,2) inew(:,4) inew(:,6)],2,'omitnan');
%
imean = inew(:,sweep);
vgefit = vge(splice);
 fnx= 1./vgefit;
 fny=log(imean./vgefit.^2);
 maxcheck = find(fnx<fitmax);
% end
% mincheck = find(fny(maxcheck)==min(fny(maxcheck)));
% fitin2 = (mincheck+maxcheck(1)+5):size(fnx,1);
% fitin = find(diff(fny(fitin2))>0.02);
% fitin = fitin+min(fitin2);
% %fitin= mincheck:size(fnx,1);
 [P S] = polyfit(fnx(maxcheck),fny(maxcheck),1);
     p = [p; P(1)];
     c = [c; P(2)];
 figure(i)
plot(fnx(maxcheck),fny(maxcheck),'bo','MarkerFaceColor','b','MarkerSize',4);
 hold on
 plot(fnx(maxcheck),polyval(P,fnx(maxcheck)), 'k')
%
 SSresid = sum((fny(maxcheck)-polyval(P,fnx(maxcheck))).^2);
 SStotal = (length(fny(maxcheck))-1) * var(fny(maxcheck));
 r2 =[r2; 1-SSresid/SStotal];
 files_name=strrep(char(files(i)),'.dat','_FN_');
 print(gcf,'-dtiff',strcat(files_name,'.tiff'));
end
end
 %p = p(2:end);
 %c = c(2:end);
 %z = z(2:end);
 %r2 = r2(2:end);
results = [z p c r2];
% Prepare for exporting data
sweep_type = string({'up','down'});
sweep_data =[];
file_temp = string(files);
file_name = [];
type_name = {'sweep_name','1st/2nd/3rd sweep','Up or Down sweep','-
bfn','afn','error'}';
for i=1:size(d,1)
    for j=1:sweep_time
        if mod(j,2) == 1
```

```
            file_name = [file_name file_temp(i)];
            sweep_data = [sweep_data ; (j+1)/2 sweep_type(1)];
        else
            file_name = [file_name file_temp(i)];
            sweep_data = [sweep_data ; j/2 sweep_type(2)];
        end
    end
end
sweep_data = sweep_data';
data_name = [ type_name(1:3)'; [file_name ; sweep_data]'];
results_cell = [type_name(4:6)'; num2cell(results)];
Final_Fitting_results = [data_name' ; results_cell']';
% cell2csv.m is used to export csv file
cell2csv('FN-fitting-results.csv',Final_Fitting_results);
```

---

(5) Matlab code for simulating different tip-size-variation conditions for the GaN NW SAGFEA (calculated results reported in chapter 4)

```
% Estimate FEA current of varied tip radius distribution
clear all;
% Extracted from GaN FEA device results with assumption of 3.8 eV work
function
% values from GaN NWs (2020 DRC) (data reported in chapter 3)
a_gan = exp(-12.47);
b_gan = 577.96;
% Constants of Field emission current from WKB approximation
A = 1.54E-6;
B = 6.83E+7;
phi = 3.8;
beta = (0.95*B*(phi)^(1.5))/b_gan;
% field factor, unit: cm^-1
alpha = (a_gan*1.1*phi)/((A*(beta^2)))/exp((B*(1.44E-7))/(phi^0.5));
% emitting area, unit: cm^2
%
%
% First tip variation distribution
tip_radius = (5.355E6 / beta)^(1/0.70735);
alpha_tip = alpha / (50*50);
sigma = 0.3;
delta = 0.01;
tip_range = [tip_radius - 5*sigma : delta : tip_radius + 5*sigma];
tip_distr = normpdf(tip_range,tip_radius,sigma)*delta;
beta_r_range = 5.355E6./(tip_range).^0.70735;
V_GE = 0.05:0.05:80; % Gate-Emitter voltage
phi = 3.8;
a_range = ((alpha_tip * A .* beta_r_range.^2) ./ (1.1 .* phi)) .* exp((B *
1.44 * 10^-7) ./ (phi).^0.5);
b_range = 0.95 * B .* (phi).^1.5 ./ beta_r_range;
I_portion = zeros(size(a_range,2),size(V_GE,2));
for n=1:size(I_portion,2)
```

```
    for m=1:size(I_portion,1)
        I_portion(m,n) = a_range(m) * (V_GE(n))^2 * exp(-b_range(m) /
V_GE(n));
    end
end
I = zeros(1,size(V_GE,2));
for n=1:size(I_portion,2)
    for m=1:size(I_portion,1)
        I(1,n) = I(1,n) + tip_distr(m) * I_portion(m,n);
    end
end
delta_I = zeros(1,size(V_GE,2));
Sensitivity = zeros(1,size(V_GE,2));
for n=1:size(I_portion,2)
    for m=1:size(I_portion,1)
        delta_I(1,n) = delta_I(1,n) + tip_distr(m) * abs(I_portion(m,n)-
I(1,n));
    end
    if I(n)>0
        Sensitivity(1,n)=delta_I(1,n)/I(1,n);
    end
end
I = I * 50*50;
%
%
% Second tip variation distribution
tip_radius_2 = 17;
sigma_2 = 2.4;
delta_2 = 0.01;
tip_range_2 = [tip_radius_2 - 5*sigma_2 : delta_2 : tip_radius_2 +
5*sigma_2];
tip_distr_2 = normpdf(tip_range_2,tip_radius_2,sigma_2)*delta_2;
beta_r_range_2 = 5.355E6./(tip_range_2).^0.70735;
a_range_2 = ((alpha_tip * A .* beta_r_range_2.^2) ./ (1.1 .* phi)) .* exp((B
* 1.44 * 10^-7) ./ (phi).^0.5);
b_range_2 = 0.95 * B .* (phi).^1.5 ./ beta_r_range_2;
I_portion_2 = zeros(size(a_range_2,2),size(V_GE,2));
for n=1:size(I_portion_2,2)
    for m=1:size(I_portion_2,1)
        I_portion_2(m,n) = a_range_2(m) * (V_GE(n))^2 * exp(-b_range_2(m) /
V_GE(n));
    end
end
I_2 = zeros(1,size(V_GE,2));
for n=1:size(I_portion_2,2)
    for m=1:size(I_portion_2,1)
        I_2(1,n) = I_2(1,n) + tip_distr_2(m) * I_portion_2(m,n);
    end
end
delta_I_2 = zeros(1,size(V_GE,2));
Sensitivity_2 = zeros(1,size(V_GE,2));
for n=1:size(I_portion_2,2)
    for m=1:size(I_portion_2,1)
        delta_I_2(1,n) = delta_I_2(1,n) + tip_distr_2(m) *
abs(I_portion_2(m,n)-I_2(1,n));
    end
    if I_2(n)>0
```

```
        Sensitivity_2(1,n)=delta_I_2(1,n)/I_2(1,n);
    end
end
I_2 = I_2 * 50*50;
figure(3)
semilogy(V_GE,I_2)
axis([0 max(V_GE) 1E-12 1])
grid on
xlabel('V_{GE} (V)')
ylabel('Emission Current per tip (A)')
title('FEA Current Estimation based on GaN NW FEA (2020 DRC)')
figure(4)
plot(V_GE,I_2)
axis([0 max(V_GE) 0 2E-5])
grid on
xlabel('V_{GE} (V)')
ylabel('Emission Current per tip (A)')
title('FEA Current Estimation based on GaN NW FEA (2020 DRC)')
%
%
% Third tip variation distribution
tip_radius_3 = 19.3;
sigma_3 = 3.1;
delta_3 = 0.01;
tip_range_3 = [tip_radius_3 - 5*sigma_3 : delta_3 : tip_radius_3 +
5*sigma_3];
tip_distr_3 = normpdf(tip_range_3,tip_radius_3,sigma_3)*delta_3;
beta_r_range_3 = 5.355E6./(tip_range_3).^0.70735;
a_range_3 = ((alpha_tip * A .* beta_r_range_3.^2) ./ (1.1 .* phi)) .* exp((B
* 1.44 * 10^-7) ./ (phi).^0.5);
b_range_3 = 0.95 * B .* (phi).^1.5 ./ beta_r_range_3;
I_portion_3 = zeros(size(a_range_3,2),size(V_GE,2));
for n=1:size(I_portion_3,2)
    for m=1:size(I_portion_3,1)
        I_portion_3(m,n) = a_range_3(m) * (V_GE(n))^2 * exp(-b_range_3(m) /
V_GE(n));
    end
end
I_3 = zeros(1,size(V_GE,2));
for n=1:size(I_portion_3,2)
    for m=1:size(I_portion_3,1)
        I_3(1,n) = I_3(1,n) + tip_distr_3(m) * I_portion_3(m,n);
    end
end
delta_I_3 = zeros(1,size(V_GE,2));
Sensitivity_3 = zeros(1,size(V_GE,2));
for n=1:size(I_portion_3,2)
    for m=1:size(I_portion_3,1)
        delta_I_3(1,n) = delta_I_3(1,n) + tip_distr_3(m) *
abs(I_portion_3(m,n)-I_3(1,n));
    end
    if I_3(n)>0
        Sensitivity_3(1,n) = delta_I_3(1,n)/I_3(1,n);
    end
end
I_3 = I_3 * 50*50;
figure(5)
```

```
semilogy(V_GE,I_3)
axis([0 60 1E-11 1E-6])
grid on
xlabel('V_{GE} (V)')
ylabel('Emission Current per tip (A)')
title('FEA Current Estimation based on GaN NW FEA (2020 DRC)')
figure(6)
plot(V_GE,Sensitivity,V_GE,Sensitivity_2,V_GE,Sensitivity_3)
axis([20 max(V_GE) -0.1 2])
grid on
xlabel('V_{GE} (V)')
ylabel('Current Sensitivity')
% End
```

This is the end of Matlab code

This is the end of this appendix document.

Appendix G

Process flow for anode integration

Process flow for anode integration
- EBL alignment and tilted metal deposition -

Pao-Chuan Shih

This is the process flow is developed for the anode integration with GaN SAGFEAs to build the fully integrated vacuum transistors. The process flow is modified from the SAGFEAs fabrication since the step of TEOS planarization. The modified part is separated out by the blue row in the process flow.

The Oxford-100 is no longer available, and the new PECVD tool for TEOS is not ready yet in 2023 Spring. The outsourcing to Lincoln Lab or Albany for TEOS deposition might be necessary.

The tool names here are mostly updated to the new name or to corresponding new tool in MIT.nano. This process flow serves as an example.

Process and Number	Process Step	Tool
1. Wafer Cleaning	10 min Piranha Clean	Acid-Etch-General-U10
2. EBL for Fin Formation	Spin coat PMMA-950 A4 750 rpm 6 sec -> 3,500 rpm 60 sec	Spinner-EBL
	Bake for 5 min at 180°C	Hot Plate
	EBL to write pattern for metal mask lift-off (device pitch ~ 600 nm)	elionix
	Evaporate 10 nm Ti / 30 nm Ni (Zero rotation)	Ebeam-Temescal-LL/ ebeamAu
	Place in acetone for lift-off (no ultrasonic)	Liftoff-L08
	Use SEM to check EBL pattern	SEM-Zeiss-Sigma300
	Remove residual PMMA by Ashing	Asher-Barrel-Thierry
3. Fin/NW Etch	Etch roughly 300 nm GaN with Recipe #45 GaN-High (~1'30") Or Recipe #46 GaN-Low (~5'30")	RIE-Cl2-SAMCO-200iP/ RIE-Mixed-SAMCO-230iP
	Use profilometer to check etch depth	Dektak-XT
4. Wafer Clean	Organic clean	Solvent-Clean-U06
	Remove Ni by Ni etchant TFB	Acid-Extended-U07
	10 min Piranha clean	Acid-Etch-General-U10
5. Digital Etching to shrink tip width	Check NWs by SEM	SEM-Zeiss-Sigma300
	Surface oxidization (1 H_2SO_4 + 1 30% H_2O_2, 4 min)	Acid-Etch-General-U10 (or L06)
	DI water soak 30 sec then rinse	Acid-Etch-General-U10

		37% HCl : H2O = 1:3, 2 min	Acid-Etch-General-U10
		DI water soak 30 sec then rinse	Acid-Etch-General-U10
		Doing above four steps several times	
		Check NWs by SEM	SEM-Zeiss-Sigma300
6.	Thick TEOS as gate insulator under pad region	400 nm TEOS deposition or SiO2 deposition	Oxford-100/ sts-CVD/ PECVD-SAMCO-PD220
		HMDS 1 min program	HMDS-YES-U10
		Spin coat AZ3312 (Default, 3,000 rpm 60 sec)	Spinner-Resist-U12
		Soft bake 100°C 1 min	Hotplate-Tower-U12
		Define etch region (375 nm laser) dose: 140 for Si sub. dose: 160 for sapphire sub.	DirectWrite-MLA-150-AirAF / DirectWrite-MLA-150-OptAF
		Post bake 110°C 1 min	Hotplate-Tower-U12
		Develop: AZ 300 MIF 80 sec -> DI water rinse	Develop-U12
		Hard bake 130°C 3 min	Hotplate-Tower-U12
		BOE etch TEOS (>130 nm/min)	Acid-Etch-General-U10
		Remove resist	Asher-Barrel-Thierry and Solvent-Clean-U06
7.	Protection layer	2nd-gen. device: Sputter 35 nm Al Now: ALD 10 nm Al_2O_3 (100 cycle, 250°C)	Sputter-AJA-LL / ALD-Ozone
8.	Gate stack deposition	200 nm TEOS deposition (or SiO2 deposition)	Oxford-100/ PECVD-STS-MMPLEX/ PECVD-SAMCO-P220
		Cr deposition (Sputtering) (100 nm)	Sputter-AJA-LL/ Sputter-AJA-ChamberLoad
9.	Gate isolation	Lithography to isolate gate metals (AZ 3312)	DirectWrite-MLA-150/ HMDS, Spinner-Resist
		Wet etch Cr	Acid-Extended-U07
		Organic clean to remove resist	
10.	TEOS planarization	1 μm TEOS deposition (thickness > device pitch)	Oxford-100
11.	Expose EBL alignment mark	Lithography to expose EBL alignment marks (AZ 3312)	DirectWrite-MLA-150/ HMDS, Spinner-Resist

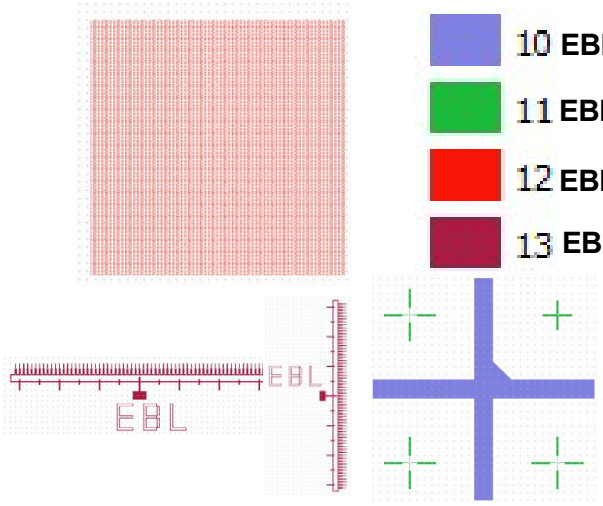
	BOE etch TEOS Cr etching etch Cr BOE etch TEOS and Al_2O_3	Acid-Etch-General-U10
12. EBL to define supporting lines	EBL to define Ti/Ni mask for TEOS supporting pillars dry etching (PMMA, cold develop)	HS-50/ Spinner-EBL
	10 nm Ti / 40 nm Ni deposition	Ebeam-Temescal-LL
	NMP lift-off (over few days)	
	Check by SEM	SEM-Zeiss-Sigma300
	Asher and organic clean	
13. Define anode metal connection and pad	Lithography to expose EBL alignment marks (PMGI + AZ 3312)	DirectWrite-MLA-150/ HMDS, Spinner-Resist, Spinner-PMGI-U12
	10 nm Ti / 50 nm Ni deposition	Ebeam-Temescal-LL
	NMP lift-off	
	Asher and organic clean	
14. TEOS supporting pillars formation (1st part)	Dry etch TEOS ~ 750 nm (SiO2-PC, with Si carrier and Santovac)	RIE-Mixed-SAMCO-230iP
	Check by SEM	SEM-Zeiss-Sigma300
15. Define gate metal	Lithography to define gate metal region (AZ 3312)	DirectWrite-MLA-150/ HMDS, Spinner-Resist
16. TEOS supporting pillars formation (2nd part)	Dry etch TEOS ~ 300 nm (SiO2-SEL)	RIE-Mixed-SAMCO-230iP
	Check by SEM	SEM-Zeiss-Sigma300
	Remove resist and clean	
17. Etch gate metal	Dry etch Cr 120 nm (overetch ~ 20 nm)	RIE-Mixed-SAMCO-230iP
	Check by SEM	SEM-Zeiss-Sigma300
18. Define source contact	HMDS 1 min program	HMDS-YES-U10
	Spin coat PMGI SF5 (750 rpm 10”-> 3500 rpm 60”)	Spinner-PMGI-U12
	Bake 235^{O}C 6 min	Hotplate-Tower-U12
	Spin coat AZ3312 (Default, 3,000 rpm 60 sec)	Spinner-Resist-U12
	Lithography: MLA **At least 180 mJ/cm^2**, 0 defocus, 375 nm	DirectWrite-MLA-150-AirAF / DirectWrite-MLA-150-OptAF

	Develop: AZ 300 MIF **90 sec** -> DI water rinse	Develop-U12
	Slowstrip-5 min	Asher-Barrel-Thierry
	BOE etch TEOS (~ 250 nm) to expose n+ layer surface for source contact (BOE etch TEOS ~ 200 nm/min)	Acid-Etch-General-U10
	Surface clean DI water dip 1 min	Acid-Etch-General-U10
	37% HCl : DI water = 1:3 dip for 1 min	Acid-Etch-General-U10
	DI water dip 1 min	Acid-Etch-General-U10
19. Source pad metal	Ti/Al/Ti/Au deposition (20 nm/ 100 nm/ 30 nm/ 50 nm)	Ebeam-Temescal-LL /ebeamAu/ebeamAJA
	Use NMP for lift-off	Liftoff-L08
	Remove residual by Ashing	Asher-Barrel-Thierry
20. Define gate pad	HMDS 1 min program	HMDS-YES-U10
	Spin coat PMGI SF5 (750 rpm 10"-> 3500 rpm 60")	Spinner-PMGI-U12
	Bake 235^{O}C 6 min	Hotplate-Tower-U12
	Spin coat AZ3312 (Default, 3,000 rpm 60 sec)	Spinner-Resist-U12
	Define gate pad region Lithography: MLA **At least 180 mJ/cm^2**, 0 defocus, 375 nm	DirectWrite-MLA-150-AirAF / DirectWrite-MLA-150-OptAF
	Develop: AZ 300 MIF **105 sec** -> DI water rinse	Develop-U12
	Slowstrip-5 min	Asher-Barrel-Thierry
21. Gate pad metal	BOE etch TEOS ~ 350 nm to expose Cr metal surface at pad area	Acid-Etch-General-U10
	Ni/Au deposition for gate pad (20 nm / 100 nm)	Ebeam-Temescal-LL /ebeamAu/ebeamAJA
	Use NMP for lift-off	Liftoff-L08
	Remove residual by Ashing	Asher-Barrel-Thierry
22. Define thick resist for metal pad protection and lift-off mask	HMDS 1 min program	HMDS-YES-U10
	Spin coat AZ-10xT 520cP (Default, 3,000 rpm 60 sec)	Spinner-Resist-U12
	Soft bake 110^{o}C 2 min	**Hotplate-Tower-U12**
	Define resists mask for protection and lift-off	DirectWrite-MLA-150-AirAF

	(405 nm laser) **Dose: 450**	
	No Post bake	
	Develop: **AZ 435 MIF 120 sec** -> DI water rinse	Develop-U12
	Hard bake 95ºC 3 min	Hotplate-Tower-U12
	Slowstrip-5 min	Asher-Barrel-Thierry
23. Expose GaN tips	Dry etch TEOS ~ 220 nm (**Slow etch needed, no high-power etch**) Recipe: SiO2-SEL (CHF_3 + CF_4) (RIE-F-SAMCO, rate 30~40 nm/min?) Recipe: SiO2-SEL (CF_4 + H_2) (RIE-Mixed-SAMCO, rate ~ 30 nm/min)	RIE-F-SAMCO-230iP/ RIE-Mixed-SAMCO-230iP
	Developer etch Al_2O_3 (AZ 300 MIF 5 min : 10 nm ALD Al_2O_3?) ⇨ DI water 2 min => blow dry	
	Check by SEM	SEM-Zeiss-Sigma300
24. **Anode metal deposition (Tilted)**	**70-degree Tilted metal deposition** **(Example stack: 20 nm Ti / 200 nm Al / 20 nm Ti / 100 nm Au)** **(Metal thickness determined if the vacuum cavity is packaged)**	Ebeam-Temescal-LL
	NMP log lift-off	
	Use pipette to help lift-off => new NMP => low power ultrasonic 1 min => IPA => DI water => IPA => blow dry	
	Check by SEM	SEM-Zeiss-Sigma300
25. Clean and finish	DI water -> IPA -> blow dry	Solvent-Clean-U06
	Bake 130ºC 5 min	Hotplate-Tower-U12

Lithography patterns design of Anode-integrated GaN field-emission-based vacuum trnasistors

Lithography patterns (I)



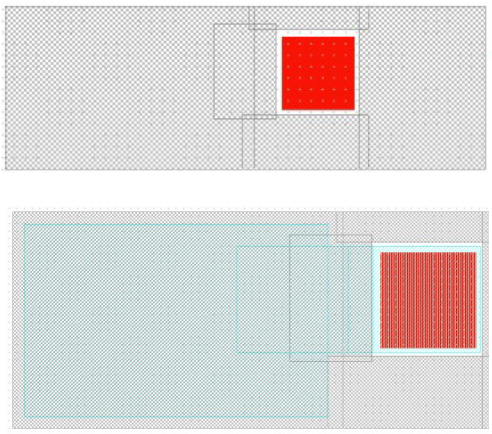
10 EBL, large notations (big current)

11 EBL, Alignment marks

12 EBL, FEA tips, 40-nm-width square

13 EBL, alignment check patterns

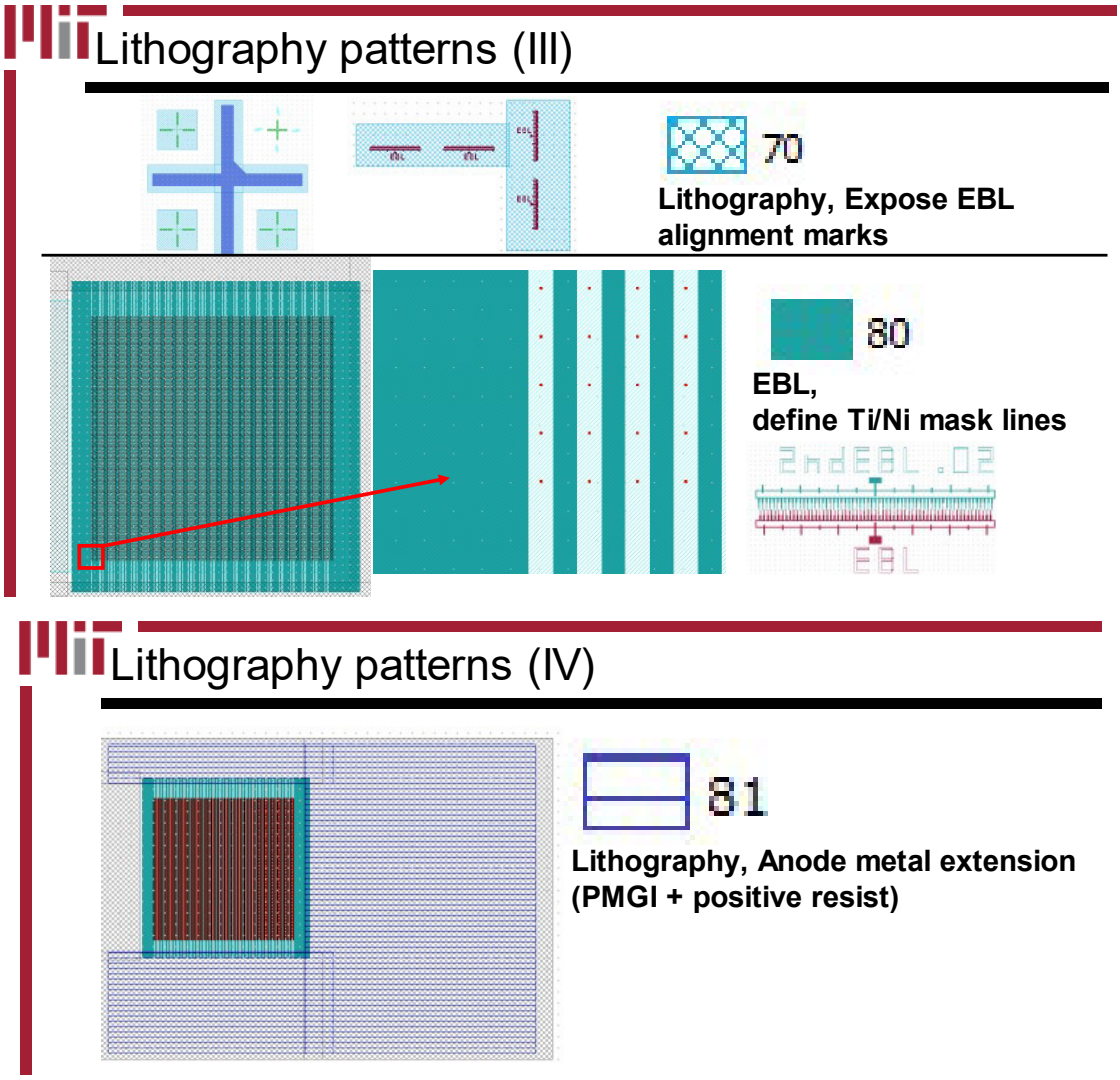
Lithography patterns (II)

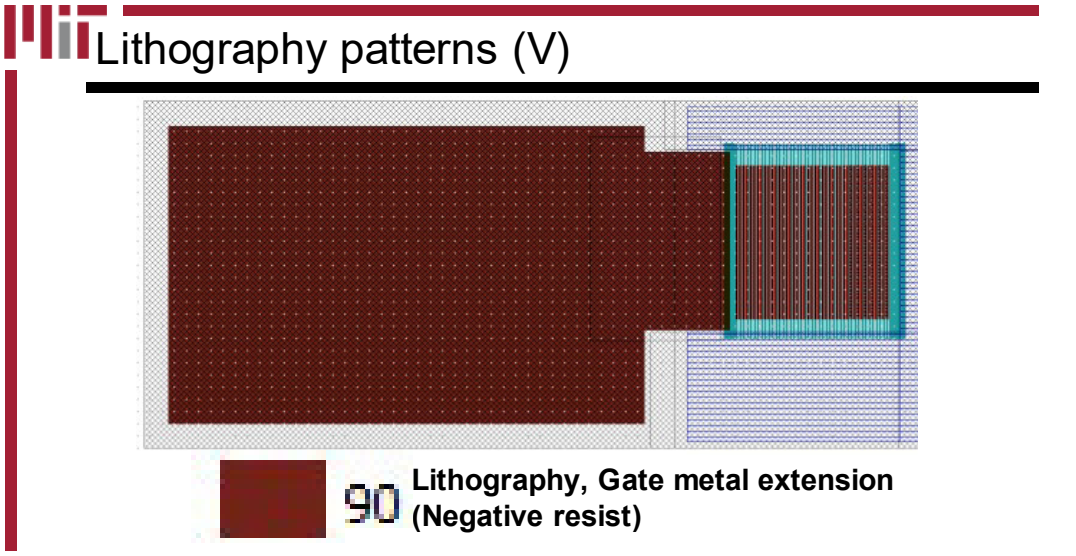


12 EBL, FEA tips, 40-nm-width square

50 Lithography, thick TEOS under gate pad (Negative resist)

60 Lithography, Gate isolation (Negative resist)


Lithography patterns (III)
70
Lithography, Expose EBL
alignment marks
80
EBL,
define Ti/Ni mask lines
2ndEBL.02
EBL
Lithography patterns (IV)
81
Lithography, Anode metal extension
(PMGI + positive resist)



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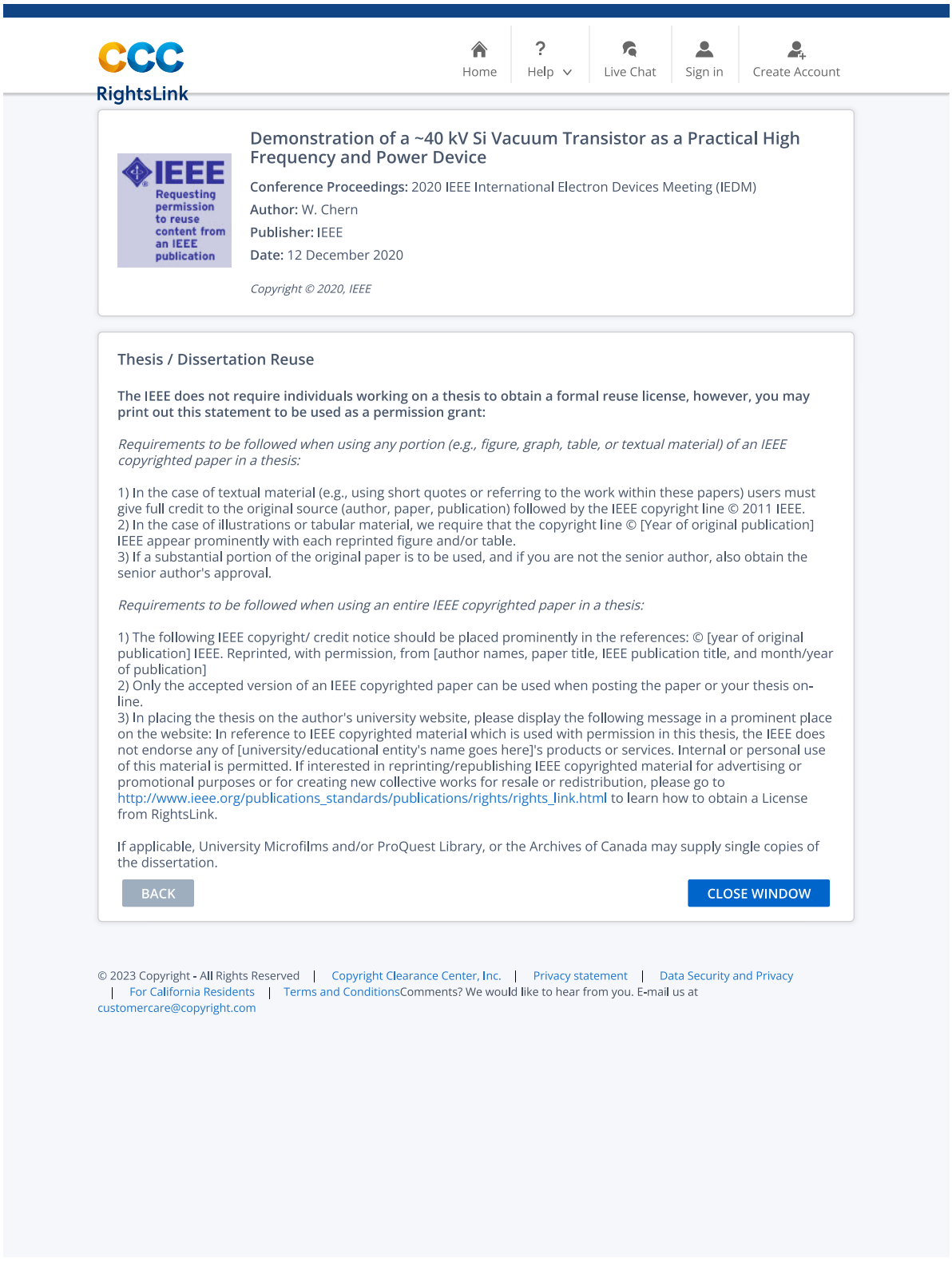

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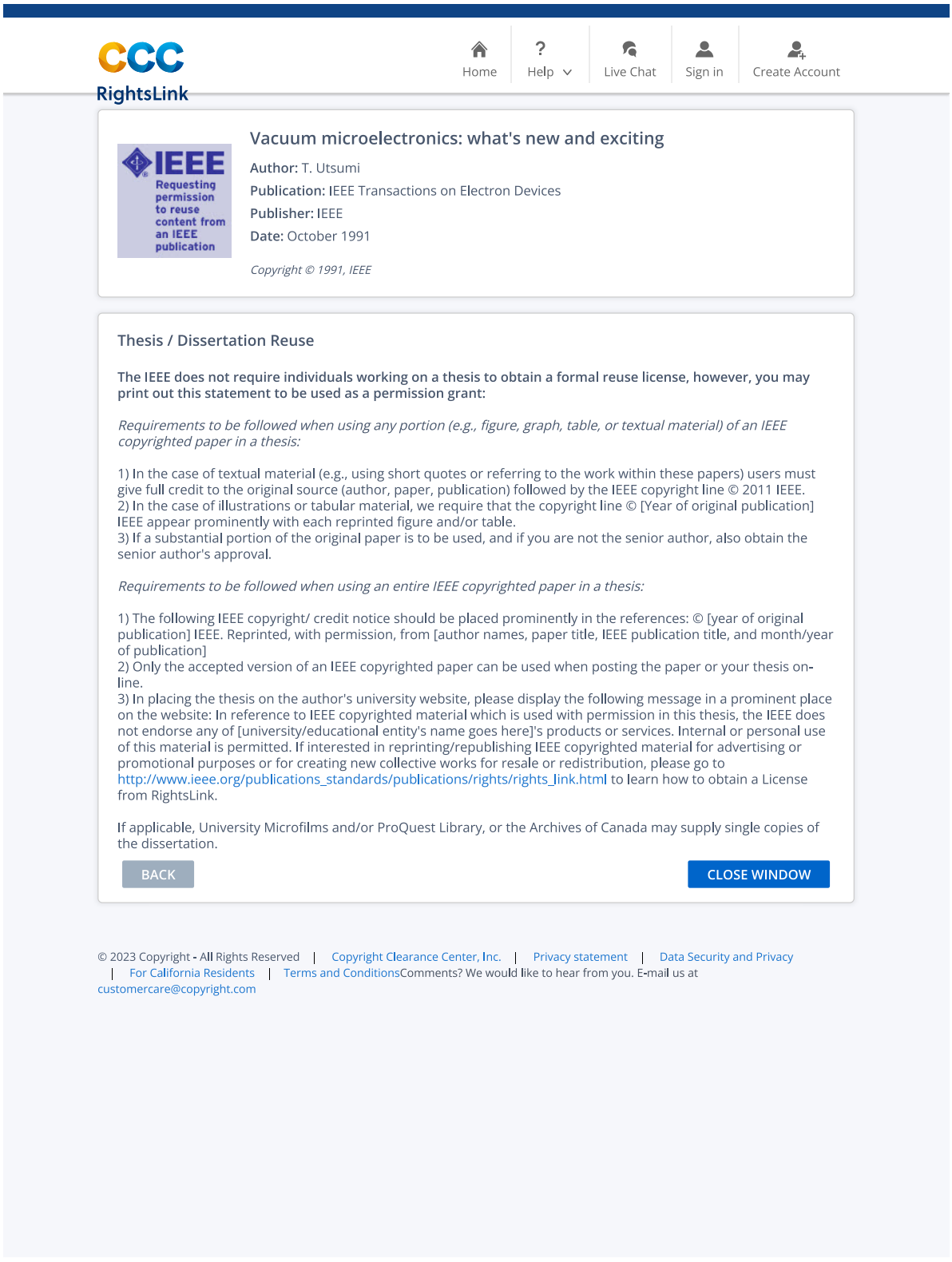

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