A superconducting nanowire binary shift register

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ABSTRACT

The development of superconducting electronics based on nanocryotrons has been limited so far to few device circuits, in part due to the lack of standard and robust logic cells. Here, we introduce and experimentally demonstrate designs for a set of nanocryotron-based building blocks that can be configured and combined to implement memory and logic functions. The devices were fabricated by patterning a single superconducting layer of niobium nitride and measured in liquid helium on a wide range of operating points. The tests show 10^{-4} bit error rates with above ±20% margins up to 50 MHz and the possibility of operating under the effect of an out-of-plane 36 mT magnetic field, with ±30% margins at 10 MHz. Additionally, we designed and measured an equivalent delay-flip-flop made of two memory cells to show the possibility of combining multiple building blocks to make larger circuits. These blocks may constitute a solid foundation for the development of nanocryotron logic circuits and finite-state machines with potential applications in the integrated processing and control of superconducting nanowire single-photon detectors.

The nanocryotron (or nTron) is a superconducting three-terminal component that was proposed as a candidate for low-power electronics in 2014.[1] This device has unique properties among superconducting devices, such as the capability of driving high-impedance loads and the possibility of operation in ambient magnetic fields. Several proof-of-concept circuits based on nanocryotrons have been demonstrated, including a memory cell,[2] a binary encoder,[3] and an artificial neuron for neuromorphic computing.[4] In addition, the possibility of interfacing the nTron with other technologies, such as superconducting nanowire single-photon detectors (SNSPDs), rapid single flux quantum (RSFQ), and cryo-CMOS, has been demonstrated.[5] Interfacing these technologies is beneficial for the development of integrated sensors and superconducting optoelectronic hardware.[6]

Despite their promising characteristics, nTron-based circuits have only been demonstrated at the scale of a few devices, thus far, limiting their potential applications. In particular, the realization of larger circuits has been hindered by the absence of nTron-based standard cells that can be easily combined together. Therefore, in this work, we introduce a set of building blocks that integrate memory and logic functions and demonstrate these blocks experimentally, in isolation as individual cells, and cascaded, to show the feasibility of large-scale logic circuits.

To understand the working principle of the circuits, it is necessary to first understand how an nTron works. The device behaves as a current-controlled normally closed switch. The gate of an nTron is connected to the device's main channel by a narrow choke. If the current in the choke exceeds the critical current of this choke, a localized resistive area, or hotspot, is generated at the gate constriction. The presence of this hotspot suppresses the critical current of the corresponding branch of the loop.

Here, we describe the elementary cell of the logic family, which is a destructive readout memory.

The circuit topology of the cell is shown in Fig. 1. It is composed of a superconducting loop containing a kinetic inductor and two nTrons whose gates are connected to the input (IN) and read (READ) terminals. The output terminal (OUT) is placed above the READ. A direct current biases the loop. The state is determined by the primary direction of the current, flowing in the left or right branch of the loop.

Due to the presence of the kinetic inductor in the right branch of the loop, when the cell is turned on, the bias current flows almost entirely into the left branch. This state, depicted in Fig. 1(a), corresponds to the zero state ("0").

The state of the cell can be modified or read by sending current pulses to the nTrons' gate terminals. The writing and reading

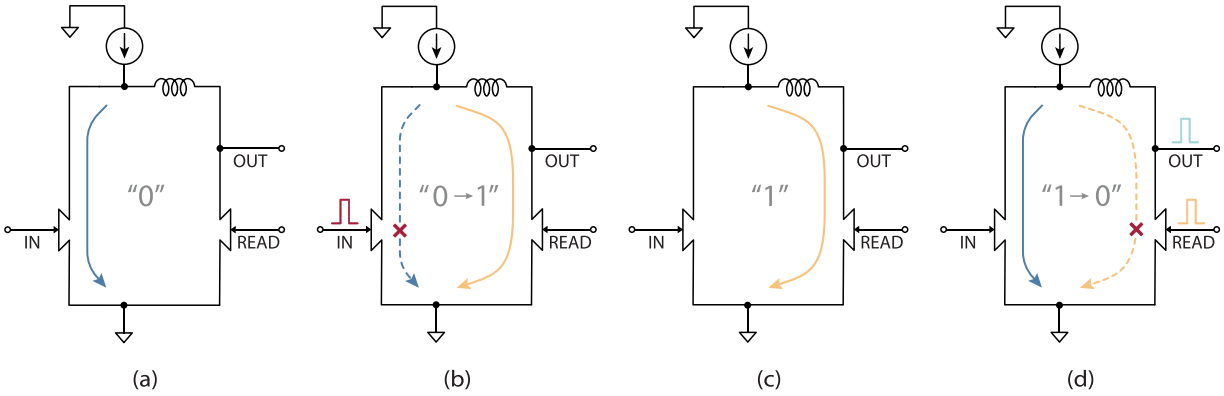

FIG. 1. Memory cell writing and reading procedures. (a) Due to the presence of the kinetic inductor, the bias current initially flows in the left branch of the loop. The cell is in the "0" state. (b) When a pulse arrives at the IN terminal, a hotspot develops in the corresponding nTron channel. The presence of this resistive region transfers the bias current to the right branch of the loop. (c) The current continues to flow in the right branch. The cell is in the "1" state. (d) If a pulse is sent to the READ terminal, a hotspot is formed in the right branch. The resistive region produces a voltage spike at the OUT terminal and moves the bias current to the left branch. The cell is reset to the "0" state, depicted in (a).

procedures are shown in Fig. 1. As mentioned, the cell is initially in the "0" state [Fig. 1(a)]. The state can be set to "1" by sending a current pulse to the input (IN) nTron [Fig. 1(b)]. If the current exceeds the gate's critical current, a hotspot is created. Since the bias current is flowing in the left branch of the loop, the hotspot expands, causing the nTron channel to switch to the normal state. Due to the presence of this normal (resistive) region, the bias current is transferred from the left branch to the right one, which is superconducting. The bias current flows in the right branch [Fig. 1(c)]. The "1" state has been written in the memory cell. Analogously, the cell can be read by sending a current pulse to the READ terminal. If the cell is in the "1" state, the formation of the hotspot moves the current back to the left branch. Moreover, due to the inductor, a voltage spike is now produced at the output terminal (OUT), as shown in [Fig. 1(d)]. During the reading, the cell returns to the "0" state. If a cell in the "0" state is read, no hotspot is generated in the right branch. Therefore, the state is left unaltered, and no output signal is generated.

The device resembles an RSFQ set-reset latch in topology and behavior.[7] However, unlike a Josephson junction, an nTron is a three-terminal device with a gate terminal that controls the state of the main channel. This geometric difference allows multiple nTrons in the same superconducting loop to be addressed individually. By adding extra nTrons to the memory cell, different logic gates can be obtained using a single loop, which is not the case for RSFQ gates.

Figure 2 illustrates three such gates. Figure 2(a) shows an OR gate, which is created by adding an extra input to the left branch of

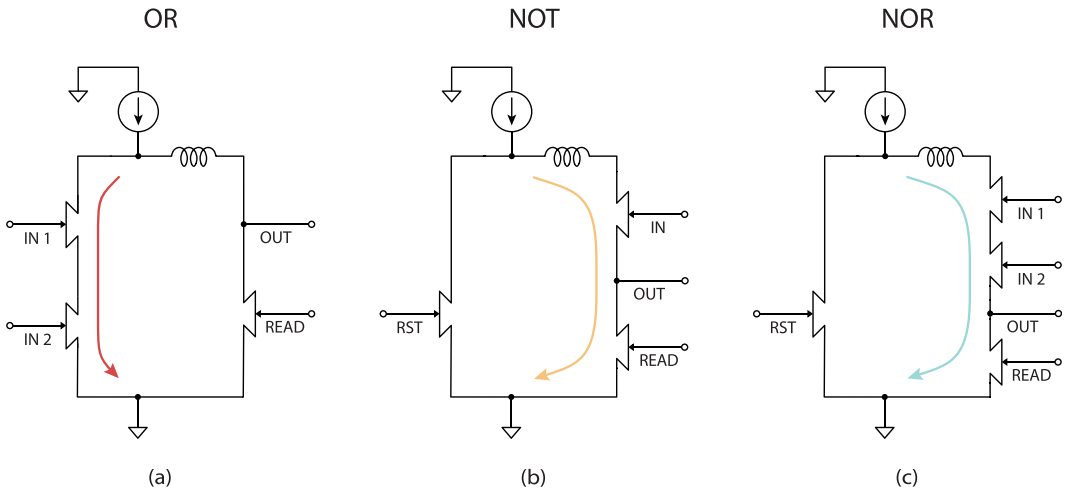

FIG. 2. Logic gates circuit schematic. (a) If extra nTrons are added to the left branch of the cell's loop, the memory switches to the "1" state if any of them receives an input spike. Therefore, the device behaves as an OR gate, in which the state is preserved until reading. (b) An analogous NOT gate can be obtained by moving the input to the right branch and adding a reset nTron in the left branch to precharge the state to "1." (c) A NOR gate can be made by adding extra inputs to the NOT gate. After reset, any input spike would move the current to the left branch and, thus, the state to "0." For the sake of simplicity, the shunt and output resistors (connected to the top of the left branch and the OUT terminal) are not shown in the schematics.

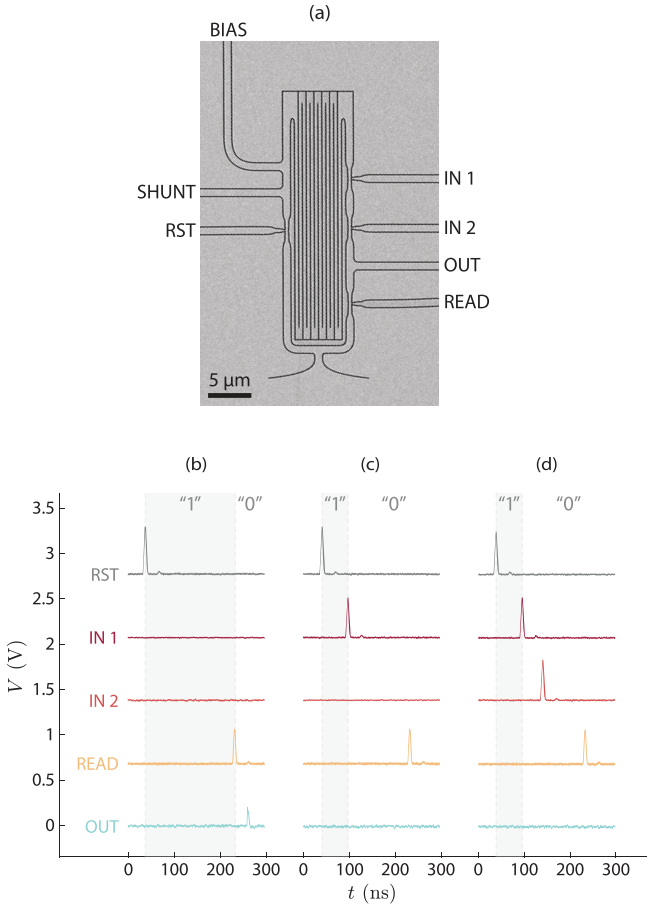

FIG. 3. NOR gate micrograph and experimental voltage traces. (a) Scanning electron micrograph of a NOR gate with a 20 nH kinetic inductor, in the middle of the loop, and all the electrical terminals. (b)–(d) Experimental voltage traces of a NOR gate with different input configurations. In the three cases, the cell was preset to "1" by sending a current spike to the RST terminal. (b) No input was sent, and thus, the state of the cell was preserved until reading. The read spike generated a corresponding output spike. (The delay between the reading spike and the output signal was mainly given by the wiring of the setup and not by internal effects.) Conversely, when one (c) or both (d) inputs fired, the cell was set back to "0," and no output was generated. The plots are vertically offset for clarity.

the memory cell. If either input receives a current spike, the bias current is diverted to the right branch, setting the cell to the "1" state. To make a NOT gate, the input terminal is moved to the right branch, and an extra reset (RST) nTron is inserted in the left branch [Fig. 2(b)]. In this case, the RST nTron is switched first, to preset the cell state to "1." If a current spike is injected into the IN terminal before reading, the cell is set to "0." Otherwise, the cell remains in the "1" state. Finally, if extra inputs are added to the NOT gate, the cell will be set to "0" if any of these receives a current spike. The cell behaves as a NOR gate [Fig. 2(c)]. Since the NOR operation is functionally complete (i.e., any logic operation can be expressed in terms of NORs), the set of these gates is logically universal. It is worth noticing that in the inverting gates, the output terminal is placed above the READ but below the inputs; otherwise, each input pulse would generate unwanted output signals due to the resistive state generation. Similar to the memory cell, each of these gates preserves the state until it is read by sending a reading signal, which releases the result of the operation.

We determined the target circuit parameters of the device designs with SPICE simulations, using an electrical model of the nTron.[8,9]

Starting from the obtained values, the devices were fabricated on thermal oxide on silicon chips, with an oxide thickness of 300 nm. A 15 nm-thick niobium nitride (NbN) film was deposited by reactive sputtering,[10] patterned with electron beam lithography, and etched with CF_4 reactive ion etching.[11] A scanning electron micrograph of a NOR gate with a 20 nH inductor is depicted in Fig. 3(a). Finally, the chip was wire-bonded to a printed circuit board on which 50 Ω shunt resistors were soldered.

The circuits were tested in liquid helium (4.2 K). We employed a custom dip probe,[12] which includes a copper coil to apply out-of-plane magnetic fields to the samples. To evaluate the devices' bit error rate (BER), we used a Keysight PXIe M3202A arbitrary waveform generator and an M3102A digitizer.

In this work, we experimentally tested multiple devices (on two chips) with different values of loop inductance: five memory cells with 60 nH, 40 nH, 20 nH, and 5 nH, two OR gates with 60 nH and 40 nH, two NOR gates with 20 nH, and a NOT gate with 20 nH. All the devices' nTrons had a 300 nm-wide main channel and a 30 nm-wide choke.

The experimental voltage traces for different input configurations of a NOR gate are presented in Figs. 3(b)–3(d).

As shown in Fig. 3(b), the cell was first set to "1" by the RST signal, and no subsequent input was applied. Therefore, when the READ signal was applied, an output pulse was generated. (The state "1" was read out.) In the traces of Figs. 3(c) and 3(d), a current spike was injected into at least one input terminal, moving the bias current to the left branch and, thus, setting the memory to "0." In this case, no output pulse was generated, as expected for a NOR gate.

We measured the bit error rate (BER) of a memory cell (with a 40 nH inductor) to characterize the performance of the devices. The analysis took into account a range of bias and input currents to study the margins of operation of the circuit. Each point of the sweep was tested on a 10^4-bit-long pseudo-random sequence. Furthermore, the BER, shown in Fig. 4, was evaluated at different frequencies and in a magnetic field.

Figures 4(a)–4(c) show the variation of the low-error operating region (in yellow) as a function of frequency. At 10 MHz, the operating point margins, from the center of the region, are greater than ±40% in both directions. With increasing frequency, the area was observed to narrow in the horizontal direction, corresponding to the peak current of the input spikes. We related this observed narrowing to a more frequent occurrence of latching of the nTrons (i.e., they do not return to the superconducting state[13]) for high bias and input currents. The device produced high error rates as well if the currents were too low to generate a hotspot (under-biasing).

The maximum frequency of operation was limited by the time needed for the nTrons to recover the superconducting state from the resistive state. Whenever a hotspot was generated in one branch of the loop before the other branch had recovered the superconducting state, the nTrons of both branches latched to the resistive state. To recover the device from this latching state, we had to reset the memory by

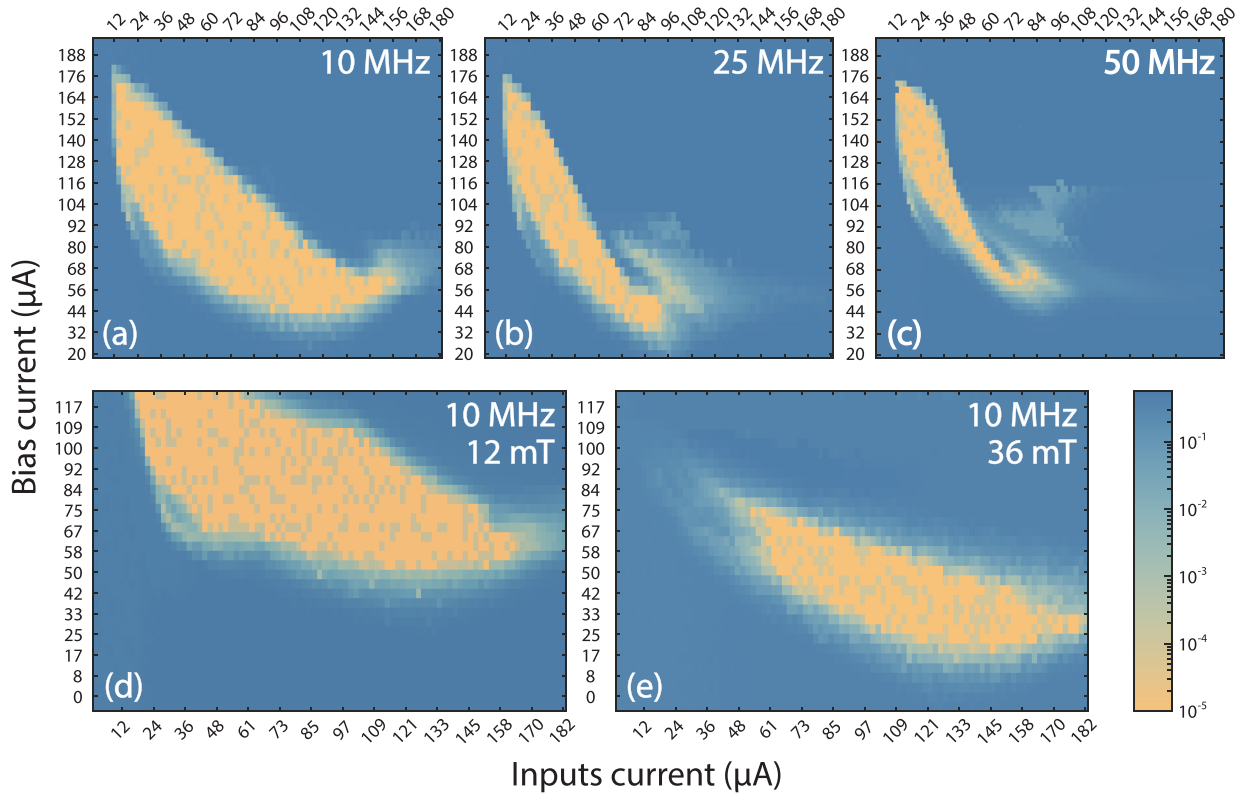

FIG. 4. Memory cell bit error rate (BER) at different frequencies and magnetic field intensities. The BER is evaluated on a range of operating points at (a) 10 MHz, (b) 25 MHz, and (c) 50 MHz, and at 10 MHz under a magnetic field of (d) 12 mT and (e) 36 mT. Each bias point was measured on 10^4 pseudo-randomly generated input bits.

removing the bias current. The occurrence of this phenomenon was mitigated by separating input and read signals by a setup time of ∼10 ns. The operation of the device was demonstrated up to 100 MHz, but with very narrow margins on the operating point, due to the shorter setup time and, therefore, a more frequent occurrence of latching events.

One of the advantages of superconducting nanowires and nTrons over other superconducting technologies is their ability to operate in a magnetic field.[14] Therefore, the BER was measured at 10 MHz in the presence of a static magnetic field. The corresponding results are shown in Figs. 4(d) and 4(e). With a 12 mT out-of-plane field applied to the chip, the BER remained essentially unaffected. In contrast, when the field was increased up to 36 mT, the operating margins shrank and shifted to lower values of bias current. This effect is likely to be related to the extra current added to the loop by flux trapping,[15] which causes a decrease in the effective switching current of branches. Despite the shift, the device continued to perform with ±30% margins around the optimal operating point.

The choice of the operating point also affects the energy per operation. An upper bound to the energy consumption can be estimated by considering the bias current to flow for 5 ns through a 50 Ω resistance (strictly higher than the parallel combination of the hotspot resistance and the shunt) during each switching event. For a reasonable choice of current magnitudes, the energy per operation was estimated to be 1 fJ.

After demonstrating and analyzing single-cell devices, we designed an equivalent primary-secondary (two-section) delay-flip-flop, made of two memories, to show the possibility of combining multiple cells. The schematic of the circuit is reported in Fig. 5(a). In this flip-flop, each cell stores its logic state until reading. When a cell is read, the state is transferred to the following stage. The reading of the two cells is performed by the out-of-phase signals CLK 1 and CLK 2.

The output of the first cell and the input of the second one were connected by a 20 Ω resistor. The presence of the resistance prevented any persistent current from being stored in the connection, which could cause unwanted switching of the second-cell input nTron. The corresponding experimental voltage traces are displayed in Fig. 5(b). Initially, both memories were in the "0" state. Therefore, any reading operation did not produce an output signal. Once a current spike was sent to the IN terminal, the first cell switched to "1." When this cell was read with a CLK 1 signal, the memory was reset, and a voltage spike was produced at the OUT 1 terminal. This spike set the second cell to the "1" state. Its state could then be read and reset by sending a current pulse to the CLK 2 terminal. The circuit demonstrates the possibility of connecting multiple cells. Moreover, it constitutes a basic element for other circuits, such as a shift register.

Following the analysis of the experimental results, it is worth examining further advantages and limitations involved in the scaling of this technology. The main limitation for shrinking the size of the device is given by the kinetic inductor. This component plays three

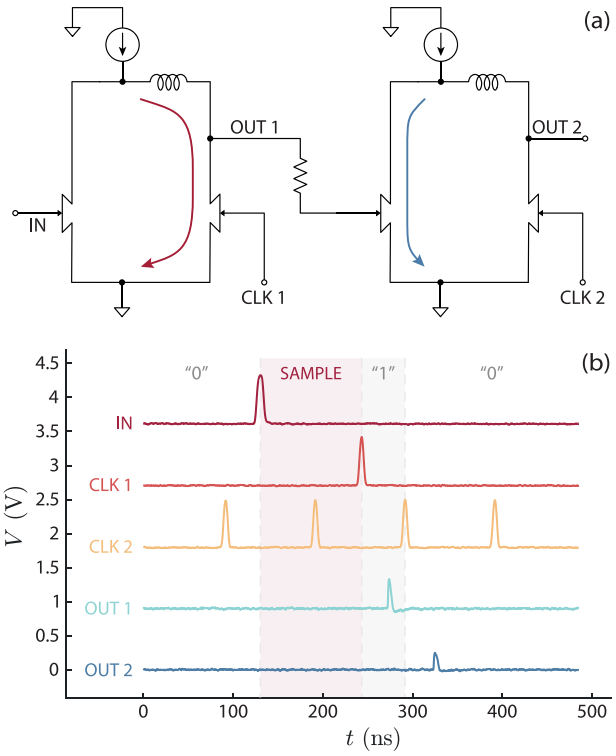

FIG. 5. Equivalent delay-flip-flop schematic and experimental voltage traces. (a) The schematic shows the resistive connection of two memory cells controlled by two clock signals. (b) Experimental voltage traces of two memory cells (with 60 nH inductors) connected together. A current spike was sent to the IN terminal of the first cell, which sampled the input and, thus, switched to the "1" state. The value was transmitted to the second cell by a CLK 1 current pulse, which also reset the first cell. Finally, the CLK 2 signal read the second cell producing an output (OUT 2 terminal) signal and set the second cell to "0" again. As can be noticed from the traces, the CLK 2 pulses produced an output spike only if the first cell was in the "1" state [a condition marked as "sample" in (b)]. The plots in (b) are vertically offset for clarity.

fundamental roles in the cells' functioning: (1) It sets the cell state to "0" when the device is turned on, (2) it increases the output impedance, and (3) it reduces the impact of latching. All three roles benefit from the use of larger inductances. Of particular importance is the effect of the inductance on the output impedance, which affects the peak voltage of the output spikes. Indeed, the smallest memory tested (5 nH inductor) worked properly but produced lower signal levels. Nevertheless, the inductor size problem could be solved by employing high-fan-in gates in logic circuits. The cost, in terms of area, of additional nTrons in the loop is negligible compared to the kinetic inductor area, which does not increase for multi-input gates. Therefore, employing multi-input gates would result in a decrease in the overall area footprint per logic function. In addition, the nTron's high output current[1] could lead to larger fan-out gates, which would reduce the number of cells of a logic circuit, resulting again in a decrease in area footprint.

To further assess the technology's applicability, future work should focus on the demonstration of multiple gates' logic circuits and integration with SNSPDs for elementary control and processing.

This work effectively creates a design methodology for nanocryotron circuits wherein a layer of digital abstraction can now be placed between the device physics and the information-processing needs of an application. The result is a much simpler, more accessible design paradigm for nanocryotrons. With this tool, future researchers can explore applications of these devices in areas such as quantum control, superconducting detector readout, and low-power electronics for extreme environments.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Alessandro Buzzi: Conceptualization (lead); Data curation (lead); Investigation (lead); Software (lead); Visualization (lead); Writing – original draft (lead). **Matteo Castellani:** Conceptualization (supporting); Data curation (supporting); Investigation (equal); Software (supporting); Supervision (lead); Validation (equal); Visualization (equal); Writing – review & editing (equal). **Reed A. Foster:** Investigation (equal); Software (equal); Writing – review & editing (equal). **Owen Medeiros:** Investigation (equal); Supervision (supporting); Validation (equal); Writing – review & editing (supporting). **Marco Colangelo:** Conceptualization (supporting); Investigation (equal); Resources (equal); Supervision (equal); Validation (equal); Writing – review & editing (equal). **Karl K. Berggren:** Conceptualization (supporting); Project administration (lead); Supervision (equal); Validation (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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