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GaN Field Emitter Arrays with J_A of 10 A/cm^2 at V_{GE} = 50 V for Power Applications

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***Abstract*—**III-Nitrides are attractive as field emission devices for high frequency, high power, and harsh environment applications. A wet-based digital etching and a novel device geometry was used to demonstrate GaN vertical self-aligned-gate (SAG) field emitter arrays (FEA) with uniform tips of sub-10 nm tip radius. The best GaN FEA has a current density (J_A) of 10 A/cm^2 at V_{GE} = 50 V, which is better than the state-of-the-art Si field emitter arrays at the same bias condition.

I. Introduction

Vacuum transistors, where electrons are injected into a vacuum channel instead of a semiconductor material, are expected to show better performance than traditional devices in a wide variety of high-frequency, high-power, and harsh environment applications [1],[2]. Si-based self-aligned-gate field emitter arrays (SAGFEAs) with sub-10 nm tip radius and current densities of 100 A/cm^2 at V_{GE} = 70 V have been demonstrated [3]. Besides Si, III-Nitrides, such as GaN and AlGaN, are promising to provide better SAGFEAs than Si because of their engineerable electron affinities and material robustness. Electron affinities in III-Nitrides can be reduced by increasing the Al composition or by using the N-polar surface instead of the more common metal-polar one. Despite the great promise of III-Nitride field emitters, there are very few demonstrations so far of high-performance III-Nitride SAGFEAs with a current density > 1 A/cm^2. Recently, we used a wet-based digital etching (DE) to demonstrate both GaN and AlGaN SAGFEAs with a turn-on voltage ($V_{GE,ON}$) of 23 V and 20 V (@ I_A = 10 pA), and with a current density (J_A) = 0.15 and 0.1 A/cm^2 at V_{GE} = 50 V and 40 V, respectively [4],[5]. In this work, the device geometry has been redesigned to provide better device stability and high current density. The best GaN SAGFEA has a $V_{GE,ON}$ of 20 V and max J_A of 10 A/cm^2 at V_{GE} = 50 V, which is better than the state-of-the-art Si FEAs [3],[6].

II. Device Fabrication

GaN SAGFEAs are fabricated on coupons which are cut from a 6-inch GaN-on-Si wafer grown by metal organic chemical vapor deposition (MOCVD). The structure consists of a 1.4 μm n^{++}-GaN (Si: 1×10^{19} cm^{-3}) layer on a buffer layer grown on the Si substrate, which was grown by Enkris Semiconductor, Inc. The process flow is shown in Fig. 1, which is similar to Ref. [4] with some minor modifications.

The cross-sectional SEM and high-resolution TEM image of the prior generation of GaN FEAs (reported in Ref. [4]) are shown in Fig. 2. A uniform tip array with sub-10 nm tip radius can be fabricated by ICP-RIE dry etching with a subsequent wet-based DE, and the tip size is further confirmed by TEM (Fig. 2(b)). Based on the cross-sectional SEM image (Fig. 2(a)), the gate-emitter field factor (β_{GE}) can be simulated by Silvaco TCAD and its dependance with the tip radius is shown in Fig. 3. Based on this dependance, assuming the gate stack, geometry, and the GaN tip surface work function are similar, the tip radius of the future GaN FEAs can then quickly be estimated by fitting their response to the formula shown in Fig. 3(b). Though the tip sharpness is comparable to the one in Si devices [6], the device stability of this prior generation GaN FEA is still an issue due to the high peak electric field in the SiO_2-covered GaN tips along the periphery of the device. These covered GaN tips are necessary to extend out the gate metal due to imperfect lithography alignment. A chemical mechanical polish (CMP) approach, as the one demonstrated in Si FEAs [3], can eliminate this alignment issue. Unfortunately, the CMP of GaN-on-Si pieces can be very challenging due to the wafer bow typical in these wafers. In this work, we reduced the peak electric field in the SiO_2 layer of the covered tips by modifying the device geometry to ensure the covered tips in the sacrificial regions have much blunter tips (i.e tip radius of about 100 nm) (Fig. 5(a)). Since these blunt tips have a much lower field enhancement factor (based on the formula in Fig. 3(b)), electrons will not emit from these blunt tips. Therefore, these blunt tips have been ignored for the current density (J_A) estimation of the GaN FEAs fabricated in this work.

During the fabrication of GaN FEAs, (1) GaN vertical nanopyramid tips are firstly formed by Cl_2/BCl_3-based ICP-RIE using a Ni hard mask defined by e-beam lithography and lift-off. The height of these nanopyramids is about 300 nm. After the hard mask is removed, the tips are sharpened by a wet-based DE (Fig. 5). The details of this DE can be found in Ref. [4], [5].

After tip formation, (2) 400 nm plasma-enhanced chemical vapor deposition (PECVD) SiO_2 is deposited to increase insulator thickness under the gate pad to improve device stability, and a 10 nm Al_2O_3 layer is deposited by atomic layer deposition (ALD) to protect tips from the following etching steps. Then (3) the gate stack is formed by PECVD tetraethyl orthosilicate (TEOS) and sputtering Cr (Fig. 5(b)). (4) Devices are then planarized by PECVD TEOS, followed by timed dry etching (Fig. 6(a)). After that, (5) gate metal Cr is dry etched using TEOS as a hard mask. Then (6) a metal stack (Ti/Al/Ti/Au) is deposited as ohmic contacts on the n^{++}-GaN layer, and a metal stack (Ni/Au) is deposited on top of the gate

as gate probing pads. Devices are then finished by (7) dry etching TEOS and a quick BOE wet etching to remove the Al_2O_3 protection layer and expose the GaN tips (Fig. 6(b)). The tip width is estimated 16-18 nm by SEM (Fig. 7(a)).

III. Device Measurement and Discussion

After the tips are exposed and are imaged by SEM, the sample is loaded into an ultrahigh vacuum (UHV) measurement system with a base pressure of 7×10^{-10} Torr. The measurement setup is shown in Fig. 7(b). The anode terminal is a suspended tungsten ball with 0.5-mm diameter and can be moved by micrometer manipulators. The anode-emitter distance (d_{AE}) is kept about 2 mm in all measurements in this work.

The I-V transfer characteristics and the corresponding Fowler-Nordheim (F-N) plot of one of the best GaN FEAs are shown in Fig. 8. Due to high anode voltage (V_A = 500 V) and high maximum anode current (I_A > 100 μA), the source measurement unit (SMU) has a high noise level (> 100 pA); however, to fairly compare with other FEAs in literature, the turn-on voltage ($V_{GE,ON}$) is defined as the V_{GE} at I_A = 10 pA. This device has $V_{GE,ON}$ of 20 V, based on the extrapolation from the parameters obtained from the F-N plot (Fig. 8(b)). This device has a maximum current density ($J_{A,\,max}$) of 10 A/cm^2 at V_{GE} = 50 V, where the FEA area is 81×96 μm^2 for 150×150 sharp tips and their surrounding gate region. This max J_A is already higher than the state-of-the-art Si FEAs at the same V_{GE} bias [3]. Furthermore, the gate leakage (I_A) is less than 10% of the I_A at V_{GE} = 50 V, which is also better than Si FEAs [3].

The measurement results of other GaN FEAs are shown in Fig. 9 and 10. The GaN FEA measured in Fig. 9 has a similar design as the one shown in Fig. 8, thus the $V_{GE,ON}$ and J_A at V_{GE} = 50 V are similar. The output characteristics of this GaN FEA are also measured (Fig. 9 (b), (c)). Clear saturation is observed at V_{AE} > 80 V region, and the emitter current (I_E) is almost constant at a fixed V_{GE} (Fig. 9 (c)), suggesting that the field emission is mainly controlled by V_{GE}. The on-state resistance (R_{ON}) is about 34.5 Ω·cm^2 at V_{GE} = 44 V. The large R_{ON} and V_{AE} values are the result from the long d_{AE} distance (= 2 mm). Significant improvements in these values can be expected in the future by integrating the anode metal onto the devices. Though there is a trade-off between R_{ON} and breakdown voltage, since the channel is vacuum, the breakdown voltage can be still higher than most semiconductors. A 500-nm vertical vacuum channel length can easily sustain 300 V bias, while the R_{ON} can be much reduced because of a 4000x reduced vacuum channel length (from 2 mm to 500 nm).

The DC lifetime test is conducted on another GaN FEAs (Fig. 10(b)). The V_A is fixed at 500 V and V_{GE} is fixed at 45 V, and all current (I_E, I_G, and I_A) are monitored simultaneously. The anode current I_A is stable at around 11-12 μA after the initial 5 mins, and gate leakage I_G is also stable at around 180-200 nA. However, the device suddenly breaks after about 95 mins of the DC lifetime test without any observable increase of I_G before the breakdown. Though the cause of this breakdown requires more investigation; this device support a higher V_{GE} for DC lifetime because of the blunt-tip design at the periphery of this device [4],[5]. There are two possible hypotheses of this failure: (1) breakdown in SiO_2 layer on the covered blunt tips and (2) arcing due to the degassing from sputtered gate metal. Though the covered tips have blunt tip radius, the peak electric field in the SiO_2 layer can still be > 7 MV/cm at V_{GE} = 45 V (Fig. 4(b)). On the other hand, since the gate metal (Cr) is sputtered for conformal deposition, it has been known that gas can be trapped in the sputtered film during the deposition. Since the electric field near the sharp tips is very high (> 10 MV/cm in vacuum), the degassing can potentially cause arcing and break the device. To solve this instability issue, sub-100 nm lithography alignment and replacing sputtered gate metal by optimized e-beam evaporated gate metal will be necessary.

Our GaN FEAs are compared with prior III-N FEAs and other materials' FEAs (Fig. 11). The turn-on voltages ($V_{GE,ON}$) of our GaN FEAs have been comparable to other materials' FEAs. While the maximum current density (J_A) is still lower than the best Si FEAs (with max J_A of 100 A/cm^2) because of gate instability at high V_{GE} bias, the J_A of our GaN FEAs at the same bias conditions is already better than other devices in literature [3-6]. The J_A is at 0.3 – 0.6 A/cm^2 at V_{OV} = 20 V and J_A is at 3-10 A/cm^2 at V_{OV} = 30 V. This performance has been shown without the need of any complex current limiter structures [3], typical in high performance Si devices. With further optimizations, such as e-beam lithography for sub-100 nm alignment, e-beam evaporated gate metal, and integrated anode terminals for sub-μm vertical vacuum channel length, the III-Nitride FEAs can provide low-operation voltage, high current density, and high breakdown voltage simultaneously for high power and harsh environment applications.

IV. Conclusion

High performance GaN SAGFEAs with max J_A of 3-10 A/cm^2 at V_{GE} = 50 V are reported. Compared to other FEAs in the literature, these GaN FEAs have the highest J_A of 0.3-0.6 A/cm^2 (at $V_{GE} - V_{GE,ON}$ = 20 V) and J_A of 3-10 A/cm^2 (at $V_{GE} - V_{GE,ON}$ = 30 V). With further optimization, III-N FEAs can be used for high-power applications in the future.

Acknowledgment

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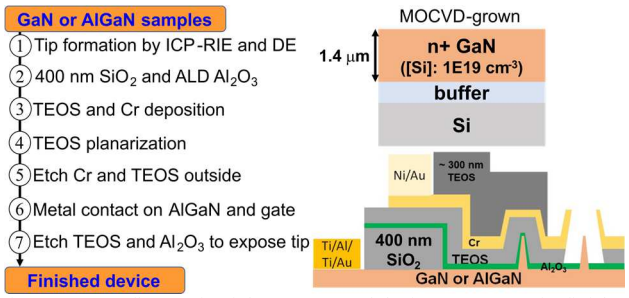

Fig. 1. Process flow, epitaxial structure, and device geometry of a finished GaN vertical FEA. Covered tips shown in cross-section device geometry are necessary to extend out the gate metal to the pad region.

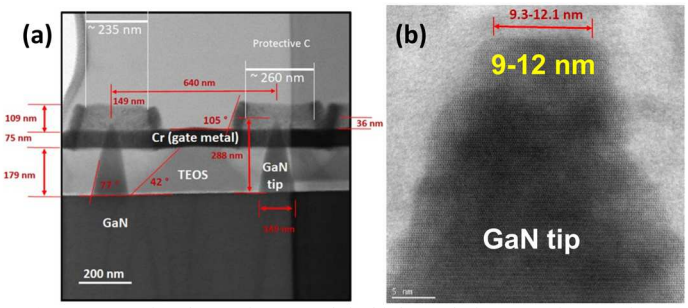

Fig. 2. (a) Cross-sectional SEM image and (b) high-resolution TEM image of a GaN tip. This device was reported in [4].

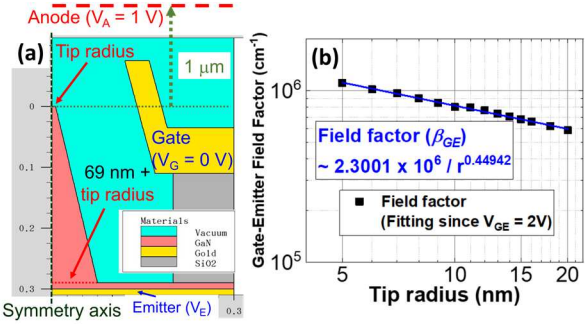

Fig. 3. (a) Device geometry and the (b) field factor simulated by Silvaco TCAD. The simulated structure is based on the cross-section SEM image in Fig. 2(a).

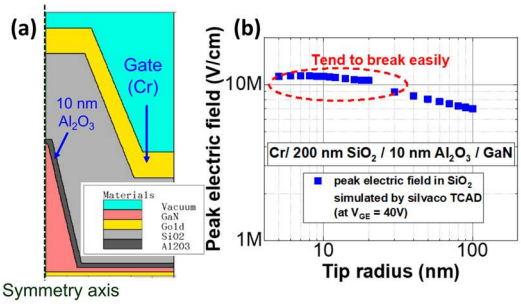

Fig. 4. (a) The MOS structure of the oxide-covered tip and (b) peak electric field in the SiO_2 layer vs. tip radius simulated by Silvaco TCAD.

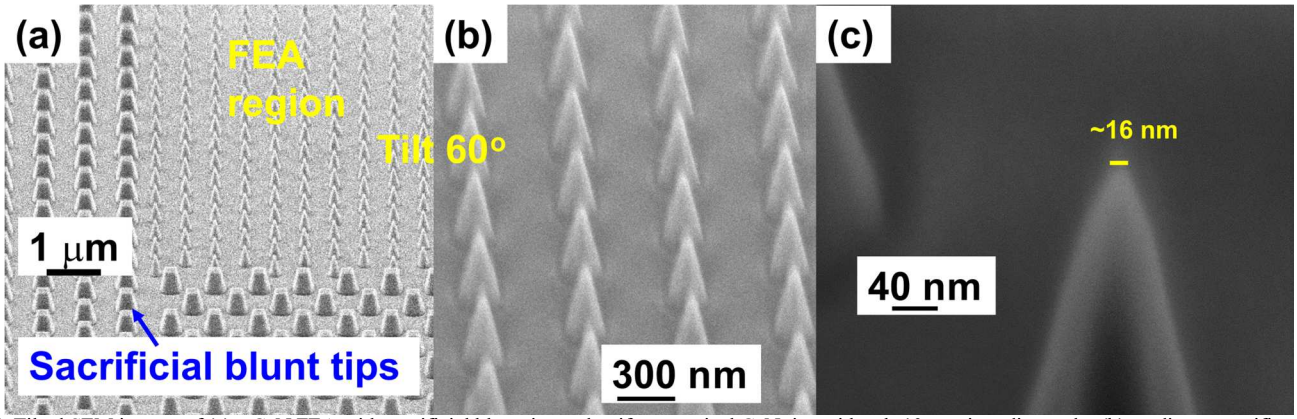

Fig. 5. Tilted SEM images of (a) a GaN FEA with sacrificial blunt tips and uniform vertical GaN tips with sub-10 nm tip radius under (b) medium magnification and (c) high magnification.

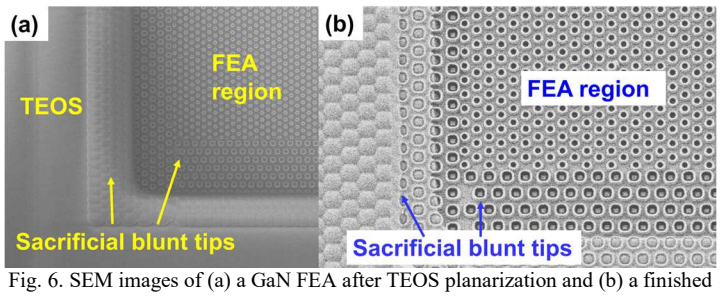

Fig. 6. SEM images of (a) a GaN FEA after TEOS planarization and (b) a finished GaN FEA.

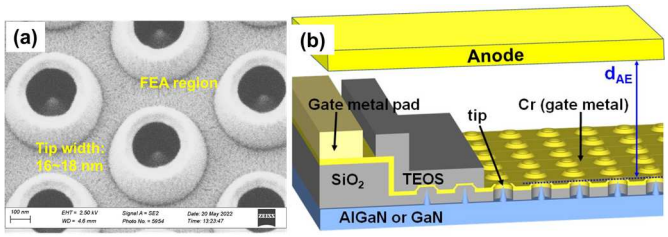

Fig. 7. (a) A zoom-in SEM image of a finished GaN FEA and (b) 3D illustration of a FEA with a suspended anode. In our measurements, the anode-emitter distance (d_{AE}) is fixed at about 2 mm in this work.

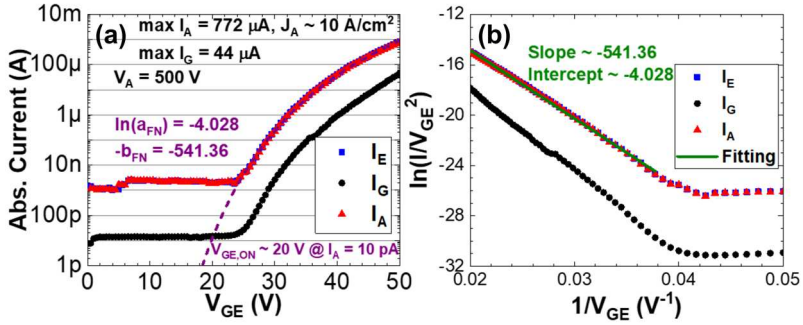

Fig. 8. (a) Transfer characteristics and (b) corresponding Fowler-Nordheim (F-N) plot of a GaN FEA with 150 × 150 sharp tips (with sub-10 nm tip radius). The FEA area is about 81 × 96 µm². This FEA has maximum J_A of 10 A/cm² at V_{GE} = 50 V. The turn-on voltage ($V_{GE,ON}$) of 20 V is extrapolated at I_A = 10 pA based on intercept (ln(a_{FN})) and slope (-b_{FN}) in (b).

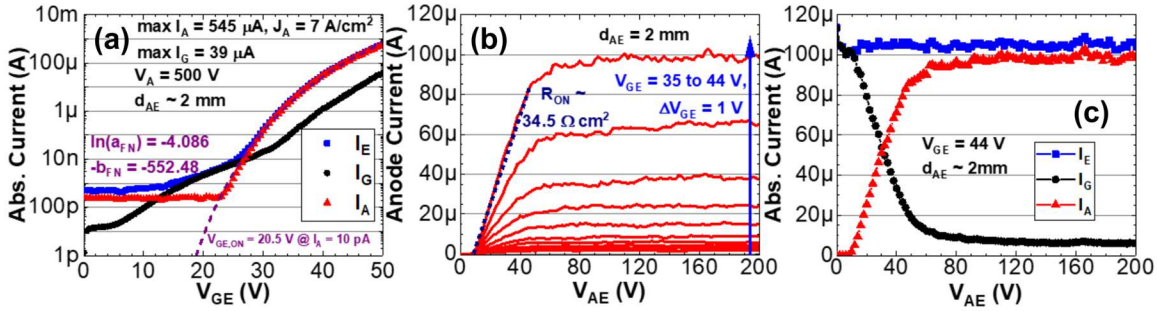

Fig. 9. (a) Transfer characteristics and (b) (c) output characteristics of a GaN FEA with 150 × 150 sharp tips (different from the device in Fig. 8). Saturation in the output characteristics is clearly observed. I_A of 100 µA is equal to J_A of about 1.3 A/cm². R_{ON} is about 34.5 Ω cm² for V_{GE} = 44 V at d_{AE} = 2 mm.

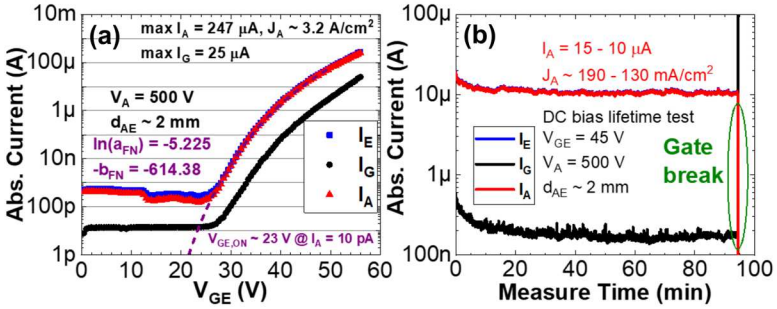

Fig. 10. (a) Transfer characteristics and (b) DC lifetime test of another GaN FEA with 150 × 150 sharp tips (different from Fig. 8 and 9).

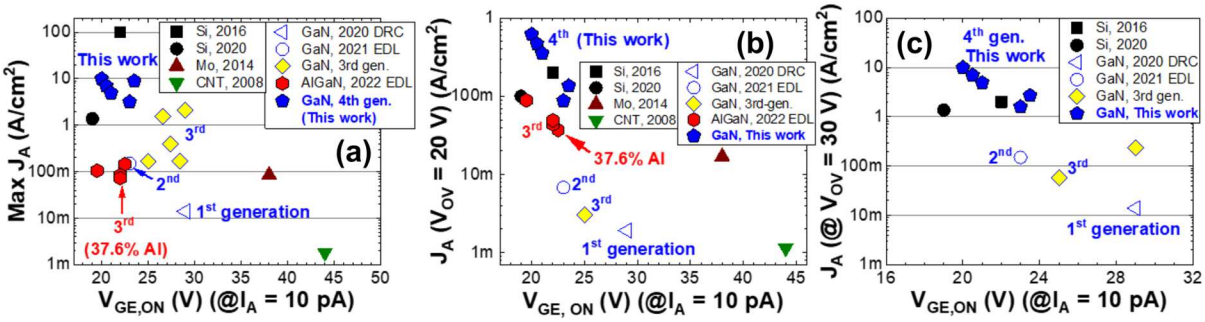

Fig. 11. Benchmark plots of (a) max J_A (b) J_A at V_{OV} = 20 V and (c) J_A at V_{OV} = 30 V among different materials' FEAs. The overdrive voltage (V_{OV}) is defined as $V_{OV} = V_{GE} - V_{GE,ON}$. The turn-on voltage ($V_{GE,ON}$) is defined at I_A = 10 pA for fair comparison [3-6]. GaN FEAs reported in this work have a higher J_A at the same $V_{GE} - V_{GE,ON}$ bias condition than the state-of-the-art Si FEAs. Some devices are not shown in (c) since they don't have data at V_{OV} = 30 V.