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Anode-Integrated GaN Field Emitter Arrays for Compact Vacuum Transistors

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***Abstract*— Field-emission-based vacuum transistors have been proposed as promising candidates for future high-power and harsh-environment electronic devices. However, the lack of an integrated anode is still an issue for vertical field-emission vacuum transistors for some applications such as radiation-hard vacuum-electronic-based circuits. In this work, an anode-integration technology enabled by tilted metal deposition is proposed and experimentally demonstrated on GaN gated field emitter arrays (FEAs). Full transistor prototypes with a 10^3 on-off ratio in anode current are demonstrated. This process is compatible with gated FEAs of various materials, the vacuum channel can be sealed during fabrication, and the vacuum channel length can be controlled via multiple process parameters.**

***Index Terms*— field emission, anode integration, vacuum transistor, GaN**

I. Introduction

VACUUM electronics have been replaced by solid-state electronics in most fields over the last 75 years. However, because of the scattering-free transport and high breakdown field of a vacuum channel, vacuum electronics are still used in high-frequency, high-power, and harsh-environment applications [1]–[3]. While some applications, such as electron sources, X-ray tubes, and space electric propulsion, may not require compact structures with an integrated anode [4]–[8], the compact and integrated device structure is necessary for circuit-level applications, such as vacuum-electronics-based circuits for harsh environments.

Different types of field-emission devices, such as tunneling-junction-based electron emitters and self-aligned-gate field emitter arrays (SAGFEAs) have been developed over years [9]–[14]. The tunneling-junction-based emitters have simple structures and low working voltages, but their performance are usually not desirable as vacuum transistors because of high leakage current [9]–[11]. SAGFEAs, on the other hand, have shown better transfer characteristics as vacuum transistors [12]–[14]. The recently developed III-Nitride SAGFEAs have achieved anode current densities ($\sim$ 10 A/cm^2) that are comparable with the state-of-the-art Si SAGFEAs at the same bias condition [15]. However, anode integration is still largely missing in these devices for circuit-level applications. In fact, the few devices that demonstrate anode integration still (1) require significant performance improvements [16], [17], (2) were based on two-terminal device [18], [19], or (3) still required vacuum packaging after device fabrication [3], [17], [20]–[22]. In this work, an approach combining e-beam lithography (EBL) and tilted metal deposition is proposed to demonstrate compact field-emission-based vacuum transistors. Tilted metal deposition has been used to fabricate metal field emitters and shows the formation of an empty cavity between the metal emitter and the upper metal layer [23]. However, there is very limited demonstration with the upper metal as the anode terminal, and the anode formation is coupled with the emitter fabrication in prior work [16]. In this proposed technology, the anode formation is decoupled from emitter fabrication, and the vacuum cavity can be potentially sealed during the device fabrication [16], [23], leading to relaxed restrictions on package and circuit-level prototypes [24].

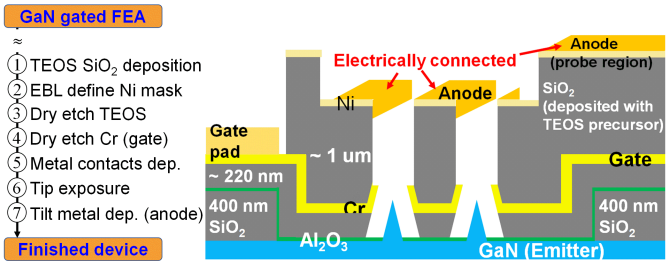

Fig. 1. Process flow and cross-section diagram (not to scale) of the proposed device. Process flow of GaN gated FEAs can be found in prior work [15], [25].

II. Device Fabrication

The gated GaN field emitter arrays (FEAs) are fabricated on GaN-on-Si coupons. The process steps can be found in Ref [15], [25] up to the SiO_2 and Cr deposition steps (gate metal deposition). GaN emitter tips with $\sim$ 20-nm tip width are formed by dry etching and sharpened by wet-based digital etching [26]. Key fabrication steps and the final structure of anode-integrated GaN vacuum transistors are shown in Fig. 1.

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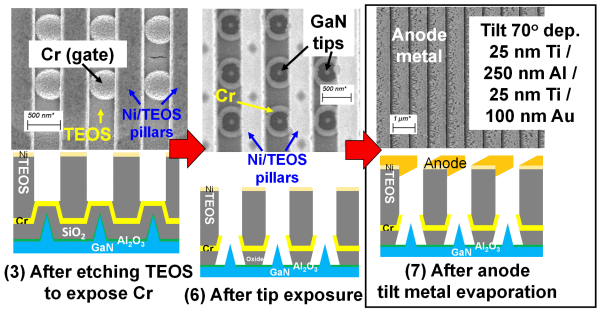

Fig. 2. Scanning electron microscope (SEM) images and device geometries after different fabrication steps. The SEM images confirm that the proposed process flow works as expected.

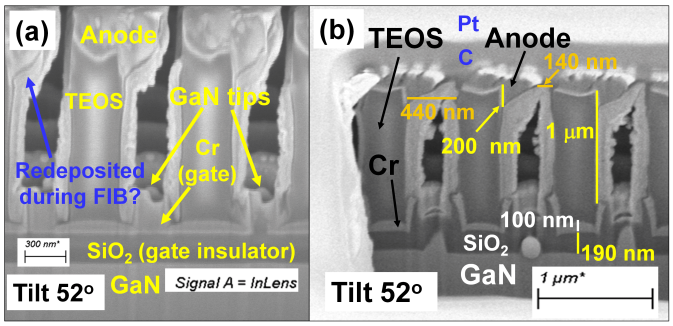

Fig. 3. Cross-sectional SEM images of devices (a) after fabrication and (b) after measurement. The cross sections are cut by a Ga focused ion beam (FIB). The Pt and C are deposited by the electron and Ga-ion beams before ion beam milling to protect structures. The materials on the sidewalls of TEOS pillars are probably the results of re-deposition after Ga ion sputtering. It should be noted that GaN tips shown in (b) does not show the apex of emitter tips since it is hard to align on the tip apex during the FIB cutting. TEM preparation might be necessary in the future to confirm the precise tip shape and structure geometries [15].

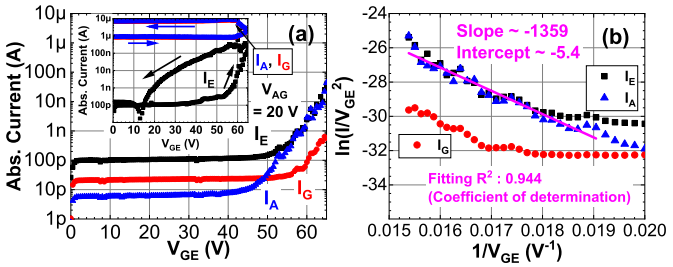

Fig. 4. (a) I-V characteristics and (b) corresponding Fowler-Nordheim (F-N) plot of I-V curves for the fabricated devices. After a few measurements, a leakage path formed between the anode and the gate as shown in the inset. The field-emission-dominant conduction for anode current (I_A) is confirmed by the F-N plot, but the noise and steep F-N slope might indicate the device is not yet fully conditioned.

After gate stack deposition, (1) a thick ($>$ 1 µm) layer of SiO_2 is deposited by plasma-enhanced chemical vapor deposition (PECVD) with a tetraethyl orthosilicate (TEOS) precursor. The oxide layer is then thinned down to $\sim$1 µm by CF_4/H_2-based inductively coupled plasma-reactive ion etching (ICP-RIE). (2) Next, the Ti/Ni hard mask for the subsequent SiO_2 and Cr dry etching is defined by EBL with a lift-off process. Based on the pitch of GaN field emitter tips and the designed patterns of Ti/Ni hard mask, an EBL alignment error below 100 nm is critical in this step. 300-nm-high GaN cross-bar mesas are etched and used as alignment marks in this work. A misalignment error below 100 nm is typically achieved in our EBL system, an Elionix ELS-HS50. (3) The SiO_2 layer is then etched by CF_4/H_2-based ICP-RIE until the gate metal is exposed (step (3) in Fig. 2) before (4) using Cl_2/O_2-based ICP-RIE to etch the gate metal (Cr). (5) After patterning the gate, the ohmic metal contact (Ti/Al/Ti/Au) and gate pad metal (Ni/Au) are defined by a lift-off process. A thick ($>$ 5 µm) photoresist layer is patterned to serve as both a dry etch mask and an undercut layer for anode metal lift-off. (6) The SiO_2 layer is then etched by CF_4/H_2-based ICP-RIE to expose the tips, and the 10-nm atomic layer deposited (ALD) Al_2O_3 layer is etched by a tetramethylammonium hydroxide (TMAH)-based developer for 5 min. Since the SiO_2 pillars are important, an HF-based etchant cannot be used to remove the Al_2O_3, which differs from the prior work in [15], [25]. It should be noted that since the devices are fabricated on small coupons, non-uniformity in some process steps from the corners of the sample to its center is observed. Therefore, we only focus on the devices at the center of the sample in this preliminary work.

The device after tip exposure is shown in Fig. 2 (step 6). It should be noted that the etching rates of TMAH-based developer on GaN and Al_2O_3 were not explicitly measured, so there may be residual Al_2O_3 on the GaN tips which may affect emission. Finally, (7) the metal layer for anode formation is deposited through tilted e-beam evaporation at an angle of 70°, and the metal on the undesired regions is lifted off by thick resist. The finished device is shown in the step (7) of Fig. 2. The cross section of the finished device is obtained by Ga focus ion beam (FIB) and is checked by SEM (Fig. 3(a)). In this work, the vacuum channel length is about 1 μm. This channel length can be controlled through multiple parameters, such as the thickness of TEOS SiO_2 pillars, the pitch of these pillars, and the tilt angle of the anode metal deposition. It should be noted that one gated FEA has multiple vacuum channel cavities (Fig. 3). There is no clear channel length variation observed within the FEA studied in this work, but the uniformity of both TEOS SiO_2 deposition and anode metal deposition and the pitch size uniformity of TEOS SiO_2 pillars can affect channel length of different devices across large area. The vacuum cavity can also be closed during the device fabrication, although more work is necessary in the future to investigate this vacuum cavity sealing approach.

III. Results and Discussion

After the device is checked by SEM (Fig. 3(a)), the sample is then loaded into an ultrahigh vacuum (UHV) measurement chamber with a base pressure of 1-2 $\times$ 10^{-9} torr. The I-V characteristics and the corresponding Fowler-Nordheim (F-N) plot are shown in Fig. 4. This device has 150 $\times$ 150 GaN emitter tips. It should be noted that instead of a fixed anode-emitter voltage (V_{AE}), the anode-gate voltage (V_{AG}) is fixed at 20 V to reduce the impact of the emitter current (I_E) on the gate leakage (I_G) at high V_{GE} if $V_{AG} < 0$ V, which has been mentioned in prior work [21]. Based on the I-V curves, most

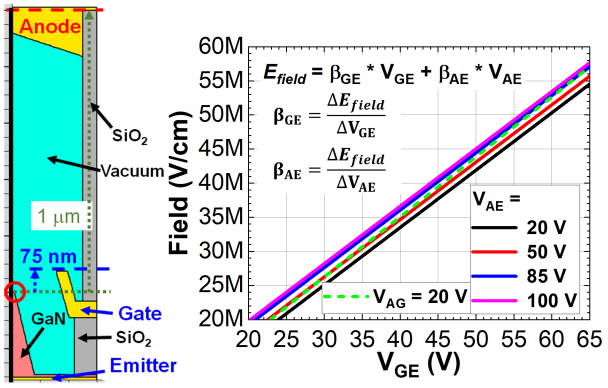

Fig. 5. Simplified structure used in TCAD simulations and a plot of the peak electric field at the emitter tip (red-circled region). The tip and gate structures are built based on prior work [15]. The black line is the cylindrical-symmetry axis. Green dashed line in the plot represents the same bias condition as measurements in Fig. 4. The GaN tip radius is set to be 10 nm for 20-nm tip width, which was confirmed by SEM before the gate stack deposition. Electric field is affected by both $\boldsymbol{V_{GE}}$ and $\boldsymbol{V_{AE}}$, while the effect from $\boldsymbol{V_{AE}}$ ($\boldsymbol{\beta_{AE}}$ =3.9×10^4 cm^{-1}) is less than 5% of the one from $\boldsymbol{V_{GE}}$ ($\boldsymbol{\beta_{GE}}$ =8.4×10^5 cm^{-1}).

current flows between the anode and the emitter while the gate leakage (I_{G}) is less than 10 % of the I_{A} before the anode-gate leakage path forms (Fig. 4(a)). The anode current has an on-off ratio greater than 10^3 over the range V_{GE} = 45-65 V, which is, to the best of the authors' knowledge, hardly demonstrated in prior work with locally integrated anodes [16], [17]. Each one of the three terminals has different noise level due to the different setting of the respective source measure unit (SMU). The anode (V_A) is set to 20 V, while the gate (V_G) is set to 0 V, and the emitter (V_E) is swept to negative voltage, leading to a higher noise level in I_E than I_A and I_G. The F-N plot (Fig. 4(b)) confirms that the anode and emitter current conduction is dominated by the field emission mechanism. However, the noisy current may indicate that the GaN emission tips are not yet fully conditioned.

Repeated I-V sweeps have been shown in the past to condition GaN SAGFEA and increase its current levels [15]; however, after a few measurements on this anode-integrated GaN SAGFEA, the anode-gate leakage suddenly increases and dominates the device behavior (inset plot in Fig. 4(a)), but there is no noticeable jump in the UHV chamber pressure. If the electrons impacting different surfaces have high enough kinetic energy, a surface leakage path may form on SiO_2 pillars due to defects generated by the high-energy electrons [21] or from electromigration. However, no noticeable damage or device distortion was observed via top-view SEM (not shown here) and cross-section cut by Ga FIB (Fig. 3(b)). More investigation is therefore necessary to understand the cause of this anode-gate leakage formation. Because the device fails before it is fully conditioned, it is hard to estimate the electron emission uniformity of the FEA and its maximum current capability.

Since the I-V characteristics are conducted with fixed V_{AG} instead of fixed V_{AE} to reduce the impact of leakage current between gate and emitter, a simplified Silvaco TCAD electrostatic simulation is used to confirm that the electric field at the GaN emission tip is still primarily controlled by V_{GE} (Fig. 5). In this simulation, the anode-gate distance is set to $\sim$ 1 μm. The electric field on the emitter tip ($\vec{E}$) can be expressed as $\vec{E} \sim \beta_{\mathrm{GE}} \cdot V_{\mathrm{GE}} + \beta_{\mathrm{AE}} \cdot V_{\mathrm{AE}}$. The β_{GE} and β_{AE} are field factors representing the effects on electric field from the V_{GE} and V_{AE}, respectively. The field factors can be extracted based on the relation: $\beta_{\mathrm{GE}} = \frac{\Delta \vec{E}}{\Delta V_{\mathrm{GE}}}$ and $\beta_{\mathrm{AE}} = \frac{\Delta \vec{E}}{\Delta V_{\mathrm{AE}}}$. Based on the simulation results (Fig. 5(b)), β_{AE} is extracted to be $3.9 \times 10^4\,\mathrm{cm}^{-1}$, which is less than 5 % of the β_{GE} (= $8.4 \times 10^5\,\mathrm{cm}^{-1}$). Therefore, though the I-V characteristics shown in Fig. 4(a) are not transfer characteristics, based on the TCAD simulation (Fig. 5), these I-V curves reasonably represent the device behavior. A different simulation with $\sim$ 500-nm anode-gate distance is also conducted to estimate the effect of vacuum channel length variation. The β_{AE} is extracted to be $6.8 \times 10^4\,\mathrm{cm}^{-1}$ and the β_{GE} is about $8.8 \times 10^5\,\mathrm{cm}^{-1}$. Therefore, small variation in channel length does not significantly affect, in first order, the gate control on electron emission.

The preliminary experimental fully-integrated vertical GaN vacuum devices presented in this manuscript demonstrate the transistor-like behavior. However, more work is still necessary in the future to understand the conditioning mechanism of GaN FEAs and the cause of anode-gate leakage formation. The investigation of different dielectric materials, such as SiN_x, for insulator pillars is also important. Furthermore, the use of a vacuum sealing technology in the future is critical [24], for which Ti getters may be necessary to maintain these vacuum cavities at the expense of more complex device structure and fabrication [19]. Prior work on vacuum cavities sealed by semiconductor fabrication technologies has shown that, if properly designed, the vacuum cavity pressure can be maintained, but more study is necessary to confirm the precise pressure in the cavity [18].

IV. Conclusion

Fully-integrated GaN field-emission-based vertical vacuum transistors are proposed and experimentally demonstrated. A novel integration scheme for the anode terminal based on tilted metal deposition is developed and is compatible with gated FEAs of different materials. Transistor-like behavior with 10^3 on-off ratio in anode current is achieved, while the gate leakage is less than 10 % of anode current before the anode-gate leakage formation. More research is still necessary to understand the cause of the anode-gate leakage and the proper conditioning procedure for GaN gated FEAs before or during the anode formation. With this understanding and further optimizations on process and device structures, these vacuum transistors can be great candidates for vacuum-electronic-based circuit aiming for harsh-environment applications, such as radiation-hard devices and systems.

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