A PHASE-LOCKED LOOP FOR LASER SCANNERS

by

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ABSTRACT

The Autokon 8400 is a laser scanner used in the graphic arts to scan, digitize and reproduce images. The scan is non-linear, and this presents difficulties in placing picture elements evenly spaced on the page. A grating and a phase-lock loop (PLL) compensate for the non-linearity.

The PLL tracks the frequency and phase of a signal, known fairly well in advance, coming from the grating. This document examines a method of predicting the present grating signal frequency from past frequency values, updating the voltage controlled oscillator (VCO) voltage on an open loop basis, and correcting for deviations from the prediction using a conventional feedback loop. The grating signal appears in bursts, and it is necessary to acquire lock at the edge of each burst. A fast lock technique is introduced to lock close to the edge of the pulse burst.

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I dedicate this work to my parents and to my friends at TCC.

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1. INTRODUCTION

In some laser scanners used in the graphic arts, non-linear deflection is provided by a galvanometer. In graphic arts applications, spatial linearity is necessary to place each picture element (pel) in its proper location on the page. Present systems such as ECRM's Autokon 8400 Laser Scanner, scan a grating concurrently with the image; the grating scan records the spatial location information while the image scan records the video information. A variable divide-by-N phase-lock loop tracks the signal created by the grating scan. Since the PLL needs to acquire lock before its output, the spatial location of the pel being scanned, will become valid, the grating dimensions must be grater than the dimensions of the image to be scanned. The faster the loop locks, the smaller the extra section of the grating allowed for acquisition. The PLL must track a smoothly changing frequency with negligible phase error. Significant phase error will create artifacts in the image. Present systems use a third order loop to provide good tracking and low phase error. In this application, the scanning frequency and the dimensions of the grating are known; therefore, the PLL input signal is known rather well at any location on on the grating. If some prediction of the input signal is used, it should be possible to track the varying input frequency with low phase error using only a second order loop.

This document discusses a new PLL design using a first order filter (a second order loop), additional prediction circuitry, and additional circuitry to aid rapid acquisition. Chapters two through four present a general overview of phase-lock loops in laser scanners, a general discussion of phase-lock, and a discussion of existing systems. Later chapters discuss the PLL under design. Grating frequency (the PLL input signal) at various spatial locations on the grating and values stored in lookup tables are listed in the appendices. Circuit diagrams are also included in appendix D.

2. THE LASER SCANNER

The laser scanner produces screened images from an opaque original, either continuous tone or line art, as an intermediate step in making printing plates. The output is either film or paper; it also has a computer interface facilitating its use in image processing systems.[1] [2]

2.1 SCANNING

The Autokon accepts input 12 inches by any length. Input and output are scanned back and forth in the 12 in direction sinusoidally, not linearly, at 60 Hz. Lengthwise scan is accomplished by paper and film motion. The image can be reduced or enlarged from 20 to 200 percent. Magnification in length is achieved by moving the output at a variable speed (2.5 to 25 in/min in the Autokon 8400) and the output at constant speed (5 in/min in the Autokon 8400). Magnification in width is achieved by the the variable divide-by-N counter in the PLL, sampling the input at a variable rate (144 to 1440 pels/in in the 8400) at the input and at a constant rate (722 pels/in) at the output. [1]

2.2 LINEARITY OF THE SCAN

Ideally a linear scan is desired, placing consecutive samples on the line an equal distance from the last sample. Instead a sinusoidal scan has been used, in itself nonlinear in time. (See Figure 1, where x is the spatial location on the grating, w is the scanning frequency, θ_m is the maximum angle of deflection, θ is the angle of deflection at any x, and F is the focal length.)

For example, if samples were placed x inches apart on the scan line and the scan starts at the edge of the line, it will take $t_1 - t_2$ seconds to move from pel one to pel two but $t_3 - t_2$ seconds to move from pel two to pel three. (Figure 2). The frequency is higher in the center than at the edges; hence it takes longer to move from one pel to another at the edges than at the center. Even though the pels are equal distances apart on the page, they are not equally spaced in time.

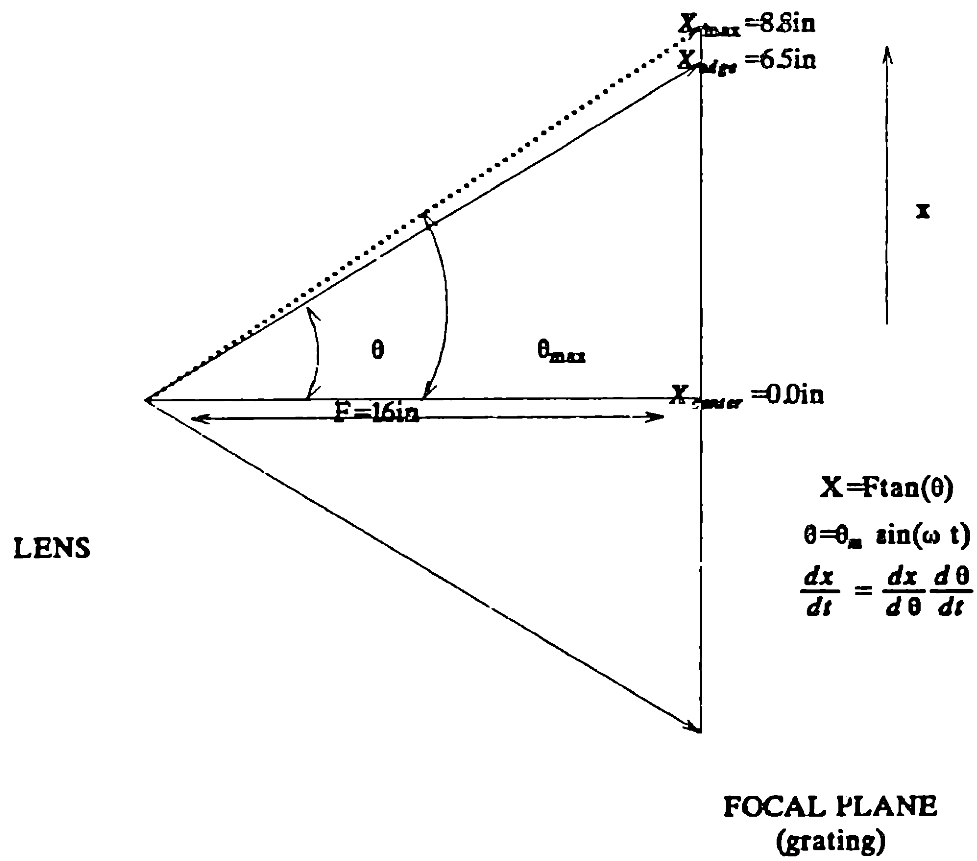
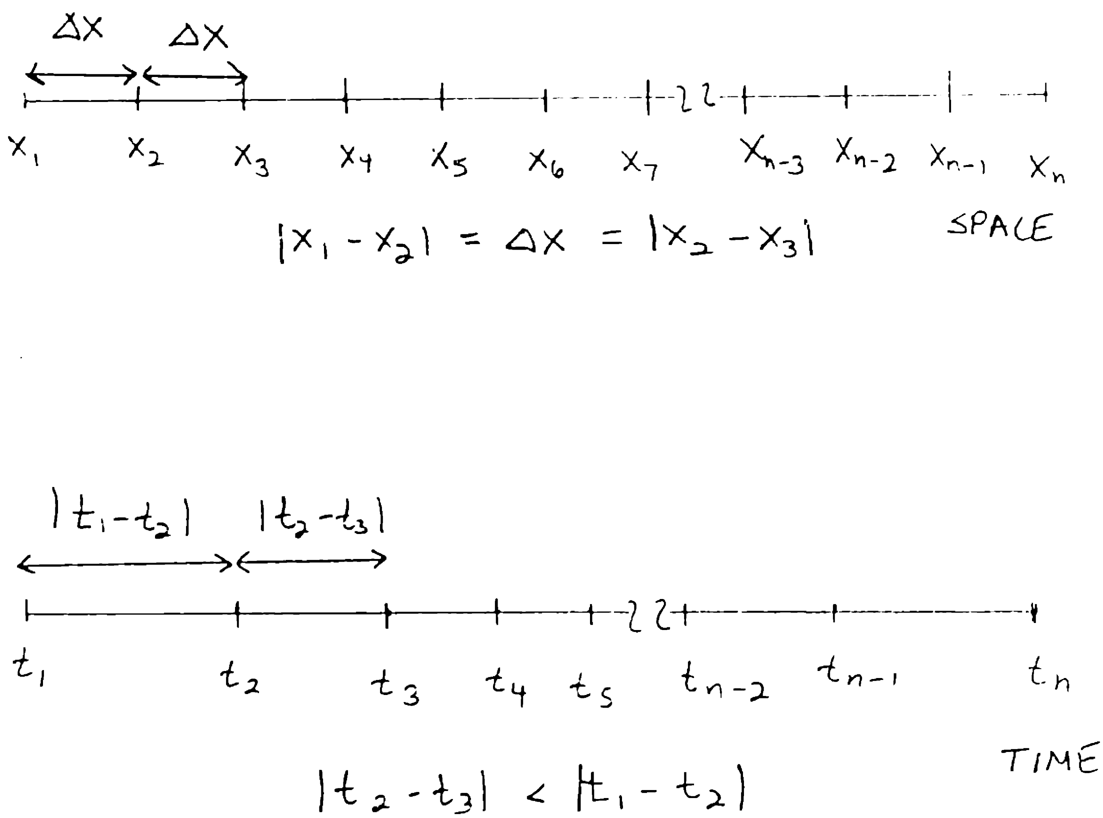


Figure 1 Sinusoidal Scan

Does it matter that the scan is not linear in time? No, not if the image can be recorded and reproduced such that the pels are linearly spaced on the page. In this system an analog video signal that contains the scanned picture information is digitized by an analog to digital converter (ADC) and stored in a buffer; then a digital to analog converter converts (DAC) the information stored in the buffer to an analog signal that is used to modulate the recording laser beam. An important consideration is what should be used as a clock for the ADC and the DAC. If the signal is sampled at a fixed frequency, samples will be equally spaced in time hence not equally spaced on the page. It can be concluded that a fixed frequency clock is not acceptable. However, it is possible to create a clock signal such that the samples will be stored in the buffer corresponding to pels equally spaced on the page.[3]

Figure 2 Time and Space on the Grating



The Autokon 8400 uses a grating or mesh of 216 lines per inch with consecutive lines placed equal distance apart. The image and grating are scanned at the same time. Video information is recorded from the scan of the image while the grating scan records the location of the beam. It is this location information that is used to create a clock for digitization.

This system is shown in Figure 3.[2] The laser beam goes through a beam splitter creating two beams. One scans the image and the other scans the copy. The image information is recorded by a photodiode that creates the analog video signal. The grating is scanned, creating a grating signal that is amplified and sent to a PLL. The output of the PLL is the clock signal.

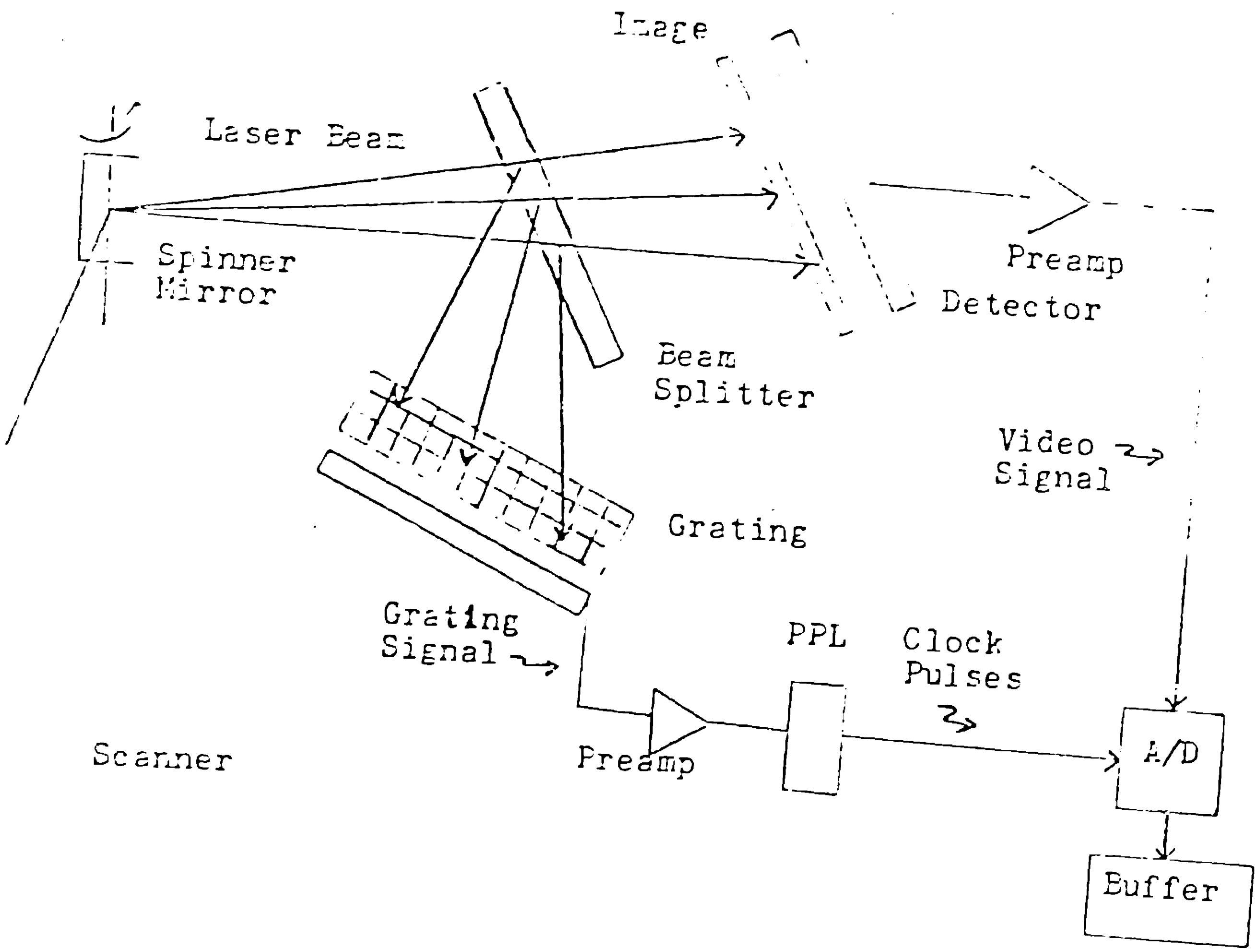
2.3 PURPOSE OF THE PLL

The grating scheme is now obvious, but what is the purpose of the PLL? Without the PLL, a grating of one line per pel is necessary; a very fine grating is needed; optically this presents a problem. Magnification presents problems as well making it necessary to vary the frequency of the clock in small steps over a large range. In addition the grating signal is noisy. Since the PLL acts as a low pass filter it eliminates much of the noise. By adding a scaling factor of N in the feedback loop of the PLL, the clock frequency can be made to be N times the grating frequency. There can by many pels, not just one, per grating bar. Magnification is made possible by adding additional scaling by making N variable. (In the 8400, N varies from 20 to 199. Initially the input frequency is scaled by 100 and then multiplied by a factor varying from 2 to 199.)[3]

2.4 PROBLEMS THAT A PLL PRESENTS

What does the signal that the PLL wants to track, the grating signal, look like? The grating signal occurs in bursts, one corresponding to each scan line, surrounded by blank intervals during which no signal is present. At the beginning of each line the loop needs to acquire lock to track the signal in frequency and phase. In the Autokon the signal is already fre-

Figure 3 The Laser Scanner



quency locked at the edge of the line but still needs to acquire phase-lock. It takes ten grating bars for the loop to acquire lock, about half an inch. A thirteen inch grating is used for a 12 inch wide image. Obviously it is desirable to lock as close to the edge of the page as possible. It is possible to design for faster lock-on, but this also results in poorer reference suppression and increased jitter. Any significant phase error is undesirable since it creates artifacts in the image. It is also necessary to track a changing input frequency. (The grating pulses are placed equally in space but not in time). If the frequency is slowly changing it can be approximated by a linear change in frequency which can be tracked. In a conventional PLL a third order loop with a second order filter is necessary to track a frequency ramp. The third order filter has stability problems. Low gain will place poles in the right half-plane and the loop will oscillate; it is important to design for a gain high enough to make the loop stable. [3]

3. GENERAL PLL THEORY: SOME BACKGROUND

3.1 INTRODUCTION TO PLL

A phase-lock loop tracks the frequency and phase of an input signal (See Figure 4); frequency can be tracked precisely, but phase may be tracked with a finite error. A PLL is very useful in recovering a signal imbedded in noise; it acts like a low pass filter, passing the signal and rejecting noise. The bandwidth of the loop can be varied; as bandwidth decreases the noise rejection increases. In a variable divide-by-N PLL, small increments of frequency can be tracked over a large frequency range[4]

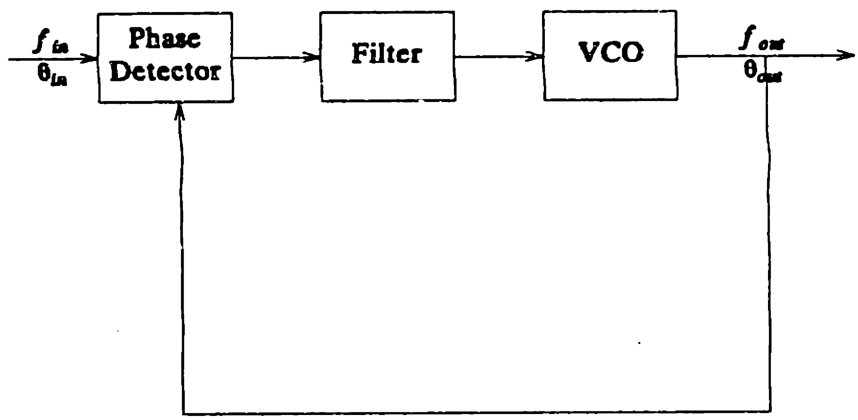


Figure 4 Block Diagram of a PLL

A PLL has three states: free-running, acquisition (sometimes called capture) and locked. In the first state the loop is free-running at the center frequency of the VCO; the output frequency is independent of the input frequency. During acquisition the loop starts from the unlocked or free-running state and tends toward the locked state. When the loop progresses from the free-running state to capture, the output of the phase detector is a voltage proportional to the difference between the input and output frequencies. The low pass filter removes the high frequency components to produce the control voltage that "controls" the output frequency, moving it closer to the input frequency. The output frequency does not equal the input frequency until the third state at which time the loop is locked. (The difference between phase-lock and frequency lock will be discussed in the section on acquisition.)[5]

32 A SINUSOIDAL PLL IN THE TIME DOMAIN

The fundamental principles of PLL operation can be better understood by looking at its operation in the time domain. Given the sinusoidal system in Figure 5, assume that the PLL is unlocked, meaning that the output is not synchronized to the input. θ_i and θ_o are the input and output phase; w_i and w_o are the input and output frequencies. Since it has been assumed that the PLL is initially locked, two assumptions can be made. One, w_o is simply the free-running VCO frequency w_{center}, and two, w_o and θ_o are independent of w_i and θ_i.

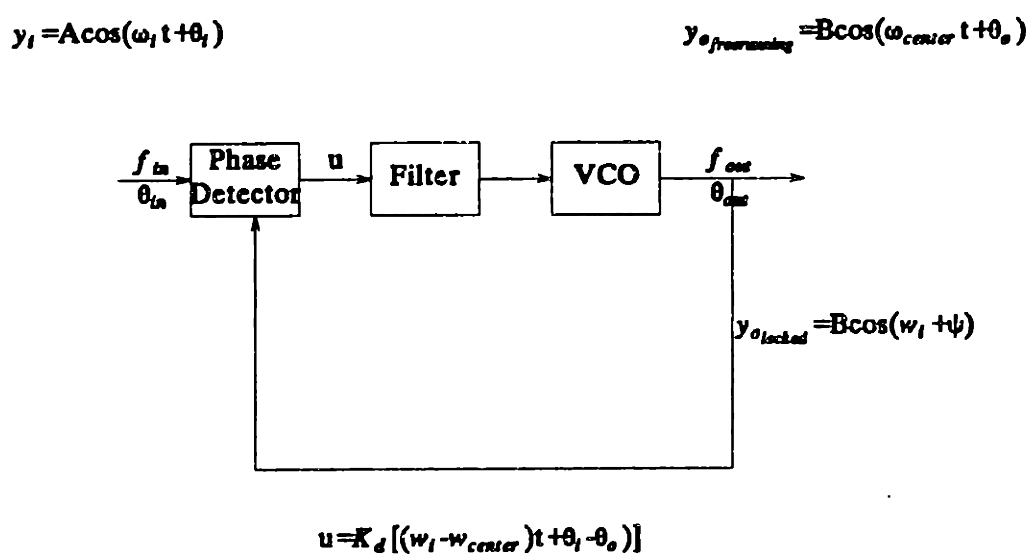


Figure 5 Sinusoidal PLL

The input and output signals are given by

$$y_i(t)=A\cos(w_i t+\theta_i) \quad \text{and} \quad y_o(t)=B\cos(w_{center} t+\theta_o)$$

where A and B are constants.

The phase detector output is given by

$u(t)=K_d \cos[(w_i - w_{center})t+\theta_i-\theta_o]$ where K_d is the phase detector gain.

As has been stated previously, if $w_i - w_{center}$ is not too large, w_o will change from w_{center} and eventually equal w_i. When $w_o = w_i$ the output $y_o(t)$ is synchronized with the input $y_i(t)$. Both the input and output have the same frequency w_i but differ in phase. The output signal is given by

$$y_o(t)=B\cos[w_i t + \psi]$$

where ψ is the output phase (when the output is synchronized in frequency with the input). The output phase is given by the sum of the initial output phase θ_o and a term proportional to time by an amount equal to the difference between the input and center frequencies or

$$\psi = \theta_o + (w_{center} - w_i)t$$

But how does this voltage control the output frequency of the VCO? The output frequency varies from the center frequency of the VCO by an amount proportional to the control voltage $V_c(t)$ by a factor K_o where K_o is the gain of the VCO. At any time the instantaneous angular output frequency w_{inst} can be expressed as the time derivative of the output phase.

$$w_{inst} = d/dt[w_{center} t + \theta_o] = w_{center} + d\theta_o/dt$$

then

$$d\theta_o/dt = K_o V_c \quad \text{and } w_{inst} = w_{center} + K_o V_c.$$

Now it can be seen that when the loop is locked, the instantaneous output frequency of the VCO is linearly proportional to the control voltage V_c. Still, what causes the output to track the input? It becomes more obvious if it can be shown that the control voltage is proportional to the difference between the input frequency and the free-running frequency of the VCO, that is

$$V_c = [w_i - w_{center}]/K_o$$

and then

$$w_{last} = w_{center} + K_o\ [w_i - w_{center}]/K_o = w_i .$$

But, the time derivative of output phase is given by

$$d\theta_o/dt = d/dt[(w_i - w_{center})t + \psi] = w_i - w_{center}$$

and

$$d\theta_o/dt = K_o V_c$$

therefore

$$(w_i - w_{center})/K_o = V_c .$$

Lastly, the output phase is no longer independent of the input but is dependent on the input phase and frequency. Since V_c is simply a low pass filtered version of a dc signal u, V_c equals u and

$$w_i - w_{center} = K_o\ u = K_o K_d\ \cos(\theta_i - \psi) \text{ then}$$

$$\psi = \theta_i - \arccos[(w_i - w_{center})/K_o K_d].$$

Note that if

$$K_o K_d$$

is significantly greater than

$w_i - w_{center}$,

$$\frac{(w_i - w_{center})}{K_o K_d}$$

is approximately zero, and

$$\psi = \theta_i - 90 \text{ degrees}$$

or the output is 90 degrees out of phase with the input. [8]

3.3 TRACKING AND ACQUISITION

What are tracking and acquisition? Are they linear or non-linear? When the PLL is tracking, it is locked; the output is following the input frequency and output phase is dependent on the input frequency and phase. Tracking can be modeled as a linear phenomenon. Acquisition, however, is nonlinear. The output frequency is no longer free-running but is moving toward the input frequency (though still not locked). [6]

3.3.1 TRACKING

Consider the tracking behavior of the PLL. Assume that the loop is synchronized (locked) and change the input frequency or phase. What happens? How does the loop track changes at the input?

The PLL can be represented by the system in Figure 6 where the variables are defined using Laplace notation where $\theta_o(s)$ is defined as $L[\theta_o(t)]$. Given the following:

$$V_d(s) = K_d[\theta_i(s) - \theta_o(s)]$$

$$V_c(s) = F(s)V_d(s)$$

$$\theta_o(s) = K_o V_c(s)/s$$

where K_d is the phase detector gain, K_o is the VCO gain, θ_i is the input phase, and θ_o is the output phase, it is possible to arrive at the following relationship between input and output

$$\theta_o(s)/\theta_i(s)=K_o K_d F(s)/[s+K_o K_d F(s)]$$

$$[\theta_i(s)-\theta_o(s)]/\theta_i(s)=\theta_e(s)/\theta_i(s)=s/[s+K_o K_d F(s)]$$

$$V_c(s)=[s K_d F(s)\theta_i(s)]/[s+K_o K_d F(s)]$$

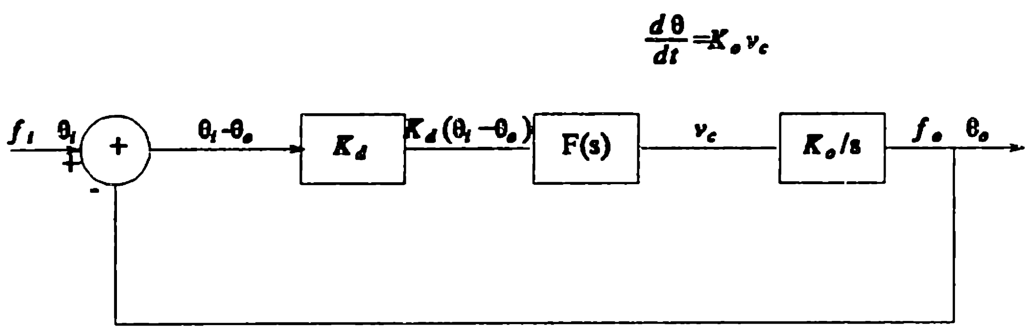
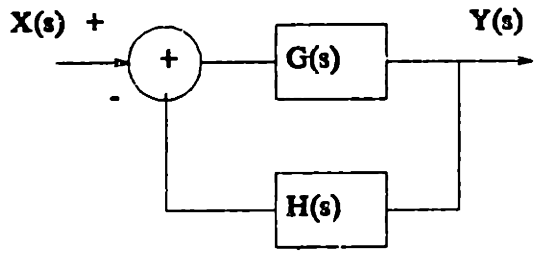


Figure 6 A Block Diagram of a PLL in the S Domain

Before examining the transient and steady state phase error $\theta_e(s)$, it is worthwhile to define the type and order of a PLL. Given that the PLL can be represented in more general terms by the feedback system in Figure 7 the type is defined by the number of poles of the loop transfer function located at the origin where the loop transfer function is given by G(s)H(s). [6] The order of the PLL is the highest degree of the characteristic equation

$$1+G(s)H(s)=0.$$



$$\frac{Y(s)}{X(s)} = \frac{G(S)}{1+G(s)H(s)}$$

Figure 7 A General Block Diagram of a Feedback System

The response to three inputs, a step in phase, a step in frequency, and a ramp in frequency is of interest. It will be seen that the choice of filter affects the phase error. It is worthwhile to look at some possible filter choices. Several filters are described in Figure 8.

332 STEADY STATE AND TRANSIENT PHASE ERRORS

Steady state error is the error after all the transients have died

$$\theta_e(t)_{steady\_state} = \lim_{t\to\infty} \theta_e(t).$$

From Laplace's final value theorem

$$\lim_{t\to\infty} \theta_e(t) = \lim_{s\to 0} s\,\theta_e(s).$$

Remembering that the phase error is given by

$$\theta_e(s) = s\theta_i(s)/[s+K_o K_d]$$

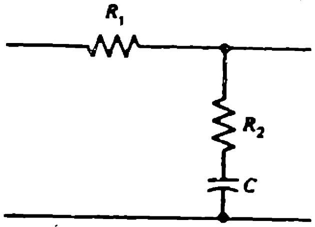
the steady state phase error can be expressed as

$$\lim_{t\to\infty} \theta_e(t) = \lim_{s\to 0} [s^2\theta_i(s)]/[s+K_o K_d\ F(s)].$$

Given the following disturbances at the input:

Figure 8 Filters and Their Transfer Functions

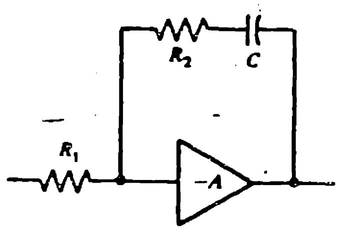
from reference [6]



$$F_1(s) = \frac{sCR_2 + 1}{sC(R_1 + R_2) + 1} = \frac{s\tau_2 + 1}{s\tau_1 + 1}$$

$\tau_1 = (R_1 + R_2)C \quad \tau_2 = R_2C$

(a)



$$F_2(s) = \frac{-A(sCR_2 + 1)}{sCR_2 + 1 + (1 + A)(sCR_1)}$$

For large A

$$F_2(s) \approx -\frac{sCR_2 + 1}{sCR_1} = -\frac{s\tau_2 + 1}{s\tau_1}$$

$\tau_2 = R_2C \quad \tau_1 = R_1C$

(b)

Passive filter	Active filter
$\omega_n = \left(\frac{K_oK_d}{\tau_1}\right)^{1/2}$	$\omega_n = \left(\frac{K_oK_d}{\tau_1}\right)^{1/2}$
$\zeta = \frac{1}{2}\left(\frac{K_oK_d}{\tau_1}\right)^{1/2}\left(\tau_2 + \frac{1}{K_oK_d}\right)$	$\zeta = \frac{\tau_2}{2}\left(\frac{K_oK_d}{\tau_1}\right)^{1/2} = \frac{\tau_2\omega_n}{2}$
$\tau_1 = (R_1 + R_2)C$	$\tau_1 = R_1C$
$\tau_2 = R_2C$	$\tau_2 = R_2C$

$$H_1(s) = \frac{K_oK_d(s\tau_2 + 1)/\tau_1}{s^2 + s(1 + K_oK_d\tau_2)/\tau_1 + K_oK_d/\tau_1}$$

$$H_2(s) = \frac{K_oK_d(s\tau_2 + 1)/\tau_1}{s^2 + s(K_oK_d\tau_2/\tau_1) + K_oK_d/\tau_1}$$

$$H_1(s) = \frac{s(2\zeta\omega_n - \omega_n^2/K_oK_d) + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$H_2(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

A step in phase Cp, where Cp is the magnitude of the phase step in radians

$\theta_i(t) = C_p \qquad t \geq 0 \qquad \theta_i(s) = C_p/s$

A step in frequency Cv, where Cv is the magnitude of the rate of change of phase in rad/sec

$\theta_i(t) = C_v t \qquad t \geq 0 \qquad \theta_i(s) = C_v/s^2$

A ramp in frequency Ca, where Ca is the rate of change of frequency in rad/sec

$\theta_i(t) = C_a t^2 \qquad t \geq 0 \qquad \theta_i(s) = 2C_a/s^3.$

Then for a step input in phase the steady state phase error is

$$\lim_{t \to \infty} \theta_e(t) = \lim_{s \to 0}[s\, C_p]/[s + K_o K_d\, F(s)] = 0$$

if $F(0) > 0$.

There is no steady state error due to a step in phase if F(0) is greater than zero. For a step in frequency (a phase ramp)

$$\lim_{t \to \infty} \theta_e(t) = \lim_{s \to 0} C_v/[s + K_o K_d\, F(s)] =$$

$$C_v/[K_d K_o\, F(0)]$$

where $C_v/[K_d K_o\, F(0)]$ is referred to as the velocity error or static phase error. For a ramp in frequency

$$\lim_{t \to \infty} \theta_e(t) = \lim_{s \to 0}[C_a/s]/[s + K_o K_d F(s)]$$

a second order loop is needed or the phase error blows up. Using the expression for a second order loop

$$\theta_e(s) = [s^2\theta_i(s)]/[s^2 + 2\delta\, w_n\, s + w_n^2]$$

then

$$\lim_{t\to\infty} \theta_e(t) = \lim_{s\to 0} C_a/[s^2 + 2\delta w_n\, s + w_n^2] \qquad = C_a/w_n^2 \text{ rad.}$$

The steady state phase errors for type one, two and three loops are summarized in Table 1. The transient response of first and second order loops is given in Table 2. It can be seen that a type 3 yields better steady state errors than a type 2, and a type 2 better than a type 1. From the transient response (Table 2) it is evident that a second order loop tracks better than a first order loop. When tracking a frequency ramp, however, both the first and second order loop have a term that is linearly proportional to time. As time increases the phase error tends to infinity.

333 ACQUISITION BEHAVIOR FOR PERIODIC PHASE DETECTORS

In an nth order loop there are n state variables (phase step, frequency step, frequency ramp, ect.), each corresponding to an intergrator in the PLL.[4] Acquisition of the input signal can be divided into two parts, phase acquisition and frequency acquisition. Acquisition, unlike tracking, is nonlinear and can not be described using linear analysis. Acquisition behavior depends on the type of phase detector; several periodic phase detectors are outlined in Figure 9. The following discussion examines acquisition behavior for a periodic phase detector; acquisition for a charge pump phase detector will be discussed in a later section.

Before looking at the mathematics of acquisition, it would be helpful to define the following:

TABLE 1
Steady State Phase Errors for Various PLL's

	Type 1	Type 2	Type 3
Input Step in Position	Zero	Zero	Zero
Input Step in Frequency	Constant	Zero	Zero
Input Ramp in Frequency	Continually Increasing	Constant	Zero

Table 2 Transient Response of First and Second Order Loops

Transient Phase Error of Second-Order Loop, $\theta_e(t)$ (in rad) (high loop gain; $K_o K_d >> \omega_n$)

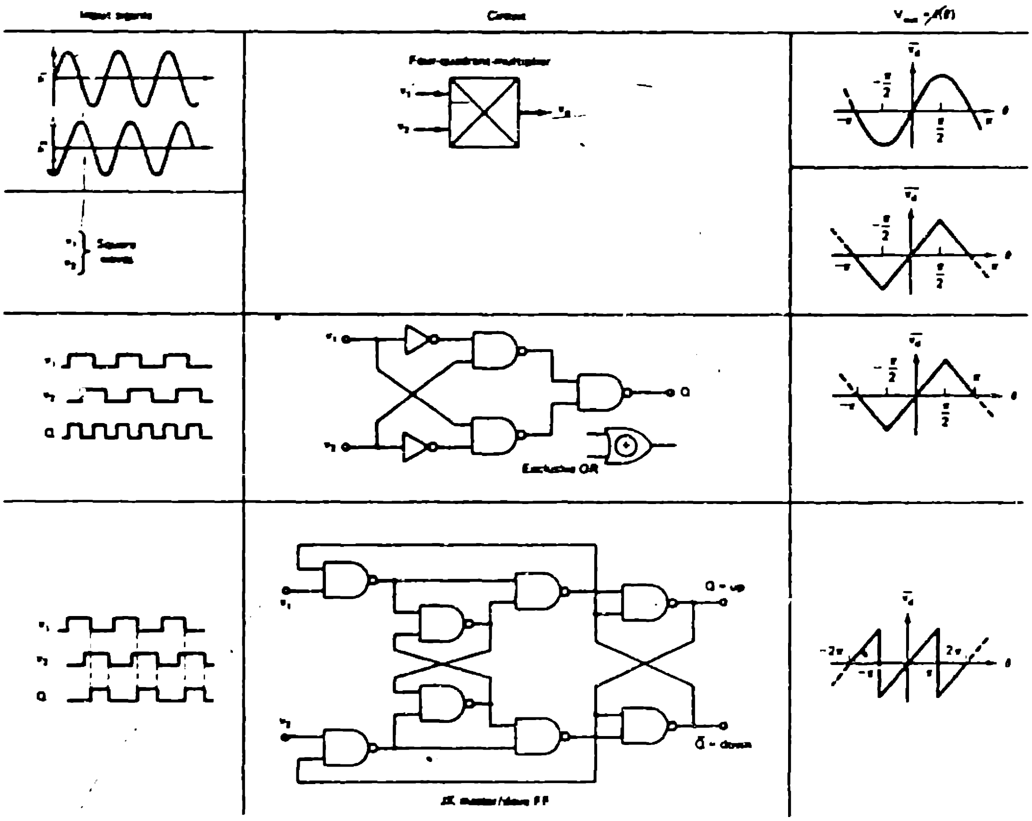
	Phase Step ($\Delta\theta$ rad)	Frequency Step ($\Delta\omega$ rad/sec)	Frequency Ramp ($\Delta\dot{\omega}$ rad/sec^2)
$\zeta < 1$	$\Delta\theta\left(\cos\sqrt{1-\zeta^2}\,\omega_n t - \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\sqrt{1-\zeta^2}\,\omega_n t\right)e^{-\zeta\omega_n t}$	$\frac{\Delta\omega}{\omega_n}\left(\frac{1}{\sqrt{1-\zeta^2}}\sin\sqrt{1-\zeta^2}\,\omega_n t\right)e^{-\zeta\omega_n t}$	$\frac{\Delta\dot{\omega}}{\omega_n^2} - \frac{\Delta\dot{\omega}}{\omega_n^2}\left(\cos\sqrt{1-\zeta^2}\,\omega_n t + \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\sqrt{1-\zeta^2}\,\omega_n t\right)e^{-\zeta\omega_n t}$
$\zeta = 1$	$\Delta\theta(1-\omega_n t)e^{-\omega_n t}$	$\frac{\Delta\omega}{\omega_n}(\omega_n t)e^{-\omega_n t}$	$\frac{\Delta\dot{\omega}}{\omega_n^2} - \frac{\Delta\dot{\omega}}{\omega_n^2}(1+\omega_n t)e^{-\omega_n t}$
$\zeta > 1$	$\Delta\theta\left(\cosh\sqrt{\zeta^2-1}\,\omega_n t - \frac{\zeta}{\sqrt{\zeta^2-1}}\sinh\sqrt{\zeta^2-1}\,\omega_n t\right)e^{-\zeta\omega_n t}$	$\frac{\Delta\omega}{\omega_n}\left(\frac{1}{\sqrt{\zeta^2-1}}\sinh\sqrt{\zeta^2-1}\,\omega_n t\right)e^{-\zeta\omega_n t}$	$\frac{\Delta\dot{\omega}}{\omega_n^2} - \frac{\Delta\dot{\omega}}{\omega_n^2}\left(\cosh\sqrt{\zeta^2-1}\,\omega_n t + \frac{\zeta}{\sqrt{\zeta^2-1}}\sinh\sqrt{\zeta^2-1}\,\omega_n t\right)e^{-\zeta\omega_n t}$

In a first-order loop, the resulting transient phase errors are simple exponentials:

$\Delta\theta e^{-Kt}$	(phase step)
$\frac{\Delta\omega}{K}(1-e^{-Kt})$	(frequency step)
$\frac{\Delta\dot{\omega}}{K^2}(Kt+e^{-Kt}-1)$	(frequency ramp)

from reference [6]

Figure 9 Various Phase Detectors



from reference [7]

LOCK RANGE: the range of frequency overwhich the loop will acquire lock without skipping cycles (phase-lock)

LOCK TIME: the time to acquire phase-lock

PULL-IN RANGE: the range of frequencies overwhich the loop will eventually lock after skipping cycles (frequency lock)

PULL-IN TIME: the time to acquire frequency lock

PULL-OUT RANGE: the maximum frequency at which the VCO can be swept to acquire lock

The PLL must first acquire frequency lock, then once the input frequency equals the output frequency, the loop must acquire phase-lock. Total acquisition time is the pull-in time plus the lock time.

Given a sinusoidal phase detector, phase acquisition of the first order system can be described by the following:

$$\theta_o(t)=w_{center}t+\int_0^t K_o K_d \sin\theta_e\, dt+\theta_o(0).$$

Phase error is given by

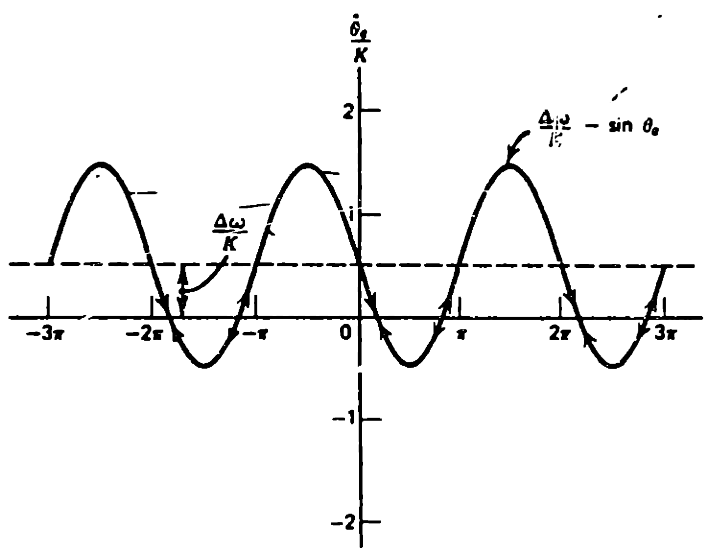
$$\theta_e=w_i t-w_{center}t-\int_0^t K\sin\theta_e\, dt-\theta_o(0)$$

and

$$d\theta_e/dt=(w_i-w_{center})-K\sin\theta_e$$

The loop is locked when the time derivative of the phase error is zero[4] (See Figure 10, where Δw is w_i-w_{center} and $K=K_o K_d$.) Each cycle has a stable null, therefore the loop will lock in one cycle. During frequency acquisition the VCO output moves closer to the input frequency. Pull-in times and pull-in ranges for various filters and phase detectors are listed in

Figure 10 Phase-lock of a First Order Loop



Phase-plane plot of first-order loop ($\Delta\omega/K = 0.5$).

from reference [6]

the Table in Figure 11.

3.4 CHARGE-PUMP PLL

Definite differences exist between PLL's using periodic phase detectors and PLL's using charge-pump phase detectors. Charge-pump phase detectors provide better phase accuracy and better frequency acquisition than periodic phase detectors. They can, however, have considerable output ripple that needs to be filtered before reaching the VCO.

In analyizing the Charge-pump PLL behavior, it is necessary to make certain assumptions. First, linearity requires small phase error, and linear analysis techniques can be used as in the case of the periodic phase detector provided that phase error is small. Second, the charge pump produces an analog signal from the digital output of the phase detector. This is a discrete time system. Continuous time analysis can be used, however, if the loop bandwidth is significantly less than the input frequency.

The charge-pump PLL shown in Figure 12 has three states Up (U), Down (D), and Null (N). When the signal at R leads the signal at V, the edge of R sets U high and the next edge of V sets U low. As long as R leads V, D is low. When V leads R, the edge of V sets D high, and the next edge of R sets D low. As long as V leads R, U is low. When in state U, U is high and D is low; in state D, D is high and U is low; and in state N, both U and D are low. When either in state up or down, current i_p is delivered to the loop filter (when in the null state the output of the phase detector is an open circuit and no current is delivered to the loop filter).

The current $i_p \text{sgn}\theta_e$ is delivered to Z_F for $t_p = |\theta_e|/w_i$ seconds (on time) each cycle of $2\pi/w_i$. The error current is then given by $i_d = i_p\theta_e/2\pi$. The transfer function and error are given by the following:

$$\theta_o(s)/\theta_i(s) = (K_o I_p Z_F(s))/(2\pi s + K_o I_p Z_F(s)) = H(s) \text{ and}$$

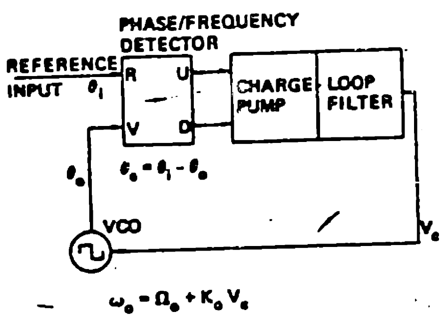
$$\theta_e/\theta_i = 1\text{-}H(s) \qquad \text{for any } Z_F.$$

Figure 11 Aquistition and Lock Behavior for Various Phase Detectors

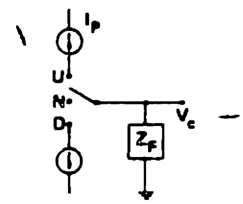
Phase frequency comparator	Exclusive-OR gate: Active filter	Exclusive-OR gate: Passive filter	Edge-triggered JK master/slave flip-flop: Active filter	Edge-triggered JK master/slave flip-flop: Passive filter
Hold-in range	$\Delta\omega_H \longrightarrow \infty$	$\Delta\omega_H = \frac{\pi}{2}\frac{K_oK_d}{N}$	$\Delta\omega_H \longrightarrow \infty$	$\Delta\omega_H = \pi\frac{K_oK_d}{N}$
Capture range				
$\tau_2 \neq 0$	$\Delta\omega_L \approx \pi\zeta\omega_n$		$\Delta\omega_L \approx 2\pi\zeta\omega_n$	
$\tau_2 = 0$	$\Delta\omega_L \approx \frac{\pi}{\sqrt{8}}\omega_n$		$\Delta\omega_L \approx \frac{\pi}{\sqrt{3}}\omega_n$	
Pull-in range	$\Delta\omega_P \approx \frac{\pi}{2}\sqrt{\frac{2\zeta\omega_nK_oK_d}{N}}$	$\Delta\omega_P \approx \frac{\pi}{2}\sqrt{\frac{2\zeta\omega_nK_oK_d}{N} - \omega_n^2}$	$\Delta\omega_P \approx \pi\sqrt{\frac{2\zeta\omega_nK_oK_d}{N}}$	$\Delta\omega_P \approx \pi\sqrt{\frac{2\zeta\omega_nK_oK_d}{N} - \omega_n^2}$
Pull-in time	$T_P \approx \frac{4}{\pi^2}\frac{\Delta\omega_0^2}{\zeta\omega_n^3}$		$T_P \approx \frac{\Delta\omega_0^2}{\pi^2\zeta\omega_n^3}$	
Pullout range				
$\zeta < 1$	$\Delta\omega_{PO} \approx 1.8\omega_n(\zeta + 1)$		$\Delta\omega_{PO} = \pi\omega_n \exp\left(\frac{\zeta}{\sqrt{1-\zeta^2}} \arctan \frac{\sqrt{1-\zeta^2}}{\zeta}\right)$	
$\zeta > 1$			$\Delta\omega_{PO} = \pi\omega_n \exp\left(\frac{\zeta}{\sqrt{\zeta^2-1}} \arctan \frac{\sqrt{\zeta^2-1}}{\zeta}\right)$	

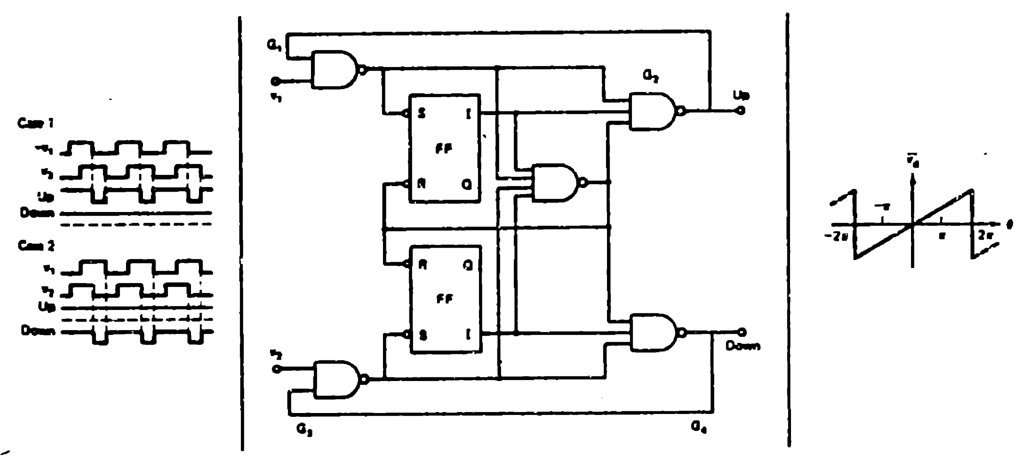
from reference [7]

Figure 12 A Charge-Pump PLL



Phase-lock loop with three-state phase detector and charge pump.





from reference [12]

The static phase error is given by

$(2\pi(w_i - w_c))/(K_o i_p Z_F(0))$ rad.

Leakage currents (due to input bias currents of an opamp filter and switches in the charge pump) cause a leakage phase error

$\theta_b = i_b 2\pi / i_p$ where i_b is the leakage current. Gardner has compared phase errors in loops with periodic phase detectors with those in charge-pump PLL's and found that typical results for the later case are on the order of $2\pi x 10^{-9}$ while those of the former are on the order of $2\pi x 10^{-4}$[7][8]

Assuming that the bandwidth is small enough for continuous time analysis the transient response is comparable to that of loops with periodic phase detectors. Acquisition time is improved. Acquisition time is discussed in reference 14.

3.5 STABILITY AND NOISE

3.5.1 THE CONTINUOUS TIME CASE

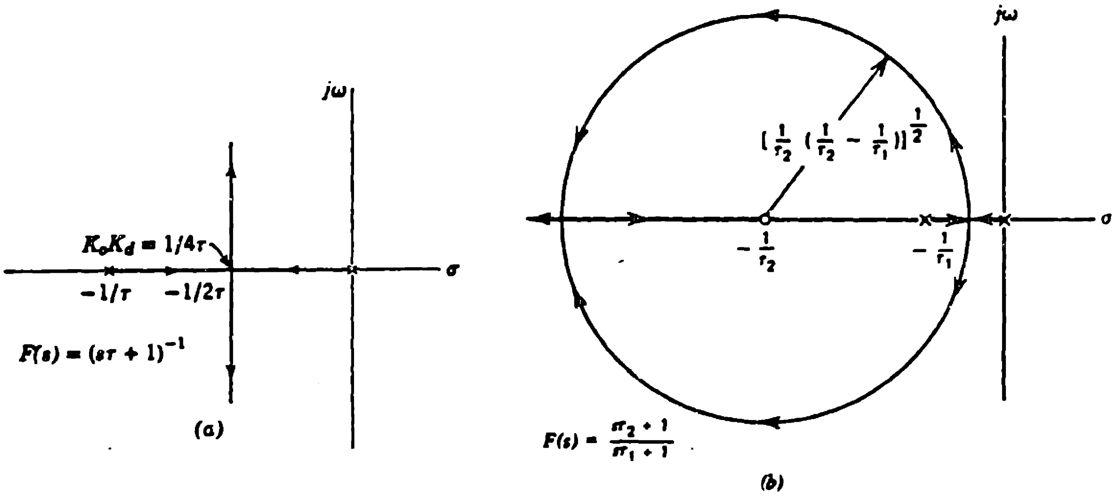
The stability of the loop is affected by the choice of filter as can be seen from the root locus of second and third order loops in Figure 13. In a continuous time system, first and second order loops are unconditionally stable, but the stability of a third order loop is dependent on loop gain. The poles of the third order loop enter the right half plane for low values of gain. Loop stability can also be determined from the phase margin where the phase margin is given by

phase margin = 180 deg + arg (open loop gain)

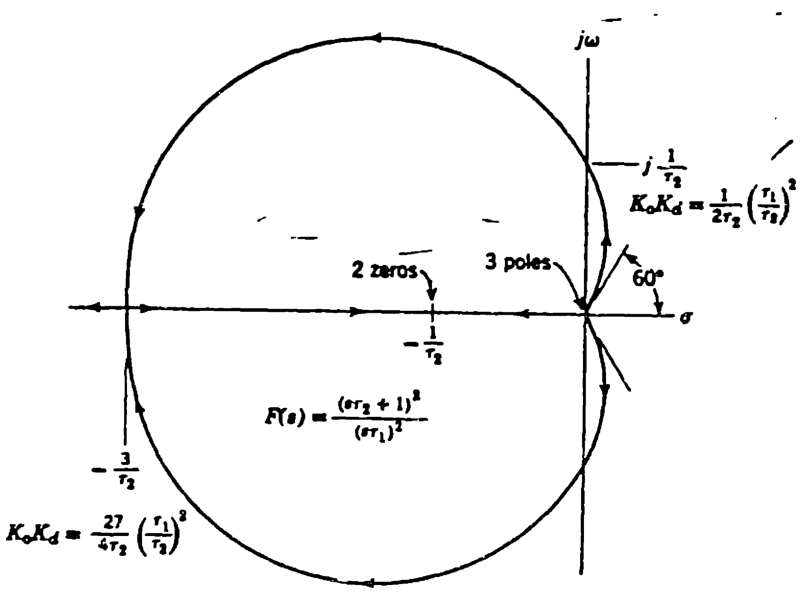
where the open loop gain is

$K_o K_d F(s)/s$.

Figure 13 Root Locus of Second and Third Order Loops



Root-locus plots for second-order loops: (*a*) lag filter; (*b*) lag–lead filter.



Root locus plot of third-order loop.

from reference [6]

Since non-ideal devices are used in any real circuit, additional phase shift can be introduced. Phase margin should be large enough to prevent this additional phase shift from causing instabilities. The larger the value of $K_o K_d$, the larger the phase margin and the more stable the loop.

A PLL often is used to detect a signal imbedded in noise. Like any filter, the narrower the bandwidth, the less noise is passed. Noise bandwidth is given by

$B_L = \int |H(jw)|^2 df$ which, for a second order loop

with an active filter is

$$B_L = K/4\ (1+a^2/K) = w_n/2(\delta+1/4\delta)$$

where δ is the damping ratio, a is a constant and K is the loop gain.

Stability and noise suppression have conflicting requirements. Stability requires a large bandwidth, and good filtering requires a small bandwidth. A summary of design criterion and tradeoffs is discussed in section 3.6.

3.5.2 THE DISCRETE TIME CASE

In a charge-pump PLL, discrete time operation causes stability problems even for small bandwidths. A second order loop is not unconditionally stable. If the gain gets too large, the poles move outside the unit circle implying instability. Gardner discusses stability issues in more detail in reference [12].

3.6 A SUMMARY OF DESIGN CRITERIA

It is desirable to design a stable loop with good noise rejection, fast acquisition, and the ability to acquire lock and to track a signal once locked over a wide range of frequencies. Some of these criteria conflict with others. The loop gain affects the phase error and the hold-in range. A high gain results is small phase error and large hold-in range. (Loop gain is not the only parameter that effects the hold-in range; other parameters, the active filter in particular, are may saturate before the extreme limits of the hold-in range are reached. In high gain loops only a couple of degrees phase error may be tolerated before saturation.) Filter components determine the loop bandwidth. Bandwidth effects noise suppression, pull-in time, hold-in range and stability. A narrow bandwidth will minimize output jitter due to external noise while a large bandwidth will minimize transient error, internal jitter due to VCO noise, and provide the best tracking and acquisition properties. The next section will discuss possible methods for eliminating some of the conflicting requirements.

4. EXISTING SYSTEMS

The Autokon 8400 Laser Scanner uses a variable divide-by-N PLL to track the grating signal described in Chapter 2. This PLL uses an MC4044 charge-pump phase detector, a discrete VCO, and a second order active filter to track the grating signal. The PLL is designed for low phase error, and additional circuitry that detects the absence of the signal and supplies a pseudo signal when the signal is absent, hastens acquisition. Some other loops utilize different bandwidths for tracking and acquisition or sweep the VCO during acquisition. Another PLL uses an open loop frequency prediction, and the loop only needs to correct for differences between the prediction and the actual signal. Mathematical analysis of the third order loop becomes much more involved than that of a second order loop. A second order filter (a third order loop) can track a frequency ramp with small phase error, but it is not unconditionally stable. Any decrease in gain may cause the closed loop poles to enter the right half plane, and the system will become unstable. Since the countdown ratio, N, is included in the gain expression, changing the countdown ratio could also lead to instabilities.

5.0 DESIGN CRITERION FOR THIS PLL

The system under design is a variable divide-by-N PLL that will track the grating signal of the laser scanner. The system should track, with small phase error, a smoothly varying input frequency (due to the sinusoidal scan). Each line consists of a burst of pulses preceded and followed by a blank area. The loop needs to acquire lock at the beginning of every scan line.

The proposed system is a second order loop consisting of a charge-pump phase detector, a first order active filter, an integrated circuit VCO, and a variable counter in the feedback loop. In addition, gap detection and pseudo signal circuitry aid frequency acquisition while resetting the counters on the first pulse zeros the phase of the VCO with respect to the input. Additional frequency prediction circuitry predicts the frequency of one pulse by measuring the frequency of the last pulse and supplies the corresponding voltage to the VCO on an open loop basis. The feedback loop will correct for differences between the input and the prediction. (See Figure 14)

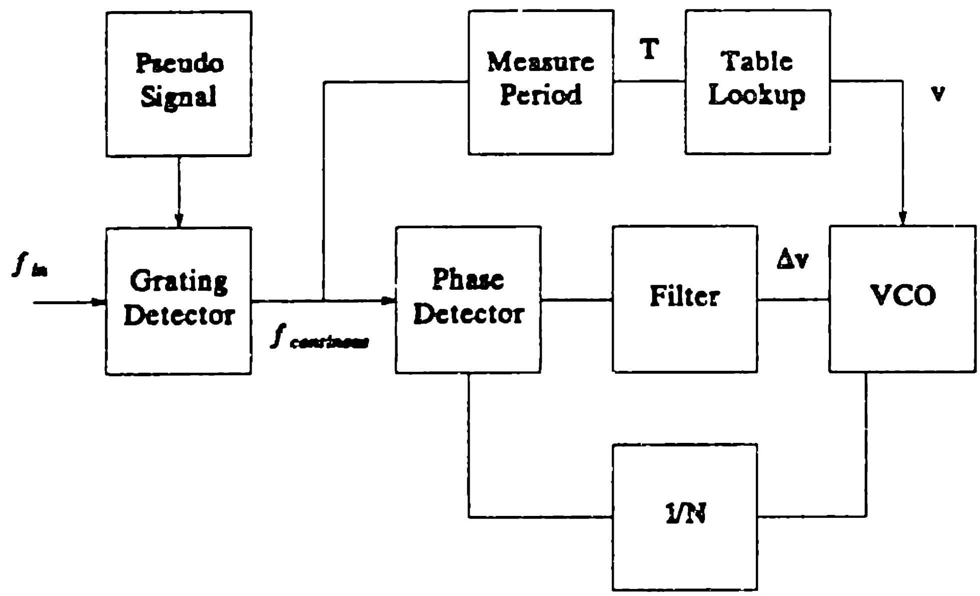


Figure 14 A General Block Diagram of the Proposed circuit

5.1 CHOOSING THE INPUT AND OUTPUT FREQUENCY RANGE

Before discussing the desired tracking and acquisition properties of the PLL, it is necessary to determine the range of input and output frequencies. First, the loop should reduce and enlarge from 20 to 200 percent in 1 percent steps. It has already been noted that for optical reasons there should be multiple pels for each grating bar. If there are 100 pels per grating bar, the output frequency will vary from 20 to 200 times the input frequency. Assuming a 13 inch grating and 216 lines per inch (lpi), grating bars are placed 1/216 inches apart. Assuming a 60 Hz scan and nominally a 65 kHz frequency at the center of the grating, it is necessary to chose the frequency at the edges. Referring to Figure 1, the velocity as a function of time is

$$v(t)=dx/dt=dx/d\theta\ d\theta/dt.$$

The frequency a the edge will be chosen to correspond to a variation of velocity at the center to velocity at the edge of 1 to 1.5 or

$$v(t)_{x=0}/v(t)_{x=6.5}=1/1.5$$

where x=0 inches corresponds to the center of the grating and x=6.5 inches corresponds to the edge of the grating. From Figure 1

$$x=F\tan\theta$$

and

$$\theta(t)=\theta_m \sin(wt)$$

and

$$v(t)=(F/\cos^2\theta)\ 6.28\ \text{rad/deg}\ \theta_m\ w\cos(wt)$$

where θ_m is the angle at which the velocity is zero. Chosing θ_m corresponding to $x_m=8.8$ inches, the ratio of velocity at the center to velocity at the edge is 1.34 (which allowing for a 5 percent variation in frequency is approximately 1.5). (See Appendix A).

It was seen in Figure 2 that the grating bars are placed an equal distance, $\Delta x=1/21.6$ inches, apart but that the time from one bar to the next is longer at the edges than in the center because of the sinusoidal scan. It is possible to calculate the time to move from one pulse to the next, Δt, by subtracting the total time to move from x=0 to one pulse from the total time to move from x=0 to the next pulse where

$$t=1/w\ \arcsin(\arctan(x/F)/\arctan(8.8/16)) \quad \text{and} \qquad \Delta t=|t_1-t_2|$$

The frequency at each grating bar can be approximated by $1/\Delta t$. The time between the two adjacent bars at the edges is

$$|t_{x=.65} - t_{x=.65-1/216}| = 2057 \text{ us}$$

and

$$1/2057 \text{ us} = 49 \text{ kHz}.$$

At the center

$$1/|t_{x=.6} - t_{x=.6-1/216}| = 65 \text{ kHz}$$

as expected. Assuming a 5 percent variation in frequency

$$49 \text{ kHz} \times .05 = 25 \text{ kHz}$$

and

$$65 \text{ kHz} \times .05 = 33 \text{ kHz}.$$

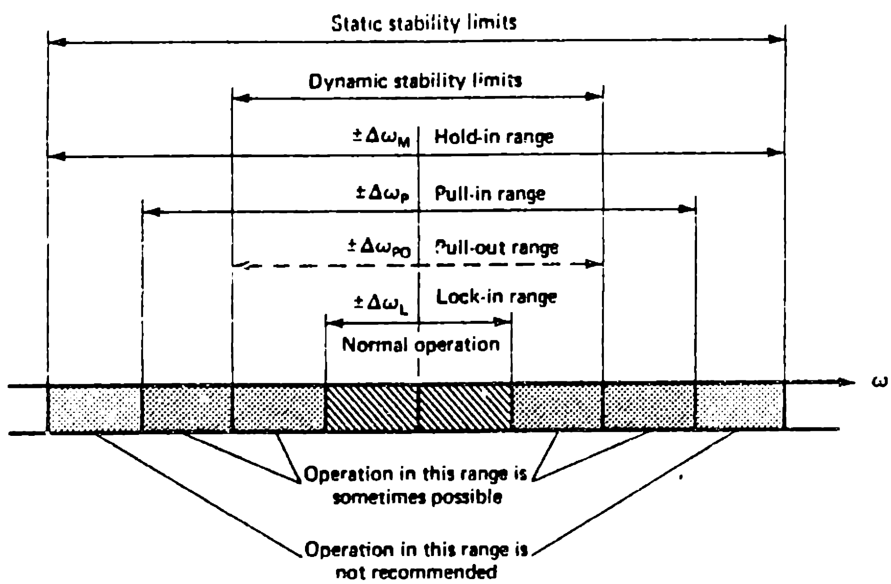
The input frequency can vary from 465 kHz at the edge of the grating to 683 kHz at the center of the grating. This is the minimum range of frequencies that the PLL must track. Since the PLL must acquire lock at the edge of the scan line, it must lock on to frequencies ranging from 465 to 515 kHz.

52 PHASE AND FREQUENCY LOCK

521 THE GAP DETECTOR AND PSEUDO SIGNAL

The input signal must be within a certain range of frequencies, the lock range, centered around the center frequency of the VCO (See Figure 15); if the signal is outside the lock range, additional time is required for the signal to pull-in. Ideally, the input and the output should be locked in frequency and in phase at the beginning edge of the line, but the input still is not phase-locked. Once locked, the loop can be designed to track while the signal is present, but when the signal is absent, the loop loses both phase and frequency lock.

Figure 15 Static and Dynamic Ranges



from reference [7]

The signal occurs in bursts corresponding to each scan line; the loop (without the gap detector and pseudo signal) will lose lock-in the blank areas, and the VCO will operate at its free-running frequency. The gap detector detects the absence of the input signal, and the pseudo signal is applied to the phase detector in place of the signal. The pseudo signal is a fixed frequency signal set to match the frequency of the signal at the edge of the scan line. Even though the grating signal contains blank areas, the PLL sees only a continuous signal and never loses frequency lock (provided the remainder of the loop is properly designed).

522 PHASE LOCK: RESETTING THE COUNTERS

Though the pseudo signal and the grating signal are the same frequency at the edge of the scan line, most probably they will not coincide in phase. The signal will be locked in frequency but will see a phase step at the beginning of each scan line. The Autokon 8400 allows an extra half inch (10 grating bars) on either side of a 12 inch image for the loop to acquire lock. If the divide-by-N counter in the feedback loop of the PLL and the VCO are reset at the edge of the scan line, it should be possible to zero the phase of the VCO with respect to the grating signal. For example, if N is set to 100, the counter puts out one pulse (that goes to the phase detector) for every 100 pulses it counts coming from the VCO. If the VCO signal is synchronized to the input signal, the counter should start counting at the edge of the input signal. Then apply a phase step at the edge of the line; the VCO may not be synchronized with the input, and the counter will not start counting at the edge of the first pulse but sometime before of after it. Resetting the divide-by-N counter to zero when the first pulse, the edge of the scan line, is detected, will force the counter to start counting at the edge of the first pulse. This should synchronize the input and the output on the first pulse. The PLL should be phase-locked after one grating bar, not ten (assuming that the filter parameters are properly chosen).

5.3 PREDICTION

The basic loop consists of a phase detector, filter, VCO and a divide-by-N counter. Ideally, the first order active filter has infinite hold-in range, but in actuality the tracking range is limited by the saturation of the opamp in the active filter. The opamp only tolerates a limited range of input voltages, and its output can not exceed its power supply. The PLL is also limited by how fast it can respond to changes in the input. The charging and discharging filter components limit the speed. Given a large enough frequency step at the input, transients will cause the loop to lose lock and skip several cycles before locking up again.

Tracking can be improved by predicting the frequency at any bar on the grating and applying the corresponding voltage to the VCO on an open loop basis. Given a 60 Hz scanning frequency and a 13 inch grating with 216 lpi, the frequency at any bar on the grating can be calculated. (See Appendix B.) From Appendix B it can be seen that the frequency is varying slowly from pulse to pulse. The scan frequency may vary slightly, and the values calculated in Appendix B may vary accordingly. A more accurate frequency prediction is obtainable if the frequency of each pulse is measured as the loop is scanning. Since it can seen from the calculation in Appendix B that the largest frequency difference between the grating pulses is at the edges, and this is only a difference of several hundred hertz, the measured value of frequency on one pulse can be used to approximate the value on the next pulse. The approximation may deviate from the actual value by several hundred hertz, but the feedback in the conventional PLL should correct for this small deviation from the prediction. The VCO voltage corresponding to the measured grating frequency can be found from a lookup table containing the voltage to frequency characteristic of the VCO. The predicted voltage from the table and the output of the filter (the feedback voltage) can then be summed and applied to the VCO.

The control voltage at the output of the filter and hence the error voltage at the output of the phase detector will be reduced by the addition of the prediction voltage. For example, from Appendix B the tenth grating pulse from the edge of the grating has frequency 52.075 kHz, and the eleventh has frequency 52.361. If the free-running frequency of the VCO were set at 49 kHz, corresponding to the frequency at the edge of the grating, the control voltage at the edge of the grating would be proportional to the difference between the input frequency and the free-running frequency or zero. Without prediction, the control voltage at the eleventh pulse would be proportional to the difference between 52.361 kHz and 49 kHz. With prediction, the control voltage on the eleventh pulse would be proportional to the difference between the frequency on the eleventh pulse and the frequency of the tenth pulse, 286 Hz.

6.0 CIRCUIT DESIGN

6.1 CHOICE OF FILTER PARAMETERS

A filter is necessary to smooth the output ripple coming from the charge-pump phase detector. A first order active filter with transfer function

$$\frac{T_2 s+1}{T_1 s}$$

shown in the PLL in Figure 16 will provide small steady state phase error and good tracking. Ideally, the static limits will provide an infinite hold-in range, though in practice opamp saturation will limit tracking.

The transfer function of the loop is given by

$$\theta_o/\theta_i = K/T_1(T_2 s+1)/(s^2+s(KT_2/T_1)+K/T_1)=$$

$$(2\delta w_n s+w_n^2)/(s^2+2\delta w_n s+w_n^2)$$

where

$$K=K_o K_d/N,$$

$$T_1=K/w_n^2=R_1 C$$

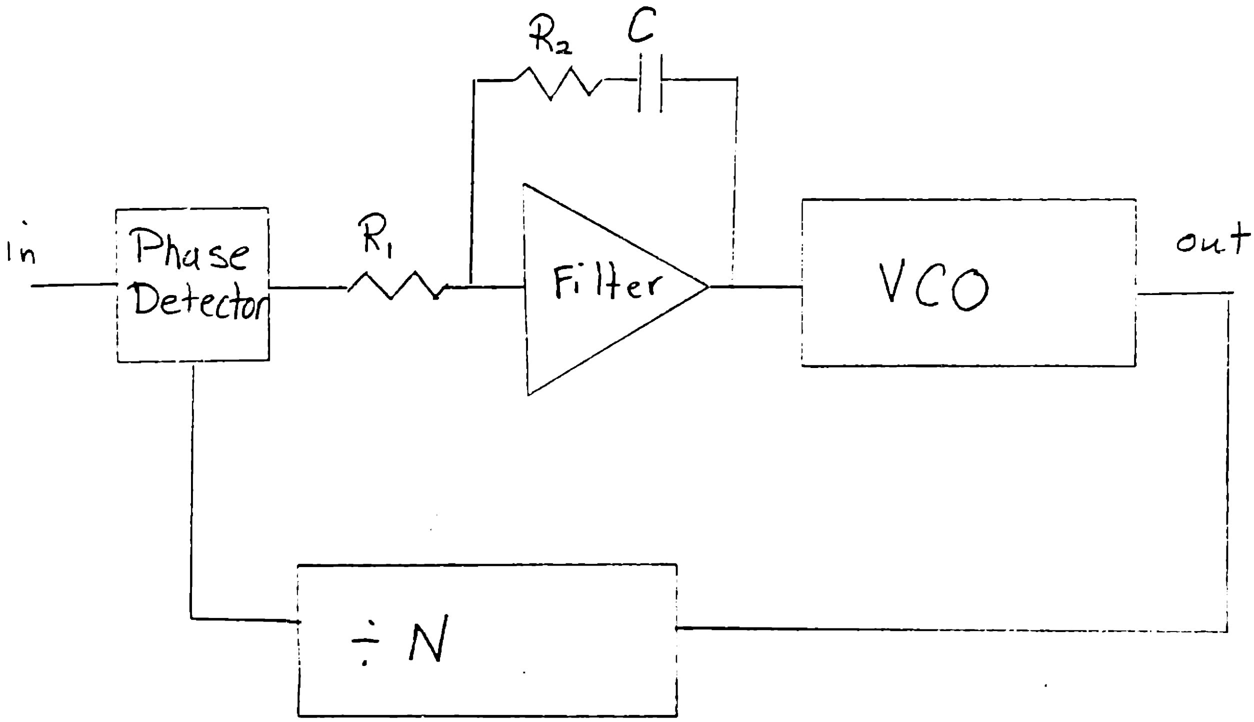
and

$$T_2=2\delta/w_n = R_2 C$$

Chosing w_n and δ for lock within 10 pulses or approximately 200 us, the following parameters where chosen:

$$w_n = 3070 \text{ rad/s}$$

Figure 16 PLL with First Order Active Filter



δ =33

T_1=1.2 ms R_1=12 kohms C=0.1 uF

T_2=2.15 ms R_2=21.5 kohms.

6.2 TRACKING CONSIDERATIONS

Both the static and dynamic behavior of the loop must be considered when evaluating the tracking behavior. The static tracking parameters for a loop with a charge-pump phase detector are simply those of a sinusoidal or X-OR phase detector multiplied by 2π. Static parameters are given by the following:

$$\text{lockrange}=2\pi K_o K_d/N(T_2/T_1)$$

$$=2\pi 2\delta w_n \text{ rad}$$

$$\text{hold-in range}=2\pi K_o K_d/N\ F(0)=\text{infinity}$$

$$\text{rate limit}=2\pi w_n^2 \text{ rad}/s^2$$

A second order loop has zero steady state error due to a step in phase; the loop will not lose lock as a result of a phase step. Though the second order loop should not lose lock permanently when a frequency step is applied (the hold-in range is infinite), it may skip cycles due to the transient phase error before it eventually locks up again. The pull out frequency, the frequency step below which the loop will not skip cycles due to transients, has been determined empirically for second order loops using sinusoidal, X-OR, and JK Master Slave Flip Flops. [4][11]

$$w_{po}=1.8w_n(1+\delta)$$

for the sinusoidal and X-OR phase detector, and

$$w_{po} = \pi w_n \exp(\delta / |(1-\delta^2)|^{1/2} \arctan(|(1-\delta^2)|^{1/2}/\delta))$$

for a JK Master Slave Flip Flop.

It should be emphasized that these are approximate expressions for equations that can not be solved analytically. Further, these are expressions for periodic phase detectors. Charge-pump phase detectors are not periodic, and these expressions are not necessarily valid for PLLs using charge-pump phase detectors. Frequency step response of the PLL under design will be measured and discussed in a later section. It should also be emphasized that the above expressions do not consider saturation which may limit PLL performance even further.

63 IMPLEMENTATION OF PREDICTION CIRCUITRY

The proposed circuitry should predict the frequency at one grating bar by measuring the frequency at the previous grating bar and sending the corresponding voltage to the VCO. This is to be accomplished by measuring the period (period is more convenient to measure than frequency), using the period to look up the VCO voltage in a lookup table (a prom with the voltage to 1/frequency characteristic of the VCO) and sending the digital output of the table to a DAC to convert it to an analog voltage suitable for the VCO input.

The prediction circuitry will consist of three sections, period measurement section, a table lookup section, and a DAC section. First, the type of table that can be constructed depends on the VCO. After chosing a linear VCO and measuring its output frequency at several values of frequency, it is possible to interpolate to find the intermediate values. Chosing a frequency range of 39.6 kHz to 71 kHz, it should be possible to measure the period of the input signal and lookup the corresponding voltage over the entire range of possible input frequencies (46.5 kHz to 68.3 kHz).

Frequency (or period) resolution of the table is determined by the accuracy of the voltage to frequency characteristic measurement and accuracy of the period measurement. Assuming that the period is measured in large enough intervals that it and not the voltage to frequency characteristic is the limiting factor, the following examination of the period measurement will determine the resolution of the table. The fixed frequency oscillator (11.36 MHz) in Figure 17 puts out pulses of period 88ns. The number of oscillator pulses in one grating pulse period can be counted to determine the period of the grating pulse (the number of oscillator pulses times 88ns is the grating pulse period). Since 88ns is simply a scaling factor, the number of oscillator pulses per grating period can be used as the address of the prom. The maximum number of oscillator pulses will occur at the minimum frequency

$$number_{max}\text{pulses}=\frac{1}{f_{maxgrating}88ns} \qquad =1/(39.6 \text{ kHz x } 88\text{ns})=287 \text{ pulses}$$

and the minimum number of pulses will be at the maximum frequency

$$number_{max}\text{pulses}=\frac{1}{f_{mingrating}88ns} \qquad =1/(71 \text{ kHz x } 88\text{ns})=160$$

pulses.

There are 128 possible values of the pulse count between 160 and 287. The frequency and corresponding VCO voltages for the 128 possible values of the pulse count were calculated and stored in the lookup table. (See Appendix C.) The pulse count is the address of the prom; it would be more convenient to address locations 0 through 127 than 160 through 287 (because of space considerations); this can be accomplished by subtracting 160 from each value between 160 and 287. The divide-by-N counter in the feedback loop can take on values between 20 and 200; there are ten voltage to frequency curves corresponding to ten percent steps in N stored in the lookup table. (The PLL has one percent steps from N=20 to 200 even though there are only ten curves stored in the lookup table; it should not be necessary to have a different curve for each N.) Therefore 1280 prom locations are needed to store all the possible voltage values.

The VCO needs an analog control voltage between 0 and about 4 volts. If the lookup table has 12 bits of resolution, the VCO voltages stored in the prom can assume values from 0 to 4095 (2^{n}-1). This is particularly convenient since one least significant bit (LSB) can correspond to 1mV. The DAC can then convert the digital voltages, 0000 to 4095, to analog voltages ranging from 0 to 4.095 volts. Six 1024 by 4 Proms are needed for 12 bits of VCO voltage resolution and 1280 addresses. (Actually 12 bits of resolution are not necessary; this section was designed before the resolution of the frequency measurement was decided upon and was left in the later design for convenience, especially in the digital to analog conversion.) Three proms (prom A) are used for six values of N between 20 and 120, and three (prom B) for the remaining four values of N between 140 and 200. A 1024 by 4 prom has 10 address lines; addresses 0 through 6 (A0-A6) are the pulse count (0 through 127), and addressed 7 through 9 (A7-A9) select the N where the following A7-A9 correspond to the following values of N:

A9 A8 A7	N	PROM
0 0 0	20	A
0 0 1	40	A
0 1 0	60	A
0 1 1	80	A
1 0 0	100	A
1 0 1	120	A
0 0 0	140	B
0 0 1	160	B
0 1 0	180	B

6.4 GENERAL DESCRIPTION OF CIRCUITRY IN THE BLOCK DIAGRAM

Figure 18 shows the block diagram of the gap detection, pseudo signal, phase zeroing, and conventional PLL circuitry. K1 generates the fixed frequency pseudo signal. The gap detector, K2 and L1, detects the presense or absence of the input signal; it outputs the input signal when it is present and the pseudo signal when the input is absent. A2, A4, and L6 zero the phase of the VCO with respect to the input frequency at the beginning of each scan line. N3 sums the feedback correction voltage with the prediction voltage from the DAC; The output of N3 is the control voltage. The phase detector, filter, VCO, and divide-by-N counter (N6, N3, N1, and M1) comprise the conventional loop. (K1 and K2 refer to actual circuit components.)

Figure 17 described the prediction circuitry. A4, B4, and C4 make up the system clock, and B5 synchronizes the input signal to the clock. A1 and A2 count the number of oscillator pulses in one input pulse; C5 detects the end of the input pulse and produces the LOAD/RESET that first, causes B1 and B2 to latch on the number of oscillator pulses in one input pulse and second, resets the counter. E2 and E3 subtract 160 from the number of oscillator pulses per input pulse; J1-J6, C1-C3, E5, and E6 comprise the lookup table; and F4 does the digital to analog conversion.

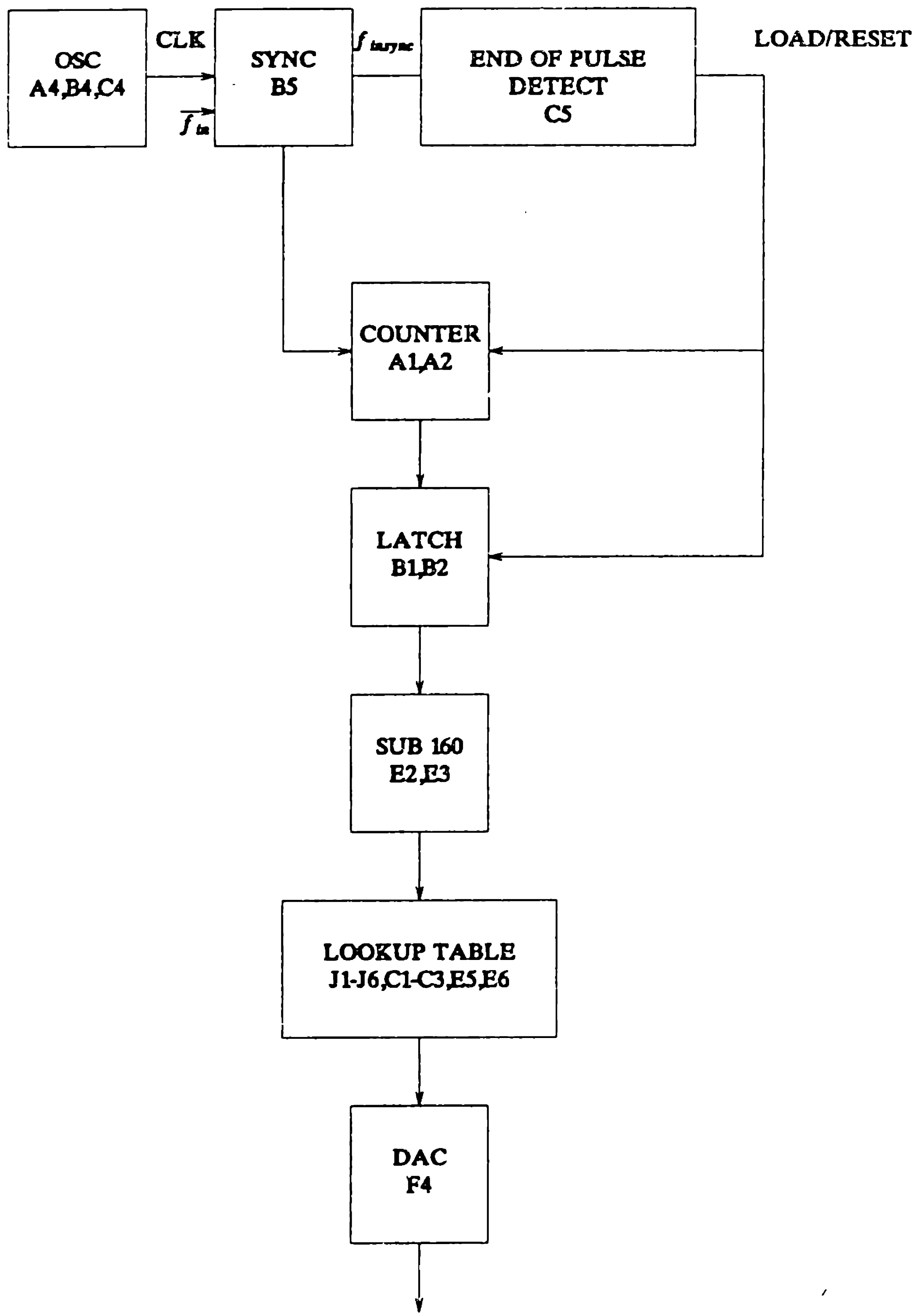


Figure 17 Block Diagram of the Prediction Circuitry

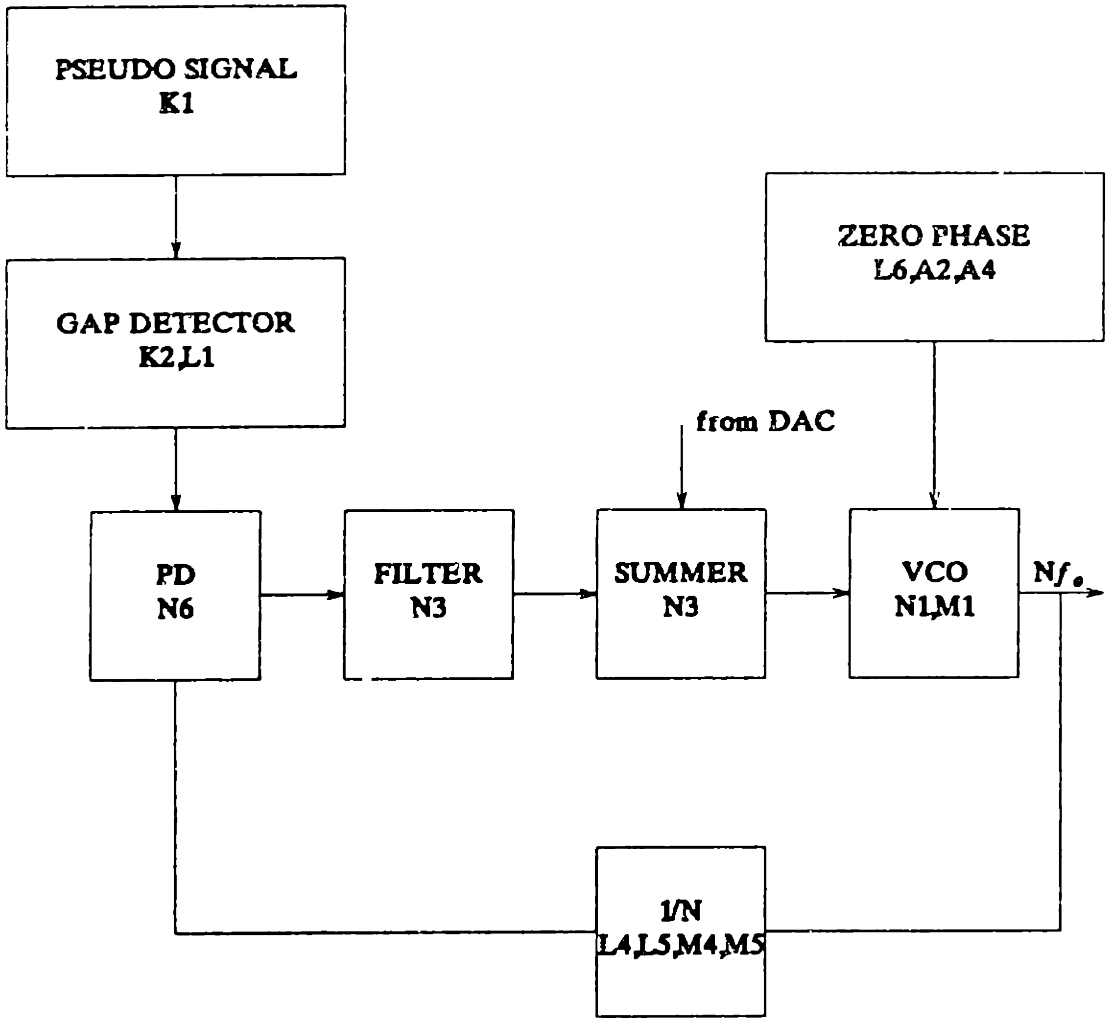


Figure 18 Block Diagram of the Circuitry

7. RESULTS

The PLL was tested over a range of tracking frequencies from 46.5 kHz to 68 kHz. At N=20 and N=40 the loop tracks with very little jitter. At N=60 the loop tracks with some jitter. At N=80 to 200 the loop tracks with a little jitter. Jitter appears to be introduced by the changing prediction voltage. A filter at the output of the DAC should smooth the output. This was tried, but the filter capacitor required finite time to charge and discharge, and this substantially reduced the step response performance. (It is likely that the filter time constant was not properly chosen.) Previously a different DAC with a smoother output was employed. It appeared to produce less jitter, but the final results with this DAC were not recorded since its plus and minus supply leads were exchanged during the testing, and the DAC was damaged. Upon inquiry, it was discovered that the part was obsolete, and it was not possible to replace it and continue testing. This suggests that it may be possible to improve performance by using a better DAC.

7.1 FREQUENCY STEP RESPONSE

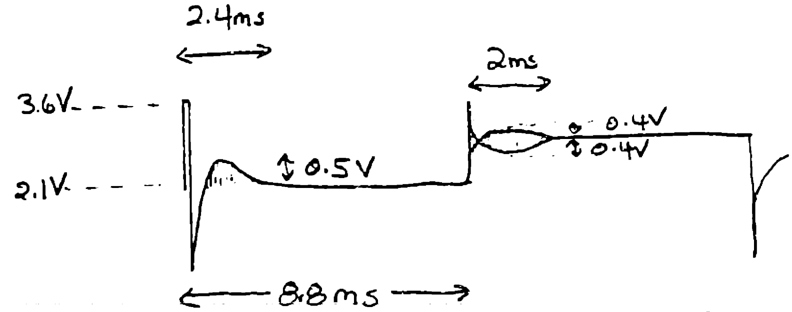
The previous results were obtained by changing the input frequency very slowly in small increments by turning the frequency dial on the function generator. The following results were obtained by applying a step in frequency to the input of the PLL. A 60 Hz square wave from one function generator was used as the voltage controlled input signal of a second function generator. The resulting output of the second function generator was a step in frequency from 50.1 kHz to 66 kHz at 60 Hz for N=20, 60, and 100 through 200 and a step in frequency from 47.6 kHz to 62.5 kHz at 60 Hz for N=40 and 80. Given a linear VCO, a step in frequency at the input should result in a voltage step in the control voltage at the input of the VCO. The control voltage with and without the prediction is shown in figure 19. Without the prediction the PLL time constants are not sufficient; the effects of charging and discharging are seen. The loop may eventually lock after skipping cycles if the step is applied slowly enough (at least less than 60 Hz), but at 60 Hz the loop can not track this frequency step. With the prediction, however, the tracking is much improved as seen in figure 19. The frequency step response in Figure 19 is shown for N=20, N=40, N=80, and N=200. N=60 and N=100 to 180 all exhibited less overshoot and faster settling time than N=200.

7.2 PHASE ACQUISITION RESULTS

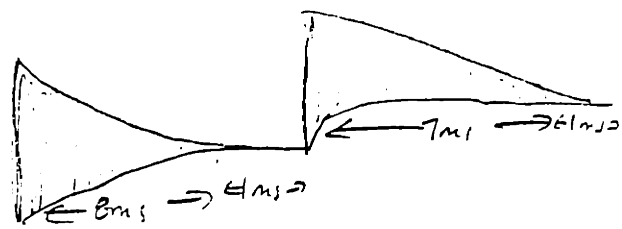
Lock time was measured by observing the duty cycle at the output of the phase-detector. Since in actuality, this is a discrete time system, it is possible to look at each cycle. The duty cycle should decrease as the loop acquires phase-lock. See the phase-lock results in Figure 20; the first ten pulses of phase-detector output are shown for N=100. The duty cycle for the sixth and tenth pulses for the remaining settings of N are listed in the figure. The counters and VCO were reset and phase acquisition was achieved in ten pulses.

Figure 19 (a)

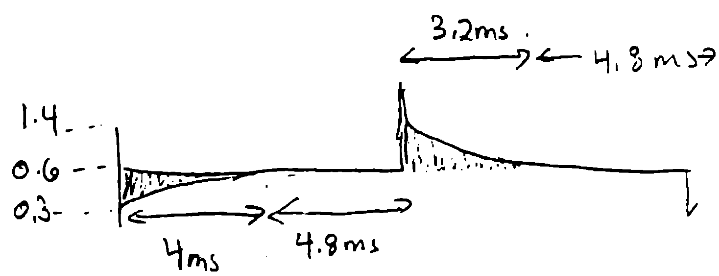
FREQ STEP RESPONSE at 60 Hz from 50.1 kHz to 66 kHz
with prediction, N=200



without prediction



FREQ STEP RESPONSE at 60 Hz from 50.1 kHz to 66 kHz
with prediction, N=20



without prediction

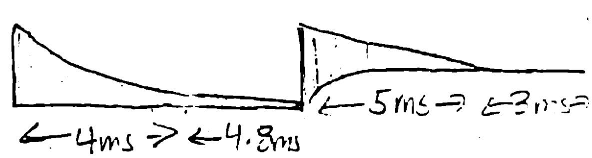
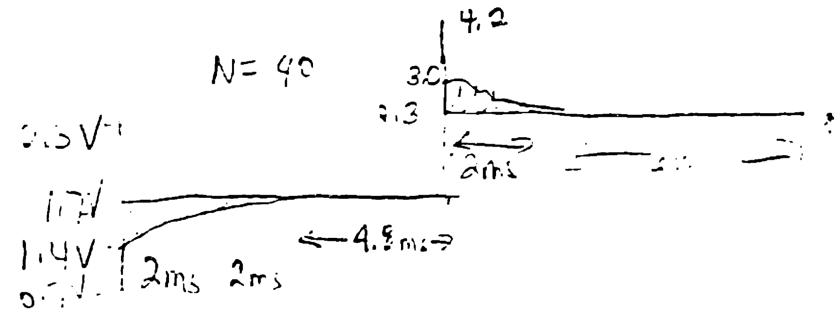
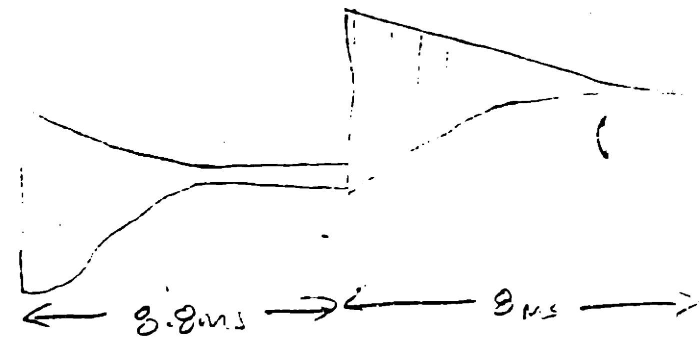


Figure 19 (b)

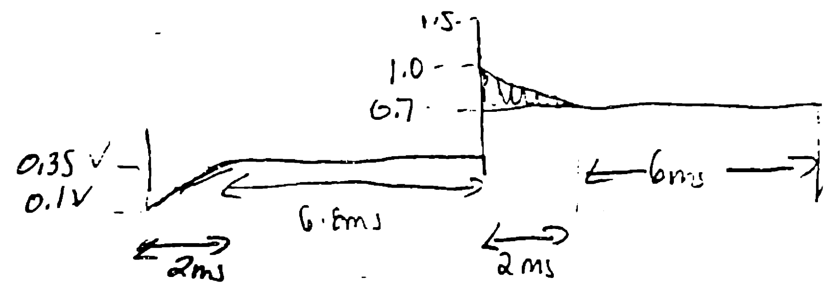
FREQ STEP RESPONSE at 60 Hz from 47.6 kHz to 62.5 kHz
with prediction, N=40



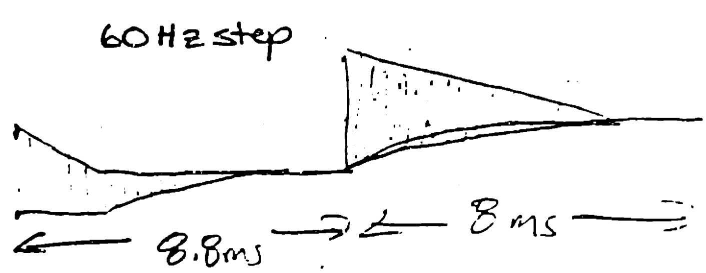
without prediction



FREQ STEP RESPONSE at 60 Hz from 47.6 kHz to 62.5 kHz
with prediction, N=80



without prediction



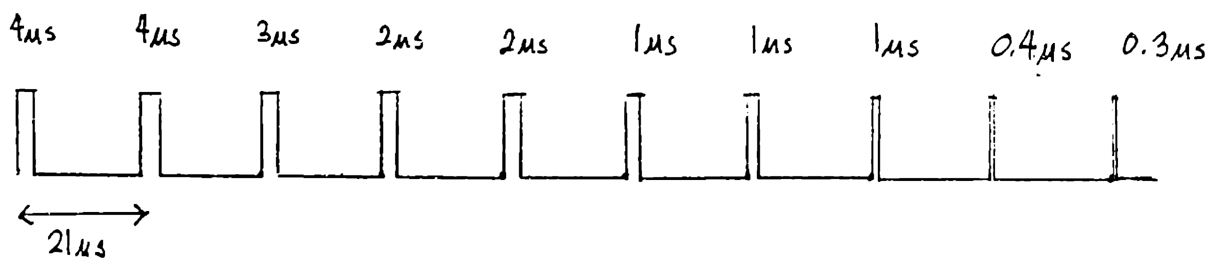


Figure 20 Phase Detector Output at N=100 Freq=47.6 kHz

N	Duty Cycle at 6th pulse (%)	Duty Cycle at 10th Pulse (%)
20	9.5	7.1
40	9.5	7.5
60	9.5	4.8
80	9.5	7.5
100	4.8	2.9 (typical)
120	9.5	7.1
140	9.5	7.1
160	9.5	7.1
180	9.5	7.1
200	9.5	7.1 (worst case)

8. CONCLUSIONS

The PLL tracks over the desired range of frequencies but not without jitter. The frequency step response of the loop is improved with the addition of the prediction circuitry. Phase-lock is sufficient but has room for improvement; phase acquisition is not as rapid as originally planned.

Jitter can cause serious problems in graphic arts applications. Jitter due to the charge-pump phase-detector was not taken into consideration in the design. The VCO tracks voltage steps resulting in "phase excursions," θ_e, during each pump pulse where

$$\theta_e = 2\pi K |\theta_e| / w_i$$

where the phase excursion vanishes for $\theta_e = 0$ since pump pulses vanish for zero phase error. [12] It should be possible to reduce the jitter by lowering the gain since from the above expression it can be seen tha jitter is proportional to gain K. Lowering the gain might also improve the stability margin. Jitter might also be reduced (as previously mentioned) by smoothing the output of the DAC. DAC output might also be smoothed by using linear interpolation to change the output voltage linearly instead of in steps.

A discrete VCO might improve loop performance. The 74LS626 was chosen for linearity, but it should be possible to design a sufficiently linear discrete VCO. It is possible that a discrete VCO would have less internal noise than an integrated circuit VCO.

The predicted value of the next pulse might be improved by predicting the "exact value" (with some error of course) – exact value meaning trying to predict the actual value of the pulse, not approximating it by the value of the previous pulse. A better prediction might also be achieved by measuring the grating frequency more accurately.

Faster lock might more easily be achieved by using a discrete VCO. The original design mistakenly did not take phase-lock, only tracking, into consideration when chosing filter parameters. Consequently, the first filter needed forty pulses to lock even when using the fast lock scheme. Changing the filter parameters to the present ones, lock was achieved in ten pulses as in the Autokon. A better prediction scheme might also contribute to faster lock.

APPENDIX A

The following is a calculation of the ratio of the velocity at the center of the grating to the edge of the grating, assuming maximum deflection θ_m at x_m = 8.8 inches. (See Figure 1.)

$$v(t)=F/\cos^2\theta \;\; 6.28 \text{ rad/deg } \theta_m w\cos(wt)$$

where

$$\theta=\arctan(x/F)$$

$$wt=\arcsin(\theta/\theta_m)=\arcsin(\arctan(x/F)/\arctan(x_m/F))$$

then in terms of position x

$$v(t)_{x=0}/v(t)_{x=6.5} =$$

$$\frac{\cos(\arcsin(0))}{\cos^2(0)} \frac{\cos^2(\arctan(6.5/16))}{\cos(\arcsin(a))} = 1.34 \text{ where}$$

$$a = \arctan(6.5/16)/\arctan(8.8/16)$$

APPENDIX B GRATING FREQUENCY AT EACH GRATING BAR

The following values were calculated using the method in section 5.1, where the frequency at any grating bar is approximated by the inverse of the time to move from one grating bar to the next. The grating bars are numbered sequentially starting at zero at the center and ending at 139 at the edges. The calculation is given for one half of the grating because of symmetry around the center of the grating.

grating bar	1/△t (Hz)	grating bar	1/△t (Hz)	grating bar	1/△t (Hz)
1	65481	22	65206	44	64372
2	65480	23	65181	45	64319
3	65477	24	65155	46	64265
4	65474	25	65127	47	64209
5	65470	26	65099	48	64153
6	65465	27	65069	49	64094
7	65458	28	65038	50	64034
8	65451	29	65005	51	63973
9	65442	30	64972	52	63910
10	65432	31	64937	53	63846
10	65422	32	64901	54	63780
11	65410	33	64864	55	63713
12	65397	34	64826	56	63644
13	65383	35	64786	57	63574
14	65368	36	64745	58	63501
15	65351	37	64703	59	63428
17	65334	38	64660	60	63352
18	65315	39	64615	61	63275
19	65296	40	64569	62	63197
20	65275	41	64522	63	63117
21	65253	42	64473	64	63035
21	65230	43	64423		

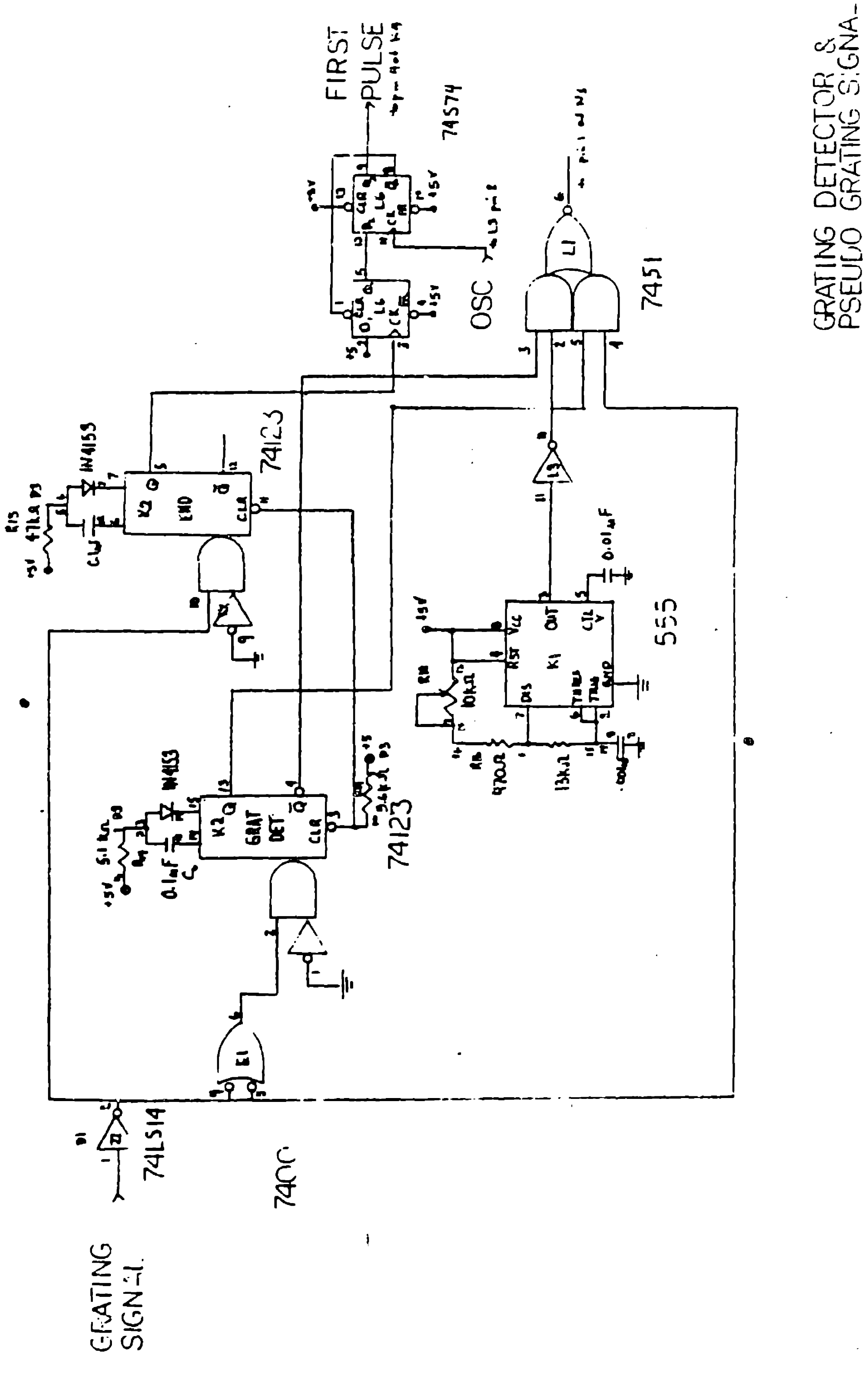
grating bar	1/△t (Hz)
66	62951
67	62866
68	62779
69	62689
70	62599
71	62505
72	62411
73	62314
74	62216
75	62115
76	62013
77	61908
78	61802
79	61693
80	61582
81	61470
82	61354
83	61238
84	61117
85	60996
86	60872
87	60745
88	60617
89	60486
90	60351
91	60216
92	60077
93	59934
94	59791
94	59644
95	59494
96	59342
97	59186
98	59029
99	58868

grating bar	1/△t (Hz)
100	58704
101	58537
102	58367
103	58193
104	58017
105	57837
106	57654
107	57468
108	57278
109	57085
110	56888
111	56687
112	56483
113	56275
114	56063
115	55848
116	55628
117	55403
118	55175
119	54943
120	54706
121	54464
122	54219
123	53968
124	53713
125	53452
126	53187
127	52917
128	52641
129	52361
130	52075
131	51782
132	51485
133	51181
134	50871
135	50555
136	50234
137	49904
138	49569
139	49227

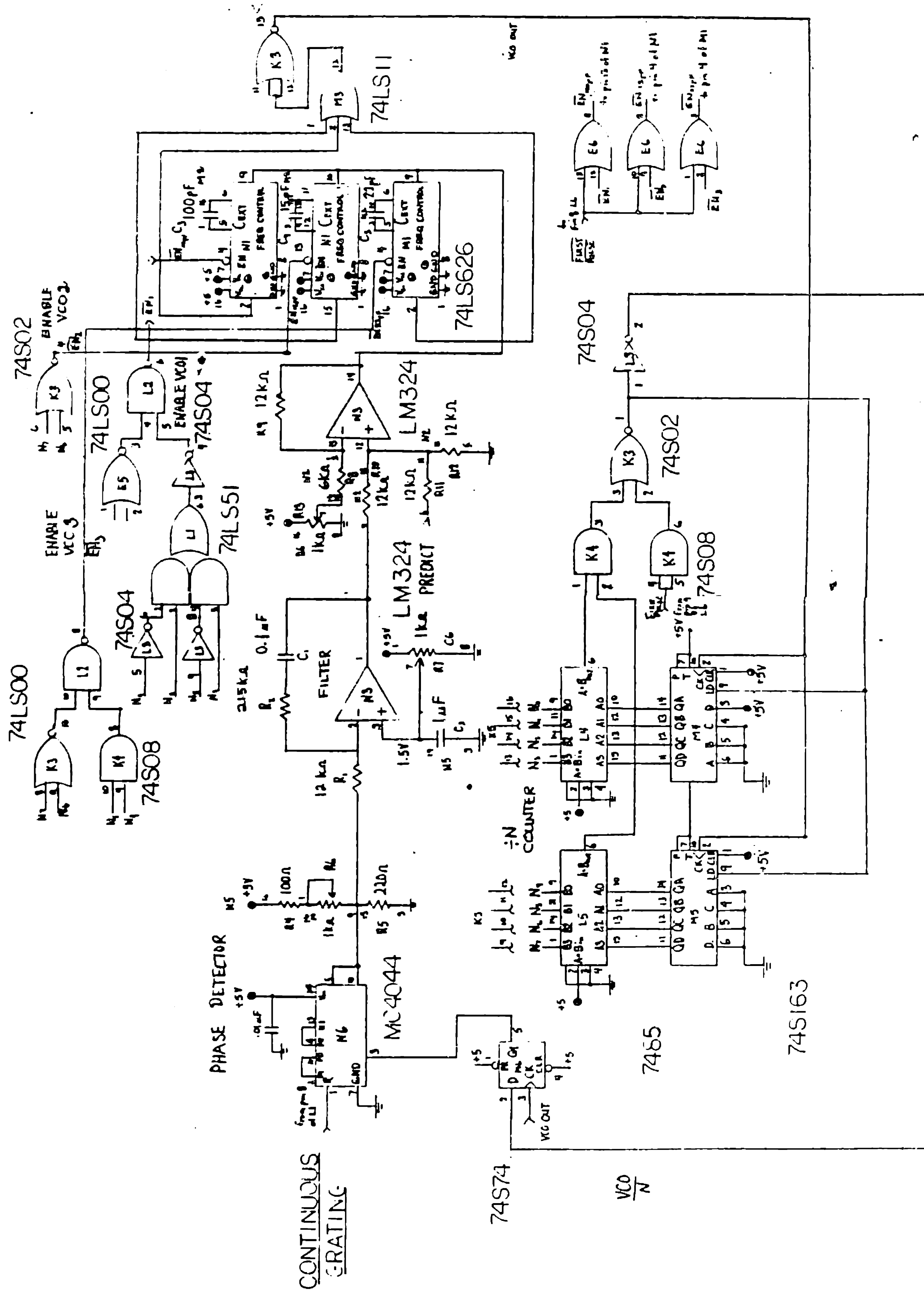
APPENDIX C TABLE OF VCO VOLTAGES STORED IN THE LOOKUP TABLE

number of osc. pulses	freq kHz	VCO Voltage in Volts at N= 20	40	60	80	100	120	140	160	180	200
160	71.0	1.198	2.692	2.377	0.912	1.326	1.741	2.155	2.570	2.985	3.399
161	70.6	1.189	2.673	2.359	0.901	1.313	1.725	2.137	2.550	2.962	3.374
162	70.1	1.179	2.655	2.340	0.891	1.301	1.710	2.120	2.529	2.939	3.348
163	69.7	1.170	2.637	2.322	0.881	1.288	1.695	2.102	2.509	2.916	3.323
164	69.3	1.161	2.619	2.304	0.871	1.276	1.680	2.085	2.489	2.894	3.298
165	68.8	1.153	2.601	2.286	0.861	1.263	1.665	2.068	2.470	2.872	3.274
166	68.4	1.144	2.584	2.268	0.852	1.251	1.651	2.051	2.450	2.850	3.250
167	68.0	1.135	2.566	2.251	0.842	1.239	1.637	2.034	2.431	2.828	3.226
168	67.6	1.127	2.549	2.234	0.833	1.227	1.622	2.017	2.412	2.807	3.202
169	67.2	1.118	2.533	2.216	0.823	1.216	1.608	2.001	2.393	2.786	3.179
170	66.8	1.110	2.516	2.200	0.814	1.204	1.594	1.985	2.375	2.765	3.155
171	66.4	1.102	2.499	2.183	0.805	1.193	1.581	1.969	2.357	2.745	3.133
172	66.0	1.094	2.483	2.167	0.796	1.182	1.567	1.953	2.339	2.724	3.110
173	65.7	1.086	2.467	2.150	0.787	1.170	1.554	1.937	2.321	2.704	3.088
174	65.3	1.078	2.451	2.134	0.778	1.159	1.541	1.922	2.303	2.685	3.066
175	64.9	1.070	2.436	2.118	0.769	1.148	1.528	1.907	2.286	2.665	3.044
176	64.5	1.062	2.420	2.103	0.761	1.138	1.515	1.892	2.269	2.646	3.022
177	64.2	1.054	2.405	2.087	0.752	1.127	1.502	1.877	2.252	2.626	3.001
178	63.8	1.047	2.390	2.072	0.744	1.117	1.489	1.862	2.235	2.607	2.980
179	63.5	1.039	2.375	2.057	0.736	1.106	1.477	1.847	2.218	2.589	2.959
180	63.1	1.032	2.360	2.042	0.727	1.096	1.464	1.833	2.202	2.570	2.939
181	62.8	1.025	2.345	2.027	0.719	1.086	1.452	1.819	2.185	2.552	2.918
182	62.4	1.017	2.331	2.012	0.711	1.076	1.440	1.805	2.169	2.534	2.898
183	62.1	1.010	2.316	1.998	0.703	1.066	1.428	1.791	2.153	2.516	2.878
184	61.7	1.003	2.302	1.983	0.695	1.056	1.416	1.777	2.137	2.498	2.859
185	61.4	0.996	2.288	1.969	0.687	1.046	1.405	1.763	2.122	2.480	2.839
186	61.1	0.989	2.274	1.955	0.680	1.036	1.393	1.750	2.106	2.463	2.820
187	60.7	0.982	2.260	1.941	0.672	1.027	1.382	1.736	2.091	2.446	2.801
188	60.4	0.975	2.247	1.928	0.665	1.017	1.370	1.723	2.076	2.429	2.782
189	60.1	0.969	2.233	1.914	0.657	1.008	1.359	1.710	2.061	2.412	2.763
190	59.8	0.962	2.220	1.900	0.650	0.999	1.348	1.697	2.046	2.396	2.745
191	59.5	0.955	2.207	1.887	0.642	0.990	1.337	1.684	2.032	2.379	2.726
192	59.2	0.949	2.194	1.874	0.635	0.981	1.326	1.672	2.017	2.363	2.708
193	58.9	0.942	2.181	1.861	0.628	0.972	1.315	1.659	2.003	2.347	2.690
194	58.6	0.936	2.168	1.848	0.621	0.963	1.305	1.647	1.989	2.331	2.673
195	58.3	0.930	2.155	1.835	0.614	0.954	1.294	1.635	1.975	2.315	2.655
196	58.0	0.923	2.143	1.823	0.607	0.945	1.284	1.622	1.961	2.299	2.638
197	57.7	0.917	2.131	1.810	0.600	0.937	1.274	1.610	1.947	2.284	2.621
198	57.4	0.911	2.118	1.798	0.593	0.928	1.263	1.598	1.934	2.269	2.604
199	57.1	0.905	2.106	1.785	0.587	0.920	1.253	1.587	1.920	2.253	2.587
200	56.8	0.899	2.094	1.773	0.580	0.912	1.243	1.575	1.907	2.238	2.570
201	56.5	0.893	2.082	1.761	0.573	0.903	1.233	1.563	1.893	2.224	2.554
202	56.2	0.887	2.070	1.749	0.567	0.895	1.224	1.552	1.880	2.209	2.537
203	56.0	0.881	2.059	1.738	0.560	0.887	1.214	1.541	1.867	2.194	2.521
204	55.7	0.876	2.047	1.726	0.554	0.879	1.204	1.529	1.855	2.180	2.505
205	55.4	0.870	2.036	1.714	0.547	0.871	1.195	1.518	1.842	2.166	2.489
206	55.1	0.864	2.025	1.703	0.541	0.863	1.185	1.507	1.829	2.151	2.474
207	54.9	0.859	2.013	1.692	0.535	0.855	1.176	1.496	1.817	2.137	2.458
208	54.6	0.853	2.002	1.680	0.529	0.848	1.167	1.486	1.805	2.124	2.443
209	54.4	0.848	1.991	1.669	0.523	0.840	1.158	1.475	1.792	2.110	2.427
210	54.1	0.842	1.980	1.658	0.517	0.833	1.148	1.464	1.780	2.096	2.412
211	53.8	0.837	1.970	1.647	0.511	0.825	1.140	1.454	1.768	2.083	2.397
212	53.6	0.831	1.959	1.637	0.505	0.818	1.131	1.444	1.756	2.069	2.382
213	53.3	0.826	1.948	1.626	0.499	0.810	1.122	1.433	1.745	2.056	2.368
214	53.1	0.821	1.938	1.615	0.493	0.803	1.113	1.423	1.733	2.043	2.353
215	52.8	0.816	1.927	1.605	0.487	0.796	1.104	1.413	1.722	2.030	2.339
216	52.6	0.811	1.917	1.594	0.482	0.789	1.096	1.403	1.710	2.017	2.324
217	52.4	0.805	1.907	1.584	0.476	0.782	1.087	1.393	1.699	2.005	2.310
218	52.1	0.800	1.897	1.574	0.470	0.775	1.079	1.383	1.688	1.992	2.296
219	51.9	0.795	1.887	1.564	0.465	0.768	1.071	1.374	1.676	1.979	2.282
220	51.6	0.790	1.877	1.554	0.459	0.761	1.062	1.364	1.665	1.967	2.269
221	51.4	0.786	1.867	1.544	0.454	0.754	1.054	1.354	1.655	1.955	2.255

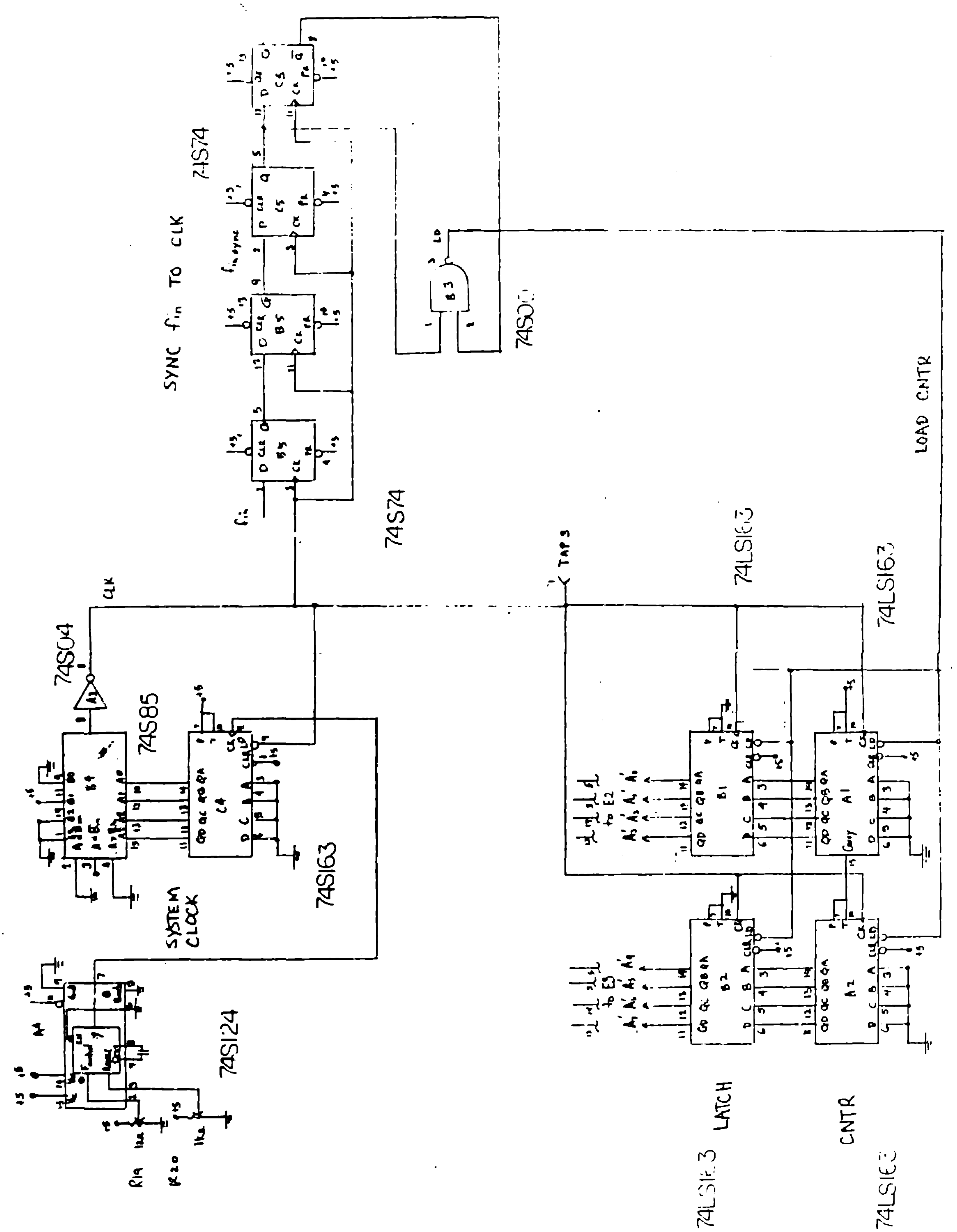
number of osc. pulses	freq kHz	VCO Voltage at N= 20	40	60	80	100	120	140	160	180	200
221	51.4	0.786	1.867	1.544	0.454	0.754	1.054	1.354	1.655	1.955	2.255
222	51.2	0.781	1.857	1.534	0.448	0.747	1.046	1.345	1.644	1.943	2.241
223	50.9	0.776	1.848	1.524	0.443	0.740	1.038	1.335	1.633	1.930	2.228
224	50.7	0.771	1.838	1.514	0.438	0.734	1.030	1.326	1.622	1.919	2.215
225	50.5	0.766	1.829	1.505	0.432	0.727	1.022	1.317	1.612	1.907	2.202
226	50.3	0.762	1.819	1.495	0.427	0.721	1.014	1.308	1.601	1.895	2.189
227	50.0	0.757	1.810	1.486	0.422	0.714	1.007	1.299	1.591	1.883	2.176
228	49.8	0.752	1.801	1.477	0.417	0.708	0.999	1.290	1.581	1.872	2.163
229	49.6	0.748	1.791	1.467	0.412	0.702	0.991	1.281	1.571	1.860	2.150
230	49.4	0.743	1.782	1.458	0.407	0.695	0.984	1.272	1.561	1.849	2.137
231	49.2	0.739	1.773	1.449	0.402	0.689	0.976	1.263	1.551	1.838	2.125
232	49.0	0.734	1.764	1.440	0.397	0.683	0.969	1.255	1.541	1.827	2.113
233	48.8	0.730	1.756	1.431	0.392	0.677	0.961	1.246	1.531	1.816	2.100
234	48.5	0.725	1.747	1.422	0.387	0.671	0.954	1.238	1.521	1.805	2.088
235	48.3	0.721	1.738	1.413	0.382	0.665	0.947	1.229	1.511	1.794	2.076
236	48.1	0.717	1.730	1.405	0.377	0.659	0.940	1.221	1.502	1.783	2.064
237	47.9	0.712	1.721	1.396	0.373	0.653	0.933	1.212	1.492	1.772	2.052
238	47.7	0.708	1.713	1.387	0.368	0.647	0.925	1.204	1.483	1.762	2.040
239	47.5	0.704	1.704	1.379	0.363	0.641	0.918	1.196	1.474	1.751	2.029
240	47.3	0.700	1.696	1.371	0.359	0.635	0.912	1.188	1.464	1.741	2.017
241	47.1	0.696	1.688	1.362	0.354	0.629	0.905	1.180	1.455	1.731	2.006
242	46.9	0.692	1.679	1.354	0.350	0.624	0.898	1.172	1.446	1.720	1.994
243	46.7	0.688	1.671	1.346	0.345	0.618	0.891	1.164	1.437	1.710	1.983
244	46.6	0.684	1.663	1.338	0.341	0.612	0.884	1.156	1.428	1.700	1.972
245	46.4	0.680	1.655	1.329	0.336	0.607	0.878	1.148	1.419	1.690	1.961
246	46.2	0.676	1.647	1.321	0.332	0.601	0.871	1.141	1.410	1.680	1.950
247	46.0	0.672	1.639	1.313	0.327	0.596	0.865	1.133	1.402	1.670	1.939
248	45.8	0.668	1.632	1.306	0.323	0.591	0.858	1.126	1.393	1.661	1.928
249	45.6	0.664	1.624	1.298	0.319	0.585	0.852	1.118	1.384	1.651	1.917
250	45.4	0.660	1.616	1.290	0.314	0.580	0.845	1.111	1.376	1.641	1.907
251	45.3	0.656	1.608	1.282	0.310	0.575	0.839	1.103	1.367	1.632	1.896
252	45.1	0.652	1.601	1.275	0.306	0.569	0.833	1.096	1.359	1.622	1.886
253	44.9	0.649	1.593	1.267	0.302	0.564	0.826	1.089	1.351	1.613	1.875
254	44.7	0.645	1.586	1.260	0.298	0.559	0.820	1.081	1.343	1.604	1.865
255	44.5	0.641	1.579	1.252	0.294	0.554	0.814	1.074	1.334	1.594	1.855
256	44.4	0.638	1.571	1.245	0.290	0.549	0.808	1.067	1.326	1.585	1.844
257	44.2	0.634	1.564	1.237	0.286	0.544	0.802	1.060	1.318	1.576	1.834
258	44.0	0.630	1.557	1.230	0.282	0.539	0.796	1.053	1.310	1.567	1.824
259	43.9	0.627	1.550	1.223	0.278	0.534	0.790	1.046	1.302	1.558	1.814
260	43.7	0.623	1.543	1.216	0.274	0.529	0.784	1.039	1.294	1.549	1.805
261	43.5	0.620	1.536	1.209	0.270	0.524	0.778	1.032	1.286	1.541	1.795
262	43.4	0.616	1.529	1.201	0.266	0.519	0.772	1.026	1.279	1.532	1.785
263	43.2	0.613	1.522	1.194	0.262	0.514	0.767	1.019	1.271	1.523	1.776
264	43.0	0.609	1.515	1.188	0.258	0.509	0.761	1.012	1.263	1.515	1.766
265	42.9	0.606	1.508	1.181	0.254	0.505	0.755	1.005	1.256	1.506	1.756
266	42.7	0.603	1.501	1.174	0.251	0.500	0.749	0.999	1.248	1.498	1.747
267	42.5	0.599	1.494	1.167	0.247	0.495	0.744	0.992	1.241	1.489	1.738
268	42.4	0.596	1.488	1.160	0.243	0.491	0.738	0.986	1.233	1.481	1.728
269	42.2	0.593	1.481	1.153	0.240	0.486	0.733	0.979	1.226	1.473	1.719
270	42.1	0.589	1.474	1.147	0.236	0.482	0.727	0.973	1.219	1.464	1.710
271	41.9	0.586	1.468	1.140	0.232	0.477	0.722	0.967	1.211	1.456	1.701
272	41.8	0.583	1.461	1.134	0.229	0.473	0.716	0.960	1.204	1.448	1.692
273	41.6	0.580	1.455	1.127	0.225	0.468	0.711	0.954	1.197	1.440	1.683
274	41.5	0.576	1.449	1.121	0.222	0.464	0.706	0.948	1.190	1.432	1.674
275	41.3	0.573	1.442	1.114	0.218	0.459	0.700	0.942	1.183	1.424	1.665
276	41.2	0.570	1.436	1.108	0.214	0.455	0.695	0.936	1.176	1.416	1.657
277	41.0	0.567	1.430	1.102	0.211	0.451	0.690	0.930	1.169	1.409	1.648
278	40.9	0.564	1.424	1.095	0.208	0.446	0.685	0.923	1.162	1.401	1.639
279	40.7	0.561	1.417	1.089	0.204	0.442	0.680	0.918	1.155	1.393	1.631
280	40.6	0.558	1.411	1.083	0.201	0.438	0.675	0.912	1.148	1.385	1.622
281	40.4	0.555	1.405	1.077	0.197	0.433	0.670	0.906	1.142	1.378	1.614
282	40.3	0.552	1.399	1.071	0.194	0.429	0.665	0.900	1.135	1.370	1.606
283	40.1	0.549	1.393	1.065	0.191	0.425	0.660	0.894	1.128	1.363	1.597
284	40.0	0.546	1.387	1.059	0.187	0.421	0.655	0.888	1.122	1.355	1.599
285	39.9	0.543	1.381	1.053	0.184	0.417	0.650	0.882	1.115	1.348	1.581
286	39.7	0.540	1.375	1.047	0.181	0.413	0.645	0.877	1.109	1.341	1.573
287	39.6	0.537	1.370	1.041	0.178	0.409	0.640	0.871	1.102	1.333	1.565


GRATING DETECTOR &
PSEUDO GRATING SIGNAL
FIRST PULSE
74S74
OSC
7451
74123
GRAT DET
555
GRATING SIGNAL
74LS14
7400

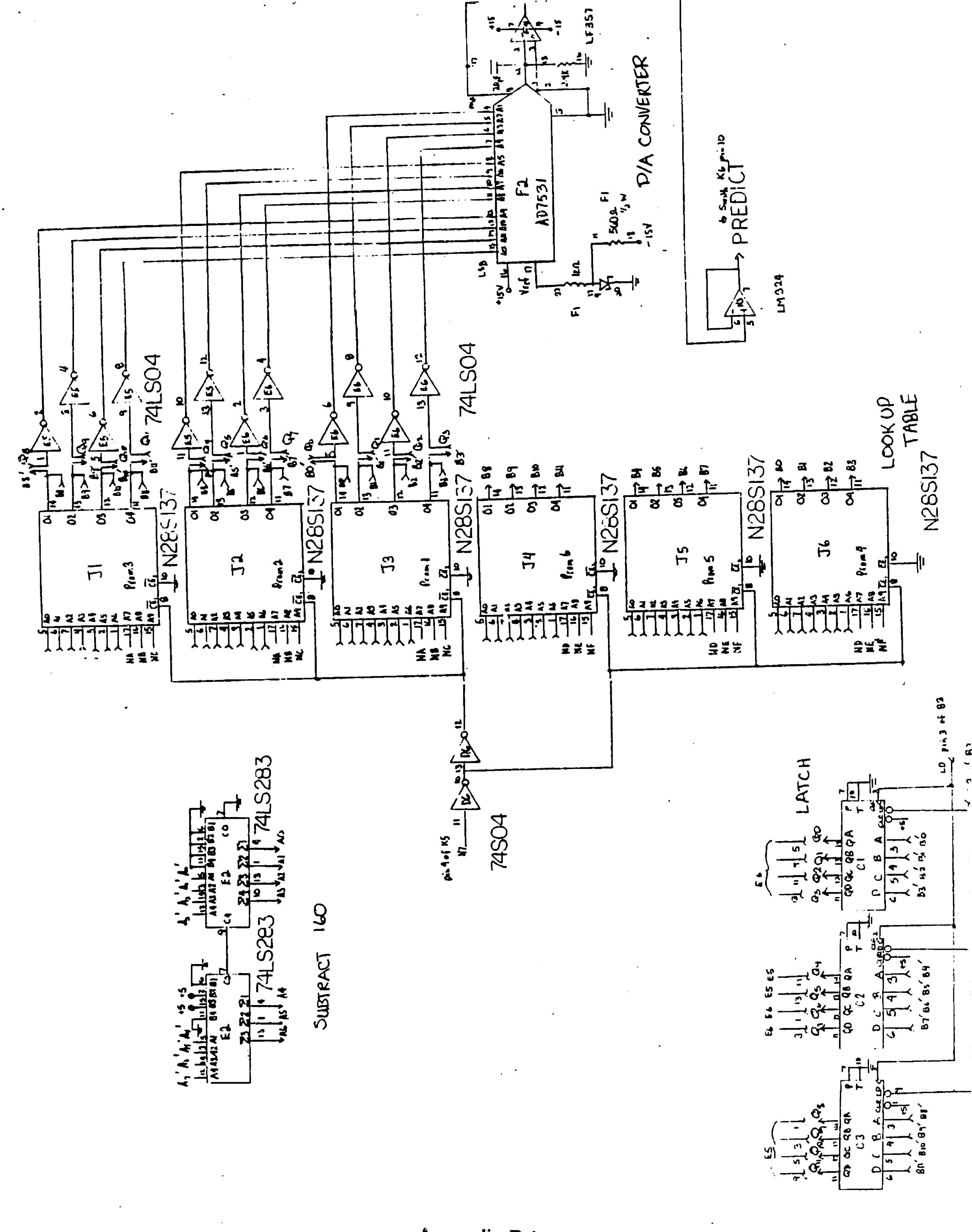
Appendix D1


CONTINUOUS GRATING
PHASE DETECTOR
MC4044
74S74
VCO OUT
VCO/N
7485
74S163
÷N COUNTER
LM324
FILTER
PREDICT
74LS51
74S04
74LS00
74S08
74S02
ENABLE VCO 3
ENABLE VCO1
ENABLE VCO2
74LS626
74LS11

Appendix D2


SYNC f_{in} TO CLK
74S74
74S74
74S00
LOAD CNTR
74S04
74S85
74S163
SYSTEM CLOCK
74S124
74LS163
LATCH
CNTR
CLK
TAPS

Appendix D3


D/A CONVERTER
F2
AD7531
LF357
PREDICT
LM324
74LS04
74LS04
N28S137
N28S137
N28S137
N28S137
N28S137
N28S137
J1
J2
J3
J4
J5
J6
LOOK UP
TABLE
74S04
74LS283
74LS283
SUBTRACT 160
LATCH
C1
C2
C3

Appendix D.4

Appendix E

Circuit Layout

A6	B6	C6	D6	E6	F6	J6	K6	L6	M6	N6
A5	B5	C5	D5	E5	F5	J5	K5	L5	M5	N5
A4	B4	C4	D4	E4	F4	J4	K4	L4	M4	N4
A3	B3	C3	D3	E3	F3	J3	K3	L3	M3	N3
A2	B2	C2	D2	E2	F2	J2	K2	L2	M2	N2
A1	B1	C1	D1	E1	F1	J1	K1	L1	M1	N1

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