NON-CONTACT DEFECT DETECTION IN SILICON

by

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ABSTRACT

Techniques for the non-contact evaluation of silicon wafers are presented and discussed. A prototype laser based scanning surface photovoltage tool was constructed which generates a high resolution image on an intensity modulated CRT of defects near the surface of p-type silicon wafers that give rise to minority carrier recombination. Samples are scanned with a HeNe laser and the surface photovoltage is detected by means of a capacitive detector. Defects detected include slip, swirl, scratches, and mobile ion contamination. The technique is completely non-contact and nondestructive. Correlations are shown between contact and non-contact scanning surface photovoltage, and x-ray topograph techniques.

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Bob Olyha

May 10, 1984

Yorktown Heights, NY
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Yonkers, NY

To a very special friend

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LIST OF ILLUSTRATIONS

NOMENCLATURE

$a(s)$ = Open loop gain
A = Area
C = Capacitance
d = $1/e^2$ Spot diameter
δ = Surface channel width
D = Diffusion constant in channel
D_s = Scan mirror diameter
ϵ_0 = Permittivity of vacuum
$\eta(x, y)$ = Excess real carrier density
f = Frequency
F = Focal length
G = Generation Rate
h = Detector to sample separation
I = Illumination
λ = Wavelength
Λ = Effective diffusion length
ω = Angular frequency
ρ = Reflectivity
r = Radius
R = Resistance
s = Complex frequency
S = Surface recombination velocity
θ = Angle
t = Time
v = Light spot velocity
V = Voltage

1.0 INTRODUCTION

1.1 SEMICONDUCTOR PROCESSING

1.1.1 Silicon Purification

After oxygen, silicon is the most abundant element in the earth's crust, accounting for 27.7% of its composition. For silicon to be used in the production of semiconductor grade crystals, electrically active impurity content must be lowered to concentrations of less than one part per billion. Metallurgical grade silicon is produced by reducing SiO_2 to silicon with carbon in a submerged electrode arc furnace. To purify the metallurgical grade silicon (98% Si), it is converted to $HSiCl_3$ in a fluidized bed reactor. The $HSiCl_3$ is then purified by conventional distillation techniques and then reacted with H_2 at high temperatures. Semiconductor grade polycrystalline silicon then deposits onto a polycrystalline silicon resistance heater over several hundred hours to achieve diameters of 200 mm.

1.1.2 Crystal Growth

Greater than 75% of the silicon grown for semiconductor fabrication employs the Czochralski method. The Czochralski process consists of dipping a small single crystal seed into molten silicon and slowly retracting the seed. The silicon melt charges are contained in silica crucibles and heated by either DC

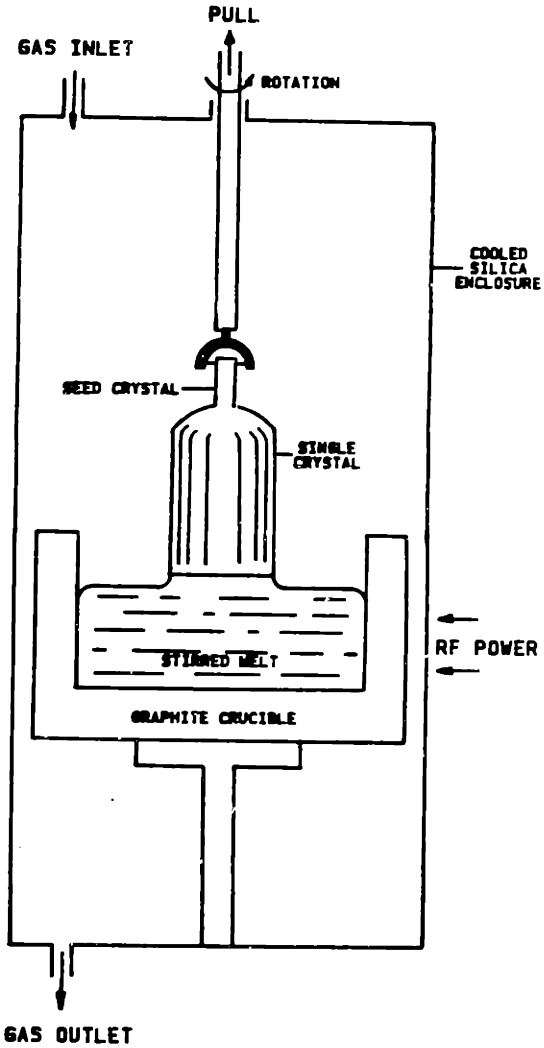

Figure 1. Czochralski Growth Apparatus

graphite heaters or three phase AC heaters. To reduce radial irregularities due to thermal gradients, the crystal seed and the crucible are counter-rotated. Very large magnetic fields are also introduced into the melt along the pull axis to compensate for the gravitational and thermal convection effects on the crystal

growth. Automatic controls are extensively used to control the diameter, pull rate, pressure, and temperature gradients in the crystal puller. The crucible is made of graphite with a fused silica lining. The atmosphere is usually argon at either slightly higher than atmospheric pressure or at a reduced pressure of 1 to 50 torr.

Industry standard crystals range in diameter from 75 - 125 mm after grinding to produce uniform crystals with diameters within $\pm$ 50 μm . Typical crystals are 1 m long.

The Czochralski technique introduces intentional and unintentional impurities into the crystal. The intentional impurities are the dopants, such as arsenic, used to determine the electrical properties of the crystal. The most important unintentional impurity is oxygen, which is introduced by the silica liner in which the melt is contained.[1] The oxygen distribution is a function of the various growth parameters used and is in the range of 10 - 50 ppm. Striations and axial variations of doping concentration[2] are also observed in Czochralski grown silicon. These are due to the nonuniformity of the thermal environment during crystal growth. Since the microscopic growth rate depends on the local temperature, the amount of dopant introduced varies slightly across the boule. The resistivity across a

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1 A. Murgai, W. J. Patrick, J. Combronde, J. C. Felix, *Oxygen Incorporation and Precipitation in Czochralski - Grown Silicon.* IBM J. Res. Dev. **26** (Sep. 1982) 546-52.

2 H. R. Huff, *Chemical Impurities and Structural Imperfections in Semiconductor Silicon.* Solid State Technol. **26** (Apr. 1983), 211-22.

typical wafer cut from a Czochralski grown crystal is within 20% of the nominal value. Another impurity introduced by the Czochralski technique is carbon. The carbon concentration is also a function of the growth rate and is believed to play a major role[3] in the segregation and formation of swirl[4] defects in silicon.

1.1.3 Wafer Production

Once the silicon single crystals are grown, they must be processed into wafers for microelectronic use. The crystals are first ground to a standardized size using a belt or wheel grinder. The crystallographic orientation of the crystal is determined through x-ray diffraction techniques and a reference flat is ground on a specific plane. The subsequent mask patterns are aligned to these flats so that the wafer will fracture along natural cleavage planes during the die separation process. The grinding damage is then removed by a chemical polishing etch.

The most common method for slicing silicon wafers employs an inside diameter saw blade supported around an outside edge. This slicing operation results in a loss of at least 250 μm of silicon for every slice, or about 30% of the crystal. The sawing process leaves a rough surface which is then removed with an isotropic silicon etch. The final front surface finish is achieved by a chemomechanical

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[3] A. Murgai, H. C. Gatos, W. A. Westdorp, *Effect of Microscopic Growth Rate on Oxygen Microsegregation and Swirl Defect Distribution in Czochralski-Grown Silicon.* J. Electrochem. Soc. **126** (Dec. 1979) 2240-45.

[4] H. Foll, U. Gosele, B. O. Kolbesen, *Swirl Defects in Silicon* in Semiconductor Silicon-77. Ed. H. R. Huff and E. Sirtl. New York: The Electrochemical Soc., 1977, 565-74.

polishing[5] process. The wafers are mounted on a carrier using wax or resin, or by friction against a silicone rubber compound. The polishing compound consists of a colloidal suspension of SiO_2 in an alkaline solution. The polishing compound is then removed with mechanical scrubbers using detergents, rinses in deionized water, and drying in nitrogen.

1.1.4 Hot Processes

Once the silicon wafers are polished, an initial heavy oxide is grown on the wafer to remove surface impurities that still remain from the manufacturing processes. During the high temperature heat treatments normally used, the oxygen introduced by the crucible liner during crystal growth forms SiO_2 micro-precipitates that getter metallic impurities and form a defect free zone[6] near the surface. In this process, known as intrinsic or back side gettering, preferential diffusion of metallic impurities occurs towards the SiO_2 precipitate sites.[7] These sites are positioned away from the active region of the devices, either on the back side of the wafer, or deep below the subcollector diffusion.

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5 F. G. Vieweg-Gutberlet, P. F. Siegesleitner, *Chemical Pretreatment and Electrical Behavior of Si Surfaces* in Semiconductor Silicon-77. Ed. H. R. Huff and E. Sirtl. New York: The Electrochemical Soc., 1977, 387-92.

6 P. Butler, *Controlling Oxygen in Silicon : Key to Higher VLSI Yields.* Semicond. Intl. 5 (Feb. 1982), 95-104.

7 S. M. Hu, W. J. Patrick, *Effect of Oxygen on Dislocation Movement in Silicon.* J. Appl. Phys. 46 (May 1975), 1869-74.

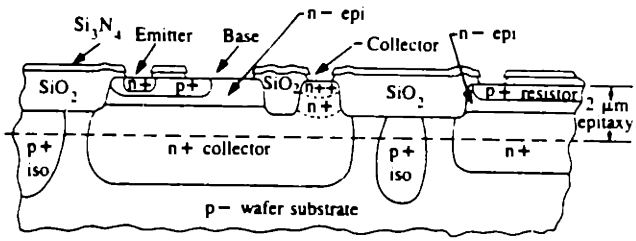

Figure 2. Bipolar Masterslice Cross-Section

Subsequent diffusions and oxidations are performed to construct the various junctions and layers as shown in Figure 2. Some of these steps can be performed at low temperatures using chemical vapor deposition (CVD) plasma oxides and ion implantations. Ion implantation is favored over thermal diffusion processes because the depth of the diffused layer can be very tightly controlled.

The initial hot processes can produce slip defects, which are line dislocations formed as a result of thermal shock to the wafer. The shocks result from abrupt temperature ramp profiles of diffusion furnaces and similar heating and cooling steps which tend to be more prominent in larger diameter wafers. As a result of the thermal shock, precipitates are nucleated at some grown-in defects. Slip dislocations then originate from these precipitate sites. These slip lines can develop and multiply during subsequent hot processes and form a grid pattern of

symmetrical cross slip dislocation loops.[8] Bipolar devices with slip dislocations were shown to exhibit significantly higher popcorn and 1/f noise characteristics as well as degraded DC performance.[9]

1.1.5 Lithographic Processes

Due to the rapid innovations in the semiconductor industry, it has quickly entered the very large scale integration (VLSI) era with the ability to mass produce integrated circuits with densities exceeding 100,000 transistors per chip. This demand for increased circuit density has resulted in significant advances into the field of lithography where micron (10^{-6} m) and sub-micron dimensions are currently being considered and implemented.[10] Optical techniques are most commonly employed in the production of line dimensions approaching 2 microns. This is limited by a combination of optical aberrations, the magnitude of the wavelength of light, and by the resolution of the photoresist systems used.[11]

A key component in optical lithography is the photomask. The accuracy and alignment of the mask has a direct impact on the resolution of the system. A major

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[8] J. Matsui, *Cross-Slip Dislocations and their Multiplication in (001),- Oriented Silicon Wafers.* J. Electrochem. Soc. **122** (Jul. 1975), 977-83.

[9] M. Conti, G. Corda, *Influence of Slip Plane Dislocations on Electrical Performances of N-P-N Planar Transistors.* IEEE Trans. Electron. Dev. **ED-18** (Dec. 1971), 1148-50.

[10] R. Moore, G. Caccoma, H. Pfeiffer, E. Weber, O. Woodward, *Electron Beam Writes Next Generation IC Patterns.* Electron. **54** (3 Nov. 1981), 138-44.

[11] P. Frasch, K. H. Saremski, *Feature Size Control in IC Manufacturing.* IBM J. Res. Dev. **26** (Sep. 1982), 561-67.

source of mask misalignment errors has been attributed to uncontrollable changes of field size.[12] Uncertainty of focus is the primary reason, but this is a function of the optical component adjustments and mask waviness. Electron beams are becoming more popular for the production of the primary photomasks for finer lines and spaces. Various efforts are underway to eliminate the photomask completely. The lift-off technology[13] is currently being used to define interconnecting metal films on ICs.

For dimensions under 2 microns, direct wafer write electron beam systems have been in industrial use for several years.[14] This has the advantages of excellent resolution and overlay, reduced defects, and quick turnaround time due to the elimination of the mask. Electron beam proximity printing is also being investigated for use in fabricating structures down to 0.3 microns.[15]

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[12] H. R. Rottmann, *Metrology in Mask Manufacturing.* IBM J. Res. Dev. **26** (Sep. 1982), 553-60.

[13] G. C. Collins, C. W. Halsted, *Process Control of the Chlorobenzene Single-Step Liftoff Process in a Diazo-Type Resist.* IBM J. Res. Dev. **26** (Sep. 1982), 596-604.

[14] H. S. Yourke, E. V. Weber, *A High-Throughput Scanning Electron Beam Lithographic System, EL-1, For Semiconductor Manufacture, General Description.* IEDM Tech. Digest. (1975), 431 - 47.

[15] H. Bohlen, J. Greschner, J. Keyser, W. Kulcke, P. Nehmiz, *Electron Beam Proximity Printing - A New High Speed Lithography Method for Submicron Structures.* IBM J. Res. Dev. **26** (Sep. 1982), 568-79.

1.2 QUALITY CONTROL

1.2.1 Cleanliness

The semiconductor device technology imposes severe conditions on the processing standards in terms of the purity of raw materials and their cleanliness during processing. As the dimensions of very large scale integrated (VLSI) circuits shrink, the situation becomes considerably more crucial. Particulate contamination and small crystalline defects will become the limiting factors to future development. In order to control the clean room environment, instruments are needed which can accurately and repeatably measure some degree of cleanliness. Numerous tools exist which can measure the particle density on semiconductor surfaces.[16]

One of the main points of wafer contamination is in their handling. Metal or vacuum tweezer damage and chipped wafer edges are common handling defects. These are usually lessened through the introduction of automatic wafer loaders, but minor problems remain. Airborne particles also produce defects in silicon. Any exposed wafer will acquire a number of particles over a period of time. Modern clean rooms[17] strictly filter the atmosphere to try and provide a particulate free environment. Laminar air flow, nonshedding synthetic coveralls,

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[16] See section 2.1.7

[17] Today's state of the art clean room (Class 50) has 50 particles per cubic foot of air equal to or greater than 0.5 micron in average diameter.

and numerous other techniques are used to limit the contamination of the clean room. The only way to reduce particulate contamination is to handle the wafers as little and as quickly as possible in an environment which is as clean as possible. All of the dust scanner tools are used to monitor how good these attempts are.

Chemicals used for semiconductor processing also have very stringent specifications. Low mobile ion electronic grade chemicals have very low levels of specific impurities which might influence the electronic properties of devices processed with their use. One of the most important chemicals used in microelectronic production is ultrahigh purity water. Deionized water is produced using a number of purification steps. Organic materials and chlorine are first removed with activated charcoal filters, and dissolved minerals are then removed through reverse osmosis. Further ion exchange cartridges and ultraviolet irradiation provide deionization and control the bacteria level. The final filtration is accomplished by passing the water through membranes that remove all particles larger than 0.22 μm.

1.2.2 Sampling Test Methods

Various methods of inspection are employed in the production of integrated circuits. A large number of tests are performed before the circuit processing even starts. Wafer manufacturers must abide by a large number of specifications and

tolerances. A representative silicon wafer quality control inspection cycle[18] is shown below.

Parameter	Method
Visual Surface	Collimated Light or Automatic Scanning Equipment
Swirl / Stacking Faults	Representative Thermal Cycle and Delineation Etch
Resistivity / Type / Gradient	Non-Contact Resistivity Gauge
Thickness / Variations	Non-Contact Thickness Gauge
Warp	Non-Contact Capacitive Sensor Probe[19]
Flatness	Interferometer or Automatic Multipoint Measurement
Flat Dimensions	Comparator or other direct measurement
Diameter	Ring Template or other direct measurement
Edge Rounding	Comparator or Visual Inspection
Oxygen Content	Fourier Transform Infrared Spectrometer
Carbon Content	Fourier Transform Infrared Spectrometer
Oxygen Precipitation Rate	FTIR before and after thermal cycle
Orientation	X-ray or Optical Diffraction

Once the wafer is accepted by the circuit processor, the wafers are processed in batches for throughput and homogeneity. Since all wafers that are processed in

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[18] J. H. Matlock, *Current Methods for Silicon Wafer Characterization.* Solid State Technol. 26 (Nov. 1983), 111-15.

[19] R. C. Abbe, *Semiconductor Wafer Measurements.* Solid State Tech. 17 (March 1974), 47-50.

parallel should have the same characteristics and develop the same faults, destructive sampling techniques can be used on a number of wafers in the batch. These wafers are known as monitor or control wafers and sometimes do not have any lithography placed on them. With these *blanket* monitors, it is easier to distinguish certain kinds of defects due to the lack of clutter from the pattern. These results are then correlated with the final device tests and yields to produce a statistical data base from which a yield model can be formed. These complex yield models[20] are then employed to update processes before the final tests are reached so that process faults can be corrected in a very short time.

1.3 PURPOSE OF RESEARCH

The objective of this research is to investigate and implement a practical tool for the detection of electrically active defects in silicon wafers. Electrically active defects are any defects that affect the final performance of an integrated circuit. These defects can be introduced anywhere during the processing cycle such as during the crystal growth step (dopant irregularities, oxygen precipitates), the wafer slicing step (saw damage, haze), the final polishing step (scratches), hot processes (slip, contamination), or the lithographic steps (particulates). In order to be a practical and attractive instrument, the tool should also be contactless, contamination free, and be able to scan a large area with high resolution in a short

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[20] C. H. Stapper, P. P. Castrucci, R. A. Maeder, W. E. Rowe, R. H. Verhelst, *Evolution ana Accomplishments of VLSI Yield Management at IBM.* IBM J. Res. Dev. **26** (Sep. 1982), 532-45.

period of time. Its sensitivity should be comparable to EBIC, x-ray topography, and selective etch techniques with ability to detect crystallographic defects and resistivity gradients.

The previous work in semiconductor characterization fulfilling these objectives will first be reviewed, highlighting each technique's strengths and faults. A theoretical discussion of the origin and potential use of the surface photovoltage will follow, with particular emphasis on the limits to sensitivity and resolution. The actual design and implementation of the experimental apparatus will then be presented followed by the design and construction of the electronic instrumentation necessary to support the tool. Scanning surface photovoltage images of various types of crystallographic defects and contaminants will then be reviewed and discussed, along with comparisons to other techniques. In conclusion, a final evaluation of the prototype and possible future improvements will be presented.

2.0 PREVIOUS WORK

2.1 SEMICONDUCTOR CHARACTERIZATION

2.1.1 Scanning Electron Microscopy

The scanning electron microscope (SEM) offers a wide variety of analytical modes applicable to semiconductor characterization. As the primary electron beam strikes the sample secondary electrons, backscattered electrons, x-rays, Auger electrons,[21] light (cathodoluminescence) and absorbed electrons are generated as in Figure 3 on page 26.[22] Electron beam induced current (EBIC) can be measured when charge carriers generated within the sample by the impinging beam move in response to an internal electric field. The electric field required may be produced by the fabrication of a p-n junction in the sample, a Schottky barrier at the surface, or by making the sample the dielectric medium of a capacitor.[23] In both cases, electrons and holes are swept in opposite directions by the field and this flow results in a current which is then displayed. Good electrical contact must be made to both sides of the junction and are usually established using spring loaded fine wire contacts or conductive paint. EBIC possesses resolution compa-

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[21] W. R. Bottoms, D. Guterman, *Electron Beam Probe Studies of Semiconductor - Insulator Interfaces.* J. Vac. Sci. Tech. 11 (Nov./Dec. 1974), 965-71.

[22] M. T. Postek, *The Scanning Electron Microscope in the Semiconductor Industry,* Test Meas. World. 3 (Sep. 1983), 54-75.

[23] H. J. Leamy, L. C. Kimerling, S. D. Ferris, *Electron Beam Induced Current,* Semicond. Int!. 2 (May 1979), 75-90.

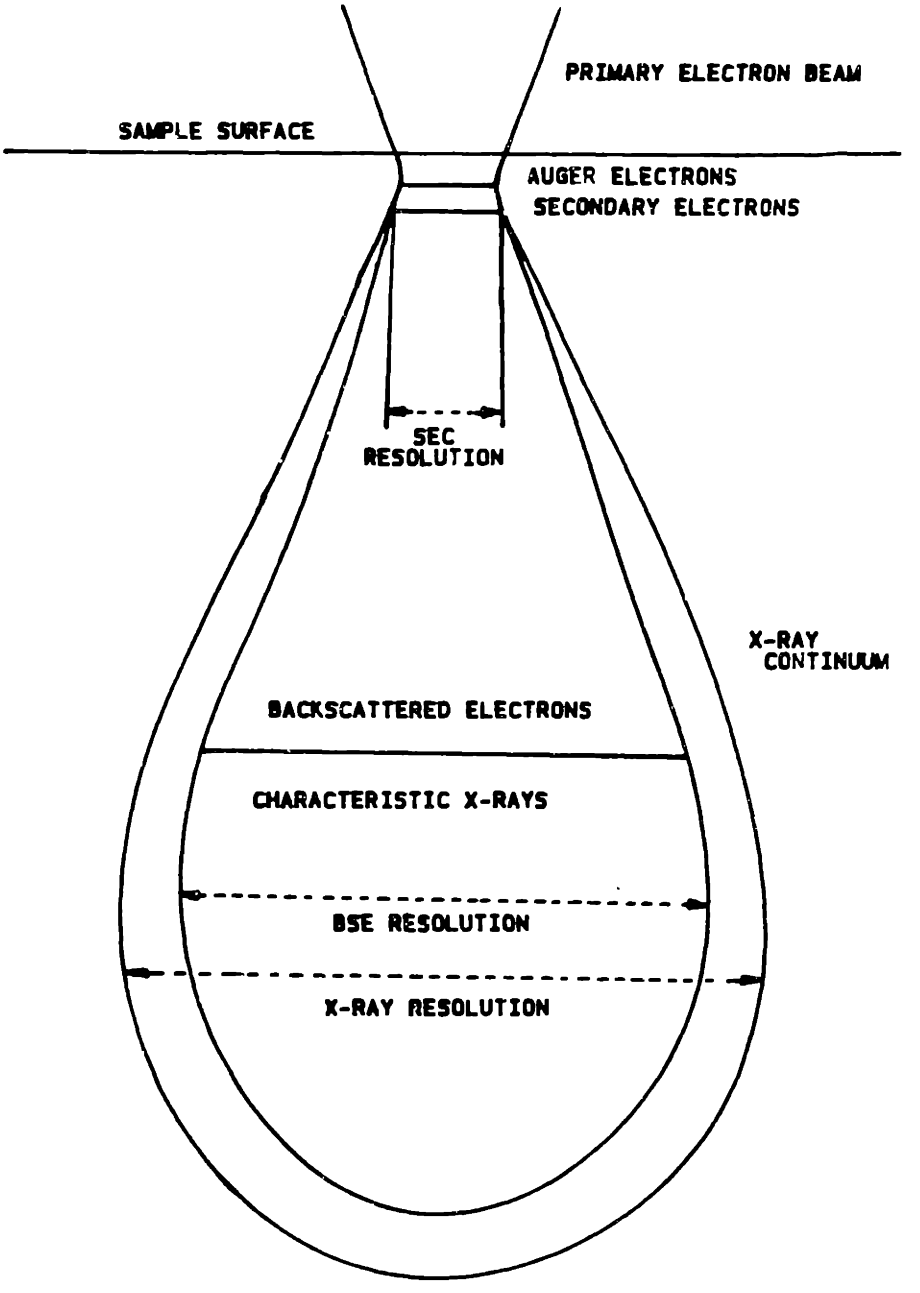

Figure 3. Signals Generated by the SEM

rable to or greater than optical microscopy and x-ray topography and is sensitive to electrically active defects such as dislocations, stacking faults, junction breakdown areas, metallization faults, and precipitates[24] on a scale comparable with the resolution of the system, (i.e. 0.5 μm). Electron beams may also be employed to study MOS structures by monitoring the secondary electron emission and x-ray fluorescence. [25]

2.1.2 X-ray Topography

Transmission x-ray topography has become the de-facto standard for nondestructive evaluation of large silicon wafers. This technique is very sensitive to lattice strain fields in the crystal formed by defects such as edge slip and double cross slip.[26] An x-ray source is projected incident upon the sample while exposing a photographic plate underneath the wafer. In this manner, a shadow is formed everywhere there is a defect at any depth in the wafer. Due to this complete lack of depth resolution, point defects have much lower resolution than defects that propagate through the entire wafer, such as slip. X-rays can also be used in conjunction with other selective decoration techniques to identify defects. Copper can be diffused onto the sample which then migrates and becomes trapped

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[24] H. F. Matare, C. W. Laakso, *Scanning Electron Beam Display of Dislocation Space Charge,* Appl. Phys. Lett. **13** (15 Sep. 1968), 216-18.

[25] W. R. Bottoms, D. Guterman, P. Roitman, *Contrast Mechanisms in Electron Beam Images of Interface Structures.* J. Vac. Sci. Tech. **12** (Jan./Feb. 1975), 134-39.

[26] A. George, G. Champier, *Double Cross-Slip in Silicon.* Philos. Mag. **31** (1975), 961-67.

around electrically active defects. In this manner, enhanced sensitivity can be obtained because the decoration shows up clearly in a subsequent x-ray topograph. This, however, is destructive.

2.1.3 Acoustic Microscopy

The electric field which accompanies surface acoustic waves has also been used to evaluate the electrical properties of semiconductor surfaces.[27] This field interacts with free charge carriers near the surface of an adjacent semiconductor to produce a DC acoustoelectric voltage across the semiconductor, which in turn, attenuates the surface acoustic wave. The degree of these effects is a function of the electric field associated with the surface acoustic wave and on semiconductor conductivity. These techniques are useful to determine the energy profile of the defect and impurity states averaged over the sample. Electrical contact must be made to the sample and these experiments are usually carried out in a liquid to enhance acoustic coupling and also at cryogenic temperatures.

2.1.4 Microwave Techniques

One of the early techniques for semiconductor characterization dating to 1958, involved the use of microwave radiation to determine lifetime in semicon-

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[27] P. Das, R. T. Webster, H. Estrada-Vazquez, W. C. Wang, *Contactless Semiconductor Surface Characterization Using Surface Acoustic Waves,* Surf. Sci. **86** (July 1979), 848-57.

ductors.[28] In the *electrodeless method* a combination of microwave absorption and optical injection was utilized. A DC white light source was swept across the sample as the transmitted power of the microwave source is measured. The source consisted of a well regulated klystron operating with 2 mW at a frequency of 24 Ghz. The transmitted power is measured with a tuned diode and the lifetime is determined by the time constant of the observed output pulse.

Although this method is truly contactless, it suffers from a lack of resolution since the measurement is averaged over the cross sectional area of the waveguide. Another problem of this technique is that the sample must be cut to the required size and shape and placed inside the waveguide. The latter problem was later solved by changing the arrangement to monitor microwave reflection rather than absorption.[29] Xenon flash lamps were used to provide the intermittent flashes of light. The resolution problem was also solved through the use of a laser source from which a full wafer could be scanned at spot size limited resolution. A commercial unit is presently available based upon this principle.[30] This instrument overcomes the area and resolution problem, but since the exponential decay time

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[28] A. P. Ramsa, H. Jacobs, F. A. Brand, *Microwave Techniques in Measurement of Lifetime in Germanium*, J. Appl. Phys. **30** (Jul. 1959), 1054-60.

[29] S. Deb, B. R. Nag, *Measurement of Lifetime of Carriers in Semiconductors Through Microwave Reflection*, J. Appl. Phys. **33** (Apr. 1962), 1604.

[30] *Wafer Tau series*, LEO Giken Co., Ltd.

must be measured at each scan point, the full wafer scan time is only useful on a sampling basis.

Microwave reflection has also been applied to the determination of bulk resistivity of polycrystalline silicon wafer utilizing the absolute measurements for absorbed power.[31] Microwaves have also been used to pulse semiconductor samples[32] to produce hot carriers which in turn modulate the photogradient electromotive force across the sample.

2.1.5 Zerbst Techniques

Carrier lifetime and surface generation velocities can also be determined from pulsed metal - insulator - semiconductor (MIS) measurements. The traditional experimental technique has been to measure the capacitance or conductance as a function of a DC or slowly varying bias voltage. By operating the device in the pulse mode, it has become feasible to investigate the recombination properties of the oxide - semiconductor interface and the silicon itself. Zerbst[33] developed a technique which allowed both the generation lifetime and the surface recombination velocity to be extracted from the capacitance time delay

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[31] J. S. Culik, *Determination of the Bulk Resistivity of Polycrystalline Silicon Wafers Using a Microwave Reflection Technique* in Proc. Fifteenth IEEE Photovoltaic Specialists Conf. (1981), 1170-73.

[32] S. Asmontas, J. Pozela, K. Repsas, *The Photogradient E.M.F. of Hot Carriers.* Phys. Stat. Sol. **51** (1 May 1972), 225-32.

[33] M. Zerbst, *Relaxation Effects in MIS Structures.* Z. Agnew. Phys. **22** (Dec. 1966), 30-33.

curve. In order to generate a lifetime map[34] of a large area semiconductor surface, a large number of small metal pads can be evaporated onto the surface and probed separately.

In a similar technique,[35] the transient decay of short circuit current after pulsed laser excitation is used to determine minority carrier lifetime in junction structures.

2.1.6 Infrared Techniques

Measurements of the infrared optical properties of semiconductors have also been applied to semiconductor characterization. The infrared transmittance or infrared reflectance of semiconductor materials can provide information on internal inhomogeneities, minority carrier lifetime,[36] and impurity precipitates.[37] The absorption coefficient increases with wavelength and also with increasing carrier concentration. The technique displays an image generated by scanning a finely focused infrared laser beam across the surface of a sample. The transmitted or reflected beam is then detected by a solid state infrared detector and displayed

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[34] D. K. Schroder, J. Guldberg, *Interpretation of Surface and Bulk Effects Using the Pulsed MIS Capacitor.* Solid-State Electron. **14** (1971), 1285-97.

[35] M. Di Giulio, S. Galassini, G. Micocci, A. Tepore, *Determination of Minority-Carrier Lifetime in Silicon Solar Cells From Laser-Transient Photovoltaic Effect.* J. Appl. Phys. **52** (Dec. 1981), 7219-23.

[36] J. C. Herper, I. Palocz, N. N. Axelrod, R. A. Stern, *Laser Probing of Carrier Diffusion Dynamics.* J. Appl. Phys. **45** (Jan. 1974), 224-29.

[37] D. C. Gupta, B. Sherman, E. D. Jungbluth, J. F. Black, *Non-Destructive Semiconductor Testing Using Scanned Laser Techniques.* Solid State Technol. **14** (Mar. 1971), 44-50.

in a raster scanned format. The amount of infrared emission from a sample which is under intense illumination is a function of its temperature. In order to raise the detectability of this signal, the sample may be heated[38] so that more of the generated emission escapes from the sample to be detected.

2.1.7 Selective Etching

Many different etch formulations have been proposed over the years to allow visibility of silicon defects. Most of the production line defect analysis employed today utilizes one of three well established etches.[39] The Sirtl, Secco, and Wright etches are all chromium and hydrofluoric acid based preferential etches which produce optically visible etch pits around defects in silicon. These decoration etches are targeted to remove the top 10 microns of the silicon surface, since this is the region of interest for actual devices.

Electrochemical etching has also been used for detecting defects in silicon.[40] Anodic bias in HF solution establishes enhanced electrochemical etching at defect sites which can then be observed optically.

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[38] J. C. White, T. F. Unter, J. G. Smith, *Contactless Nondestructive Technique for the Measurement of Minority-Carrier Lifetime and Diffusion Length in Silicon.* Solid-State Electron. Dev. 1 (Sep. 1977), 139-45.

[39] J. H. Matlock, *Current Methods for Silicon Wafer Characterization.* Solid State Technol. 26 (Nov. 1983), 111-15.

[40] J. L. Deines, J. W. Philbrick, M. R. Poponiak, D. B. Dove, *Correlation of Electrolytic-Etch and Surface - Photovoltage Techniques for the Detection of Electrically Active Defects in Silicon.* Appl. Phys. Lett. 34 (1 June 1979), 746-48.

2.1.8 Angle Lapping

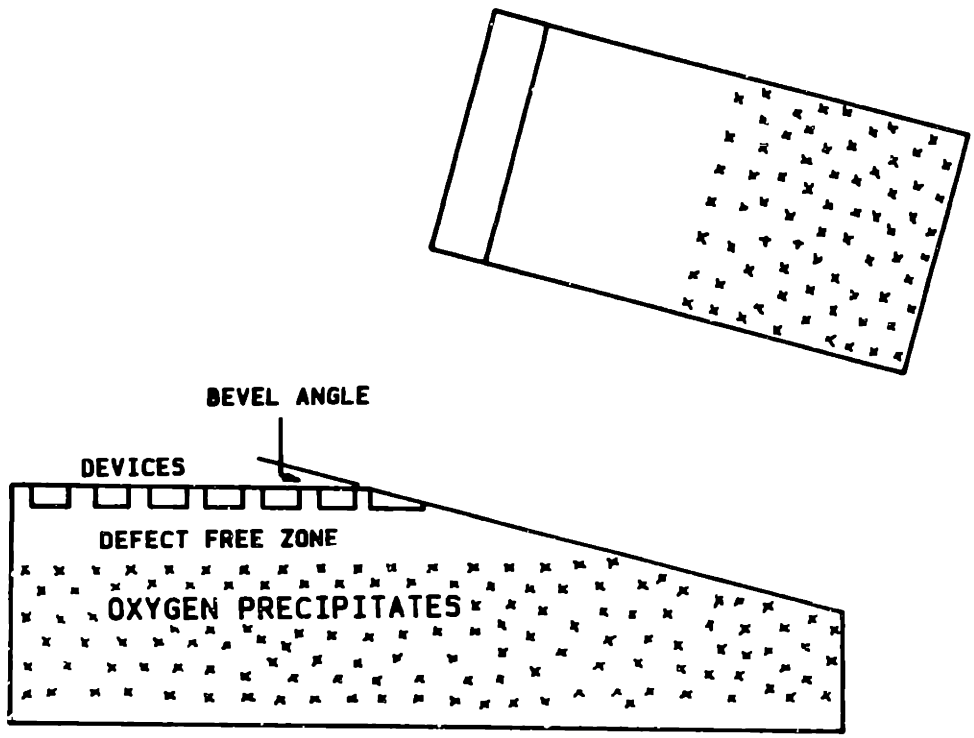

Figure 4. Bevel Angle Lap

The measurement of the depth of the denuded or defect free zone is commonly accomplished by using a bevel polish or angle lapping technique (Figure 4). This effectively magnifies the depth of the denuded zone so that for an accurately lapped angle, this can be measured directly with an optical microscope. For a typical angle of 2° this yields a magnification factor of almost 30.

2.1.9 Scattered Light

Surface evaluation of semiconductor materials is commonly done through the use of reflected and scattered light detection. In these techniques, a finely focused intense illumination source is projected onto the surface of interest, and any particles present will reflect and disperse the light. Subjective means were used to compare marks on the surface with standardized scratches on sample wafers, but these manual methods varied considerably among inspectors. For this reason, a number of automated laser based scanners were developed to provide repeatable and accurate results. The tools detect reflected light back through the beam path,[41] [42] through an alternate lens system,[43] or through the use or large angle light collectors[44] and fiber optic arrays.[45] Photomultiplier tubes and

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[41] L. R. Baker, B. J. Biddles, *Surface Inspection of Optical and Semiconductor Components.* Opt. Eng. **15** (May-June 1976), 244-46.

[42] D. R. Oswald, D. F. Munro, *A Laser Scan Technique for Electronic Materials Surface Evaluation.* J. Electron. Mater. **3** (Feb. 1974), 225-42.

[43] H. J. Ruiz, C. S. Williams, F. A. Padovani, *Silicon Slice Analyzer Using a He-Ne Laser.* J. Electrochem. Soc. **121** (May 1974), 689-92.

[44] P. Gise, *Principles of Laser Scanning for Defect and Contamination Detection in Microfabrication.* Solid State Tech. **26** (Nov. 1983), 163-65.

[45] J. W. Alford, R. D. Vanderneut, V. J. Zaleckas, *Laser Scanning Microscopy.* Proc. IEEE. **70** (Jun. 1982), 641-51.

polarized illumination[46] have also been used to produce an automatic dust scanner for which a U.S. patent was awarded.[47]

2.1.10 Photoluminescence

Photoluminescence measurements are among the simplest methods for detecting defects in luminescent crystals and have been widely applied to compound semiconductors such as GaAs.[48] However, this method has not been applied as easily to silicon because of its low luminescence efficiency at room temperature. With the use of a high power ion laser as the source of excitation, photoluminescence profiles can be taken at room temperatures with conventional photomultiplier tubes.[49] The luminescence spectra is in the infrared region and hence can also be observed with an infrared vidicon TV camera[50] for large area, real time imaging. For detection of small defects such as stacking faults and dislocations, scanning spot excitation and modulation techniques are needed to

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[46] E. F. Steigmeier, H. Auderset, *Optical Scanner for Dust and Defect Detection.* RCA Rev. 44 (Mar. 1983), 5-18.

[47] U.S. patent 4,314,763 filed Jan. 4, 1979, issued Feb. 9, 1982.

[48] O. D. Knab, V. I. Magalyas, V. D. Frolov, V. I. Shveikin, I. A. Shmerkin, *Measurement of the Photoluminescence Photo-EMF and Electroluminescence of Semiconductor Materials and Structures.* Instrum. & Exp. Tech. 14 (Jul.-Aug. 1971), 1219-21.

[49] H. Nakashima, Y. Shiraki, *Photoluminescence Observation of Swirl Defects and Gettering Effects in Silicon at Room Temperature,* Appl. Phys. Lett. 33 (1 Aug. 1978), 257-58.

[50] H. Nakashima, Y. Shiraki, *Photoluminescence Topographic Observation of Defects in Silicon Crystals,* Appl. Phys. Lett. 33 (15 Sep. 1978), 545-46.

obtain the desired resolution. This technique is good for quick, large full wafer probing, but for small areas the time required is considerable.

2.1.11 Photoemission

Scanned internal photoemission (SIP) has been used[51] to display lateral inhomogeneities between semiconductor interfaces in a manner which is very similar to EBIC. The process of internal photoemission can best be understood in terms of a three step process. First there is the photoexcitation of electrons, followed by the carrier transport to the surface, and then transmission over the barrier. SIP primarily determines the presence of small inhomogeneities in the contact barrier between the semiconductor and insulator. This is useful in imaging local variations of the barrier due to contamination, impurity segregation, and structural or crystallographic defects. Photoemission images are usually obtained from the Schottky barrier of MOS structures in which the metal contact is semi-transparent (such as indium tin oxide).

2.1.12 Junction Scanning Surface Photovoltage

Various techniques have been presented and widely used to characterize the

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[51] T. H. Di Stefano, *Photoemission and Photovoltaic Imaging of Semiconductor Surfaces.* NBS Pub. 400-23. (Mar. 1976), 197-209.

photoresponse of p-n junction structures.[52] These methods are also directly analogous to EBIC results and are extensively used for photocell evaluation. Large area scans have given qualitative and quantitative information about semiconductor diode and transistor junction properties near the semiconductor surface. These methods can obtain the effective minority carrier lifetime by monitoring the decay rate of current[53] after pulsed laser excitation. The standardized test method for carrier diffusion length measurements is done in this manner.[54]

2.1.13 Contact Scanning Surface Photovoltage

Some surface photovoltage methods have been demonstrated that do not require a p-n junction in the sample. Instead, a wire mesh is pressed against the surface to form Schottky barriers at all contact points.[55] This method produces a voltage replica of the resistivity variations in the wafer under test. This also requires that the wafer be oxide free, to provide a good electrical connection to the sample. Early techniques employed soldered connections[56] while more recent

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[52] C. N. Potter, D. E. Sawyer, *A Flying-Spot Scanner.* Rev. Sci. Instrum. **39** (Feb. 1968), 180-83.

[53] L. A. Kasprzak, *High Resolution System for Photoresponse Mapping of Semiconductor Devices.* Rev. Sci. Instrum. **46** (Mar. 1975), 257-62.

[54] ANSI / ASTM F 391-78, *Standard Test Method for Minority Carrier Diffusion Length in Silicon by Measurement of Steady State Photovoltage.*

[55] H. F. Matare, *Photoelectric Scanning of Wafer Inhomogeneities.* Solid State Technol. **20** (Sep. 1977), 56-60.

[56] J. Oroshnik, A. Many, *Evaluation of the Homogeneity of Germanium Single Crystals by Photovoltaic Scanning.* J. Electrochem. Soc. **106** (Apr. 1959), 360-62.

ones have used electrolytes,[57] ,[58] ,[59] evaporated metal,[60] ,[61] ,[62] single point,[63] and multiple point edge contacts.[64] When these multiple edge contacts are made, considerable mathematical transformations must be performed to relate the resistivity gradient along a wafer diameter to the photovoltage measured at the diameter ends on the rim of the wafer. Blackburn[65] and Larrabee[66] later developed transformations that allowed them to determine the resistivity gradient across the wafer from a single edge contact.

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[57] D. L. Lile, N. M. Davis, *Semiconductor Profiling Using an Optical Probe.* Solid-State Electron. **18** (1975), 699-704.

[58] E. Kamieniecki, *Determination of Surface Space Charge Capacitance Using a Light Probe.* J. Vac. Sci. Technol. **20** (Mar. 1982), 811-14.

[59] D. E. Hill, *Detection of Latent Scratches and Swirl on Silicon Wafers by Scanned Surface Photoresponse.* J. Appl. Phys. **51** (Aug. 1980), 4114-18.

[60] H. Reichl, H. Bernt, *Lifetime Measurements in Silicon Epitaxial Materials.* Solid-State Electron. **18** (1975), 453-58.

[61] C. R. Viswanathan, S. Ogura, *Silicon-Oxide Interface Studies by a Photoelectric Technique.* Proc. IEEE. **57** (Sep. 1969), 1552-57.

[62] U. Efron, J. Grinberg, *Characterization of Low-Doped Metal Oxide Semiconductor (MOS),Structures Using Pulsed Photoinjection.* Proc. Soc. Photo-Opt. Instrum. Eng. **276** (1981), 59-60.

[63] L. B. Valdes, *Measurement of Minority Carrier Lifetime in Germanium.* Proc. IRE. **40** (Nov. 1952), 1420-23.

[64] D. L. Blackburn, H. A. Schafft, L. J. Swartzendruber, *Nondestructive Photovoltaic Technique for the Measurement of Resistivity Gradients in Circular Semiconductor Wafers.* J. Electrochem. Soc. **119** (Dec. 1972), 1773-78.

[65] D. L. Blackburn, *Photovoltaic Technique for Measuring Resistivity Variations of High Resistivity Silicon Slices.* J. Res. Natl. Bur. Stand. **83** (May-June 1978), 265-71.

[66] R. D. Larrabee, D. L. Blackburn, *Theory and Application of a Nondestructive Technique for the Measurement of Resistivity Variations in Circular Semiconductor Slices.* Solid-State Electron. **23** (Oct. 1980), 1059-68.

2.1.14 Capacitive Surface Photovoltage

It has been claimed[67] that neither lifetime gradients nor the Dember effect can be measured if the specimen is terminated by ohmic contacts. This is due to the contact photoemf that is generated. To eliminate this problem, capacitive contacts are needed. Capacitive sensors for the detection of the surface photovoltage exist in a number of different form and geometries. The most sensitive contacts are those made with MOS structures, where a metallic pad is evaporated onto an oxidized silicon sample.[68] Vibrating reed electrometers[69] (Kelvin probes), and transparent electrodes[70,71] with mylar[72] or mica[73] dielectrics are also used to provide coupling to the signal.

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67 R. M. Esposito, J. J. Loferski, H. Flicker, *Concerning the Possibility of Observing Lifetime-Gradient and Dember Photovoltages in Semiconductors.* J. Appl. Phys. **38** (Feb. 1967), 825-31.

68 O. Engstrom, B. Drugge, P. A. Tove, *Laser Scanning Technique for the Detection of Resistivity and Lifetime Inhomogeneities in Semiconductor Devices.* Phys. Scr. **18** (Dec. 1978), 357-63.

69 B. Goldstein, D. Redfield, D. J. Szostak, L. A. Carr, *Electrical Characterization of Solar Cells by Surface Photovoltage.* Appl. Phys. Lett. **39** (1 Aug. 1981), 258-60.

70 A. M. Goodman, *A Method for the Measurement of Short Minority Carrier Diffusion Lengths in Semiconductors.* J. Appl. Phys. **32** (Dec. 1961), 2550-52.

71 R. S. Nakhmanson, Z. Sh. Ovsyuk, L. K. Popov, *Frequency Dependence of the Photo-EMF of Strongly Inverted Ge and Si MIS Structures-II. Experiments.* Solid-State Electron. **18** (1975), 627-34.

72 C. Munakata, N. Honma, H. Itoh, *A Non-Destructive Method for Measuring Lifetimes for Minority Carriers in Semiconductor Wafers Using Frequency-Dependent AC Photovoltages.* Jpn. J. Appl. Phys. Pt. 2. **22** (Feb. 1983), L103-5.

73 E. O. Johnson, *Measurement of Minority Carrier Lifetimes with the Surface Photovoltage.* J. Appl. Phys. **28** (Nov. 1957), 1349-53.

2.1.15 Dember Effect

The Dember or photodiffusion effect can be observed in semiconductors when the electrons and holes have different mobilities and the illumination of the sample leads to a non-uniform distribution of carriers.[74] The difference of mobility yields an internal electric field which produces a voltage whose magnitude is[75]

$$V_{Demb} = \frac{kT}{q} \frac{(\mu_n - \mu_p)}{(\mu_p p_e + \mu_n n_e)} (\Delta n_L - \Delta n_0) \qquad [2.1]$$

where Δn_0 and Δn_L are the extra electron concentration at the surfaces ($x = 0$ and $x = L$) due to the illumination, and n_c and p_c are the equilibrium carrier concentrations. For typical silicon wafers, this expression yields an open circuit voltage of approximately 1 mV for a light intensity of 5×10^{15} photons/cm^2-sec. This is also slightly sensitive to the wavelength of illumination due to the change in absorption coefficient of the sample.[76]

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[74] G. Forgacs, G. Pataki, *Anomalous Dember Effect in the Case of Cylindrical Illumination.* Acta Phys. Acad. Sci. Hung. **34** (1973), 311-25.

[75] Y. Moreau, J. C. Manifacier, H. K. Henisch, *On the Dember-Effect and a New Trap-Controlled Photo- Polarization.* Solid-State Electron. **24** (Sep. 1981), 883-85.

[76] I. P. Zhad'ko, *Spectral Characteristic of the Transverse Dember Effect in Inhomogeneous Anisotropic Semiconductors.* Sov. Phys.-Semicond. **11** (Aug. 1977), 952-53.

2.1.16 Other Techniques

When a mechanical stress is applied to a semiconductor wafer with a depletion surface layer, (nearly insulating), an electric polarization (surface piezoelectric effect[77]) is induced at the surface layer. Surface states then change due to the recombination transitions and can be monitored by the charge transfer between the surface and the bulk. This transfer of charge can then be measured with a vibrating reed electrometer and a reference MIS contact.

Semiconductor samples have also been placed in magnetic fields and illuminated to determine carrier density through the photoelectromagnetic effect.[78] This observed effect is a function of the surface recombination velocity and the roughness of the surface.

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[77] J. Lagowski, I. Baltov, H. C. Gatos, *Surface Photovoltage Spectroscopy and Surface Piezoelectric Effect in GaAs.* Surf. Sci. **40** (1973), 216-26.

[78] W. J. Lum, A. K. Nedoluha, H. H. Wieder, *Electro-Optical Characterization of Semiconductors.* Proc. Soc. Photo-Opt. Instrum. Eng. **276** (1981), 48-54.

3.0 THEORETICAL DISCUSSION

3.1.1 Background

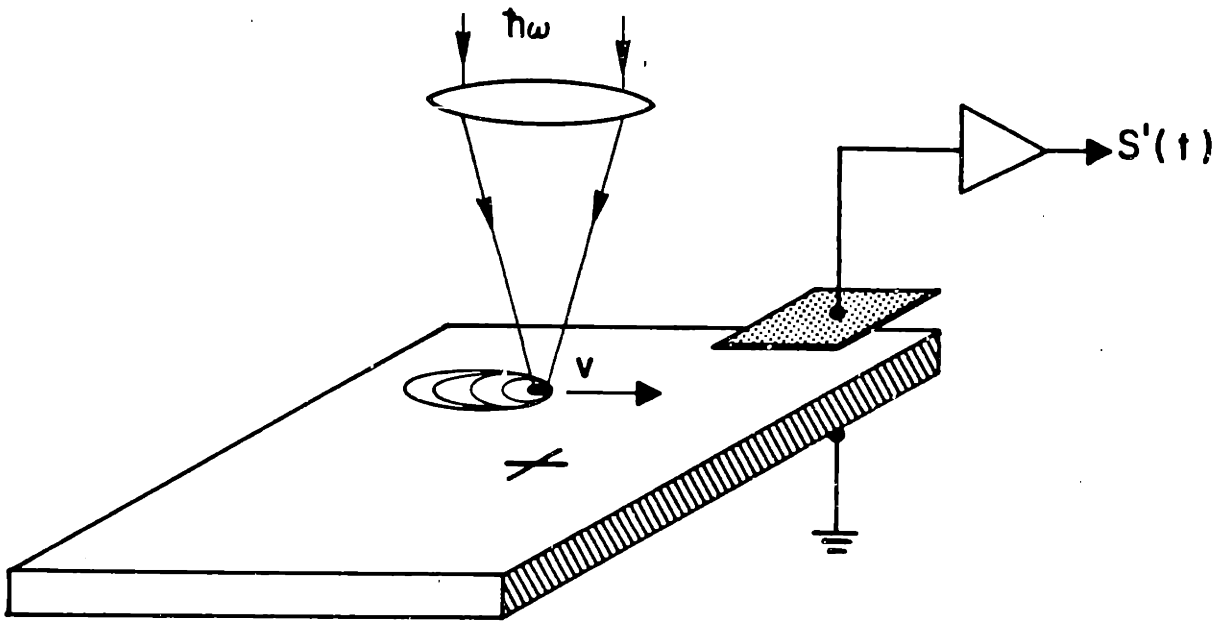

Figure 5. Scanning Surface Photovoltage Measurement: The light spot, scanned at a velocity v, traverses the sample producing a comet shaped excess carrier distribution. The resulting surface charge is detected by measuring the displacement current in a capacitively coupled electrode.

The method used in this technique will be the capacitive scanning surface photovoltage as discussed earlier in section 2.1.14. The approach used here produces an image of minority carrier recombination sites over the surface of a semiconductor which are caused by crystallographic defects. A focused DC light spot is scanned across the sample at high rates, developing a comet shaped cloud of minority carriers. Some of these carriers become trapped in a shallow depletion

region while most diffuse over the sample and develop the surface potential which can be measured by the capacitively coupled detector. When the charge cloud traverses a defect at high rates, the local recombination produces a drop in the local surface potential. This abrupt change in potential produces a displacement current in a capacitive detector which is coupled to the surface which is then displayed as a function of the light spot position (x, y) on an intensity modulated CRT.

3.1.2 Experimental Resolution

In order to determine the resolution capabilities of this method it is necessary to investigate the carrier diffusion equations. In order to keep things simple, the density of optically generated carriers is assumed to be small (low level injection) so that the average surface recombination rate is not greatly effected by the presence of surface defects. In this manner also, most of the excited carriers will be trapped in the surface depletion region. In equilibrium, the generation rate, G, then equals the total recombination rate, R,

$$G - \int\int N\eta(x - x_0, y - y_0)R(x, y)dxdy = 0 \qquad [3.1]$$

and N is the number of excess minority carriers with a distribution of $\eta(x,y)$ around the light spot (x_0,y_0), and R(x, y) is the local recombination rate for the two

dimensional carrier density $N\eta$. The detected signal, S, is proportional to the time rate of change of the average photovoltage

$$S \propto \frac{G\delta\epsilon_I v}{\epsilon_S \tau} \int\int \frac{\partial \eta}{\partial x}(x - x_0, y - y_0) R(x, y) dx dy \qquad [3.2]$$

where δ is the effective depletion layer width, ϵ_I and ϵ_S are the permittivity of the oxide and silicon respectively, v is the scanning spot velocity, and τ is the average lifetime of the surface carriers. The signal is proportional to a convolution of the recombination rate R(x, y) with the sampling function $\frac{\partial \eta}{\partial x}$. The sample function is ideally a double Dirac delta function, but the finite diameter of the light spot causes the delta function to become slightly smeared and the resolution is reduced.

To estimate the experimental resolution, $\frac{\partial \eta}{\partial x}$ is evaluated under the low level injection conditions stated earlier. In order to determine $\eta(x,y)$ the diffusion equation in the coordinate frame of the moving light spot and an unilluminated sample becomes

$$D\nabla^2\eta - v\frac{\partial \eta}{\partial x} - \frac{\eta}{\tau} = 0 \qquad [3.3]$$

where D is the effective diffusion coefficient in the surface channel. Using the transformation,

$$\eta = ne^{vx/2D} \qquad [3.4]$$

the equation simplifies to

$$D\left[\frac{\partial^2 n}{\partial x^2}+\frac{\partial^2 n}{\partial y^2}+\frac{\partial n}{\partial x}\frac{v}{D}+n\frac{v^2}{4D^2}\right]-v\left[n\frac{v}{2D}+\frac{\partial n}{\partial x}\right]-\frac{n}{\tau}=0$$

$$D\nabla^2 n-n\left(\frac{v^2}{4D}+\frac{1}{\tau}\right)=0$$

$$\nabla^2 n-\frac{n}{\Lambda^2}=0 \qquad [3.5]$$

where the effective diffusion length, Λ, depends upon the scanning velocity

$$\Lambda=\frac{\sqrt{D\tau}}{\sqrt{1+\frac{v^2\tau}{4D}}}. \qquad [3.6]$$

The solution for $\eta(x,y)$ in mixed coordinates becomes

$$\eta=Be^{-vx/2D}K_0\left(\frac{r}{\Lambda}\right) \qquad [3.7]$$

where K_0 is a modified Bessel function of the second kind[79] and B is defined as

$$B=\frac{2(1-\rho)I\tau}{\pi\hbar\omega\Lambda^2} \qquad [3.8]$$

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[79] F. B. Hildebrand, Advanced Calculus For Applications. Prentice-Hall: New Jersey, 1976.

where ρ is the reflection coefficient of the surface. The surface carrier density is comet shaped (see Figure 5 on page 42), especially for scan velocities $v > \sqrt{\frac{4D}{\tau}}$. The asymptotic solutions for η are

$$\eta(r \to \infty) \cong B\sqrt{\frac{\pi\Lambda}{2r}}\, e^{\frac{-r}{\Lambda}} \qquad [3.9]$$

$$\eta(r \to 0) \cong B\, ln\left(\frac{\Lambda}{r}\right) \qquad [3.10]$$

The sampling function $\frac{\partial\eta}{\partial x}$ is plotted[80] in Figure 6 on page 47 for several scan velocities and reasonable values for D and τ. The form of $\frac{\partial\eta}{\partial x}$ near the origin deviates marginally from $1/r$ except at small τ and large scan velocities. As shown in the figure, the leading edge of the charge cloud becomes sharper with increased scan velocities while the trailing edge goes through a transition of getting wider and then sharper with increased velocities. This change in the trailing edge is due to the decreasing logarithmic slope and the increasing magnitude of the tail of the charge distribution with increasing scan velocity.

The biggest advantage to using high scan rates with the scanning surface photovoltage is the high resolution sampling function $\frac{\partial\eta}{\partial x}$. This sampling function is much sharper than the photoexcited charge density η due to the loga-

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[80] From J. W. Philbrick, T. H. Di Stefano, *Scanned Surface Photovoltage Detection of Defects in Silicon Wafers.* IEEE 13th An. Proc. Rel. Phys. (1975), 159-67.

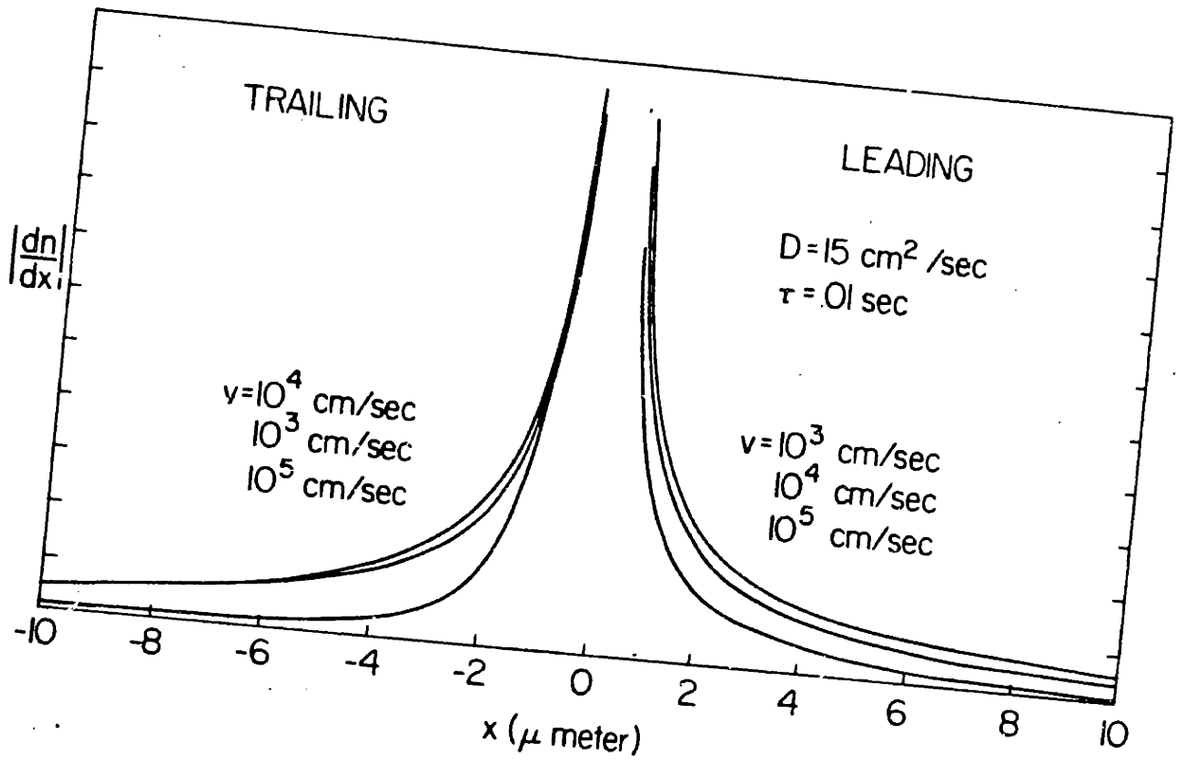

Figure 6. Sampling Function $\frac{\partial \eta}{\partial x}$: The normalized differentiated surface charge due to a light spot scanned at a velocity v.

rithmic singularity at r = 0. As an example, for large τ the 1/e resolution of the fast scan surface photovoltage is $\frac{r}{d} \cong 2.718$, where d is the light spot diameter.

4.0 EXPERIMENTAL

4.1 OPTICAL SYSTEM

4.1.1 Scanning System

As the name scanning surface photovoltage implies, a focused spot of light must be scanned over the area of the sample. For use in this application, a number of constraints limit our choices of scanning topologies. The specifications of interest are -

- Small Spot Size
- Flat Field Focal Plane
- Accurate Spot Positioning
- High Spot Velocity
- High Optical Efficiency
- Compact
- Reasonable Cost

The first consideration is the choice of the light source. Monochromatic illumination is desired for the optics, as a white light source cannot be easily focused to the fine spot needed. A very high power incandescent or gas discharge source followed by a monochromator can be used at the expense of very large power

losses. Since the successful operation of the first laser in 1960, they have virtually replaced all other monochromatic light sources.[81] Modern lasers are capable of providing higher power densities than any incoherent light source.[82] For example, a 15 mW helium neon gas laser can produce power densities in excess of 1 GW/m^2. The use of a laser also simplifies the design of the optical components due to the fixed wavelength output. For this application, a Spectra Physics Model 124B HeNe laser specified to 15 mW at 6328Å is used. The output beam diameter ($1/e^2$) is 1.3 mm with a divergence of less than 1 mrad. Since the signal generated is a direct function of the laser power, changes in laser power would result in a signal being detected by the signal preamplifier. The 124B's laser output stability also led to its choice, with output power fluctuations that are guaranteed to be less than 0.3% rms.

4.1.2 Deflection System

To obtain the desired signal, the capacitive detector element must be located close to the illuminating spot. If a large area of the sample is to be scanned, this means that either the detector moves synchronously with the laser beam over a stationary sample, or the sample is translated under a stationary beam and detector. Since we would like to perform the scan in a reasonable amount of time,

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[81] W. R. Sooy, *Lasers and Optics-An Overview,* Proc. Soc. Photo-Opt. Instrum. Eng. 69 (1975), 3-9.

[82] V. J. Fowler, *Laser Scanning Techniques.* Proc. Soc. Photo-Opt. Instrum. Eng. 53 (1974), 30-43.

the spot scanning velocity must be high. Due to the finite mass of the sample and transport, they cannot be accelerated at high rates without an elaborate mechanical system. It is also a mechanical nightmare to move the detector in proper synchronization with the laser spot. For these reasons, the system chosen is very similar to that which is used in primary pattern generators[83] and other very high accuracy applications. With this technique it is possible to scan large areas at high scan rates with proper beam/detector registration. The high speed is obtained by using a one dimensional scanning element in the optical path to generate a line scan. To achieve the second dimension of the raster scan, the sample is translated orthogonally to the scan line. The beam deflector in the optical path now governs the spot velocity and the linear transport speed determines the resolution or number of scan lines per image.

4.1.3 Lens System

Now that the scan format has been established, a lens must be chosen to produce a focused spot across the desired field. The field of view in this case is the sample which has a very flat surface. This eliminates a simple converging lens which provides a curved field of focus. However if a very long focal length lens is used, exhibiting a long depth of focus, it is possible to deflect it by a small angle

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[83] M. J. Cowan, D. R. Herrott, A. M. Johnson, A. Zacharias, *The Primary Pattern Generator-Optical Design*, Bell Syst. Tech. J. 49 (Nov. 1970), 2033-41.

and maintain the desired degree of focus. In our case the focal length required would be a number of meters making its implementation impractical.

In order to get the desired flat field focussing characteristics, the scanning component must be placed before the scan lens.[84] . For optimum resolution, a large input beam is required for the scan lens. Since the scanning element must deflect a non-converging beam, this specifies a layout of the optical path as shown in Figure 7 on page 52. The scan lens provided (Figure 8 on page 53) is a four element f/16 nontelecentric flat field lens with a 600 mm focal length (F). It is corrected for Fθ distortion[85] which ensures that the spot position on the focal plane is directly proportional to θ rather than tan θ.

For minimum power loss in the deflection system, the scan lens will be illuminated with a Gaussian underfill[86] beam profile. This will yield a diffraction limited spot diameter (d) of[87]

$$d = \frac{2.54\lambda F}{D_s} \qquad [4.1]$$

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[84] L. Beiser, *Laser Scanning Systems* in Laser Applications. Vol. 2. Ed. M. Ross. New York: Academic Press, 1974.

[85] P. M. Emmel, *System Design Considerations for Laser Scanning.* Proc. Soc. Photo-Opt. Instrum. Eng. **222** (1980), 2-14.

[86] I. H. Mallender, *Resolution Intensity and Power in Diffraction Limited Laser Systems.* Proc. Soc. Photo-Opt. Instrum Eng. **84** (1976), 132-37.

[87] R. E. Hopkins, M. J. Buzawa, *Optics for Laser Scanning.* Opt. Eng. **15** (Mar.-Apr. 1976), 90-94.

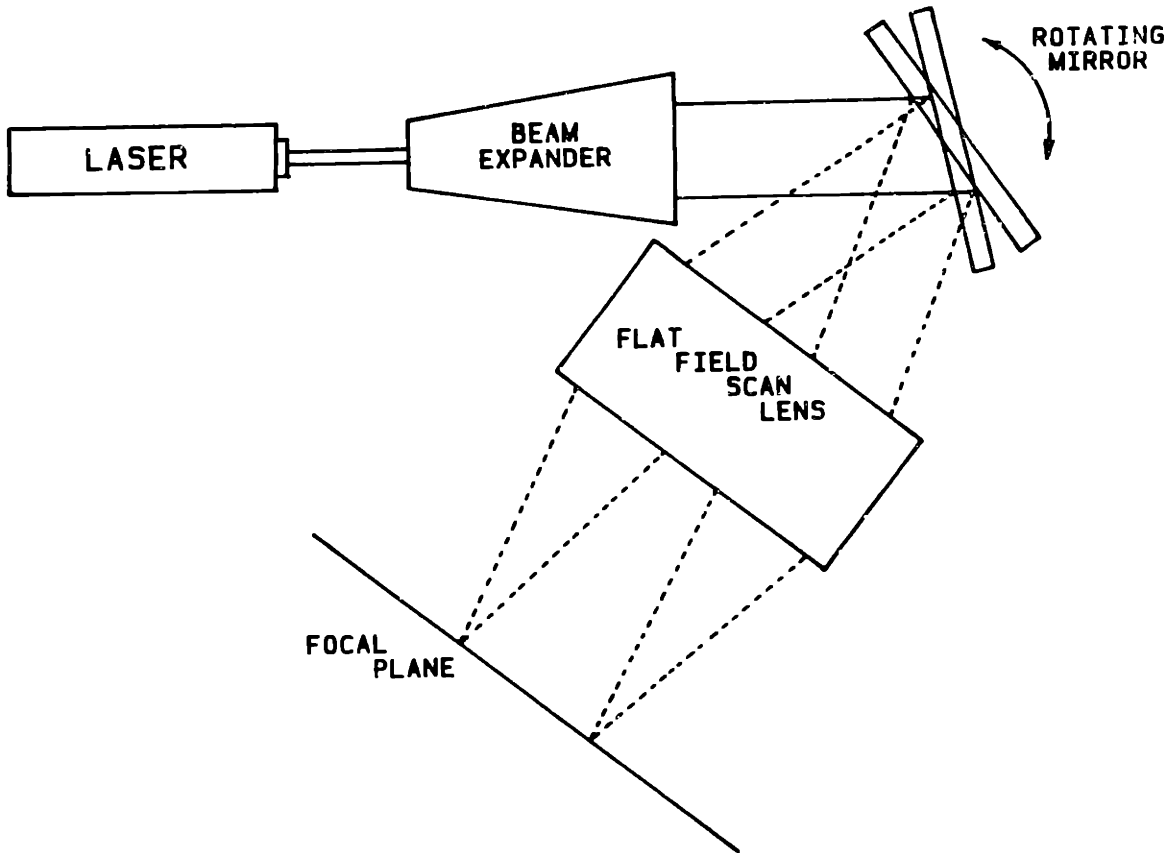

Figure 7. Flat Field Preobjective Scanning Arrangement

where the aperture diameter is defined by the scan mirror diameter (D_s). For operation with the HeNe laser this yields a diffraction limited spot size of

$$d = \frac{2.54 \times 0.6328 \times 600}{32} = 30\mu m \qquad [4.2]$$

In order to obtain a beam diameter large enough to fill the scan mirror, a beam expander must be used. The beam diameter at the laser is specified as 1.3 mm, so a 25× beam expander is needed to raise the beam diameter to 33 mm. A spatial

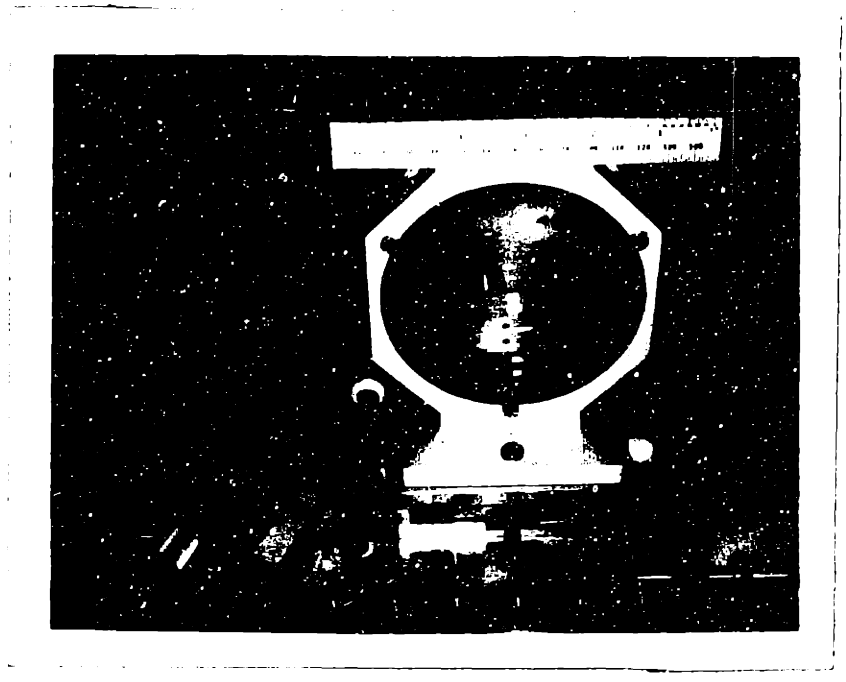

Figure 8. Flat Field Scanning Lens

filter (Figure 9 on page 54) should be used in conjunction with the beam expander as this will provide a smooth Gaussian expanded beam output, and the beam perturbations (localized, scattered changes of intensity in the output beam) will be eliminated. When properly aligned, the spatial filter should optimize the final spot energy, reducing the spot size to the theoretical minimum.

Now that the lens system has been specified, the scanning element must be chosen. Popular, compact scanning elements are acousto-optic and totally internally reflected (TIR) spatial light modulators.[88] These are widely used as

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[88] R. A. Sprague, J. C. Urbach, T. S. Fisli, *Advances in Laser and E-O Printing Technology.* Laser Focus. 19 (Oct. 1983), 101-08.

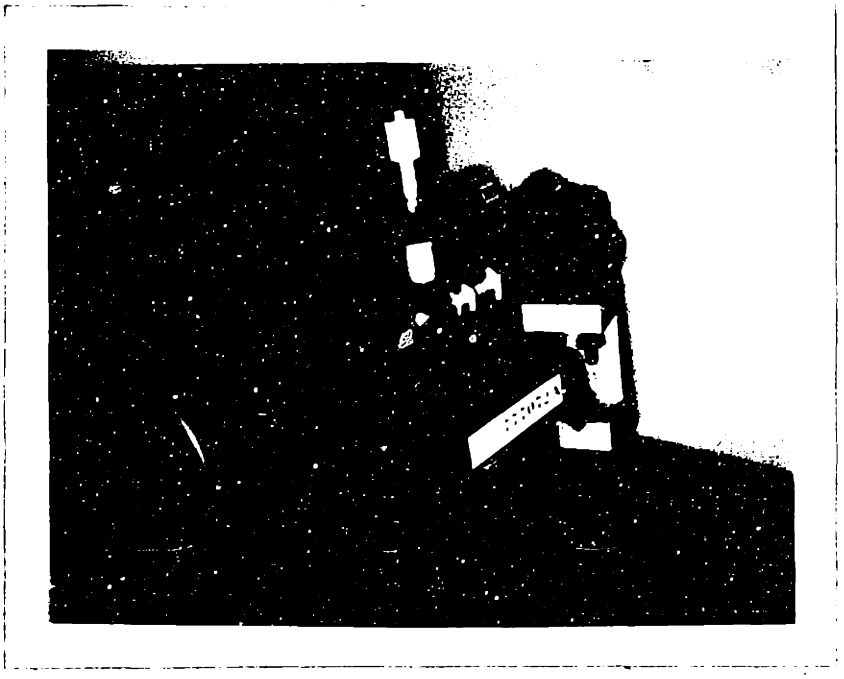

Figure 9. Spatial Filter Assembly

small diameter beam deflectors but suffer from low optical efficiencies.[89] The choice of scan lens eliminates these devices since the scan element must be able to deflect a beam with a diameter of at least 32 mm. This leads to the use of a mirror which is mounted on some type of electromechanical device. There are three major types of electromechanical scanners available.[90] Taut band and torsion rod units constitute the self resonant class. These operate at a fixed frequency set by the natural spring constants and the inertia of the moving elements, including the

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[89] I. Gorog, J. D. Knox, D. V. Goedertier, *A Television-Rate Scanner-I. General Considerations,* RCA Rev. **33** (Dec 1972), 623-28.

[90] S. Reich, *The Use of Electro-Mechanical Mirror Scanning Devices,* Proc. Soc. Photo-Opt. Instrum. Eng. **84** (1976), 47-56.

mirror. Power requirements are low, in the 200 mW range, and can accommodate large mirrors with approximately 20° peak to peak excursions. The position versus time waveform is sinusoidal and, depending on mirror size, can operate between 5 hz and 10 Khz.

The variable frequency devices include piezoelectric and galvanometer scanners. Piezoelectric devices can operate from DC - 45 Khz but only with angles less than 2° peak to peak. Moving iron galvanometer scanners (Figure 10 on page 56) are very versatile devices, capable of a large range of operating modes. Rotation is achieved by varying the current in an electromagnet which is rotated in a fixed magnetic field. The armature is supported on a shaft with precision bearings and by a torsional spring which assists with mechanical damping. Electrical damping can also be employed to improve their bandwidth. Except when operating at their natural frequency, power requirements are orders of magnitude more than self resonant types, with typical values of 5 - 20 W.

Rotating polygons offer the ultimate combinations of scan speed, duty cycle and linearity. These units can be operated from DC to 1,000,000 rpm (air turbine driven) with scan angles up to 180°. Their deflection waveform is a linear ramp whose frequency is controllable by the motor speed. Power requirements for the synchronous motor drive is also high due to the relatively large armature and mirror mass being driven.

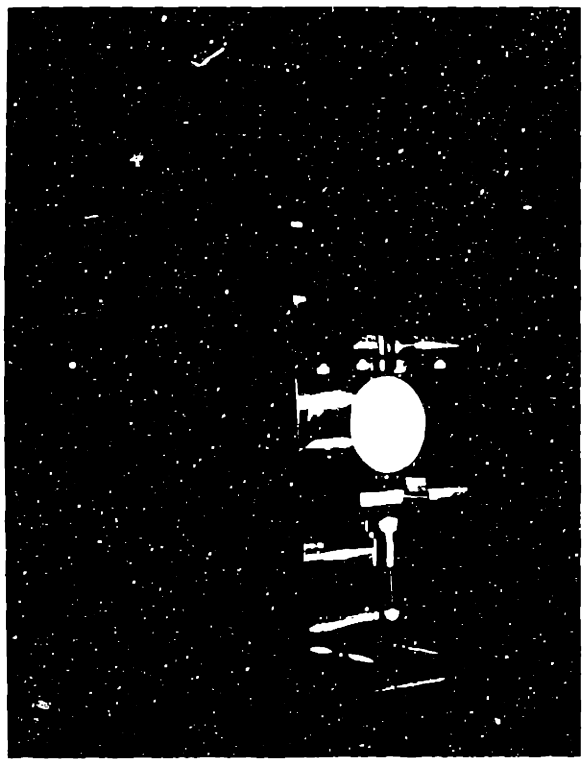

Figure 10. Moving Iron Galvanometer Scanner

Due to the versatility and wide availability of the galvanometer scanners, they were chosen over the rotating polygon scanners. However, if a fixed scan rate is desired and settled upon, a rotating polygon should replace the galvanometer for enhanced performance.

4.1.4 Layout, Alignment, and Performance

The simplified tangential plane view of the optical system is shown in Figure 11 on page 57 and the layout in Figure 12 on page 58. The beam origi-

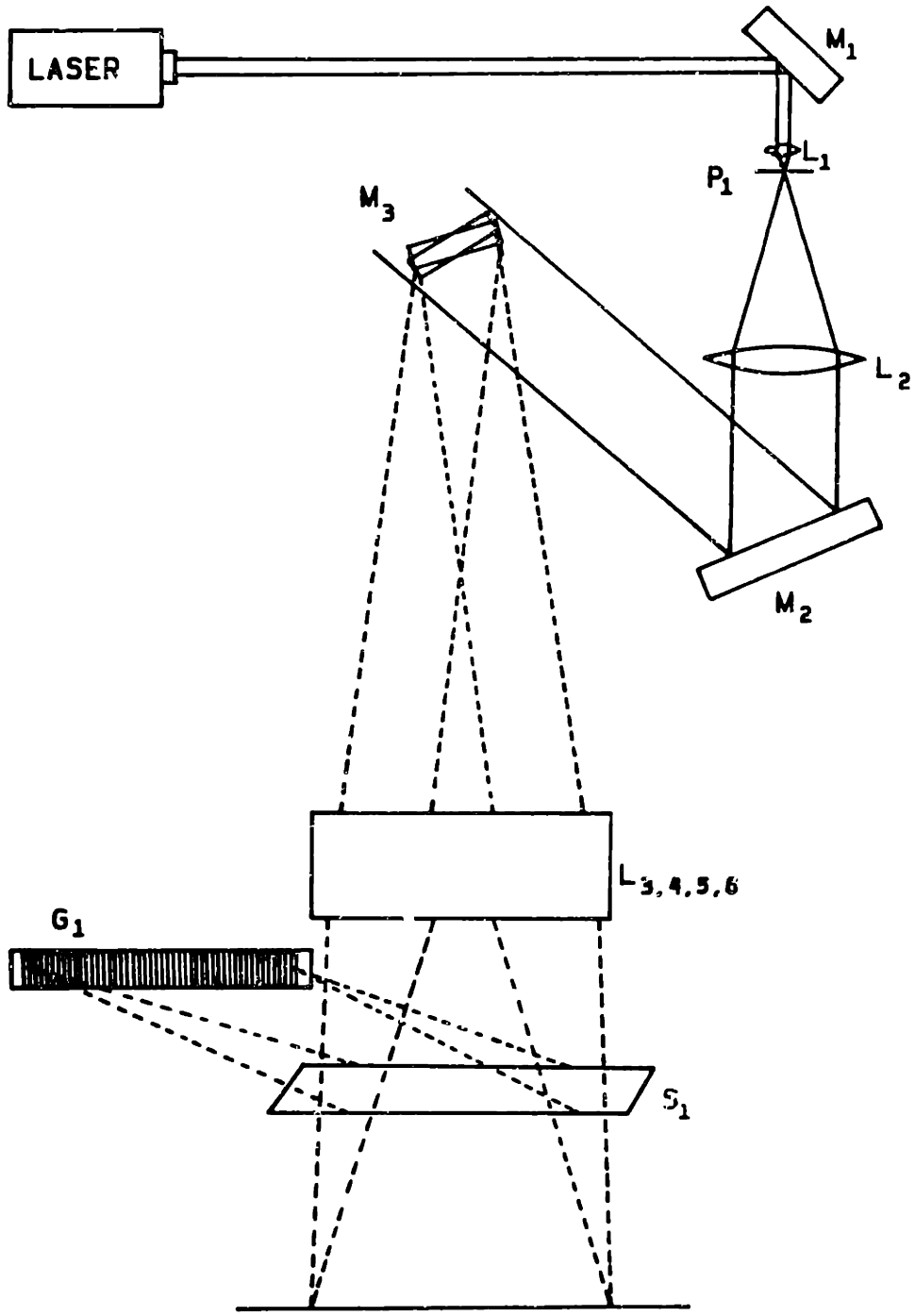

Figure 11. Simplified Tangential Plane Optics

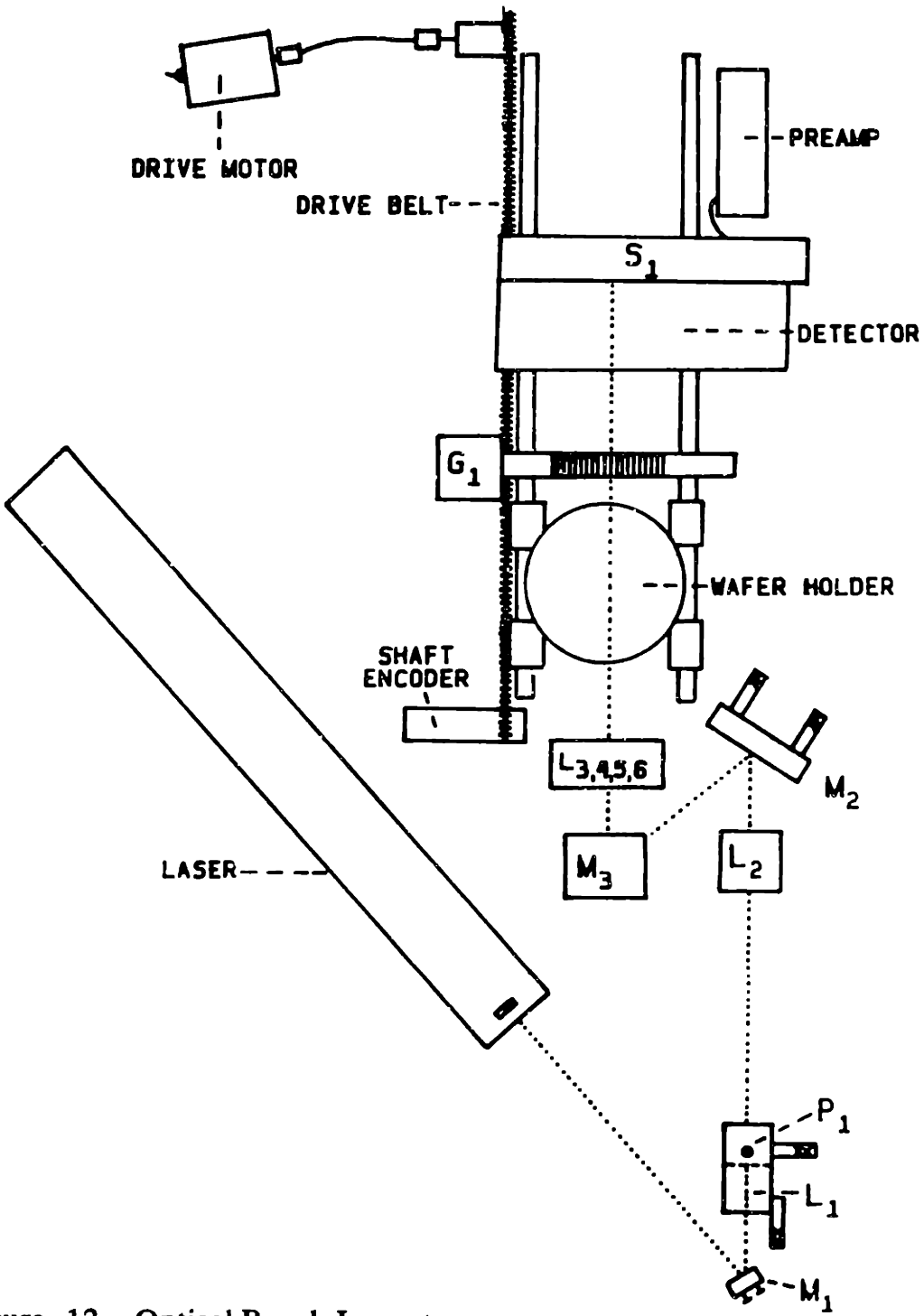

Figure 12. Optical Bench Layout

nates at the laser with a power of 20 mW and a beam diameter of 1.3 mm. It is then deflected off of M_1 into the microscope objective, L_1. The adjustments on M_1 position the beam through the entire system to check center line alignment. After passing through the 25 × objective, the beam is threaded through a 25 μm pinhole (P_1) which serves as a spatial filter. The diverging beam is then recollimated by passing through the collimating lens L_2. The $1/e^2$ beam diameter is now 33 mm. This beam is positioned onto the scanning mirror, M_3, with the adjustments on M_2. The diameter of the scanning mirror truncates the scan lens input beam to the desired 32 mm. After passing through the scan lens ($L_3 - L_6$) the converging beam is projected onto the sample. A beam splitter, (S_1) is placed between the scan lens and the focal plane to provide illumination for the position grating (G_1) as later described in section 5.4.1.

4.2 MECHANICAL SYSTEM

4.2.1 Isolation

In order for the optical system to remain stable and in alignment, it must be built on a isolated optical bench. This provides the necessary mechanical damping and a flat reference surface for mounting of the optical components. The optical bench itself has a stainless steel top surface with an aluminum honeycomb interior. Besides providing isolation from external vibrations, the honeycomb isolates one portion of the bench from another. This is very important since the galvanometer generates a substantial amount of local acoustic vibration which

must be damped out by the time it reaches the detector. The detector itself must be rigidly mounted due to the tight tolerances required between the detector and sample.

4.2.2 Wafer Transport

For the scanning system chosen, the wafer must be translated under the stationary detector and laser beam projection to provide area coverage of the sample. There are a number of constraints governing the design and implementation of the wafer transport. The first of which is linearity of travel. A stepper motor driven stage would be the best choice in this case but the time required for the stage to reach and settle on a new location is on the order of 5 ms. For a high resolution scan having thousands of scan lines this would add an unreasonable amount of time to the overall scanning interval. Therefore, instead of the transport traveling in discrete steps, It is more desirable for it to move at a constant rate. A tachometer controlled DC motor or a synchronous (constant speed) AC motor can be used as a constant rate driver. The DC motor should be of the brushless type in order to minimize the radiated electrical noise output. Since the AC motor's speed regulation is inherent in its design, and the DC motor must use and external controller, an AC motor was chosen for this application.

The actual transport as shown in Figure 13 on page 61 consists of a quartz sample holder mounted on a supporting plate. Ball bearing blocks are mounted to the plate which is then run horizontally on a parallel pair of precision cylindrical

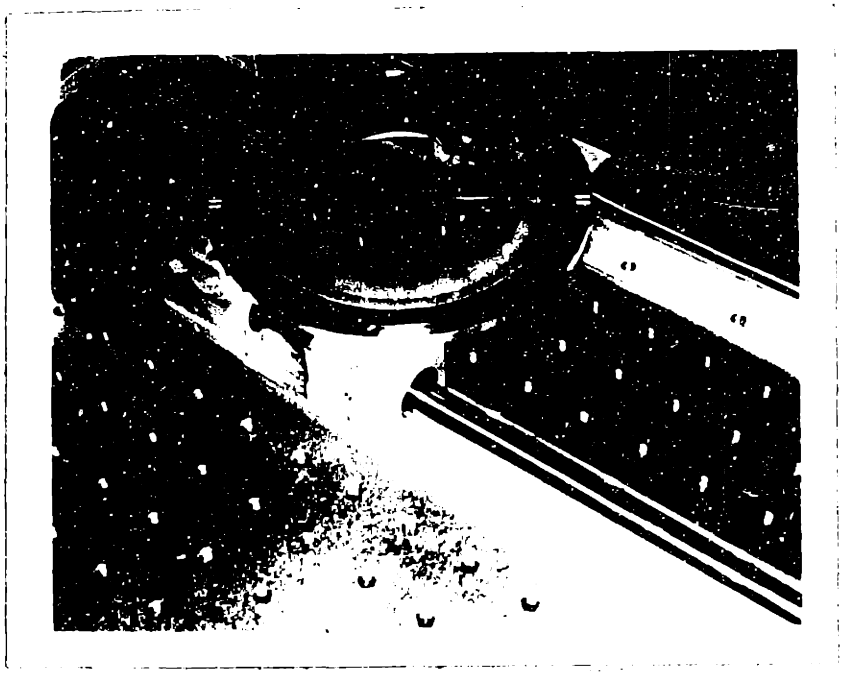

Figure 13. Wafer Transport

rails. This scheme was chosen to eliminate any extraneous motion along the z axis[91] which would cause errors to be produced in the capacitive detector.

This stage is driven with a belt drive which is shaft driven with the AC motor. The belt used is a polyurethane timing belt with a Dacron core which has less than 0.5% elongation for tensions under 25 Kg. In our application, the only backlash involved in the drive system is in the gear reduction box in the motor itself. Under normal unidirectional operation, there is no measurable slippage at all.

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[91] The bearings used are Thomson Super Ball Bushing pillow blocks which have a runout tolerance of ± 10 μm.

5.0 ELECTRONICS

5.1 SIGNAL PATH

5.1.1 Capacitive Detector

Techniques similar to scanning surface photovoltage claim to be non-contact when in reality, a direct electrical contact is being made to the sample under test. Usually the sample is held with a metallic vacuum chuck or immersed in an electrolyte solution[92] to provide the necessary return electrical path through the substrate. In the technique to be discussed here, the wafer is kept completely electrically isolated and no contact is made to the sample in any manner. The sample holder is provided only for mechanical support and consists of a quartz plate mounted on the wafer transport system.

As discussed earlier, the parameter to be measured is the local change in surface potential. This charge imbalance is detected using a differential capacitor arrangement as shown in Figure 14 on page 63. The actual signal detected is a displacement current in two air gap parallel plate capacitors which results from changes in the local surface charge around the laser spot and the average surface charge far from the laser spot. The lateral distance separating the two capacitors must be greater than the effective diffusion length as derived in section 3.1.2. The

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[92] D. L. Lile, N. M. Davis, *Semiconductor Profiling Using an Optical Probe.* Solid-State Electron. **18** (1975), 699-704.

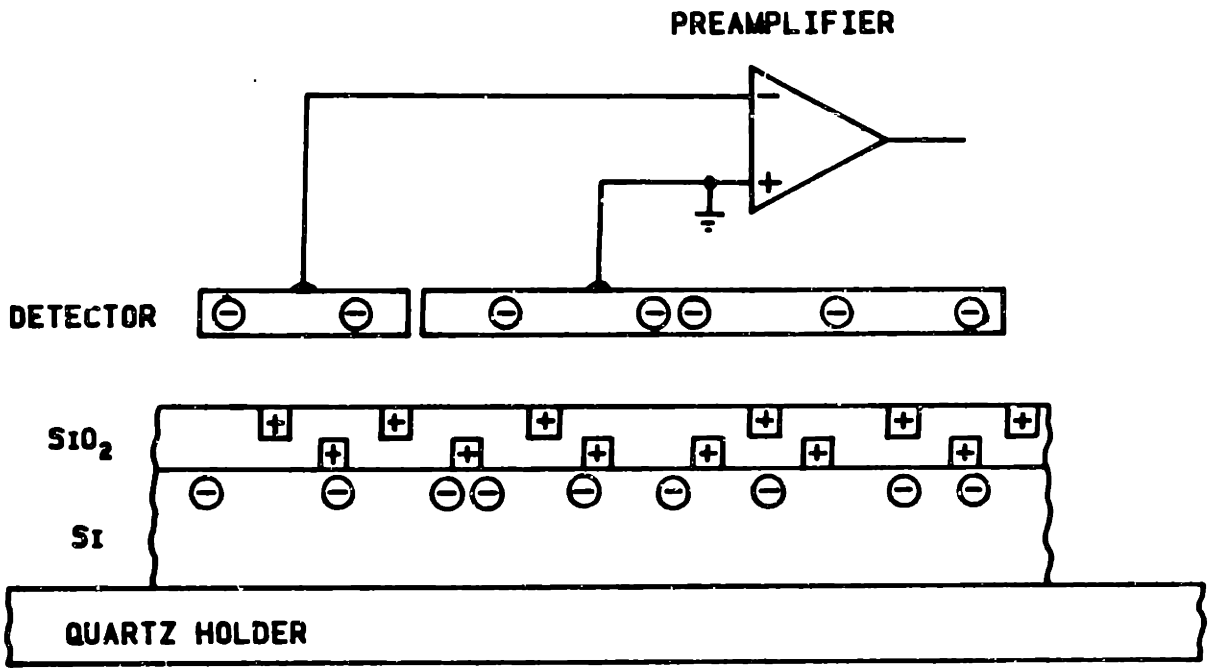

Figure 14. Capacitive Detector

capacitors are formed between two metallic conductors and the sample with an air gap of nominally 100 μm separating them. Since this air gap has a direct effect on the signal measured, the sample must be held as steady as possible to eliminate false signals. The detector is very sensitive to acoustical vibrations as well. Whispers many meters from the detector are readily picked up by the preamp. Attempting to hold the detector spacing constant in practice is very hard to achieve due to changes in sample thickness, warpage of the wafer, and transport system runout. If the signal frequency spectrum is high compared to these mechanical disturbances, the signal can be filtered to remove all of the low

frequency components while retaining the signals of interest. The detector is also mounted in such a way that the preamp can be positioned as close as possible.

5.1.2 Signal Analysis

In order to properly specify the preamplifier electronics, it becomes necessary to determine the frequency spectrum of the signals of interest. It has already been established that the low frequency components were to be filtered away so this implies the use of a differentiator or high pass filter topology. Since all realizable differentiators are limited in their high frequency performance, it is desirable to determine the highest frequency that is likely to be encountered.

The frequency spectrum is directly related to the rise time of the signals observed. In this case, the detected signal is excited by a gaussian spot traversing across a point or line defect, producing a gaussian shaped output pulse. The difference between the 10% and 90% intensity levels can now be determined as a function of the $1/e^2$ beam diameter.

x_r = Rise time distance

d = $1/e^2$ Spot diameter = 30 μm[93]

t_r = Rise time

v = Surface scan velocity = 80 m/s

f_h = High frequency cutoff point

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[93] See Section 4.1.3

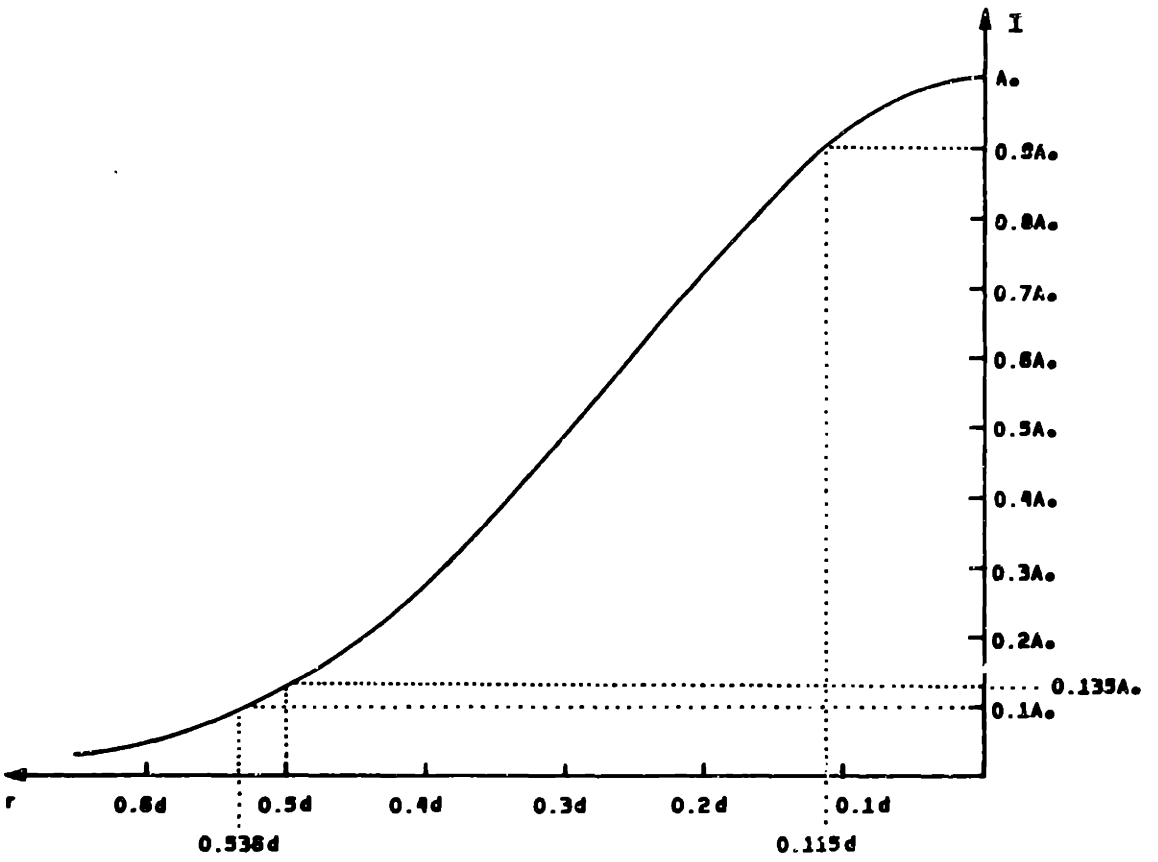


Figure 15. Gaussian Output Pulse $I = A_0 e^{-8r^2/d^2}$

$$x_r = (.536 - .115)d = 0.421d \qquad [5.1]$$

$$t_r = \frac{x_r}{v} \qquad [5.2]$$

$$f_h = \frac{0.35}{t_r} = \frac{0.35v}{x_r} = \frac{0.35(80)}{0.421(30\mu)} = 2.2 \text{ Mhz} \qquad [5.3]$$

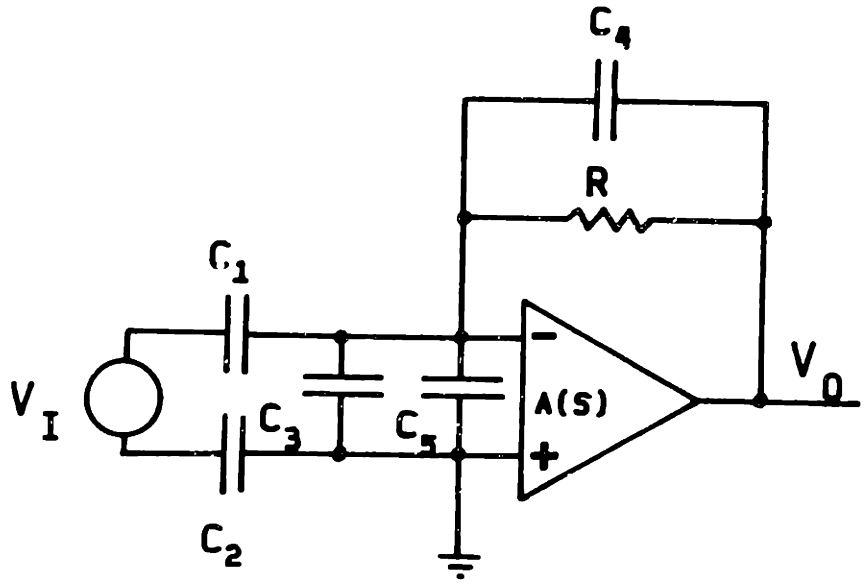
The preamp must now have its high frequency breakpoint above 2.2 Mhz for optimum operation.

5.1.3 Preamp Design / Analysis

The preamp is the most important section of the detection electronics. The amplifier itself must be a current to voltage converter which may be implemented in two basic topologies. The first method is to return the input signal through a large resistor to ground and follow the potential across it with a high input impedance buffer. The second topology is to feed the input directly into the inverting terminal of an operational amplifier which is operating at a virtual ground (low impedance). The first method is plagued with noise problems due to the inherent pickup by the high impedance buffer. For these noise reasons, the virtual ground topology was chosen. The feedback resistor was set to 10 MΩ for a closed loop gain of 10 V/μA.

In order to determine the closed loop transfer function of the preamp it becomes necessary to include the stray capacitances in the circuit as the very large resistor values generate parasitic poles below the open loop crossover frequency of the amplifier, degrading its performance. The circuit in Figure 16 on page 67 will be used to model the behavior of the preamplifier.

The two detector elements described in Figure 14 on page 63 correspond to the two capacitors C_1 and C_2 . The smaller of the two, C_1 , has an area,(A), of $1.55 \times 10^{-4}\,m^2$ and the large ground plane, C_2 , has an area of $4.12 \times 10^{-2}\,m^2$. The values of C_1 and C_2 have been calculated using the formula



Element	Value	Description
C_1	13.7 pF	Detector to sample capacitance
C_2	3646 pF	Ground plane to sample capacitance
C_3	2.0 pF	Amplifier input capacitance
C_4	0.25 pF	Stray capacitance
C_5	23.0 pF	Stray capacitance
R	10 MΩ	Feedback resistor

Figure 16. Preamplifier Model

$$C = A\frac{\varepsilon_0}{h} \qquad [5.4]$$

where the spacing, h, is 100 μm. This yields the values tabulated in Figure 16. The previous circuit model can now be simplified to the form as shown in Figure 17 on page 68.

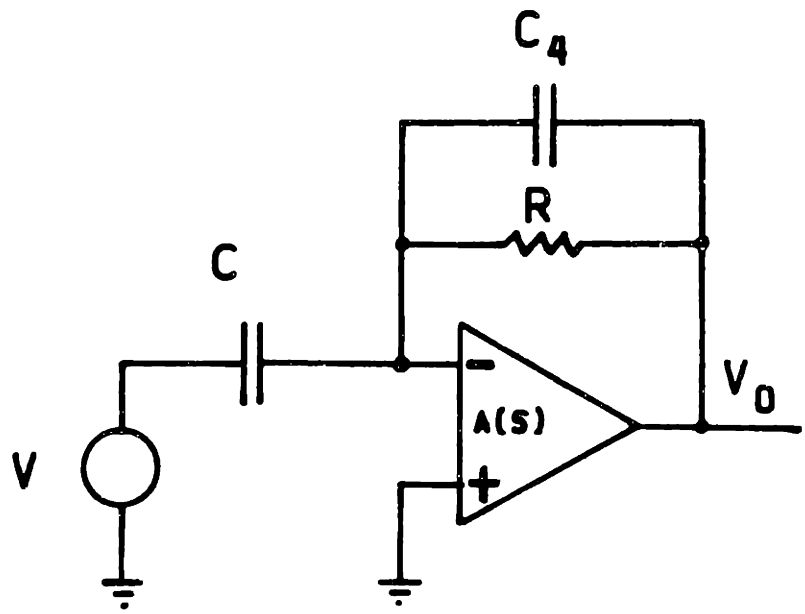


Figure 17. Simplified Preamplifier Model

Where the source term is now,

$$V = V_I \left[\frac{\frac{1}{C_3 + C_5}}{\frac{1}{C_3 + C_5} + \frac{1}{C_2} + \frac{1}{C_1}} \right] = k_6 V_I = 0.353 V_I \qquad [5.5]$$

The effective source capacitance is now,

$$C = C_3 + C_5 + \frac{C_1 C_2}{C_1 + C_2} = 38.6 \text{ pF} \qquad [5.6]$$

The closed loop gain expression now becomes,

$$\frac{V_O}{V} = \frac{-a(s)\dfrac{R}{RC_4s+1}}{\dfrac{1}{Cs}(1+a(s)) + \dfrac{R}{RC_4s+1}}$$

$$\frac{V_O}{V} = \frac{-RCsa(s)}{(RC_4s+1)(a(s)+1)+RCs} \qquad [5.7]$$

Substituting the open loop gain expression for the op amp,

$$a(s) = \frac{a_0}{\left(1+\frac{s}{s_1}\right)\left(1+\frac{s}{s_2}\right)} \qquad [5.8]$$

$$\frac{V_O}{V} = \frac{-RCsa_0}{s^3\frac{R}{s_1s_2}(C+C_4) + s^2\left[\frac{1}{s_1s_2} + R\left(\frac{1}{s_1}+\frac{1}{s_2}\right)(C+C_4)\right] + s\left[RC_4(a_0+1)+\frac{1}{s_1}+\frac{1}{s_2}+RC\right] + a_0 + 1}$$

This is then simplified to

$$\frac{V_O}{V} = \frac{k_5s}{s^3k_1 + s^2k_2 + sk_3 + k_4} \qquad [5.9]$$

Where

$$k_1 = \frac{R}{s_1s_2}(C+C_4) = 3.09 \times 10^{-16}$$

$$k_2 = \frac{1}{s_1s_2} + R\left(\frac{1}{s_1}+\frac{1}{s_2}\right)(C+C_4) = 3.09 \times 10^{-8}$$

$$k_3 = RC_4(a_0+1) + \frac{1}{s_1} + \frac{1}{s_2} + RC = 0.5305$$

$$k_4 = a_0 + 1 = 212001$$

$$k_5 = -RCa_0 = -81.83$$

The magnitude of the transfer function versus frequency[94] , can now be evaluated as

$$\left|\frac{V_O}{V_I}\right| = \frac{k_6 k_5 \omega}{\sqrt{\left(k_4 - \omega^2 k_2\right)^2 + \left(\omega k_3 - \omega^3 k_1\right)^2}} \qquad [5.10]$$

The frequency response of the preamplifier was also measured and plotted with the calculated response in Figure 18.

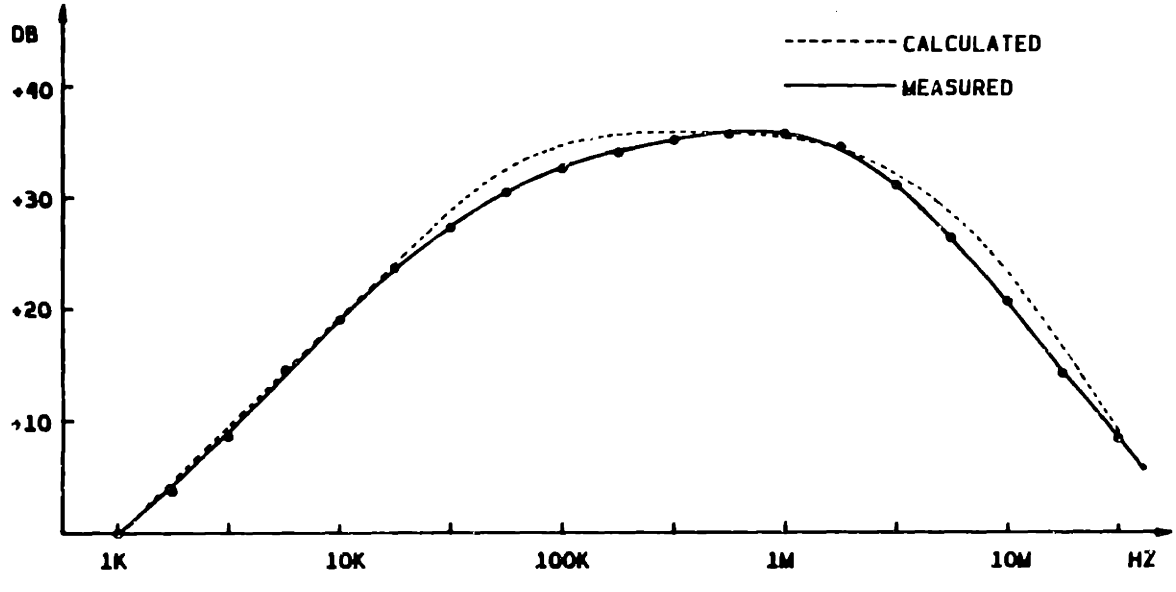


Figure 18. Preamplifier Frequency Response

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[94] $\omega = 2\pi f$

The preamp was constructed on a separate printed circuit board positioned close to the detector. A teflon printed circuit board and a ground plane were used to reduce leakage currents and noise susceptibility. For further electromagnetic and radio frequency (RF) interference rejection, the preamplifier board was placed in a RF shielded box as shown in Figure 19. The full schematic is illustrated in Appendix D.1.

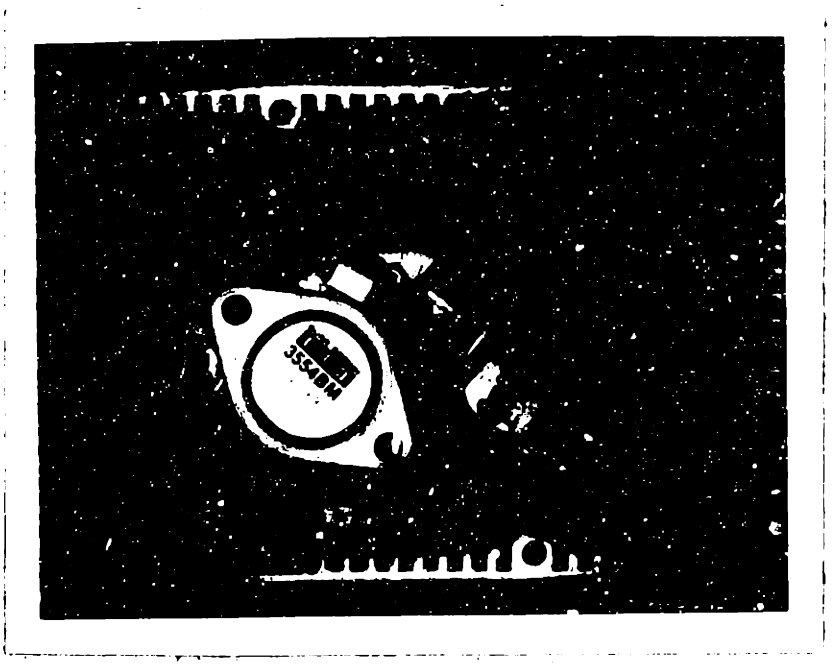

Figure 19. Constructed Preamplifier

5.1.4 Signal Amplifier Design

Figure 20 on page 72 outlines the signal path of the signal amplifier. the signal amplifier performs the functions of amplification, filtering, and video

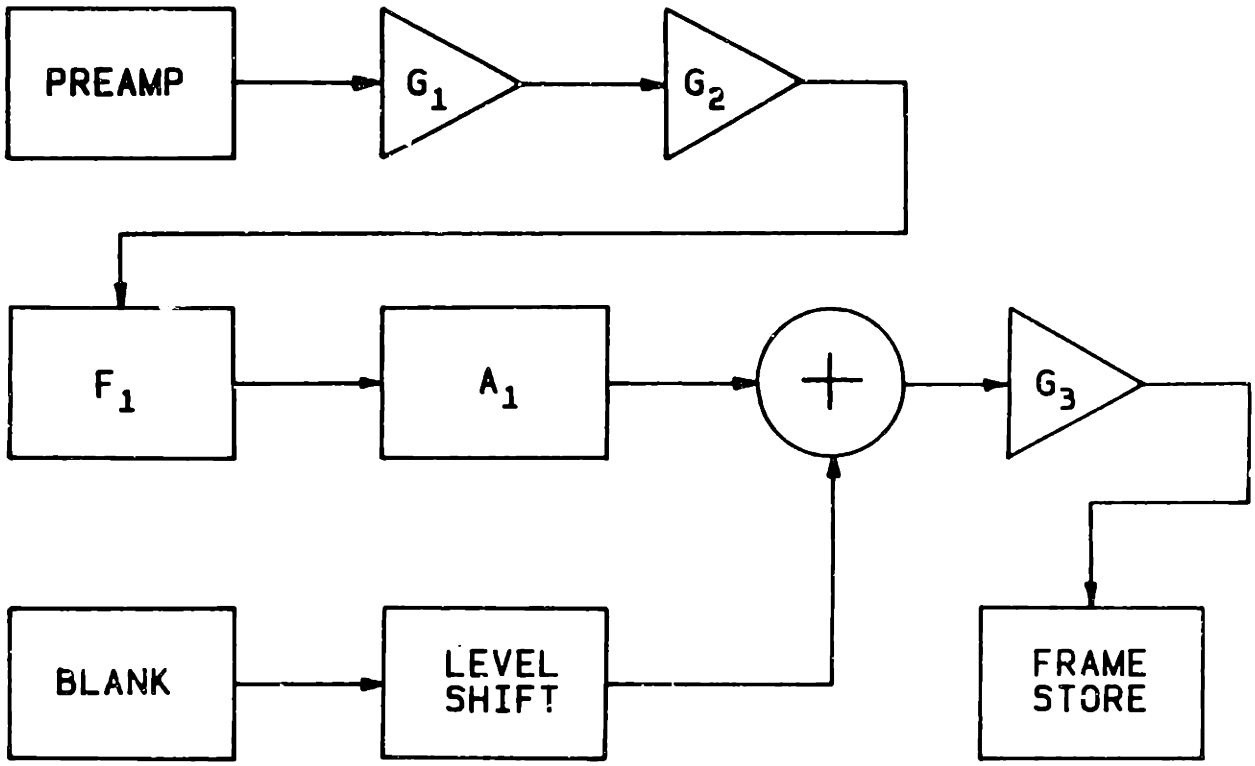

Figure 20. Signal Amplifier Block Diagram

display interfacing. The full schematic for this amplifier can be found in Appendix C.1.

The input stage must interface with the preamplifier which provides a low impedance drive source transmitted via RG58A/U coaxial cable. For accurate frequency response, the input is terminated into 50Ω which is the characteristic impedance of the transmission line. The first two gain stages are identical AC coupled video amplifiers operating at a gain of 16.3 db each over a 3 db bandwidth of 28 hz - 40 Mhz. Each of these stages consists of current mode (Norton) operational amplifiers capable of gain bandwidth products in excess of 400 Mhz.

Following the main gain stage is a passive high pass filter. In order to optimize the degree of filtering, the low frequency breakpoint is variable in steps between 1 Khz and 1 Mhz. It is desirable to have this adjustment in order to vary the sharpness of the displayed image.

A variable attenuator is also included in the gain path and acts as a gain control. This control is in calibrated steps instead of a variable control due to the problems introduced by the stray inductances of most potentiometers.

In order to interface correctly with the frame store unit, the intensity modulated signal must be turned off or blanked during the interval that the raster generators are retracing across the screen. This is accomplished by adding a pedestal (Figure 21 on page 74) to the signal which translates the video signal through the black / white threshold, effectively blanking the display.

A level control is included which varies the height of the blanking pedestal, which in turn, controls the intensity level of the display. The final output stage provides an additional gain of 15.6 db with a 3db bandwidth of DC to 30 Mhz. The drive capability of the video output is ± 10 V into a terminated 50Ω cable with slew rates in excess of 1000 V/μs.

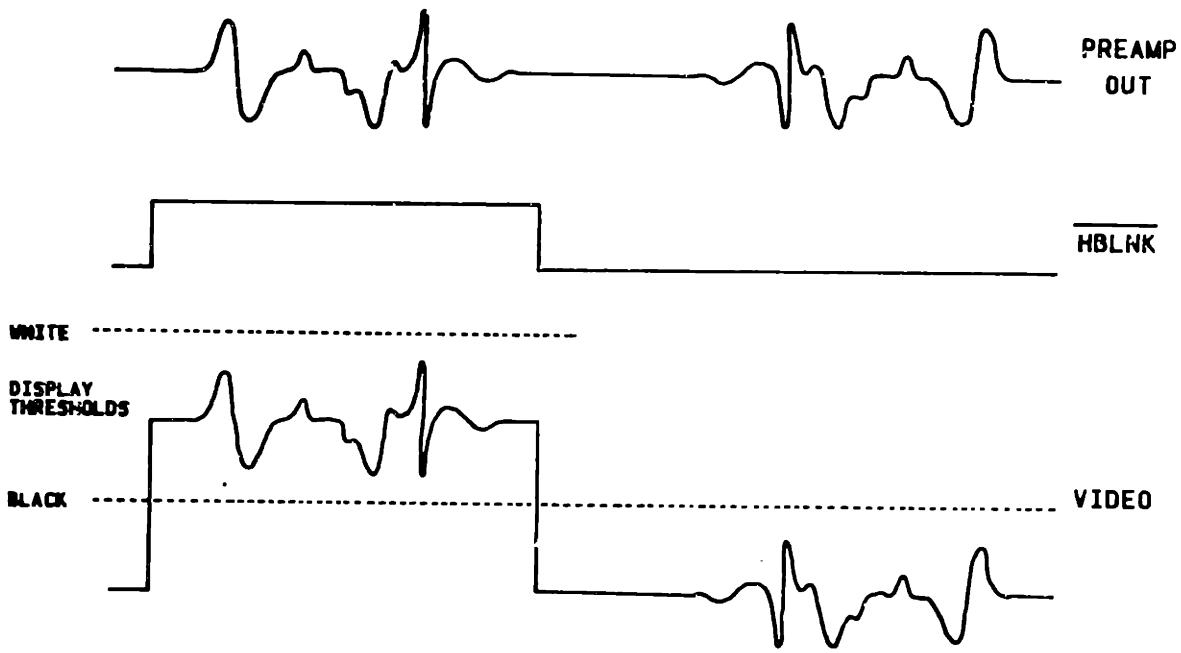

Figure 21. Video Blanking Waveforms

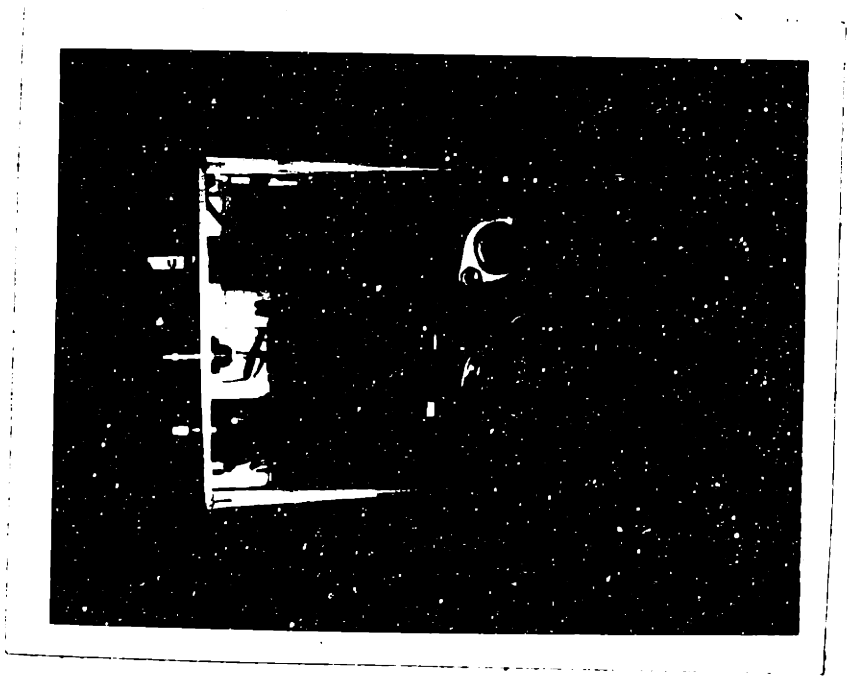

Figure 22. Top View of Signal Amplifier Circuit Board

The signal amplifier was also built on a printed circuit board and mounted in a modular expansion unit compatible with Tektronix TM500 series power modules. These power modules provide unregulated DC power as well as an external cabinet. The power supply regulator was placed in the same module as the signal amplifier and can be seen in the top view of the circuit board as pictured in Figure 22 on page 74.

5.1.5 System Performance

It now becomes necessary to evaluate the overall performance of the electronics system. If an oscilloscope such as a Tektronix 606B is used as the recording CRT, the display bandwidth is DC - 5 Mhz (some of the other display techniques can be as high as 27 Mhz).[95] In order to utilize the display up to its abilities, the overall bandwidth of the remaining electronics should be much greater. The measured and calculated signal amplifier frequency response as depicted in Figure 23 on page 76 is broader than either the preamp (Figure 18 on page 70) or display so that its contribution to the overall response can be modelled just as a gain factor. The dominant poles in the system are the 2 poles at 5 Mhz, one from the preamp and one from the display. The other poles reside at 30 Mhz and 60 Mhz from the signal amplifier's output and gain stages respectively. Determining the system upper frequency breakpoint from these figures places the cutoff at 2.3 Mhz, which is just above the optimum as derived in section 5.1.2.

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[95] Hughes 639H Scan Converter Memory with a Tektronix 634 High Resolution Monitor.

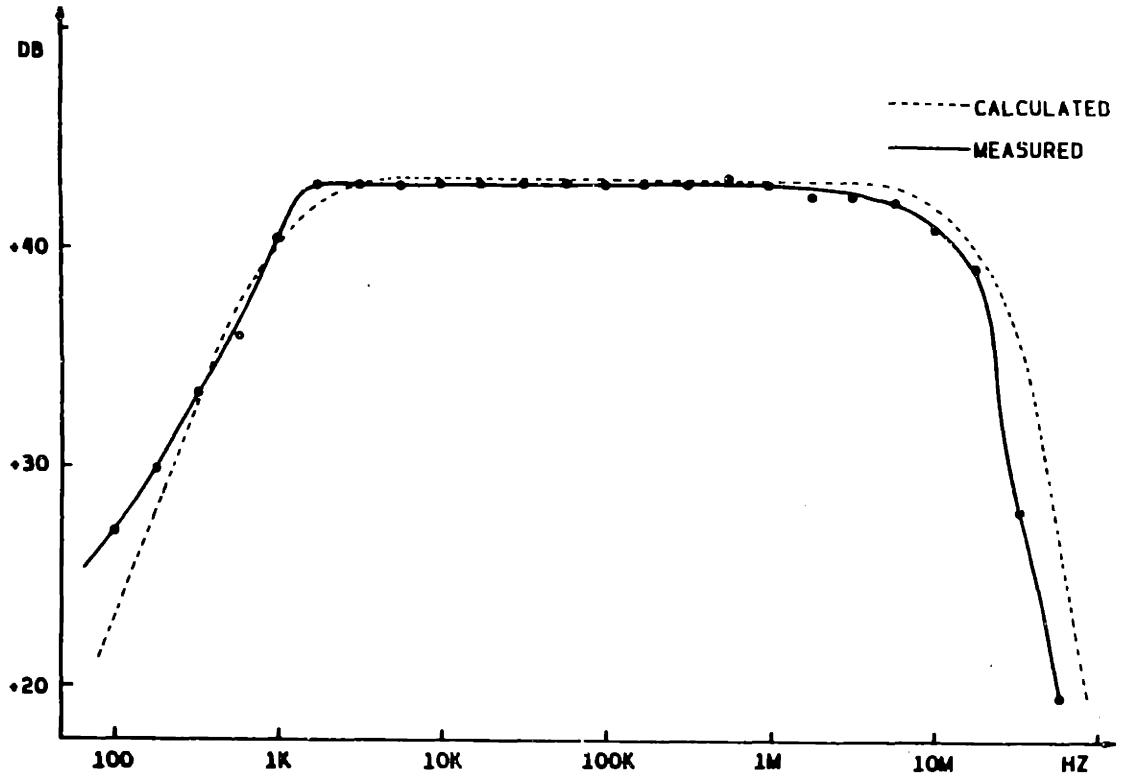

Figure 23. Signal Amplifier Frequency Response

The minimum signal level required for the display to modulate a perceivable amount is approximately 10 mV. This corresponds to a change in surface potential of 1 μV or a 5 pA displacement current in the capacitive detector.

5.2 FRAME STORE

5.2.1 Alternatives

Once the signal has been detected and amplified it must be presented in some manner for further analysis. There are a number of ways to display sequentially

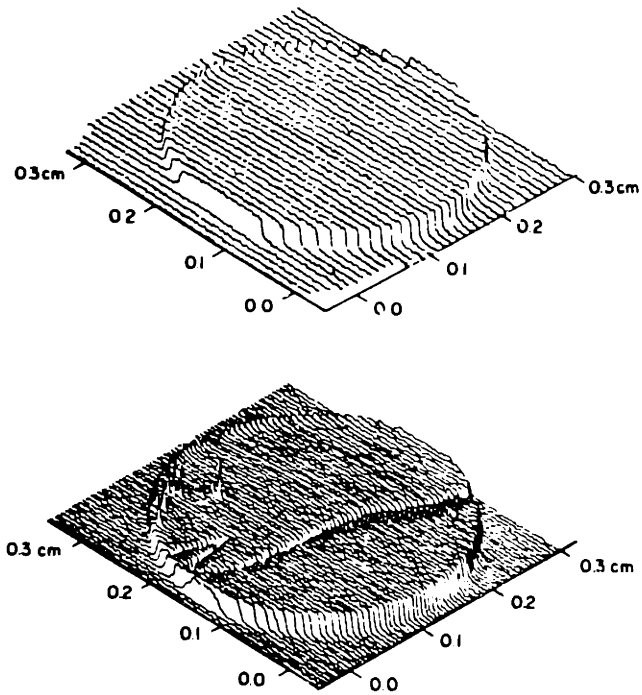

Figure 24. Chart Recorder Output Samples

or raster scanned data. The simplest of these is a chart recorder. This mode of data collection is precise but is useful only with very low data rates. The next step is to raster scan the sample and display successive "strip charts" as shown in Figure 24. This method gives the impression of a third dimension, depth, which aids in quick interpretation while using only a two axis recording instrument. This technique is limited in the number of scan lines since higher line densities degrade the image. The preferred technique for displaying a large volume of data at high rates is through the use of raster scanned intensity modulated CRT displays. Using this technique the signal level determines the intensity of each pixel. The

display media can be a number of different formats which are described in the next section.

5.2.2 Intensity Modulating Schemes

The most straightforward method of displaying intensity modulated data is to use a cathode ray tube (CRT) which is being refreshed at television line rates (60 frames per second). This implies that the sample scanning rate has to be just as fast. Since this is not practical in our case, a method with a longer storage time is needed.

A CRT containing a long persistence phosphor or a storage oscilloscope can be used to provide a stable display which does not need to be refreshed. These techniques suffer from two basic problems. The resolution of a standard storage oscilloscope is only a few hundred lines per frame whereas video monitors or recording CRTs reach as high as 1500 lines per frame. Another problem with bistable storage oscilloscopes is their lack of dynamic range or gray scale. These oscilloscopes were meant more for displaying a binary image rather than a true gray scale.

To get around the problems of both resolution and viewing time, a high resolution CRT can be mated with a photographic camera to produce a permanent photograph of the display. In this mode a time exposure photograph is taken of the CRT while the screen is being deflected at a low rate. This produces displays with up to 2000 lines per frame with excellent gray scale characteristics with are

now limited by the film. All of the images presented later in Chapter 7 were produced in this manner.

A very similar image generation scheme can be carried out using a graphics printer in place of the camera and film. The printer can be of the ink jet type for high resolution, or a dot matrix for lower resolution. If the sampling data rate is on the order of the printer's speed, this method can be used in real time. If the scanning rate is faster, a local printer buffer can be used to temporarily store the data, which can then be printed out at a later.

In a clean room environment, it is not desirable to have photographic materials or impact printers due to their particulate generation properties. An alternate way to preserve a large amount of analog data is with a device known as a scan conversion memory.[96] These devices feature a nondestructive electron beam addressed charge storage tube which can be randomly addressed during the writing interval and then read out at standard video rates. The display can then be viewed on a video monitor at resolutions approaching 1300 lines per frame. If hardcopy is still desired, an off-line video hardcopy unit can be provided.

All of the storage techniques discussed thus far have used purely analog storage media. There are of course, numerous digital storage techniques. Magnetic or semiconductor materials can serve as the proper storage medium depending on the specific application. To keep these applications in perspective,

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[96] Hughes 639H Scan Converter Memory or EG&G PEP-500 Analog Storage Tube.

the amount of memory allocation needed to store a 1500 line digitized image is over 2 M bytes. Pixel compression techniques can be employed to reduce this burden substantially through the use of additional hardware. This nearly limits our storage choices to magnetic hard discs. The image could again be displayed on a high resolution monitor and printed off-line if hardcopy is desired. The digital storage technique has the additional advantage of being able to transport the recorded data. In order to form comparisons between large sets of samples the digital storage is more desirable, whereas for fast simple analytic work the CRT and film technique is more versatile.

5.3 LASER BEAM POSITIONING

As described in section 4.1.2, a moving iron galvanometer will be utilized to achieve the horizontal axis beam deflection. The galvanometer was chosen mainly for its versatility in being able to attain various modes and frequencies of operation. The scanner can only operate over a limited angular excursion, and its speed of response is determined by the mass of the armature and mirror, the drive limitations of the external drive circuits, and the power dissipation limits of the galvanometer windings. There are a number of scanning errors or irregularities inherent in the use of moving iron galvanometer scanners. Among them are drift errors, repeatability errors, linearity or gain errors, and wobble.[97] Drift errors are

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[97] P. Brosens, *Scanning Accuracy of the Moving-Iron Galvanometer Scanner,* Opt. Eng. **15** (Mar.-Apr. 1976), 95-98.

mainly a function of the temperature dependence of the position sensors used and the temperature coefficients of the drive circuits. This source of error is effectively controlled through the use of temperature regulators built into the scanner assembly. Repeatability errors are attributable to hysteresis of the galvanometer but through the use of a suitable feedback scheme, these too can be eliminated. Temperature gradients and power supply drifts are also the cause of gain and linearity errors, which with the proper drive circuitry and compensation, can be diminished.

Errors produced by the mirror's rotation about an axis orthogonal to that of normal rotation are known as wobble errors. This parasitic mode will arise whenever forces orthogonal to the mirror surface are applied to the rotor to displace it in a lateral direction. Minor contributions to wobble error are unsymmetrical magnetic flux and bearing imperfections, while the major contribution is from mirror imbalance. This results when the mirror is not mounted with its center of gravity located on the center of rotation. This can be solved by carefully mounting the mirror on a balanced shaft. Since the mirrors are generally thick, the armature mounting surface must be off center. The mounting technique is pictured in Figure 25 on page 82 where a flat has been milled in the cylindrical galvanometer shaft and the mirror attached to it using optical cement. Since the mirror being used has a diameter of 32 mm, the mirror was tapered to reduce the moment of the mirror mass even further. The actual armature mounting bracket is machined out

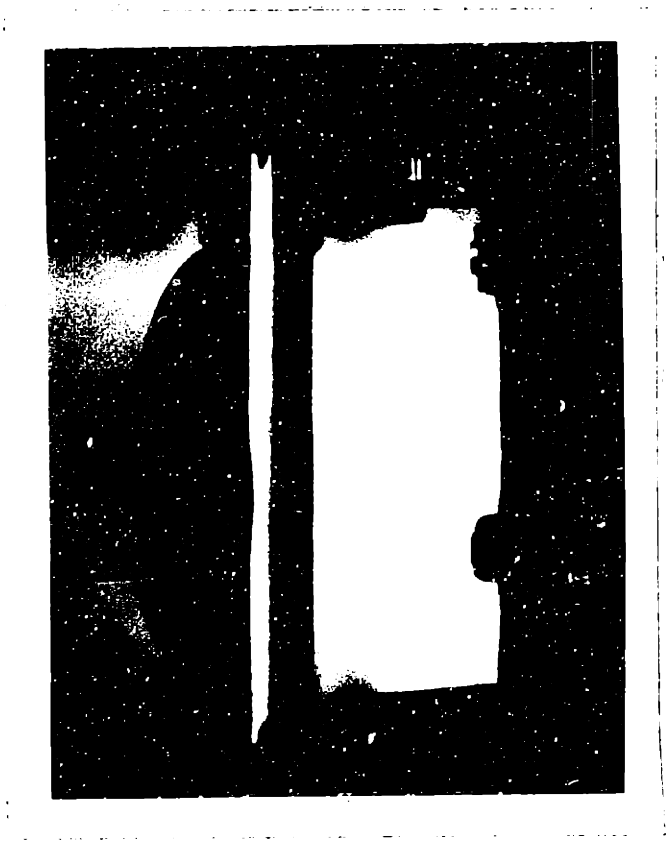

Figure 25. Tapered Deflection Mirror and Mount

of titanium for light weight and high strength. As a final method of reducing wobble, the unconstrained end of the armature/mirror mount is captured in a jewelled bearing for increased support. The only source of error remaining is due to deformation of the mirror surface which results from the dynamic torque applied by the shaft. For the mirror in use, the degree of distortion is limited to 0.1λ .[98]

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[98] P. J. Brosens, *Dynamic Mirror Distortions in Optical Scanning,* Appl. Opt. **11** (Dec. 1972), 2987-89.

5.3.1 Horizontal Axis

5.3.1.1 Open loop

While most of the control problems associated with galvanometer scanners are resolved through the use of servo controllers, there are certain applications where open loop (non-feedback) driving schemes are advantageous. The most significant advantage is speed of operation. For closed loop systems, the operating speed is usually limited to between 20 and 30% of the natural frequency. For the galvanometer being used this corresponds to about a 60 hz operating frequency. During open loop operation, the galvanometer may be excited at, or above, its natural frequency. However, this mode of operation can only be used when the desired deflection waveform is to be sinusoidal. If the galvanometer is operated at its natural frequency, very little drive power is required. If a waveform such as a sawtooth is desired, there is another method which can be used to shorten the flyback and recovery time of the mirror. As shown in Figure 26 on page 84, the actual galvanometer deflection has a large amount of ringing and overshoot during the desired linear portion of the waveform. If the drive signal is modified with a step of the proper height and width the ringing can be cancelled quickly, leading to very short settling times. As shown in the figure the added pulse has an amplitude of half the peak to peak amplitude and a width of one half the period of the ringing frequency. In order to sustain this driving waveform, which has a very high time rate of change in current, the compliance of

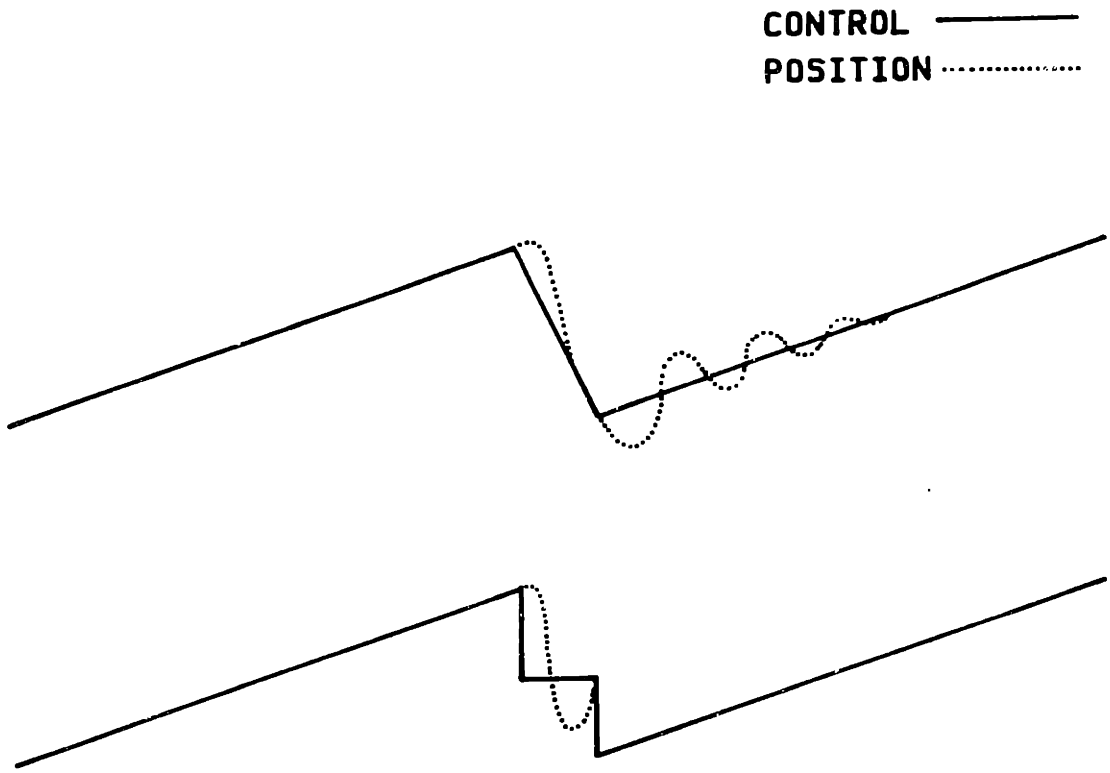

Figure 26. Waveforms for Step Compensated Galvo Drive

the source must approach 200 volts. While this drive capability is attainable, the power dissipating capability of the galvanometer is well under the supplied 300 watts leading to accelerated aging and failure of the galvanometer windings.

For high speed operation at a reduced duty cycle, the scanner can be driven with a high frequency sinusoid. A somewhat linear scan results if only a small portion of the angular deflection is used as the active scan area. This scan length restriction can be relaxed slightly if scan nonlinearity correction is performed at a later point in the data collection. One of these techniques is later described in

section 5.4.1. These two techniques coupled together yield the highest scan rates with very low distortion.

5.3.1.2 Closed loop

Most galvanometers in use today use a closed loop servo control mechanism to regulate the angular position of the armature. These techniques can increase the normal sawtooth scan limits from 10 - 30% of their natural frequency. Various pre-emphasis and feedback compensation schemes can be employed.[99] At their typical operating frequencies, galvanometers behave as second order systems and the classic feedback and linear system analysis can be applied to their compensation. [100]

Modern moving-iron galvanometers employ capacitive position transducers installed in the stator structure of the scanner for use in the feedback control loops. Electrodes mounted on the armature and stator form a capacitive bridge whose charge-discharge currents are monitored with an internal high frequency oscillator housed in the stator assembly.[101] This sensor is integrated into the feedback amplifier to form a closed loop feedback control system. In our application, this feedback was also included with the sinusoidal drive techniques to improve

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[99] H. M. Tenney, J. C. Purcupile, *Galvanometer Compensation to Extend its Frequency Range,* Proc. Soc. Photo-Opt. Instrum. Eng. **84** (1976), 62-68.

[100] J. K. Roberge, Operational Amplifiers , Wiley Press: New York, 1975.

[101] P. J. Brosens, E. P. Grenda, *Applications of Galvanometers to Laser Scanning,* Proc. Soc. Photo-Opt. Instrum. Eng. **53** (1974), 54-59.

long term stability and drift in the angular displacement of the armature. The feedback is rolled off at high frequency to maintain stability.

5.3.2 Vertical Axis

The scanning system chosen translates the sample under the stationary beam so that the vertical beam position is kept fixed during the scanning interval. The relay mirror prior to the scan lens can be adjusted to alter the vertical beam positioning in cases of misalignment.

5.4 FRAME STORE RASTER GENERATORS

5.4.1 Horizontal Axis

The horizontal or X axis ramp that is generated must be synchronized with the scanning motion. This can be accomplished by using the signal generated by the scanner controller which is the feedback systems' guess at the true mirror position. Alternatively, a photodiode can be mounted at the beam start position to produce a synchronization pulse that initializes a preset ramp generator. If the scan path is highly repeatable and known precisely, this method works very well. Unfortunately, the mirror position has many irregularities as described earlier so that this method is unsatisfactory.

In order to determine the true position of the beam, the spot position must be sensed after the beam has been through most of the optical path. In this manner all of the distortions introduced by the optics can also be corrected.

There are a number of different methods used to determine the linear position of a light spot. The simplest is to use a linear position sensing photodiode, whose conductivity fluctuates as a function of the light spot position. These photodiodes are adequate only for short distances as their linearity is marginal. A very high speed technique uses a fiber optic array feeding a single small area PIN photodiode. The output from this photodiode is then used to generate a pixel clock for use in a data acquisition system. The resolution is determined solely by the fiber spacing and alignment.

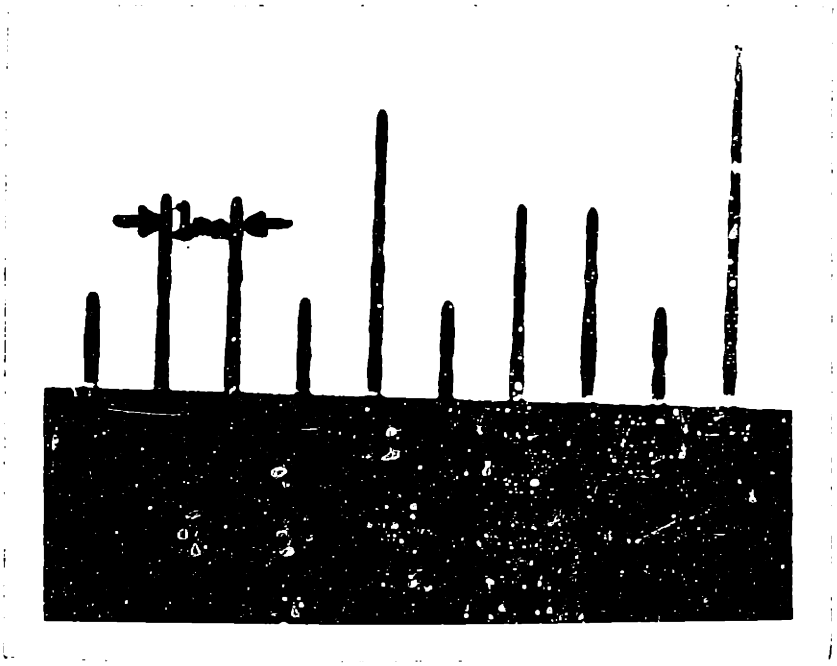

Figure 27. Photodiode Grating

For the best resolution, a lithographically produced grating can be used as a reference to generate the same pixel clock in a number of different ways. A

number of methods suggested by Jablonowski[102] ,[103] detect the light reflected from the grating back through the optical path to modulate a single small photodiode. Since the percentage of the input beam that reaches the detector is very small, a large portion of the input beam can be spent in this manner. An alternate method is to use the grating as a shield which is laid over a long photodiode. This method is limited by speed due to the high capacitance of the long diode junction but requires much lower power to operate. The grating consists of an antireflection coated chromium grating pattern evaporated onto a 0.125 inch thick strip of soda lime glass. The grating lines (Figure 27 on page 87) are 2 mils wide placed on 4 mil centers. At the normal scanning rates this produces pulse repetition rates approaching 1 Mhz.

Due to the large junction capacitance of the grating photodiode, it will be reverse biased at -15v in a photoconductive mode to maximize response speed. The preamp used to amplify the signal is also mounted as close as possible to the diode (see Figure 28 on page 89) to reduce stray loading effects. The circuit shown in Appendix E.1 is a transresistance or current to voltage amplifier with a power output drive stage. The output stage is included so that the preamp can drive a long length of 50Ω line to maximize the speed of the grating output.

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[102] D. P. Jablonowski, J. Raamot, *Beam Deflection at High Accuracy and Precision,* Proc. Soc. Photo-Opt. Instrum. Eng. **84** (1976), 69-76.

[103] D. P. Jablonowski, J. Raamot, *Galvanometer Deflection : A Precision High Speed System.* Appl. Opt. **15** (June 1976), 1437-43.

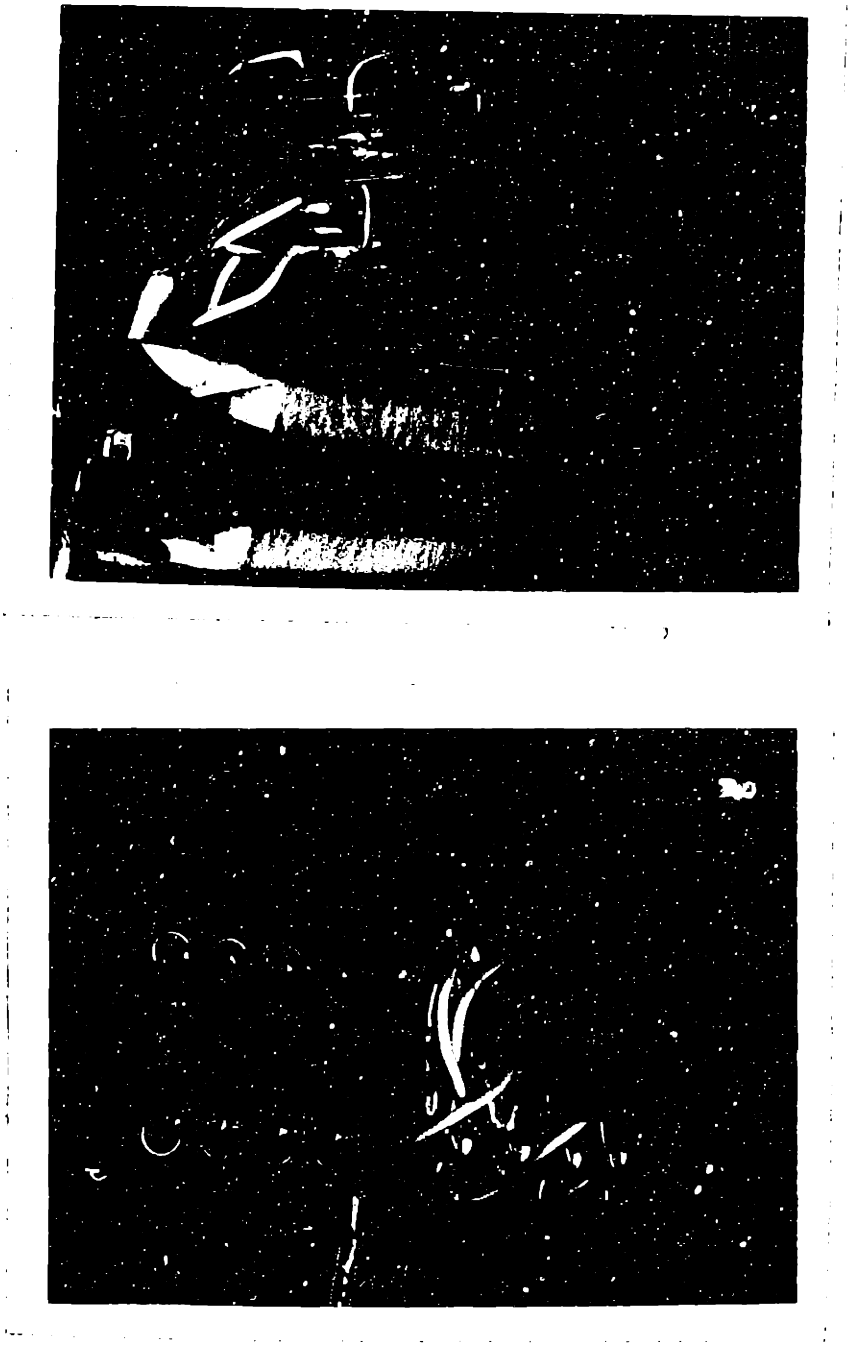

Figure 28. Grating, Photodiode Assembly, and Grating Preamp

The grating signal is routed to the main electronics section where it is terminated into 50Ω. The pulse train is then conditioned using a zero crossing detector and a one shot which will generate a fixed duration, logic level pulse for each grating stripe. Since the beam deflection is sinusoidal, it passes over the grating during the active and retrace intervals. Additional logic circuitry is needed to determine the direction of the beam travel. The timing waveforms describing this function is included with the full schematics in Appendix B.1.

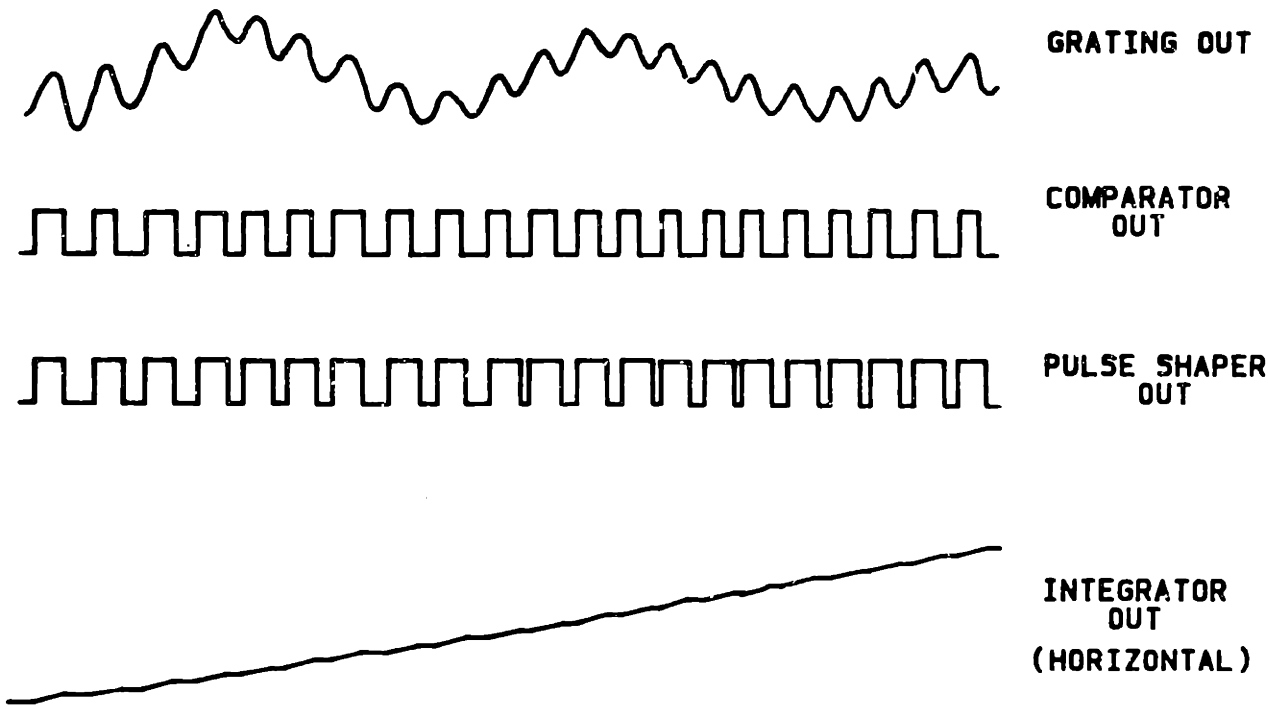

Figure 29. Integrator Output Waveforms

A voltage ramp must now be generated from the conditioned grating pulse train. This is accomplished through the use of a precision integrator which is fed by a controllable charge pump. A current source is connected to the input with a switch that is being controlled by the pulse train. In this manner, one grating pulse injects a fixed amount of current into the integrating capacitor yielding an output waveform as in Figure 29 on page 90. The integrator output is then filtered to remove the high frequency switching transitions and spikes. Level and gain adjustments are performed and the output is fed to the horizontal axis of the recording CRT.

5.4.2 Vertical Axis

The vertical raster generator circuit is much easier to implement due to the lack of problems similar to the mirror nonlinearities. The ramp must be synchronized with the linear position of the sample as it is being translated under the detector by the wafer transport. As discussed in section 4.2.2, an AC hysteresis motor will be called upon to drive the sample translation stage. Although the motor has intrinsic speed regulating properties, the transport speed is still very sensitive to friction along the drive path due to the low speed that it is traveling. To eliminate these and other remaining nonlinearities, a feedback mechanism can be mounted on the transport itself to provide a true positional output. For short transport strokes, a magnetic linear position transducer could have been used for

best results, but in our case, since the transport moves a long distance, a multiturn potentiometer mounted on the shaft serves the purpose (Figure 30 on page 93).

The shaft potentiometer is biased with a voltage reference so that the output voltage is now proportional to the linear position of the wafer transport. This proportionality constant can be adjusted by changing the diameter of the idler gear to which the potentiometer is mounted. In order to initiate the scanning cycle, the transport position must be monitored until it passes a preset threshold. Consequently when the transport has progressed beyond the active scan field, the scanning cycle must be terminated. This function is performed with the use of a window comparator[104] as implemented and described in Appendix B.2.1. The output stage consists of a follower which tracks the input and then subtracts the analog start threshold so that the output will start from 0 volts at the initiation of the sweep. The relevant deflection waveforms are also shown in Appendix B.2.3.

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[104] Electronics, Designer's Casebook No. 6, New York: McGraw-Hill, 1983.

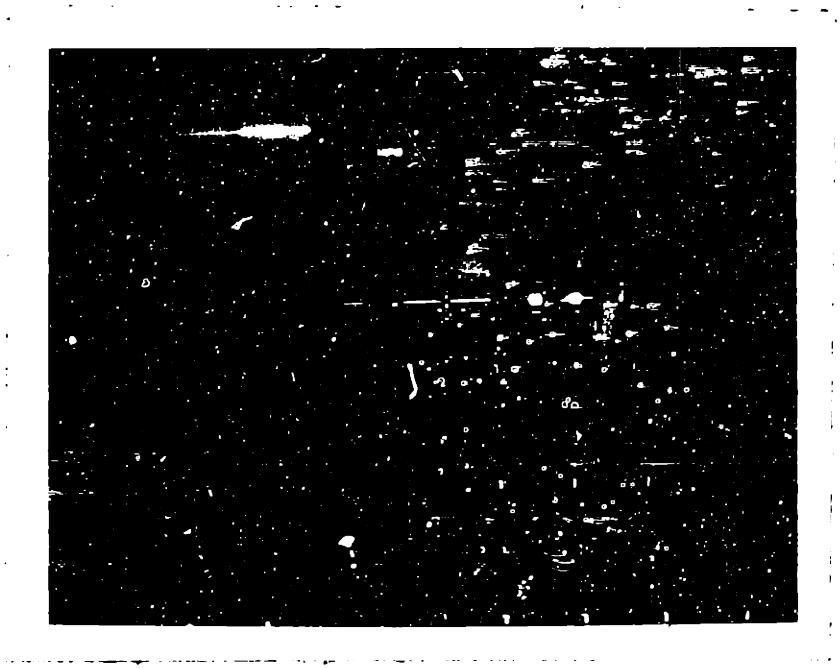


Figure 30. Shaft Mounted Position Transducer

6.0 RESULTS

6.1 PHOTOVOLTAGE IMAGES

6.1.1 Contamination

The first photovoltage image (Figure 31 on page 95) shows the result of dust and other particulate contamination on a silicon wafer. This is a p-type wafer with a low temperature CVD plasma oxide. Also note the prominent swirl pattern. As mentioned earlier in chapter 3, the detected signal is a result of the abrupt change in surface potential when the scanned charge cloud traverses a defect. If the defect is a line dislocation and not a point defect, the direction in which the beam scans over the defect determines how well it shows up in the image. Since the signal pickup is capacitive, the sharper the transition the bigger the signal. Swirl, for example, is normally distributed as a set of concentric circles around the center of the wafer. Therefore, for any scan line on the wafer, the line will perpendicularly intersect a given swirl line along the diameter of the wafer at the edges, and tangent to the swirl line at the top and bottom. When the scan line intersects a line dislocation at right angles, the maximum signal is produced due to the very abrupt transition in the surface charge. However, when the scan line is parallel to the swirl line, only small changes in the differentiated surface potential are detected. In the photograph, note how the swirl lines seem to disappear when they are parallel to the scan direction (horizontally). This only happens with line

defects parallel to the scan line. Point defects or very short line defects are not affected by this phenomena.

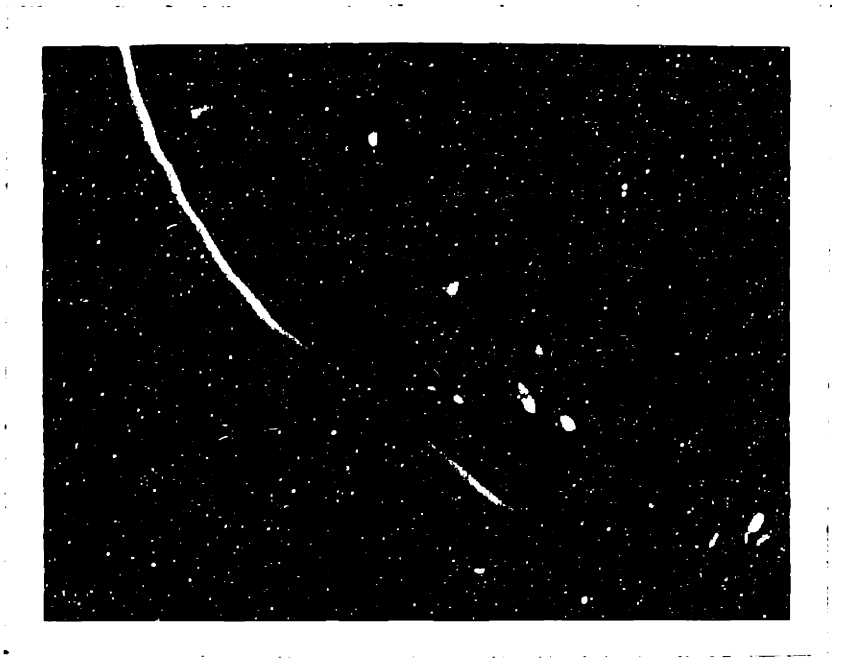


Figure 31. CVD Wafer With Particulates

Shown in Figure 32 on page 96 is the result of possible sodium contamination. Note how the swirl is washed out around the defects, implying very short lifetimes in their vicinity indicating that most of the carriers recombined very quickly around these high recombination sites. Since the magnitude of the resistivity gradient is much greater around these defects than for the swirl, it becomes the dominant factor in that section of the image.

Figure 32. Sodium Contaminated Wafer

Figure 33 on page 97 also shows the effect of possible sodium or other mobile ion contamination on a wafer with very little swirl. This contamination could have resulted from particles introduced prior to a hot process which diffused the contaminant over a large area.

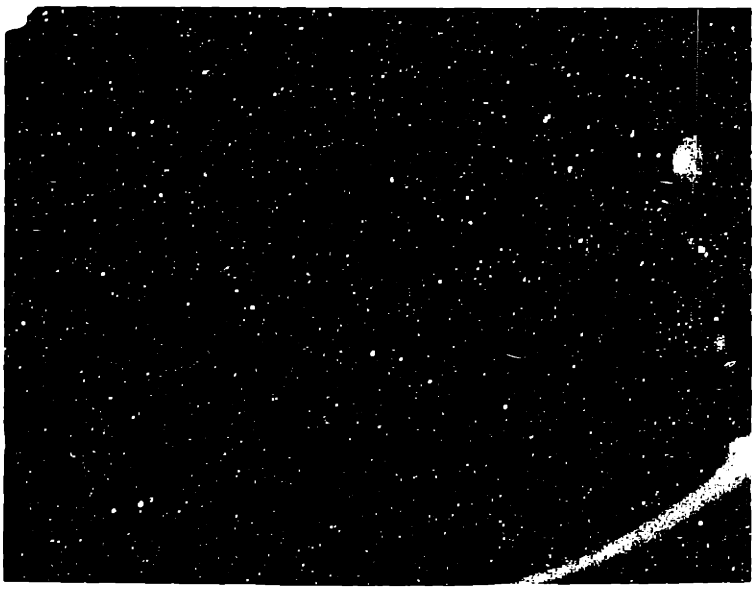


Figure 33. Mobile Ion Contaminated Wafer

6.1.2 Mechanical Defects

An example of crystallographic damage introduced during handling is illustrated in Figure 34. This particular set of scratches was the result of normal handling with a pair of metal tweezers only once. The scratches were not visible to the naked eye.

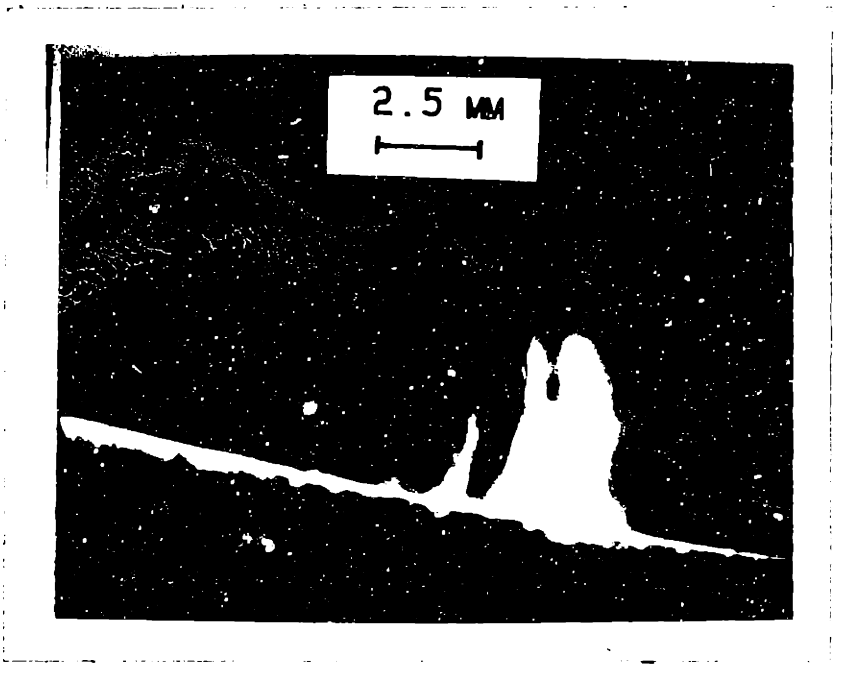


Figure 34. Metal Tweezer Damage

Teflon tipped vacuum tweezers are now used during most of the manual handling operations used during processing. Although these are much better than their metal predecessors, they can still leave minute scratches as shown on the wafer below. This scratch was introduced while a closely packed cassette full of wafers was being manually unloaded with a vacuum pencil. This was actually a

minute scratch in the oxide layer which was slightly visible as a blemish on the surface. Note the huge contrast between the scratch and the background swirl. The shadow from the scratch in the image resulted from an overload of the display electronics due to the large signal.

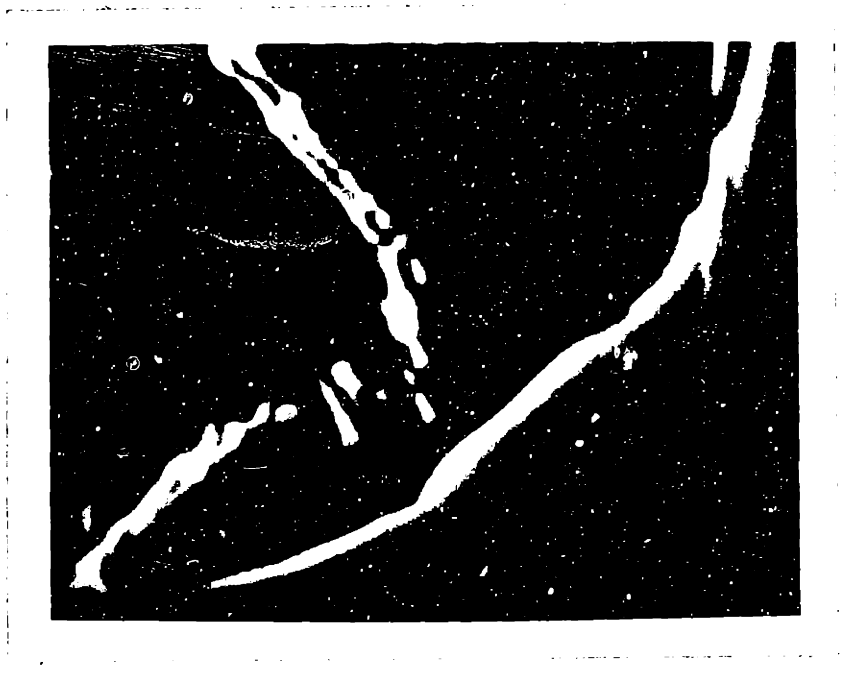


Figure 35. Vacuum Tweezer Scratch

6.1.3 Crystallographic Defects

A number of crystal growing and initial process defects are shown below. The first (Figure 36) pictures a wafer with an off center swirl distribution implying that non-uniform temperature gradients existed during the crystal pulling process.

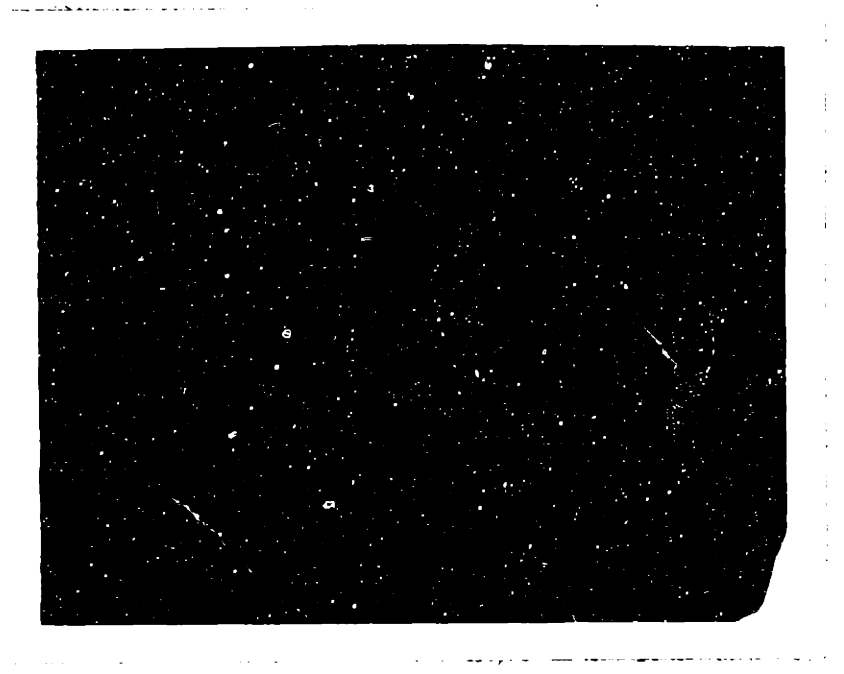


Figure 36. Off Center Swirl

A number of slip examples follow, Figure 37 on page 101 shows massive edge slip, Figure 38 on page 102 shows a comparable x-ray topograph, while Figure 39 on page 102 shows some edge and center slip. Note the difference between the contrast of the swirl and slip in the x-ray topograph and in the scanning surface photovoltage image. Since the x-ray topograph is a bulk sensing

technique so that many of the swirl lines average out over the thickness of the wafer and their contrast is reduced. Since the photovoltage probes only at the surface, its sensitivity to these surface states is much higher.

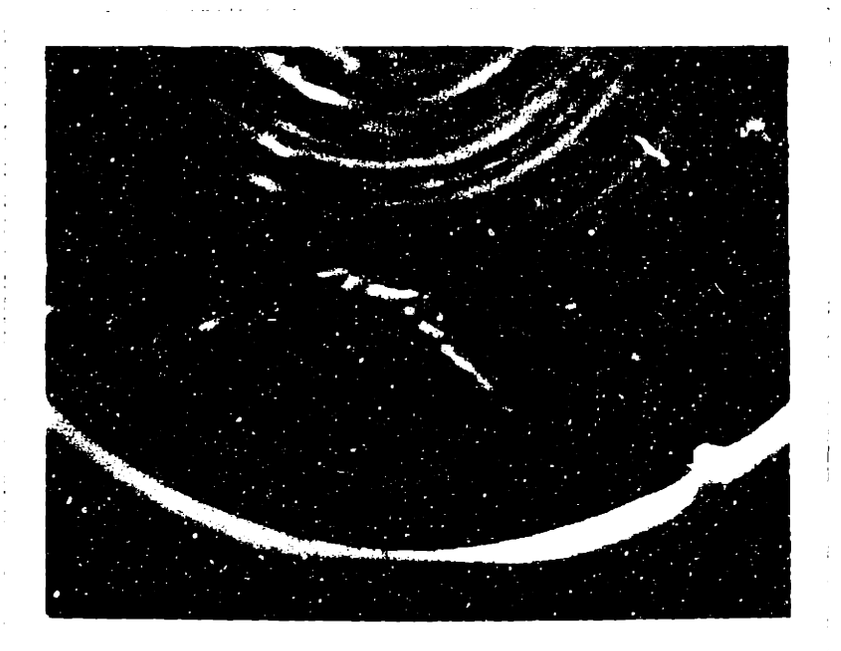


Figure 37. Edge Slip

Center slip results from internal stresses introduced by a wafers which are concave or convex. During hot processes, thermal stresses deform the wafer sufficiently to cause slip dislocations in the center as well as the edges of the wafer. The density of dislocations at the center is much greater, hence the area in the image appears as a solid defect. In reality, this region is made up of a very fine grid of slip dislocations.

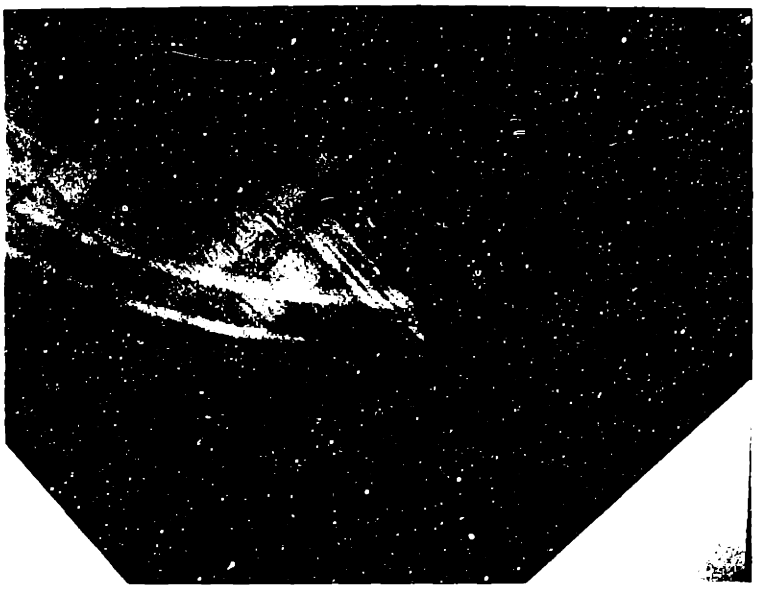


Figure 38. X-ray Topograph of Edge Slip

Figure 39. Center and Edge Slip

6.1.4 Contact vs. Non-contact

Figure 40 on page 104 shows the result of making a contact to the substrate instead of running with a full differential capacitive detector. This was achieved by coupling the back surface of the wafer with water to a metallic plate referenced to the preamplifier ground terminal. In this manner, the current could be directly measured by the preamplifier. The numerous small spots in the photograph are dust particles on the wafer surface. The white tail following the spots are due to the pulse recovery characteristics of the CRT used to form the image. The vertical bars are due to very slight changes in the laser beam intensity as it is scanned across the sample. These striations were later removed by using a cleaner optical system.

The same wafer was later scanned with the full differential detector and the result is pictured in Figure 41 on page 104. This detector kept the wafer electrically floating and supported only by a quartz plate. Since the coupling is now capacitive and not direct, the signal levels are much less. The high frequency gain suffers the most, resulting in an image that is not quite as sharp as the contacting image. Later improvements in the detection electronics led to the results as shown in Figure 42 on page 106. This shows that comparable results can be achieved without the use of any external contacts.

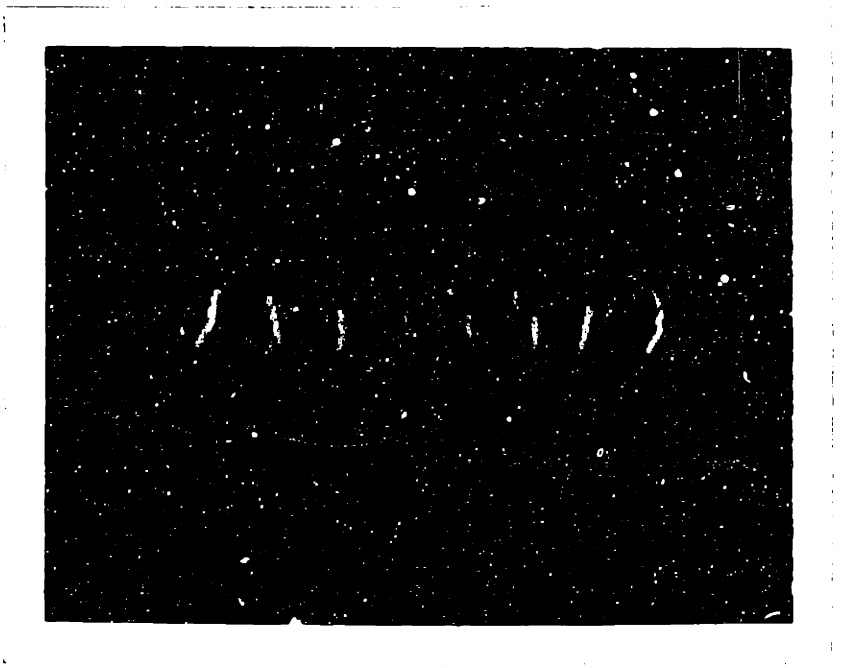


Figure 40. Contact Scanning Surface Photovoltage

Figure 41. Capacitive Scanning Surface Photovoltage.

6.1.5 High Resolution

Since the resolution of the tool is an important specification, an attempt was made to generate the highest resolution image that was possible with the present apparatus. A number of problems were encountered when this was tried. The largest difficulty was trying to accurately position the laser beam. Due to the random nonlinearities in the galvanometer, very repeatable scan lines were very hard to obtain, resulting in lateral shifts in the images. As shown in Figure 42 on page 106 a number of scan line shifts are evident in the middle of the numbers. For this image the optical system was optimized and higher performance electronics were utilized resulting in an improvement in the earlier images in Figure 41 on page 104. Th notch at the bottom of the image is the wafer orientation notch on the edge of the wafer. Also note the edge slip at the very top of this notch. The digits pictured in here are laser scribed trenches in the oxide of the wafer. The center to center distance of the individual lines making up the digits is 65 microns. Since our laser spot size is only 30 microns, this image is limited by the laser spot diameter.

Figure 42. High Resolution Laser Scribed Numbers

7.0 CONCLUSIONS AND RECOMMENDATIONS

7.1 RESULTS

The scanning surface photovoltage images produced by this completely non-contact method correlate directly with the conventional contacting and destructive techniques such as x-ray topography and selective etching. It is furthermore shown that to detect a surface photovoltage signal sufficient to image semiconductor defects, a simple air gap capacitor can be used in place of a MOS or Schottky contact. The line scanning rate of 200 hz has also made this tool applicable to real time analysis with high throughput rates. Since there is no contact to the sample whatsoever, contamination does not become a problem. The achieved resolution has been limited by the laser beam diameter as expected from the analysis in section 3.1.2. The tool's sensitivity to swirl, slip, and surface contamination has also been shown to be very good. Epitaxial silicon layers, nitride layers, and low temperature CVD plasma oxides have been scanned as well with very good results. It can also be used to probe wafers anywhere along the processing cycle, from initial oxide growth to metallization. Potential uses for this tool also exist in n-type silicon and GaAs wafers.

7.2 FUTURE IMPROVEMENTS

Many of the problems associated with the scanning system and subsequent horizontal raster synchronization are a result of the nonlinearities of the

galvanometer scanner. It's replacement with a rotating polygon mirror would improve linearity and scanning efficiency greatly and provide more accurate laser beam placement. This latter point becomes especially crucial in high resolution applications. A superior lens that could achieve a tighter focus would also improve the resolution.

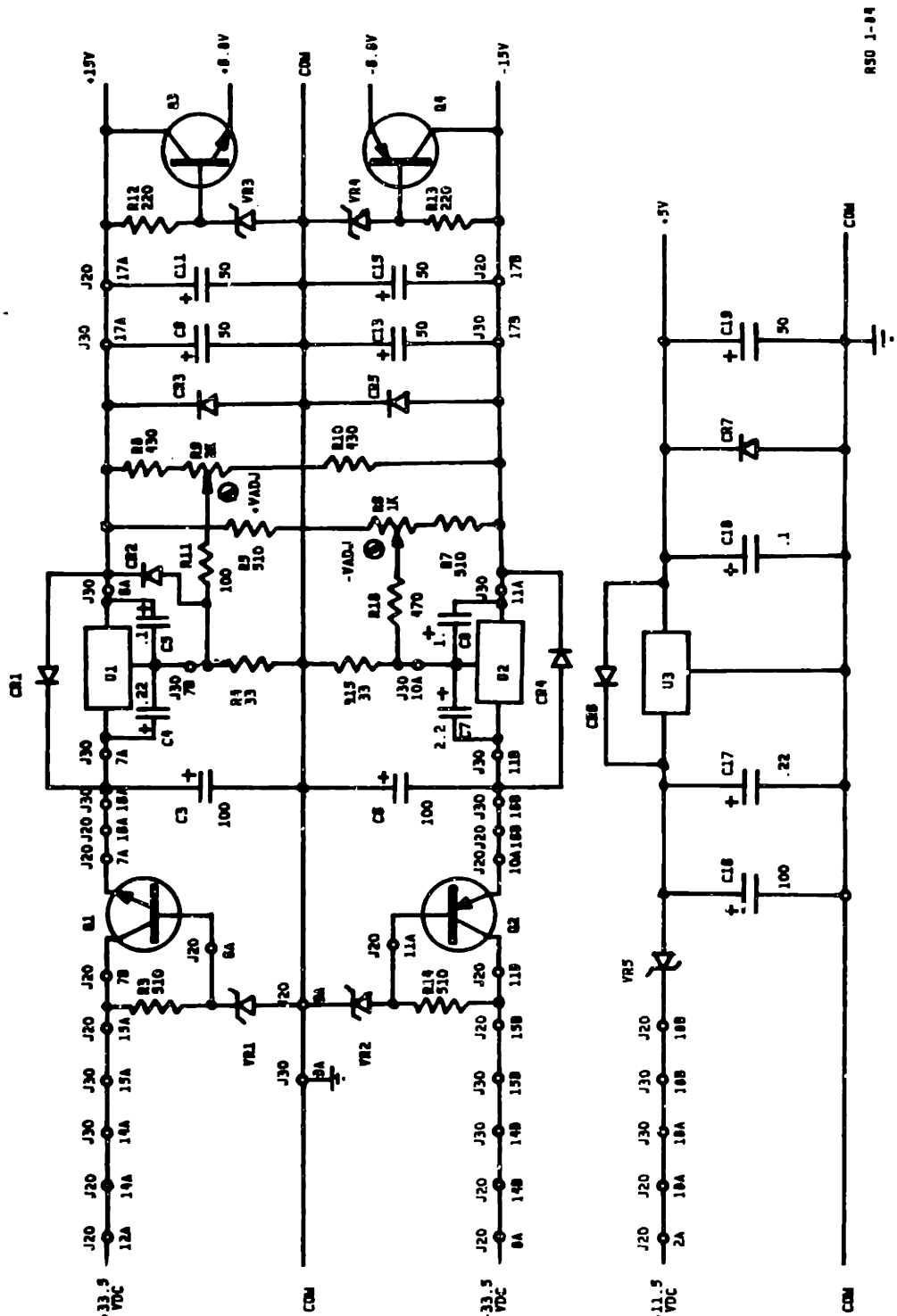
There are, however, other limits that restrict the scanning speed and spot size. If the scanning speed is too high or the spot size become too small, the signals produced will have frequency components well above the gain rolloff point of the amplifiers. Another consequence of a decreasing spot size is the need to display a larger amount of data. It would be foolish to scan the sample at a resolution much greater than you could ever display.

Tighter tolerance on the wafer transport that would reduce the detector to sample spacing would provide higher sensitivity due to the increased capacitive coupling. Improved electronic filtering and a possible change to a synchronous detection scheme (with chopped illumination) may place a tighter limit on the probe depth. A high speed digital acquisition system with image enhancement capabilities could also provide large improvements in the perceivable quality of the image.

APPENDIX

A. POWER SUPPLY

A.1 Schematic



A.2 Circuit Description

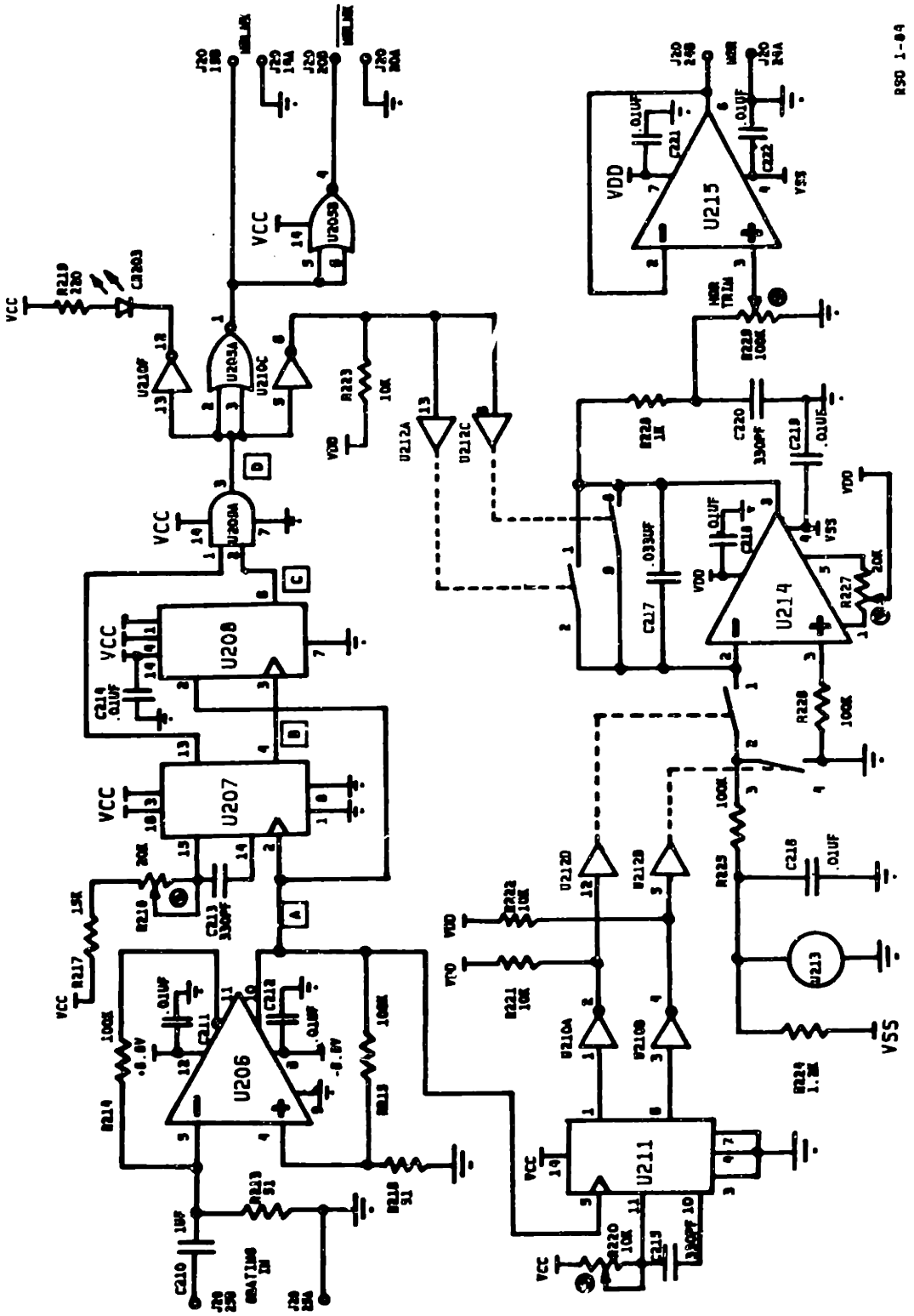
This power supply provides the signal amplifiers and raster generators with highly regulated DC power. The ± 15 V supplies are rated at ± 500 mA each and the + 5 V logic supply at 1000 mA. An additional bipolar supply of ± 6.8 V is provided for the high speed differential comparator in the horizontal ramp generator circuit. The power supply is fully protected against short circuits, thermal overloads, and load transients. The bipolar supply uses a series pass preregulator (Q1, Q2) to filter and attenuate the raw DC input voltage to approximately 19 V. These power transistors are mounted on an external heat dissipating surface in the mainframe cabinet and are not on the power supply printed circuit board itself. This greatly reduces the internal power dissipation of the power supply module. A linear regulator integrated circuit is then used to derive to final 15 V supplies. The maximum output current for these supplies is limited by the primary supply's current limit of 500 mA.

The + 5 V logic supply utilizes a series connected zener diode to drop the input voltage to the linear regulator to reduce the power dissipation in the regulator. The current capacity of this supply is limited by the regulator's power capacity to 1000 mA.

B. RASTER GENERATORS

B.1 Horizontal Ramp Generator

B.1.1 Schematic

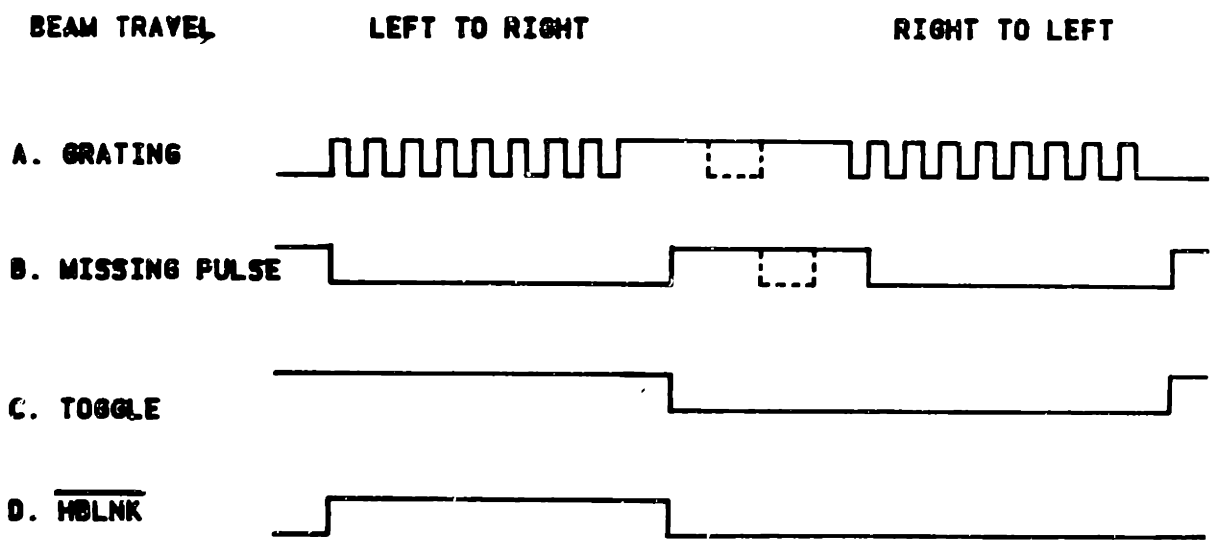


B.1.2 Circuit Description

The horizontal ramp generator circuit produces a positive going linear ramp which is synchronized to the lateral position of the laser beam on the sample. The pulse train from the reference grating is received and shaped by a high speed differential comparator (U206). In order to obtain a fixed duration pulse, the squared signal is applied to a one-shot (U211) which then controls the charge pump and integrator (U214). A missing pulse detector and an assortment of logic are used to determine the direction of travel of the beam on the wafer. The output waveforms for this circuit are shown in Figure 29 on page 90.

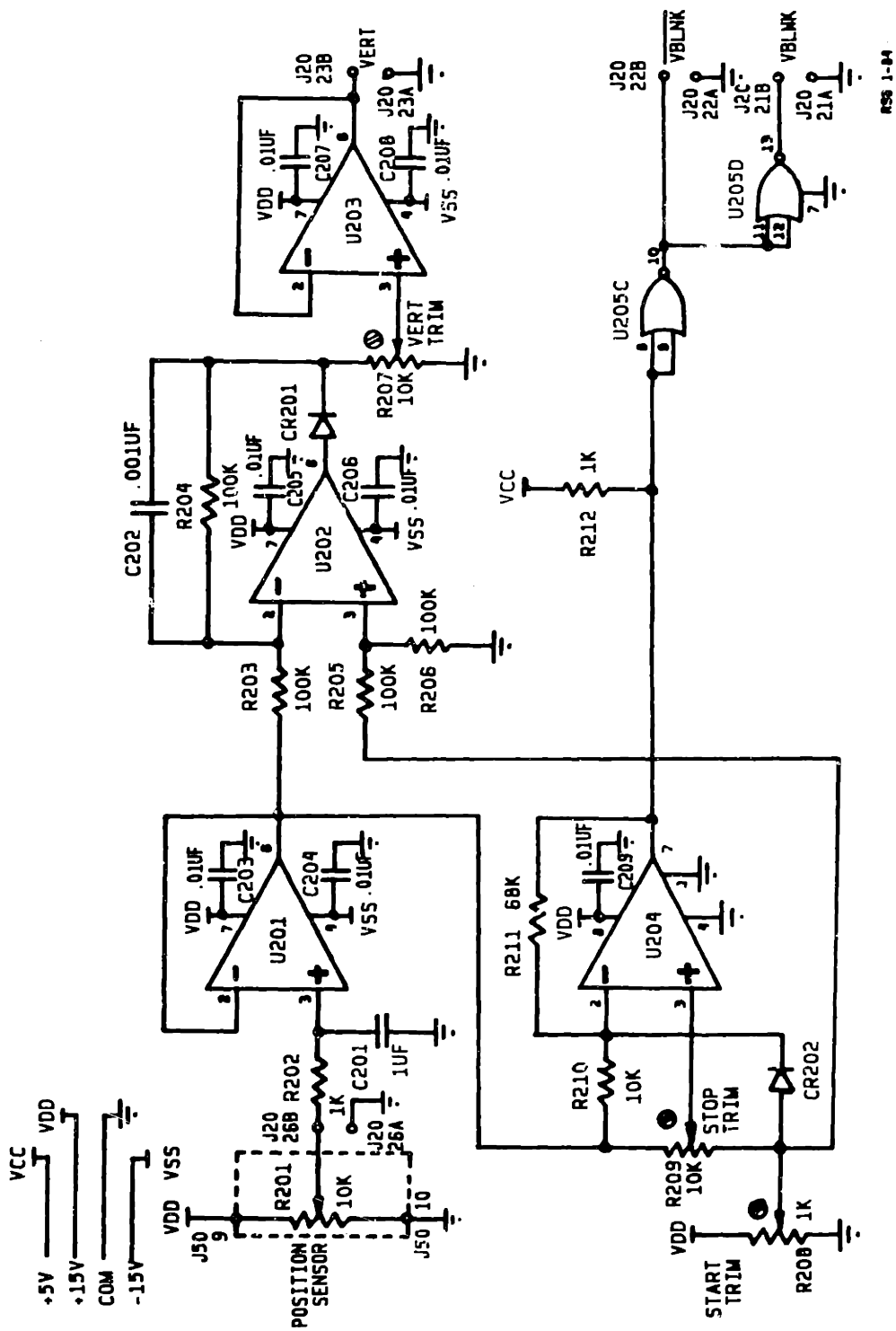
B.1.3 Grating Timing Waveforms

The logic residing in the horizontal ramp generator determines the direction that the beam is traversing the grating in order to produce the horizontal blanking signal. The letters on the following diagram correspond to points on the previous schematic.



B.2 Vertical Ramp Generator

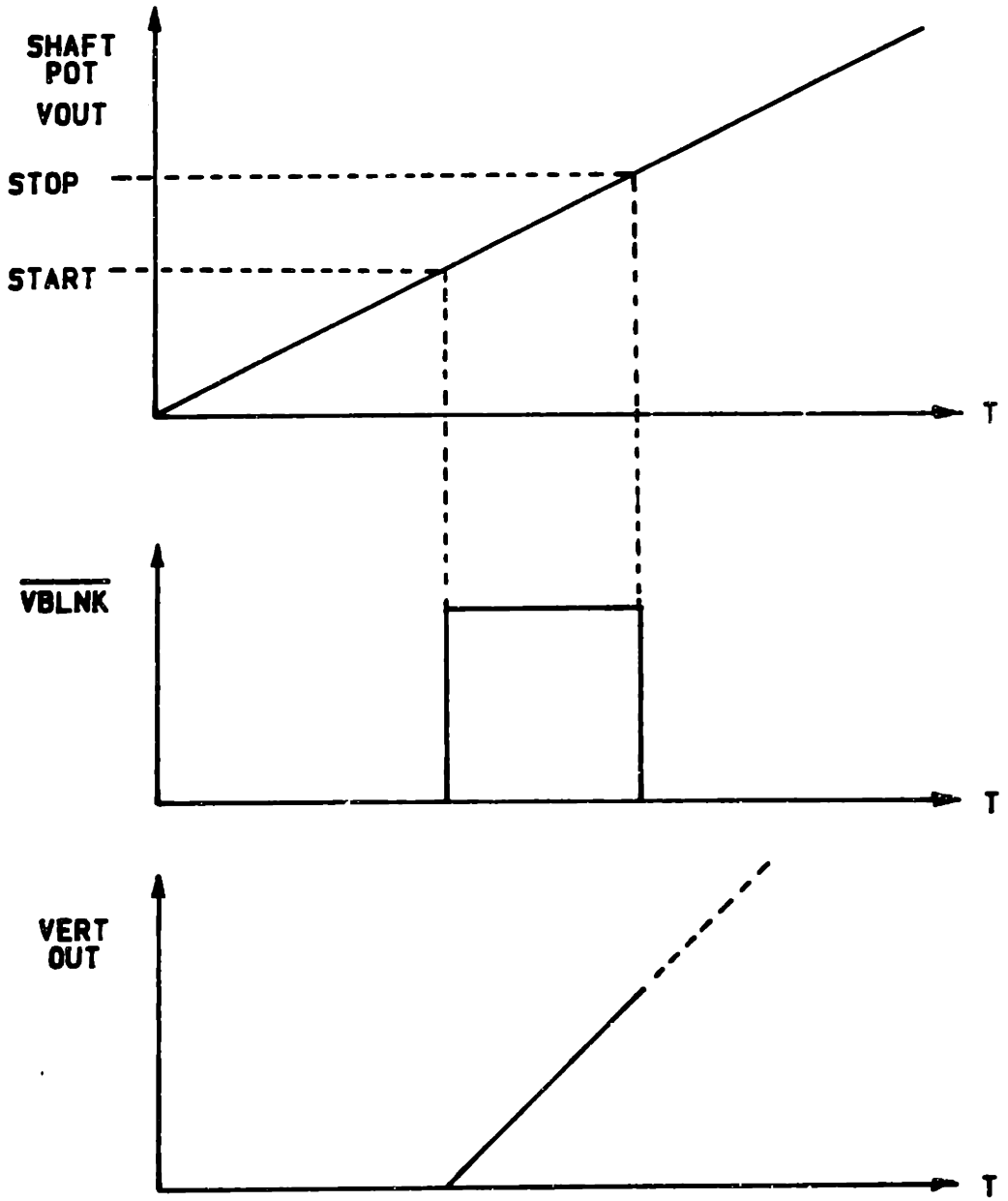
B.2.1 Schematic



B.2.2 Circuit Description

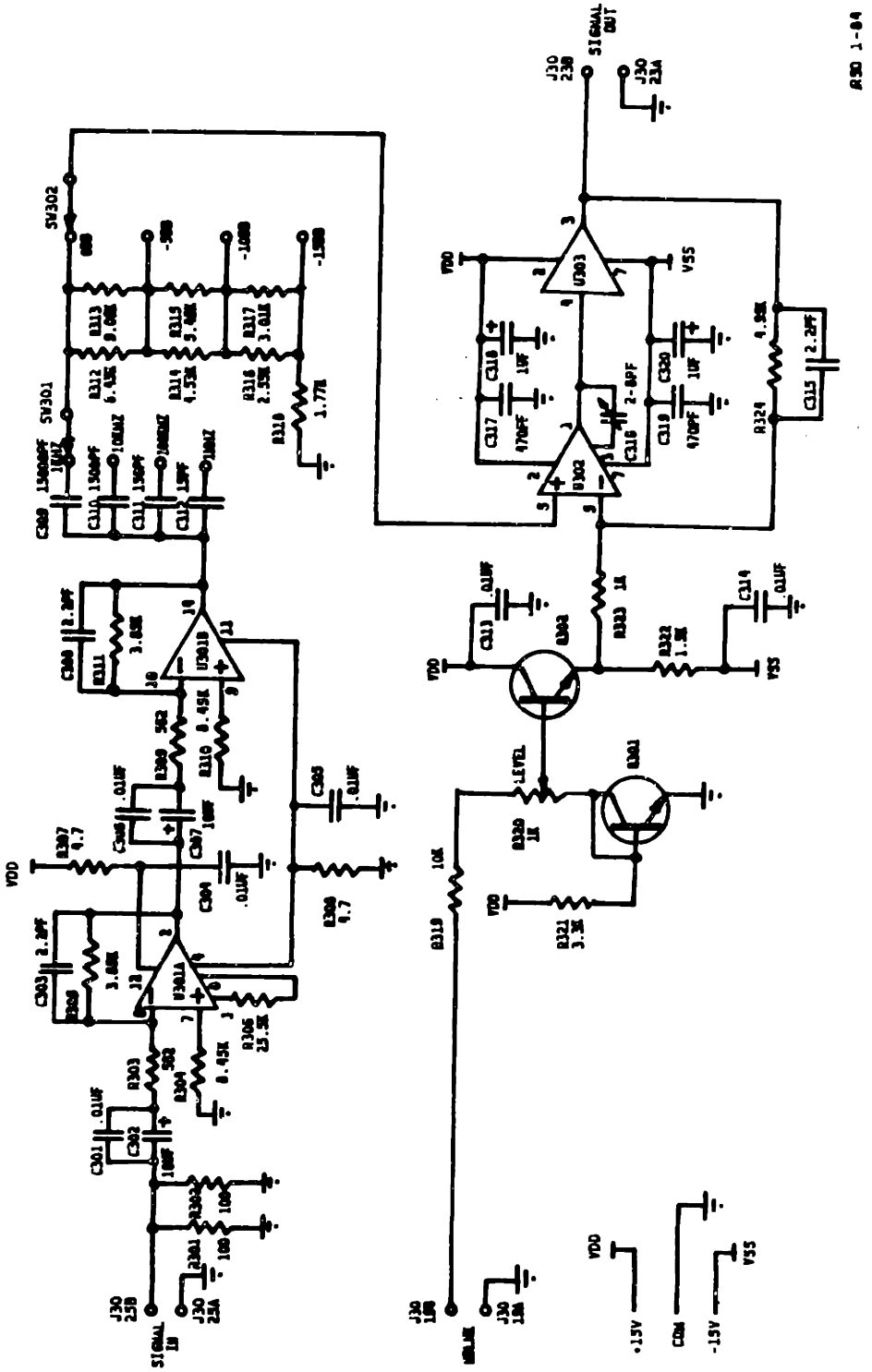
The vertical ramp generator produces a linear ramp proportional to the travel of the wafer transport. A multiturn potentiometer is mounted on the drive shaft of the wafer transport to function as a position transducer. The output voltage of the potentiometer 0 and +15 V at the two end limits of the transport. In order to produce an output ramp that starts at 0 V and increases linearly, the scan start position must be subtracted from the potentiometer's output. This is performed through the use of a differential amplifier (U202). A window comparator (U204) is used to determine the scan stop position and to generate the vertical blanking signal. The remaining amplifiers and gates in the circuit provide input buffering and output drive capability.

B.2.3 Vertical Timing Waveforms



C. SIGNAL AMPLIFIER

C.1 Schematic



C.2 Circuit Description

The signal amplifier provides the functions for amplification, filtering, and level shifting. The input signal from the signal preamplifier is AC coupled to two identical amplifier stages (U301) operating with a gain of 16.3 db each over a 3 db bandwidth of 28 hz - 40 Mhz. Following the initial gain stages is a variable high pass filter whose low frequency cutoff is switchable from 1 Khz to 1 Mhz. A passive attenuator is included for gain control after which the output amplifier provides an additional 15.6 db of gain from DC to 30 Mhz. The horizontal blanking signal and a DC offset are added into the output signal to provide the appropriate video waveform. The overall gain of the signal amplifier is 48.2 db over a 3 db bandwidth of 1 Khz to 10 Mhz. The output stage has a drive capability of $\pm$ 10 V into a 50 Ω load with slew rates in excess of 1000 V / μs.

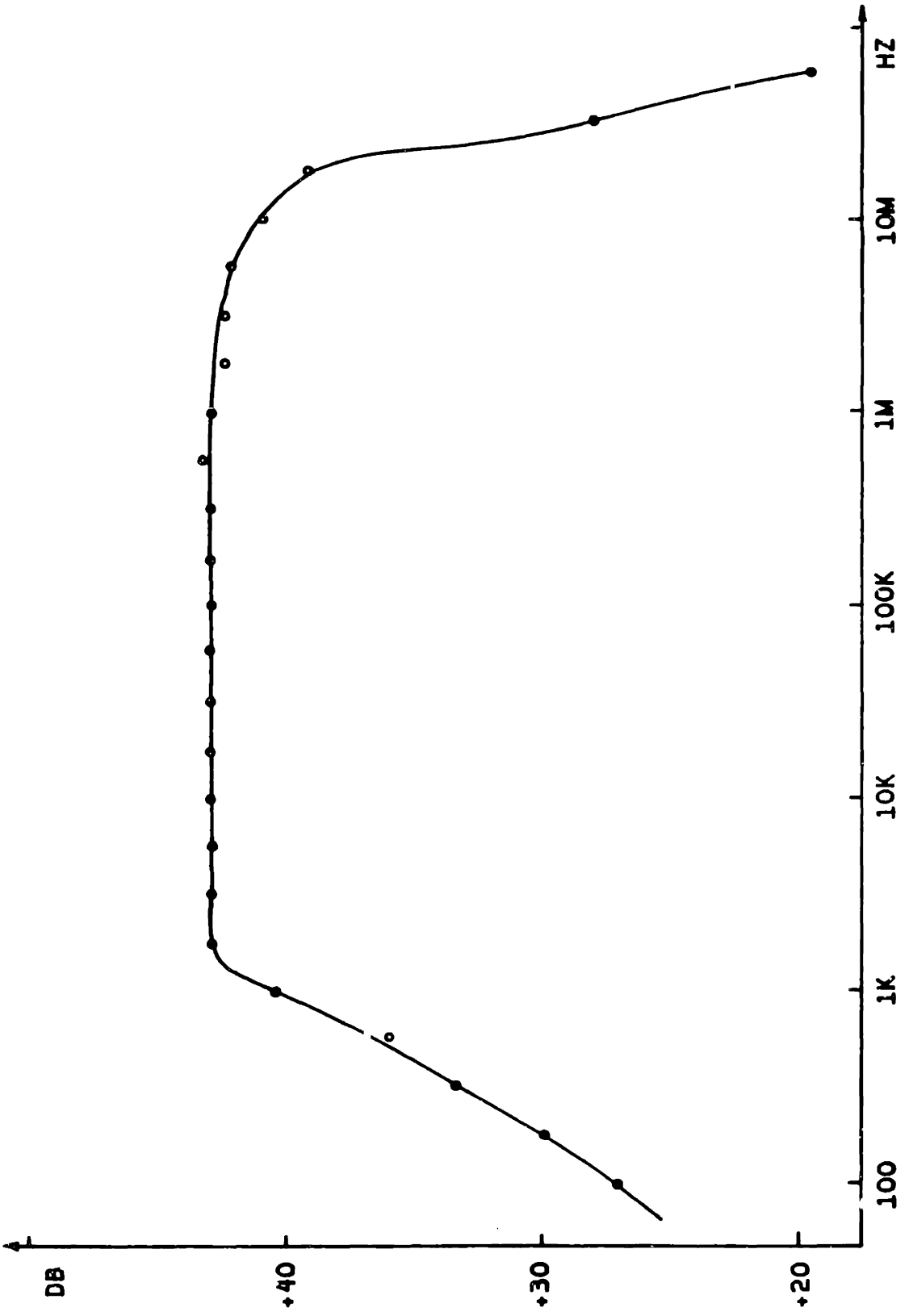
C.3 Signal Amplifier Measured Frequency Response

C.3.1 Frequency Response Data

Gain Control = -5 db
Bandwidth Control = 1 Khz
Vin = 8 mV Sine wave

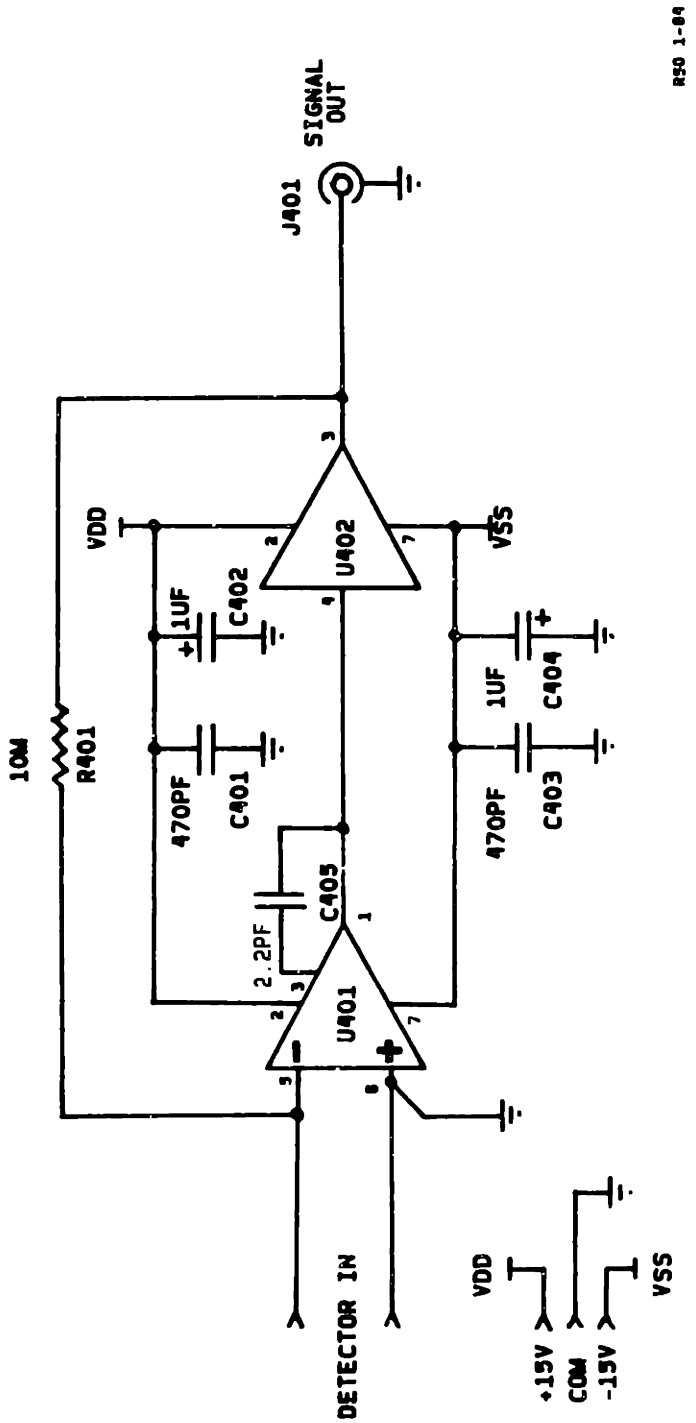
f hz	log f	Vout mV	Gain V/V	Gain db
100	2.00	180	22.5	27.0
178	2.25	250	31.3	29.9
316	2.50	370	46.3	33.3
562	2.75	500	62.5	35.9
1 K	3.00	840	105	40.4
1.78 K	3.25	1110	139	42.8
3.16 K	3.50	1110	139	42.8
5.62 K	3.75	1110	139	42.8
10 K	4.00	1110	139	42.8
17.8 K	4.25	1110	139	42.8
31.6 K	4.50	1110	139	42.8
56.2 K	4.75	1110	139	42.8
100 K	5.00	1110	139	42.8
178 K	5.25	1110	139	42.8
316 K	5.50	1110	139	42.8
562 K	5.75	1140	143	43.1
1 M	6.00	1110	139	42.8
1.78 M	6.25	1050	131	42.4
3.16 M	6.50	1050	131	42.4
5.62 M	6.75	1020	128	42.1
10 M	7.00	870	109	40.7
17.8 M	7.25	720	90.0	39.1
31.6 M	7.50	200	25.0	28.0
56.2 M	7.75	80	10.0	20.0

C.3.2 Signal Amplifier Bode Plot



D. SIGNAL PREAMP

D.1 Schematic



D.2 Circuit Description

The signal preamplifier consists of an operational amplifier (U401) connected in a transresistive topology that provides a voltage output for a current input. The feedback resistor (R401) sets the gain at 10 V / μA while the output buffer (U402) provides enhanced output drive capabilities. This output stage is capable of driving a 50 Ω line $\pm$ 10 V with slew rates approaching 2000 V / μs. The circuit is constructed on a teflon printed circuit board to minimize leakage currents and is placed in an radio frequency shielded box as as shown in Figure 19 on page 71.

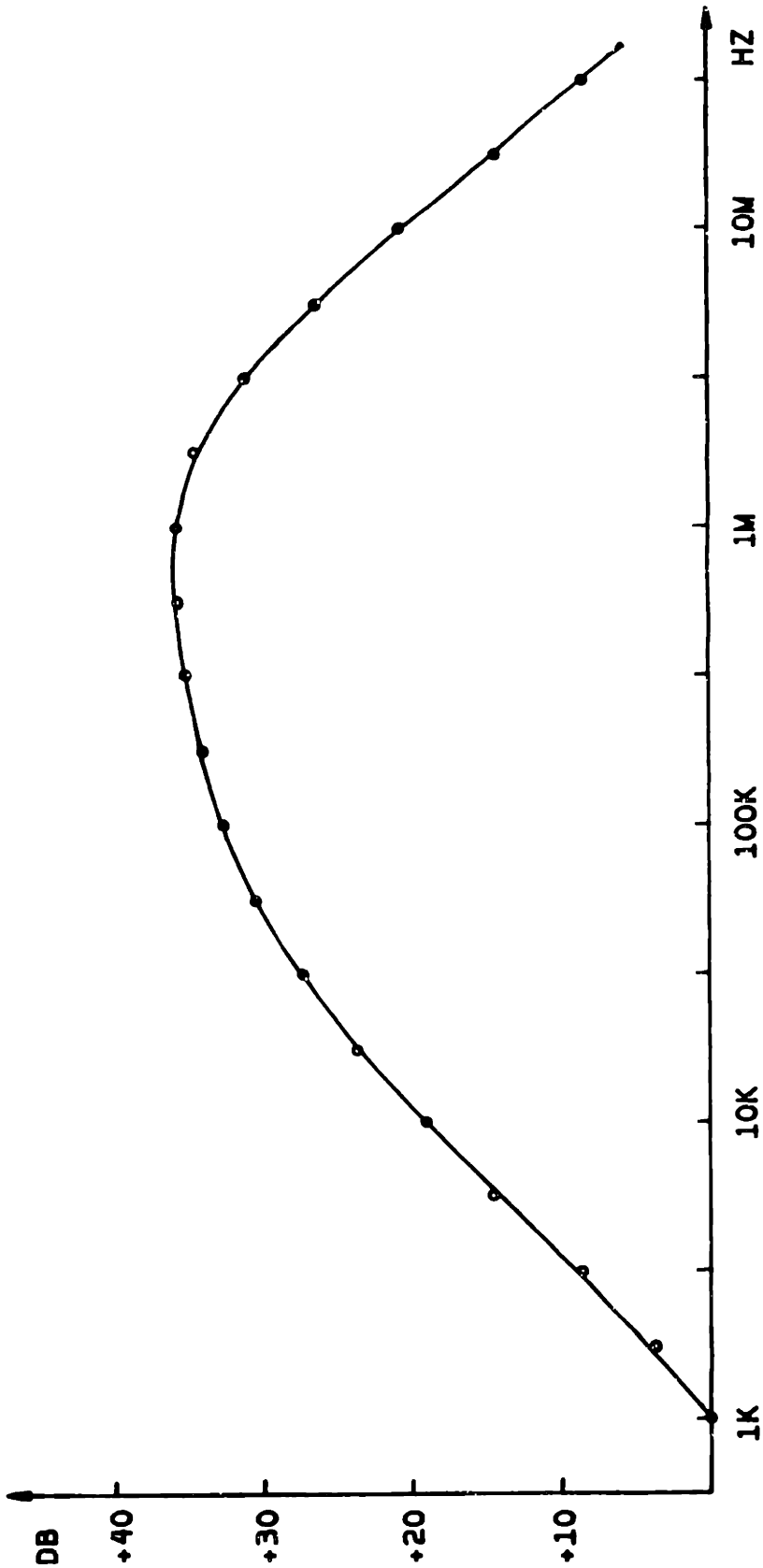
D.3 Signal Preamplifier Measured Frequency Response

D.3.1 Frequency Response Data

$C_1 = 15$ pF
$C_2 = \infty$
$V_I = 10$mV Sine wave

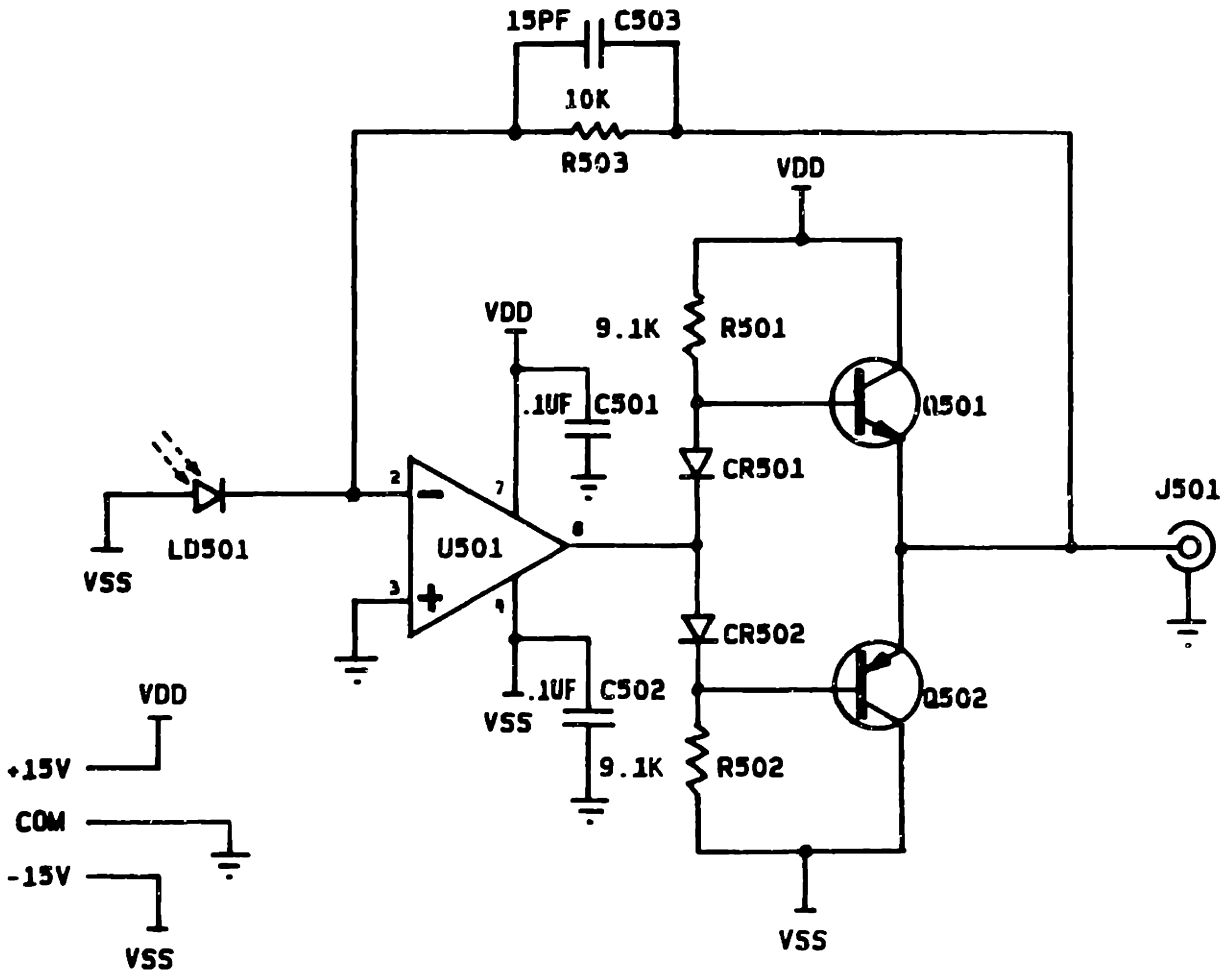
f hz	log f	Vout mV	Gain V/V	Gain db
1 K	3.00	10	1.0	0
1.78 K	3.25	16	1.6	3.9
3.16 K	3.50	28	2.8	8.9
5.62 K	3.75	53	5.3	14.5
10 K	4.00	89	8.9	19.0
17.8 K	4.25	155	15.5	23.8
31.6 K	4.50	229	22.9	27.2
56.2 K	4.75	331	33.1	30.4
100 K	5.00	427	42.7	32.6
178 K	5.25	501	50.1	34.0
316 K	5.50	569	56.9	35.1
562 K	5.75	610	61.0	35.7
1 M	6.00	624	62.4	35.9
1.78 M	6.25	525	52.5	34.4
3.16 M	6.50	359	35.9	31.1
5.62 M	6.75	211	21.1	26.5
10 M	7.00	110	11.0	20.8
17.8 M	7.25	51	5.1	14.1
31.6 M	7.50	26	2.6	8.2

D.3.2 Signal Amplifier Bode Plot



E. POSITION GRATING PREAMP

E.1 Schematic



E.2 Circuit Description

The grating photodiode is operated in the photoconductive mode for high speed operation. It is reverse biased at - 15 V and the resulting photocurrent is connected to a transresistive or current to voltage converter to produce the desired voltage output. The feedback resistor (R503) sets the gain to 10 V / mA while the feedback capacitor (C503) compensates for the large junction capacitance of the photodiode. The output drive buffer (Q501, Q502) provides a very low impedance output so that the preamp can drive a 50 Ω line at the speeds of interest. The output will have a DC offset due to the dark current of the photodiode but this is removed at the input to the next stage.

G. ELECTRONICS PARTS LIST

CR 1	Semicond. Device : Silicon, 200 V, 1.5A	1N4818
CR 2	Semicond. Device : Silicon, 200 V, 1.5A	1N4818
CR 3	Semicond. Device : Silicon, 200 V, 1.5A	1N4818
CR 4	Semicond. Device : Silicon, 200 V, 1.5A	1N4818
CR 5	Semicond. Device : Silicon, 200 V, 1.5A	1N4818
CR 6	Semicond. Device : Silicon, 200 V, 1.5A	1N4818
CR 7	Semicond. Device : Silicon, 200 V, 1.5A	1N4818
CR 201	Semicond. Device : Silicon, 100 V, 100 mA	1N914
CR 202	Semicond. Device : Silicon, 100 V, 100 mA	1N914
CR 203	Semicond. Device : LED, Panel Mount	
CR 501	Semicond. Device : Silicon, 100 V, 100 mA	1N914
CR 502	Semicond. Device : Silicon, 100 V, 100 mA	1N914

C 3	Capacitor, Fixed, Electrolytic : 100 μF, 20%, 50 V
C 4	Capacitor, Fixed, Solid Tantalum : 0.22 μF, 20%, 35 V
C 5	Capacitor, Fixed, Solid Tantalum : 0.1 μF, 20%, 35 V
C 6	Capacitor, Fixed, Electrolytic : 100 μF, 20%, 50 V
C 7	Capacitor, Fixed, Solid Tantalum : 2.2 μF, 20%, 35 V
C 8	Capacitor, Fixed, Solid Tantalum : 1 μF, 20%, 35 V
C 9	Capacitor, Fixed, Electrolytic : 50 μF, 20%, 50 V
C 11	Capacitor, Fixed, Electrolytic : 50 μF, 20%, 50 V
C 13	Capacitor, Fixed, Electrolytic : 50 μF, 20%, 50 V
C 15	Capacitor, Fixed, Electrolytic : 50 μF, 20%, 50 V
C 16	Capacitor, Fixed, Electrolytic : 100 μF, 20%, 50 V
C 17	Capacitor, Fixed, Solid Tantalum : 0.22 μF, 20%, 35 V
C 18	Capacitor, Fixed, Solid Tantalum : 0.1 μF, 20%, 35 V
C 19	Capacitor, Fixed, Electrolytic : 50 μF, 20%, 50 V
C 201	Capacitor, Fixed, Solid Tantalum : 1 μF, 20%, 35 V
C 202	Capacitor, Fixed, Ceramic Disc : 0.001 μF, 20%, 100 V
C 203	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V
C 204	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V
C 205	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V
C 206	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V
C 207	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V
C 208	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V
C 209	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V
C 210	Capacitor, Fixed, Solid Tantalum : 1 μF, 20%, 35 V
C 211	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V
C 212	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V
C 213	Capacitor, Fixed, Mica Dipped : 330 pF, 1%, 100 V
C 214	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V
C 215	Capacitor, Fixed, Mica Dipped : 330 pF, 1%, 100 V

C 216	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V	
C 217	Capacitor, Fixed, Polystyrene : 0.033 μF, 5%, 100 V	
C 218	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V	
C 219	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V	
C 220	Capacitor, Fixed, Ceramic Disc : 330 pF, 20%, 100 V	
C 221	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V	
C 222	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V	
C 301	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V	
C 302	Capacitor, Fixed, Solid Tantalum : 10 μF, 20%, 35 V	
C 303	Capacitor, Fixed, Porcelain : 2.2 pF, 2%, 500 V	
C 304	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V	
C 305	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V	
C 306	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V	
C 307	Capacitor, Fixed, Solid Tantalum : 10 μF, 20%, 35 V	
C 308	Capacitor, Fixed, Porcelain : 2.2 pF, 2%, 500 V	
C 309	Capacitor, Fixed, Mica Dipped : 15000 pF, 1%, 100 V	
C 310	Capacitor, Fixed, Mica Dipped : 1500 pF, 1%, 100 V	
C 311	Capacitor, Fixed, Mica Dipped : 150 pF, 1%, 100 V	
C 312	Capacitor, Fixed, Mica Dipped : 15 pF, 1%, 100 V	
C 313	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V	
C 314	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V	
C 315	Capacitor, Fixed, Porcelain : 2.2 pF, 2%, 500 V	
C 316	Capacitor, Variable, Ceramic : 2 - 8 pF, 200 V	
C 317	Capacitor, Fixed, Ceramic Disc : 470 pF, 20%, 100 V	
C 318	Capacitor, Fixed, Solid Tantalum : 1 μF, 20%, 35 V	
C 319	Capacitor, Fixed, Ceramic Disc : 470 pF, 20%, 100 V	
C 320	Capacitor, Fixed, Solid Tantalum : 1 μF, 20%, 35 V	
C 401	Capacitor, Fixed, Ceramic Disc : 470 pF, 20%, 100 V	
C 402	Capacitor, Fixed, Solid Tantalum : 1 μF, 20%, 35 V	
C 403	Capacitor, Fixed, Ceramic Disc : 470 pF, 20%, 100 V	
C 404	Capacitor, Fixed, Solid Tantalum : 1 μF, 20%, 35 V	
C 405	Capacitor, Fixed, Porcelain : 2.2 pF, 2%, 500 V	
C 501	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V	
C 502	Capacitor, Fixed, Ceramic Disc : 0.01 μF, 20%, 100 V	
C 503	Capacitor, Fixed, Mica Dipped : 15 pF, 1%, 100 V	
J 401	Connector, BNC, Male	
J 501	Connector, BNC, Male	
LD 501	Semicond. Device : Silicon, Quantrad Linear Photodiode	LL-6E
Q 301	Transistor : Silicon, Switching, NPN	2N3904
Q 302	Transistor : Silicon, Switching, NPN	2N3904
Q 501	Transistor : Silicon, Switching, NPN	2N3904

Q 502	Transistor : Silicon, Switching, PNP	2N3906

R 3	Resistor, Fixed, Cmpsn. : 510Ω, 5%, 0.5 W
R 4	Resistor, Fixed, Cmpsn. : 33Ω, 5%, 0.5 W
R 5	Resistor, Fixed, Cmpsn. : 510Ω, 5%, 0.5 W
R 6	Resistor, Variable, Trimmer : 1 KΩ, 0.25 W
R 7	Resistor, Fixed, Cmpsn. : 510Ω, 5%, 0.5 W
R 8	Resistor, Fixed, Cmpsn. : 430Ω, 5%, 0.5 W
R 9	Resistor, Variable, Trimmer : 2 KΩ, 0.25 W
R 10	Resistor, Fixed, Cmpsn. : 430Ω, 5%, 0.5 W
R 11	Resistor, Fixed, Cmpsn. : 100Ω, 5%, 0.5 W
R 12	Resistor, Fixed, Cmpsn. : 220Ω, 5%, 0.5 W
R 13	Resistor, Fixed, Cmpsn. : 220Ω, 5%, 0.5 W
R 14	Resistor, Fixed, Cmpsn. : 510Ω, 5%, 0.5 W
R 15	Resistor, Fixed, Cmpsn. : 33Ω, 5%, 0.5 W
R 16	Resistor, Fixed, Cmpsn. : 470Ω, 5%, 0.5 W
R 201	Resistor, Variable, Panel : 10 KΩ, 0.25%, 0.5 W
R 202	Resistor, Fixed, Cmpsn. : 1 KΩ, 5%, 0.25 W
R 203	Resistor, Fixed, Film : 100 KΩ, 1%, 0.25 W
R 204	Resistor, Fixed, Film : 100 KΩ, 1%, 0.25 W
R 205	Resistor, Fixed, Film : 100 KΩ, 1%, 0.25 W
R 206	Resistor, Fixed, Film : 100 KΩ, 1%, 0.25 W
R 207	Resistor, Variable, Trimmer : 10 KΩ, 0.25 W
R 208	Resistor, Variable, Trimmer : 1 KΩ, 0.25 W
R 209	Resistor, Variable, Trimmer : 10 KΩ, 0.25 W
R 210	Resistor, Fixed, Cmpsn. : 10 KΩ, 5%, 0.25 W
R 211	Resistor, Fixed, Cmpsn. : 68 KΩ, 5%, 0.25 W
R 212	Resistor, Fixed, Cmpsn. : 1 KΩ, 5%, 0.25 W
R 213	Resistor, Fixed, Cmpsn. : 51Ω, 5%, 0.5 W
R 214	Resistor, Fixed, Cmpsn. : 100 KΩ, 5%, 0.25 W
R 215	Resistor, Fixed, Cmpsn. : 100 KΩ, 5%, 0.25 W
R 216	Resistor, Fixed, Cmpsn. : 51Ω, 5%, 0.25 W
R 217	Resistor, Fixed, Cmpsn. : 15 KΩ, 5%, 0.25 W
R 218	Resistor, Variable, Trimmer : 20 KΩ, 0.25 W
R 219	Resistor, Fixed, Cmpsn. : 220Ω, 5%, 0.25 W
R 220	Resistor, Variable, Trimmer : 10 KΩ, 0.25 W
R 221	Resistor, Fixed, Cmpsn. : 10 KΩ, 5%, 0.25 W
R 222	Resistor, Fixed, Cmpsn. : 10 KΩ, 5%, 0.25 W
R 223	Resistor, Fixed, Cmpsn. : 10 KΩ, 5%, 0.25 W
R 224	Resistor, Fixed, Cmpsn. : 1.2 KΩ, 5%, 0.25 W
R 225	Resistor, Fixed, Film : 100 KΩ, 1%, 0.25 W
R 226	Resistor, Fixed, Film : 100 KΩ, 1%, 0.25 W
R 227	Resistor, Variable, Trimmer : 20 KΩ, 0.25 W
R 228	Resistor, Fixed, Cmpsn. : 1 KΩ, 5%, 0.25 W

R 229	Resistor, Variable, Trimmer : 100 KΩ, 0.25 W	
R 301	Resistor, Fixed, Cmpsn. : 100Ω, 5%, 1 W	
R 302	Resistor, Fixed, Cmpsn. : 100Ω, 5%, 1 W	
R 303	Resistor, Fixed, Film : 562Ω, 1%, 0.25 W	
R 304	Resistor, Fixed, Film : 8.45 KΩ, 1%, 0.25 W	
R 305	Resistor, Fixed, Film : 3.65 KΩ, 1%, 0.25 W	
R 306	Resistor, Fixed, Film : 25.5 KΩ, 1%, 0.25 W	
R 307	Resistor, Fixed, Cmpsn. : 4.7Ω, 5%, 0.25 W	
R 308	Resistor, Fixed, Cmpsn. : 4.7Ω, 5%, 0.25 W	
R 309	Resistor, Fixed, Film : 562Ω, 1%, 0.25 W	
R 310	Resistor, Fixed, Film : 8.45 KΩ, 1%, 0.25 W	
R 311	Resistor, Fixed, Film : 3.65 KΩ, 1%, 0.25 W	
R 312	Resistor, Fixed, Film : 8.45 KΩ, 1%, 0.25 W	
R 313	Resistor, Fixed, Film : 9.09 KΩ, 1%, 0.25 W	
R 314	Resistor, Fixed, Film : 4.53 KΩ, 1%, 0.25 W	
R 315	Resistor, Fixed, Film : 5.49 KΩ, 1%, 0.25 W	
R 316	Resistor, Fixed, Film : 2.49 KΩ, 1%, 0.25 W	
R 317	Resistor, Fixed, Film : 3.16 KΩ, 1%, 0.25 W	
R 318	Resistor, Fixed, Film : 1.77 KΩ, 1%, 0.25 W	
R 319	Resistor, Fixed, Cmpsn. : 10 KΩ, 5%, 0.25 W	
R 320	Resistor, Variable, Trimmer : 1 KΩ, 0.25 W	
R 321	Resistor, Fixed, Cmpsn. : 3.3 KΩ, 5%, 0.25 W	
R 322	Resistor, Fixed, Cmpsn. : 1.5 KΩ, 5%, 0.25 W	
R 323	Resistor, Fixed, Film : 1 KΩ, 1%, 0.25 W	
R 324	Resistor, Fixed, Film : 4.99 KΩ, 1%, 0.25 W	
R 401	Resistor, Fixed, Cmpsn. : 10 MΩ, 5%, 0.25 W	
R 501	Resistor, Fixed, Cmpsn. : 9.1 KΩ, 5%, 0.125 W	
R 502	Resistor, Fixed, Cmpsn. : 9.1 KΩ, 5%, 0.125 W	
R 503	Resistor, Fixed, Cmpsn. : 10 KΩ, 5%, 0.125 W	

U 1	Integrated Circuit, Linear : Voltage Regulator, 15 V, 1.5 A	LM7815CT
U 2	Integrated Circuit, Linear : Voltage Regulator, -15 V, 1.5 A	LM7915CT
U 3	Integrated Circuit, Linear : Voltage Regulator, 5 V, 1.5 A	LM7805CT
U 201	Integrated Circuit, Linear : Operational Amplifier	LF356N
U 202	Integrated Circuit, Linear : Operational Amplifier	LF356N
U 203	Integrated Circuit, Linear : Operational Amplifier	LF356N
U 204	Integrated Circuit, Linear : Comparator	LM311N
U 205	Integrated Circuit, Digital : Quad Line Driver	SN74128N
U 206	Integrated Circuit, Linear : Comparator	μA760DC
U 207	Integrated Circuit, Digital : One Shot	SN74LS123N
U 208	Integrated Circuit, Digital : Dual Flip Flop	SN74LS74N
U 209	Integrated Circuit, Digital : Quad AND Gate	SN7408N
U 210	Integrated Circuit, Digital : Hex O.C. Not Gate	SN7406N
U 211	Integrated Circuit, Digital : One Shot	SN74121N

U 212	Integrated Circuit, Digital : Quad CMOS Switch	CD4066BC
U 213	Integrated Circuit, Linear : Voltage Reference	AD581JH
U 214	Integrated Circuit, Linear : Operational Amplifier	LF356N
U 215	Integrated Circuit, Linear : Operational Amplifier	LF356N
U 301	Integrated Circuit, Linear : Operational Amplifier	LM359N
U 302	Integrated Circuit, Linear : Operational Amplifier	BB3554AM
U 303	Integrated Circuit, Linear : Operational Amplifier	BB3553BM
U 401	Integrated Circuit, Linear : Operational Amplifier	BB3554AM
U 402	Integrated Circuit, Linear : Operational Amplifier	BB3553BM
U 501	Integrated Circuit, Linear : Operational Amplifier	LF356N
VR 1	Semicond. Device : Zener, 1 W, 20 V, 5%	1N4747A
VR 2	Semicond. Device : Zener, 1 W, 20 V, 5%	1N4747A
VR 3	Semicond. Device : Zener, 1 W, 7.5 V, 5%	1N4737A
VR 4	Semicond. Device : Zener, 1 W, 7.5 V, 5%	1N4737A
VR 5	Semicond. Device : Zener, 5 W, 3.9 V, 5%	1N5335B

BIBLIOGRAPHICAL NOTE

Robert Stephen Olyha, Jr. *21 Cliff Avenue, Yonkers, New York 10705-2209.* Mr. Olyha has been enrolled in the Massachusetts Institute of Technology Electrical Engineering and Computer Science department's cooperative education program since May 1981. His co-op assignment was with Central Scientific Services, I.B.M. Thomas J. Watson Research Center, Yorktown Heights, New York, working in the Electronic Engineering Group. He became involved with the surface photovoltage tool during the summer of 1982 and continued on after May 1983, which became the basis of this thesis research. Upon completion of his S.B. and S.M. degrees in May 1984, Mr. Olyha will be joining I.B.M. and continuing work on semiconductor material characterization. His main interests are high performance analog instrumentation and numerical circuit analysis. Mr. Olyha is a student member of the I.E.E.E. and a member of Eta Kappa Nu.

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