Modulated Frequency Multiplier Inverter

by

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B.S. Electrical Engineering and Computer Science, MIT, 2023

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

MASTER OF ENGINEERING IN ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

May 2024

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ABSTRACT

Many industrial applications such as plasma generation and wireless power transfer require high frequency power inverters (or rf power amplifiers) that are able to output a wide power range despite highly variable load reactances, while also maintaining high efficiency. Previous approaches to this problem, such as switched-mode inverters combined with tunable matching networks provide adequate, albeit bulky, costly, and complex solutions at lower HF frequencies, while at higher frequencies inefficient linear amplifiers dominate. This thesis introduces an efficient inverter (or switched-mode power amplifier) approach that can provide efficient wide-power-range control into a variable load, while being scalable to increased output frequencies compared to conventional designs. We introduce a wide-range power amplifier that uses frequency control to manage reactive load variations, and phase modulation to modulate output power, and frequency multiplication to achieve high output frequency, all while maintaining soft switching. The proposed thesis provides a preliminary development of this modulated frequency multiplier inverter, analyzing and demonstrating it functionality and effectiveness through simulation, showing its ability to achieve high output frequencies, manage wide load reactances, control power over a wide range, and maintain a high efficiency.

Thesis supervisor: David J. Perreault
Title: Ford Professor of Engineering,

Acknowledgments

I would like to give a big thank you to Professor Perreault for being a wonderful teacher and mentor. I'd also like to thank Mansi Joisher and Rachel Yang for answering my countless questions and for their constant warmth and joy. Lastly, I'd like to thank everyone in the LEES group for being so welcoming and embracing me in the group. I hope to see you all soon!

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Chapter 1

Introduction

High frequency power amplifiers are crucial for a variety of applications, particularly plasma generation, wireless power transfer, battery chargers, induction heating, dc-dc converters, RF welding, and more. These applications require a number of criteria for the converters, namely that they must operate at high frequency (HF, 3-30MHz), or very high frequency (VHF, 30-300MHz) control output power over a wide range into highly variable loads and, to the extent possible, operate at high efficiency. Meeting all these criteria is challenging and more often than not, efficiency is sacrificed to meet the other design metrics, yielding inefficient and bulky designs. Compared to prior designs, new switched-mode frequency multiplier topologies can achieve increased output frequency (relative to device switching frequency) and efficiently and rapidly control power over a wide range into a variable load impedance. The proposed modulated frequency multiplier uses frequency modulation and beta (or phase) modulation to control power delivered to the load. Additionally, it uses the frequency modulation to manage load reactance variations. This design is able to do all this efficiently by also implementing zero-voltage soft switching for all switches, and uses frequency multiplication to operate the switches at half the output frequency, thereby further lowering the frequency-dependent switching losses.

Chapter 2

Related Work

Previous works that address the need for a highly efficient inverter capable of rapid power and response to a wide load impedance range include more complex architectures such as the combination of several HF inverters with a power combining network or an HF inverter connected to a tunable impedance matching network. The proposed design is inspired by the recently proposed wide-range switched-mode amplifier [4].

2.1 HF Inverter with Tunable Impedance Matching Network

One commonly used approach is to cascade a conventional HF inverter designed for a single load impedance (usually 50 ohms) with a tunable matching network (TMN) that dynamically matches the variable load impedance to the desired load impedance of the inverter as in [1-3]. Tunable matching with high speed can be accomplished through phase-switched impedance modulation (PSIM) which modulates the effective impedances seen looking into the terminals of passive elements at the RF operating frequency by adjusting the phase and/or duty cycle of a switch. While some TMNs such as that demonstrated in [1] provide accurate and fast impedance matching over a wide impedance range, TMNs are nonetheless commonly bulky, expensive, and inefficient, thereby creating a clear need for a converter that is able to deliver RF power without the need for a separate TMN.

2.2 HF Inverter for Variable Load Operation

An alternative approach to this design problem, compared to the previous, is the use of two HF inverters with independently controllable amplitude and phase connected to one another and to the load through a lossless power combining immittance network [6]. Varying the amplitude and relative phase of the inverters keeps the impedance seen by each within a desired range regardless of load variations. The immittance network is comprised of several reactive elements in parallel and transforms the capacitive reactance that cannot be driven by the inverters into inductive loads that can. It also converts a voltage applied to one port into a current out of the other port. The inverters can be highly efficient converters that are

able to implement zero-voltage soft switching such as Class D or E amplifiers, though supply modulation (or "envelope tracking) of the inverters is needed as well. While this approach requires no variable reactive components or additional changes to the load as the previous approach necessitates, this design is limited by its complexity, large number of magnetics, and high-bandwidth power supply modulations, which not only add cost and take up board space, but also can limit efficiency. Thus a converter that is able to simultaneously provide a wide output power to a highly variable load range while also maximizing efficiency and using a simple design with minimum magnetics or additional circuitry Would be desirable.

2.3 Wide-Range Switched-Mode Power Amplifier

One of the most recent approaches to this problem whose functionality surpasses both aforementioned designs is the wide-range switch-mode power amplifier [4]. This design is based on a voltage mode class-D power amplifier. It uses a version of phase, or β, control to control the fundamental rf output amplitude, and dynamic frequency tuning (DFT) is used to address load reactance variations. One implementation of this converter generates a square wave that is then "chopped" based on the control angle β, resulting in a second waveform of controllable pulse width. An LC tank extracts the fundamental of this chopped square wave and delivers it to the load. To manage load reactance variations, frequency modulation (FM, sometimes also called dynamic frequency tuning, or DFT) is used to keep the net reactance of the combined tank and load constant. This constant value is used to make the tank and output network appear inductive, so as to achieve zero-voltage switching (ZVS) through the load. Another inductor is used to achieve ZVS of the other switches in the network. While this power amplifier provides a simpler structure than both approaches previously described, there is a desire to improve upon the converter's efficiency, eliminate complexity and loss, and achieve higher output frequencies, and provide a wider available range of output power control. Towards this end, this thesis introduces a modulated frequency multiplier approach that is inspired by the wide-range switched-mode power amplifier.

Chapter 3

Relevant Concepts and Challenges in High Frequency Inverter Design

3.1 Single-Ended Half-Bridge Resonant Inverter

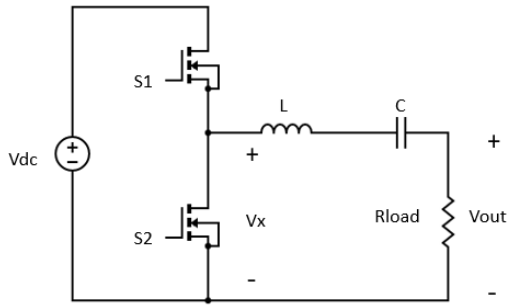


Figure 3.1: Single-ended series resonant inverter topology

This work builds upon the single-ended “class-D" half-bridge resonant inverter [5] which consists of a half bridge switching network connected to a resonant filter network (LC tank) and a load (illustrated here as a resistor, but possibly including a reactive component of load impedance). The half bridge synthesizes an approximately square-wave voltage v_x from which the LC tank then extracts the fundamental which is delivered to the load. The load network is connected between the switching node and ground, or between the switching node and two large blocking capacitors which are each large enough to hold an approximately constant voltage $\frac{V_{dc}}{2}$. The former is depicted in Fig. 3.1. The LC tank and load resistor look like a series RLC circuit. With the output voltage taken across the load resistor, the RLC circuit acts as a bandpass filter, selecting a narrow frequency range (in this case, the fundamental) such that the power is delivered at the selected frequency.

3.1.1 Frequency Modulation

One of the common control methods used to address load reactance variations is frequency modulation (sometimes also referred to as "dynamic frequency tuning". Consider a load impedance $Z_{load} = R_{load} + j\omega L_{load}$.

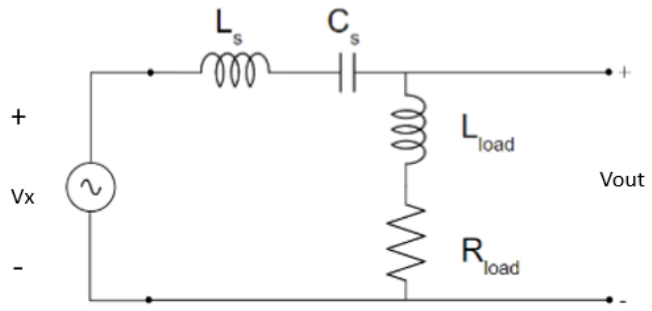


Figure 3.2: LC tank and real and reactive load

The net reactance of the LC tank and the load is:

$$X_{net} = \omega L - \frac{1}{\omega C} + \omega L_{load}$$

where ω is the switching frequency in rad/sec

In order for the output power to not change with variations in the load reactance, X_{net} must be kept constant. Therefore, as seen in the equation above, if L_{load} varies, X_{net} can be maintained at a specified value by changing ω. For example, X_{net} can either be kept at 0 if it were desired to maximize the load current (with the circuit driven on resonance, that is $\omega_{sw} = \omega_o$). In this case, the impedances of the inductor and capacitor cancel making the current depend solely on R. Alternatively, frequency can be controlled to maintain X_{net} at a non-zero value for reasons discussed below.

Frequency modulation can also be used as a method of controlling the output power. As shown in Fig. 3.3, if the tank is driven slightly off resonance, the LC filter either looks like a small inductor or a large capacitor at the operating frequency ω. If driven above resonance, this additional inductive reactance impedance posed by the series LC network reduces the magnitude of the voltage across the load. The reason for this is the LC tank and load can be thought of as a voltage divider where V_{out} falls across the load. $V_{out} = V_x \frac{Z_{load}}{Z_{load}+Z_{tank}}$ where $Z_{load} = R$ and $Z_{tank} = j\omega L - \frac{1}{j\omega C}$. So as we increase the switching frequency, Z_{tank} also increases, which in turn decreases V_{out}.

If the quality factor, Q_o of the output network is high then we are able to achieve a large change in output power with only a small change in the switching frequency. This is possible because a high Q means a large peak at resonance with a steep slope [5]. A steep admittance slope means that small changes in frequency result in large changes in the admittance. And large changes in admittance result in large changes in the output voltage as discussed above, this also results in large changes in the output power!

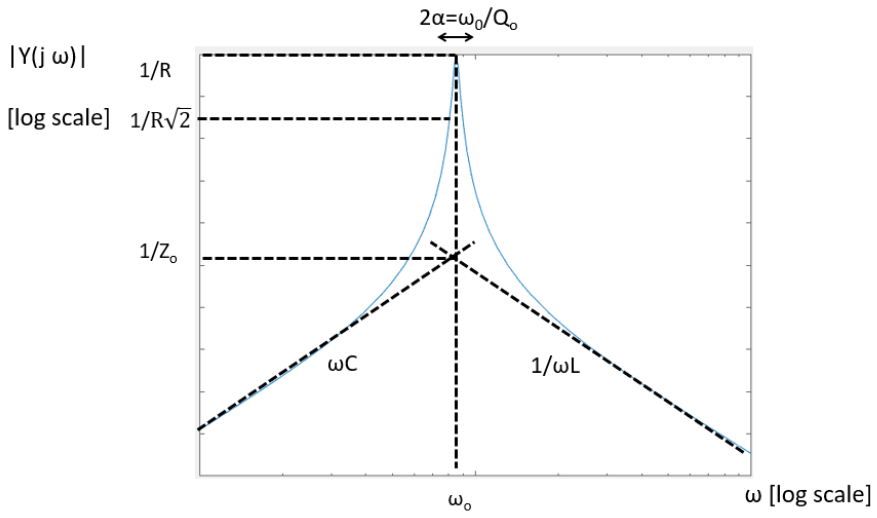


Figure 3.3: Series RLC admittance curve

Though we have described the case of operating above the resonant frequency, frequency modulation can be performed with below or above resonance operation. If operating below resonance it is possible for the third harmonic of the generated square wave to be relatively high, resulting in significant third harmonic content delivered to the load. If an output with low distortion is desired, this presents a problem. However, with above resonance operation, the harmonics are somewhat attenuated, but higher switching frequencies result in higher switching losses. So there are tradeoffs to both.

3.1.2 Zero-Voltage Soft Switching

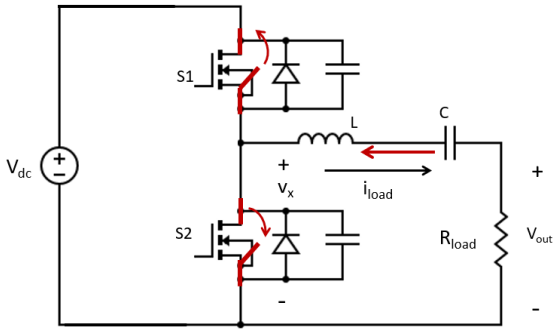


Figure 3.4: Single-ended resonant inverter v_x and i_{load} at duty cycle = 0.5.

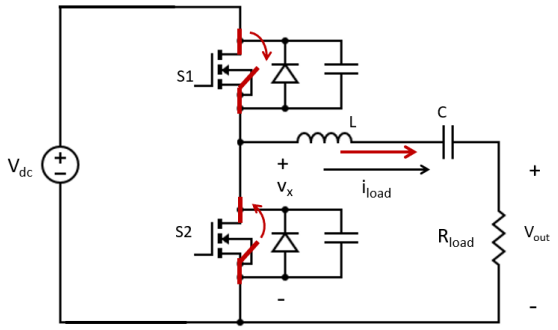


Figure 3.5: Single-ended resonant inverter v_x and i_{load} at duty cycle = 0.5.

In order to attain a high efficiency, resonant converters often implement zero voltage soft switching (ZVS). One option is to do this by tuning the load inductively (i.e. by operating above resonance for the series-resonant network). When switch 2 turns off and S1 turns on, the switch voltage v_x goes from low to high, therefore the load current must be negative in order to discharge switch 1's capacitor and charge switch 2's capacitor. When switch 1 turns off and switch 2 turns on, v_x goes from high to low, thus the load current must be positive. Looking at the case where the duty ratio is $\beta = \pi$, one can see that when the load is tuned inductively, the load current lags the voltage, thus at $\omega t = 0$, when v_x goes from low to high, the load current is appropriately negative, and at $\omega t = \pi$, when v_x goes from high to low, the load current is positive. This example is shown in Fig. 3.6.

Another option is to add an inductor L_{zvs} along with two blocking capacitors, C_{block},to achieve ZVS as shown in Fig. 3.7. The direction of i_{zvs} and i_{load} during each deadtime is shown in Fig. 3.8 and 3.9. The use of L_{zvs} to aid soft switching can be done in conjunction with or in place of tuning the load inductively.

The current i_{zvs} through this inductor L_{zvs} is triangular, reaching a negative maximum when v_x is transitioning from low to high, and reaching a positive maximum when v_x is

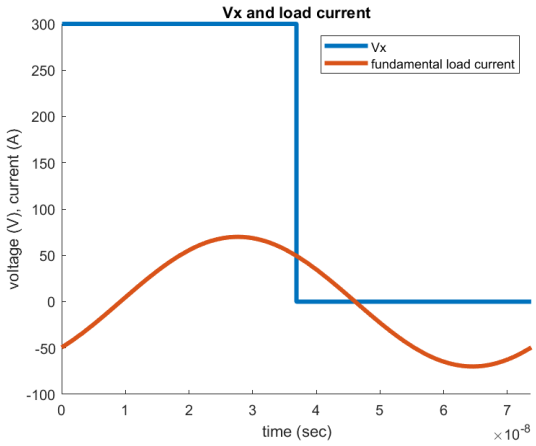


Figure 3.6: Single-ended resonant converter v_x and load current at duty cycle = 0.5, $V_{dc} = 300V$, and $f_{sw} = 6.78MHz$ for an inductively tuned load network

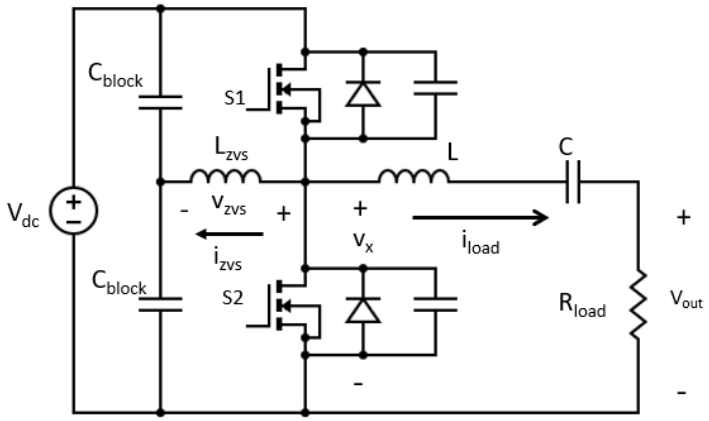


Figure 3.7: Single-ended resonant inverter with inductor for ZVS

transitioning from high to low. This is shown in Fig. 3.10. One benefit of this approach is that soft-switching is no longer dependent on the output current magnitude, meaning that load variations and output power modulation no longer have an impact on the converter's soft-switching functionality. Additionally, switching losses can be reduced because the current in L_{zvs} is triangular, the conduction losses due to i_{zvs} can be lower than if the load current alone is used.

If the load is tuned resistively, then the i_{zvs} current alone that contributes to ZVS as illustrated in Fig. 3.10. However, if the load is tuned inductively, it is the combination of the load current and current through L_{zvs} that enable soft switching of the two MOSFETs.

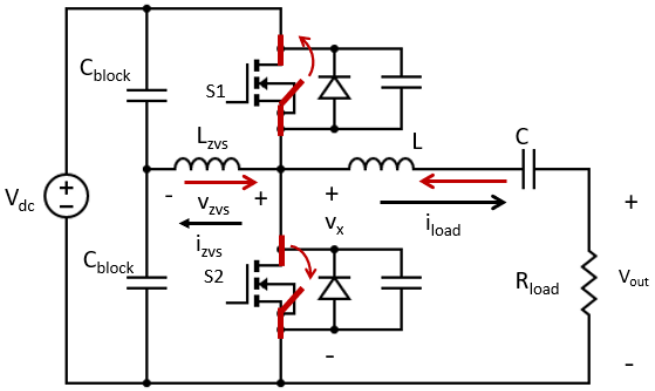


Figure 3.8: Single-ended resonant inverter deadtime

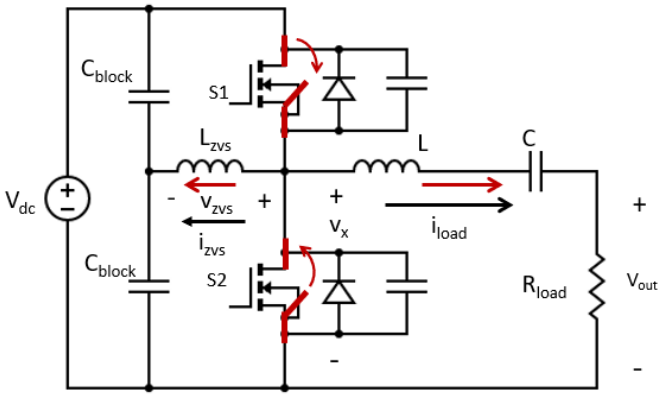


Figure 3.9: Single-ended resonant inverter deadtime

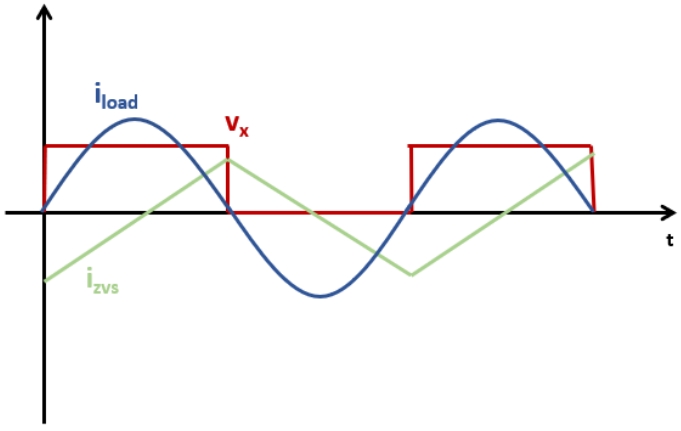
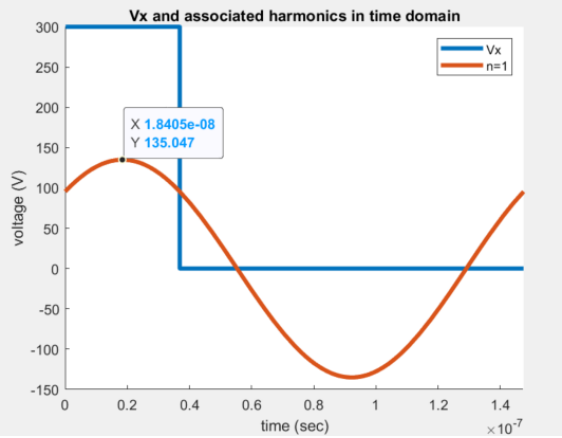


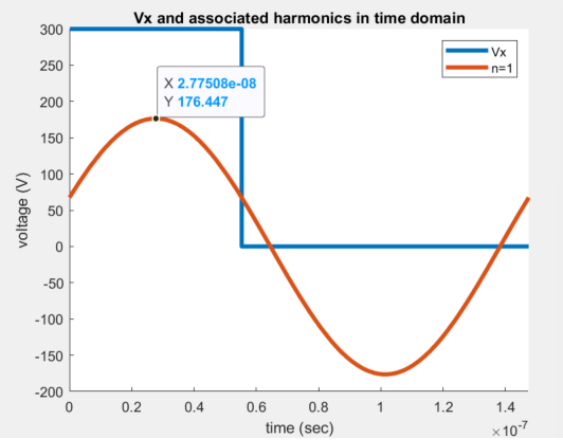
Figure 3.10: Single-ended resonant inverter v_x, i_{load}, and i_{zvs} for duty cycle = 0.5

3.1.3 Beta Modulation

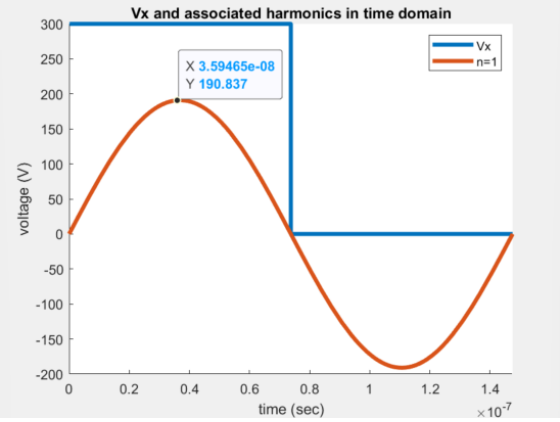
Phase control, or beta modulation, can also be used to control the power delivered to the load. By controlling the duty ratio with which the half-bridge is switched, or equivalently, the electrical angle, β, at which the switching transition takes place, the width of the synthesized voltage, v_x is modulated, which then controls the amplitude of the fundamental voltage and current across and through the load. This is shown in Fig. 3.11 as β is modulated from $\pi/2$ to π.



(a) $\beta = \frac{\pi}{2}$



(b) $\beta = \frac{3\pi}{4}$



(c) $\beta = \frac{3\pi}{2}$

Figure 3.11: Single-ended resonant converter v_x and fundamental component as β varies with $V_{dc} = 300V$ and $f_{sw} = 6.78MHz$.

One challenge to implementing beta modulation in a resonant inverter is maintaining ZVS, which is usually necessary for high-efficiency operation. In [4] this is achieved via the introduction of further switches and passive elements. In the simpler half-bridge structure, one cannot easily maintain ZVS over a wide output range. With beta modulation, a wide beta range is desired, ranging from a very small switching angle to a very large $\beta = \pi$, or operating from $\beta = \pi/2$ up to nearly π. At the extreme ends of the beta range, the switching edges of the half bridge are close together. In these extreme cases, the load current cannot be negative and positive, respectively, during both of v_x's transitions. This phenomenon can be seen in Fig. 3.12.

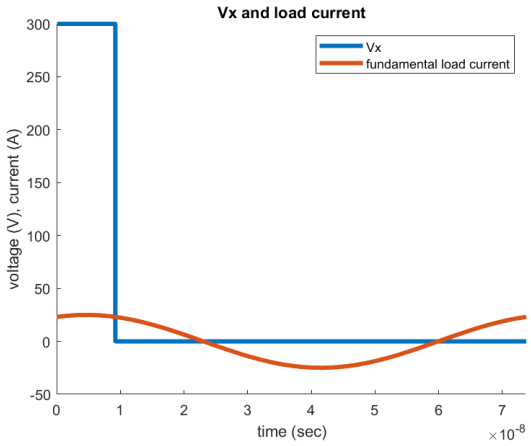
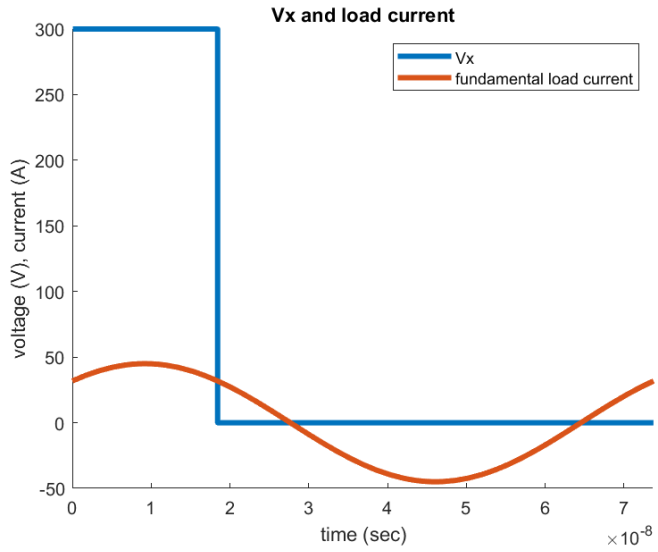
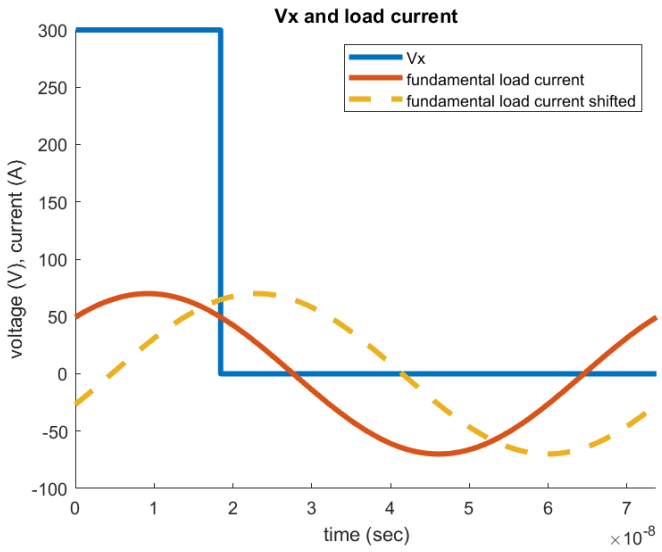


Figure 3.12: Single-Ended Resonant Converter V_x and Load Current at duty cycle = 0.125

The difficulty of realizing ZVS with large variations of switching angle (or duty ratio), as needed for a wide power control range, is a key reason this control technique is not conventionally used in half-bridge and similar resonant inverters.



(a)



(b)

Figure 3.13: Single-Ended Resonant Converter V_x and Load Current at duty cycle = 0.25

Even with the contribution for L_{zvs}, it can still be very challenging to achieve ZVS when implementing beta modulation. As shown in Fig. 3.14, when β is small, i_{zvs} has to go from negative to positive very quickly, so its $\frac{di}{dt}$ can be very high. In order to achieve a high $\frac{di}{dt}$, a large negative voltage must be placed across the inductor which is not always feasible in a design. The same thing occurs when β is very large, except i_{zvs} now has to go from positive to negative within a short period of time. As such, the challenges of implementing both these strategies is clear.

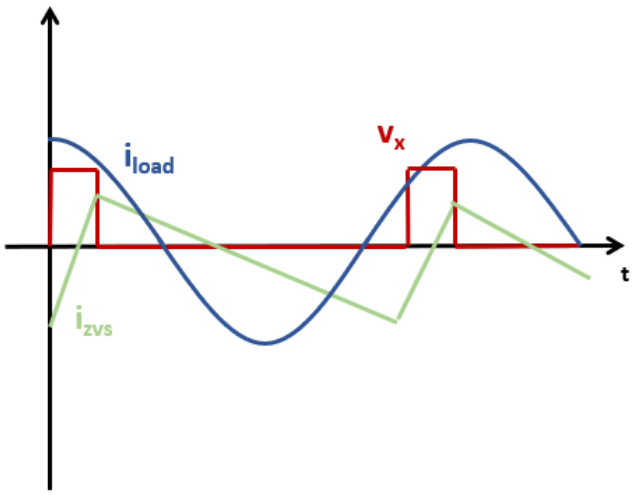


Figure 3.14: Single-ended resonant inverter v_x, i_{load}, and i_{zvs} for duty cycle < 0.5

Chapter 4

Single-Ended Direct Synthesis Frequency Multiplier

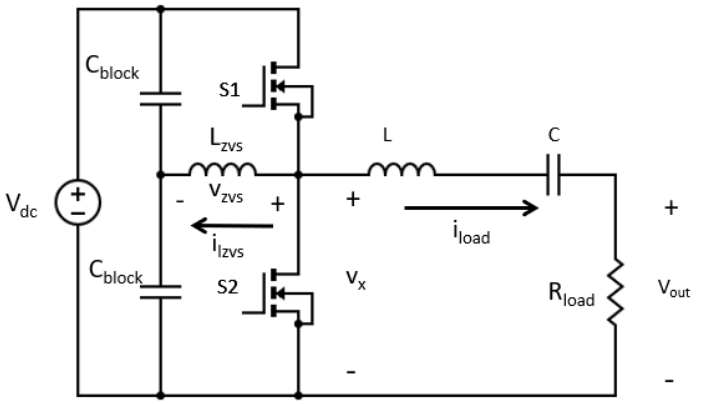


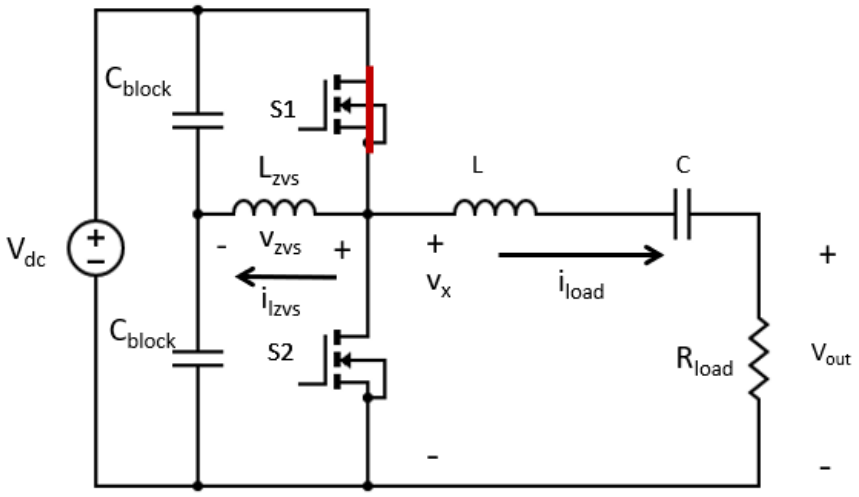
Figure 4.1: Single-ended direct synthesis frequency multiplier circuit topology

The single-ended direct synthesis frequency multiplier has the same topology of Fig. 3.1, which is identical to some versions of a half-bridge resonant inverter, albeit with different component values and tunings. However, it uses differently selected component values (especially the output tank) and different control techniques that allow it to provide different performance and controllability than a typical resonant inverter.

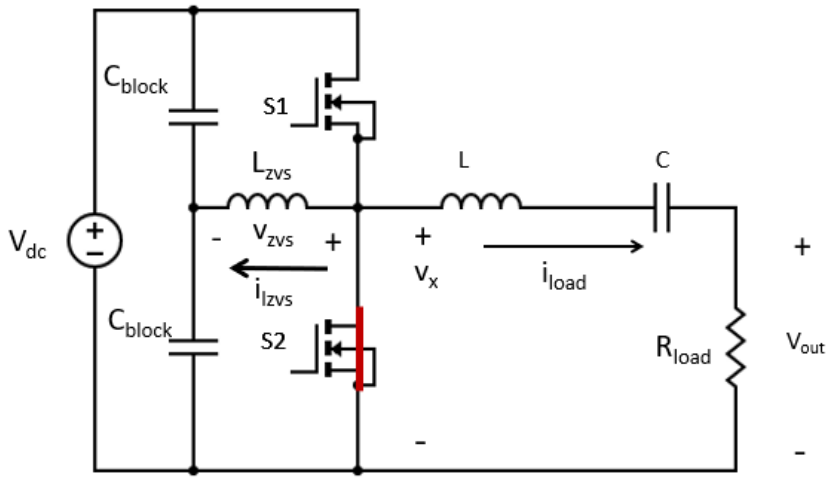
4.1 Idealized Operation

4.1.1 General Operation

The single ended frequency multiplier has the same switching scheme as the resonant converter. That is, S1 and S2 switch in a complementary fashion, generating a voltage V_x with a duty cycle expressed as β in electrical degrees. This operation is shown in Fig. 4.2 below (not including dead-time periods described later in association with Fig. 4.7).



(a) $0 \leq \omega t \leq \beta$



(b) $\beta \leq \omega t \leq 2\pi$

Figure 4.2: Ideal circuit operation of single-ended direct synthesis frequency multiplier inverter.

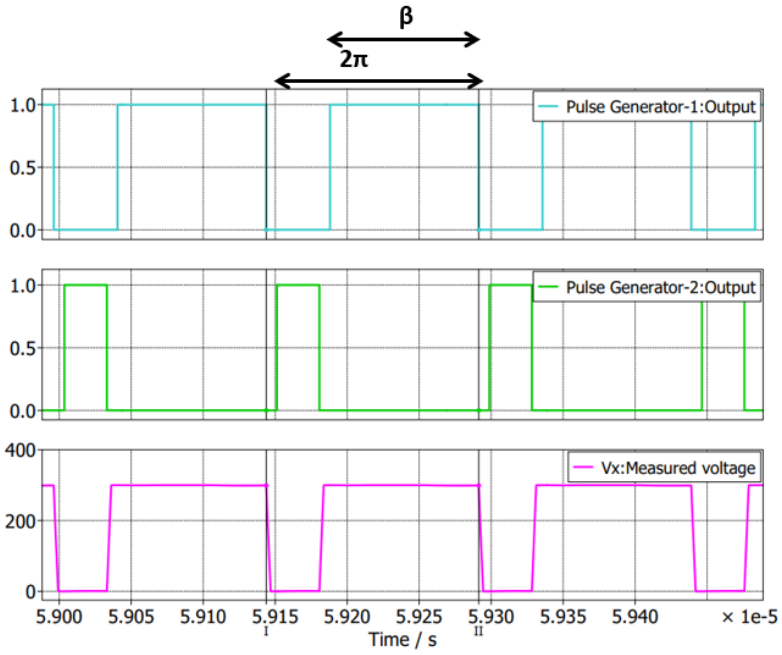


Figure 4.3: Single-ended direct synthesis frequency multiplier gate drive and v_x waveforms vs. time for the circuit implementation of Fig. 4.1 with simulation conditions as described in Table 4.1

However, while the LC tank of the typical resonant converter extracts the fundamental, the LC tank of the direct synthesis frequency multiplier extracts a harmonic frequency (e.g., the second harmonic in a frequency-doubler implementation). One benefit of doing this is it allows the converter to switch at a fraction (e.g. half) the output frequency, thereby reducing switching losses and achieving a higher output frequency than would otherwise be possible. The synthesized voltage v_x, along with the load current and voltage are shown in Fig. 4.4.

Parameter	Value
V_{dc}	300V
f_{sw}	6.78MHz
L_s	$2.35\mu H$
C_s	$58.7pF$
L_{zvs}	$0.25\mu H$
C_{block}	$5\mu F$
R_{load}	5 Ω
C_{sw}	80pF
$R_{ds,on}$	$42m\Omega$
β	$3\pi/2$
δ	.05

Table 4.1: PLECS simulation specifications for the single-ended direct frequency multiplier

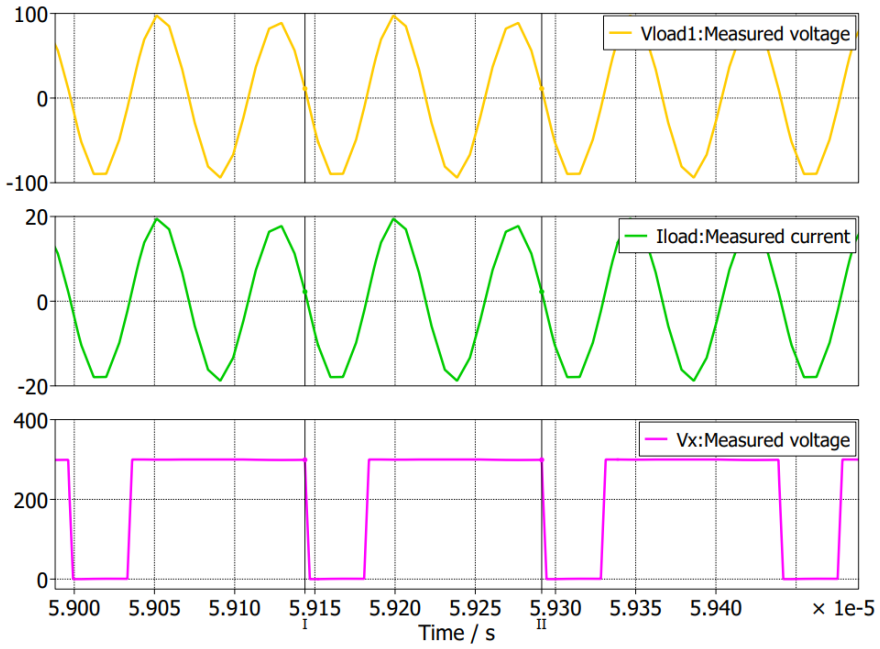


Figure 4.4: v_{load}, i_{load}, and v_x waveforms vs. time for the circuit implementation of Fig. 4.1 with simulation conditions as described in Table 4.1

4.1.2 Beta Modulation

The full range of achievable second harmonic in voltage v_x is achievable when β is varied over a limited range, such as π to $\frac{3\pi}{2}$. This range was selected by analyzing the magnitude and phase of the second harmonic of the square wave, as shown in Fig. 4.5. The second harmonic voltage is described by the following equation for a rectangular wave with its positive-going transition at $\omega t = 0$ and its negative-going transition at $\omega t = \beta$:

$$v_2(t) = \frac{V_{dc}}{\pi} sin(\beta) sin(2\omega t - \beta)$$

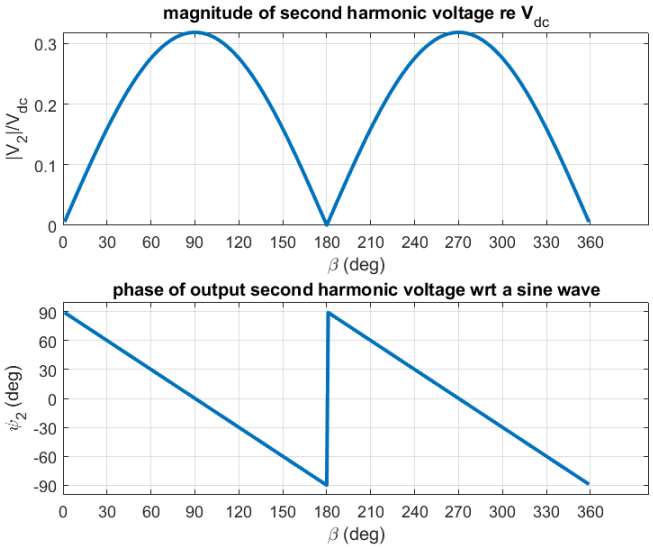
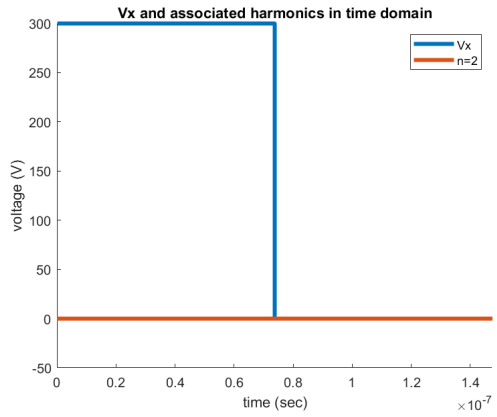
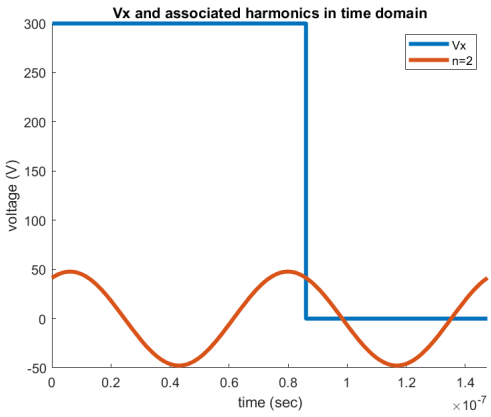


Figure 4.5: Magnitude and phase of the second harmonic wrt a sine wave

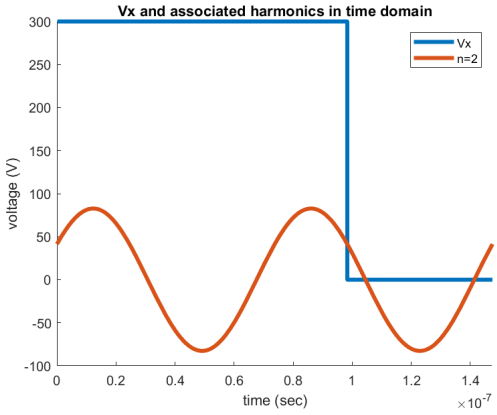
The magnitude is at a maximum and the phase is 0 degrees out of phase with a sine wave at $\omega t = \frac{3\pi}{2}$. Correspondingly, the magnitude is a minimum and the phase is 90 degrees at $\omega t = \pi$. Thus to achieve the widest range in second-harmonic amplitude possible we can modulate the switches with a duty cycle between π and $\frac{3\pi}{2}$. Alternatively, β could be modulated between $\pi/2$ and π, achieving the same results. An explanation of why the other two ranges, from 0 to $\pi/2$ and from $3\pi/2$ to 2π are not preferred will come later. Modulating β changes the width of v_x, thereby changing the amplitude and phase of the second harmonic as shown in Fig. 4.6.



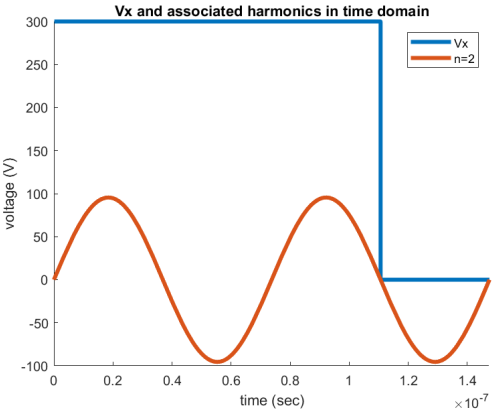
(a) $\beta = \pi$



(b) $\beta = \frac{4\pi}{3}$



(c) $\beta = \frac{7\pi}{6}$



(d) $\beta = \frac{3\pi}{2}$

Figure 4.6: v_x and its second harmonic as β is increased from π and $3\pi/2$ considering a dc bus voltage of $V_{dc} = 300$ and a switching frequency of 6.78MHz.

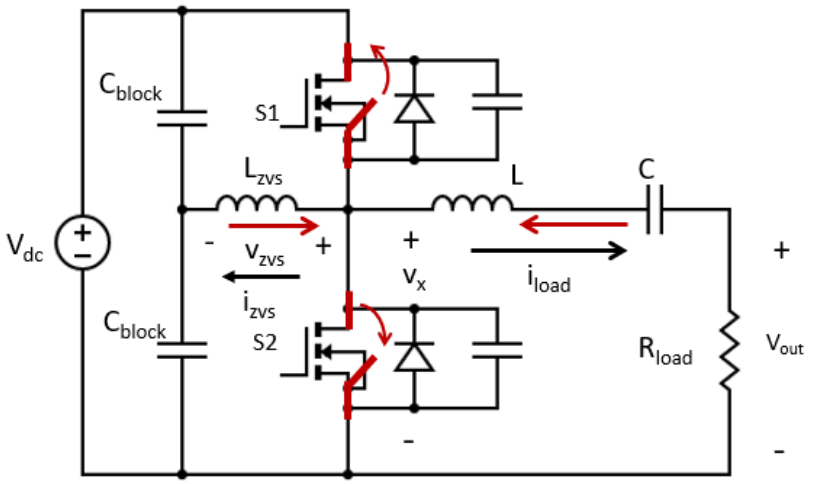
4.2 Practical Realization

In order for the converter to achieve high efficiency, zero voltage soft switching is needed to minimize switching losses, which means deadtimes must be inserted into the switching scheme, with appropriate currents in the switching transitions to achieve ZVS. The frequency multiplier achieves ZVS using the fundamental elements of v_x and v_{zvs}. Fig. 4.7 below shows the direction of current flow during the deadtimes illustrating how L_{zvs} is used to achieve ZVS for all switching transitions.

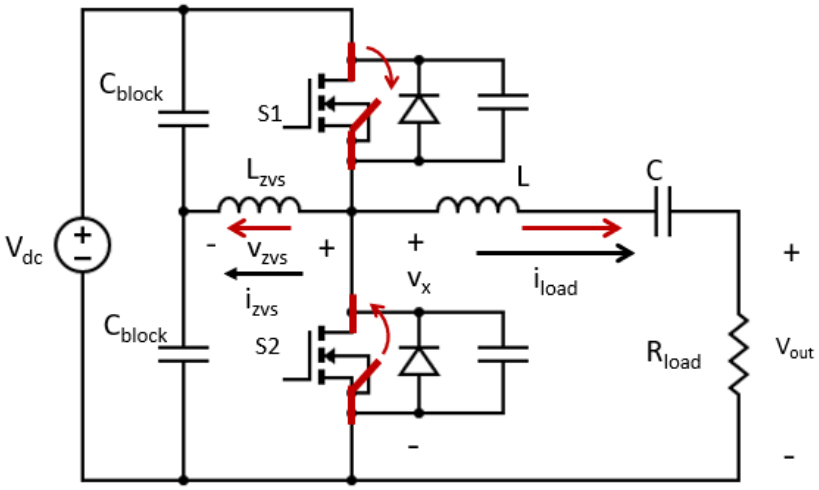
As mentioned in the previous chapter, it is difficult to realize ZVS for both transitions when implementing duty ratio (beta) control because a minimum on-time period is required to achieve soft switching (either by tuning the load inductively and/or adding an inductor). However, because we are tuning the load to use the second harmonic of the switching frequency, we are able to use components of v_x including the fundamental to drive current i_{zvs} to realize soft switching. By modulating beta between π and $3\pi/2$ or $\pi/2$ and π, we only use duty ratios providing v_x a relatively wide duration at both V_{dc} and 0. It is thus simpler to ensure that over a wide range of output amplitudes that the ZVS current i_{zvs} will always be negative on the rising edge of v_x and it will always be positive of the falling edge, as shown in Fig. 4.8.

The ability to achieve the desired ZVS current, largely driven by the fundamental component of v_x, is why we select a switching angle range between either pi/2 and pi or between pi and 3pi/2. If we modulated between 0 and $\pi/2$ or $3\pi/2$ and 2π, we would still see the same small durations in a given state that are typically seen in a standard resonant converter that make it impractical to soft switch when the duty cycle is very low or so high.

Thus by using the second harmonic to deliver power to the load and the fundamental to achieve ZVS, we are able to use beta modulation to control the output power, while still maintaining soft switching across all switching transitions!

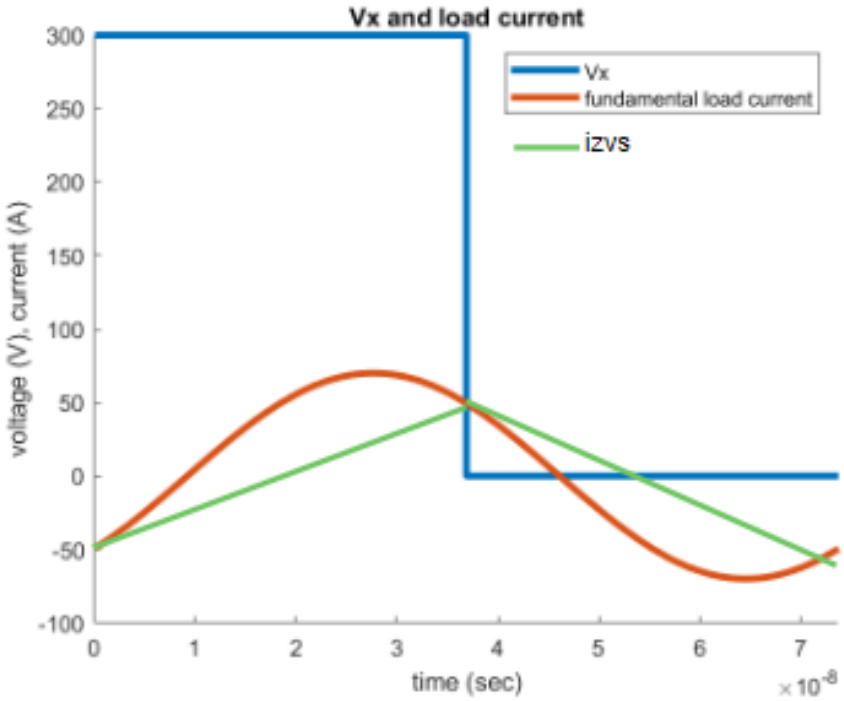


(a) Deadtime 1

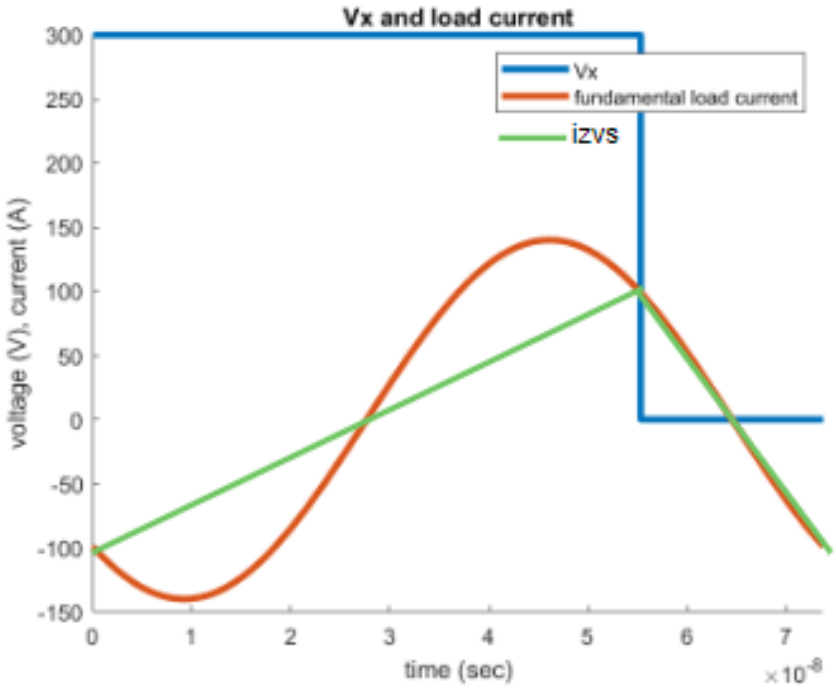


(b) Deadtime 2

Figure 4.7: Dead time periods for circuit operation of the single-ended direct synthesis frequency multiplier inverter. These states are interspersed with the states of the idealized operation in Fig. 4.1.



(a) v_x, i_{load}, and i_{zvs} for $\beta = \pi$



(b) v_x, i_{load}, and i_{zvs} for $\beta = 3\pi/2$

Figure 4.8: Synthesized voltage v_x, fundamental of load current, and current through L_{zvs}

4.3 Calculations

Output Voltage, Current, and Power

The load voltage can be calculated in the following manner using fourier analysis. v_x is some square wave with duty β and period 2π. Expressing the voltage v_x as a Fourier series:

$$v_x(t) = V_o + \sum_{n=1}^{\infty} V_x sin(n\omega t + \phi_n)$$

The fourier coefficients a_n and b_n are:

$$a_n = \frac{2}{2\pi} \int_0^{\beta} V_{dc} cos(n\omega t \, d(\omega t)$$

$$a_n = \frac{V_{dc}}{n\pi}(sin(n\beta))$$

$$a_2 = \frac{V_{dc}}{2\pi}(sin(2\beta))$$

$$b_n = \frac{2}{2\pi} \int_0^{\beta} V_{dc} sin(n\omega t \, d(\omega t)$$

$$b_n = \frac{V_{dc}}{n\pi}(1 - cos(n\beta))$$

$$b_2 = \frac{V_{dc}}{2\pi}(1 - cos(2\beta))$$

So the magnitude V_2 is:

$$V_2 = \sqrt{a_2^2 + b_2^2} = \sqrt{(\frac{V_{dc}}{2\pi}(sin(2\beta)))^2 + (\frac{Vdc}{2\pi}(1 - cos(2\beta)))^2}$$

$$= \sqrt{\frac{V_{dc}^2}{4\pi^2}(1 - 2cos(2\beta) + (sin(2\beta))^2 + (cos(2\beta))^2)}$$

$$= \sqrt{\frac{V_{dc}^2}{4\pi^2}(2 - 2cos(2\beta))}$$

$$V_2 = \frac{V_{dc}}{\sqrt{2}\pi}\sqrt{(1 - cos(2\beta)}$$

and the phase of the 2nd harmonic voltage ϕ_2 is:

$$\phi_n = arctan(\frac{a_n}{b_n}) = arctan(\frac{(\frac{V_{dc}}{n\pi}(sin(2\beta)))}{(\frac{V_{dc}}{n\pi}(1-cos(2\beta)))})$$

$$\phi_2 = arctan\frac{sin(2\beta)}{1-cos(2\beta)}$$

The second harmonic of V_x is thus:

$$V_{x,2} = \frac{V_{dc}}{\sqrt{2}\pi}\sqrt{(1-cos(2\beta)}sin(2\omega t + arctan\frac{sin(2\beta)}{1-cos(2\beta))})$$

The magnitude of the tank and load impedance is:

$$|Z| = \sqrt{(\omega(L_s + L_{load} - \frac{1}{\omega C_s})^2 + R_{load}^2}$$

The magnitude of the second harmonic component of the current is thus:

$$|I_2| = |V_2|/|Z|$$

$$|I_2| = \frac{\frac{V_{dc}}{\sqrt{2}\pi}\sqrt{(1-cos(2\beta)}}{\sqrt{(\omega(L_s+L_{load})-\frac{1}{\omega C_s})^2+R_{load}^2}}$$

The average load power owing to the second harmonic component is thus:

$$P_2 = \frac{1}{2}|I_2|^2 R_{load}$$

$$P_2 = \frac{1}{2}\frac{R_{load}\frac{V_{dc}^2}{2\pi^2}(1-cos(2\beta)}{(\omega(L_s+L_{load})-\frac{1}{\omega C_s})^2+R_{load}^2}$$

4.3.1 Zero-Voltage Switching

Because the voltage across L_{zvs} is a square wave, we can approximate the current through the inductor as a triangle wave as shown in Fig. 4.8 with the following method.

$$v = L\frac{di}{dt}$$

$$\frac{2I_{zvs,pk}}{2\pi/\beta} = \frac{\alpha V_{dc}-0}{L}$$

$$I_{zvs,pk} = \frac{2\pi/\beta\alpha V_{dc}}{2L}$$

$$I_{zvs,pk} = \frac{V_{dc}}{L_{zvs}}$$

where $\alpha = \beta/2\pi$ and αV_{dc} is the voltage across the bottom blocking capacitor.

$$i_{zvs} = \begin{cases} \frac{2I_{zvs,pk}}{\beta}\omega t - I_{zvs,pk} & 0 \leq \omega t < \beta \\ \frac{-2I_{zvs,pk}}{\beta}\omega(t-2\pi) - I_{zvs,pk} & \beta < \omega t \leq 2\pi \end{cases}$$

As described above, there are are two deadtimes in which the switches turn on and off. Let's take a look at the simplest case in which the load is not tuned inductively, thus only L_{zvs} is being used to achieve soft-switching.

For the first deadtime, δ_1, KCL at the switching node is:

$$i_{zvs} = i_1 + i_2$$

where

$$i_1 = C_1 \frac{d(v_x - V_{dc})}{dt} = C_1 \frac{dv_x}{dt}$$

and

$$i_2 = C_2 \frac{d(v_x - 0)}{dt} = C_2 \frac{dv_x}{dt}$$

because the current through L_{zvs} discharges S1 and charges S2.

Integrating over δ_1 where δ_1 is a percentage of the total period multiplied by 2π,

$$\int_0^{V_{dc}} (C_1 + C_2)\, dv_x = \int_0^{\delta_1} i_{zvs}(\omega t)\, d(\omega t)$$

During this deadtime, we can approximate $i_{zvs}(\omega t) = i_{zvs}(\beta) = I_{zvs,pk}$. This gives the new approximation:

$$\omega(C_1 + C_2)V_{dc} = I_{zvs,pk}\delta_1$$

Assuming that $C_1 = C_2 = C_{sw}$ and solving for L_{zvs} we get

$$L_{zvs} = \frac{\delta_1 T_{sw}}{2\omega C_{sw}}$$

The same analysis can be done for the second deadtime, except we must make the approximation that $i_{zvs} = i_{zvs}(0) = I_{zvs,pk}$.

For simplicity, we can keep the deadtimes constant, then use the known values of β, ω, and C_{sw} to find the minimum required L_{zvs}.

4.3.2 LC Tank Selection

The following equations were used to calculate Ls and C_s

$$L_s/C_s = Q_{min}^2 R_{max}^2$$

$$L_s C_s = 1/\omega_c^2$$

An $R_{max} = 20\Omega$ was arbitrarily selected and a $Q_{min} = 10$ was selected through simulation trial and error. As previously noted, a high quality factor is desirable for eliminating unwanted harmonic content, but also requires larger passive components.

If there is no ZVS current through the load, the tank is driven at resonance and designed as such. However, if there is ZVS current provided by the load network, then the tank must be driven slightly above resonance to make the load look inductive. This offset can be defined as L_{net} such that $X_{net} = \omega_c L_{net}$ and $L_s = L_s' + L_{net}$.

4.3.3 Frequency Selection

In order to ensure the output power is resistant to variations in the load reactance, it is desirable to keep the net load and LC tank reactance constant. If there is zero-voltage switching through the load, then $X_{net} = 0$. X_{net} can be defined as follows

$$X_{net} = \omega(L_s + L_{load}) - \frac{1}{\omega C_s}$$

As L_{load} changes, ω can be varied to ensure X_{net} remains constant.
The new output frequency in rad/sec, ω can thus be calculated as

$$\omega = \frac{X_{net} + \sqrt{X_{net}^2 - 4(L_s + L_{load})(-1/C_s)}}{2(L_s + L_{load})}$$

This equates to a new switching frequency in Hz of

$$f_{sw} = \omega/(4\pi)$$

The division by 4 comes from the conversion to Hz and from the fact that the switching frequency is half the output frequency.

4.4 Results and Discussion

The following results are for the case with no ZVS through the load and a 5 percent deadtime.

V_{dc}	300V
f_{sw}	6.78MHz
L_s	$2.35\mu H$
C_s	$58.7pF$
L_{zvs}	$0.25\mu H$
C_{block}	5 μF
R_{load}	5-20 Ω
C_{sw}	80pF
$R_{ds,on}$	$42m\Omega$
L_{load}	0-187nH

The calculation methods described above were used as a starting point, then adjusted based on simulation results. As such, the value I selected for L_{zvs} was approximately a quarter of what was calculated.

4.4.1 Power vs. β for R_{load} range

Fig. 4.9 shows the relationship between power and β when the LC tank is driven at resonance so ZVS is only achieved through the additional inductor and blocking capacitors.These results were obtained through time-domain simulation using the simulation package PLECS, with the simulation setup illustrated in Appendix .While we are able to achieve a high power range, one thing to note is the peak to peak I_{zvs} is around 40A.

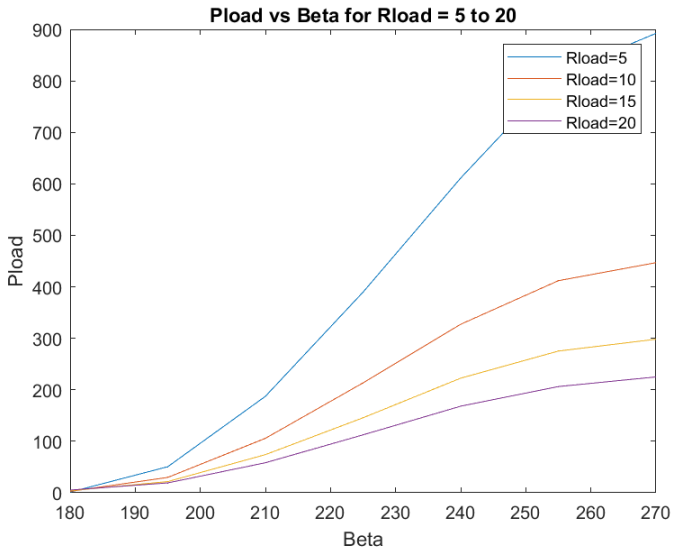


Figure 4.9: Power vs. β for different R_{load} with no ZVS through load (i.e., with the frequency selected for X_{net}=0). Results were obtained through simulations carried out in the circuit simulator PLECS, using the setup shown in Appendix A.

Switching Frequency (kHz)	Load Inductance (nH)	Load Resistance (Ohms)
6.78	0	5
6.64	97	5
6.53	187	5
6.78	0	20
6.64	97	20
6.53	187	20

Table 4.2: Relationship between switching frequency and load inductance

4.4.2 Power vs. β for R_{load} and L_{load}

The following graphs depict the relationship between the output power and β as the load resistance is held constant (from 5Ω to 20Ω) and the load inductance is varied (from 0nH to 187nH). As expected, the power varies very little as the load inductance changes, thanks to frequency modulation. The table shows how the switching frequency changes as the load inductance is varied as well. The code for these graphs can be found in Appendix B.

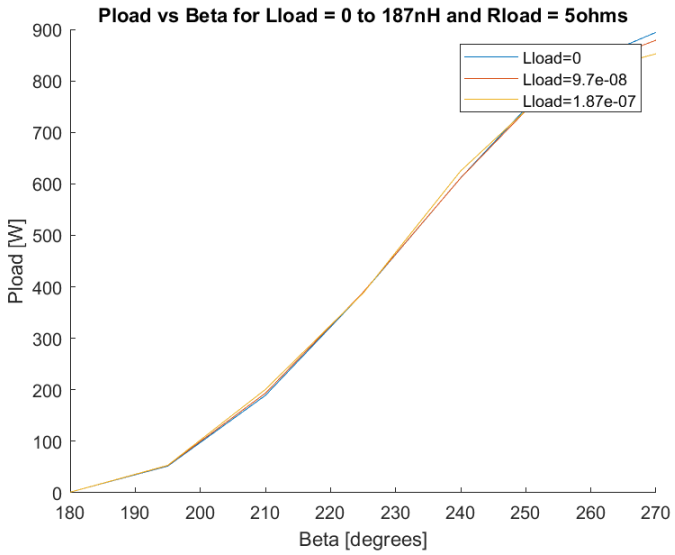


Figure 4.10: Power vs. β for different L_{load} with $R_{load} = 5\Omega$

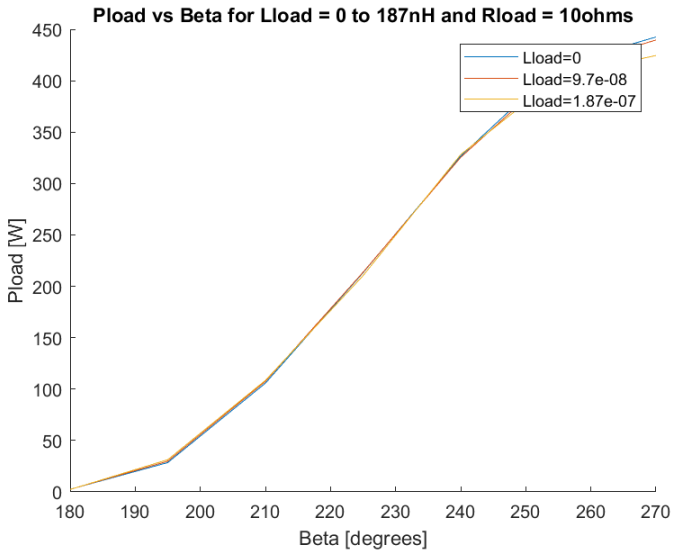


Figure 4.11: Power vs. β for different L_{load} with $R_{load} = 10\Omega$

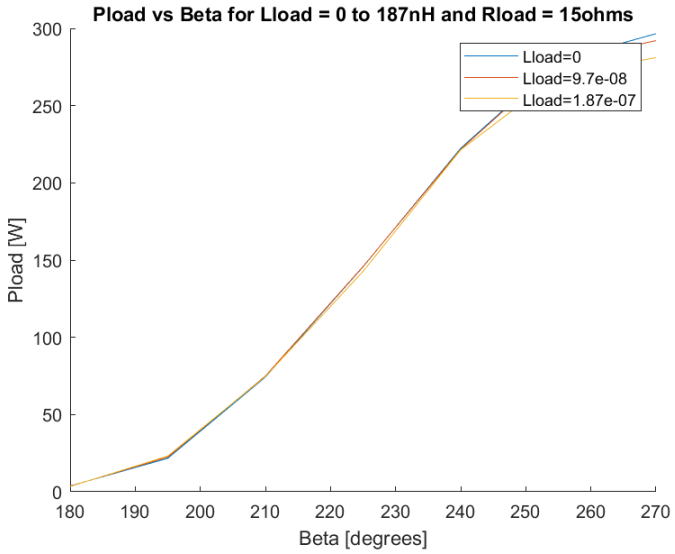


Figure 4.12: Power vs. β for different L_{load} with $R_{load} = 15\Omega$

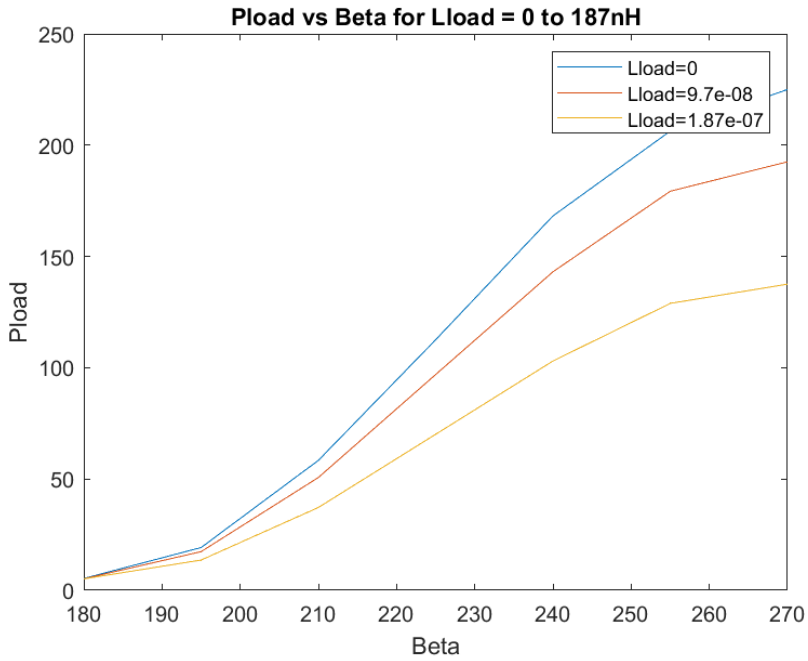


Figure 4.13: Power vs. β for different L_{load} with $R_{load} = 20\Omega$

4.4.3 ZVS switching transitions

The following images show the switch voltage and current during the turn on and turn off transitions. The images show that there is no overlap between the current and voltage, demonstrating successful implementation of ZVS.

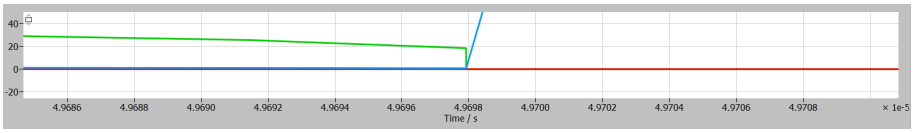


Figure 4.14: S1 turn off with blue = switch voltage, green = switch current, red = diode current

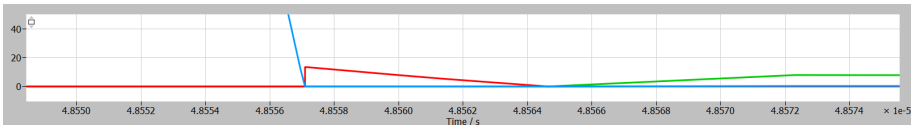


Figure 4.15: S1 turn on with blue = switch voltage, green = switch current, red = diode current

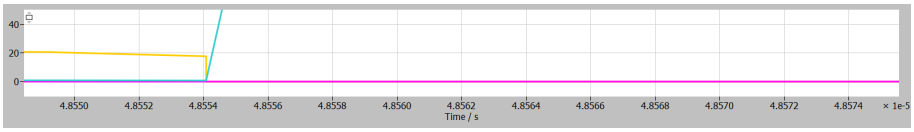


Figure 4.16: S2 turn off with blue = switch voltage, yellow = switch current, pink = diode current

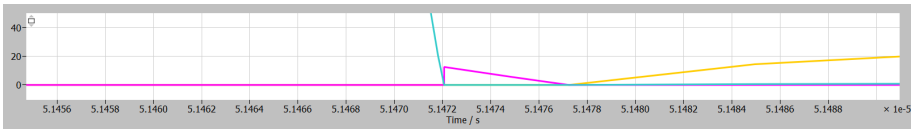


Figure 4.17: S2 turn on with blue = switch voltage, yellow = switch current, pink = diode current

4.4.4 Harmonic Content

While we are able to achieve a wide power range over a resistive range of 5-20Ω and reactive load range of 0-187nH, a high Q tank is needed to extract the second harmonic and suppress the fundamental component at the load. If the quality factor is not high enough, parts of the fundamental can be found in the load current and voltage. This is undesirable for a number of reasons. The primary reason is that in order to achieve a wide output power range we must be able to minimize and maximize the magnitude of the output waveform. We cannot do this with the fundamental and second harmonic simultaneously, so the presence of the fundamental limits our output power range. Using a high Q tank is challenging as it requires the peak energy storage of the circuit to be high, resulting in larger passive components which can be poor for losses, cost more, and take up more board space. Thus to eliminate this problem, the a double-ended implementation of the modulated-frequency multiplier is introduced in Chapter 5.

Chapter 5

Double-Ended Direct Synthesis Frequency Multiplier

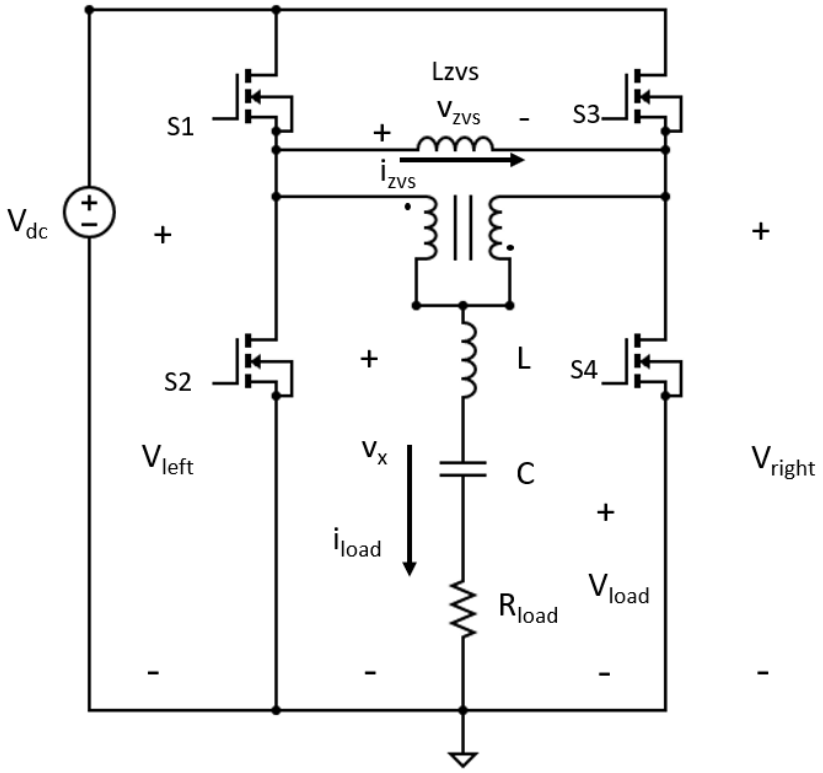


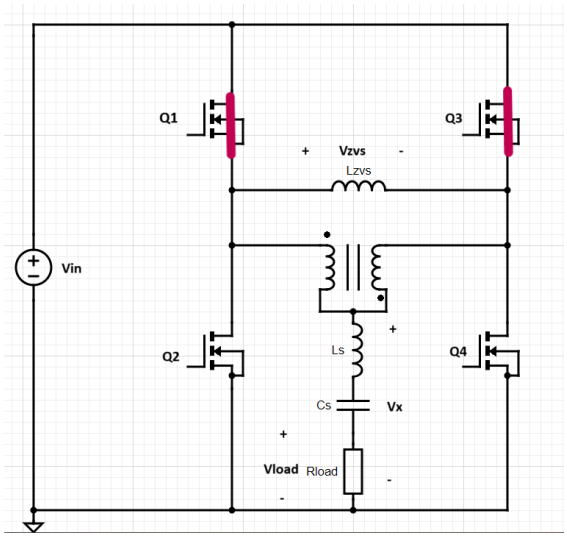
Figure 5.1: Double-ended direct synthesis frequency multiplier circuit topology

The double-ended frequency multiplier shown in Fig. 5.1 consists of four switches arranged in a full h-bridge topology. The two switching nodes are connected to an common-mode combiner transformer (or "interphase" transformer) which is then connected to an LC tank and the load. The switching nodes are also connected to an inductor which provides current for ZVS soft-switching of all four switches.

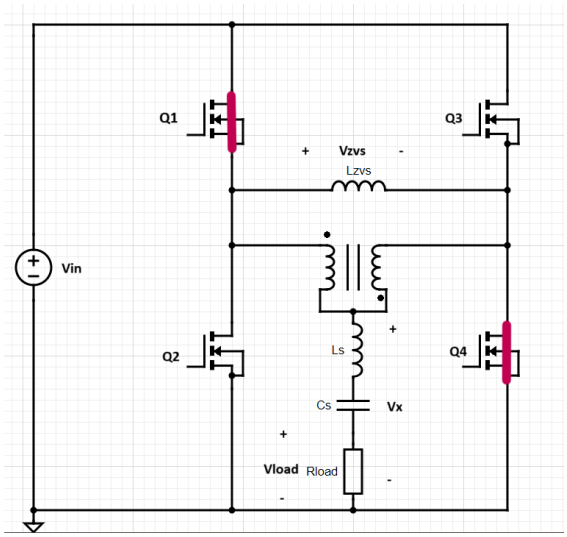
5.1 Idealized Operation

5.1.1 General Operation

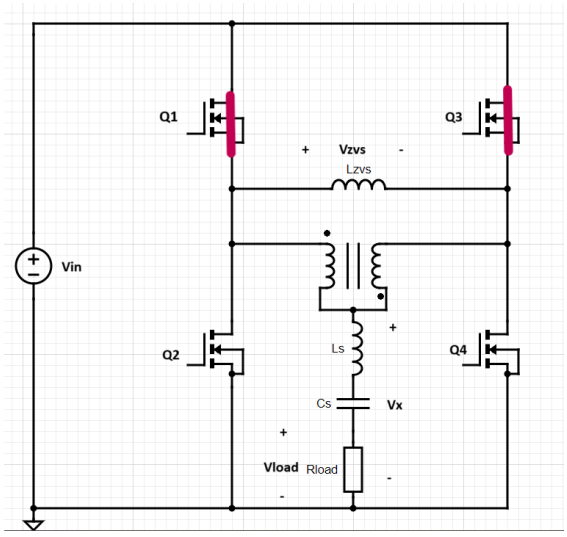
As shown in Fig.5.2 and 5.3, beta (or phase) modulation is used to modulate Q1 and Q2 to generate a rectangle wave, v_{left}, that has a duty cycle β at the switching frequency, ω_{sw}. Q3 and Q4 generate a rectangle wave v_{right} that is 180 degrees (of the fundamental) out of phase with V_{left} with the same duty cycle β.



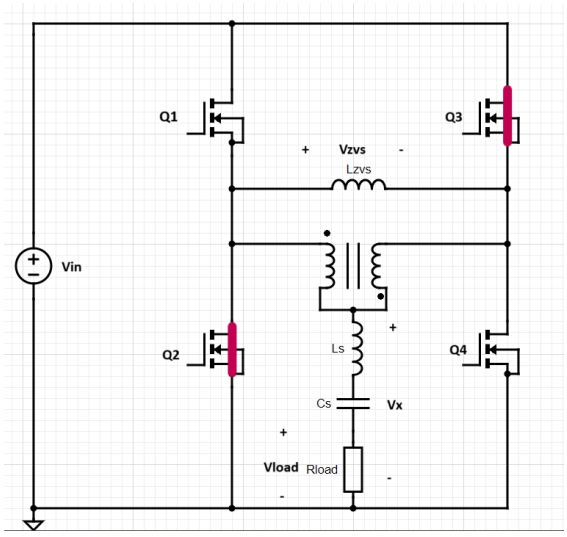
(a) $0 \leq \omega t \leq \beta - \pi$



(b) $\beta - \pi \leq \omega t \leq \pi$



(c) $\pi \leq \omega t \leq \beta$



(d) $\beta \leq \omega t \leq 2\pi$

Figure 5.2: Ideal circuit operation of double-ended direct synthesis frequency multiplier inverter

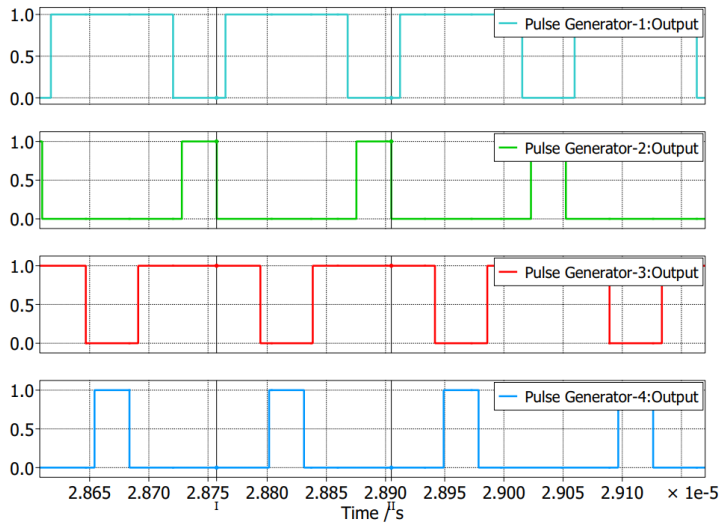


Figure 5.3: Double-ended direct synthesis frequency multiplier gate drive waveforms for simulation parameters described in Table 5.1

The two waveforms, v_{left} and v_{right} are then fed into a common-mode combiner which acts like a differential-mode choke by taking the average of the two half-bridge outputs, v_x. The fundemental components of v_{left} and v_{right} cancel in the average waveform, v_x, and oscillates at twice the switching frequency. The waveforms for v_{left}, v_{right}, and v_x are shown in Fig. 5.4.

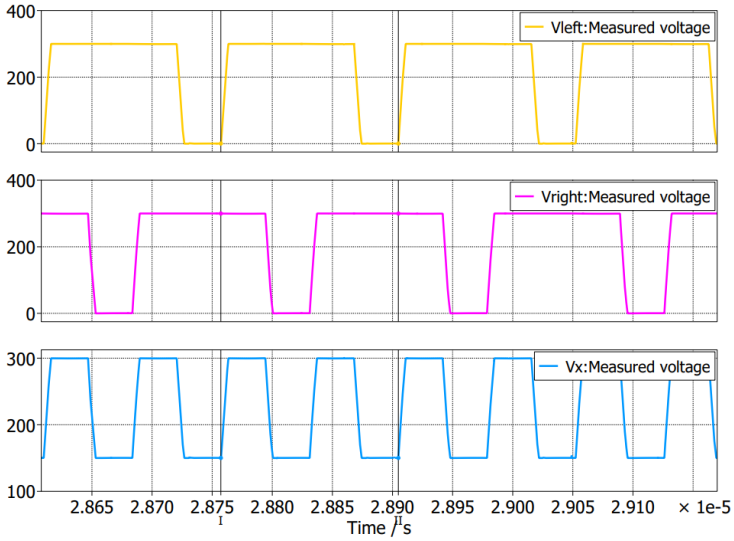


Figure 5.4: Double-ended direct synthesis frequency multiplier left and right voltage waveforms and v_x for simulation parameters described in Table 5.1

The LC tank then extracts the fundamental of v_x, or the second harmonic of v_{left} or v_{right}, which it then delivers to the load. v_x, v_{load}, and i_{load} are shown in Fig. 5.5 below.

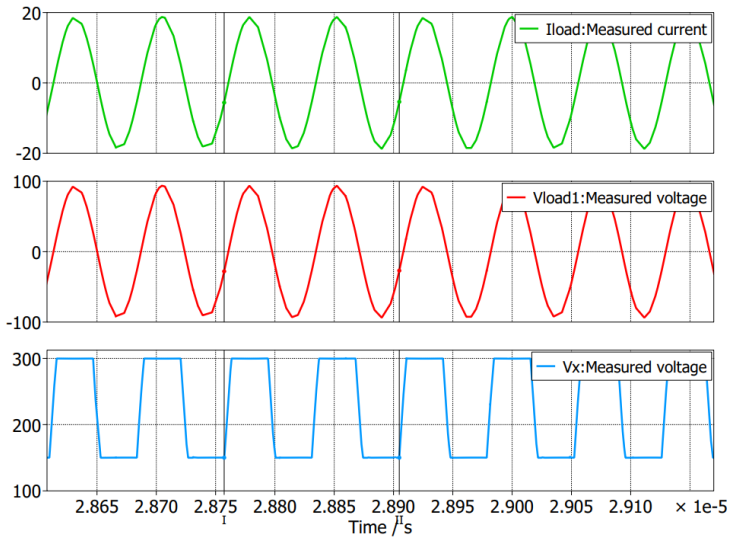


Figure 5.5: Double-ended direct synthesis frequency multiplier load voltage and current waveforms and v_x waveform for simulation parameters described in Table 5.1

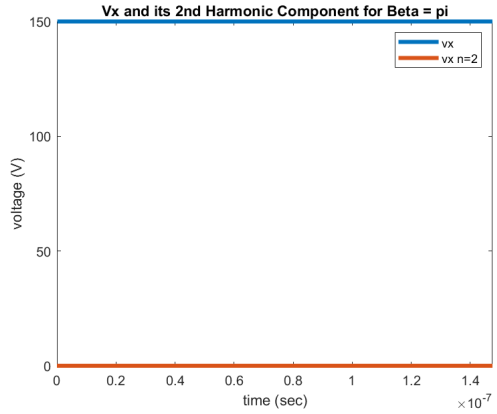
Parameter	Value
V_{dc}	300V
f_{sw}	6.78MHz
L_s	$2.35\mu H$
C_s	$58.7pF$
L_{zvs}	$0.7\mu H$
R_{load}	5 Ω
C_{sw}	80pF
$R_{ds,on}$	$42m\Omega$
β	$3\pi/2$
δ	.05

Table 5.1: PLECS simulation specifications for the single-ended direct frequency multiplier

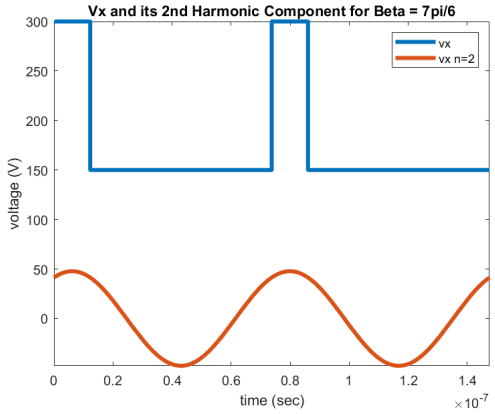
5.1.2 Beta Modulation

The waveforms v_{left} and v_{right} are selected to be 180 degrees of the fundamental out of phase such that their fundamentals cancel and their second harmonic components reinforce at the output of the common-mode combiner. This eliminates the problem seen in the single-ended converter in which the fundamental could still be seen in the load unless a high Q tank was used.

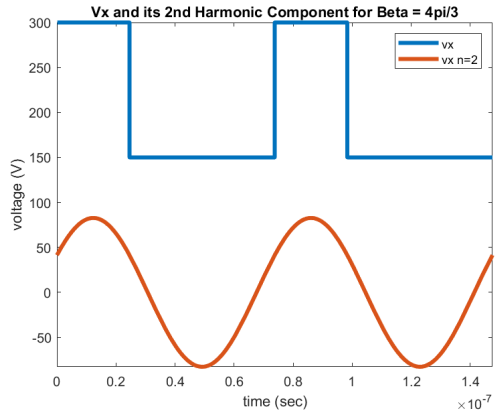
β is varied from π to $\frac{3\pi}{2}$. This range was selected by analyzing the magnitude and phase of the second harmonic of the square wave, as done in the previous section for the single-ended frequency multiplier. Modulating β changes the width of v_x, thereby changing the amplitude and phase of the second harmonic as shown in Fig. 5.6.



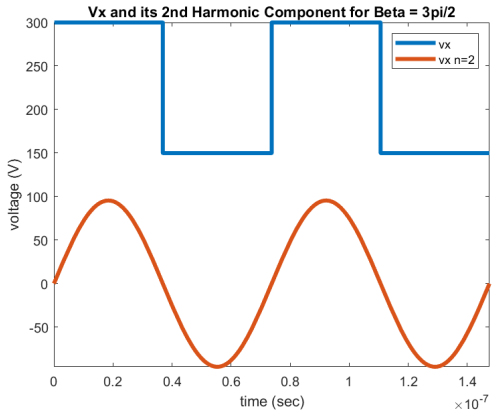
(a) $\beta = \pi$



(b) $\beta = 7\pi/6$



(c) $\beta = 4\pi/3$



(d) $\beta = 3\pi/2$

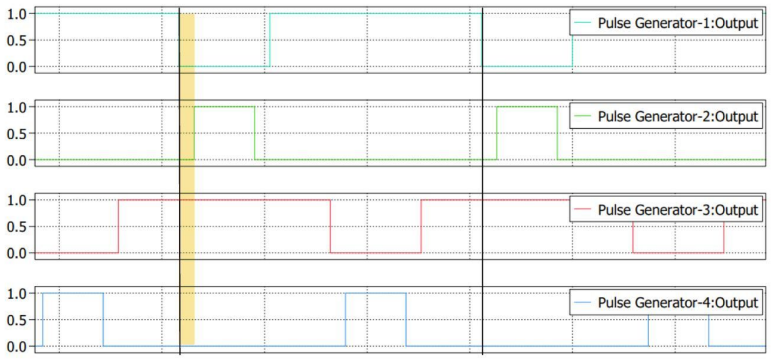
Figure 5.6: v_x and its second harmonic as β is increased

5.2 Practical Realization: Zero-Voltage Switching

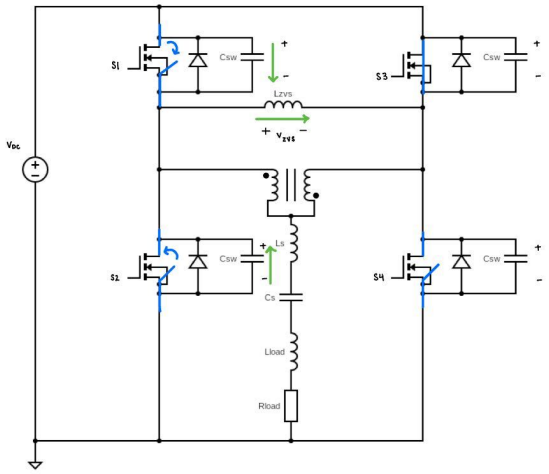
In order for the converter to achieve high efficiency, zero voltage soft switching is needed to minimize switching losses, which means deadtimes must be inserted into the switching scheme. The 2-way class D based frequency multiplier achieves ZVS using the difference of voltages of v_{left} and v_{right}. Fig. 5.7-5.10 below show the direction of current flow during the deadtimes illustrating how L_{zvs} is used to achieve ZVS for all switching transitions. As mentioned in chapter 3, it is difficult for a fundamental-output inverter to realize ZVS when implementing wide-range duty ratio (beta) control because of the short pulse-widths that may occur (either by tuning the load inductively or adding an inductor). However, because we are tuning the load to use the second harmonic of the switching frequency, we are able to use the fundamental to realize soft switching, and narrow pulse widths of either v_{left} or v_{right} are not required. By modulating beta between π and $3\pi/2$ or $\pi/2$ and π, we are ensuring that the ZVS current will always be negative on the rising edge of v_x and it will always be positive of the falling edge. If we modulated between 0 and $\pi/2$ or $3\pi/2$ and 2π, we would still see the same component stresses at the fundamental that are typically seen in a standard resonant converter that make it impractical to soft switch when the duty cycle is very low or very high.

5.2.1 Qualitative Analysis

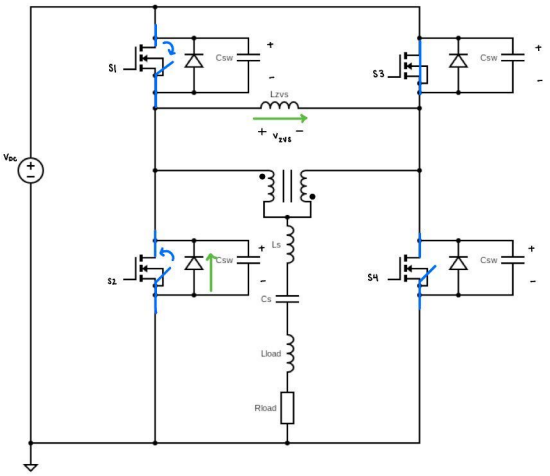
During the first deadtime, δ_1, S1 turns off and S2 turns on. In the first portion, the capacitance across S1 holds the voltage across the switch low while the current through the switch decreases. At the same time, the capacitor across S2 is discharged. Once the voltage across S2 goes to 0, in the second portion of the deadtime, the internal diode across S2 becomes forward biased and turns on. A similar process occurs during the second deadtime, δ_2, during which S2 turns on and S2 turns off.



(a) δ_1 : S1 OFF, S2 ON

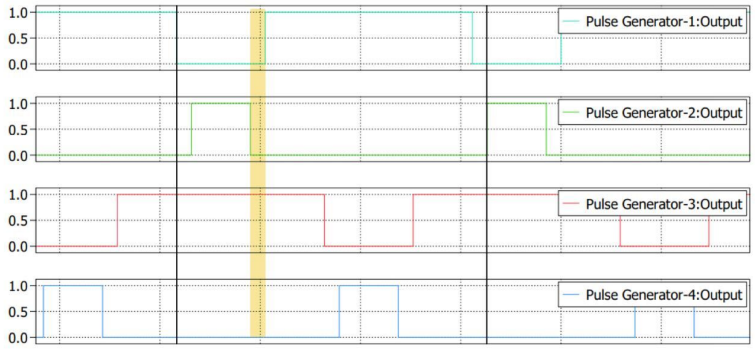


(b)

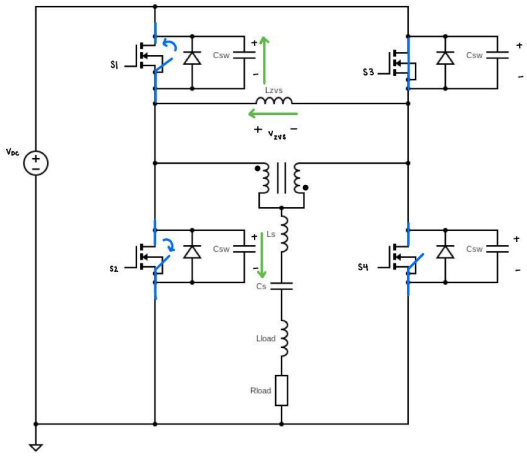


(c)

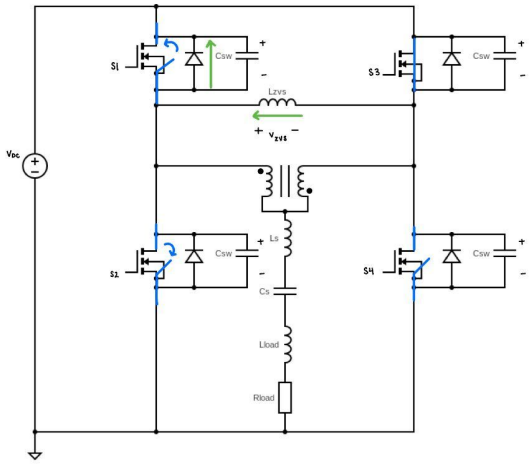
Figure 5.7: ZVS during δ_1



(a) δ_2 : S1 ON, S2 OFF

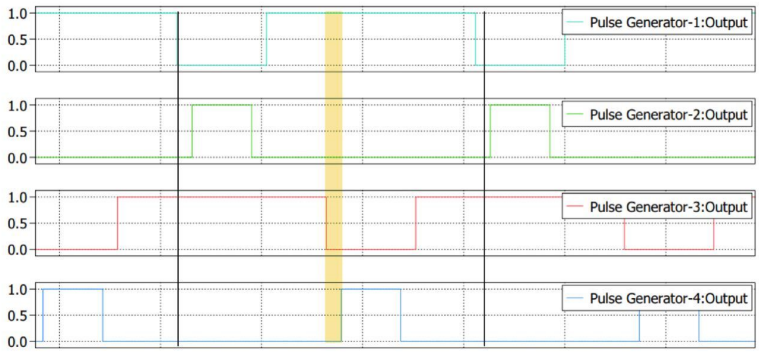


(b)

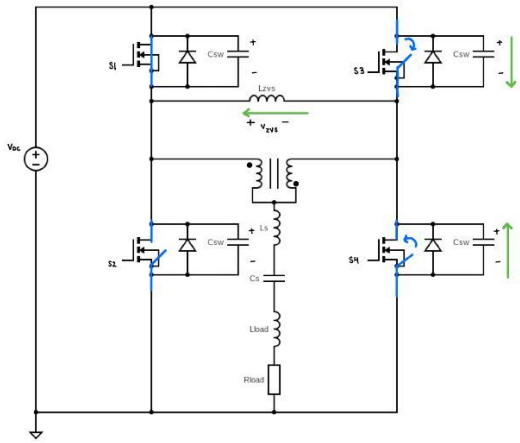


(c)

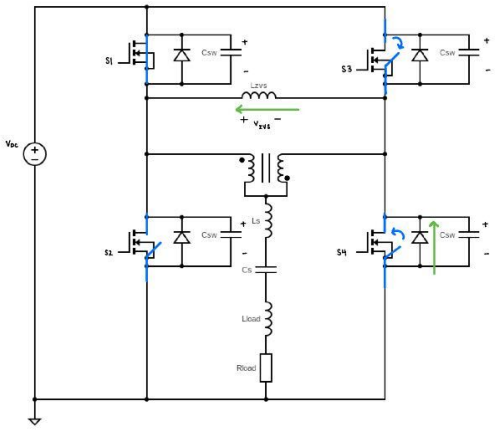
Figure 5.8: ZVS during δ_2



(a) δ_1 : S3 OFF, S4 ON

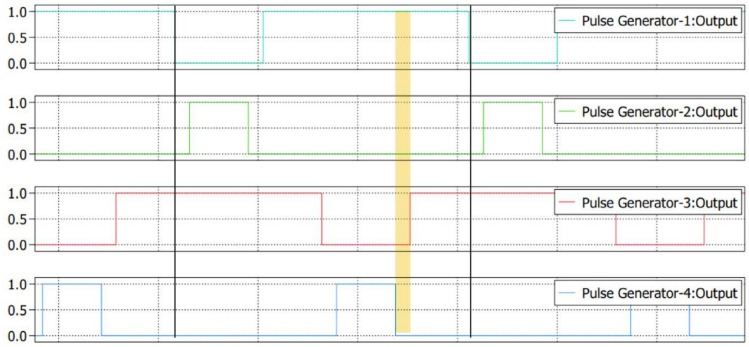


(b)

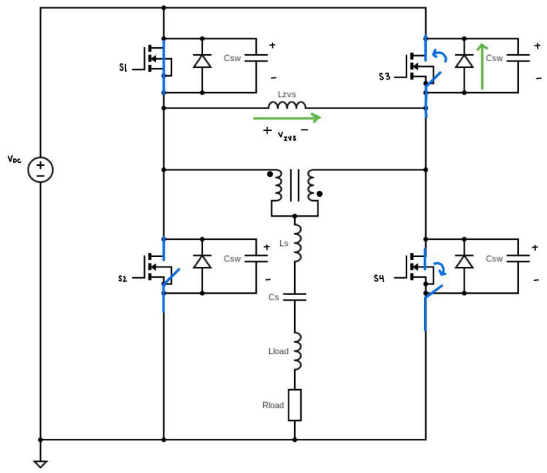


(c)

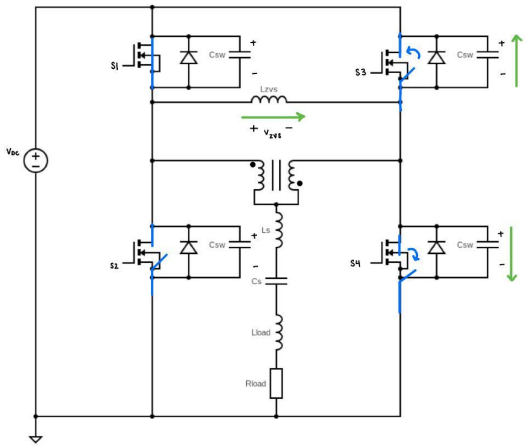
Figure 5.9: ZVS during δ_3



(a) δ_1 : S1 OFF, S2 ON



(b)



(c)

Figure 5.10: ZVS during δ_4

5.3 Calculations

Frequency modulation and LC tank selection was done in the same manner described in the previous chapter and yielded the same values, thus will not be described in further detail here.

5.3.1 Output Voltage

The synthesized voltage v_x was calculated in the same manner as v_{left} described in the single-ended section, included here once more. From the equation for V_n it can be seen that the fundamental and odd harmonics are zero, while the even harmonics (notably the second harmonic) are reinforced. This is consistent with the expectation that the double-ended inverter cancels the fundamental frequency while reinforcing the second harmonic which is delivered to the load.

$$v_x(t) = V_o + \sum_{n=1}^{\infty} V_x sin(n\omega t + \phi_n)$$

The fourier coefficients a_n and b_n are:

$$a_n = \frac{2}{2\pi} \int_0^{\beta} V_{dc} cos(n\omega t \, d(\omega t)$$

$$a_n = \frac{V_{dc}}{n\pi}(sin(n\beta))$$

$$a_2 = \frac{V_{dc}}{2\pi}(sin(2\beta))$$

$$b_n = \frac{2}{2\pi} \int_0^{\beta} V_{dc} sin(n\omega t \, d(\omega t)$$

$$b_n = \frac{V_{dc}}{n\pi}(1 - cos(n\beta))$$

$$b_2 = \frac{V_{dc}}{2\pi}(1 - cos(2\beta))$$

So the magnitude V_n is:

$$V_n = \frac{V_{dc}}{\sqrt{2}n\pi}\sqrt{1 - cos(n\beta)}$$

$$V_2 = \frac{V_{dc}}{\sqrt{2}\pi}\sqrt{(1 - cos(2\beta)}$$

5.3.2 Zero-Voltage Switching

The current in the single-ended frequency multiplier was triangular, however in the double ended inverter with a differentially-connected ZVS inductor, i_{zvs} is trapezoidal. Analysis for selecting L_{zvs} was nevertheless done in a similar manner as with the single-ended version, but accounting for the change in waveshape. It should be noted that one can alternatively use two ZVS inductors (one for each half-bridge), each connected to a blocking capacitor. In that case, each half-bridge will see a triangular i_{zvs} current, just as in the single-ended version.

5.4 Results

Using the values described in the table below, the following results were obtained for the double-ended direct synthesis frequency multiplier of Fig. 5.1 using the design parameters in Table 5.2. Simulations were carried out using PLECS simulation software.

Parameter	Value
V_{dc}	300V
f_{sw}	6.78MHz
L_s	$2.35\mu H$
C_s	$58.7pF$
L_{zvs}	$0.7\mu F$
R_{load}	1-20 Ω
C_{sw}	80pF
$R_{ds,on}$	$42m\Omega$

Table 5.2: Simulation specifications for the double-ended direct frequency multiplier

5.4.1 Power vs. β for resistive load

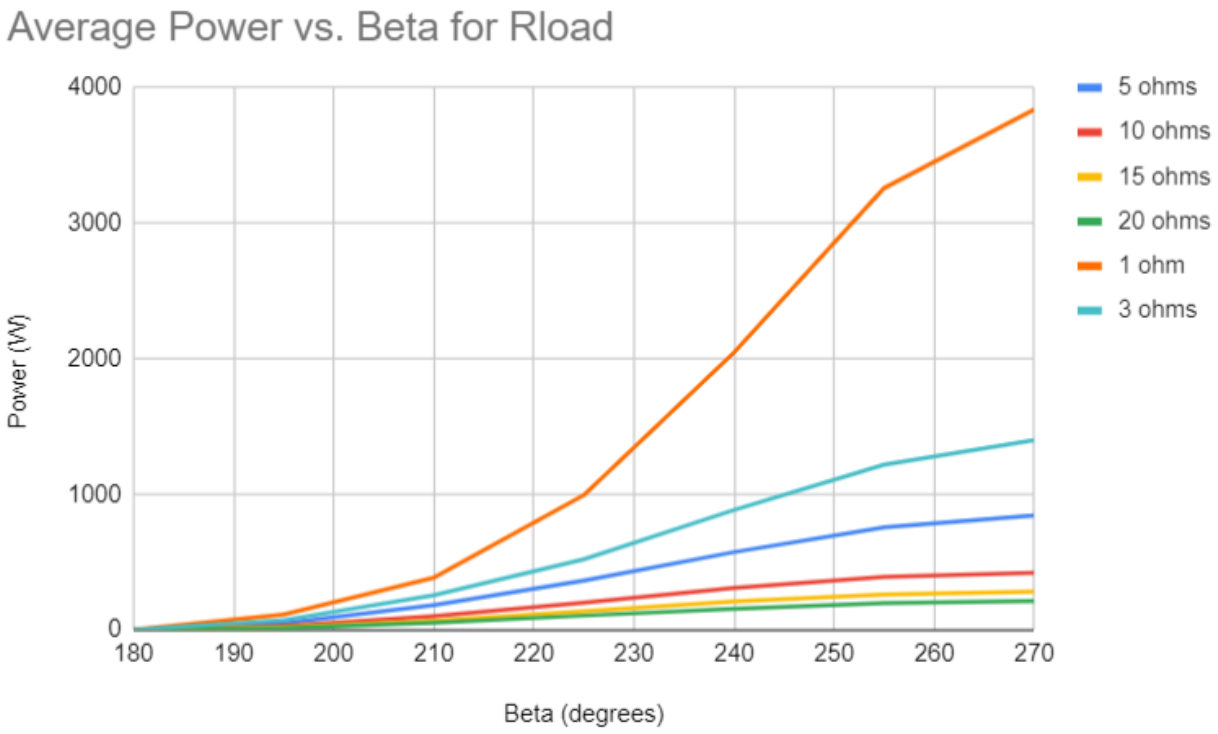
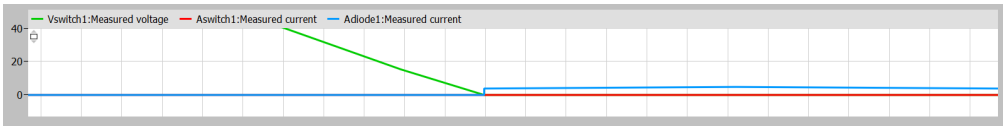


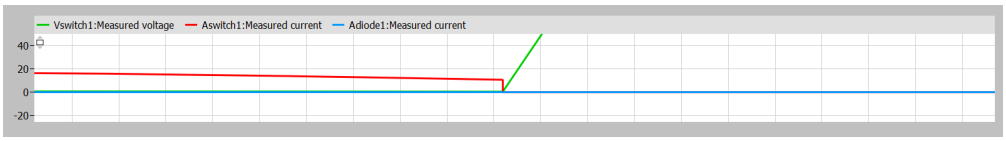
Figure 5.11: Power vs. β for R_{load}

5.4.2 ZVS

In the figures below, the simulation switch current and voltage are plotted, clearly showing that the area under the two curves has been minimized, showing that ZVS is being successfully achieved at turn off for all switches!

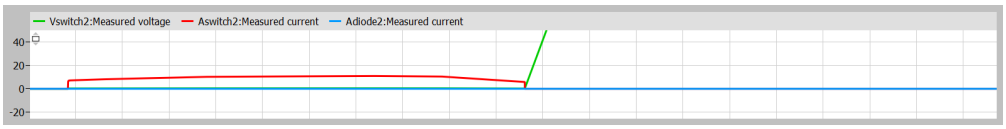


(a) δ_1 : v_{switch} and i_{switch} turn on

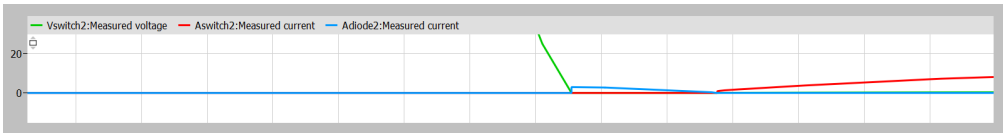


(b) δ_1 : i_{zvs} and v_{zvs} turn off

Figure 5.12: ZVS demonstrated in simulation for S1

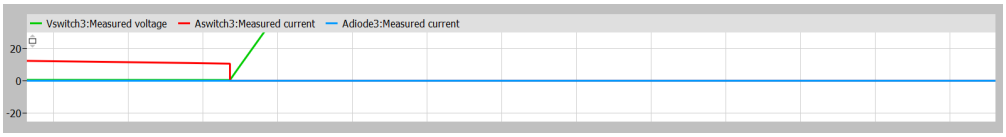


(a) δ_2 : v_{switch} and i_{switch} turn off

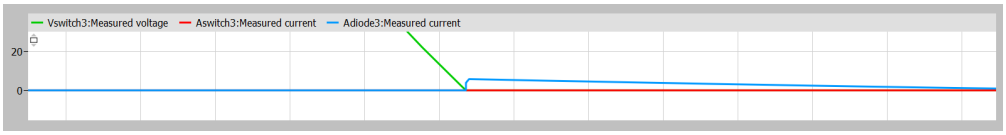


(b) δ_2 : v_{switch} and i_{switch} turn on

Figure 5.13: ZVS demonstrated in simulation for S2

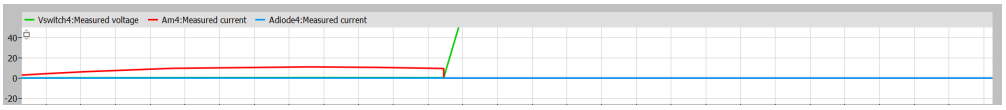


(a) $\delta_3 : v_{switch}$ and i_{switch} turn off

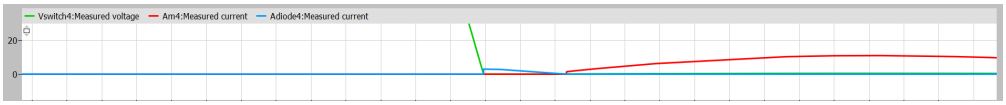


(b) $\delta_3 : v_{switch}$ and i_{switch} turn on

Figure 5.14: ZVS demonstrated in simulation for S3



(a) $\delta_4 : v_{switch}$ and i_{switch} turn off



(b) $\delta_4 : v_{switch}$ and i_{switch} turn on

Figure 5.15: ZVS demonstrated in simulation for S4

Fig. 5.11 illustrates that we are able to get wide-range power control via beta modulation. We are simultaneously able to minimize the second harmonic at π and maximize it $3\pi/2$. This is to say that we are able to make large changes in the second harmonic and very small changes in the fundamental by varying β by a quarter of a cycle! This was done symmetrically, though it can also be designed asymmetrically as is described in the next section.

Chapter 6

2-Way Frequency Multiplier Combiner

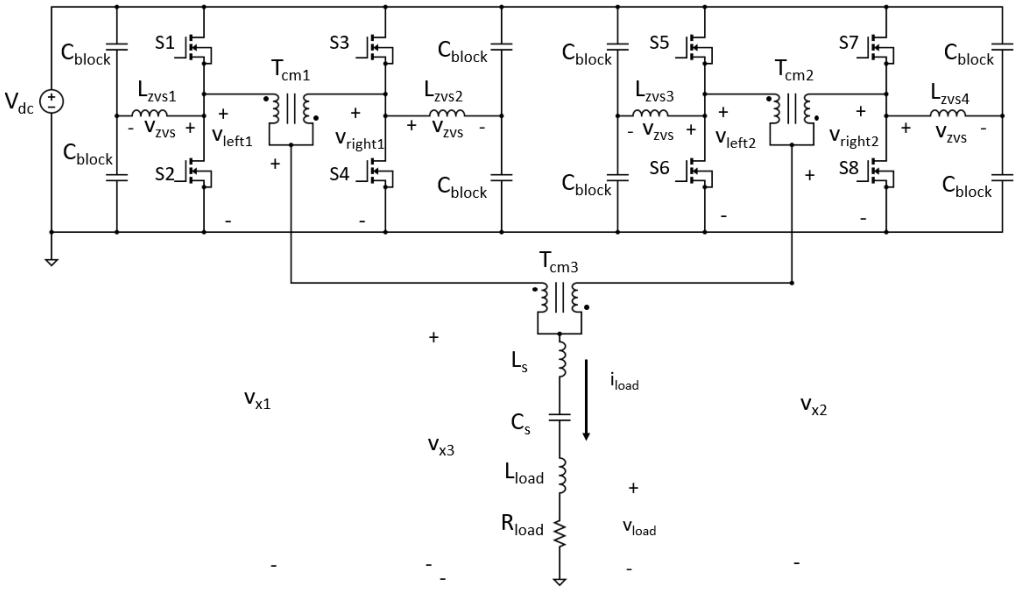


Figure 6.1: 2-way frequency multiplier combiner topology

In order to achieve even higher power outputs it is possible to construct an N-way converter. It is also possible to take advantage of many-way systems to achieve further power modulation capability.

6.1 Idealized Operation

6.1.1 General Operation

This thesis explores the functionality of combining the outputs of two double-ended frequency multipliers with a 2-way combiner to yield a four-way system. This strategy, shown in Fig. 6.1 in which the outputs of two double-ended frequency multiplier inverters are combined to drive a load. Such a structure could be used in multiple ways. One way would be to

realize a frequency quadrupler. A second way would be to operate as a frequency doubler in which the two double-ended frequency doublers operate identically and, the final two-way combiner is simply used to provide "in-phase combining" to achieve increased output power. However, still better control performance for frequency doubler operation can be achieved through asymmetric operation, as described below.

Looking at the first double-ended inverter, the switches S1 and S2, along with S3 and S4, operate in a complementary fashion, generating a voltage v_{left1} and v_{right1} respectively, each with a duty cycle β. β is varied between π and $3\pi/2$ for v_{left1} and it is modulated between $\pi/2$ and π for v_{right1}. In particular, we can operate the left-hand half-bridge at an angle $\beta_{left} = \pi + \gamma$ and the right-hand half-bridge at an angle $\beta_{right} = \pi - \gamma$ for values of γ between 0 and $\pi/2$. This means that the inverter is operating asymmetrically, such that the second harmonic delivered to the load is at a maximum when $\beta_{left} = 3\pi/2$ and $\beta_{right} = \pi/2$ ($\gamma = \pi/2$) and is at a minimum when $\beta_{left} = \pi$ and $\beta_{right} = \pi$ ($\gamma = 0$). The switching scheme for this first double-ended inverter is shown in Fig. 6.2.

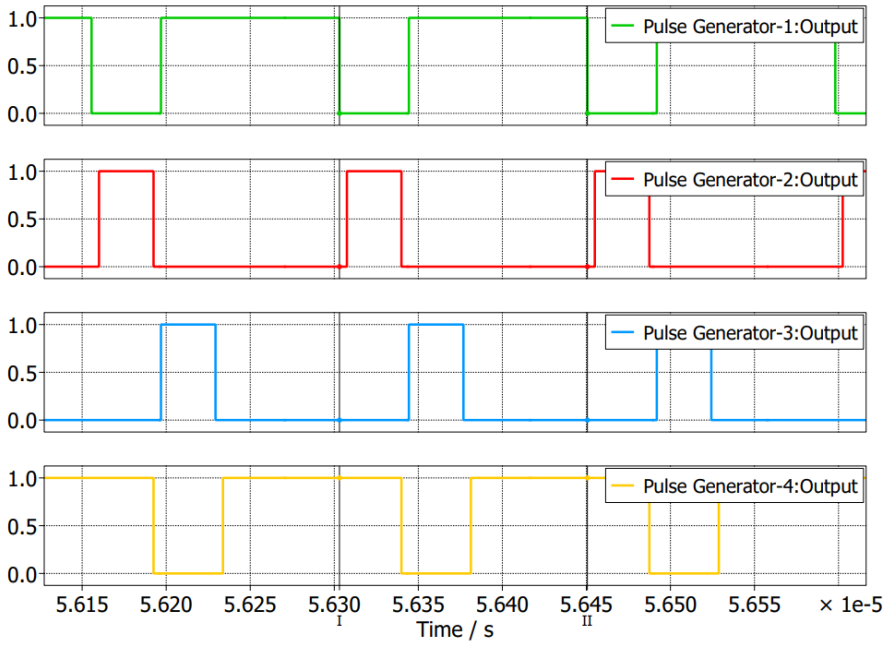


Figure 6.2: Gate drives for first double-ended inverter in 2-way combiner with asymmetric operation at $\beta_1 = 4\pi/3$ and $\beta_2 = 2\pi/3$ (or equivalently, with $\gamma = \pi/3$).

The second (right-hand) double-ended inverter operates in the same fashion, except each of the half bridges is 180° out of phase with its respective half bridge in the first inverter.

The generated waveforms are combined with v_{left1}, v_{right1}, common-mode combined to form v_{x1} as the average of v_{left1} and v_{right1}, and v_{left2}, and v_{right2} common-mode combined to form v_{x2} as the average of v_{left2} and v_{right2}. v_{x1} and v_{x2} thus have the same waveshape, but are shifted by half a fundamental cycle.

v_{x1} and v_{x2} are then combined using a final common mode combiner, producing voltage v_{x3}, which has the effect of canceling the fundamental and odd-harmonic components of v_{x1} and v_{x2} in v_{x3} while having the same even-harmonic components as v_{x1} and v_{x2}. Lastly, the

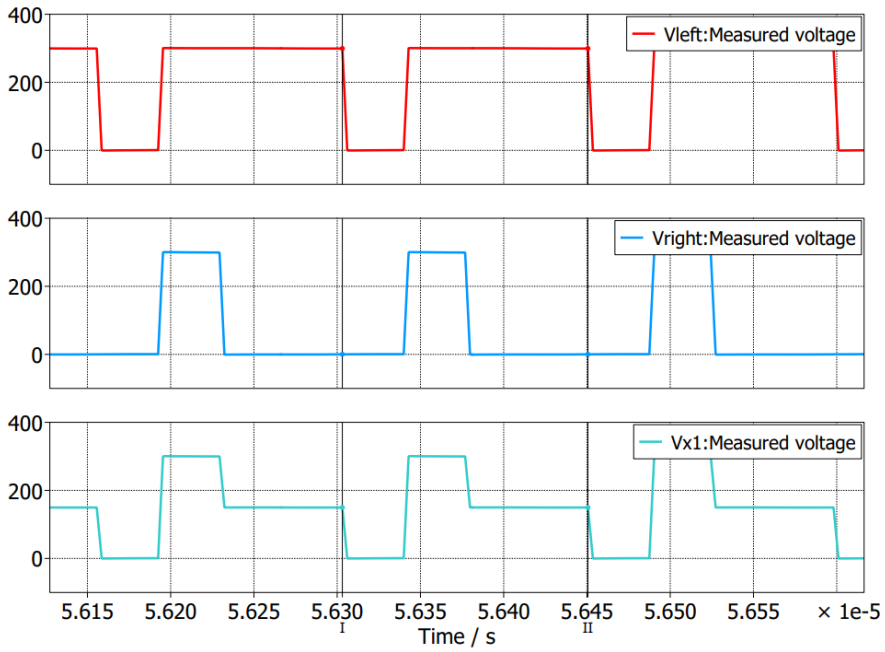


Figure 6.3: v_{left1}, v_{right1}, and v_{x1} for first double-ended inverter in 2-way combiner at simulation conditions described in Table 6.1

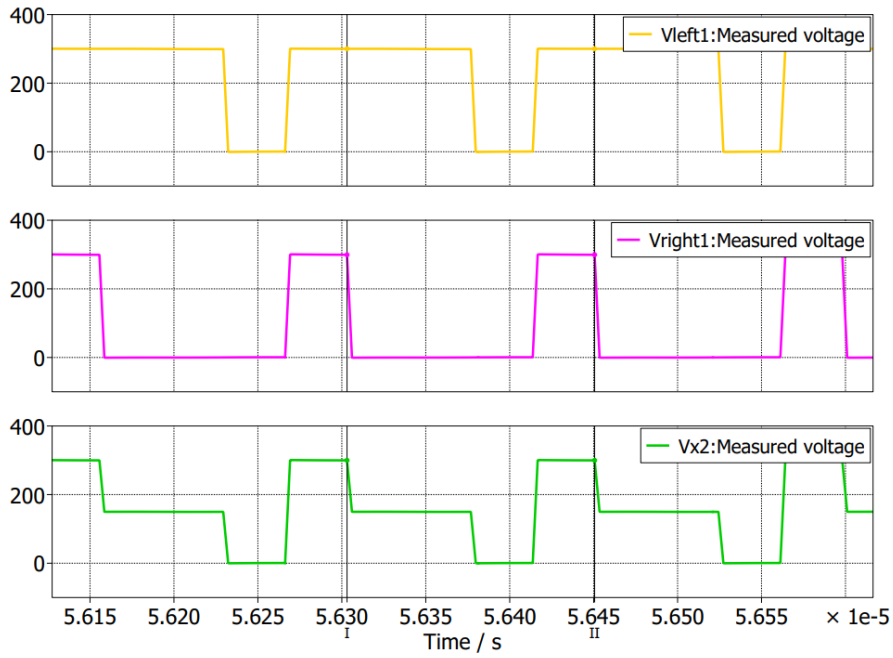


Figure 6.4: v_{left2}, v_{right2}, and v_{x2} for second double-ended inverter in 2-way combiner at simulation conditions described in Table 6.1

LC tank extracts the second harmonic which is delivered to the load. Thus modulating the angles β_{left} and β_{right} changes the duty cycle of the voltage v_{x3}, which in turn controls the

amplitude of the output, as was done with the single-ended and double-ended inverters. An advantage of this asymmetric control scheme is that it effectively provides outphasing of the second harmonic components of v_{x1} and v_{x2} to provide increased ability to modulate the output as compared to a 4-way multiplier with symmetric control.

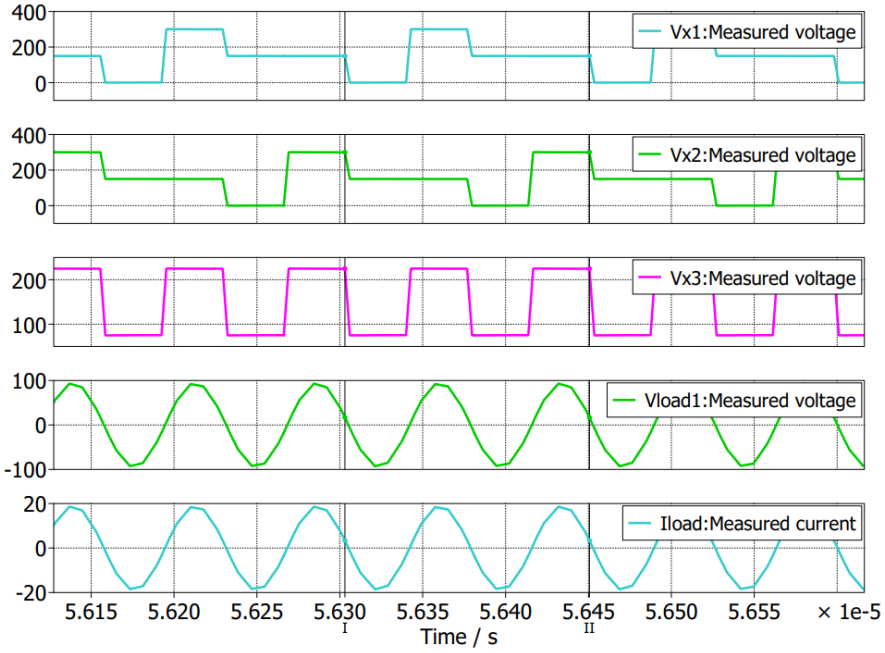


Figure 6.5: v_{x1}, v_{x2}, v_{x13}, v_{load}, and i_{load} for 2-way combiner at simulation conditions described in Table 6.1

Zero-voltage switching and frequency modulation were implemented in the same way as with previously-described double-ended frequency multipliers with the same values as the previously mentioned inverters, thus the calculations and descriptions are not included here. This design follows the single-ended inverter's zero voltage switching approach with an inductor connected to the switch node and to two blocking capacitors. However, ZVS can also be implemented as demonstrated in the double-ended inverter section in which L_{zvs} was differentially connected.

Parameter	Value
V_{dc}	300V
f_{sw}	6.78MHz
L_s	$2.35\mu H$
C_s	$58.7pF$
L_{zvs}	$0.2\mu H$
C_{block}	5 μ F
R_{load}	5 Ω
C_{sw}	80pF
$R_{ds,on}$	$42m\Omega$
β_{left}	$3\pi/2$
β_{right}	$\pi/2$
δ	.03

Table 6.1: PLECS simulation specifications for the 2-way combiner with asymmetric operation

6.2 Results

6.2.1 Power vs. R_{load} for various β

Parameter	Value
V_{dc}	300V
f_{sw}	6.78MHz
L_s	$2.35\mu H$
C_s	$58.7pF$
L_{zvs}	$0.2\mu H$
C_{block}	5 μ F
R_{load}	5-20 Ω
C_{sw}	80pF
$R_{ds,on}$	$42m\Omega$
β_{left}	$3\pi/2$ to π
β_{right}	$\pi/2$ to π
δ	.03

Table 6.2: PLECS simulation specifications for the 2-way combiner with asymmetric operation for power vs beta plot

Fig. 6.6 shows the relationship between the load resistance, output power, and β. This topology helps us to better maintain a constant output power across a wide resistive range, as opposed to the output power being limited by the load resistance as seen in the previous designs.

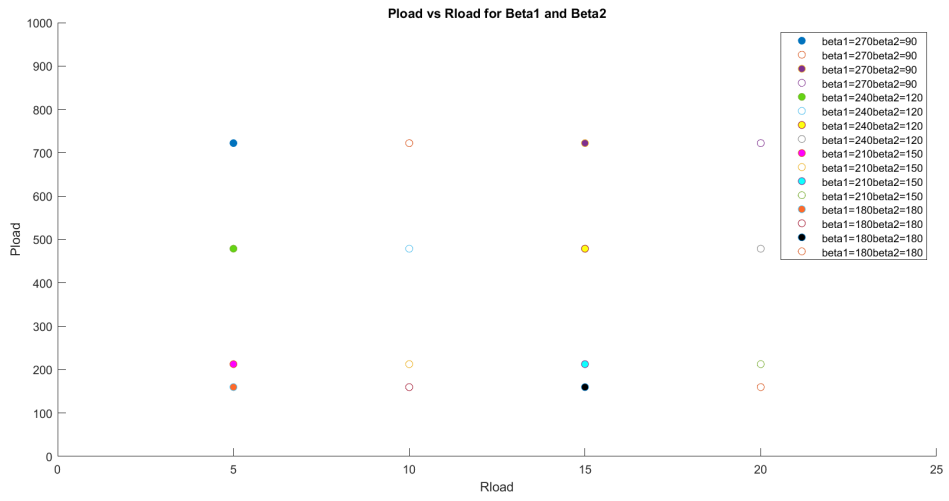


Figure 6.6: Power vs. R_{load} for β combinations

Appendix A

Code listing

Matlab code for generating power vs beta plots for single-ended inverter for various Rload.

```
1
2  proxy = jsonrpc('http://localhost:1080', 'Timeout', 100);
3
4  path = 'C:\Users\Sarah Coston\Documents\Plexim\PLECS 4.7 (64 bit)\';
5  model_name = 'RF_amp_singleended_SarahCoston';
6
7  proxy.plecs.scope([model_name '/Scope3'], 'ClearTraces');
8
9  simStruct = struct('ModelVars', struct('Beta', 50e-6, 'Rload', 50));
10
11 % Set values for Beta and Rload to be swept
12 betaValues = 180:15:270;
13 resistorValues = [5, 10, 15, 20]; % Define resistor values to be
       swept
14
15
16 % Allocate memory for cell array
17 simStructs = cell(length(betaValues)*length(resistorValues), 1);
18
19 % Initialize simStruct as cell array with all combinations of Beta
       and Rload
20 idx = 1;
21 for ix = 1:length(betaValues)
22     %disp(betaValues(ix));
23     for jx = 1:length(resistorValues)
24         simStructs{idx}.ModelVars.Beta = betaValues(ix)*pi/180;
25         simStructs{idx}.ModelVars.Rload = resistorValues(jx);
26         simStructs{idx}.Name = ['Beta=' mat2str(betaValues(ix)) ',
               Rload=' mat2str(resistorValues(jx))];
27         idx = idx + 1;
28     end
29 end
30
```

```
31
32 results = proxy.plecs.simulate(model_name, simStructs); %Results is
       Pload and Psource
33
34 % Preallocate array for power values
35 Pload = zeros(length(resistorValues), length(betaValues));
36
37 for jx = 1:length(resistorValues)
38     disp(resistorValues(jx));
39     for ix = 1:length(betaValues)
40         disp(betaValues(ix));
41         % Extract Pload value from the last column of Values
42         Pload(jx, ix) = results((ix-1)*length(resistorValues)+jx)
               .Values(1,end); % Assuming Pload is the first element in
               Values
43         disp(Pload(jx, ix));
44         %Psource(jx, ix) = results((ix-1)*length(resistorValues)+jx)
               .Values(2,end);
45     end
46 end
47 %%
48
49
50 % Plot Pload vs Beta for given Rload
51  figure;
52 for resistorIndex = 1:length(resistorValues)
53  % Choose the index of the beta you want to plot
54  plot(betaValues, Pload(resistorIndex, :),'DisplayName', ['Rload='
       mat2str(resistorValues(resistorIndex))]);
55  hold on;
56 end
57  xlabel('Beta');
58  ylabel('Pload');
59  title(['Pload vs Beta for Rload = 5 to 20']);
60  xlim([180 270]); % Set x limits
61
62
63 legend('show');
64
65
66 \end{luacode*}
```

Appendix B

Code listing

Matlab code for generating power vs beta plots for single-ended inverter for various Lload.

```
1
2  proxy = jsonrpc('http://localhost:1080', 'Timeout', 100);
3
4  path = 'C:\Users\Sarah Coston\Documents\Plexim\PLECS 4.7 (64 bit)\';
5  model_name = 'RF_amp_singleended_SarahCoston';
6
7  proxy.plecs.scope([model_name '/Scope3'], 'ClearTraces');
8
9  simStruct = struct('ModelVars', struct('Beta', 50e-6, 'Lload', 50));
10
11 % Set values for Beta and Rload to be swept
12 betaValues = 180:15:270;
13 loadinductorValues = [0,97e-9,187e-9];
14
15 % Allocate memory for cell array
16 simStructs = cell(length(betaValues)*length(loadinductorValues), 1);
17
18 % Initialize simStruct as cell array with all combinations of Beta
      and Rload
19 idx = 1;
20 for ix = 1:length(betaValues)
21     %disp(betaValues(ix));
22     for jx = 1:length(loadinductorValues)
23         simStructs{idx}.ModelVars.Beta = betaValues(ix)*pi/180;
24         simStructs{idx}.ModelVars.Lload = loadinductorValues(jx);
25         simStructs{idx}.Name = ['Beta=' mat2str(betaValues(ix)) ',
              Lload=' mat2str(loadinductorValues(jx))];
26         idx = idx + 1;
27     end
28 end
29
30
```

```
results = proxy.plecs.simulate(model_name, simStructs); %Results is
    Pload and Psource

% Preallocate array for power values
Pload = zeros(length(loadinductorValues), length(betaValues));

for jx = 1:length(loadinductorValues)
    disp(loadinductorValues(jx));
    for ix = 1:length(betaValues)
        disp(betaValues(ix));
        % Extract Pload value from the last column of Values
        Pload(jx, ix) = results((ix-1)*length(loadinductorValues)+jx)
            .Values(1,end); % Assuming Pload is the first element in
            Values
        disp(Pload(jx, ix));
        %Psource(jx, ix) = results((ix-1)*length(resistorValues)+jx)
            .Values(2,end);
    end
end
%%


% Plot Pload vs Beta for given Rload
 figure;
 hold on;
for loadinductorIndex = 1:length(loadinductorValues)
 % Choose the index of the beta you want to plot
 plot(betaValues, Pload(loadinductorIndex, :),'DisplayName', ['Lload=
    ' mat2str(loadinductorValues(loadinductorIndex))]);
end
 xlabel('Beta [degrees]');
 ylabel('Pload [W]');
 title('Pload vs Beta for Lload = 0 to 187nH and Rload = 20ohms');
 xlim([180 270]); % Set x limits
hold off;

legend('show');
```

Appendix C

Code listing

Matlab code for generating power vs resistance scatterplots for 2-way asnychronous inverter for different values of beta.

```
1
2  proxy = jsonrpc('http://localhost:1080', 'Timeout', 100);
3
4  path = 'C:\Users\Sarah Coston\Documents\Plexim\PLECS 4.7 (64 bit)\';
5  model_name = '2way_frequencymultipliercombiner';
6
7  proxy.plecs.scope([model_name '/Scope3'], 'ClearTraces');
8
9  simStruct = struct('ModelVars', struct('beta', 50e-6, 'beta2', 50e-6,
       'Rload', 50));
10
11 % Set values for Beta and Rload to be swept
12 betaValues = [180]; %[180,210,240,270];
13 beta2Values =  [180]; % [180, 150, 120,90];
14 resistorValues = [5, 10, 15, 20]; % Define resistor values to be
       swept
15
16
17 % Allocate memory for cell array
18 simStructs = cell(length(betaValues)*length(beta2Values)*length(
       resistorValues), 1);
19
20 % Initialize simStruct as cell array with all combinations of Beta
       and Rload
21 idx = 1;
22 %for ix = 1:length(betaValues)
23     %disp(betaValues(ix));
24  %    for jx = 1:length(resistorValues)
25   %       simStructs{idx}.ModelVars.beta = betaValues(ix)*pi/180;
26    %      simStructs{idx}.ModelVars.Rload = resistorValues(jx);
```

```
    %    simStructs{idx}.Name = ['beta=' mat2str(betaValues(ix)) ',
       Rload=' mat2str(resistorValues(jx))];
     %   idx = idx + 1;
    %end
%end

for ix = 1:length(resistorValues)
    for jx = 1:length(betaValues)
        simStructs{idx}.ModelVars.beta = betaValues(jx)*pi/180;
        simStructs{idx}.ModelVars.beta_2 = beta2Values(jx)*pi/180;
        simStructs{idx}.ModelVars.Rload = resistorValues(ix);
        simStructs{idx}.Name = ['beta=' mat2str(betaValues(jx)) '
           beta2=' mat2str(beta2Values(jx)) 'Rload=' mat2str(
           resistorValues(ix))];
        idx = idx + 1;
    end
end
disp(simStructs);
results = proxy.plecs.simulate(model_name, simStructs); %Results is
   Pload and Psource

% Preallocate array for power values
Pload = zeros(length(resistorValues), length(betaValues), length(
   beta2Values));

for jx = 1:length(resistorValues)
    disp(resistorValues(jx));
    for ix = 1:length(betaValues)
        disp(betaValues(ix));
        % Extract Pload value from the last column of Values
        Pload(jx, ix) = results((ix-1)*length(resistorValues)+jx)
           .Values(1,end); % Assuming Pload is the first element in
           Values
        disp(Pload(jx, ix));
        %Psource(jx, ix) = results((ix-1)*length(resistorValues)+jx)
           .Values(2,end);
    end
end
%%

 %figure;
hold on;
beta2Index = 1:length(beta2Values);
for betaIndex = 1:length(betaValues)
 % Choose the index of the beta you want to plot
 scatter(resistorValues, Pload(betaIndex, :),'DisplayName', ['beta1='
     mat2str(betaValues(betaIndex)), 'beta2=' mat2str(beta2Values(
```

```
    beta2Index)) ]);

end
 xlabel('Rload');
 ylabel('Pload');
 title(['Pload vs Rload for Beta1 and Beta2']);
 xlim([0 25]); % Set x limits
 ylim([0 1000]);
 legend('show');

hold off;

% Plot Pload vs Beta for given Rload
 %figure;
%for resistorIndex = 1:length(resistorValues)
 % Choose the index of the beta you want to plot
 %yyaxis left
 %scatter(Pload(resistorIndex, :),betaValues,'DisplayName', ['Rload='
     mat2str(resistorValues(resistorIndex))]);
 %hold on;
%end


%for resistorIndex = 1:length(resistorValues)
 %   yyaxis right
  %  scatter(Pload(resistorIndex, :), beta2Values,'DisplayName', ['
     Rload=' mat2str(resistorValues(resistorIndex))]);
%end
%hold off;

%legend('Rload = 5', 'Rload = 10', 'Rload=15', 'Rload = 20');
```

Appendix D

Code listing

PLECS code for single-ended inverter simulations.

```

freq = 6.78e6; %center switching frequency (Hz)
Beta = 3*pi/2; %varies between pi and 3pi/2

delta = 0.05;
period = 1/freq;
duty_1 = Beta/(2*pi);
duty_2 = (2*pi-Beta)/(2*pi);
on_resistance_sw = 42e-3;
switch_capacitance = 80e-12;
Vdc=300;
omega_c = 2*pi*freq;

Lnet = 0; %ZVS through load --> 100e-9; %no ZVS through load --> Lnet
    = 0;
Ls = 2.35e-6 + Lnet; %Ls = Ls' + Lnet for Q = 20 --> 4.7e-6 Q = 10 ->
    2.345e-6
Cs = 58.7e-12 ; %Q = 20 --> 2.94e-11 Q = 10 --> 5.86e-11
Lload = 0e-9;
Rload = 5;

Lzvs = 0.25e-6; %no ZVS through load --> Lzvs = 0.25e-6
C3 = 5e-6;
C4= 5e-6;

Xnet = 2*omega_c*Ls-(1/(2*omega_c*Cs)); %Xnet = 0 when there is no
   ZVS through the load --> driving at resonance
omega = (Xnet+sqrt((Xnet)**2+(4/Cs)*(Ls+Lload)))/(2*(Ls+Lload));
freq_new = omega/(4*pi);
period_new = 1/freq_new;
```

Appendix E

Bibliography

[1] A. S. Jurkov, A. Radomski, and D. J. Perreault, “Tunable matching networks based on phase-switched impedance modulation,” IEEE Transactions on Power Electronics, vol. 35, no. 10, pp. 10 150–10 167, 2020.

[2] A. Bastami, A.S. Jurkov, D.M. Otten, D.T. Nguyen, A. Radomski and D.J. Perreault, “A 1.5 kW Radio-Frequency Tunable Matching Network Based on Phase-Switched Impedance Modulation,” IEEE Open Journal of Power Electronics, Vol. 1, pp. 124-138, April 2020.

[3] A. Al Bastami, H. Zhang, A. Jurkov, A. Radomski and D. Perreault, “Comparison of Radio-Frequency Power Architectures for Plasma Generation,” 2020 IEEE Workshop on Modeling and Control in Power Electronics, November 2020.

[4] Z. Xin, K.N.R. Islam, and D.J Perreault, "Wide-Range Switched-Mode Power Amplifier Architecture," 2023 IEEE 24th Workshop on Control and Modeling for Power Electronics (COMPEL), 2023.

[5] Kassakian, John G., David J. Perreault, George C. Verghese, et al. “Chapter 10: Resonant Converters.” Principles of Power Electronics, 2nd ed., Cambridge University Press, Cambridge, Massachusetts, 2024, pp. 249–284.

[6] W. D. Braun and D. J. Perreault, “A high-frequency inverter for variable-load operation,” IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 7, no. 2, pp. 706–721, 2019.

[7] D.J.Perreault, S.M.Coston, M.V. Joisher, Modulated Frequency Multiplier Inverter. United States Provisional Patent US 63/554,435. U.S. Patent and Trademark Office. February 16, 2024.