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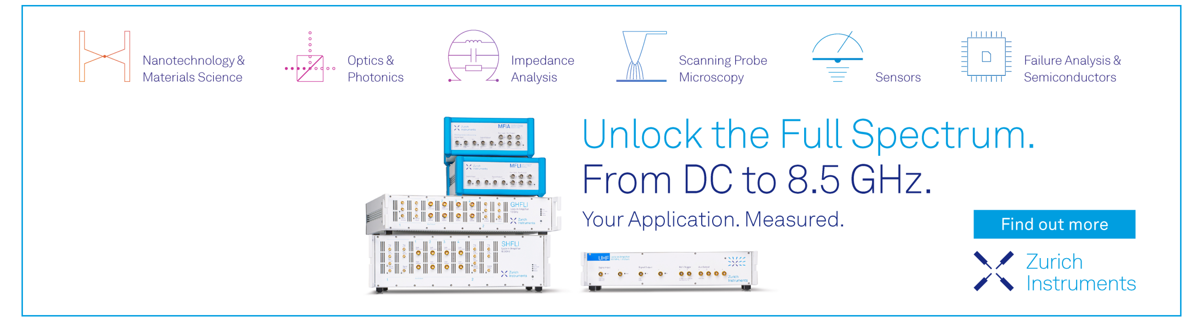

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ABSTRACT

Reduced thermal budget is required for back-end-of-line (BEOL) integration of application specific functionality into the multilevel metal stack of a processor "substrate." We report 400 °C BEOL-compatible Ge-on-Si growth (LT Ge) that is epitaxial and single crystalline with a defect density similar to high temperature growth and a small 0.05% tensile strain. Room temperature methanol–iodine passivation is employed pre-growth in lieu of the typical 800 °C oxide removal step. Undoped LT Ge exhibits p-type conductivity initially and n-type conductivity conversion upon annealing. Hall effect measurements following post growth heat treatment between 400 and 600 °C reveal an acceptor removal reaction that follows first-order kinetics with an activation energy of 1.7 ± 0.5 eV and a pre-exponential factor of $2.3 \times 10^7\ s^{-1}$ consistent with a point defect, diffusion limited process. We also observe that 90° sessile dislocations identified via transmission electron microscopy are annihilated in the same temperature regime, which is evidence for point defect-mediated climb. Ensuring high-quality epitaxy by characterizing defect reactions in a BEOL-compatible Ge-on-Si process flow is key to enabling vertical integration of optical interconnects.

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As Moore's law demands increasingly small features, electrical interconnects face major time delay and power consumption challenges. Monolithic integration of germanium (Ge) on silicon (Si) is a critical part of the roadmap for scaling optical communication systems.[1] Ge's absorption in the Telecom wavelength range along with its ease of integration on Si make it an ideal photodetector for optical interconnects. Various monolithic integration strategies have been employed, including utilizing rapid melt growth to crystallize a SiGe waveguide during rapid thermal anneal for CMOS source–drain implant activation in the front-end-of-line (FEOL).[2] Vertical integration would allow optical interconnects to be fabricated on layers of other devices, thus alleviating the FEOL device density issues of larger feature sizes, and it would introduce the concept of functionality retrofit onto standard circuit designs. Integration in the back-end-of-line (BEOL) introduces strict thermal budget requirements of $T < 450\,°C$ to preserve the integrity of fine line components fabricated in the FEOL.[3]

Epitaxial growth of high-quality Ge-on-Si has been studied to achieve planarity and reduce threading dislocation density (TDD). The Ge lattice constant is 4.2% larger than that of Si, resulting in compressive strain that is relieved by interfacial misfit dislocations (MDs). The MDs generate threading dislocations (TDs) that extend to the Ge surface along the (111) plane. The lattice misfit can also lead to islanding or Stranski–Krastanov growth mode—Ge grows layer-by-layer until reaching a critical thickness where island formation occurs. To maintain planarity, the surface migration length is reduced by first growing a low temperature thin (<50 nm) buffer layer at 350 °C for a two-step growth process where the second high temperature growth step is at 600–750 °C.[4–6] TDD reduction to $<10^6\ cm^{-2}$ has been achieved via growth of a graded Si_xGe_{1-x} buffer, low temperature buffer layer, and/or post-growth annealing.[7] State-of-the-art Ge-on-Si is grown via a two-step deposition process followed by post-growth cyclic annealing, achieving TDDs of $10^6\ cm^{-2}$ for selectively grown Ge and $10^7\ cm^{-2}$ for blanket films. Typical growth temperatures are around 650–730 °C with post-growth anneals at 900 °C.[8] An 800 °C pre-growth anneal in hydrogen (H_2) is conducted in order to remove silicon dioxide that may have formed on the Si surface.[9] Laterally confined growth of single-crystal Ge grains on amorphous Si has been explored to mediate the lack of the crystalline Si substrate in the BEOL.[10] In this Letter, we report single-step low temperature (400 °C)

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BEOL-compatible blanket Ge-on-Si epitaxy utilizing room temperature (RT) methanol–iodine pre-growth passivation. We explore post-growth annealing at low temperatures and identify that acceptor-like point defects and vertical dislocations play a crucial role in the point defect–dislocation interactions responsible for type conversion upon annealing. Understanding these defect reactions guides process design rules for BEOL-compatible interconnects.

Ge was grown via ultra high vacuum chemical vapor deposition (UHVCVD) on silicon and silicon on insulator (SOI) substrates. The SOI used had 250 nm thick near-intrinsic Si on a 5.1 μm thick buried oxide layer. The base pressure of the UHVCVD chamber is low 10^{-9} Torr with substrates loaded at 400 °C. During growth, germane (GeH_4) flow of 10 sccm was employed with no carrier gas. Hall effect samples were fabricated by patterning metal contacts via E-beam evaporation on $1.2 \times 1.2\,cm^2$ Ge on SOI pieces. The contact structure consisted of 20 nm of titanium (Ti), 20 nm of titanium nitride (TiN), and 300 nm of aluminum (Al). The TiN acts as a diffusion barrier between Al and Ge, and the Ti provides an adhesion layer. Hall effect measurements were conducted using 4-point probes and the van der Pauw technique to measure resistivity and current. A magnetic field of 4200 Gauss produced the Hall voltage. Transmission electron microscopy (TEM) and x-ray diffraction (XRD) were also utilized to characterize LT Ge's material properties. Samples were prepared for transmission electron microscopy (TEM) by using focused ion beam along the [110] direction to make a sample cross section. Cross-sectional TEM measurements were conducted along the g vector for imaging from the Kikuchi lines [220] and [004]. X-ray diffraction (XRD) was performed using 1.54 Å Cu x-rays to obtain lattice constant and subsequent strain.

The typical SC1/SC2 pre-growth clean produces a surface that degrades in air by native oxide formation. Standard Ge-on-Si CVD growth is preceded by an *in situ* anneal in H_2 ambient at 800 °C to remove native silicon oxide (SiO_2) from the silicon surface. This 800 °C temperature excursion violates the BEOL thermal budget requirement. We used a room temperature (RT) methanol–iodine solution, which results in superior passivation from Si-OCH_3 compared to Si-H, potentially due to the bulkier OCH_3.[11,12] Other reported solutions include integrated dry-cleaning plasma modules and optimized *ex situ* dilute HF wet cleaning—costly modifications restricted to 300 mm wafers.[13] Our LT clean sequence is comprised of SC1/SC2, then 5 min dilute HF (HF:H_2O is 1:100), and then 20 min methanol–iodine solution. The methanol–iodine solution molarity is 5×10^{-4}, prepared by grinding iodine pellets of 99.999% purity from Sigma-Aldrich and combining with J. T. Baker reagent-grade methanol. This sequence passivates the silicon surface for 30–60 min, in comparison with 10–20 min of H-passivation, which is insufficient for wafer transfer/loading time. Other LT passivation attempts reported include a hydrogen desorption step at 450 °C prior to Ge-on-Si MBE growth. The Ge films grown after the 450 °C desorption step suffered from lower diffusion lengths compared to films grown after standard 800 °C desorption.[14] We compared LT Ge films grown on Si pretreated using dilute HF only and dilute HF + methanol–iodine. We did not include the typical SC1/SC2 steps as we were using brand new nitrogen-packed wafers. As shown in Fig. 1, Ge-on-Si layers grown at 400 °C following our LT clean are specular, comparable to layers grown with the 800 °C step. A specular surface is indicative of planar morphology and uniform crystalline growth. Layers grown following HF-last were hazy and polycrystalline in some cases, representing heterogeneous growth nucleation and SiO_2 particulates on the surface. AFM confirmed nearly equivalent rms roughness for LT Ge grown using the typical SC1/SC2/HF + 800 °C pre-growth anneal in H_2 (7.36 nm) as LT Ge grown using our LT clean (7.47 nm).

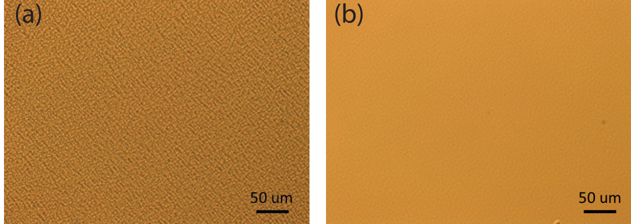

FIG. 1. Nomarski interference microscopy of LT Ge-on-Si wafers from the same growth run: (a) visible haze for wafers with HF-last passivation and (b) specular surface for wafers with methanol–iodine passivation.

We compare the growth rate of our LT Ge grown at 400–430 °C to Cunningham *et al.*'s higher growth temperatures[15] (Fig. 2). LT Ge growth follows an Arrhenius dependence with an activation energy of 1.25 eV, slightly lower than that reported by Cunningham *et al.*, 1.46 eV.[15] The abrupt change in temperature dependence beyond 430 °C indicates that 350–430 °C is in the surface decomposition limited regime. At 400 °C, we obtain the best surface planarity and growth rate of 7 nm/min. Though the growth rate is lower than that of HT Ge, high-performing waveguide-integrated photodetectors have been reported with Ge film thicknesses as low as 300–400 nm.[16,17] XRD plots of LT Ge grown with and without a 350 °C buffer prior to the 400 °C growth step (see Fig. 3) confirm that LT Ge is single crystalline due to the presence of a single Ge peak. The broadening of the Bragg peak, or full width half maximum, from the XRD plots is related to crystallite size using the Scherrer equation:[18]

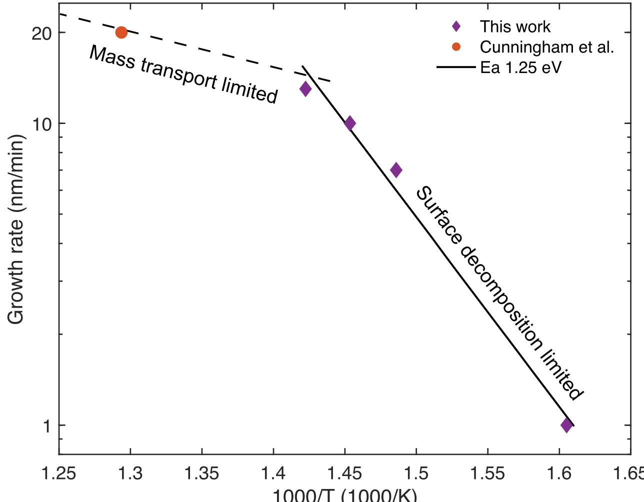

FIG. 2. Growth rate for Ge grown at 350–430 °C via UHVCVD in this work compared to Cunningham *et al.*[15]

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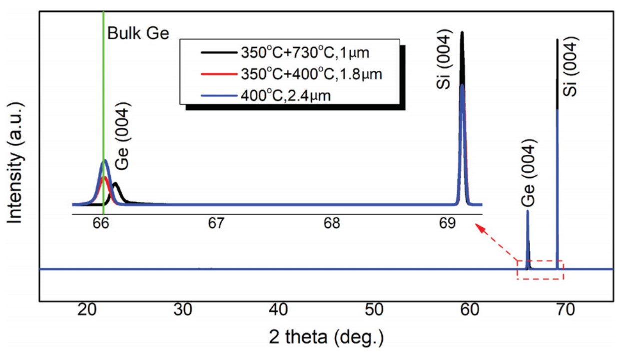


FIG. 3. XRD plot for LT Ge grown at 400 °C both with (red) and without (blue) a 350 °C buffer layer, and HT Ge grown via the two-step process, 350 °C buffer followed by 730 °C growth step (black). Similar full width half maximum of LT Ge to HT Ge indicates that LT Ge is also single crystalline and exhibits similar defect density.

$$\beta_D = \frac{k\lambda}{D\cos(\theta)}, \tag{1}$$

where β_D is the peak broadening (full width half maximum), k is the crystallite shape factor taken as 1 based on the 100 reflection from a cubic crystal,[19] λ is the x-ray wavelength, D is the crystallite size, and θ is the Bragg angle. The size of the "crystallite" is interpreted as the spacing between heterogeneous strain in the material or the distance between dislocations. The dislocation density is calculated as

$$\rho = \frac{1}{D^2} = 2 \times 10^9\ \text{cm}^{-2}. \tag{2}$$

We estimate dislocation density of $\approx 10^9$ cm^{-2} from XRD for LT Ge, which is also typical of HT Ge TDDs pre-cyclic annealing.[6]

The difference in thermal expansion coefficients of Ge and Si leads to a thermal shear stress experienced by Ge upon cooling, resulting in a build-up of tensile strain in Ge during cooling to room temperature. We anticipate that tensile strain will be lower in LT Ge than in HT Ge. We calculate the perpendicular strain in the film via

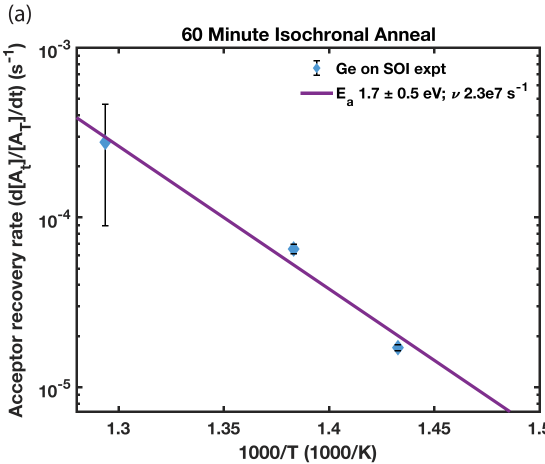
$$\varepsilon_\perp = \frac{d_{400}^{film} - d_{400}^{bulk}}{d_{400}^{bulk}}, \tag{3}$$

where d_{400}^{film} is the spacing of the Ge(400) planes obtained from the $K\alpha_1$ peak in XRD and d_{400}^{bulk} is the spacing between bulk Ge(400) planes, 0.1414 nm. The film is under biaxial stress so the perpendicular strain is related to the in-plane strain via

$$\varepsilon_\parallel = \varepsilon_\perp \left(-\frac{C_{11}}{2C_{12}}\right), \tag{4}$$

where $C_{11} = 128.5$ GPa and $C_{12} = 48.3$ GPa are Ge's elastic constants.[20] We find that LT Ge exhibits low 0.05% tensile strain.

Reactions between point defects and dislocations were investigated to understand the mechanism behind conductivity type conversion in LT Ge. Hall effect measurements were employed to determine the majority carrier density and mobility of LT Ge-on-Si epitaxial films. Isothermal anneals at 450 °C and 60-min isochronal anneals (Fig. 4) were conducted in an *ex situ* quartz tube furnace in N_2 ambient post-growth. As-grown (AG), undoped LT Ge exhibited p-type conductivity with a carrier density of 3.0×10^{16} cm^{-3} $\pm 0.7 \times 10^{16}$ cm^{-3}. Other studies report background p-type carrier density in the $10^{17}-10^{18}$ cm^{-3} range for CVD grown Ge-on-Si at 380–900 °C.[21,22] Annealing of 500 nm thick LT Ge films at 500 °C for 60 min consistently resulted in type conversion to n-type Ge with average carrier density of 2.2×10^{17} cm^{-3} $\pm 1.7 \times 10^{17}$ cm^{-3}. The mechanism for type conversion and the temperature range at which it occurs implies either (1) acceptor-like defects are annihilated or (2) donor states are introduced upon annealing. We later show that TDD reduction by climb is consistent with case 1, increase in native n-type character by the removal of acceptors. In our analysis, any p-type carrier density measured is interpreted as p-type carrier compensation of the underlying n-type conductivity. The total acceptor density, according to this model, is the sum of the initial hole concentration, p_0, measured in the AG devices plus the final electron concentration, n_f, measured in the annealed devices: $[A_T] = p_0 + n_f$. The acceptor removal reaction kinetics are followed as changes in acceptor density at time t, $[A_t]$. When the annealed Ge measures p-type at time t,



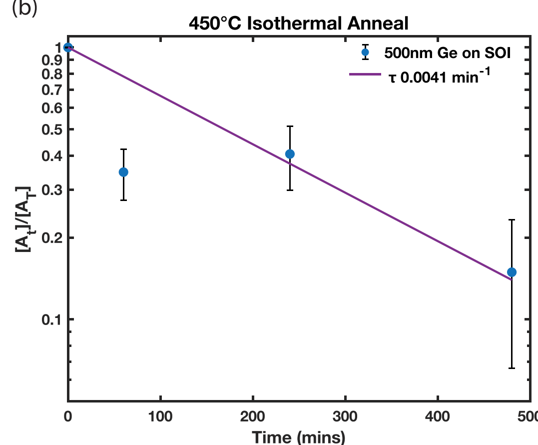


FIG. 4. (a) Effect of 60 min isochronal anneals on acceptor annealing rate in LT Ge. (b) Effect of 450 °C isothermal anneals on acceptor fraction in LT Ge.

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$[A_t] = [A_T] - (p_0 - p_t)$, and when annealed Ge measures n-type, $[A_t] = [A_T] - (p_0 + n_t)$. We observe from isothermal anneals [Fig. 4(b)] that the change in acceptor density follows first order reaction kinetics, exhibiting a single time constant, exponential decay. Sources of error for the 60 min point include the following: (1) additional temperature equilibration and loading/unloading time estimated at 10–15 min, resulting in a faster reaction rate from an underestimate of annealing time and (2) material non-uniformity. The decay rate is expressed as

$$\frac{d[A_t/A_T]}{dt} = \nu \exp\left(\frac{-E_a}{k_B T}\right), \quad (5)$$

where A_T determines the end point of the exponential acceptor decay; ν is the pre-exponential factor representing the success rate for each attempt to react; E_a is activation barrier to the defect reaction; k_B is the Boltzmann constant; and T is the temperature in Kelvin. The best fit line for isochronal decay rate Arrhenius dependence [Fig. 4(a)] yields a pre-exponential factor of 2.3×10^7 s^{-1} and E_a of 1.7 ± 0.5 eV. The pre-exponential factor ν can be expressed as the diffusion jump attempt frequency divided by the number of jumps it takes to reach a sink to annihilate,[23]

$$\nu = \frac{\nu_{attempt}}{N_j}. \quad (6)$$

We estimate ν for a diffusion limited reaction within the Ge layer to be 2×10^6 s^{-1}, as follows. The attempt frequency is taken as the Debye frequency[24] in Ge at room temperature, 7.5×10^{12} s^{-1}, and the expected number of random walk diffusion jumps of interatomic distance, a, through the 500 nm thickness, t_{Ge}, of the Ge is approximately $N \approx (\frac{t_{Ge}}{a})^2 = 3.2 \times 10^6$. The estimated pre-exponential factor is within one order of magnitude of the measured value, which is consistent with a diffusion-limited process.[23] The relevant time and temperature scales of this acceptor annealing reaction can be utilized for *in situ* annealing in interval growth steps of LT Ge for future Ge-on-Si photodetectors, where Ge films should be intentionally doped higher than the n-type density post-annealing to achieve desired device performance.

Dislocation microstructure in AG and 500 °C annealed-LT Ge was investigated via TEM cross sections in Fig. 5. Misfit dislocations (MDs) form at the Si-Ge interface to relieve strain when the low temperature buffer layer reaches the critical thickness. These MDs terminate at a surface, via threading dislocations.[25] We estimate $\approx 10^{10}$–10^{11} cm^{-2} TDD in AG LT Ge [Fig. 5(a)]. Every distinguishable dislocation above the interface was counted, including dislocations that did not completely thread to the surface to best inform defect reactions. The smaller estimate of TDD from XRD, 10^9 cm^{-2}, is due to averaging over the entire film thickness. Annealing at 500 °C for 60 min results in similar microstructure and TDD to the AG sample [Fig. 5(b)]. We use vertical and slanted dislocations to describe dislocations with line vector perpendicular and at 60° to the interface, respectively. From g · b analysis [Figs. 5(c) and 5(d)] of the AG LT Ge, we observed that some vertical threading dislocations (VTDs) appeared only in cross sections imaged along the [220] direction but did not appear along the [004] direction. We concluded that these are pure edge, or 90°, dislocations with Burgers vector in the ⟨110⟩ direction.[26] The constant presence of threading dislocations in both AG and 500 °C-annealed Ge (where we have measured n-type conductivity) demonstrates that

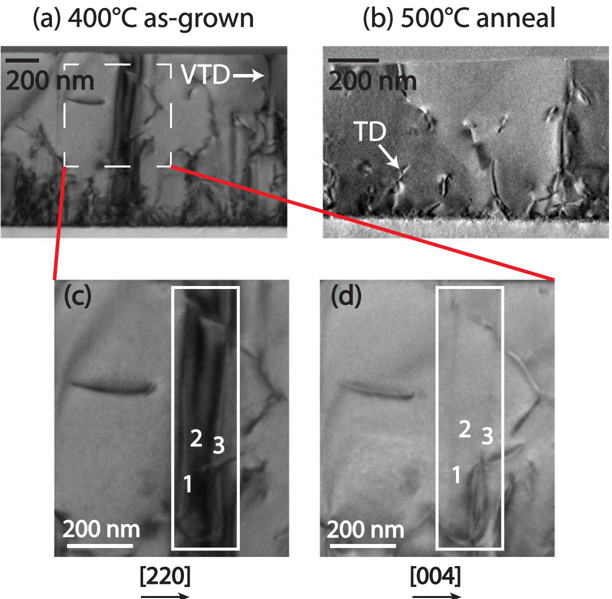

FIG. 5. Characteristic dislocation distribution in LT Ge (a) as-grown and (b) after post-growth 60 min anneal *in situ* at 500 °C. VTD density is slightly reduced after annealing at 500 °C, while the typical slanted TDD remained the same. LT Ge AG cross sections were also imaged along the (c) [220] and (d) [004] directions for g · b analysis. VTDs 1, 2, and 3 appear in the [220] cross section but 1 and 3 only appear very faintly in the [004] cross section and 2 is completely absent, indicating that 1, 2, and 3 are pure edge dislocations with Burgers vectors parallel to the ⟨110⟩ direction.

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neither vertical nor slanted TDs are responsible for p-type compensation of undoped Ge as was previously believed.[27,28]

Conductivity type conversion due to point defect–dislocation interactions has been studied in plastically deformed bulk Si[29–31] and bulk Ge.[32] Grillot *et al.* postulated that increased dislocation reactions generated acceptor-like point defects in plastic relaxation-induced conductivity type conversion in SiGe-Si heterostructures.[33] Acceptor-like traps in Ge-on-Si have also been associated with either impurities decorating dislocations or relaxation induced point defect clusters.[34] The impact of point defects on Ge-on-Si photodetector performance has been implied by improvement in device performance of Ge on SiGe buffer layers at annealing temperatures that kept TDD constant. These point defects were also attributed to relaxation-induced point defect clusters.[35] Conversely, we have shown that acceptor-like point defects are natively present in UHVCVD-grown LT Ge. When Ge is grown in far-from-equilibrium conditions, such as LT growth of 400 °C,[36] supersaturations of point defects are readily present. Due to the low contamination and low base pressure of UHVCVD, a supersaturation of vacancies is likely this acceptor-like defect. Additionally, we observed a drastic reduction in VTD density at 600 °C, which is surprising given some VTDs are sessile and the temperature is prohibitive to dislocation glide. The annihilation of vertical dislocations at temperatures where dislocations do not have enough energy to glide distances required to annihilate[37,38] is evidence that inherent acceptor-like point defects are participating in point defect-mediated climb of vertical dislocations. Point defects may also annihilate at self-interstitial defects, stacking faults, and surfaces. Type conversion may

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also occur in lower dislocation dense films if defects generated from dislocation interactions do not alter conductivity type compensation. Future work is necessary to determine the contributions of these various pathways to acceptor annihilation and type conversion.

In conclusion, we developed a BEOL-compatible Ge-on-Si epitaxial growth process, incorporating a pre-growth Si clean that can be conducted at room temperature to achieve specular, planar Ge films. We found that LT Ge exhibits very low tensile strain, 0.05%, and XRD indicates that LT Ge is single crystalline with similar defect density to typical HT Ge pre-cyclic annealing. We conducted Hall effect to identify conductivity type conversion that occurs in our materials upon post-growth anneals between 450 and 500 °C with an activation energy of 1.7 ± 0.5 eV. We correlated this type conversion with the annihilation of acceptor-like defects by first order, diffusion limited reaction kinetics. We established that point defects are responsible for p-type conductivity of as-grown Ge and not dislocations as was previously understood. VTD density reduction at low temperatures was attributed to point defect-mediated climb, demonstrating that dislocation sinks may be beneficial to recovery of points defects at low temperatures. The low temperature pre-clean and growth recipe developed in this work can be used for BEOL-compatible Ge-on-Si epitaxy. Understanding the impact of point defect–dislocation interactions in conductivity type conversion is an important step forward in the development of high performing BEOL-compatible Ge-on-Si photodetectors for optical interconnects.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Eveline Postelnicu: Conceptualization (equal); Formal analysis (lead); Investigation (lead); Methodology (lead); Visualization (lead); Writing – original draft (lead). **Rui-Tao Wen:** Conceptualization (supporting); Investigation (supporting); Resources (equal); Writing – review & editing (equal). **Danhao Ma:** Investigation (supporting); Resources (equal); Writing – review & editing (equal). **Baoming Wang:** Investigation (supporting); Resources (equal). **Kazumi Wada:** Conceptualization (equal); Funding acquisition (equal); Resources (equal); Supervision (equal); Writing – review & editing (equal). **Jurgen Michel:** Conceptualization (equal); Funding acquisition (equal); Resources (equal); Supervision (equal); Writing – review & editing (equal). **Lionel C. Kimerling:** Conceptualization (equal); Funding acquisition (equal); Resources (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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