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ABSTRACT

Integration of near-infrared photodetectors in the back-end-of-line requires low temperature growth of Ge (<450 °C). We have fabricated high performance, vertical incidence Ge-on-Si photodiodes under thermal budget constraints with as-grown diodes achieving an internal quantum efficiency (IQE) of 38% and a dark current density of $J_d = 272 \mu\text{A}/\text{cm}^2$ at a reverse bias of $V_r = 5 \text{ V}$ and a wavelength of $\lambda = 1310 \text{ nm}$. The photodiode design incorporates a remote heterointerface, demonstrating that Ge material quality is sufficiently high for minority carriers to diffuse to the Ge/Si interface. Post-growth annealing improves device performance, including 500 °C 3 h exposure that improves IQE to 57% and $J_d = 165 \mu\text{A}/\text{cm}^2$. Low-temperature grown Ge-on-Si photodiodes give comparable performance to diodes processed at high temperatures despite thermal budget constraints.

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Photodetection in the near-infrared is widely used in optical communication, imaging, and spectroscopy. III–V materials perform well at telecommunication wavelengths (1.3–1.6 μm), but CMOS incompatibility has proven to be a significant hurdle, inspiring research in alternative solutions. In particular, monolithic integration of Ge on Si has been researched extensively.¹ Optimized SiGe graded buffer layers were used to achieve low threading dislocation densities (TDDs),^{2,3} but the thick buffer layers had integration difficulties. Thin buffer layers deposited at low temperatures were developed as part of a two-step growth process in UHVCVD, achieving low TDD that was further reduced with cyclic annealing.⁴ High performance photodetectors using this methodology have since been reported,^{5–7} and Ge photodetectors are currently included in photonic foundry PDKs.⁸

However, the remaining limitations of Ge optoelectronic integration with Si CMOS circuits reduce design flexibility and increase device size. The metal interconnect layers in the back-end-of-line (BEOL) serve as the ideal placement for these photodetectors, but high quality Ge growth on an amorphous substrate and a strict thermal budget of < 450 °C are required.¹ The lack of a semiconductor substrate was addressed with single crystalline Ge growth on SiO₂ at 450 °C using 2D confinement.^{9,10} Alternatively, a process may not need to be integrated in the interlayer dielectric (ILD), but it must be

compatible with existing metal interconnects and satisfy the required thermal budget. Low temperature deposition methods, such as e-beam evaporation^{11–13} and molecular beam epitaxy,¹² have also been attempted, but each technique revealed performance limitations. In this work, high performing Ge photodiodes were grown on a Si substrate at BEOL-compatible temperatures.

Ge was grown epitaxially via low pressure chemical vapor deposition (LP-CVD) and ultra-high vacuum chemical vapor deposition (UHV-CVD) on a p-Si epi (10^{15} – 10^{16} cm^{-3})/n-Si substrate ($2 \times 10^{18} \text{ cm}^{-3}$) at nominal 400 °C growth and fabricated into remote heterointerface photodetectors, as shown in Fig. 1. Ge mesas with radii of 250 μm –2 mm were defined via chlorine-based RIE-etching. The metal contacts consisting of Ti (20 nm)/TiN (20 nm)/Al (300 nm) were deposited with an E-beam evaporator and patterned using standard lithography and liftoff methods. Devices were passivated with 20 nm Al₂O₃ and predominantly showed a dark current dependence with area as opposed to diode periphery.

Photoresponse measurements were performed using a laser diode pigtailed with a single-mode optical fiber at $\lambda = 1310 \text{ nm}$. A Keithley sourcemeter was used in conjunction with an optical chopper and a bias tee in order to direct the modulated photocurrent to a lock-in amplifier. Measurements were taken at 1 V intervals on separate

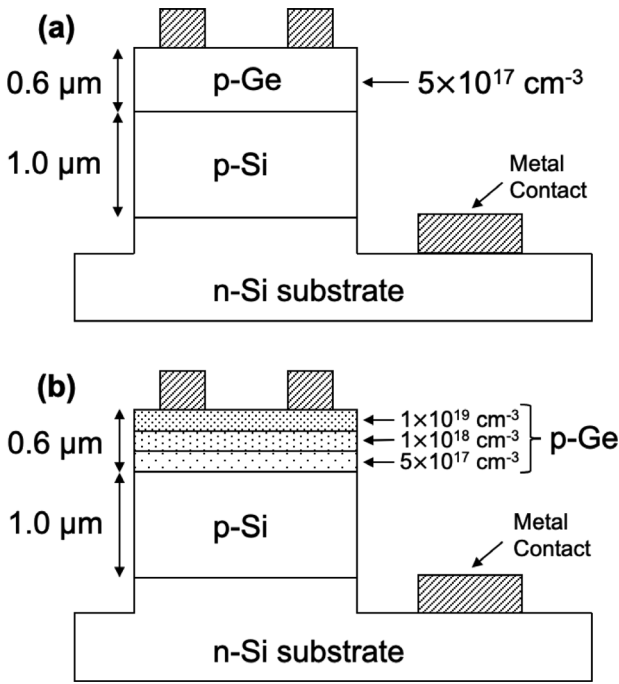


FIG. 1. Schematic of the Ge-on-Si photodiode with (a) uniform doping in the Ge layer and (b) graded boron doping in the Ge layer. The doping concentrations were p-Si = 10^{15} – 10^{16} cm^{-3} and n-Si = 2×10^{18} cm^{-3} .

devices with each error bar representing a 68% confidence interval. Due to the thin Ge absorption layer, internal quantum efficiency (IQE) was used as a performance metric for device quality. Responsivity measurements are also reported to aid in comparison with the literature, despite the lack of adjustment for surface reflection or absorption for a given Ge thickness.

The photodetector designs in Fig. 1 share some characteristics with a uni-traveling carrier (UTC) photodiode structure such as an absorbing p-Ge layer and ballistic electron transport in the depleted collector (p-Si/n-Si).¹⁴ The design selection was motivated by potential for lower leakage current and evaluation of carrier recombination at the Ge/Si interface. In addition, the incorporation of graded boron (B) doping in Fig. 1(b) generates an electric field in Ge, which promotes a drift current in order to reduce recombination at the Ge surface and transit time to the Ge/Si interface. Similar examples of this device structure grown at elevated temperatures have been reported in the literature.^{15–17}

Figure 2 illustrates the quantum efficiency of uniform and graded doping devices from Fig. 1. Devices with graded B-doping had higher IQE at $\lambda = 1310$ nm by approximately 4%–5% relative to devices with uniform Ge doping. However, the latter achieved a remarkable responsivity of 0.10 A/W and an IQE of 34% at $V_r = 5$ V without annealing, despite the reliance on carrier diffusion to the Ge/Si interface. The minority carrier lifetime of low-temperature grown Ge was, therefore, sufficiently high to largely overcome diffusion time in the 0.6 μm Ge absorption layer.

The IQE turn-on at $V_r = 3$ –4 V in Fig. 2 marks the range over which the p-Si region approaches full depletion such that the E field

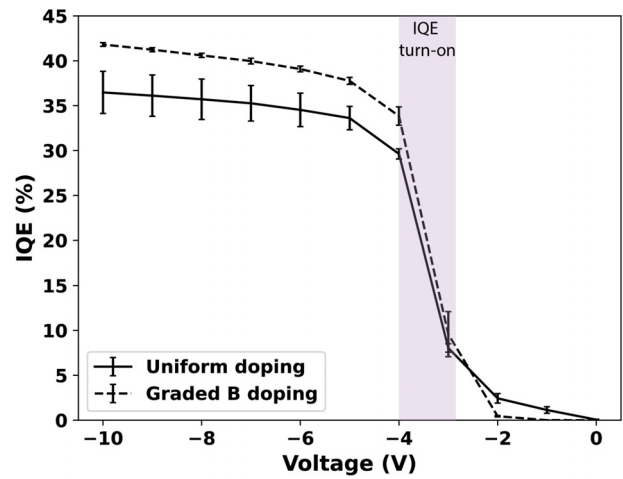


FIG. 2. Internal quantum efficiency at $\lambda = 1310$ nm of low-temperature, as-grown Ge-on-Si devices with uniform and graded doping in Ge.

may reach the Ge/Si interface. At zero bias, the device structure inherently includes E fields from both the p-Ge/p-Si interface and the p-Si/n-Si junction. The E field at the interface results in an energy barrier that inhibits carrier collection at zero bias, as shown in the energy band diagram of Fig. 3. The inset plot in Fig. 3 shows that a reverse bias of $V_r = 5$ V is required for the E field from the homojunction in silicon to extend to the interface and fully lower the barrier. The minor increase in IQE between $V_r = 5$ and 10 V results from slight extension of the depletion zone into the highly doped p-Ge. The higher E field in p-Ge also provides faster drift transport through the defective Ge/Si interface and minimizes carrier recombination.

The voltage required to lower the energy barrier (V_{barrier}) is quadratic in p-Si thickness and linear with p-Si doping concentration.

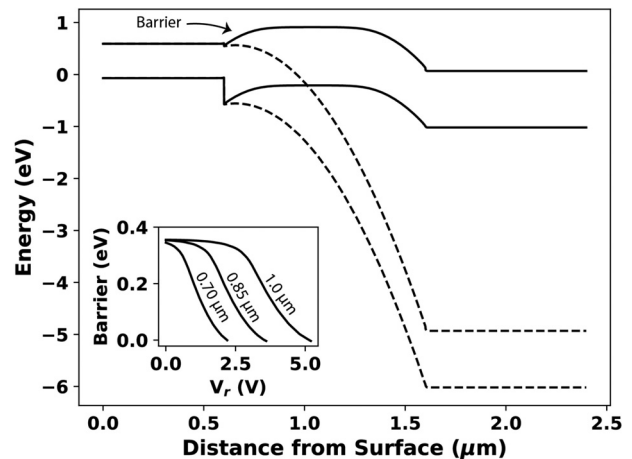


FIG. 3. Simulated energy band diagrams for a Ge-on-Si device with uniform Ge doping at $V_r = 0$ V (solid) and $V_r = 5$ V (dashed). In the band diagrams, the doping concentration of p-Si = 8×10^{15} cm^{-3} and p-Si thickness = 1.0 μm . The inset plot shows the reduction in the energy barrier at the p-Ge/p-Si interface with reverse bias for several p-Si thicknesses.

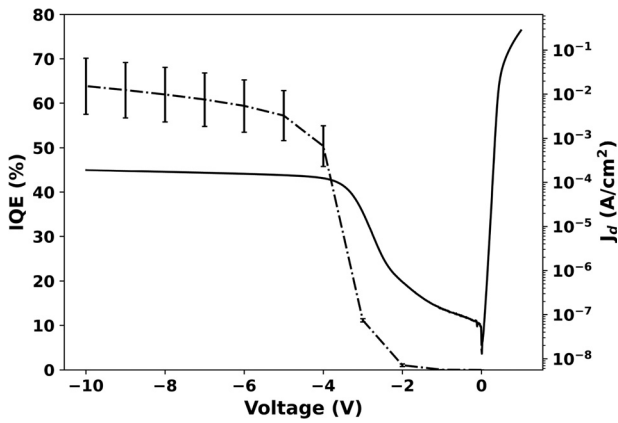


FIG. 4. Dark current density J_d (solid) and IQE (dotted-dashed) at $\lambda = 1310$ nm of a Ge-on-Si photodiode with graded B-doping, annealed at 500°C for 3 h.

This relation may be obtained from Eq. (1), where $x_p(V)$ represents the depletion of p-Si at a given voltage for an asymmetric junction. The final result in Eq. (2) is obtained by approximating that V_r is much greater than the built-in voltage (ϕ_{bi}) and by recognizing that $V_r = V_{\text{barrier}}$ when $x_p(V)$ is equivalent to the p-Si thickness ($t_{p\text{-Si}}$). The expected reduction of V_{barrier} with reduced $t_{p\text{-Si}}$ is also shown in the inset plot of Fig. 3. Increasing $t_{p\text{-Si}}$ from 0.7 to $1.0\ \mu\text{m}$ causes V_{barrier} to roughly increase from 2.5 to 5.0 V, which is consistent with the relation in Eq. (2). Although Si doping parameters directly impact V_{barrier} , device measurements at voltages exceeding V_{barrier} result in responsivity and J_d values that are primarily determined by the Ge crystal quality,

$$x_p(V) = \sqrt{\frac{2\epsilon(\phi_{bi} - V)}{qN_A}}, \quad (1)$$

$$V_{\text{barrier}} \propto t_{p\text{-Si}}^2 N_A. \quad (2)$$

The possibility of further improving the device performance with low temperature anneals ($500\text{--}550^\circ\text{C}$) was motivated by Hall effect results of undoped Ge epitaxy on SOI, grown via UHV-CVD at low temperatures. The conductivity of Ge was initially p-type, and heat

TABLE I. Impact of annealing conditions on IQE and J_d at $\lambda = 1310$ nm of Ge-on-Si photodiodes with graded B-doping. J_d is reported at $V_r = 5$ V, and IQE is reported at $V_r = 10$ V. IQE measurements took into account surface reflection and Ge layer absorption, while responsivity values were calculated only using incident light.

	As-grown	500°C 3 h	550°C 1 h
IQE (%)	41.8 ± 0.2	63.8 ± 6.3	58.6 ± 4.3
Responsivity (A/W)	0.12 ± 0.00	0.19 ± 0.02	0.17 ± 0.01
J_d ($\mu\text{A}/\text{cm}^2$)	272 ± 4	165 ± 40	110 ± 4

treatments at 450°C converted the Ge to n-type conductivity. The p to n-type conversion followed first-order kinetics with 1.7 eV activation energy and was associated with acceptor-like point defect removal.¹⁸ Annealing of the Ge epilayer in photodiodes was projected to improve the device performance by the same mechanism, and the level of IQE improvement could be correlated with the reduction in the point defect density for a given annealing time and temperature.

The Ge-on-Si photodiode with the highest collection efficiency was annealed at 500°C for 3 h with J_d and IQE shown in Fig. 4. As expected from device design, J_d was suppressed at low voltages and increased to near its final value of $165\ \mu\text{A}/\text{cm}^2$ at $V_r = 5$ V. Responsivity improved with annealing from 0.11 A/W at $V_r = 5$ V as-grown to 0.17 A/W after 500°C 3 h. Although the theoretical responsivity limit at $\lambda = 1310$ nm is 1.06 A/W, the $0.6\ \mu\text{m}$ Ge layer only absorbs 45% of the incident light, reducing the responsivity limit to 0.48 A/W. The surface reflection due to lack of anti-reflection (AR) coating further reduces the maximum possible responsivity to 0.30 A/W. In our design, a perfect AR coating would increase responsivity of as-grown and 500°C 3 h annealed devices to 0.18 and 0.27 A/W, and complete absorption in the 600 nm Ge epi would further increase responsivity values to 0.40 and 0.60 A/W, respectively.

The impact of $500\text{--}550^\circ\text{C}$ annealing on IQE for Ge-on-Si photodiodes with graded B-doping is shown in Table I. Annealing reduced J_d by $\sim 100\text{--}150\ \mu\text{A}/\text{cm}^2$ for graded B-doped devices, and photodiodes with uniform doping exhibited a similar trend. The annealing conditions of 500°C 3 h and 550°C 1 h increased IQE by $\sim 19\%$ and were not statistically different from one another. This similarity in IQE improvement is supported by the defect kinetics model, as relatively small acceptor-like point defect fractions under 5% were expected for

TABLE II. Comparison of device performance and process parameters for normal-incidence Ge-on-Si photodiodes. The wavelength, presence of AR coating, and Ge thickness are included for each device to aid in interpretation of the responsivity, but design and measurement variations prevent direct comparison. The responsivity and J_d of a given reference are reported at the same reverse bias, V_r .

	Responsivity (A/W)	AR coating	λ (nm)	Ge (μm)	J_d ($\mu\text{A}/\text{cm}^2$)	V_r (V)	Max process temperature ($^\circ\text{C}$)	Design
This work	0.17	N	1310	0.6	165	5	500	p-Ge/p-Si/n-Si
	0.11	N	1310	0.6	272	5	450	p-Ge/p-Si/n-Si
State-of-the-art	Piels and Bowers (2012) ¹⁵	Y	1310	0.8	35,000	1	< 800	p-Ge/i-Si/n-Si
	Osmond <i>et al.</i> (2009) ¹⁹	Y	1550	1.0	63	3	780	p-Ge/i-Ge/n-Si
	Lin <i>et al.</i> (2021) ²⁰	N	1550	1.1	780	1	750 (300 $^\circ\text{C}$ wafer bonded)	p-Ge/i-Ge/n-Ge
Sorianello <i>et al.</i> (2012) ¹¹	0.1	N	1550	1.3	200,000	1	580	p-Ge/n-Si
Colace <i>et al.</i> (2007) ¹³	0.002	N	1310	...	700	1	< 300	poly-Ge/n-Si

both annealing conditions relative to as-grown material. Although the 500–550 °C anneals were beyond BEOL-compatibility, the observed device improvements with annealing reinforced some of the findings in prior work, in particular, the conductivity type conversion with annealing.¹⁸

A comparison with previous work on Ge-on-Si photodiodes processed in a wide temperature range demonstrates competitive responsivity and dark current density in our low-temperature grown photodiodes. Low-energy plasma-enhanced chemical vapor deposition growths are performed at 450–500 °C followed by 780 °C cyclic annealing resulted in $J_d = 41 \mu\text{A}/\text{cm}^2$ and $0.4 \text{ A}/\text{W}$ at $\lambda = 1.55 \mu\text{m}$,¹⁹ while UHV-CVD growths on 10 μm thick, optimized relaxed buffers yielded $J_d = 150 \mu\text{A}/\text{cm}^2$ and $0.13 \text{ A}/\text{W}$ at $\lambda = 1.3 \mu\text{m}$.³ In a different approach, a BEOL-compatible process designed for low-temperature bonding and layer transfer at 300 °C has deposited Ge epitaxy via metal organic chemical vapor deposition and included a furnace anneal in O_2 at 750 °C, yielding a responsivity of $0.29 \text{ A}/\text{W}$ and $J_d = 780 \mu\text{A}/\text{cm}^2$ at $\lambda = 1.55 \mu\text{m}$.²⁰ Table II provides a performance summary of comparable device structures with process parameters included.

High performance was demonstrated in this work for low-temperature grown Ge-on-Si photodiodes with and without post-growth annealing. Responsivity and dark current density comparable to devices processed at high temperatures were achieved at thermal budget conditions of $< 450 \text{ }^\circ\text{C}$. As-grown diodes showed a responsivity of $0.11 \text{ A}/\text{W}$ and $J_d = 272 \mu\text{A}/\text{cm}^2$ at $V_r = 5 \text{ V}$, and annealing conditions of 500 °C 3 h improved such performance to $0.17 \text{ A}/\text{W}$ and $J_d = 165 \mu\text{A}/\text{cm}^2$. Relating the observed improvements in IQE with point defect annihilation highlighted the importance of point defects in the Ge material quality and addressed that the threading dislocation density is not the only significant factor in characterization of defects for Ge epitaxy.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Stephanie Epstein Marzen: Data curation (equal); Formal analysis (equal); Investigation (lead); Methodology (supporting); Validation (lead); Visualization (lead); Writing – original draft (lead); Writing – review & editing (lead). **Eveline Postelnicu:** Conceptualization (lead); Data curation (equal); Formal analysis (equal); Investigation (supporting); Methodology (supporting); Resources (equal); Writing – original draft (supporting); Writing – review & editing (supporting). **Jurgen Michel:** Conceptualization (supporting); Funding acquisition (equal); Methodology (supporting); Project administration (equal); Resources (equal); Supervision (equal); Writing – review & editing (supporting). **Kazumi Wada:** Conceptualization (supporting); Funding acquisition (equal); Methodology (lead); Project administration (equal); Resources (equal); Supervision (equal); Writing – review & editing (supporting). **Lionel C. Kimerling:** Conceptualization (supporting); Funding acquisition (equal); Methodology (supporting); Project administration (equal); Resources (equal); Supervision (equal); Writing – review & editing (supporting).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

- 1J. Michel, J. Liu, and L. C. Kimerling, “High-performance Ge-on-Si photodetectors,” *Nat. Photonics* **4**, 527–534 (2010).
- 2E. A. Fitzgerald, Y. Xie, M. L. Green, D. Brasen, A. R. Kortan, J. Michel, Y. Mii, and B. E. Weir, “Totally relaxed $\text{Ge}_x\text{Si}_{1-x}$ layers with low threading dislocation densities grown on Si substrates,” *Appl. Phys. Lett.* **59**, 811–813 (1991).
- 3S. Samavedam, M. T. Currie, T. A. Langdo, and E. A. Fitzgerald, “High-quality germanium photodiodes integrated on silicon substrates using optimized relaxed graded buffers,” *Appl. Phys. Lett.* **73**, 2125–2127 (1998).
- 4H.-C. Luan, D. R. Lim, K. K. Lee, K. M. Chen, J. G. Sandland, K. Wada, and L. C. Kimerling, “High-quality Ge epilayers on Si with low threading-dislocation densities,” *Appl. Phys. Lett.* **75**, 2909–2911 (1999).
- 5G. Masini, L. Colace, G. Assanto, H.-C. Luan, K. Wada, and L. C. Kimerling, “High responsivity near infrared Ge photodetectors integrated on Si,” *Electron. Lett.* **35**, 1467–1468 (1999).
- 6L. Colace, G. Masini, G. Assanto, H.-C. Luan, K. Wada, and L. C. Kimerling, “Efficient high-speed near-infrared Ge photodetectors integrated on Si substrates,” *Appl. Phys. Lett.* **76**, 1231–1233 (2000).
- 7J. Liu, D. D. Cannon, K. Wada, Y. Ishikawa, S. Jongthammanurak, D. T. Danielson, J. Michel, and L. C. Kimerling, “Tensile strained Ge *p-i-n* photodetectors on Si platform for C and L band telecommunications,” *Appl. Phys. Lett.* **87**, 011110 (2005).
- 8E. Timurdogan, Z. Su, C. V. Poulton, M. J. Byrd, S. Xin, R.-J. Shiu, B. R. Moss, E. S. Hosseini, and M. R. Watts, “AIM process design kit (AIMPDKv2.0): Silicon photonics passive and active component libraries on a 300 mm wafer,” in *Optical Fiber Communication Conference* (Optica Publishing Group, 2018) p. M3F.1.
- 9K. A. McComber, X. Duan, J. Liu, J. Michel, and L. C. Kimerling, “Single-crystal germanium growth on amorphous silicon,” *Adv. Funct. Mater.* **22**, 1049–1057 (2012).
- 10B. S. Pearson, L. C. Kimerling, and J. Michel, “Germanium photodetectors on amorphous substrates for electronic-photonics integration,” in *2016 IEEE 13th International Conference on Group IV Photonics (GFP)* (IEEE, 2016), pp. 20–21.
- 11V. Soriano, A. De Iacovo, L. Colace, A. Fabbri, L. Tortora, E. Buffagni, and G. Assanto, “High responsivity near-infrared photodetectors in evaporated Ge-on-Si,” *Appl. Phys. Lett.* **101**, 081101 (2012).
- 12P. Bandaru, S. Sahni, E. Yablonoitch, J. Liu, H.-J. Kim, and Y.-H. Xie, “Fabrication and characterization of low temperature ($< 450 \text{ }^\circ\text{C}$) grown p-Ge/n-Si photodetectors for silicon based photonics,” *Mater. Sci. Eng. B* **113**, 79–84 (2004).
- 13L. Colace, G. Masini, S. Cozza, G. Assanto, F. DeNotaristefani, and V. Cencelli, “Near-infrared camera in polycrystalline germanium integrated on complementary-metal-oxide semiconductor electronics,” *Appl. Phys. Lett.* **90**, 011103 (2007).
- 14T. Ishibashi and H. Ito, “Uni-traveling carrier photodiodes: Development and prospects,” *IEEE J. Sel. Top. Quantum Electron.* **28**, 1–6 (2022).
- 15M. Piels and J. Bowers, “Si/Ge uni-traveling carrier photodetector,” *Opt. Express* **20**, 7488–7495 (2012).
- 16M. Piels and J. E. Bowers, “40 GHz Si/Ge uni-traveling carrier waveguide photodiode,” *J. Lightwave Technol.* **32**, 3502–3508 (2014).
- 17C. Li, C. Xue, Z. Liu, H. Cong, B. Cheng, Z. Hu, X. Guo, and W. Liu, “High-responsivity vertical-illumination Si/Ge uni-traveling-carrier photodiodes based on silicon-on-insulator substrate,” *Sci. Rep.* **6**, 27743 (2016).
- 18E. Postelnicu, R.-T. Wen, D. Ma, B. Wang, K. Wada, J. Michel, and L. C. Kimerling, “Point defect–dislocation interactions in BEOL-compatible Ge-on-Si epitaxy,” *Appl. Phys. Lett.* **123**, 031103 (2023).
- 19J. Osmond, G. Isella, D. Christina, R. Kaufmann, M. Acciarri, and H. von Kaenel, “Ultra low dark current Ge/Si(100) photodiodes with low thermal budget,” *Appl. Phys. Lett.* **94**, 201106 (2009).
- 20Y. Lin, B. Son, K. Lee, J. Michel, and C. Tan, “Sub-mA/cm² dark current density, buffer-less germanium (Ge) photodiodes on a 200-mm Ge-on-insulator substrate,” *IEEE Trans. Electron Devices* **68**, 1730 (2021).