Design and Analysis of a Transformer-Based Solid-State Relay

by

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S.B. Electrical Engineering and Computer Science
Massachusetts Institute of Technology, 2023

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

MASTER OF ENGINEERING IN ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

May 2024

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ABSTRACT

Automatic Test Equipment (ATE) systems require relays to perform complex high-speed tests on semiconductor devices. However, existing relays all come up short in some aspect. Electromechanical reed relays have a limited lifetime and slow switching speeds, while solid-state photoMOS relays have high on-resistance and low bandwidth. This thesis presents the design, simulation, and analysis of a new solid-state relay tailored for ATE applications. We use Analog Devices' iCoupler technology to design this relay, relying on on-chip transformers to provide reliable input-to-output isolation. In Cadence simulations, the iCoupler relay achieves 100 mOhm on-resistance, 7.5 us turn-on time, and 4.8 GHz output 3dB bandwidth.

Thesis supervisor: David J. Perreault
Title: Ford Foundation Professor of Engineering

Thesis supervisor: Ruida Yun
Title: Senior Manager at Analog Devices

Acknowledgments

This thesis would not have happened without Ruida Yun, my manager and mentor at Analog Devices. Not only did Ruida provide invaluable support throughout my thesis work, he also pushed me to take on new challenges during my internship at ADI, and my experience was more rewarding because of it. I also want to thank all of the other talented engineers I met on the ISO team at ADI who helped me feel welcome, including Baoxing, Allison, Adarsh, Yilu, Yulun, Leo, Eric, Nadir, Abhi, Jim, and Chris. Special thanks to Allison and Yulun for helping me debug my Cadence issues, to Yilu and Nadir for joining me on lunch and ice cream breaks, and to Abhi and Jim for the Monday morning football talk.

On the MIT side, I want to first thank Priscilla Capistrano from the 6A program for the help she provided throughout the entire 6A MEng process. I am grateful to Professor David Perreault for his valuable feedback on my thesis, and to Professor Dirk Englund, my academic advisor, for his support in my MIT journey. I am also very thankful to Professor Kerri Cahoy for giving me the opportunity to be an RA in the STAR Lab this spring, an incredible lab full of amazing people that has helped shape my career decisions.

I want to thank my friends Chris, Raiphy, Travis, Ahmad, Ahmed, Spencer, and Matt for the great memories over the past five years. Their support helped me carry on through the tough times.

There is no way I can adequately thank my Mom and Dad in a couple short sentences here, but thank you. Your constant guidance, support, and unconditional love are why I am where I am today. And thank you to my little sister Sneha, the best sibling in the whole world; your bright smile and jokes always cheered me up after a long day at work or school.

Thank you God, for giving me this opportunity and for making all of this possible.

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Chapter 1

Introduction

The global semiconductor industry is currently worth just over half a billion dollars and is projected to break 1 trillion dollars by 2030 [1],[2]. In 2023 alone, the industry shipped over 1 trillion semiconductor units [3]. Chip makers must test all of these units to their design specifications before sending them out. Therefore, chip makers use Automatic Test Equipment (ATE) to perform a large number of tests on chips quickly and accurately.

ATE systems use switches to perform high-speed test sequences on the device under test (DUT). For example, a test may involve connecting a DUT to a voltage source and measuring its output on an oscilloscope. Switches can be programmed to quickly test many DUTs using the same oscilloscope, or test the same DUT on several voltage sources. Switches also allow the ATE system to be easily reconfigured for different devices with different pinouts [4].

However, each switch is a potential source of signal degradation, noise, or interference. Therefore, the ATE switches should be as close to ideal as possible: they should turn on and off instantaneously; they should have infinite resistance when off and no resistance when on; and they should have infinite bandwidth, conducting high-frequency signals with no attenuation or distortion. In addition, there should be a galvanic isolation barrier that prevents current flow between the input control side and the output load side of the switch. This isolation barrier serves two purposes. For one, high-voltage tests are often run on the

DUT, and isolation protects the low-voltage control system and any human operators from electric shock. Secondly, isolation prevents noise from the control circuitry from interfering with the sensitive test signals. For this reason, ATE applications generally use relays, which are electrically-operated switches that have galvanic isolation between their input and output.

One of Analog Devices' customers is looking for a relay to use in their ATE. For this customer, the most important quality is that the resistance of the relay is low and stable. If the resistance of the relay is changing (for example, if the resistance slowly increases over many switching cycles), then the customer would need to recalibrate their equipment. Additionally, the customer desires a relay with a long lifetime, ideally over 1 billion cycles, since relay replacement on ATE can be expensive and time-consuming [5]. On an ATE board with over 1000 relays, fixing even one relay failure could require taking the entire system offline, resulting in costly downtime. In this thesis, we will design a relay that meets the ATE customer's needs for low on-resistance and high reliability, as well as improves on existing relays in other parameters such as switching speed and bandwidth.

Chapter 2

Current Relay Solutions

There are many types of relays currently on the market, ranging from electromechanical to solid-state. However, all of the current relay options fall significantly short of an ideal switch in some way, whether it is high on-resistance, limited lifetime, low bandwidth, or slow switching speed. None of the current market solutions fully meet the ATE customer's need for a relay with low and stable on-resistance.

2.1 Reed Relay

In a reed relay, two electrical contacts made of a ferromagnetic material are enclosed in a glass capsule, and a coil of wire is wrapped around the capsule. By applying a current through the coil, the resulting magnetic field will cause the contacts to either repel or attract each other, causing the switch to open or close [6].

Reed relays are currently the most common relay used in ATE. Because there is physical contact between the terminals, reed relays can have a low on-resistance under 100 mΩ and a 3dB bandwidth of up to 8 GHz. [7]. However, because of the moving physical parts, reed relays are slow at switching, with max operate times ranging from 0.5 ms up to 5 ms [8],[9]. Additionally, the contacts wear down over time and increase the on-resistance; at heavy load conditions above 1 W, a reed relay's lifetime can drop to below 50 million cycles [7]. Finally,

reed relays are large compared to modern integrated-circuit technology, taking up valuable board space on ATE. While reed relays are the traditional ATE solution, they have numerous shortcomings in a market demanding smaller, faster, and more reliable devices.

2.2 MEMS Switch

MEMS, or micro-electromechanical systems, is an integrated-circuit technology that uses both semiconductors and mechanical moving parts. The typical MEMS switch consists of a small bendable armature (about 100 μm wide and several hundred μm long) that can be electrically actuated, as shown in Figure 2.1 [10]. Applying a voltage across the two actuation electrodes causes the armature to bend down and the two contact electrodes to meet, turning the switch on [10]. Other than being much smaller than reed relays, MEMS switches share most of the same advantages and disadvantages. They have low on-resistance and high bandwidth, but suffer from limited lifetime. At hot switching of 1 W loads, the lifetime of MEMS devices can drop to 400,000 cycles [7]. In fact, the ATE customer previously used MEMS switches in their equipment but had significant issues with on-resistance drift and unreliable turn-on, and therefore decided to move away from them.

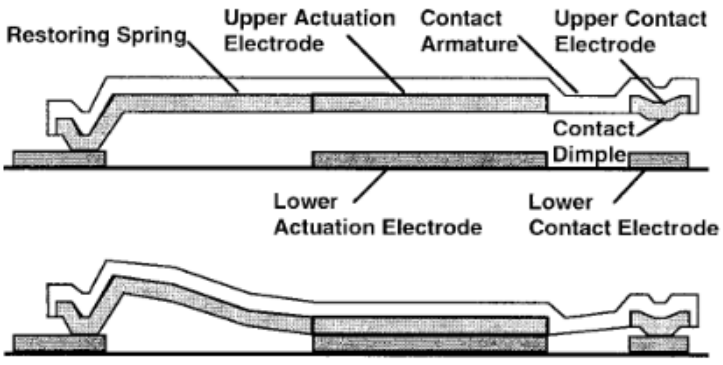


Figure 2.1: MEMS switch in open and closed configuration [10]

2.3 PhotoMOS Relay

While the reed relay and the MEMS switch are electromechanical switches, the photoMOS relay is a solid-state switch, involving no moving parts. In addition, the photoMOS relay uses an optical solution for isolation. When a small current is applied on the control side of the relay, an LED inside the relay turns on. The emitted light from this LED turns on a photodiode on the isolated load side. Circuitry on the load side then turns on the output MOSFET that conducts the load signal [11]. Because there are no moving parts, photoMOS relays have a longer lifetime compared to mechanical relays. However, photoMOS relays still suffer somewhat from reliability issues; the LED can degrade over time, and the LED luminosity and turn-on time will change depending on operating temperature [12], [13]. LED wear-out will cause the on-resistance to increase near the end of the photoMOS relay's lifetime. PhotoMOS relays do have a faster switching time of around 50-250 μs [13]; the downside is that they also have a high on-resistance (around 1-10 Ω for 60-80V load devices [13]) and a lower bandwidth than reed relays due to higher output capacitance [7]. As a result, photoMOS relays are not ideal for the ATE customer either.

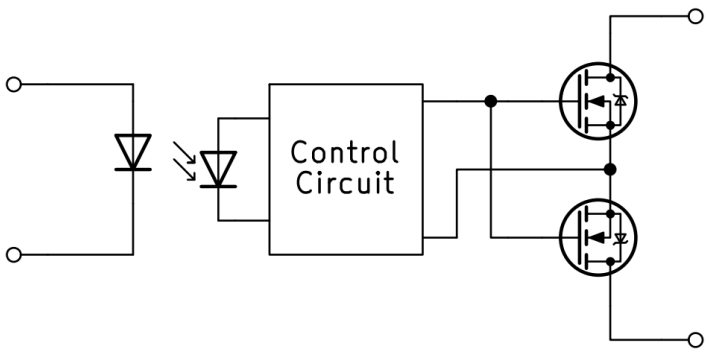


Figure 2.2: circuit diagram of a typical photoMOS relay

Chapter 3

Proposed iCoupler Relay

We want to design a relay that combines the best qualities of electromechanical reed relays (low on-resistance and high bandwidth) and best qualities of solid-state photoMOS relays (fast switching speeds and long lifetime). We also want our relay to offer high reliability and isolation performance. The goal is to create a relay that is not only ideal for Analog Devices' ATE customer, but also for modern ATE systems in general.

3.1 iCoupler Overview

In order to achieve reliable galvanic isolation and long lifetime, the proposed relay will use Analog Devices' proprietary iCoupler technology. iCoupler uses on-chip planar transformers; as shown in Figure 3.1, these transformers are built with a top and bottom metal coil and a polyimide dielectric sandwiched in between. This polyimide dielectric has a high breakdown strength (over thousands of volts), high thermal and mechanical stability, and good ESD performance [14]. Analog Devices already has several iCoupler products that offer reliable isolation for digital and power applications, including the ADuM3166 (a USB 2.0 digital isolator that provides 3750 Vrms isolation) and the ADuM4221 (an isolated gate driver with 5700 Vrms isolation) [15], [16]. Since iCoupler has a proven history of excellent isolation performance, it is a good choice for the solid-state relay.

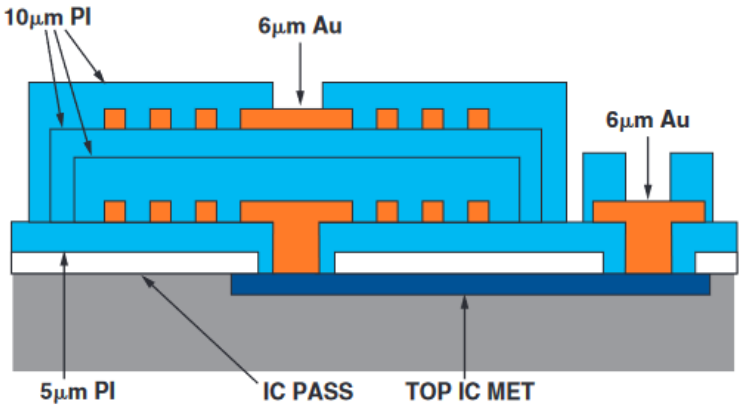


Figure 3.1: cross-section of iCoupler on-chip transformer, with top and bottom metal coils in orange and polyimide dielectric in light blue [17]

3.2 High-Level Design

At a high level, the proposed iCoupler relay will operate similarly to other solid-state relays. As shown in Figure 3.2, by applying an input voltage and current, a transistor switch is controlled at the output. However, while photoMOS solid-state relays rely on an optical solution for galvanic isolation, the proposed relay will use an iCoupler transformer for a magnetic isolation solution. Transformers can only couple ac signals, but both the input voltage and the output voltage for closing the load switch will be dc signals. Therefore, two additional stages are required: an oscillator to convert from dc to ac, and a rectifier to convert the ac voltage back to dc. An external current-limiting resistor R_{lim} is used to adjust the input current for the relay.

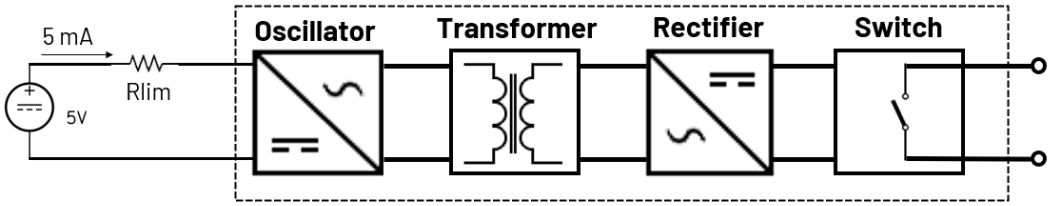


Figure 3.2: high-level iCoupler relay with four stages

3.3 Target Specifications

The target specifications for the iCoupler relay are the following:

1. Rated for operation with a 5V/5mA input.
    - This is to match other solid-state relays, which are designed for similar input voltages and currents. As shown in Figure 3.2, we can use an input resistor external to the IC to limit the current to 5 mA.
2. Efficiency of at least 20%.
    - This is to match the efficiency of other iCoupler products from Analog Devices. This efficiency is for the relay IC itself, so it does not include the losses through the current-limiting resistor.
3. On-resistance less than 150 mΩ.
    - This is to target the low on-resistance the ATE customer desires. It is comparable to the on-resistance of typical reed relays.
4. Turn-on and turn-off times less than 100 μs.
    - This is to target the fast switching speeds typical of other solid-state relays.
5. Bandwidth of at least 1 GHz.
    - This is to target a high bandwidth comparable to electromechanical reed relays.
6. Working isolation voltage of 400 Vrms and surge withstand voltage of 16 kV (input to output).
    - This is to meet the isolation requirements of ATE and other high-voltage applications.

7. Lifetime of at least 1 billion cycles.

    - This is to meet the long lifetime the ATE customer desires.

In this thesis, we will focus on designing a relay that meets specifications 1 through 5. Validating specifications 6 and 7 will require either further simulation testing or bench testing with the actual chip once it has been fabricated. One complication of the proposed iCoupler relay is the risk of ac cross-coupling, which is not present with optical solid-state relays. The concern is that the ac excitation signals of the transformer might couple and interfere with load signal being switched. This will also need to be tested with future simulation and bench testing.

Chapter 4

Background on Oscillators

4.1 RLC Circuit

To better understand the physics behind the iCoupler transformer, we can start by analyzing a simple model of a transformer coil. This model includes not only an inductor, but two main parasitics as well: a parallel capacitance and series resistance.

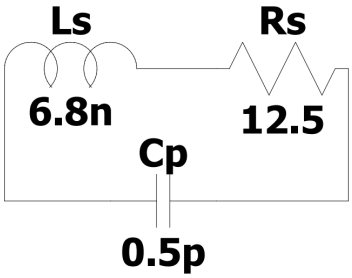


Figure 4.1: LTspice transformer coil model with parallel capacitance and series resistance

Because of these parasitics, the transformer coil is a resonant RLC circuit. The resonant frequency is the frequency at which $|Z_{L_s}| = |Z_{Cp}|$, which is $\omega_0 = \frac{1}{\sqrt{L_s C_p}}$. At resonance, the impedance of the coil RLC network will reach its maximum and look purely resistive. Above the resonant frequency, the parasitic capacitor decreases the impedance.

Another important measure is the quality factor Q, which is defined as [18]:

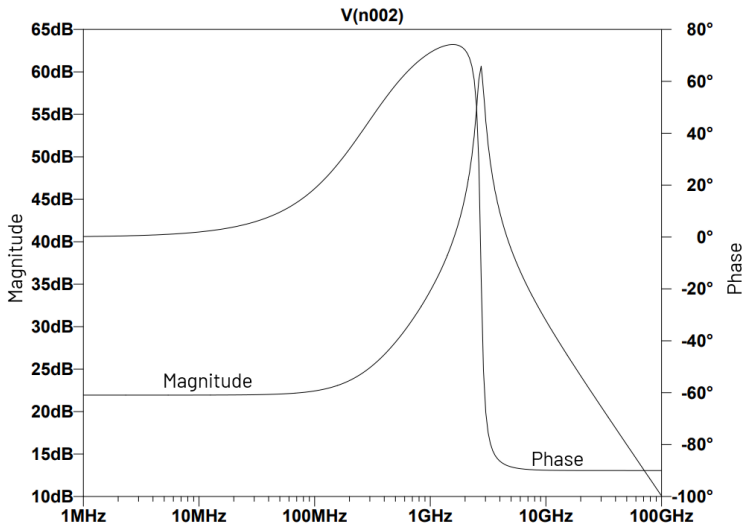


Figure 4.2: Bode plot of impedance of coil model from Figure 4.1, with resonant frequency near 2.7 GHz

$$Q = 2\pi \frac{\text{peak energy stored}}{\text{energy dissipated per cycle}}$$

Note that the same current passes through the inductor and the series resistor. Assuming this current is sinusoidal with amplitude I_{pk}, we can calculate the peak energy stored in the inductor and the energy dissipated in the resistor per cycle:

$$E_{L,pk} = \frac{1}{2} L_s I_{pk}^2$$

$$E_R = \frac{1}{2} I_{pk}^2 R_s T = \frac{\pi I_{pk}^2 R_s}{\omega}$$

So we have that

$$Q = 2\pi \frac{E_{L,pk}}{E_R} = \frac{\omega L_s}{R_s}$$

And at resonance,

$$Q_0 = \frac{\omega_0 L_s}{R_s} = \frac{\sqrt{L_s / C_p}}{R_s}$$

Maximizing Q_0 is important for maximizing the efficiency of the iCoupler transformer.

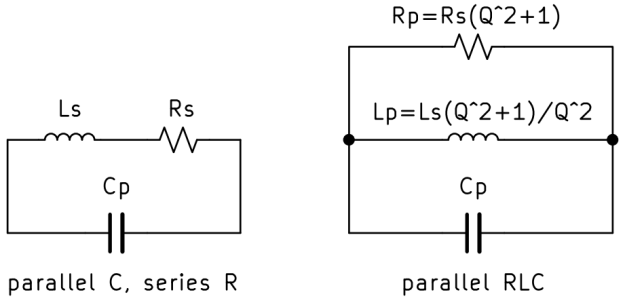


Figure 4.3: these circuits have equivalent impedance at resonance

To calculate the impedance of the coil RLC network at resonance, we need to first convert our circuit into a fully parallel RLC network. This can be done by applying the transformation indicated in Figure 4.3, which holds for frequencies close to resonance [19]:

$$R_p = R_s(Q^2 + 1)$$

$$L_p = L_s\left(\frac{Q^2+1}{Q^2}\right)$$

And if $Q^2 \gg 1$ we can make the approximation that $L_p \approx L_s$ and $R_p \approx Q^2 R_s$. Additionally, using the earlier derivation for Q_0, we have that

$$R_p \approx \left(\frac{\sqrt{L_s/C_p}}{R_s}\right)^2 R_s = \frac{L_s}{C_p R_s}$$

At resonance, the coil will have an impedance of R_p, since the reactances of the capacitor and inductor will cancel.

Note that, by itself, this RLC circuit will not oscillate indefinitely if a dc voltage is applied, since there will be losses through R_p. However, the larger R_p is (and therefore the smaller R_s is), the smaller those losses will be, and the closer the system will be to instability.

4.2 Cross-Coupled Pair (XCP) Oscillator

In order to get the coil RLC network to oscillate, we need to somehow cancel the parallel resistance R_p. This can be done by connecting a MOSFET cross-coupled pair (XCP), where the drain of one MOSFET is tied to the gate of the other. In the small-signal model, the XCP has a negative impedance of $Z_{XCP} = -\frac{2}{g_m}$, where g_m is the transconductance of each MOSFET [20]. This negative impedance can be used to cancel out the parasitic resistance of the coil and make an oscillatory system. All that is needed now is a current or voltage source to power the system, which can be connected to the center-tap of the coil, as shown in Figure 4.4. We can then replace the XCP with its small-signal negative impedance and replace R_s with the equivalent R_p to reduce the entire circuit into a parallel RLC network, as shown in Figure 4.5.

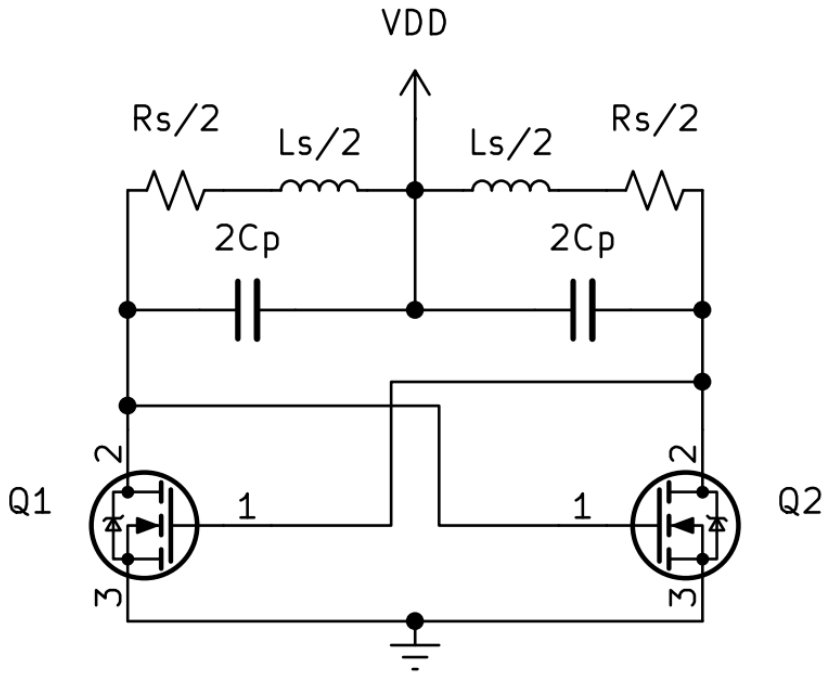


Figure 4.4: transformer coil from Figure 4.1 connected to XCP and center-tap voltage source

We will have undamped oscillations if the admittance of the parallel RLC network is negative. We can now solve for the g_m needed for oscillations:

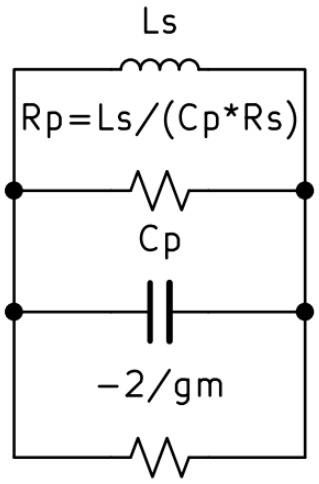


Figure 4.5: small-signal RLC simplification of Figure 4.4

$$Y_{R_p} + Y_{XCP} < 0$$

$$\frac{1}{R_p} - \frac{g_m}{2} < 0$$

$$\frac{g_m R_p}{2} > 1$$

$$g_m > \frac{2C_p R_s}{L_s}$$

For margin, we want the g_m of the transistors to be about 10 times greater than this minimum amount. The higher g_m is, the easier it will be for the system to start oscillating. In addition, smaller R_s reduces the minimum g_m needed, making it easier for oscillations to occur.

This g_m equation was verified by simulating the circuit in Figure 4.4 in LTspice, as shown in Figure 4.6. In the simulation, a 5 mA current source was connected to the transformer coil's center-tap. Since the circuit is symmetric, transistors M1 and M2 each have an average I_{DS} of 2.5 mA. The other transistor parameters are $k = 156\mu A/V^2$, $W = 20\mu$m and $L = 0.5\mu$m, so the g_m of each transistor is

$$g_m = \sqrt{2 I_{DS} k \frac{W}{L}} = \sqrt{2 \cdot 2.5\text{mA} \cdot 156\mu\text{A/V}^2 \cdot \frac{20\mu\text{m}}{0.5\mu\text{m}}} = 5.59\text{mA/V}$$

And then rearranging the minimum g_m formula to solve for R_s, we can expect oscillations to stop when

$$R_s > \frac{g_m L_s}{2C_p} = \frac{(5.59\text{mA/V})(6.8\text{nH})}{2 \cdot 0.5\text{pF}} = 38\Omega$$

In simulation, the oscillations stop at around $R_s = 34\Omega$. In addition, the oscillation frequency is 2.62 GHz, close to the expected resonance frequency of $\frac{1}{2\pi\sqrt{L_s C_p}} = 2.73$ GHz. The oscillation frequency is near the resonance frequency since frequencies far from resonance simply get shunted through the coil RLC tank; the inductor looks like a short at low frequencies, and the capacitor looks like a short at high frequencies.

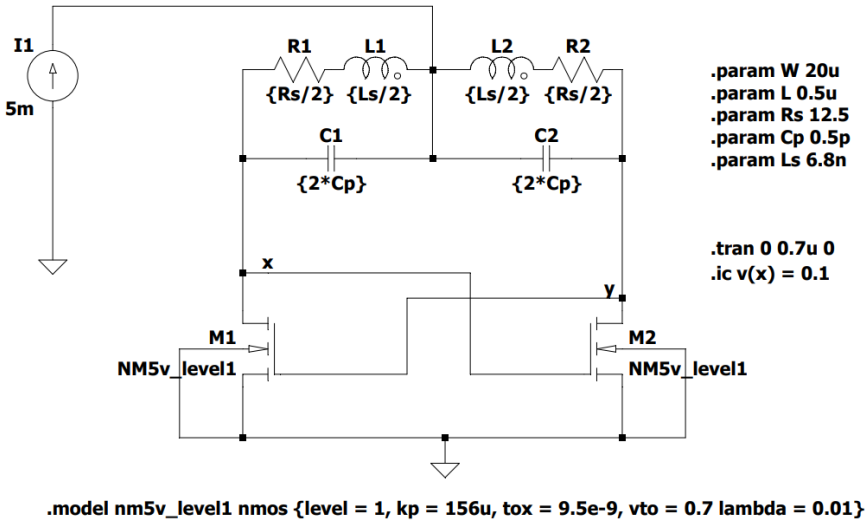


Figure 4.6: LTspice simulation of transformer coil, center-tap current source, and XCP oscillator

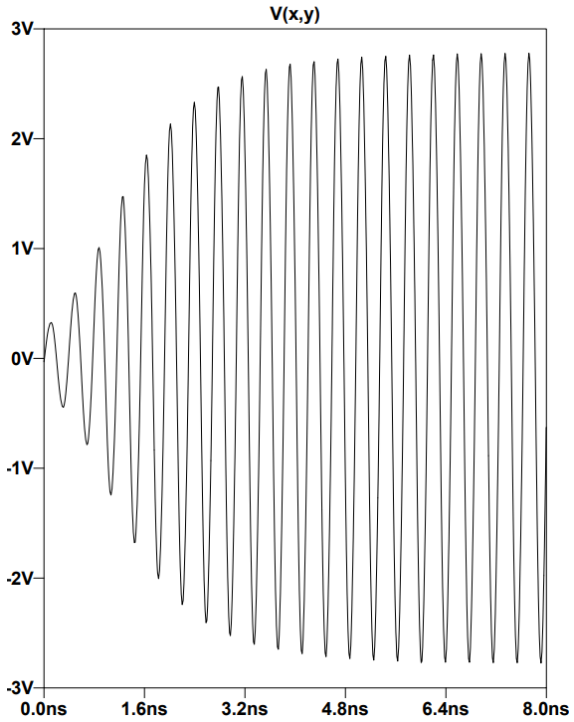


Figure 4.7: voltage oscillation across the transformer coil

Chapter 5

Relay Architecture

5.1 Oscillator

The oscillator stage converts the input dc voltage into an ac signal for the transformer. As shown in Section 4.2, a MOSFET XCP can convert a dc source into an ac excitation.

Initially, we considered using a NMOS/PMOS dual oscillator, as shown in Figure 5.1 (A). By using two oscillators in parallel, this design will provide a high effective g_m, providing faster startup and higher efficiency. However, this design leaves the center-tap of the transformer's primary coil floating, which will lead to poor radiated emissions results. Radiated emissions are a type of mid- to high-frequency electromagnetic interference, and standards such as CISPR 32 limit the amount of emissions allowed at certain frequencies [21]. In the case of this dual oscillator design, the floating center-tap will be oscillating at the transformer's oscillation frequency of around 100-1000 MHz, which is in the range tested by radiated emissions standards.

In order to keep radiated emissions low, the center-tap should be connected to some stable voltage, either ground or VDD (the input voltage). If the center-tap is grounded, then a PMOS XCP is used; if the center-tap is connected to VDD, then an NMOS XCP is used. As Figure 5.2 shows, for the same device size, NMOS transistors have about 50%

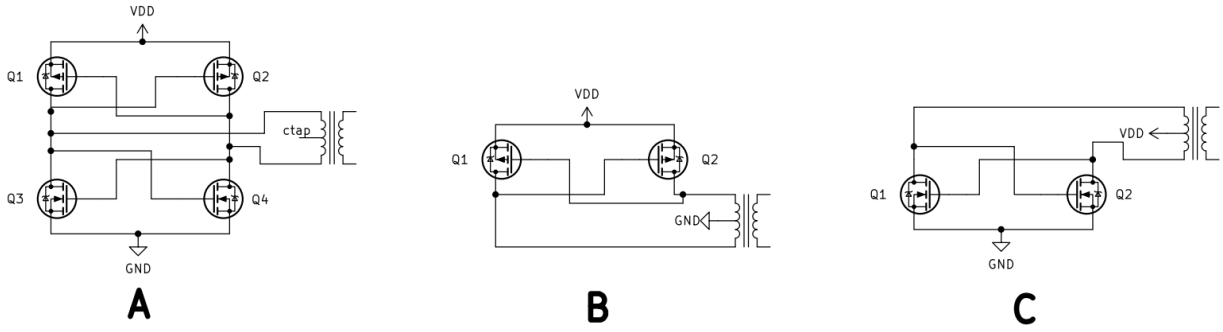


Figure 5.1: (A) NMOS/PMOS dual oscillator, (B) PMOS oscillator, (C) NMOS oscillator

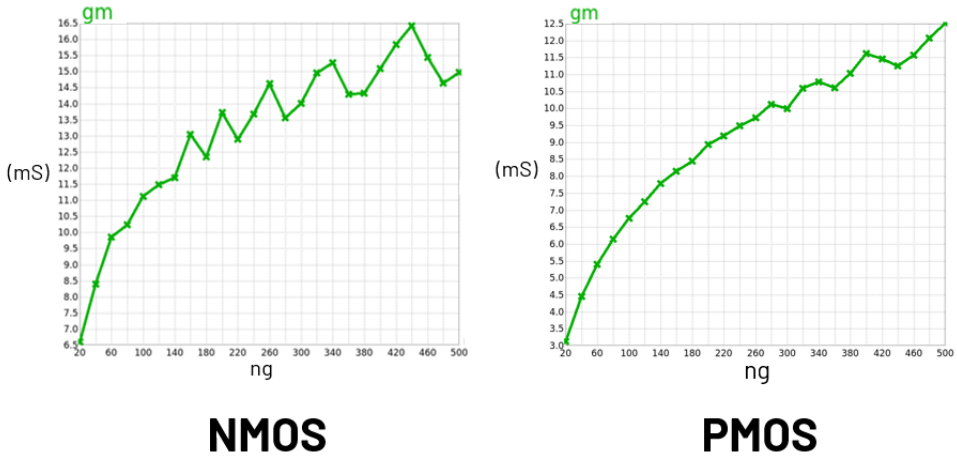


Figure 5.2: g_m of NMOS and PMOS transistors vs. ng (number of gates)

higher g_m than PMOS transistors. Therefore, the NMOS XCP will give the best startup performance, so we chose an NMOS XCP for the oscillator design.

5.2 Transformer

The design of the iCoupler transformer involves two planar coils, stacked vertically with a 20 μm polyimide insulation barrier in between. There are several design parameters to consider in the design of both the top and bottom coil, including:

- Number of sides/shape of coil (square, hexagonal, circular, etc.)
- Inner radius

- Outer radius
- Track width
- Track spacing
- Number of turns

For simplicity, when designing this transformer we constrained the top and bottom coils to both be circular coils with identical inner radius, outer radius, and number of turns. The only difference between the top and bottom coils is that the top coil will have a slightly larger track spacing (and therefore a slightly smaller track width) due to manufacturing process constraints.

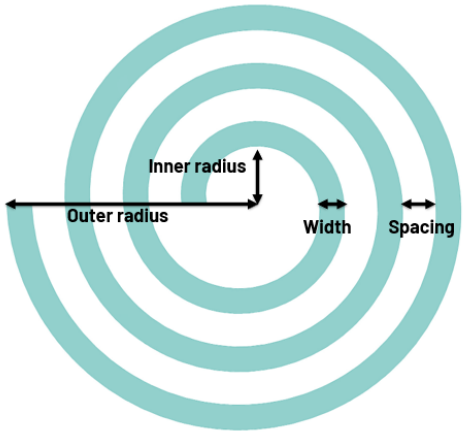


Figure 5.3: 3-turn circular coil with track width, track spacing, inner and outer radius labeled

We used a program called ASITIC (Analysis and Simulation of Inductors and Transformers for Integrated Circuits) to evaluate different transformer designs. Given a transformer design and an operation frequency, ASITIC can calculate the coupling coefficient, the coil quality factor, the coil inductance, and other key performance parameters of the transformer. In order to automate this process and test hundreds of different transformer designs at once, we wrote a Python script to sweep through different parameters, generate the transformer design files, and automatically run ASITIC on each design file. Then, we extracted the trans-

former parameters from the ASITIC log file and organized them into a CSV to be plotted. The details of the first sweep are shown in Figure 5.4.

Sweep 1 Parameters

Parameter	Value
Number of Turns	1-8
Inner Radius (um)	75, 125, 175, 225, 275
Outer Radius (um)	< 400
Top Track Width (um)	10, 20, 30, 40, 50, 60
Bottom Track Width (um)	Top track width + 2 um
Top Track Spacing (um)	4
Bottom Track Spacing (um)	2
Simulation Frequency	100 kHz

Best Transformer from Sweep 1

Parameter	Value
Number of Turns	8
Inner Radius (um)	125
Outer Radius (um)	397
Top Track Width (um)	30
Coupling Coefficient *k*	0.813
Top Coil Quality Factor *Q*	6.77
Top Coil Inductance (nH)	31.1
Top Coil Series Resistance (Ω)	2.79
Max Efficiency	69.7%

Figure 5.4: parameters of first sweep and the best transformer from the first sweep

After performing this sweep, the next step was to identify the best-performing transformers. The objective is to maximize efficiency, which is also highly correlated with maximizing coupling coefficient k and the quality factor Q of each coil. In fact, a transformer's maximum achievable efficiency can be calculated from k and Q using the equation below, assuming that the top and bottom coils have the same quality factor Q [22]:

$$\eta_{max} = \frac{k^2 Q^2}{(1 + kQ)^2}$$

In reality, the bottom coil will have lower Q due to increased substrate capacitance and substrate losses [17], and so our calculated efficiency values are a slight overestimate.

As shown in Figure 5.5 (A), increasing the outer radius generally leads to a higher efficiency transformer. However, the outer radius cannot be larger than 400 μm due to die size constraints. Figure 5.4 and 5.5 (B) show the best-performing transformer that met the 400 μm outer radius constraint. This transformer achieves a high coupling coefficient of around 0.8 and a maximum efficiency of around 70%. Since this best-performing transformer had the highest turn count tested in the sweep (8), maximizing number of turns even further could potentially lead to increased performance.

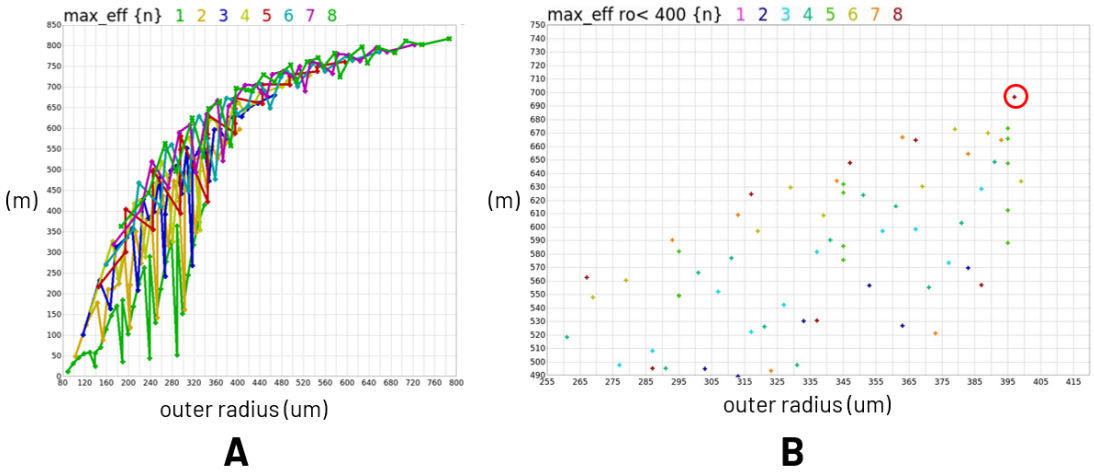


Figure 5.5: (A) max efficiency of all transformers vs. outer radius, (B) max efficiency of transformers with outer radius under 400 μm, with best transformer circled in red

Therefore, in order to find a better transformer, we performed a second sweep, this time testing designs with a fixed outer radius of 400 μm and up to 11 turns. In this sweep, the new constraint is that the inner radius must be at least 50 μm, since a minimum area is needed at the center of each coil to attach the bond wire.

Sweep 2 Parameters

Parameter	Value
Number of Turns	1-11
Inner Radius (um)	> 50
Outer Radius (um)	400
Top Track Width (um)	10, 20, 30, 40, 50, 60
Bottom Track Width (um)	Top track width + 2 um
Top Track Spacing (um)	4
Bottom Track Spacing (um)	2
Simulation Frequency	100 kHz

Best Transformer from Sweep 2

Parameter	Value
Number of Turns	11
Inner Radius (um)	136
Outer Radius (um)	400
Top Track Width (um)	20
Coupling Coefficient *k*	0.832
Top Coil Quality Factor *Q*	6.89
Top Coil Inductance (nH)	62.5
Top Coil Series Resistance (Ω)	5.63
Max Efficiency	70.7%

Figure 5.6: parameters of second sweep and the best transformer from the second sweep

Figure 5.6 shows the performance of the best transformer from this second sweep. Compared to the best transformer from the first sweep, this second transformer has more turns (11 vs. 8) and twice the coil inductance, but it also has twice the coil series resistance. As a result, this second transformer has only marginally better quality factor, coupling coefficient, and maximum efficiency compared to the first transformer. To understand why this is the

case, recall from Section 4.1 that the quality factor of a non-ideal transformer coil is

$$Q = \frac{\omega L_s}{R_s}$$

Where ω is the oscillation frequency, L_s is the inductance and R_s is the coil's series resistance. Increasing turn count does increase L_s, but it also increases R_s due to longer coil length. As turn count increases further, the track width must be reduced in order to fit all of the turns within the 400 μm outer radius constraint, further increasing coil resistance.

Figure 5.7, which plots the performance of all of the transformers from this second sweep, further illustrates this turn count vs. efficiency tradeoff. For each track width tested, increasing number of turns does increase maximum efficiency initially, but at some point there are diminishing returns. Eventually, efficiency can actually decrease.

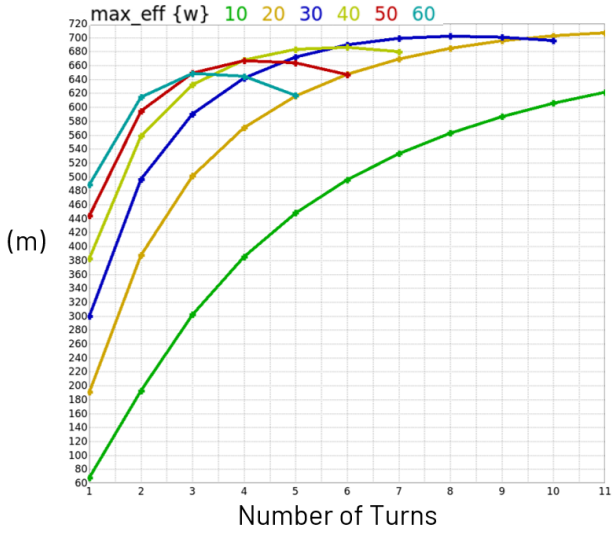


Figure 5.7: transformer efficiency vs. turn count for various track widths (μm)

Because increasing turn count provides limited improvement in performance, we chose to remain with the best transformer from the first sweep. We then used the parameters of this transformer to construct a model using Cadence EMX Planar 3D Solver. From the EMX model, we created a simplified circuit representation of the transformer in Cadence Virtuoso, which can then be connected with the other relay stages to create a full circuit simulation.

5.3 Rectifier

The rectifier converts the ac signal from the secondary side of the transformer into a dc voltage of around 1.8V to turn on the output load switch. The simplest solution is to use two Schottky diodes in a full-wave rectifier configuration, as shown in Figure 5.8 (A). However, Schottky diodes are not available in the transistor process that will be used for this relay, so a different solution is needed.

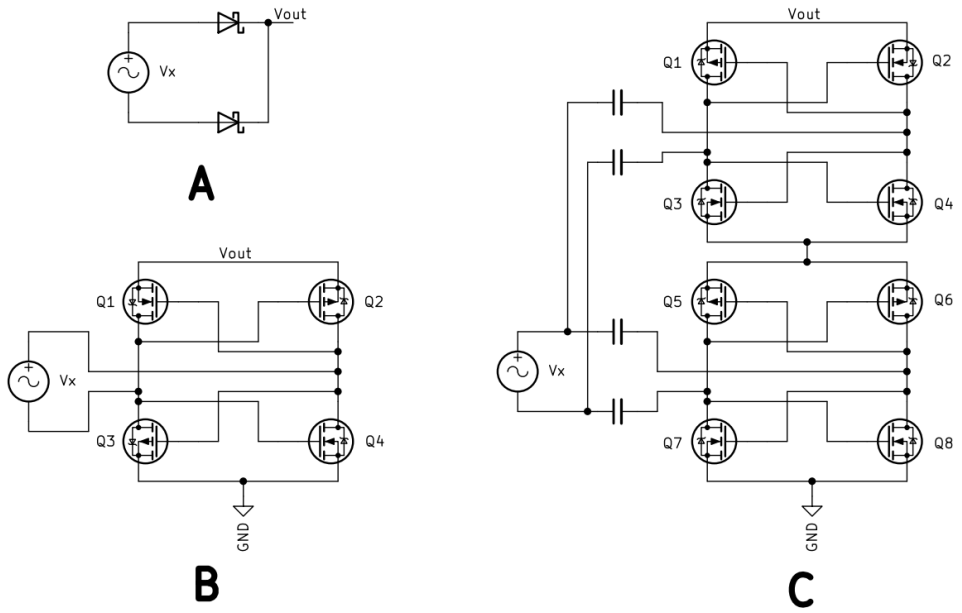


Figure 5.8: (A) Schottky full-wave rectifier, (B) cross-coupled rectifier, (C) stacked cross-coupled rectifier

One potential solution is a cross-coupled rectifier, as shown in Figure 5.8 (B). This rectifier uses two PMOS and two NMOS devices, and functions similarly to a full-bridge diode rectifier. When the voltage across the secondary-side coil V_x is positive, Q2 and Q3 are conducting the output current; when V_x is negative, Q1 and Q4 are conducting the output current. Regardless of the sign of V_x, V_{out} is always positive.

However, in testing with the oscillator and the transformer, this rectifier design was not able to reach the 1.8V desired to turn on the output switch, only reaching about 1.2 V. In order to increase the output voltage, we can stack two cross-coupled rectifiers, as shown in

Figure 5.8 (C). AC coupling capacitors are added as the top and bottom rectifiers can be at different dc voltages. With this design, we are able to achieve 1.8V output.

5.4 Output Switch

The output switch is turned on by the 1.8V rectifier output and conducts the load signal. There are two important specifications for the output switch:

- **standoff voltage:** This is how much voltage the output switch can block when it is off. This should be as high as reasonably possible.
- **on-resistance:** While the overall target on-resistance for this relay is 150 mΩ (specification 3 from Section 3.3), we want to design the output switch for a max on-resistance of 100 mΩ, since there will be additional resistance in the bond wires of the device.

There are several possible NMOS transistor choices for the output switch, each with a different standoff voltage, on-resistance, and size. Transistors with higher standoff voltage require a larger device size for the same on-resistance. In order to strike a good compromise between high standoff voltage and small device size, we chose a 65V transistor.

The output switch should also be able to conduct ac and dc current. We can achieve this by placing two transistors in series with their source connected, as shown in Figure 5.9.

In addition to the NMOS transistors, which are mainly a capacitive load, the output stage includes a parallel resistor load, in order to simulate secondary-side control circuitry that may be added to the design later and will consume steady-state dc current. Initially, we set this R_{load} to 1.8kΩ, for 1 mA of dc current draw at 1.8V; however, this is a conservative estimate since the control circuitry will likely not consume more than 100μA. In Section 6.5, we will adjust R_{load} to optimize the output voltage and efficiency of the design.

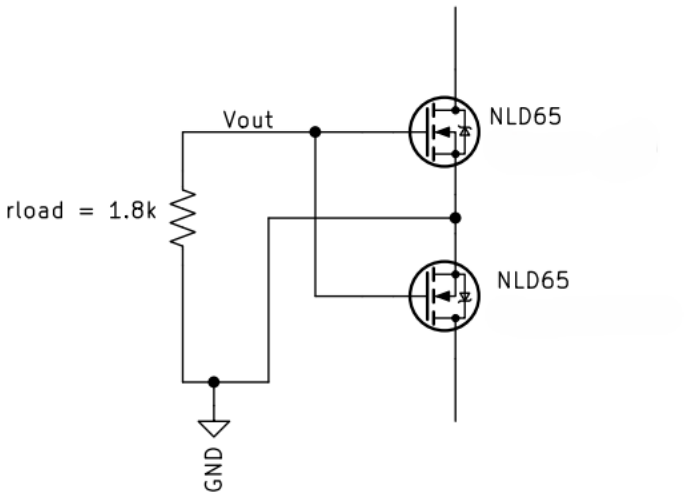


Figure 5.9: output switch, with source-connected transistors and resistor load in parallel

5.5 Overall Design

Figure 5.10 shows the overall design of the iCoupler relay, grouped into the oscillator, transformer, rectifier, and output switch stages. The 5V input voltage and the current-limiting resistor are external to the relay IC. The next step is to optimize the relay design to achieve at least 20% efficiency and under 100 mΩ on-resistance using a 5V, 5 mA input (specifications 1, 2, and 3 from Section 3.3).

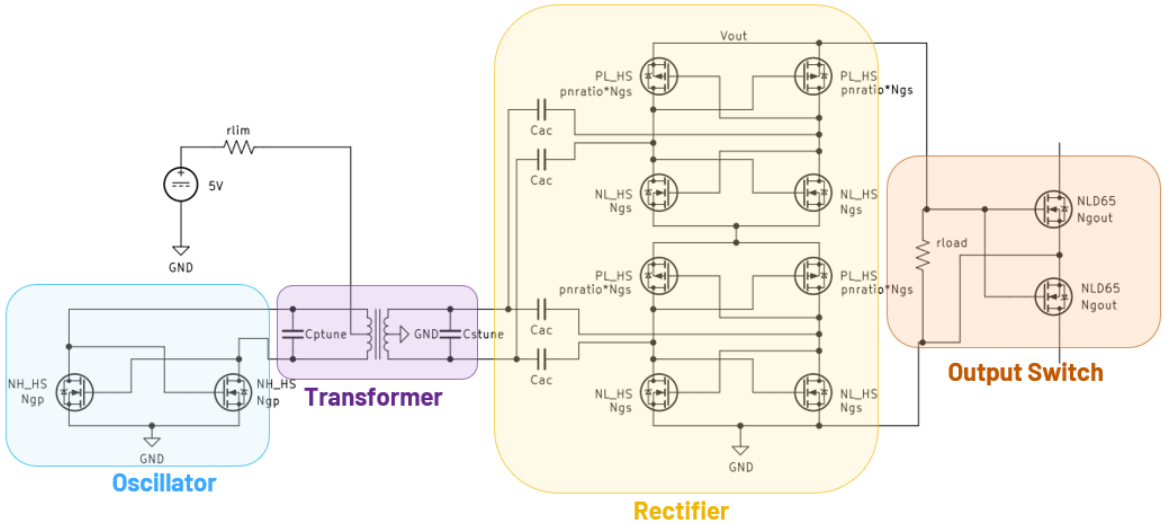


Figure 5.10: overall relay design

Parameter	Description
Rlim	Current-limiting resistor
Cptune	Primary-side tuning capacitor
Cstune	Secondary-side tuning capacitor
Cac	AC coupling capacitors
Ngp	Number of gates on primary-side transistors
Ngs	Number of gates on secondary-side NMOS transistors
pnratio	Gate count ratio between secondary-side PMOS and NMOS transistors
Ngout	Number of gates on the output switch
Rload	Parallel load resistor

Figure 5.11: relay design parameters

Transistors	W/L
NH_HS	10um/800nm
NL_HS	10um/180nm
PL_HS	10um/180nm
NLD65	100um/250nm

Figure 5.12: transistor types and sizes

Chapter 6

Design Optimization

6.1 Initial Trial-and-Error Solution

To begin the optimization process, we started with trial-and-error, testing out reasonable values for the circuit parameters from Figure 5.11 and manually adjusting each parameter in the direction that seemed to increase the output gate voltage and efficiency while keeping the input current under 5 mA. The initial circuit is shown in Figure 6.1. This circuit is similar to Figure 5.10, except it is designed with a PMOS oscillator instead of an NMOS oscillator; this will be changed later in the design process. The best solution found after a few rounds of trial-and-error testing is shown in Figure 6.2.

While this initial solution does limit the input to 5 mA, it has a slightly lower efficiency than desired (18% vs 20%), and most importantly, has an output gate voltage of only 1.22V instead of the desired 1.8V. At this lower gate voltage, the NLD65 output switch transistors will not turn on as strongly, so they will need to be larger to achieve the target 100 mΩ on-resistance. As shown in Figure 6.3, the switches will need to be about 15% larger to achieve the same on-resistance at 1.22V that they achieve at 1.8V. Additionally, this simulation is calculating the output voltage for ideal conditions; in reality, extra parasitic resistance or capacitance in the iCoupler transformer, the bond wires, and the transistors could drop

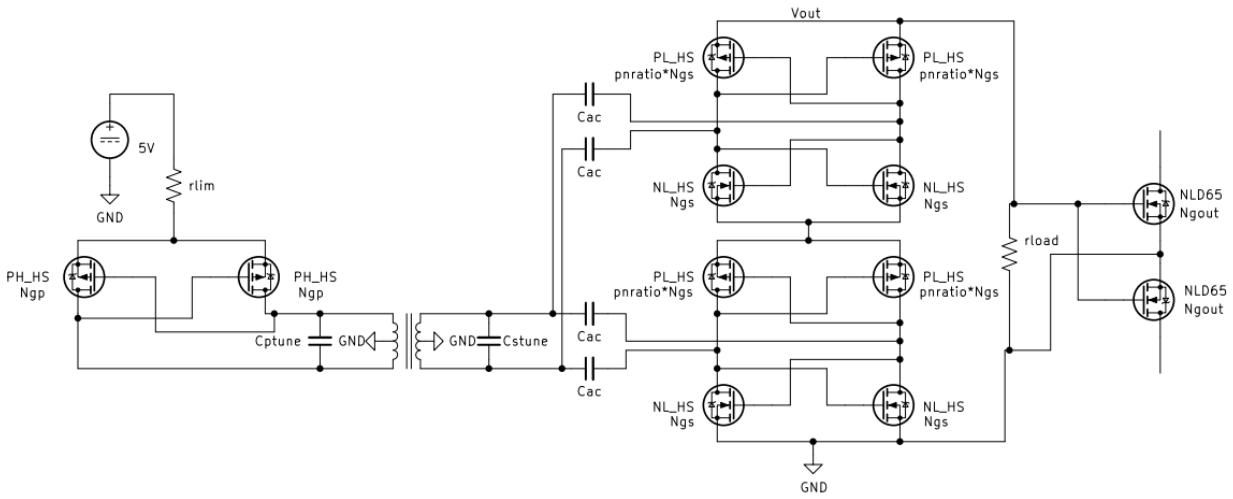


Figure 6.1: initial relay schematic with PMOS oscillator

Initial Relay Design

Parameters	Value
Rlim	815
Cptune	1f
Cstune	1f
Cac	50p
Ngp	400
Ngs	12
pnratio	3
Ngout	3050
Rload	1.8k

Initial Relay Performance

Performance Metric	Target	Actual
Output Voltage	1.8V	1.22V
Input Current	<5 mA	4.98mA
Efficiency	> 20%	18%
Frequency	--	395 MHz

Figure 6.2: initial relay design and performance

the output voltage further; as Figure 6.3 shows, once the gate voltage goes below 1.1V the transistor size required increases dramatically.

We decided that further trial-and-error testing would be infeasible for optimizing the solution, since the solution space is multi-dimensional and highly nonlinear.

6.2 Multi-Objective Genetic Algorithm

In order to quickly explore the entire solution space, we used a multi-objective genetic algorithm (MOGA) provided in the Analog Devices simulation toolkit. MOGAs are optimization algorithms used to solve problems where multiple, often conflicting objectives are desired; in our case, we have three objectives: maximize efficiency and output voltage and minimize

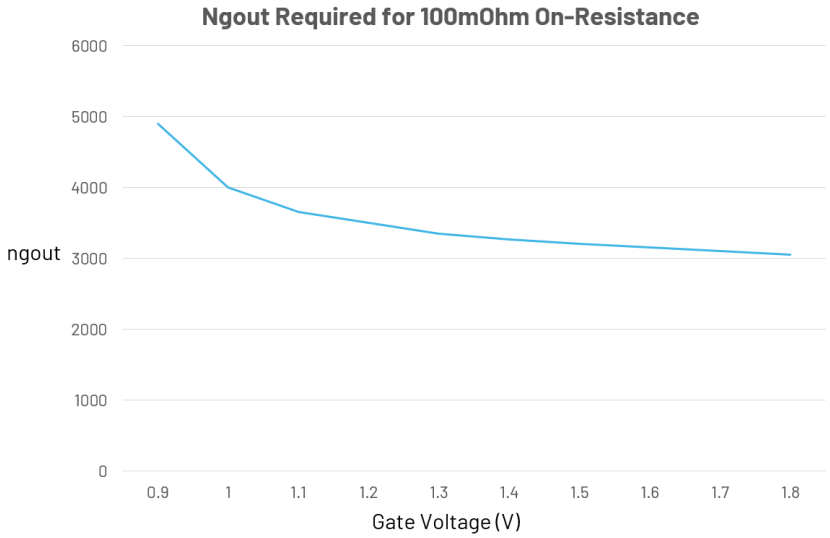


Figure 6.3: NLD65 required device size vs. gate voltage

input current. The MOGA runs in generations; each generation, the algorithm explores several possible solutions, and the "fittest" solutions are used to create the solutions in the next generation [23]. In this way, the optimization algorithm converges to finding one or more optimal solutions that meet the desired objectives [23].

We ran the optimizer for 25 generations, with the initial solution from Figure 6.2 used as the starting seed. Figure 6.4 shows what parameters we gave to the optimizer; for these parameters, we gave the optimizer a wide search range to ensure that it could explore as much of the solution space as possible. For the remaining parameters, we kept them fixed at their values from Figure 6.2.

Optimizer Parameters and Results

Parameters	Min	Max	Starting Seed	Best Solution
Rlim	100	1000	815	636
Ngs	4	32	12	6
Ngp	4	500	400	4
Cstune	1f	10p	1f	4.5f
Cptune	1f	10p	1f	2.2f
Cac	10p	100p	50p	69p

Starting Seed vs Optimizer Solution

Performance Metric	Starting Seed	Best Solution
Output Voltage	1.22V	1.80V
Input Current	4.98 mA	3.07 mA
Efficiency	18%	19.4%
Frequency	395 MHz	5.27 GHz

Figure 6.4: parameters of the optimizer run and the best solution found

While there is often no clear "best" solution in multi-objective algorithms, when we ran the optimizer there was one solution that met or came close to our efficiency, voltage,

and current targets. This solution is shown in Figure 6.4, and it appears to be a significant improvement over the initial trial-and-error solution. The new solution is able to reach 1.80V output voltage and 19.4% efficiency with only about 3 mA of input current. Interestingly, the new solution has an oscillation frequency of over an order of magnitude higher than before, at 5.27 GHz. The biggest difference between the two solutions is the transistor sizes; while the initial solution had very large transistors, especially on the primary-side oscillator, the new solution uses transistors with a single-digit number of gates. This is surprising since from the earlier trial-and-error testing, reducing the size of the transistors seemed to decrease the efficiency and output voltage; the optimizer has clearly found some previously unexplored part of the solution space.

6.3 Analysis and Rejection of High-Frequency Solution

Out of all the parameters, the size of the oscillator and rectifier transistors (ngp and ngs, respectively) seems to have the largest impact on circuit performance. Therefore, to better understand this relationship, we ran a sweep of ngp and ngs; we swept ngp from 6 to 160, and ngs from 6 to 30. The resulting efficiency, oscillation frequency, output voltage, and input current are plotted in Figure 6.5.

As ngp is increased, efficiency and output voltage peak at some point, before quickly falling and slowly rising back up again. Meanwhile, oscillation frequency steadily decreases as ngp is increased, before dropping suddenly around the point where efficiency and output voltage fall to their minimum. This suggests the circuit operates in one of two distinct modes, a high-frequency or a low-frequency mode, depending on the size of the oscillator and rectifier transistors. Performance is better for the high-frequency mode, where higher voltage and efficiency can be achieved with lower input current.

AC analysis of the circuit supports the sweep results. Figure 6.6 shows the Bode plots of the small-signal voltage across the primary-side coil at different values of ngp. When

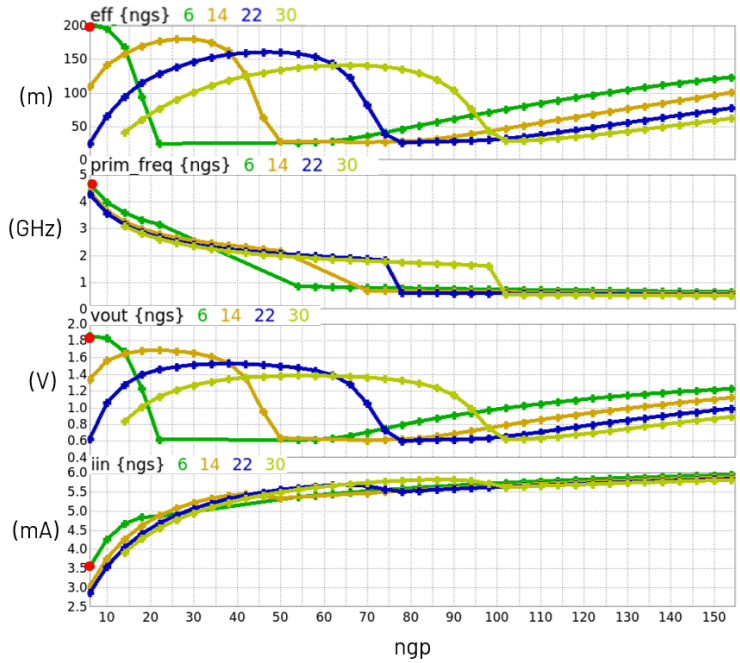


Figure 6.5: relay performance across ngp and ngs, with best solution from Figure 6.4 in red

ngp = 6, there are two peaks in the Bode plot, one at about 1.2 GHz and one at around 5 GHz, indicating that the transformer coil has two resonant frequencies. However, since the high-frequency peak is taller, the circuit ends up oscillating at the higher frequency of 5 GHz. As ngp increases both peaks move to lower frequencies, and the lower peak also begins to dominate. At around ngp = 48, both peaks are at about the same magnitude; in Figure 6.5, this corresponds to the region where the frequency is about to jump down and the efficiency and output voltage are at their minimum. Once ngp increases past 66, the low-frequency peak dominates and the circuit enters the low-frequency operation region.

The optimizer's solution is marked on Figure 6.5. This solution is in the high-frequency operation region, and it offers the maximum efficiency and output voltage at a very low input current. However, small changes to the optimizer's solution cause the performance to change quite dramatically; increasing ngs from 6 to 14 drops efficiency from 20% to 11% and output voltage from 1.8V to 1.4V. In contrast, in the low-frequency region performance is less sensitive to parameter variations, as indicated by the flatter and closer lines at high ngp.

Increasing ngp or ngs increases the transistor sizes, which in turn increases the capacitance

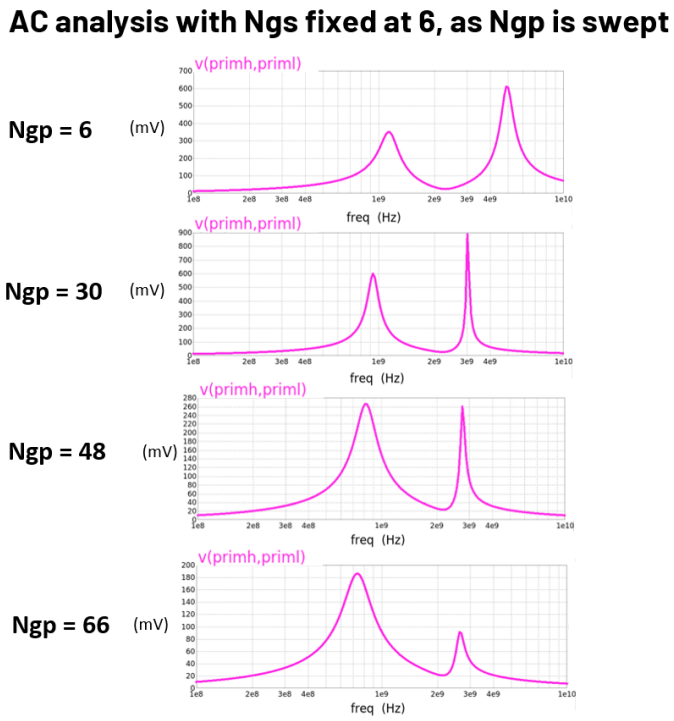


Figure 6.6: Bode plot of voltage across the primary transformer coil as ngp is varied

across the transformer coils. Therefore, the sensitivity of the optimizer's solution to ngp and ngs suggests that this solution may also be sensitive to parallel capacitance across the transformer. This is a cause for concern, since in the actual device there may be additional parasitic capacitances from the bond wires; it is important the relay's operation remains stable over small variations in capacitance.

To test how the relay responds to extra capacitance, we performed a capacitance sweep on both a high-frequency and a low-frequency circuit solution, shown in Figure 6.7. In the high-frequency case, adding just 1pF of capacitance across either the primary or secondary coil can cause efficiency and output voltage to lower drastically. When cstune is at 0 pF, adding even 250 fF to cptune causes the output voltage to fall to 0.8V and efficiency to fall to 4%. On the other hand, in the low-frequency solution the performance remains mostly unchanged even when adding 2-3 pF of extra capacitance. The flatter and closer lines indicate the improved stability over capacitance variations.

Therefore, while the high-frequency solution that the optimizer found appears to offer

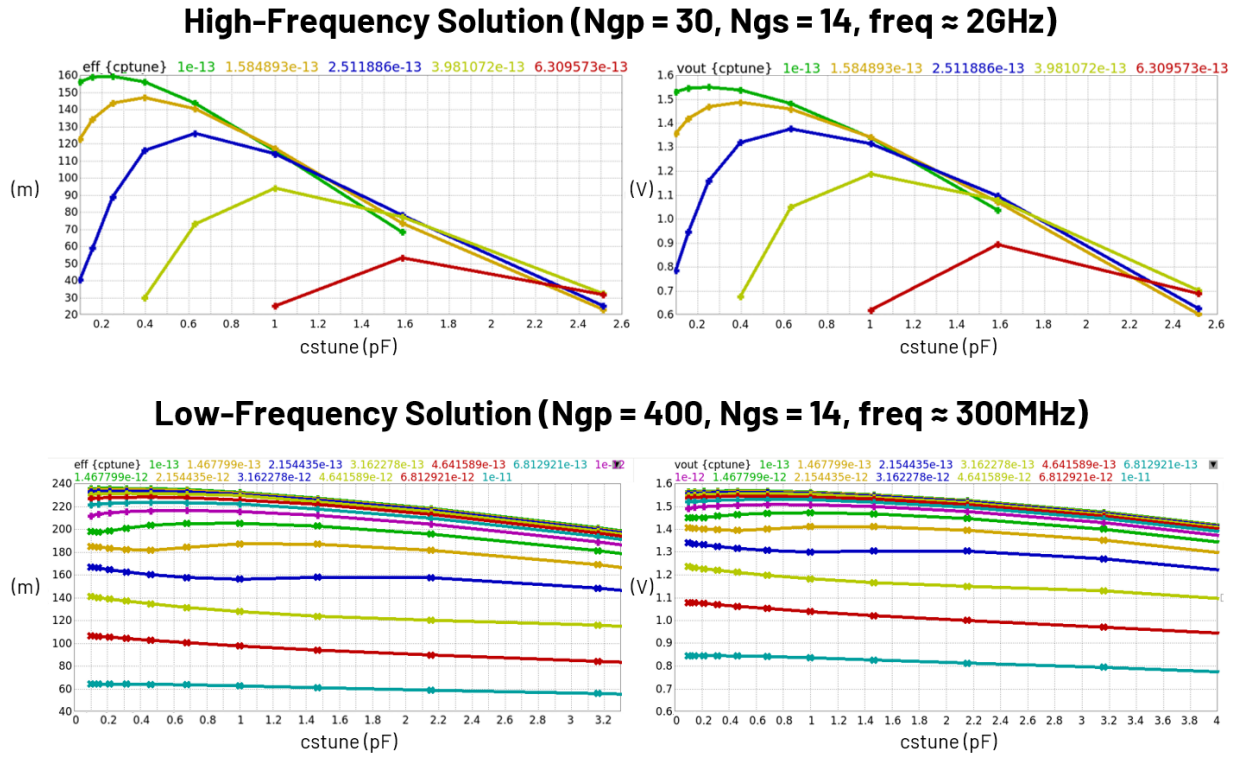


Figure 6.7: sweep of cptune and cstune on high and low frequency relay solutions

promising performance, that performance is very unstable and likely not replicable in an actual real-world device with parasitic capacitances. For the rest of the design, we shift the focus to optimizing the low-frequency solution, which will require using large transistors (typically ngp $>$ 100) on the oscillator.

6.4 Using NMOS Transistors for Oscillator Improvement

In the initial design from Section 6.1, we designed the primary-side oscillator using a cross-coupled PMOS oscillator. However, from the results in Section 5.1, an NMOS oscillator should yield better performance due to the higher g_m of NMOS transistors. Figure 6.8 compares the efficiency and output voltage of the relay circuit with a PMOS and an NMOS oscillator. The NMOS oscillator provides higher peak efficiency and higher output voltage, and does so at a smaller device size. While the circuit with a PMOS oscillator needs ngp = 300, ngs = 14 to reach its maximum output voltage of 1.6V, with an NMOS oscillator it can

achieve 1.64V output with ngp = 160, ngs = 6. Therefore, we switched the oscillator design to an NMOS cross-coupled oscillator.

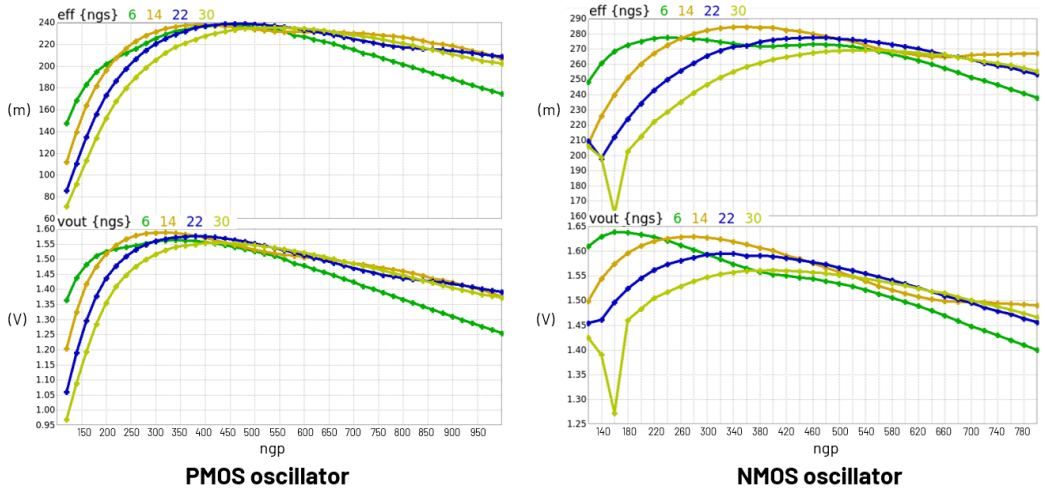


Figure 6.8: performance of relay with PMOS vs NMOS oscillator

However, the results shown in Figure 6.8 are with about 6.3 mA of input current. Once the input current is limited to 5 mA by increasing the input current-limiting resistor, the output voltage drops down to 1.32V, as shown in Figure 6.9.

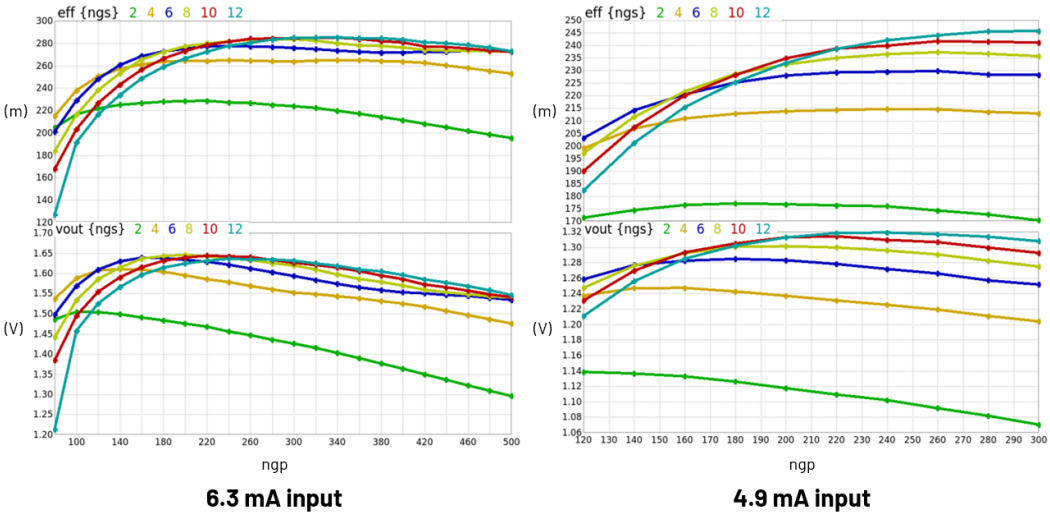


Figure 6.9: performance drop when limiting input current to 5 mA

6.5 Redesigning for Optimal Load

In order to increase the output voltage back up to 1.8V, we can adjust the rectifier's load resistance. In the initial solution, we conservatively set the load resistance to 1.8kΩ to simulate a 1 mA steady-state current draw from the secondary-side control circuitry; however, as mentioned in Section 5.4, the control circuitry will likely not consume more than 100 μA from the rectifier. Increasing the load resistance does help increase the output voltage, as shown as Figure 6.10. However, the efficiency is peaking at the load resistance of 1.8kΩ that we have currently designed for. The circuit needs to be re-optimized so that the peak efficiency is occurring where the output voltage reaches 1.8V, at around 3.5kΩ to 4.5kΩ of load resistance.

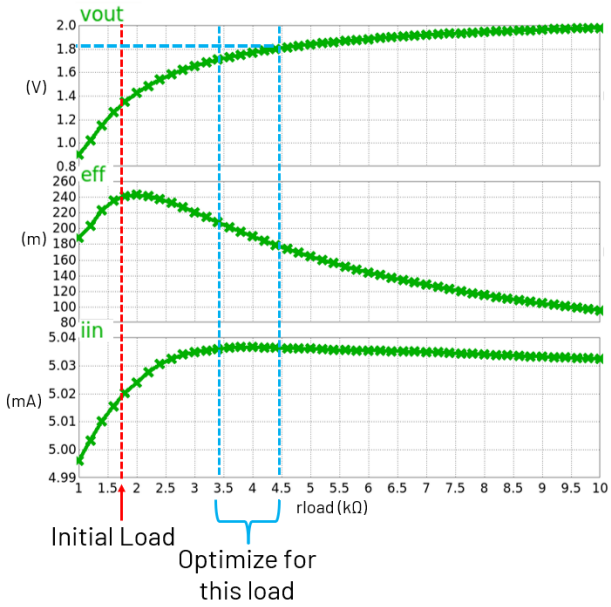


Figure 6.10: performance across rload

We therefore increased the load resistance to 3.6kΩ; now the dc current draw is 500 μA, still more than enough for the auxiliary control circuitry. With the lighter load, smaller transistor sizes are required for optimizing the output voltage. From Figure 6.11, we chose ngp = 120, ngs = 4 to get an output voltage close to 1.8V. Efficiency at this maximum output voltage point is slightly above 20%.

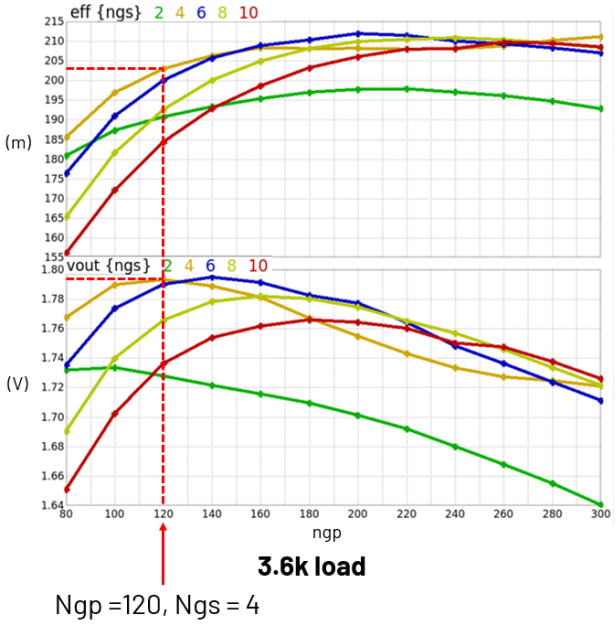


Figure 6.11: ngp and ngs sweep for relay with 3.6kΩ rectifier load

6.6 Optimizing Other Parameters

With ngp and ngs determined, we can now optimize the remaining parameters of the circuit. Compared to transistor size, however, these parameters have less effect on circuit performance.

Increasing Cac, the rectifier ac coupling capacitance, increases efficiency and output voltage but only up to a certain point. Therefore, we set Cac to 10 pF, since beyond that there is little performance benefit to justify the increased component size.

For pnratio, the ratio between the gate count of the PMOS and NMOS rectifier transistors, optimal results are seen with pnratio between 2 and 4. Therefore, we set pnratio to 3, meaning the PMOS transistors will be about 3 times larger than the NMOS transistors.

For cptune and cstune, the parallel tuning capacitance across each transformer coil, adding any extra capacitance only decreases performance. Therefore, we set cptune and cstune to 1 fF in simulation, effectively removing them from the circuit.

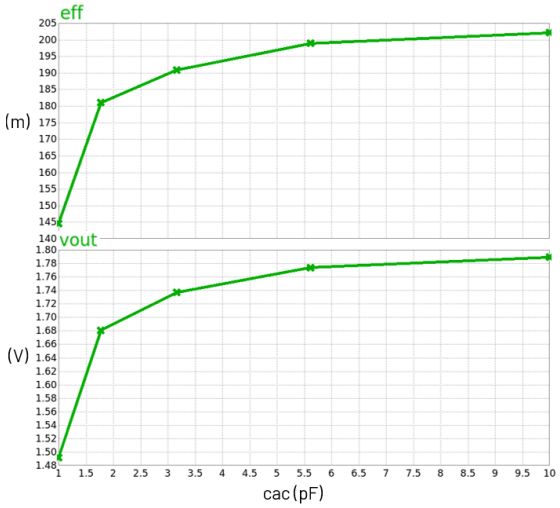


Figure 6.12: Cac sweep

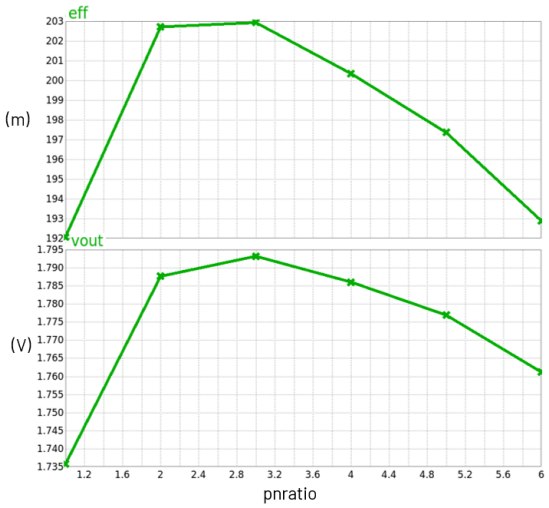


Figure 6.13: pnratio sweep

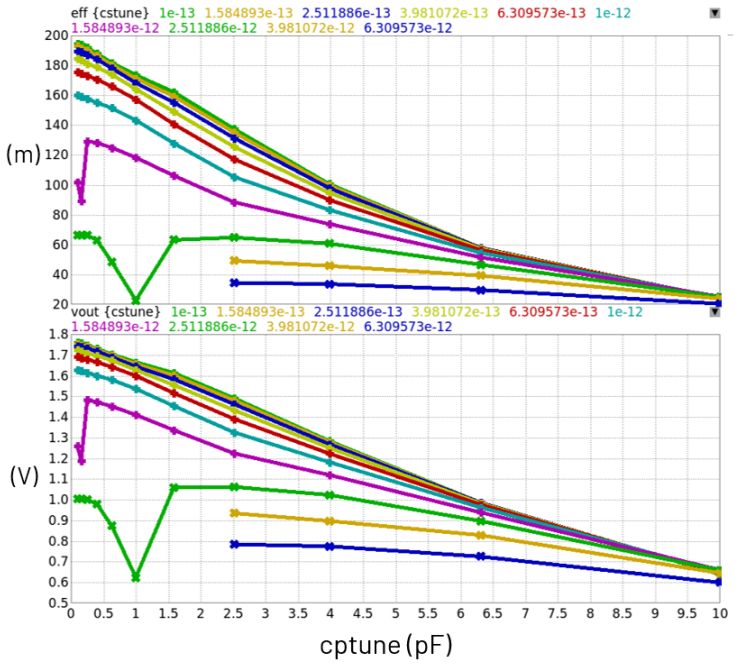
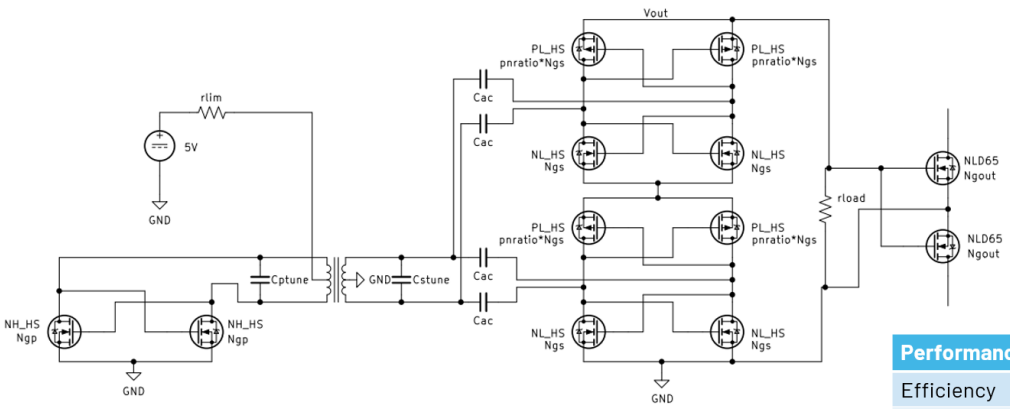


Figure 6.14: Cstune and Cptune sweep

6.7 Final Design

The resulting final design is able to achieve 20% internal efficiency and run on a 5 V, 5 mA input as desired. Based on the output voltage of 1.79V, we chose ngout = 3200 so that the output transistors would be able to reach 100 mΩ on-resistance within a reasonable amount of time when the relay is switched on. In the next section we will verify this on-resistance and turn-on time.



Parameters	Value
Rlim	820Ω
Ngs	4
Ngp	120
pnratio	3
Cstune	1fF
Cptune	1fF
Cac	10pF
rload	3.6kΩ
Ngout	3200

Performance Metric	Value
Efficiency	20.2%
Input Current	5.02 mA
Vout	1.79 V
Frequency	729 MHz

Figure 6.15: final relay design and performance

iCoupler Transformer Design

Parameter	Value
Number of Turns	8
Inner Radius (um)	125
Outer Radius (um)	397
Top Track Width (um)	30
Bottom Track Width (um)	32
Top Track Spacing (um)	4
Bottom Track Spacing (um)	2

Figure 6.16: final iCoupler transformer design (from Section 5.2)

Chapter 7

Performance Analysis

7.1 On-Resistance

To calculate the on-resistance of the simulated relay design, we connected an ideal 0.1V dc voltage source to the relay's output switch stage. Figure 7.1 shows a plot of switch voltage and conduction current as the switch turns on. The switch is able to reach a minimum on-resistance of 96 mΩ, and reaches 100 mΩ within 7.5 μs.

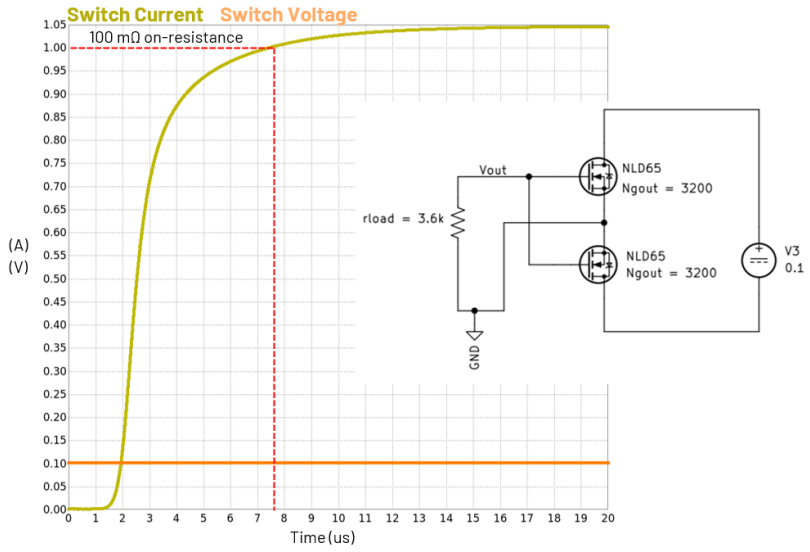


Figure 7.1: relay turn-on and on-resistance test

7.2 Bandwidth

To calculate the bandwidth, we used a similar circuit, instead this time we connected an ac voltage source and measured the magnitude of the switch impedance as we swept the source frequency, as shown in Figure 7.2. The 3 dB bandwidth of the switch is the frequency where the magnitude of the impedance falls to 70.7% of its dc value; from Figure 7.2, we can see that happens at around 4.8 GHz. This meets our bandwidth target of 1 GHz and is comparable to the bandwidth of the best reed relays. The bandwidth can be used to calculate the switch's output capacitance; modeling the switch as a parallel RC circuit, with R = 98 mΩ, the output capacitance is found to be:

$$\frac{1}{2\pi(98\text{m}\Omega)C} = 4.8 \text{ GHz}$$

$$C = 340 \text{ pF}$$

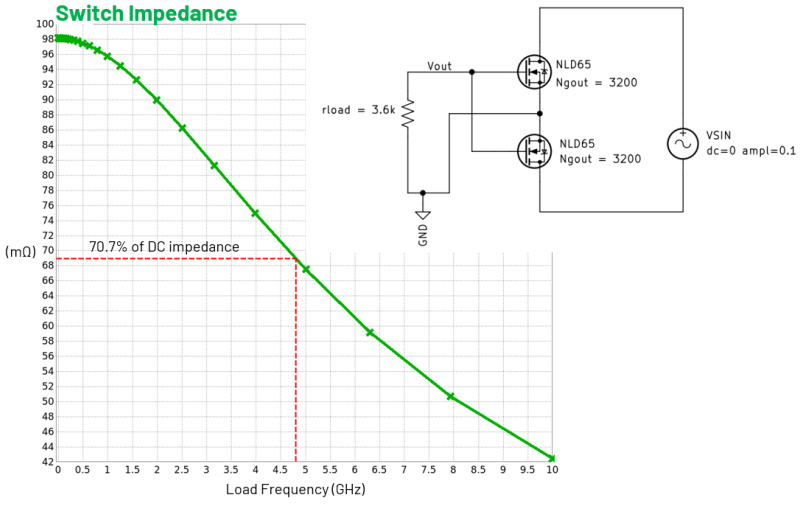


Figure 7.2: magnitude of relay output impedance vs. load frequency

This calculation is a simplification, since the switch's output capacitance will depend on the switch voltage. Further simulation testing or actual silicon testing will be needed to more accurately determine the output capacitance.

7.3 Switching Speed

The switch can reach 100 mΩ on-resistance within 7.5 μs; when turning off, the switch takes 21 μs to reach 100 kΩ. Both the turn-on and turn-off times are within the desired 100 μs targets. When turning the relay on and off very quickly, the relay remains stable, with the output gate voltage not rising above 1.85V or falling below 1.65 V.

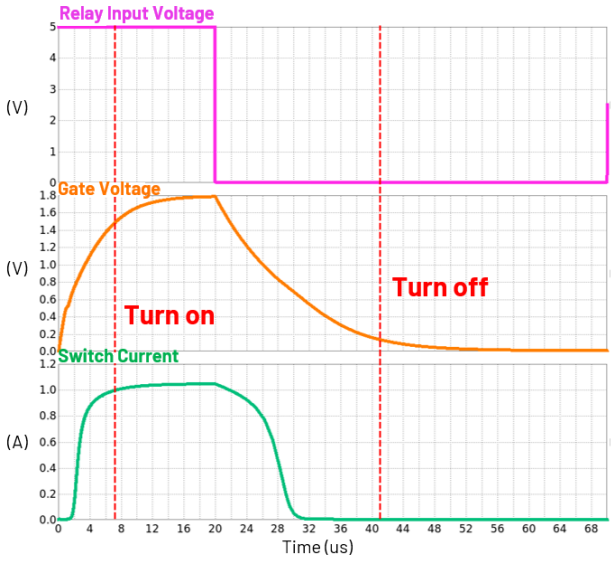


Figure 7.3: turn-on and turn-off of relay switch

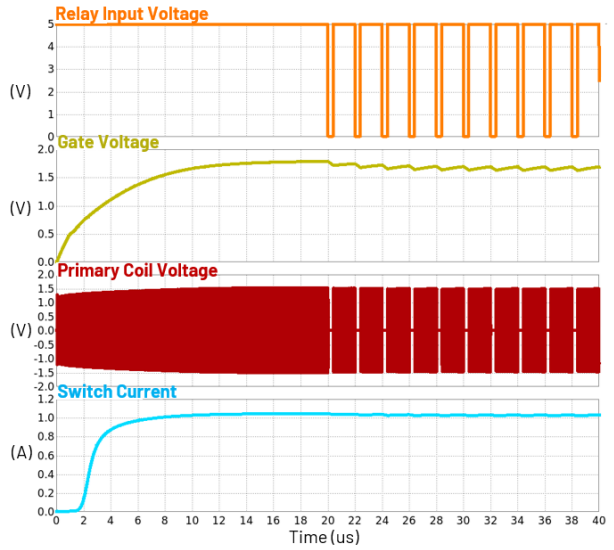


Figure 7.4: fast switching of the relay does not lead to instability

Chapter 8

Future Work

8.1 Improving Performance Using Closed-Loop Control

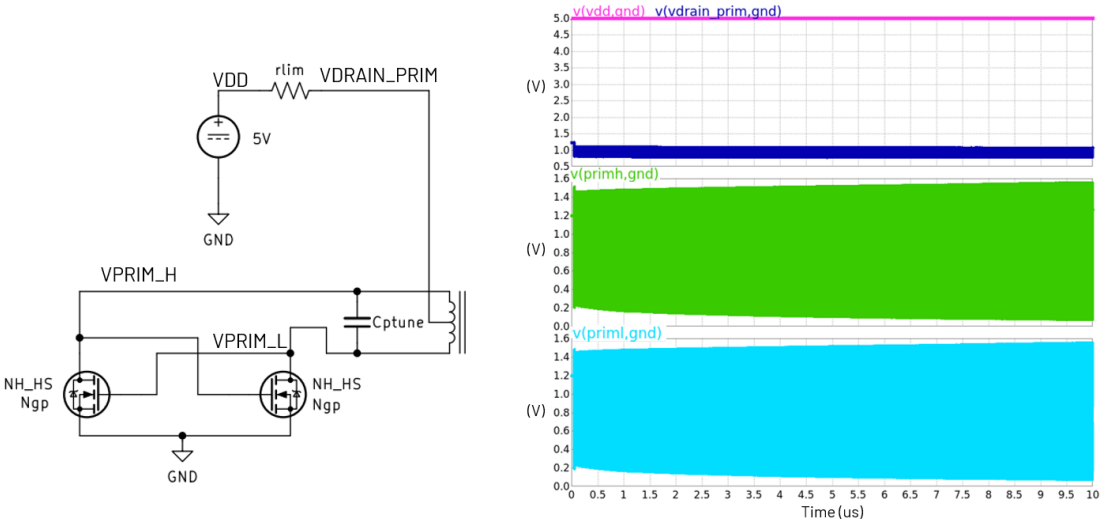


Figure 8.1: voltage waveforms on oscillator, with significant voltage drop across rlim

A significant weakness of the current design is the external current-limiting resistor. There is a large voltage drop across this resistor; as shown in Figure 8.1, even though VDD is set to 5V, VDRAIN_PRIM is only at around 1V. This limits the maximum amplitude that the primary-side oscillator can produce, which limits the available voltage for the rectifier on the secondary. A potential solution is to implement an active control scheme to regulate

the input current and output voltage, rather than using a passive component. The control circuitry would be able to turn off the oscillator (for example, by shorting the gates of the NMOS oscillator transistors to ground) when needed to keep the input current and output gate voltage at a desired setpoint.

8.2 Relay for High-Voltage Applications

The relay in this thesis was designed for a standoff voltage of 65V, which is suitable for most ATE. However, there are many other high-voltage applications that require relays with standoff voltages of above 1000V. One potential application is electrical vehicles (EVs). EVs contain an Insulation Monitoring Device (IMD) that periodically checks the galvanic isolation barrier between the high-voltage battery and the vehicle chassis. IMDs typically use relays to measure the leakage current across this isolation barrier [24]. A high-voltage iCoupler relay would be a space-efficient solution that provides the high reliability required in this safety-critical application. While the transistor process used in this thesis would not be adequate, gallium nitride (GaN) or silicon carbide (SiC) FETs could provide up to 1300V of output standoff voltage. We can adapt the rest of the relay architecture—including the oscillator, iCoupler transformer, and rectifier—from this thesis.

Chapter 9

Conclusion

We designed a galvanically-isolated solid-state relay to meet the increasing reliability and performance demands of modern ATE. Our ATE customer's most important needs were low on-resistance, stable operation, and long lifetime; additionally, we wanted the relay to have high bandwidth, fast switching speed, and high isolation voltage, combining the best features from existing electromechanical and solid-state relays. Finally, we wanted the relay to work off of a 5V/5mA input and have an efficiency of 20%, typical of similar devices.

For our relay's galvanic isolation barrier, we used the on-chip transformers of Analog Devices' iCoupler technology, which offer high withstand voltage and high reliability. However, since transformers can only couple ac signals, we also needed an oscillator and rectifier in our relay. We first determined the optimal architecture and design for each of the four stages of our relay: oscillator, transformer, rectifier, and output switch. Once the top-level architecture was set, we optimized the full design to increase the efficiency, limit the input current draw, and increase the gate voltage to achieve low on-resistance with smaller output switches.

We started out by using trial-and-error to test different design parameter values, but decided that this method would be infeasible. Therefore, we used a multi-objective genetic algorithm to quickly explore the large solution space, and we discovered a solution that hit

the efficiency, output voltage, and current targets. However, further analysis revealed that this solution was in fact very sensitive to parasitic capacitance and therefore could not be used in a real-world circuit.

Ultimately, lightening the output load on the rectifier and adjusting the transistor sizes on both the oscillator and the rectifier enabled us to achieve acceptable performance. The simulated relay is able to reach 100 mΩ on-resistance within 7.5 μs and has an output 3dB bandwidth of 4.8 GHz. The next steps will be to build on this working proof-of-concept simulation by testing at different process, voltage, and temperature (PVT) corners and adding closed-loop input current control. Then, we will perform layout, tapeout, and validate the target specifications, including the isolation voltage and lifetime requirements, on actual silicon. While silicon might not be able to achieve our ideal simulation results, we are still likely to hit our initial targets of 150 mΩ on-resistance, 100 μs turn-on and turn-off times, and 1 GHz bandwidth. From the simulation results presented in this thesis, the iCoupler relay shows strong potential to meet the ATE customer's low on-resistance requirement and to compete with existing reed and photoMOS relays on bandwidth and switching speed.

Bibliography

[1] "Wsts semiconductor market forecast fall 2023," World Semiconductor Trade Statistics, 28 November 2023. [Online]. Available: https://www.wsts.org/76/Recent-News-Release.

[2] O. Burkacky, J. Dragon, and N. Lehmann, "The semiconductor decade: A trillion-dollar industry," McKinsey & Company, 1 April 2022. [Online]. Available: https://www.mckinsey.com/industries/semiconductors/our-insights/the-semiconductor-decade-a-trillion-dollar-industry.

[3] "2023 state of the u.s. semiconductor industry," Semiconductor Industry Association, 2023. [Online]. Available: https://www.semiconductors.org/2023-state-of-the-u-s-semiconductor-industry/.

[4] *Switching handbook: A guide to signal switching in automated test systems*, 4th ed., Kiethley Instruments, Inc., July 2001, ch. 1. [Online]. Available: https://assets.testequity.com/te1/Documents/pdf/keithley/switching-handbook.pdf.

[5] P. Roettjer, "Testing techniques to improve relay reliability," *EE, Evaluation engineering*, vol. 44, pp. 44–48, Apr. 2005.

[6] "Reed relay basics." (26 March 2024), [Online]. Available: https://www.pickeringrelay.com/introduction-reed-relay-basics-part-1/.

[7] "Reed relays for automated test equipment applications," Coto Technology, Tech. Rep., 2022. [Online]. Available: https://cotorelay.com/wp-content/uploads/2023/07/ReedRelays-in-AutomatedTestEquip.pdf.

[8] "High voltage mini-sil/sip reed relays," Pickering, Data Sheet, 2022. [Online]. Available: https://www.farnell.com/datasheets/3716005.pdf.

[9] "G5v-1 low signal relay," Omron Corporation, Data Sheet. [Online]. Available: https://omronfs.omron.com/en_US/ecb/products/pdf/en-g5v_1.pdf.

[10] D. Hyman and M. Mehregany, "Contact physics of gold microcontacts for mems switches," *IEEE Transactions on Components and Packaging Technologies*, vol. 22, no. 3, pp. 357–364, 1999. DOI: 10.1109/6144.796533.

[11] "Application note 028: Photomos relays," Panasonic, Tech. Rep., 29 August 2005. [Online]. Available: https://www.mouser.com/pdfdocs/PanasonicPhotomosRelayPanasonicPhotoMOSRelays.PDF.

[12] "Lifetime of optocouplers," Wurth Elektronik, Tech. Rep., 17 February 2021. [Online]. Available: www.we-online.com/catalog/media/o303314v410%20ANO006a%20EN.pdf.

[13] "Photomos rf sop 1 form a low c×r product catalog," Panasonic, Data Sheet, 2022. [Online]. Available: https://mediap.industry.panasonic.eu/assets/download-files/import/semi_eng_rf1a_aqy22_s_cr.pdf.

[14] "Icoupler® technology: An alternative to optocouplers." (26 March 2024), [Online]. Available: https://www.analog.com/en/lp/001/icoupler-technology-alternative-to-optocouplers.html.

[15] "Adum3165/adum3166: 3.75 kv rms digital isolators for isolated usb 2.0 high, full, and low speed," Analog Devices, Data Sheet, 2020. [Online]. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/adum3165-3166.pdf.

[16] "Isolated, half bridge gate drivers with adjustable dead time, 4 a output," Analog Devices, Data Sheet, 2022. [Online]. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/adum4221_4221-1_4221-2.pdf.

[17] B. Chen, "Icoupler® products with isopower™ technology: Signal and power transfer across isolation barrier using microtransformers," Analog Devices, Tech. Rep., 1 April 2016. [Online]. Available: https://www.analog.com/en/resources/technical-articles/icoupler-products-with-isopower-technology.html.

[18] J. G. Kassakian, D. J. Perrault, G. C. Verghese, and M. F. Schlecht, *Principles of Power Electronics*, 2nd ed. October 2023, p. 296, ISBN: 9781316519516.

[19] T. H.Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, 2012, p. 93, ISBN: 9780521835398.

[20] B. Razavi, "The cross-coupled pair? part iii [a circuit for all seasons]," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 1, pp. 10–13, 2015. DOI: 10.1109/MSSC.2014.2369332.

[21] M. Chavez and E. Schott, "What is emc? 4 questions about emi, radiated emissions, esd and eft in isolated systems," Texas Instruments, Tech. Rep., August 2020. [Online]. Available: https://www.ti.com/lit/ab/slla524/slla524.pdf.

[22] M. W. Baker and R. Sarpeshkar, "Feedback analysis and design of rf power links for low-power bionic systems," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 1, no. 1, pp. 28–38, 2007. DOI: 10.1109/TBCAS.2007.893180.

[23] S. B. Selçuklu, "Multi-objective genetic algorithms," in *Handbook of Formal Optimization*, A. J. Kulkarni and A. H. Gandomi, Eds. Singapore: Springer Nature Singapore, 2023, pp. 1–37, ISBN: 978-981-19-8851-6. DOI: 10.1007/978-981-19-8851-6_31-1. [Online]. Available: https://doi.org/10.1007/978-981-19-8851-6_31-1.

[24] "Automotive high-voltage and isolation leakage measurements reference design," Texas Instruments, Tech. Rep., February 2023.