Towards a Single Bio-molecule Detector Based on CMOS Nanofluidic Platform

by

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Submitted to the Program in Media Arts and Sciences,
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Abstract

Cytokines secretion is a core component of the function of many cell therapy products: It affects the tissue repair capacity of induced Pluripotent Stem Cells (iPSCs) and Mesenchymal Stem cells (MSCs) and the tumorigenicity of Chimeric Antigen Receptor (CAR) T-cell therapies. Ideally, we would be able to continuously monitor the secretome of these cell therapies as they are transformed and expanded in manufacturing.However, state-of-the-art techniques for monitoring typically low concentrations of cytokines require either Mass Spectroscopy (MS) or immunoassays like Enzyme-linked Immunosorbent Assay (ELISA).
We propose the use of CMOS technology to build a proteomic platform with a single biomolecule resolution. A prototype chip has been designed and fabricated using standard foundary process incorporating a new implementation of a Solid State Nanopore (SSN) of size 55nm×162nm×100nm (w×l×h) with nanofluidic access channels that bridge the buffer solution between the assay space in the packaging structure – a poly carbonate/Polydimethylsiloxane (PDMS) package- and the nanopore on the chip. A silicon Single Photon Avalanche Detectors (SPADs) was also implemented and placed near the nanochannels to utilize fluorescence labeling imaging techniques. In addition, a read-out amplifier that achieves a midband gain of 36.2 dB at a 3 dB bandwidth of 0.1-3.6 MHz is also implemented on the same silicon die, paving the way to superior performance compared to ionic current read-out systems used earlier for electrical biomolecule detection, thanks to low parasitics as a result of integration. The aforementioned modalities integrated on a single chip open the space for the use of CMOS platforms in the electrical and optical interrogation of biomolecules, opening a new horizon for near real-time biomarker assays.
The following thesis builds on earlier work that was performed in [1][2] with the objective of expanding on different techniques to interface and characterize the performance of these modalities, especially after post-processing the chips with the aid of tools at MIT.nano. The thesis explores the further deployment of integrated SPAD in a Fluorescence Lifetime Imaging (FLIM) system to image fluorescence-labeled molecules, showcasing the capabilities of the CMOS nanofluidic platform to detect biomarkers such as cytokines.

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To Mona Elgareeb, My beloved Mother

Without your dedication and sacrifices, I wouldn't be where I am today.

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Acronyms

ASIC	Application Specific Integrated Circuits
BCD	Bipolar-CMOS-DMOS
BEOL	Back End OF the Line
bp	Base Pair
BSA	Bovine Serum Albumin
CAD	Computer Aided Design
CAR	Chimeric Antigen Receptor
CMOS	Complementary Metal-Oxide-Semiconductor
COB	Chip On Board
CRS	Cytokine Release Storm
DCR	Dark Count Rates
DFT	Density Functional Theory
DNA	Deoxyribonucleic Acid
ELISA	Enzyme-linked Immunosorbent Assay
EMCCD	Electron Multiplying Charge Coupled Device
FEM	Finite Element Method
FLIM	Fluorescence Lifetime Imaging
FRET	Förster Resonance Energy Transfer
FWHM	Full Width at Half Maximum
ICB	Inductively Coupled Plasma
iPSC	induced Pluripotent Stem Cell
LC/MS	Liquid Chromatography-Mass Spectrometry
LDO	Low Dropout
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MS	Mass Spectroscopy
MSC	Mesenchymal Stem cell
NAA	N-terminal Amino Acid

NGS	Next-Generation Sequencing
NS-PNP	Navier Stokes-Poisson Nernst Planck
PCB	Printed Circuit Board
PCR	Polymerase Chain Reaction
PDMS	Polydimethylsiloxane
PDP	Photon Detection Probabilities
RIE	Reactive Ion Etching
ROIC	Readout Integrated Circuit
RPS	Resistive Pulse Shaping
SBS	Sequencing By Synthesis
SEM	Scanning Electron Microscope
SiN_X	silicon nitride
SNR	Signal to Noise Ratio
SPAD	Single Photon Avalanche Detector
SSN	Solid State Nanopore
TCR	T-Cell Receptor
TCSPC	Time Correlated-Single Photon Counting
TIA	Transimpedance Amplifier

Chapter 1

Introduction

Personalized medicine, also known as precision medicine, is gaining popularity as a prominent approach to health care that seeks to offer personalized medical care to each patient, taking into account their distinct genetic, environmental and lifestyle characteristics. At the heart of this approach is the advent of new technologies that make them more accurate and tailored to the needs of each patient [3]. Motivated by the utility of omics: genomics, transcriptomics, and proteomics, this work aims to explore the potential of a Complementary Metal-Oxide-Semiconductor (CMOS)-based nanofluidic platform that features seamless integration of a nanopore, nanofluidic channels, an electrical read-out amplifier, and optical read-out photonics. This integration enables proteomic functions by detecting biomolecules in low abundance or, ultimately, on an individual basis. The goal of this CMOS platform is to create a real-time cell secretion monitoring tool for a specific personalized cancer therapy technique: CAR T cell therapy.

The approach of using a nanopore-based system to resolve biomolecules in cellular secretion is inspired by the ground-breaking work that started in 2005 when a variety of Next-Generation Sequencing (NGS) techniques emerged in which by labeling nucleotides in random fashion and aggregating over a multitude of samples, a technique referred to as Sequencing By Synthesis (SBS) [4], the DNA sequencing capability went from 1 million

Base Pair (bp)/day to more than 100 million bp/hour in some desktop DNA sequencing machines [5]. The natural evolution of this technology should be employed in proteomics and protein sequencing [6]. In Figure 1-1 we can spot the drastic effect of commercializing NGS systems on the total cost of genome sequencing [7], a cost reduction of five orders of magnitude was achieved in two decades, suggesting the potential to investigate personalized medicine solutions through the lens of NGS applied to proteomics.

The remainder of this chapter provides an overview of the challenges and potential of using a nanopore-based platform to augment CAR-T cancer cell therapy manufacturing. Then it expands on the capabilities that the foundry CMOS process offers in the implementation of a nanofluidic delivery system and the further integration of electrical and optical sensing modalities on the same silicon die. Quantitative metrics for this kind of platform will be discussed briefly in this chapter and in more detail as we progress through the thesis. This includes ionic current amplifier performance metrics such as gain and noise performance and photodetector characteristics such as detection efficiency and responsivity in order to assess benefits and limitations of the CMOS nanofluidic platform. This chapter is organized as follows. Section 1.1 introduces one of the motivating problems for real-time biomolecule monitoring, how it is currently dealt with, and how the CMOS platform can help in this context. Section 1.2 presents an overview of the novel techniques for integrating nanofluidics into the flow of the CMOS design. Section 1.3 introduces the electrical modality of the proposed platform, where the physics of transduction, practical limitations in terms of noise performance, and integrated signal readout are introduced. Section 1.4 introduces the optical modality of the proposed platform, in which the benefits of optical detection of labeled biomolecules and their practical implementation are briefly discussed, along with the integrated optical detector readout circuitry. Finally, Section 1.5 provides an overview of the current strategies of the NGS systems and how the proposed platform fits into this picture.

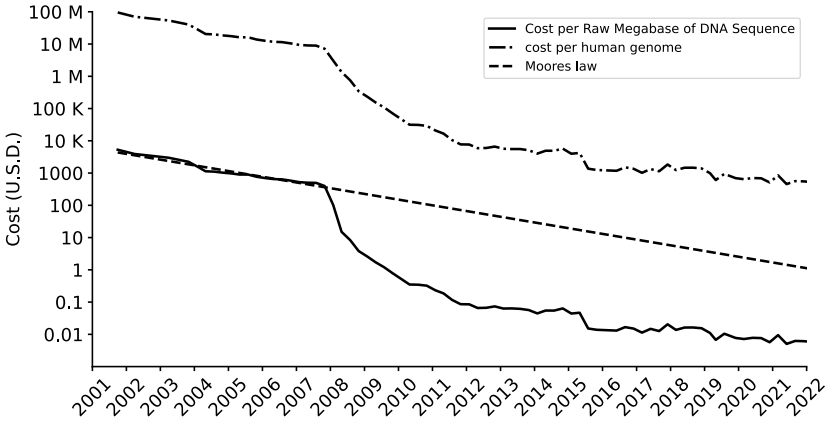


Figure 1-1: The cost-accounting data for genome sequencing for two metrics: Cost per Megabase of DNA Sequence and Cost per Genome. Hypothetical data based on Moore's Law, which predicts the doubling of compute power every two years, for comparison [7].

1.1 Motivation: Continuous Monitoring of Cytokine Secretion for CAR-T Cell Therapy

Immunotherapy represents an important milestone in cancer treatment advances, employing the immune system of the body to combat malignant cells. This approach involves the genetic modification of T cells extracted from a patient's blood, enabling them to express synthetic receptors that integrate antigen-binding domains with T cell properties. These genetically engineered cells, known as CAR T cells [8] are expanded and reinfused in the patient to target and eradicate chemotherapy resistant cancer cells through a process known as adoptive cell transfer therapy [9]. CAR T cell therapy, still under development, has been approved by the FDA for certain lymphomas and leukemias [10] and represents a significant change compared to conventional treatments such as surgery, chemotherapy and radiation.

The CAR component in these modified T cells specifically binds to antigens in cancer cells, triggering a potent immune response upon encountering target cancer cells. This response not only involves direct cytotoxicity through the secretion of pro-inflammatory cytokines and other cytotoxic molecules but also stimulates broader immune reactions against the tumor, significantly reducing off-target effects and sparing healthy cells. However, a major side effect of CAR T cell therapy is Cytokine Release Storm (CRS), an acute inflammatory process that can have severe and even fatal consequences [11] that requires careful monitoring and management of the release of pro-inflammatory cytokines.

In parallel, the potential of CAR-T cell therapy has spurred research into various stem cell platforms capable of differentiating into T cells. iPSCs, for example, can be induced to differentiate into thymocytes, which further mature in the thymus through rigorous selection processes, eventually becoming functional T cells with diverse T-Cell Receptors (TCRs) [12]. This in vitro replication of the development of T cells from iPSCs underscores the viability of the method to generate mature functional T cells. In addition, MSCs harvested from patient tissues or other sources exhibit the capacity to modulate T-cell functions through paracrine

signaling and direct cell-cell interactions. These cells not only support the development of regulatory T cells, promoting immune tolerance, but also suppress excessive immune responses by inhibiting T-cell activation and proliferation. This comprehensive strategy underscores the need to integrate biomarker identification and verification throughout the drug development process, from discovery through clinical trials, to ensure the efficacy of personalized cancer treatments. Current clinical trial designs, however, often overlook the incorporation of molecular diagnostics and biopsies due to financial constraints and patient recruitment challenges, despite a growing trend to include biomarkers in trials assessing biological therapies [13].

To address the problem of secretome monitoring of these cell therapies as they undergo transformation and expansion during manufacturing, we can start by identifying examples of those secretions in terms of concentration and sizes listed in Table 1.1. Analysis of the secretome can help in detecting immune-related adverse events in CAR T cell therapies. Unlike protein therapeutics, whose functional potency can be assessed through structural and affinity analyses, cell therapies pose challenges in potency evaluation due to the complexity of cell functions. It is posited that the most direct method to evaluate the functional potency of cells is by measuring their capacity to secrete bioactive proteins. Considering the human genome's encoding capacity, approximately 15% of the around 20,000 protein-coding genes are predicted to be secretory, in stark contrast to the roughly 5,000 that code for membrane-bound proteins [14]. Second, we look at the available platforms currently used for quantifying cytokine levels. The ELISA is a widely accepted method for quantifying cytokine levels [15][16], with traditional protocols typically lasting 1-3 hours [17]. Picokine has refined this to a faster 90-minute protocol capable of detecting cytokines concentrations as low as 156 pg/ml [18]. Despite its precision, the utility of ELISA in clinical settings is constrained by its time-consuming nature. As an alternative, proteomic barcode assays have emerged, utilizing fluorescent labeled secondary antibodies and spatial recognition for protein identification. IsoPlexis has further advanced this technology with a proteomic barcode assay that requires only a 5-minute sample preparation time and can detect a broad spectrum of cytokines and chemokines [19]. MS based proteomics are considered the

Cytokines	Cytokine type	Concentration [pg/ml]	molecule size
IL-6	Pro- and anti-inflammatory	22 ± 8.6	21-30 KDa [24]
TNF-α	Pro-inflammatory	5.9 ± 0.4	55-75 KDa [25]
INF-γ	Pro-inflammatory	7 ± 2.5	33 KDa [26]
IL-4	Anti-inflammatory	230 ± 50	12-20 KDa [27]
IL-10	Anti-inflammatory	38 ± 2.1	18 KDa [28]

Table 1.1: Listing of various cytokines and their properties

current gold standard in large-scale protein characterization, however, it exhibits limited sensitivity and coverage when confronting low-concentration protein samples [20]. Liquid Chromatography-Mass Spectrometry (LC/MS) has also shown promise in cytokine profiling within the field of proteomics [21]. Nonetheless, these methods are generally limited by their sensitivity when analyzing low-abundance proteins and require significant time to accumulate and analyze each ion. For example, work in [22] reports 0.5 second time allocated per peptide which results in a 160-minute run to consistently quantifying about 1000 proteins per cell making continuous cytokine monitoring challenging, on the other hand, LC/MS can reach to 0.74 ng/mL for detection of a specific protein in biological sample [23].

The techniques outlined in the above discussion summarized in Figure 1-2 establish the criteria for an ideal continuous cell secretion profiling system. The motivation of integrating fluidic compartments with optical and electrical readout systems on the same chip is to explore the possibility of achieving real-time monitoring system for proteomics that achieves the high sensitivity, multiplexing capability, noninvasiveness, and long-term stability. Such a system would allow for the continuous and dynamic analysis of secretion patterns, capturing subtle changes in secretion levels at high sensitivity, potentially down to the picogram per milliliter range. Moreover, it would enable the simultaneous monitoring of multiple analytes without disrupting cell function or viability, and maintain reliable performance over extended monitoring periods.

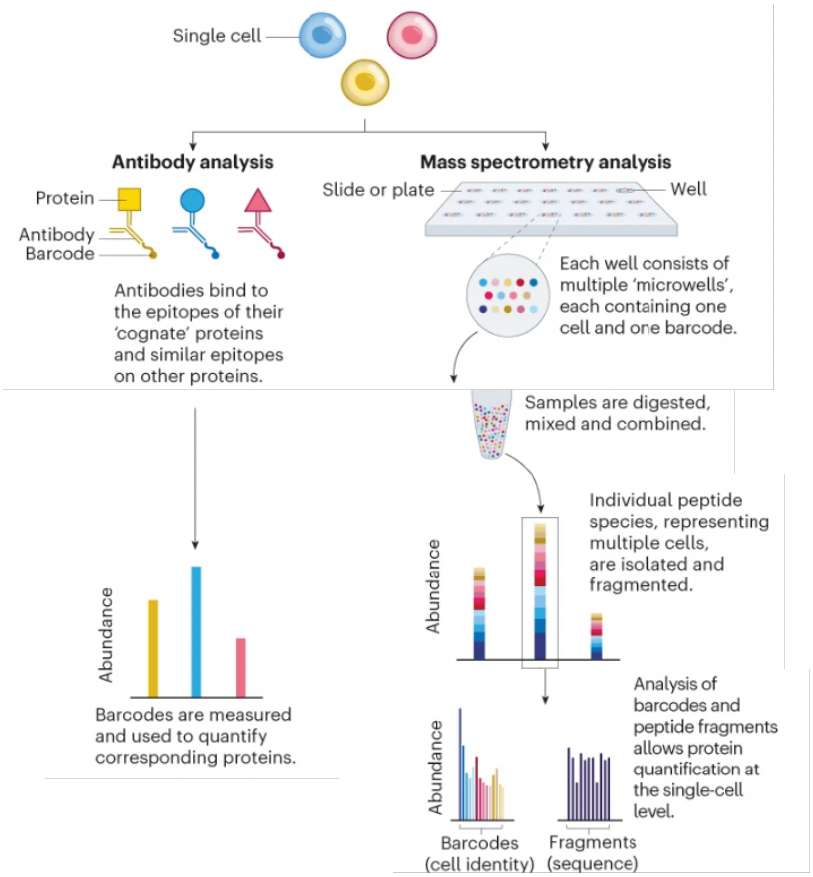


Figure 1-2: Established Single Cell biomarker analysis techniques adopted from [29], [30]. Antibody based techniques like ELISA quantify abundance by monitoring the binding antibodies where as in MS the abundance is characterized by binding ions which segregates different peptides.

1.2 Motivation for CMOS Nanofluidics

The advancement highlighted in Section 1.1 has a common feature inherent, that is miniaturizing sample size by utilizing the micro / nano fluid handling structure. Although microfluidic devices are commonly employed in transcriptomics, their application in proteomics is still emerging motivated by the fact that there is currently no known way to artificially amplify the amount of protein in a cell, and therefore reduced sample handling is required and essential for real-time monitoring. Figure 1-3 provides an overview of the role of microfluidics in miniaturized cell secretion monitoring systems, especially in cell compartmentalization and sorting. In [19] the 5-minute sample preparation was achieved utilizing a 2 nl micro well fabricated on a custom chip that can handle 0 to 5 cells. A similar scheme is in [21] where a custom nanoletre fluid handling chip was designed by etching and patterning glass slides followed by Silane treatment and micro-ring surrounding [31].

Microfluidic device development relies on well-established and consistent soft lithography fabrication techniques. These techniques utilize lithography-based processes to pattern microfluidic devices made of materials such as PDMS. Other polymers such as SU-8 are utilized to fabricate masters for PDMS replication [32]. The feature size of these devices is limited by the soft lithography resolution, which can reach 1 μm size. We would like to bridge the gap between using custom glass to pattern nanometer size well and the conventional microfluidics platform such as PDMS using CMOS technology driven by the advancement in CMOS nanoprocessing techniques. In addition, this aligns with the main objective of real-time monitoring of secretion by embedding the sample preparation stage alongside sensors and data readout compartments. The researchers in [33] presented a prototype of nanochannels with dimensions of 367 nm in depth and 100 nm in width by post-processing a periodic layer of Si_3N_4 residing on a flat SiO_2 layer on top of a Si wafer serving as a substrate using e-beam lithography patterning. In contrast to post-processing a CMOS compatible material, the work in [2] proposed the first full silicon nanochannels integrated in a CMOS die that was fabricated earlier in a standard CMOS process by employing polysilicon as a sacrificial layer. This approach opens the doors to the use of Computer Aided Design

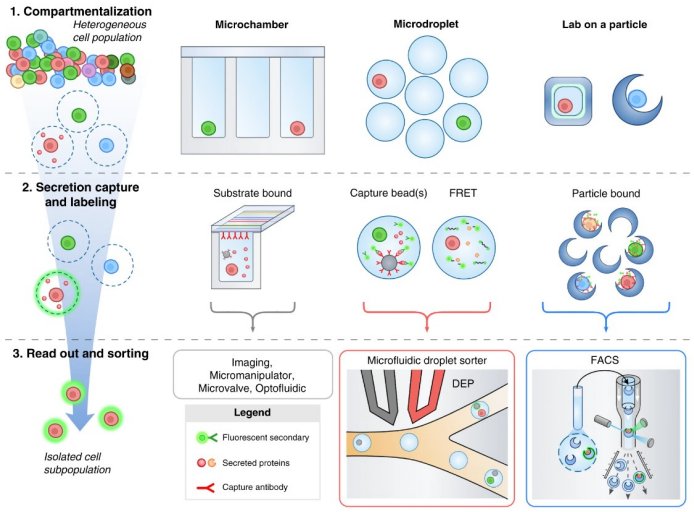


Figure 1-3: Illustration adopted from [35]: The analysis of secreted products from individual cells involves three key steps: (1) Compartmentalization where Cells are isolated into individual compartments to prevent cross-talk between cells and concentrate their secreted products.(2) Accumulation and Detection of Secretions which involves variant sensors to identify labels or molecules themselves. (3) Recovery of Target Cells using low-throughput liquid handling, microvalves, optofluidics, and micromanipulation are used for cells in microwells.

(CAD) tools to pattern wide varieties of shapes and designs that were not feasible before using conventional nanofluidic patterning techniques. This is achieved by controlling the shapes that will be fabricated on the defined sacrificial layer, a standard flow used to control the shape of transistor gates, and it has recently been adopted to integrate photonic devices in a zero-change CMOS process [34]. Later, the same approach was successfully adopted to implement and fabricate a nanofluidic channel on other CMOS die [1]. Figure 1-4 shows the fabricated channel which is designed in a throttling fashion to mimic the function of a nanopore, which will be highlighted in some detail in the coming section, confining the biomolecules for electrical characterization. In fact, the dimensions of this throttling are limited by the technology node on which the chip is designed, GF 55BCDLite but we can argue that benefits outweigh this limitation specially as we go through the coming chapters which report that the post processing required to etch away the sacrificial layer has minimal effect on the other integrated modalities.

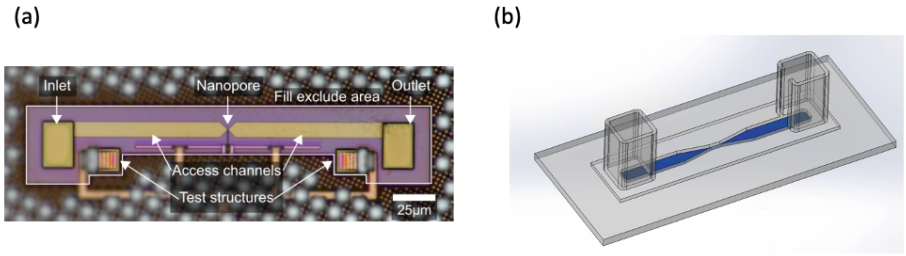


Figure 1-4: Nanofluidic CMOS Solid State Nanopore: (a) Micrograph from second version of the nanofluidic platform chip for the nanopore with access channels [1] (b) 3D illustration for fluidic path (not to scale).

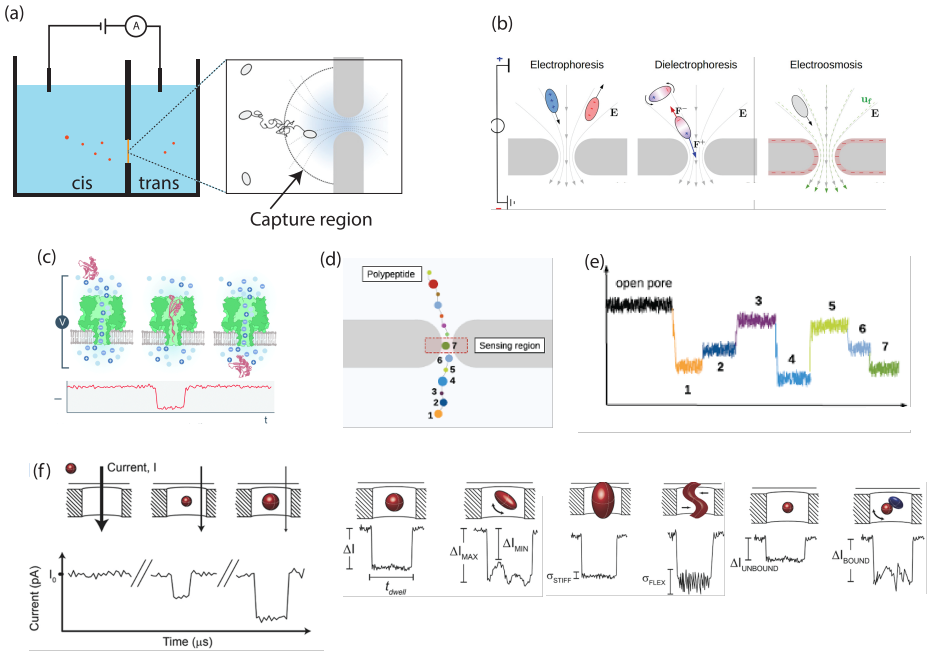


Figure 1-5: Conventional nanopore: outlook (a) Particles translocate through nanopores when it approaches the capture region, at which forces different forces resulting from confinement of electric field near nanopore overcomes Brownian motion (b) Electrophoresis, Dielectrophoresis and Electroosmosis are examples of those forces affecting biomolecules depending on their properties [36] (c) Illustration of dynamics of transduction adopted from [37] (d) Extending the transduction through different peptides that requires thickness of sensing region of the same order as biomolecule (e) Conceptual trace for capturing different polypeptides, this can occur if the nanopore is well designed with a good readout system that have sufficient SNR (f) Work in [38] arguing that particles with different volume, shape, aggregation state, or conformational differences can be resolved by translocation current readout.

1.3 Electrical Modality: Nanopore for Single-Molecule Measurements

Nanopores, a de novo sensing method that aims to detect proteins at the level of a single molecule, can be traced back to the 1950s when they were used in Coulter counters to count red blood cells. This technique, coupled with the introduction of single-channel ionic current recording in the 1970s, which was recognized with the 1991 Nobel Prize in Physiology or Medicine awarded to Erwin Neher and Bert Sakmann, paved the way to next-generation nucleic acid sequencing introduced in the late 1990s [39]. Nanopores have been extensively utilized for stochastic sensing and characterization of various molecules, including DNA [40], RNA [41], peptides [42], proteins [37], metabolites, and protein-DNA complexes [43], at the single-molecule level. In particular, the commercial success of nanopore-based DNA/RNA sequencing has spurred numerous potential applications in single-cell proteomics, offering a relatively straightforward high-throughput format [44]. In what follows is a justification for the motive of adapting the SSN in CMOS nanofluidic platform and how this could solve the real-time cell secretion problem.

1.3.1 Nanopores: Paving the way to real-time single cell proteomics

A nanopore is a tiny pore with dimensions on the nanometer scale, located within an insulating membrane. These pores can be naturally occurring within biological systems, typically formed by proteins within lipid bilayers, or artificially engineered in materials such as silicon, silicon dioxide, silicon nitride, or two-dimensional materials such as graphene [45]. Hybrid structures that combine protein channels with synthetic membranes are also feasible [46].

Biological nanopores are typically self-assembled from protein subunits, peptides, or DNA scaffolds within lipid bilayers or block copolymer membranes [47]. In contrast, SSNs are crafted in durable materials such as silicon nitride, boron nitride, molybdenum disulfide and

graphene, which are supported by substrates such as silicon or glass. These SSNs can be created using various nanoprocessing techniques, such as Focused Ion Beam milling, controlled dielectric breakdown, Reactive Ion Etching, and Atomic Layer Deposition. Moreover, the surface properties of SSNs can be modified, for example, by using surfactants such as sodium dodecyl sulfate to enhance electrokinetic sensing capabilities for detecting unfolded proteins [48]. Examples of these structures are shown in Figure 1-6. The unique single molecule sensing capability of nanopores is derived from their ability to confine molecules within the minuscule spatial area of the opening of the nanopore, allowing for precise detection and analysis via electrical stimuli. Applying a voltage across the nanopore that separates two different electrolytes (referred to as the cis and trans sides) induces the translocation of analytes, as the forces resulting from electrophoresis, dielectrophoresis, and advection overcome Brownian motion [49]. Figure 1-6 illustrates these forces and how monitoring ionic current resulting from translocation events can inform some properties of the biomolecule properties such as size, orientation, and morphology [38].

1.3.2 Nanopores: Physics of Transduction

The setup for the measurement of molecular translocation is shown in Figure 1-5(a). The nanopore is located at the separating membrane between cis and trans, while the change in current is monitored using a sophisticated amplifier with certain gain and noise specification that will be discussed in a later section. Particles, depending on their material properties and charges, experience forces in aqueous environment such as dielectrophoresis, electrophoresis, and electroosmosis. There is a certain distance known as the capture region when these forces overcome a Brownian motion such that it is pulled from one side to another [36]. As the particle threads through the nanopore it blocks the flow of ionic current for a finite time, as illustrated in Figure 1-5(c) which changes the overall resistance seen by the amplifier [37]. This method, referred to as Resistive Pulse Shaping (RPS) is conceptually the simplest means to interrogate molecular structure, Consequently, it was the first nanopre sensing modality to achieve commercial impact in Deoxyribonucleic Acid (DNA) sequencing [50] [51]. If ohmic behavior is assumed for the baseline ionic current,

then it follows Equation 1.1 and the perturbation in conductance as defined Equation 1.2 is related to the baseline current following Equation 1.3. The ratio $\Delta I_t/I_{base}$ is what correlates with each individual particle, oligomer, or biomolecule, and the hope is that each of them correlates to the fixed ratio with a high confidence interval stochastically. For DNA sequencing experiments using SiN_X where homopolymers such as adenine and cytosine are the objective of detection, this ratio lies in the range 30 to 80% [52].

$$I_{base} = G_p V_{dc} \tag{1.1}$$

$$G_p = G_{dc} - \Delta G_t \tag{1.2}$$

$$I_p = I_{base} - \Delta I_t = I_{base} - \Delta G_t V_{dc} \tag{1.3}$$

For a particle/biomolecule to produce a detectable pulse in a scheme RPS, it is argued that the particle size should be no smaller than three orders of magnitude than the nanopore volume [38]. This fact is formulated in Equation 1.4 where the right-hand side is a volumetric ratio of the particle to the nanopore. However, the lower limit on the nanopore size is set by the system allowed bandwidth, as smaller nanopores would lead to a more intense electric field, i.e. faster translocation event.

$$\frac{\Delta I_t}{I_{base}} = \frac{\Delta V_t}{V_{pore}} \tag{1.4}$$

The thickness of the nanopore in the RPS method should be comparable to the size of the biomolecule that is detected. For example, a 10-nm thick nanopore matches the lateral dimension of about 30 DNA bases, making it less effective for DNA analysis since all bases impact the blockade current simultaneously. However, SSNs allows for discerning the shapes and orientations of the particles relative to the electric field. The method can also detect dynamic behaviors such as particle rotation within the electric field, which introduces current fluctuations. In addition, it can integrate multiple events into a single pulse and link even small temporal changes to the surface morphology of the detected molecules, as shown in Figure 1-5(f).

Another nanopore transduction variant is the detection of transverse tunneling current variations which requires a few nanometer gab between two conducting electrodes which is challenging to achieve in a CMOS node but has the advantage of decoupling the molecule driving potential from the sensing potential. The nanopore can also be implemented in a transistor gate Metal Oxide Semiconductor Field Effect Transistor (MOSFET) where the translocation event contributes to a change in gate charge that is proportional to the gate voltage ($\Delta q = C\Delta V$) [53] . Figure 1-7 summarizes the three transduction techniques. To add a layer of translocation speed control to these different techniques, researchers often functionalize the membrane surface containing the nanopore [54] to either catch a certain molecule or slow down the translocation which sacrifices the real time aspect of detection. The current version of the proposed CMOS nanopore only implements the RPS for biomolecule sensing, although the metal stack of the CMOS Back End OF the Line (BEOL) and integrated MOSFETs leaves the space open to explore other electrical sensing modalities.

1.3.3 Nanopores: Transduced Signal Dynamics and Readout Schemes

Nanopores are inspired by ion channels in biological cell membranes, which are protein structures that create pores for ions to pass in and out of cells, thus regulating processes such as electrical signaling, nutrient uptake, and cell volume. Due to this similarity, clamping amplifiers have been widely adopted for nanopore readout [55]. From its name, clamping amplifiers fix the voltage "clamp it" at certain value and monitor the change in ionic current induced by the transfer of ion species. This is a well-established technique for recording macroscopic whole-cell or microscopic single-channel currents flowing across biological membranes through ion channels, to study the properties of the ion channels. Figure 1-8 (a) illustrates this concept, where as in Figure 1-8 (b), (c) shows an example of a sub-2 μm needle designed to surround a single cellular ionic channel in a neuronal cell [56]. For a single nanopore experiment, a flow cell such as the one depicted in Figure 1-8 (c) can serve well in capturing translocation events, where the ionic current between the two reservoirs is measured by a pair of Ag/AgCl electrodes. However, the micropippet can be combined

with SSN nanopores for automation purposes and to reduce the volume of the liquid [57].

The patch clamp amplifier typically consists of an amplifier, a digitizer, and a filter. Low-pass filters are used to reduce high-frequency noise, improving the SNR ratio but sacrificing time resolution [58]. This trade-off is critical in nanopore sensing, as it affects the ability to detect fast translocation events. A well-known instrument in this context is the Axopatch amplifier [59], a specialized Transimpedance Amplifier (TIA) designed specifically to amplify current levels of a few picoamperes [60] which is equivalent to the ion flux exhibited by a single-ion channel that is normally expected to conduct approximately 10 million ions per second considering the low noise restrictions at these levels of current. Recent advances have led to the development of Readout Integrated Circuits (ROICs), which integrate the necessary read-out functions into a microelectronic chip and open the door to the implementation of multiple-channel read-out on a single chip. The first monolithic integration of a SSN with a readout CMOS based amplifier was introduced in [61]. More sophisticated trials have followed, such as the one depicted in Figure 1-8 (e), in which a biological nanopore, the type 1 ryanodine receptor (RyR1), is placed in a libid bilayer that is formed in a microwell SU8 flow cell dedicated to monitor flickering of Ca^{+2} ions [46]. Another variant following the same strategy was introduced in [62] and is shown in Figure 1-8 (f) where a silicon nitride-made SSN is utilized to measure short translocation DNA but with a larger Teflon flow cell. In both studies, the integrated amplifier was designed to operate at a bandwidth of up to 500 kHz, which indeed adds to the baseline noise as can be seen in Figure 1-8 (g).

Noise in nanopores are the collective contribution of (i) low-frequency $1/f$ noise ($\lesssim$ 100 Hz), also known as "flicker", "pink" or "protonation" noise, (ii) shot noise and thermal current noise ($\sim$ 0.1-2 KHz) which are white noise sources, i.e. frequency independent, (iii) high-frequency dielectric noise ($\sim$ 1-10 KHz), (iv) capacitive noise ($>$ 10 KHz)[58]. The dominant noise at higher end of the spectrum can be described by Equation 1.5 where C_{total} is the effective total parasitic capacitance at the input of amplifier and the root mean square value of noise current follows Equation 1.6. These contributions are depicted in Figure

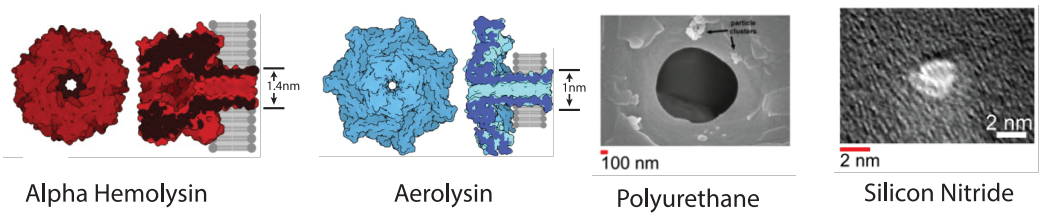


Figure 1-6: Illustrations of two examples of biological nanopores adopted from [47] and SEM images of fabricated solid state nanopores adopted from [63].

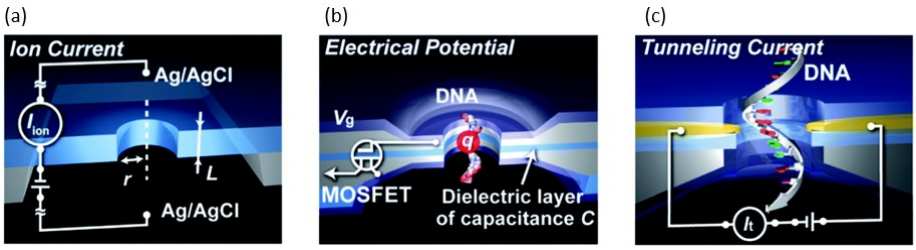


Figure 1-7: Different variations of label free sensing using nanopore (a) RPS based sen sing (b) MOSFET capacitance based sensing (c) Sensing through monitoring transverse tunneling current. Illustration adopted from [53].

1-8 (k) where we can see the immediate effect on noise owing to reduction of parasitic capacitance as a direct result of tight integration maintaining the SNR at an acceptable level to resolve translocation events shorter than 3 μs albeit the increase in baseline noise. Similar argument holds for the proposed CMOS nanofluidic platform where the amplifier electrodes are directly embedded in the access channels as shown in Figure 1-8 (i). The total parasitic capacitance components are now dependent on the metal layers and vias of the CMOS BEOL as shown in the cross section in Figure 1-8 (j) which is inherently low compared to any flow cell integration schemes and operates up to a 1 MHz bandwidth. Capacitance extraction for CMOS nanofluidic platform is detailed in Chapter 2.

$$S_{I,capacitance} = 4\pi^2 C_{total}^2 \nu_n^2 f^2 \tag{1.5}$$

$$I_{noise} = \sqrt{\int_0^{B_{max}} (S_{I,flicker} + S_{I,thermal} + S_{I,shot} + S_{I,dielectric} + S_{I,capacitance})\, df} \tag{1.6}$$

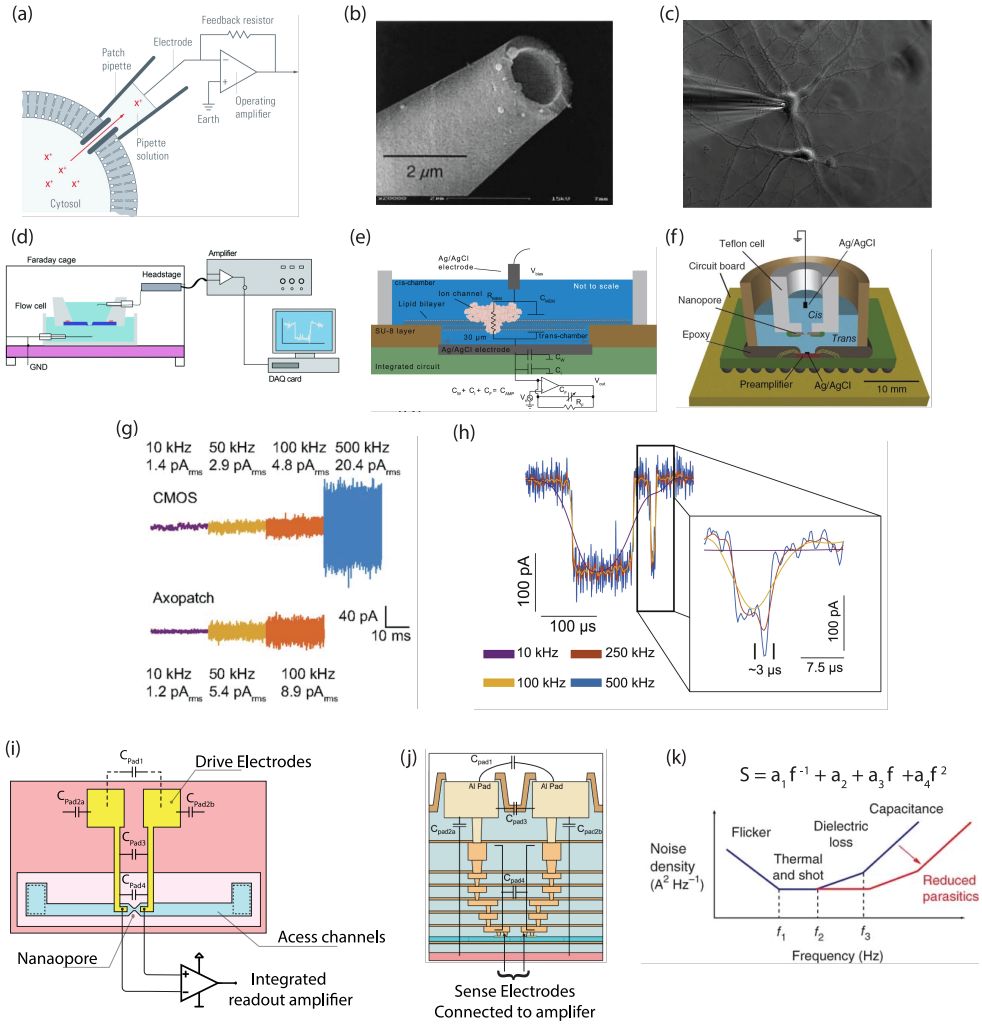


Figure 1-8: Nanopore readout schemes and its signal dynamics: (a) Schematic illustration of the use of clamp amplifiers to monitor ionic current through a cell membrane [60] (b) Fabricated micro pipette used to surround single ion channel [56] (c) Phase contrast image of a patch pipette attached to the membrane of a cultured neuron courtesy of Dr. Ainhara Aguado, Ruhr University Bochum, Germany. (d) Schematic illustration of using the patch clamp amplifier in a nanopore experiment [37] (e) Implementation of tight integration of a CMOS amplifier with a biological nanopore to monitor Ca^{+2} ions [46] (f) SSN integration with a a CMOS readout amplifier to monitor short DNA translocation [62] (g) Effect of readout amplifier bandwidth on baseline noise current in both integrated and Axopatch amplifier showing drastic increase at 500 kHz bandwidth [46] (h) Capturing sub 3μs translocation event of Ca^{+2} ions at 500 kHz bandwidth Vs. missing the same event at 100 KHz Bandwidth[64] (i) Schematic of integration of readout amplifier achieved in CMOS nanofluidic platform (j) Cross section of BEOL of the GF 55BCDLite used to build the CMOS nanofluidic chip showing different contributions of metal layers and vias to parasitic capacitane [1] (k) Different components of noise spectrum in a nanopore system [64], [58].

1.4 Optical Modality: Fluorescence Spectroscopy for the Characterization of Biomolecules

Fluorescence-based methodologies are foundational to numerous modern instruments in life sciences. For example, replacing radioactive labels with fluorescence labeling in the Sanger sequencing method revolutionized DNA sequencing. The sequencing speed was initially reported to improve from 100-200 bp per day to 200 bp in 13 hours after its introduction [65]. When applied to next-generation sequencing (NGS), the SBS method achieved sequencing rates of 6 terabases in a 13-hour run, as demonstrated by the Illumina NovaSeq 6000 system [4]. This system relies on the integration of microfluidics with flourescence imagers for various steps of the sequencing protocol, including library preparation, cluster generation, and the process of sequencing itself where the ability to quickly and accurately switch between different nucleotide solutions governs the accuracy of the sequencing process. Pacific Biosciences has also developed a platform for real-time observation of fluorescently labeled nucleotides incorporated into a DNA strand, enabling the sequencing of individual DNA molecules in real time. This system uses Zero-Mode Waveguides—nanophotonic structures that confine the optical observation volume to a zeptoliter scale—and a confocal fluorescence detection system with an Electron Multiplying Charge Coupled Device (EMCCD) camera for optical detection. The system shown in Figure 1-9 (a), (b) allows real-time monitoring of fluorescent signals emitted during DNA synthesis at the single molecule level [66].

Transcriptomics and single cell proteomics also benefit significantly from fluorescence spectroscopy techniques. Protein fingerprinting, a simplified scheme in which a subset of amino acids is fluorescently labeled and detected, is used to identify certain pathogens and biomarkers. In [67], researchers identified Escherichia coli by fluorescently labeling a range of 50 to 160 kbp and stretching DNA strands using nanofluidic channels. In [68], a computational framework proposed the feasibility of identifying more than 70% of nearly 20,000 human proteins by labeling only two amino acids, cysteine (C) and lysine (K) and determining the distance between them on the protein chain. This approach can be extended to

more challenging problems, such as protein sequencing. The principle of identification of protein polypeptides through Edman degradation cycles is demonstrated in Figure 1-9 (c). Quantum-Si [69] implemented a similar scheme in CMOS nanowells to process dye-labeled peptides added as recognizers for N-terminal Amino Acids (NAAs) from other peptides. These labeled peptides bind to NAAs and are sequentially cleaved by aminopeptidases, which are monitored by a light-sensitive photodiode equipped with high-speed global shutters (collect and reject gates) to manage photon detection. However, cleaving peptides is a lengthy process that is not a real-time assay.

Of all the attributes of the fluorescence process, the fact that the fluorescence lifetime of a fluorophore depends on its molecular environment rather than its concentration has generated significant scientific interest in FLIM [70]. FLIM is particularly valuable because it can resolve changes in the binding, conformation, and composition of biologically relevant molecules, providing insights that are not obtainable through steady-state fluorescence techniques. The fluorescence decay function offers the most direct insight into the molecular interactions of a fluorophore with its biological environment [71]. Time Correlated-Single Photon Counting (TCSPC) is the preferred technique for characterizing the fluorescence decay lifetimes of low-light signals emitted from single dye molecules in response to synchronized optical impulses, making it a good candidate for the single biomolecule sensing platform, as it offers picosecond accuracy and high photon efficiency, allowing precise multiexponential analyzes of molecular interactions within live cells using methods such as Förster Resonance Energy Transfer (FRET) [72].

Typical TCSPC apparatus includes a pulsed optical source, a discrete detector such as a SPAD or photomultiplier tube (PMT), external time-to-digital conversion (TDC) hardware, and a PC to compute the decay constant. Optical filters are used to separate the excitation pulse from the fluorescence response to enhance SNR. In the context of a single biomolecule sensing platform, a low abundance sample needs to be brought in close proximity to the detector. The breakthrough implementation of the first SPADs in standard CMOS technology [73] motivated the exploration of integrated SPAD detectors in a FLIM setup where

the implementation of a TDC circuit and the readout circuit are on the same chip [74]. Several milestones in CMOS implementation of FLIM followed which incorporate number of integrated SPAD ranging from 1 to an array of 256 by 256 detector (pixel) for imaging [75]. In what follows a brief introduction of the integrated CMOS nanofluidic detector that potentially allows fluorescence lifetime measurements for biomolecules confined in the integrated nanopore where the discussion is limited to performance of detectors placed around nanochennels, and not in an imaging array fashion.

1.4.1 Integrated Optical Detector: Zero-Change CMOS SPAD

The CMOS nanofluidic platform offers tight integration of a zero change SPAD close to the access nanochannel and below the channel in some instances. These variants are shown in Figure 3-4 where the active area of the cmos nanofluidic chip is depicted. The same CMOS foundry process (GF 55BCDLite) used to build nanofluidics and integrated amplifier also offers multiple doping profiles originally intended for high-power and RF devices, but was ultimately employed in creating deeper junctions and enabling controlled higher-voltage operation by exploring the parameter space of various photodiodes available in this process. Several specific parameters were adjusted during the investigation to assess their impact on detector performance. These parameters include the detector's active diameter (ranging from 4 to 20 µm), the type of guard ring (STI, p-substrate, or both), the width of the guard ring (ranging from 1.5 to 2 µm), the outer contact width, and the contact geometries. Efforts are underway to integrate single-photon avalanche diodes (SPADs) into deep-scaled CMOS technologies with the aim of achieving higher performance electronics, improved fill factor photodetectors, and integration with finer nanopore structures. However, scaling faces a significant limitation, the use of higher doping levels and abbreviated annealing steps in highly scaled technologies leads to thinner depletion layers, resulting in lower Photon Detection Probabilities (PDP) at longer wavelengths. Furthermore, a higher defect concentration in these technologies leads to a higher Dark Count Rates (DCR). These effects will be discussed in detail in Chapter 3.

1.4.2 Integrated SPAD Readout: Detection, Quenching and Reset

The SPAD is basically a photodiode whose pn junction is reverse biased above its breakdown voltage, such that a single photon incident on the active (i.e. photosensitive) device area can create an electron-hole pair and thus trigger an avalanche of secondary carriers. The avalanche build-up time is typically on the order of picoseconds, so that the associated change in voltage can be used to precisely measure the time of the photon arrival. This operation regime is known as the Geiger mode; hence, the devices are also known as Geiger-mode APDs. To prevent damage to the device, the self-sustaining avalanche in SPAD needs to be quickly stopped by reducing the bias voltage below the breakdown voltage, that is, the "quenching" phase. This is typically done using a series resistor, known as the quench resistor. After quenching, the voltage across the SPAD must be restored above the breakdown voltage before it can be triggered by another photon. During this dead time, the SPAD is nearly unresponsive, but its sensitivity gradually increases as it recharges, that is, the "reset" phase. A front-end discriminator, such as a single transistor or inverter, can convert the voltage change during a detection event into a digital signal, that is, the "Detection" phase. This signal, independent of the photon's wavelength, is compatible with standard electronics, enabling easy integration of SPADs into larger circuits and detector arrays. The timing of this process depends on the R-C time constant of the circuit formed by the series combination of the quench resistor and the SPAD junction capacitance. An active version of this quench-reset scheme is shown in Figure 1-12 (b), where we notice that the combination of reset and quench switches should direct the sensing and reset signal faster than the inherent RC time constant. In order for this detector to be utilized in a TCSPC apparatus, the active quenching-reset system should restore SPAD in active detection mode in a time less than 1/10th of the shortest fluorescence decay time [70]. Several architectures for integrated quenching/reset integrated circuits were proposed in literature, for example the work in [76] proposes a system 256 filterless SPAD pixels in two rows were used for in vivo neural activity monitoring, each pixel having an active quenching circuit that employs an avalanche detector, a timing logic, and an output stage for capturing counts. A discrete circuit version of this system is implemented in a custom designed Printed Circuit Board

(PCB) to interface with the integrated nanofluidic CMOS SPAD and will be introduced in Chapter 4 to validate the use of this particular detector in a TCSPC apparatus.

1.4.3 Integrated SPAD in a Time Correlated Apparatus: Special Consideration

TCSPC operates by recording the arrival times of individual photons relative to a synchronized excitation pulse, typically from a laser. This relies on the statistical accumulation of photon events over many excitation cycles to reconstruct the fluorescence decay profile. The pulse repetition rate is a key parameter that needs to be carefully selected based on the fluorescence lifetime of the sample and the recovery time of the detector. The repetition rate of the excitation pulse can be as low as 1 kHz or up to 100 MHz [70]. The characteristics of SPAD and the design of the active quenching circuit should carefully examine the selected repetition frequency. The recording of events occurs in a fraction of cycles to circumvent the photon pile-up phenomenon [77], which the readout circuit should be able to accommodate.

Most fluorescence spectroscopy experiments deploy optical filters to reject certain wavelengths, TCSPC is no exception; however, the CMOS nanofluidic platfrom does not have this capability as it will require further die processing to add optical filtering films. Electronic gating is deployed in some fluorescent detection platforms such as the 1 ns reject and collect gates on the Quantum-Si platform [69]. A discussion in [1] suggests that certain specifications for the integrated photodiode junction capacitance and space charge resistance could induce an electrical low-pass filter effect that attenuated the excitation pulse equivelent to optical density filter of order 6.4 rejection.

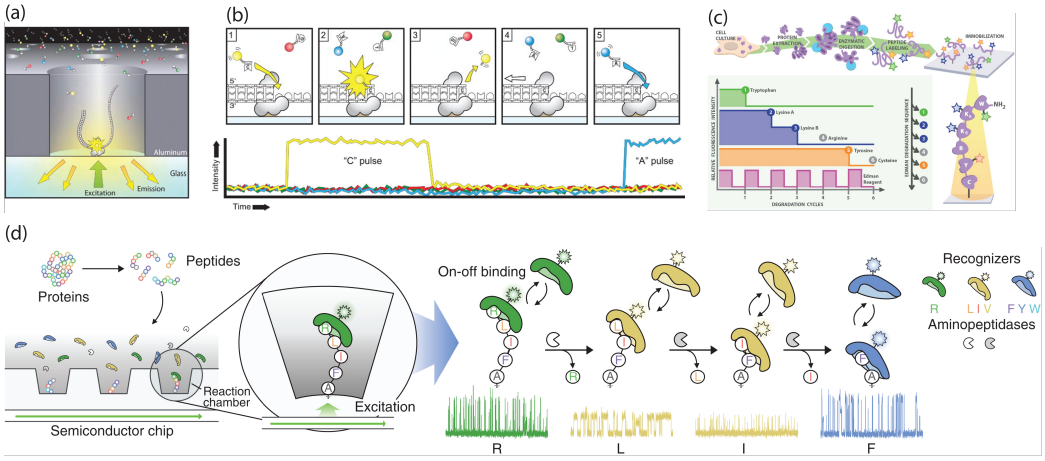


Figure 1-9: Examples of using fluorescence spectroscopy in biomolicule identification (a) Single-molecule, real-time DNA sequencing: The DNA is attached to a well acting as zero-mode waveguide illuminated from below to detect individual phospholinked nucleotide substrates (b) Cyclic forming of cognate association, flourescence detection, libration of die-linker ending flourescence pulse, polymerase translocation to next position and cognate associtaion of the next active binding cite [66] (c) a proposed scheme for single molecule peptide sequencing: Specific amino acids within these peptides are marked with fluorescent dyes (yellow for tyrosine, green for tryptophan, blue for lysine) and attached to a surface for imaging The peptides undergo Edman degradation where detected fluorescence dye is removed sequentially identifying the whole chain [78] (d) Implementation of dynamic protein sequencing in a semiconductor nanoscale reaction chambers: attaching peptide fragments inside and incubating with a mixture of freely diffusing NAA recognizers and aminopeptidases that carry out the sequencing process. The NAA is cleaved by an aminopeptidase The characteristic pulsing patterns is produced when these recognizers bind on and off [69].

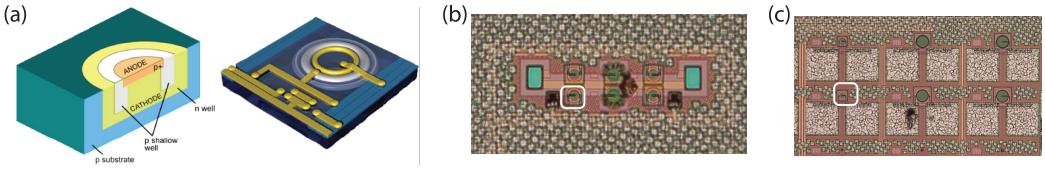


Figure 1-10: Integrated CMOS SPAD: (a) 3D illustration of CMOS SPAD detector both cross section and wiring [79] (b) Actual implementation of SPAD in the TC2 CMOS nanofluidic platform where the highlighted device is one of 6 detectors surrounding the nanochannel (c) Test detectors with different variations (diameter, doping, etc.) on the same die.

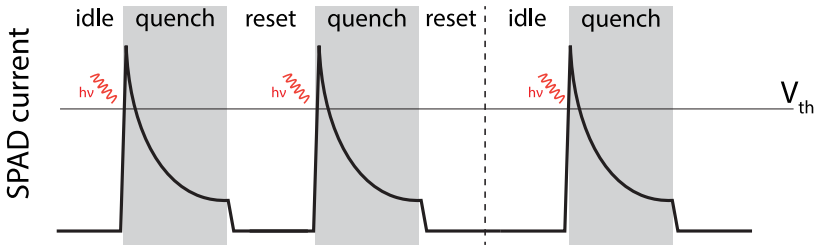


Figure 1-11: SPAD operation: Cycles of detection and reset

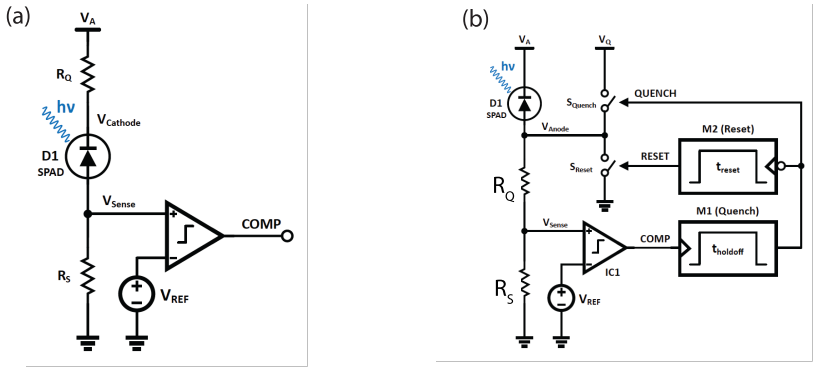


Figure 1-12: Top level diagram of SPAD interface circuitry: (a) Passive quenching circuit with a discriminator (b) Active Quenching and Reset topology adopted from [80].

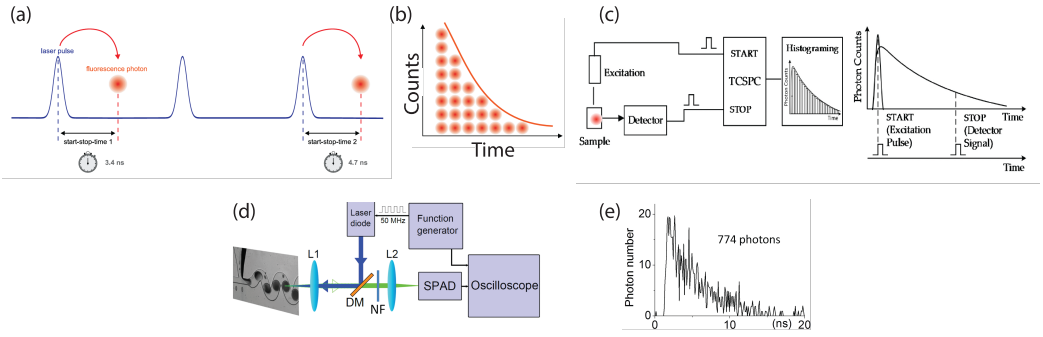


Figure 1-13: (a) Time Correlated Single Photon Counting Setup: Role of the detector which acts as a stop watch measuring the time of arrival of fluorescent photon at each cycle (b) A histogram created by pinning the photon arrival time which reflects the decay time of fluorophore die[77] (c) Schematic diagram of a TCSPC system highlighting the synchronization between excitation laser pulse and photon counting module[75] (d) Actual implementation of fluorescent labeled cell sorting system using microfluidic channel and (e) results of life time data by means of a TCSPC measurement [81]

1.5 Outlook, Strategies and Proposed Technique Positioning

Nanopore-based protein sequencing and sensing can be classified into three main strategies illustrated in Figure1-14 (a) [82]: (1) direct detection of the amino acid sequence of polypeptides by threading them through a nanopore, similar to nanopore DNA sequencing; (2) identification of proteins based on unique fingerprints without the need for de novo (that is, from the ground up) amino acid sequencing; and (3) identification of folded proteins by analyzing specific current patterns when the protein is inside the nanopore. Although the first strategy may seem appealing not only for single cell proteomic but also for the whole protein sequencing problem, it turns out that the size of the amino acid portion of the protein molecule is of lengths in all dimensions that are comparable to or smaller than the thickness of the pores, in addition to a variety of different charges that the protein possesses that are distributed unevenly throughout its structure [83]. However, there is potential that single cell proteomics will benefit from the development of single-molecule protein sensing technologies, including nanopore protein sequencing, which could provide higher sensitivity, inherent digital quantification through single-molecule counting, and better proteoform. The enthusiasm for nanopores comes from the fact that nanofabrication techniques can replicate it to achieve parallel identification, as shown conceptually in Figures 1-14(b)&(c). The success of adapting flow cell integration, Application Specific Integrated Circuitss (ASICs) and parallel processing is commercialized, and systems such as the one depicted in Figure 1-15 are used for sequencing DNA. The proposal of adding nanofluidics and integrated detectors is suitable for proteomics analysis as it significantly reduces the required analyte volumes and should, in theory, eliminate the need for molecule replication techniques such as Polymerase Chain Reaction (PCR) while increasing the sensitivity and efficiency of the assay. The remainder of this thesis will explore the integration scheme of these different modalities on a single silicon chip. Chapter 2 will cover the characterization process of the integrated amplifier designed for the reading of nanofluidic integrated nanopore. Chapter 3 covers the integrated SPADs characterization process and the effect of die post-processing to release the channels on the performance of those detectors. Chapter 4 introduces a discrete passive quenching active reset circuit designed to interface SPAD

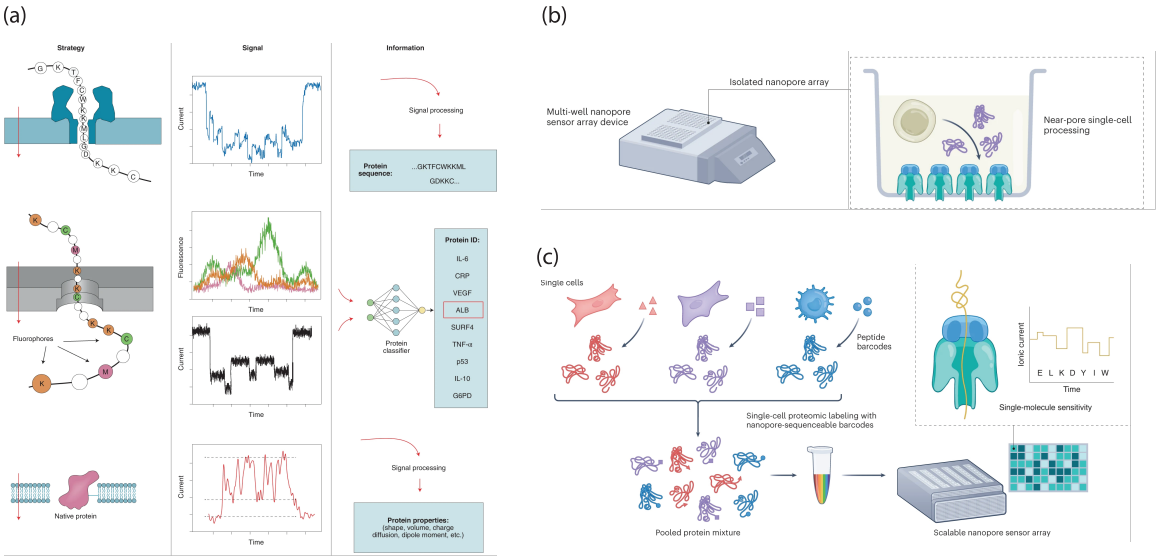


Figure 1-14: Nanopre based platforms: (a) sensing strategies (b) Parallel sensing using multiwell nanopore (c) Multiplexing results for pooled proteins mixture to achieve single cell proteomics. adopted from [6]

and reduce its reset time to optimize its performance such that it can be used in a TCSPC setup. Finally, we build upon these results of characterization and conclude what possible directions this platform can help in the real-time cell secretion monitoring problem.

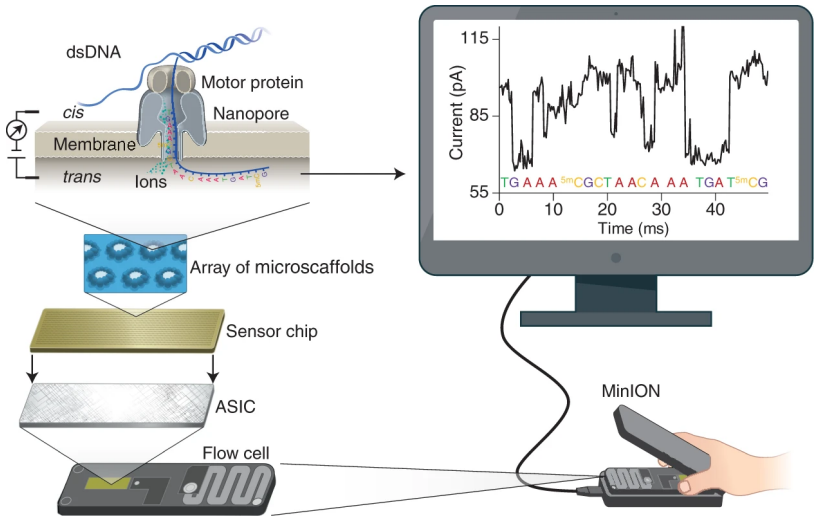


Figure 1-15: Top down nanopore integration with emphasis on multiplexing:A MinION flow cell contains 512 channels with 4 nanopores in each channel, for a total of 2,048 nanopores used to sequence DNA or RNA. The wells are inserted into an electrically resistant polymer membrane supported by an array of microscaffolds connected to a sensor chip. Each channel associates with a separate electrode in the sensor chip and is controlled and measured individually by the application-specific integration circuit (ASIC) at a rate of 450 bases/second. Illustration adopted from [44].

Chapter 2

Characterization of the proposed CMOS Nanopore Ionic Current ROIC

The use of the CMOS process to construct nanofluidic channels was established in Section 1.2. The channels were designed in a funnel fashion so that a nanochannel of the least dimension of the CMOS technology node emulates the function of a nanopore. Figure 1-4(a) shows the micrograph of the actual nanochannel on a Global Foundries 55nm silicon die that was post-processed and etched in MIT.nano. In the following discussion, the RPS sensing scheme in the CMOS nanofluidic platform is investigated to conclude the sensing limits of this specific technique with respect to the size and abundance of biomolecules. The relatively wide dimension of an unmodified CMOS nanopore (55nm×162nm×100nm cuboid) is expected to result in faster translocation (i.e., dwelling) times compared to conventional SSN made of a silicon nitride (SiN_X) membrane or a nanopore based on 2D material with an opening diameter of 1 nm. As a result, the conventional Axopatch ionic current amplifier setup with its limited bandwidth cannot capture such events. This chapter summarizes the efforts to design and characterize an amplifier that was integrated along side the nanopore using the CMOS process. Section 2.1 starts with summarizing previous work to develop the

co-design strategy that yielded specifications for an amplifier design by studying a simplified multiphysics model of a biomolecule in a nanopore [1]. Section 2.2 previews the efforts to characterize this amplifier by designing a testbench to characterize the amplifier and the subcircuitry to emulate the translocation event. Section 2.3 introduces the custom PCB designed to interface with the silicon die and the data obtained by this setup.

2.1 Overview of TC2 amplifier specification

The nanopore readout circuitry, whether integrated or discrete, is directly dependent on the electrohydrodynamics of biomolecules in the vicinity of the pore area [49]. This is understood qualitatively given the illustrations in Section 1-5, particularly the electric field lines depicted in inset (a) of the same figure highlighting the capture region. The co-design methodology proposed in [1] suggests the use of a simplified physics model and solves it numerically to understand the dynamics of the biomolecule translocation time. These calculations are later used to inform the integrated amplifier specifications necessary for an effective readout. This section summarizes the previous work on co-design the TC2 final design, and further, the impact of parasitics on the performance of this nanofluidic platform performance is previewed.

2.1.1 Multiphysics modeling of the CMOS nanopore

The difficulty in modeling a confined biomolecule surrounded by a carrier fluid lies in the nature of the molecules and their interaction with their carrier fluid. For example, interleukin-2 (IL-2) which is used in the expansion and activation of T cells during the manufacture of CAR-T cells has an isoelectric point of 6.6-7.0, which means that below this pH the IL-2 molecule would have a net positive charge, which naturally affects the translocation speed of this molecule if we were to pass it through the aforementioned nanopore. Another point to consider is the physical size that the molecule itself occupies which has a ramification not only on the translocation speed but also on the pulse shape in an RPS based sensor (Figure 1-5(f)). IL-2 is a 15.5 kDa 133 amino acid protein, based on the assumption that the spatial average of molecular density is 1.35 g/cm^3 [84] the IL-2 molecular volume[1] is approximately 2.64 nm^3.

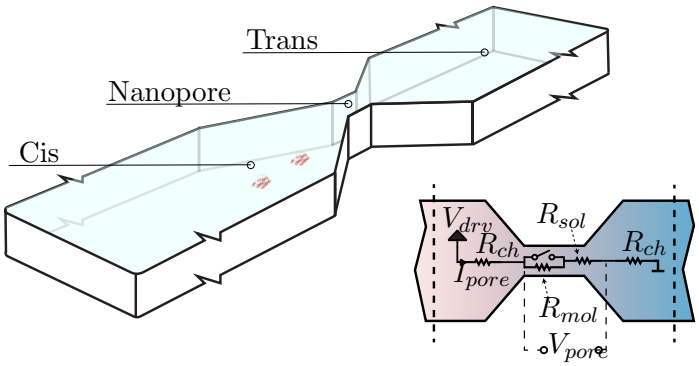
[1]The number of molecules is related to molecular weight (in kDa) through Avogadro's number. Furthermore, in [84] an argument is made that the protein molecular density does not show large variations as a function of molecular weight for proteins greater than 50 KDa

The translocation of biomolecules through CMOS nanopores involves complex interactions with the carrier fluid, dependent on the properties of the biomolecules (e.g. charge and size) and the physical characteristics of the nanopore. Mathematical models, including Poisson's equation for electric fields, Navier-Stokes for fluid flow, and Nernst-Planck for ion mass transport, describe these interactions. This model is referred to in the literature as Navier Stokes-Poisson Nernst Planck (NS-PNP) and can be solved numerically using FEM tools such as Comsol Multiphysics [85] to provide estimates for translocation times and ionic currents. An example of validating these numerical solutions versus experimental measurement of ionic current can be found in [86] where the authors modeled the Bovine Serum Albumin (BSA) biomolecule as a non-conductive volume that displaces the conductive fluid to estimate its traversal current blockage effect through a 16-nm diameter and 10-nm thick pore. The Comsol model predicts a 3.48 nA of ion current in contrast to measured 7.40 nA for a drive voltage of 0.12V and a KCL filled domain, for the translocation event, the simulation predicts a current drop of 66.1 pA versus 50.0 pA measured experimentally. In the same model, another simulation was performed that adopts the dimensions of the CMOS nanofluidic channels to numerically solve NS-PNP equations for the geometry shown in Figure 2-1 that maps the nanofluidic system in TC2 with two main objectives: (i) build a lumped element circuit model for the nanofluidic channel to use it in the integrated readout amplifier design, and (ii) estimate the time of translocation of a certain biomolecule through the relatively long nanopore to set a criteria on the integrated amplifier bandwidth [1]. For the first objective, the ionic current density was calculated for an empty and filled nanopore. The equivalent circuit in Figure 2-1(a) is deduced based on the values where R_{ch} represents the ratio of drive voltage to ionic current in that part of the system, similarly R_{sol} reflects the same value for fluid volume in the nanopore region, finally, R_{mol} is the component that is added to the system to reflect the current drop that occurs when a blockade event takes place, such as the one seen in Figure 1-5(c).

The values of the equivalent circuit components for CMOS nanopores are listed in Table 2.1. Intuitively, the switch in the circuit model emulates the translocation time when it opens for t_{tr} seconds. The particle tracking utility in Comsol's Nernst-Planck-Poisson

Simulation Parameters	Value
Nanopore Geometry	55 nm-wide, 100 nm-high, 162 nm-long cuboid
Access channels	10 μm-wide, 0.1 μm-high, 100 μm long cuboid
Sense electrode spacing	162 nm
Wall material	silicon nitride

Table 2.1: Comsol parameters used in Finite Element Method (FEM) simulation



(a)

Parameter	Value
	$V_{drv} = 120mV$
R_{mol}	3.15 MΩ
R_{sol}	1.47 MΩ
R_{ch}	6.39 MΩ

(b)

Figure 2-1: Comsol model of CMOS nanofluidic platform: (a) Geometry of the simulated nanopore with access channels and equivalent circuit parameters derive from the FEM solver (b) Summary of deduced values of nanopore model based on the solver results

Equations interface, the two main forces that affect particles, namely the electrophoretic force $\vec{F_e}$ and the drag force $\vec{F_d}$ for the ion species i, are calculated and the particle's translocation velocity was deduced, at which point we have an estimate for translocation rate of molecules within this geometry for BSA molecule where caalculations show that at drive voltage of 0.12 V the translocation time is 160 μsec.

2.1.2 Signal integrity in CMOS nanopore

The phenomenon of ion transport in a nanopore system is coupled to two types of capacitance, an inherent capacitance resulting from the accumulation of counterions in a biased electrolyte, and the other is the parasitic capacitance that emerges between the electrodes. It is imperative to address each type of capacitance and incorporate it into the circuit model in Figure 2-1 if we were to infer the specifications of the readout amplifier based on that model, since that capacitance will define the system time constant, translating into a

limitation on the fastest translocation event the system can resolve. Figure 2-2(a) shows a pictorial summary of different layers of ions that form as a result of an electrical bias in the fluid. Considering the placement of electrodes with respect to the nanopore, we can argue qualitatively that the dominant capacitance from the electrical double layer is equivalent to a series capacitance with respect to the pore resistance. However, the parasitic capacitance shown in Figure 2-2(b),(c) creates a path to the ground. This qualitative reasoning is important to interpret the impedance computation using Comsol and impedance measurements using instruments such as the LCR meter to extract an accurate circuit model for the nanopore. Double layer capacitance values can be analytically estimated by calculating the Debye length, which is a function of the ion concentration [87]. Similarly, empirical models are adopted to estimate the capacitance of the pad [88] based on the geometry and dimensions listed in Table 2.2. Ultimately, the setup in Figure 2-4(a) was built to measure the impedance of an empty and fluid-loaded nanopore. The solution used is a 1 M KCl solution prepared by dissolving KCl salt weighed accordingly in 10 mL of DI water and loaded following the procedure in [1], where it was passed through a 0.2 μm filter and then micro-pipetted onto the chip surface. Figure 2-3 illustrates the fluid loading sequence by capillary forces, indicating that this method requires a hold time of around 10 seconds and an additional time for complete evaporation from the chip surface at room temperature that takes about 3 minutes leaving only the liquid in the nanochannels, thus ensuring no parallel electrical path through the fluid on the surface of the chip and providing ample time for impedance measurements. HP 4285A precision LCR meter was deployed with four prope measurement covering the frequency band from 75 kHz to 20 MHz. The calibration of the LCR meter was performed using both open-circuit correction and short-circuit correction, where a standard gold-plated contact substrate was used to short the probes[2]. The calibration takes into account the length of coaxial cables (3 ft) connecting the instrument terminal to the probe needles to ensure accuracy. Figure 2-4(b), (c) shows the results of the measurements comparing them to the Comsol results, where good agreement between the model and the measurements is observed for the magnitude measurements and the discrep-

[2]The contact substrate is a PCB provided by Cascade Microtech (P/N: 005-018) used with the HP 4285A instrument for short circuit calibration and can be replaced by any metallic element that is guaranteed to exhibit short circuit behavior in the frequency range of interest.

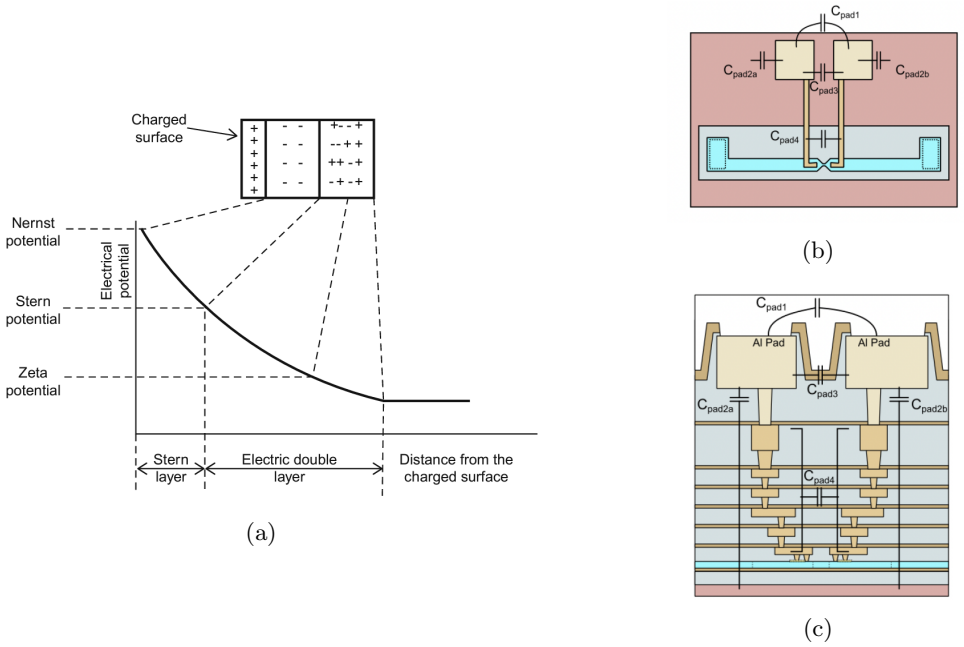


Figure 2-2: Two sources of equivalent capacitance in CMOS nanopore (a) Electrostatic forces near a charged surface, ions tend to be highly organized close to the charging boundary. The second layer, termed the electric double layer, has ions less organized but still introduces a capacitance effect that we incorporate into the amplifier design adopted from [89]. (b) Parasitic capacitance emerging from aluminum traces in proximity, top view (c) Cross section of the TC2 stack showing the parasitic capacitance across the vias [1].

ancy in the phase measurements beyond 1 MHz, which is attributed to the emergence of more parasitic between prope and pads at higher frequencies. Table 2.3 summarizes the parameters extracted based on LCR measurements where C_{dl} and C_{pad} are in good agreement, R_{pore} however shows a disagreement that may be reasoned to the effect of the conductive fluid on the capacitance of the double layer that leads to the thinning of the double layer and inhibiting the electoosmotic transport; hence, an equivalent higher pore resistance is observed. The fact that the chemical transport module in Comsol Multiphysics does not model ohmic properties of the fluid by imposing electric insulation boundary condition on the simulated domain supports this reasoning.

Parameter	Value
W_{pad}	80 μm
L_{pad}	80 μm
t_{pad}	3 μm
d_{pad}	20 μm
L_{trace}: trace length from pad to nanopore	30 μm
t_{trace}: the thickness of metal trace	2 μm
d_{trace}: the normal distance between two trace pairs	10 μm

Table 2.2: Dimensions of Aluminum pads fabricated on the BEOL of BCD process used in parasitic extraction

Nanochnnel State	Parameter	Comsol result	LCR measurement
Empty	C_{pad} (fF)	30.4	32.2
KCL Filled	C_{dl} (fF)	15.3	11.3
KCL Filled	R_{pore} (MΩ)	0.452	1.17

Table 2.3: Nanopore equivalent circuit parameters: Comsol Simulations vs. LCR measurements

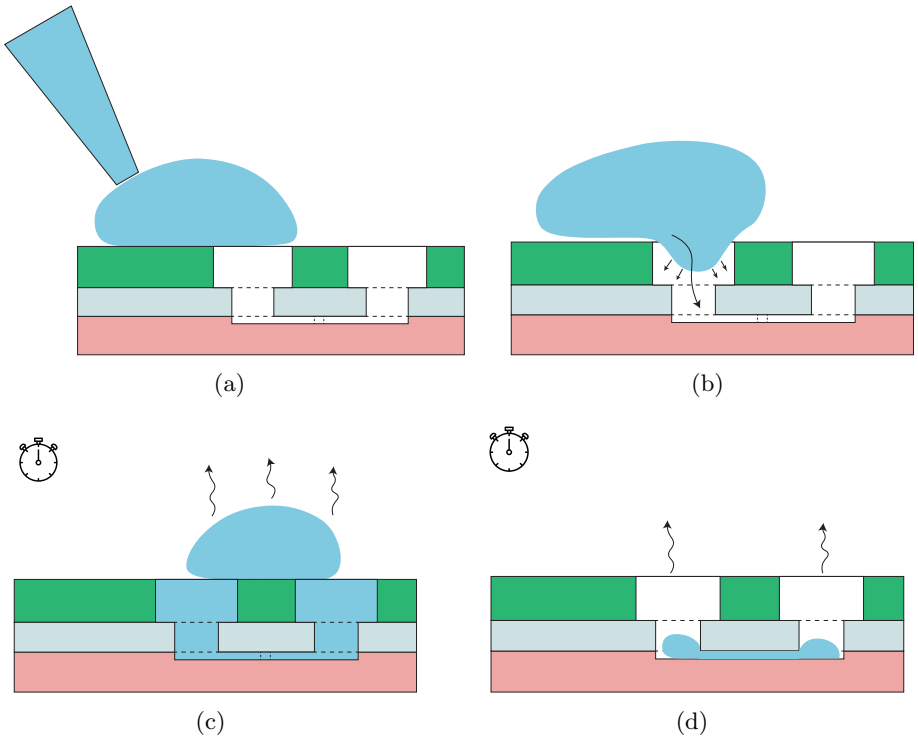


Figure 2-3: Nanochannel loading sequence (a) Micropipetted liqued is landed on the chip surface, which is the SU-8 layer (b) Capillary forces pull the lequid to the micro channels (c) The liquid filles the channel after waiting time of approximately 3 minutes the liquid on the chip surface is totally evaporated (d) 0 seconds later, the liquid inside nanochannel evaporates, the LCR reading is acquired before that time passes

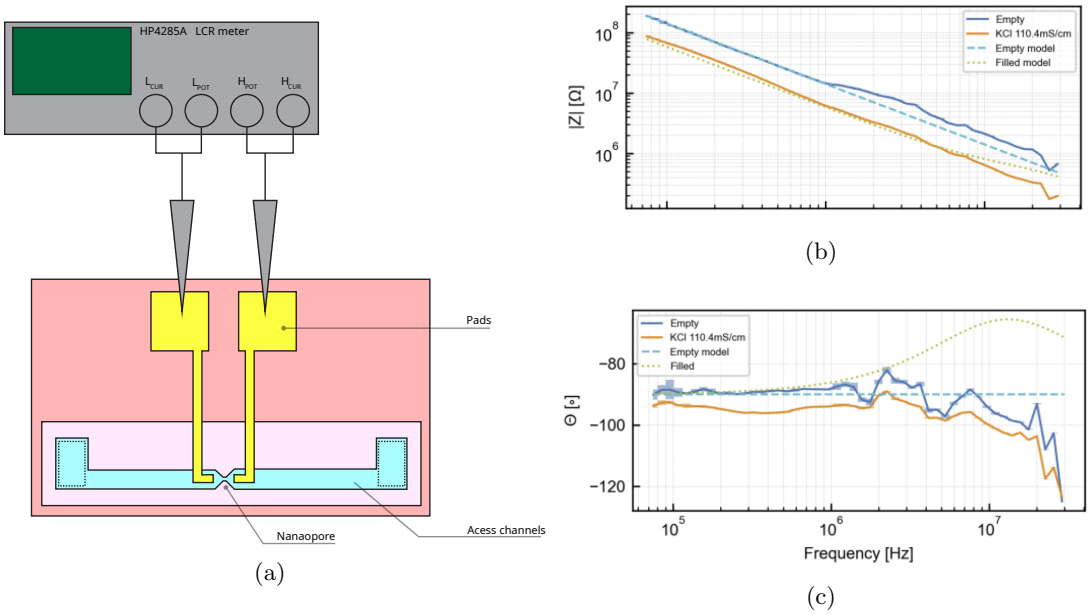


Figure 2-4: Nanopore circuit parameter extraction setup (a) Schematic of LCR meter connections to the nanopore (b) LCR measurements frequency sweep for impedance magnitude and phase

2.1.3 Putting all together: From multiphysics modeling to amplifier specification

We now combine two pieces of information from Section 2.1.1 where the translocation time for BSA molecule is 160 μsec together with the circuit model deduced in Section 2.1.2, the equivalent circuit of the nanopore that incorporates two capacitors is depicted in Figure 2-5 (a), and part (b) of the same figure shows how this equivalent circuit is connected to a read-out amplifier. Figure 2-5 shows the circuit model for the nanopore system. The switch represents a translocation event when opened and the objective is to see how that would translate at the input amplifier. The arrangement of sense and drive electrodes, as shown in the schematic, allows frequency modulation of the drive signal to boost noise performance. This concept is tested in the nanopore emulation circuit added to the amplifier testbench.

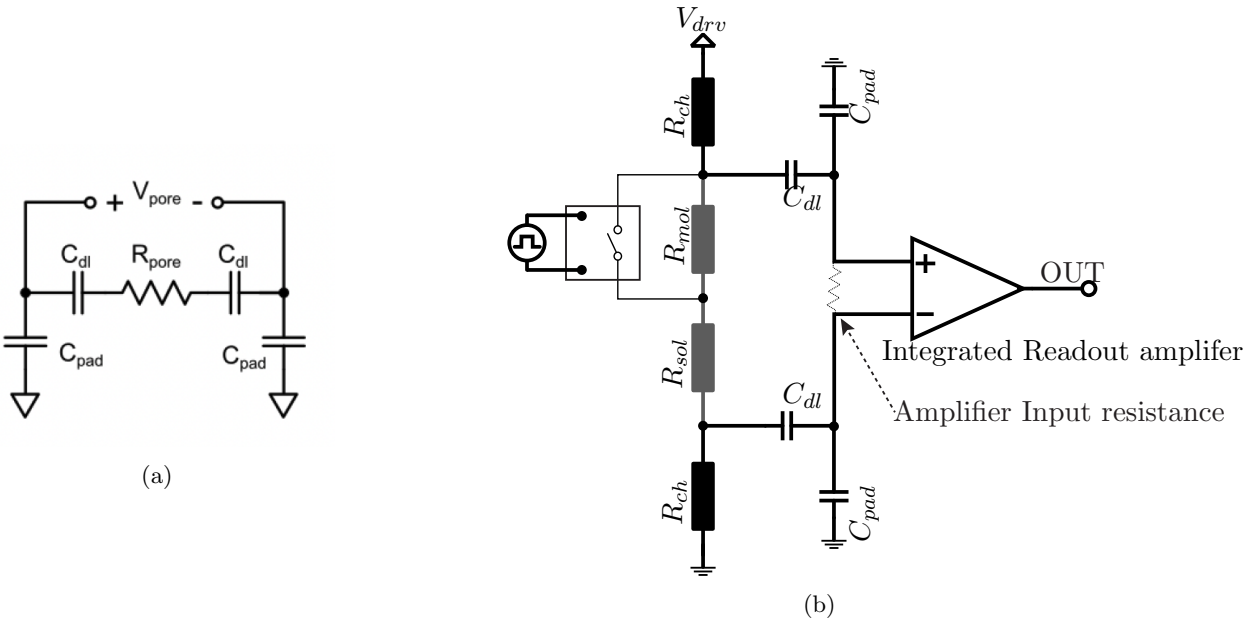
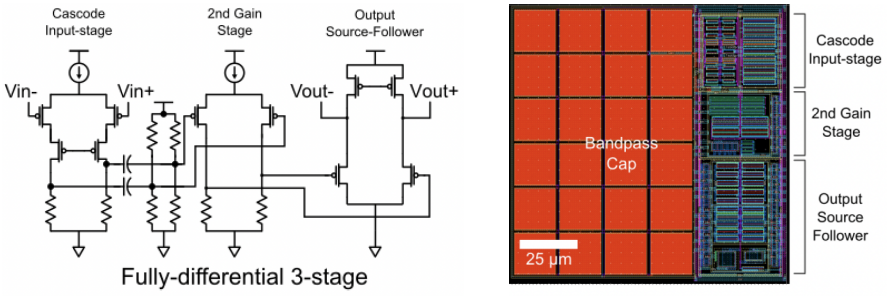


Figure 2-5: The CMOS nanofluidic physics informed circuit model (a) The nanopore model where the double layer capacitance and parasitic pad capacitance are added (b) The nanopore model is connected to the fluid access channel equivelent resistance and the readout amplifier, a switch is added to model the translocation event.

2.1.4 The integrated readout amplifier

A three stage fully differential amplifier was designed and integrated with the nanofluidic channel [1]. The topology shown in Figure 2-6 comprises input PMOS transistors to improve flicker noise performance with a cascoded gain stage to avoid Miller effect. The second stage is used to boost the gain while maintaining the same 1 MHz bandwidth. The biasing of this stage was set by passive load, which is not ideal for power consumption, ultimately it maximized the output range. This biasing adds to the power budget of the circuit, which is not the limiting factor for this application at the prototyping stage. Finally, a source follower output stage is added, which enables the amplifier to drive a capacitive load up to 15 pF while maintaining the same gain characteristics and isolating the nanochannel ionic current from the readout utility (such as digital acquisition systems). In contrast to conventional ion channel readout amplifiers which often deploy a TIA to funnel the ionic current through a resistance converting it to voltage while fixing the drive voltage, this setup decouples the drive voltage from the sensing ports by virtue of electrodes arrangement (Figure 2-2(b))



(a) (b)

Figure 2-6: TC2 integrated amplifier (a) Schematic (b) Layout adopted from [1]

Parameter	Value
Supply	2.5 V
Gain (V/V)	70.4
Open loop 3-dB Bandwidth	0.12-9.52 MHz
Input referred Noise (simulated)	2.70 μV_{rms}
Input Common Mode Range (V)	0.2 - 1.5 V
Output Common Mode Range	0.9 - 2.4 V
Output differential Mode Range	-0.7 - 0.7 V
Power (mW)	2.87 mW
Die Area (mm^2)	120 $\times$ 118 μm^2

Table 2.4: TC2 amplifier specification

which also allows experiments such as lock-in detection. Another important aspect of this architecture is reflected in the noise contribution in comparison to the anticipated noise generated by the nanopore. To get a sense of this ratio, the thermal noise floor of the nanopore can be estimated by plugging the resistance value (Table 2.3) into the Johnson noise equation previewed earlier in Section 1.3.3. [64] which results in 118 μV_{rms} of noise at 1 MHz bandwidth compared to the simulated value of 2.87 μV_{rms} of the amplifier, therefore an approximate estimate of the contribution of the amplifier with properties listed in Table 2.4 to the system noise is 0.1%.

2.2 Testbench design and simulation

Verification of integrated amplifier functionality and readout requires a careful design of test bench circuitry that interrogates the amplifier specification and verifies whether it matches the simulation results of Cadence Virtuoso as specified in Table 2.4. The following section provides details of the test bench circuitry used for the TC2 integrated amplifier, which was designed to ensure the provisioning of the external current source that biases the input and gain stages and the injection of a differential tone to characterize the gain and bandwidth of the amplifier. In addition, the test bench has a discrete amplifier to probe the nanopore electrodes, i.e. the biomolecule translocation input signal to the amplifier, to get a sense of the actual signal and isolate the effect of the integrated amplifier specifically, the distortion resulting from its frequency response shape. Indeed, it should be taken into account that nanopore probing pads will add pad capacitance as discussed in Section 2.1.2 however, with the calculations discussed in the same section the effect of the amplifier can be decoupled and compared to another off-shelf amplifier to verify its operation. In addition, the test bench has a sub-circuit that provides an emulation to the translocation action by means of a discrete transistor switch that is controlled by an external trigger with a timing set to expected translocation duration and resistors of values deduced from the Comsol simulation that were previously viewed in Section 2.1.3 for the purpose of further validating the nanopore modeling methodology. Figure 2-8(a) shows the main blocks of the test bench and how they connect to the TC2 die and its nanofluidic compartment. The remainder of this section elaborates on the specification of components used to build the test bench.

2.2.1 DC Biasing of the TC2 amplifier

Two biasing DC voltages are produced by discrete low dropout voltage regulators, the NCV4276B from On-Semi provides 2.5 V at 400mA to power the TC2 amplifier and other discrete amplifiers on board. The choice for this package was based on its moderate power supply rejection ratio of 70 dB and relatively low load regulation of 3 mV at a load of 5 mA. Another 1.25 V regulator was needed for signal leveling and DC biasing of the nanochannel,

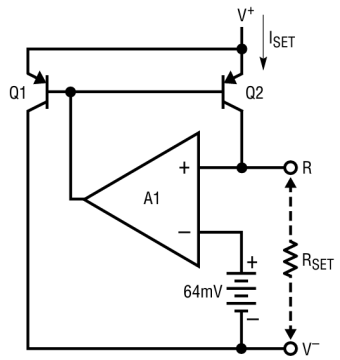


Figure 2-7: LM134 external current source schematic, adapted from Analog Devices datasheets website

especially for the lock-in detection scheme. For that purpose, another Low Dropout (LDO) regulator was cascaded, Analog Devices ADP163 and configured to provide this specific bias voltage. The APD163 chip has less load regulation which can be tolerated given that its fed from the NCV4276B. In addition, ADP163 is adjusted by a pair of resistors connected to the feedback pin. This choice is used to compensate for the variance and drift of other components and always ensure the bias value before performing any experiment.

The integrated TC2 amplifier was designed to be externally biased, and the pair of current sources depicted in the first two stages in Figure 2-6 should be provided externally. For that purpose, Analog Devices LM134 is used as a bias current source, a chip for each stage. To understand how this external chip works, Figure 2-7 from its data sheet shows a basic block diagram for its operation where a reference voltage is internally provided to an operational amplifier that drives a 1: 17 current mirror, the voltage set on the resistor will always be fixed by the feedback action of the internal chip operational amplifier so that the current is totally controlled by the set resistor in an ohmic fashion. In the testbench design, a variable resistor is connected to the LM134 to allow for varying the bias current from 10 to 200 μA to allow quantification and control of amplifier parameters such as the transcendence of each stage.

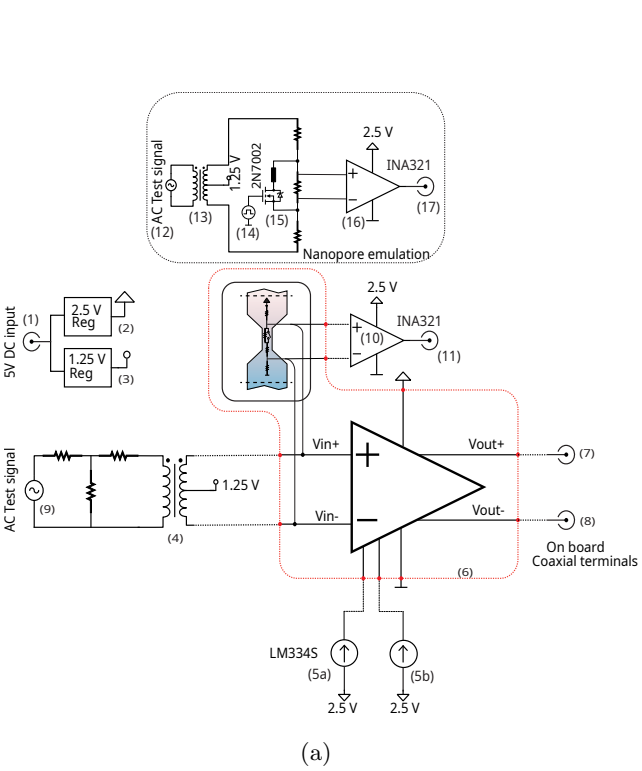
2.2.2 AC charcterization of TC2 amplifier

To characterize the differential AC gain of the amplifier, two out-of-phase sinusoidal tones are produced using the transformer configuration shown in Figure 2-8(a). The center tapped transformer provides a DC level shift of 1.25 V to maintain the DC bias (above threshold operation) for the first stage of the integrated amplifier. The resistive network provides 1:50 attenuation, a common technique used for sub 100 mV test signal generation to avoid unaccommodating cable attenuation. The resistors were chosen so that it maintains the 50 ohm input impedance. The transformer used is TT1-6-KK81 from Mini-Circuits, which has a small surface mount footprint for reduced stray capacitance and $\approx$ 0.1 dB insertion loss around 1 MHz.

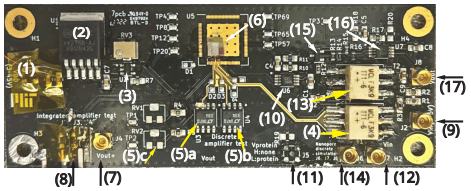
In the design of TC2 chip, the sensing electrodes were brought closely to the integrated amplifier for the reasons discussed in Sections 1.3.3 and 2.1.2. However, two metal routes were added to give direct access to the nanochhannel and bypass the integrated amplifier for debugging purposes. For that reason, an external instrumentation amplifier was added to the testbench. The Texas Instruments INA321 was chosen to probe these signals for its low offset voltage ($\pm 200\mu V$) and input referred noise of $20\mu V_{pp}$ although it has a bandwidth of 500 KHz, the advantages outweighed this aspect for initial debugging. Two external resistors of values $190K\Omega$ and $10K\Omega$ are used to fix the gain to 20 V/V. A 0.1 μF capacitance is added in the feedback path to tune the frequency response, in terms of frequency response, this capacitor adds a zero centered at 100 KHz so that the gain profile of this circuitry is shaped as a band bass filter, similar to that of the TC2 amplifier. The frequency response of this circuitry is shown in Figure 2-9(b). It is worth noting that this amplifier is single-ended in contrast to the TC2 integrated amplifier that was designed to be differential-ended.

2.2.3 Emulation of Nanopore Translocation

A nanopore emulation circuit was attached to the test bench, which is not connected to any of the other blocks discussed above. Figure 2-9(a) expands on this subcircuit that



(a)



(b)

1. Coaxial DC input to regulators
2. NCV4276B: 2.5 V regulator
3. APD163: 1.25 V regulator
4. TT1-6-KK81 Center tapped transformer
5. (a), (b) LM334S current generator, (c) control resistor
6. The TC2 wire-bonded chip
7. Coaxial termination of TC2 non-inverting output
8. Coaxial termination of TC2 inverting output
9. AC input to test TC2 amplifier
10. INA321 external opamp: to TC2
11. Coaxial termination - output of (10)
12. AC input to nanopore emulation circuit
13. TT1-6-KK81 Center tapped transformer
14. coaxial to external pulsed sourse
15. 2N7002 nmos transistor
16. INA321 external opamp: Nanopore emulation
17. Nanopore emulation circuit output termination

Figure 2-8: Schematic diagram showing high level blocks of the testbench and its connectivity to the the integrated TC2 chip with its nanopore. The blocks in red perimeter are on the TC2 die, connected to other blocks by means of wire bonding, as shown in Figure 2-10(b)

comprises discrete resistors equal in value to those deduced from the Comsol ion transport model discussed in Section 2.1.1. A transistor switch was implemented to connect extra resistance when switched on, in an action similar to moelcule translocation from circuits prespective of resistive pulse shaping transduction. This switching action is triggered by an external signal source that provides the $V_{control}$ signal with a temporal width equal to the expected translocation time of the molecule. The On-Semi 2N7002 was chosen for its 10 nsec turn on/off times, which is four orders of magnitude less than the time scale of molecule translocation estimated by the same Comsol model. The DC drive voltage used typically used to thread molecules through the nanopore by electrophoretic action is emulated using a DC supply of 1.25 V and the AC drive is split into balanced form by aid of another TT1-6-KK81 transformer. Similarly to the case of the actual nanopore, the emulation circuit is followed by an INA321 instrumentation amplifier to probe the signal across R_{pore}. This kind of configuration completes the cross-validation needed for this platform. Figure 2-9(c) depicts the PSPICE simulation results for translocation events and AC modulation at 1 MHZ, which is the tone proposed for optimal SNR translocation locked mode detection [1].

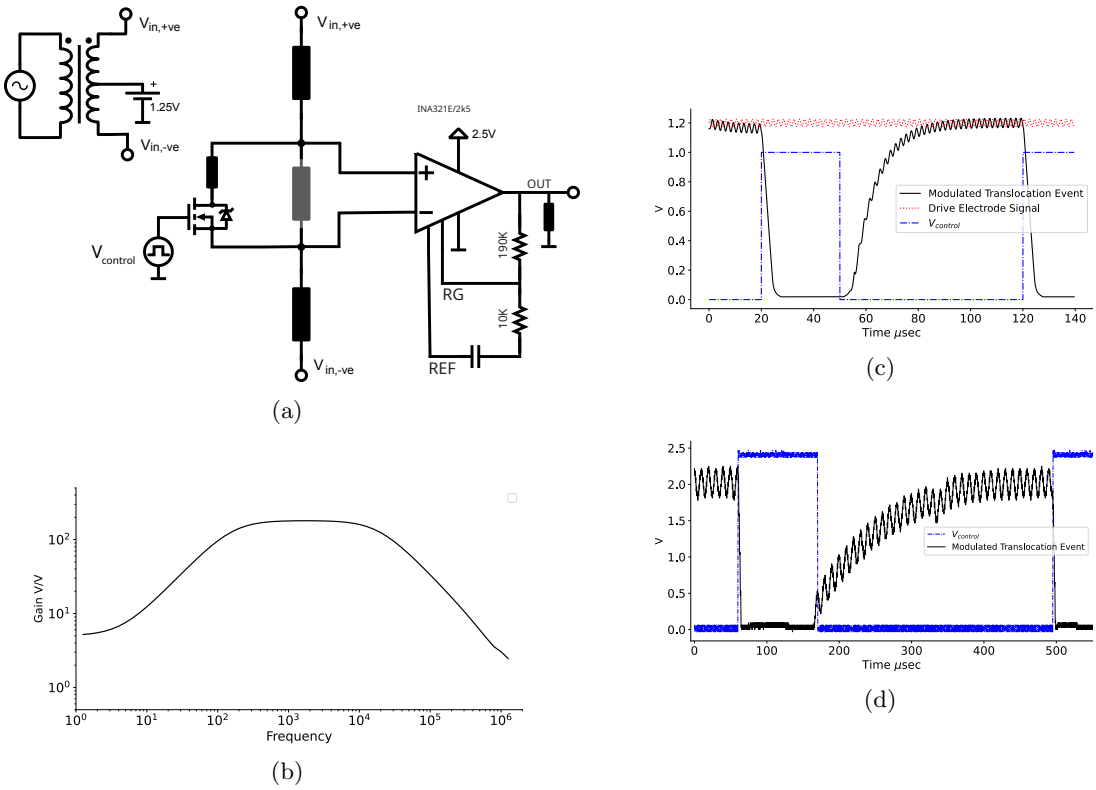
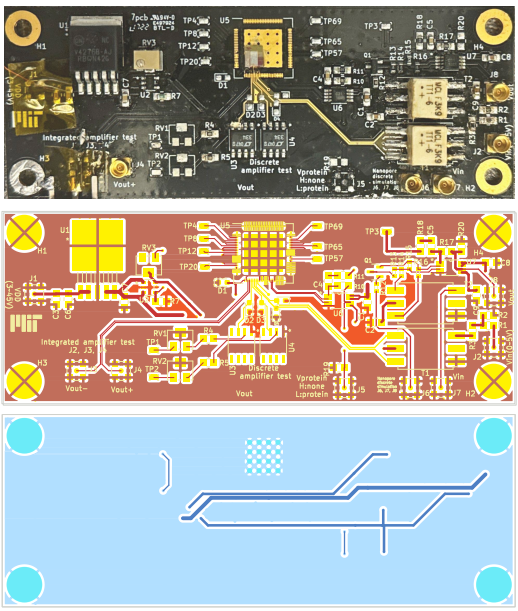
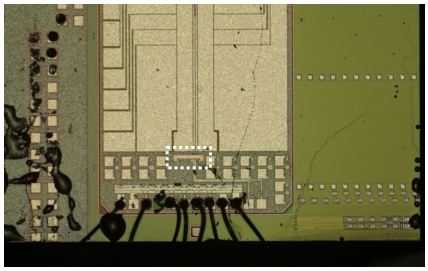


Figure 2-9: Proposed circuit for emulation of translocation event (a) schematic diagram showing the feedback network that ensures a mid band gain of 100 V/V and low frequency zero at 100Hz so that the frequency response exhibits a band pass behaviour. (b)The PSPICE simulation of the amplifier frequency response (c) PSPICE simulation results showing drive signal modulation where the translocation event is differentiated from other drive signal by having near zero modulation depth[4] (d) Oscilloscope traces of the INA321 output and $V_{control}$ in the actual implemented subcircuit in Figure 2-10



(a)



(b)

(c)

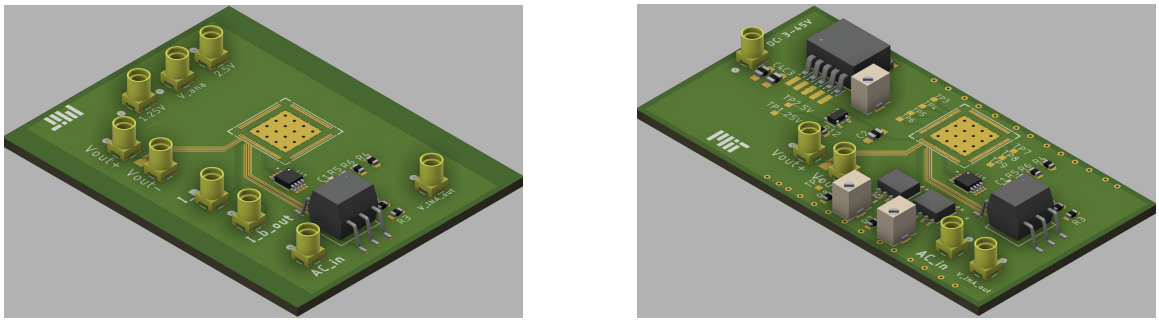
Figure 2-10: Testbench PCB (a) Top: Fabricated PCB with wireponded TC2 chip, middle: the layout of top layer with emphasis on surface mount pads, bottom: the layout of bottom layer of the PCB which is mostly a grounded plan except for the dark blue traces that are DC supply line (b) Wire bonding from chip side (c) Wire bonding pads on the PCB side: the pads on PCB were manufactured with the gold immersion finish to ensure compatibility with gold wire bonds commonly used

2.3 Printed Circuit Board Design & Characterization Experiment

A custom board was designed and fabricated to relize the proposed schematic in Figure 2-8(a). Several iterations were made to converge to a final design that fits all components for both the testbench and nanopore emulation circuits, preserving a size that would fit later into the wire bonding machine. Figure 2-10 highlights the traces on both the top and bottom sides of the two-layer PCB. Note that the design maintains differential signal lines to and out of the die at the same length. A Chip On Board (COB) scheme is implemented where the bare chip is bonded directly to the PCB. Figures 2-10 (b), (c) show a microscope image of the die after bonding. This approach offers several benefits for our case where direct access to the nanochannels and SPADs is a must.

2.3.1 PCB Design Iterations

While the design process went through several iterations, three design trials capture the highlights of the design flow until it converged to the last design. Figure 2-11(a) captures the first trial, which basically provides a large grounded pad where the TC2 die will be glued and a 96 large pad for wire bonding. The chosen dimension of the PCB wire bonding pad is 250 $\mu m \times 750\ \mu m$ with a spacing of 100 μm squarely placed around the perimeter of the grounded pad. It was important to assign the PCB pads that will be routed to the rest of the components in the same order as they were on the TC2 die to avoid bridging the wire bond. This trial also included BNC connectors for DC bias voltages, two terminals externally connected to an external LM334S-based bias current generator, and a bias network that generates two out-of-phase signals from a single-ended AC test input and DC couples it to 1.25 V; this is the transformer network labeled (4) and (9) in Figure 2-8(a). Additionally, the instrumentation amplifier INA321E was added to externally probe the nanopore signal pads. The second iteration in Figure 2-11(b) adds a couple of LDOs (2.5 V NCV4276B and 1.25 V APD163) to generate the bias voltages on board. At the time of the design the current consumption of the TC2 amplifier was debugged using the GS probe, where a layout short was detected and corrected using the FIB fix provided by external supplier. Since current consumption is known and no external supply is needed to track it, the PCB was modified to include those LDOs to simplify the setup around the board, and current generator chips (the LM334S) were added. Notice also that the large grounded pad was shifted to the edge of the board for convenience of a wire bonding machine with some external test points for generic use. The final design implemented and shown in Figure 2-10(a) adds to the previous trial the nanopore emulation circuitry with its own external INA321E amplifier, while the emulation circuit shares DC bias with the rest of the circuit, it has its own AC single to differential converter network to aid with separate lock-in measurements. This subcircuit implements the schematic in Figure 2-9(a) with resistor values similar to those extracted from the Comsol Multiphysics model in Figure 2-1(b).



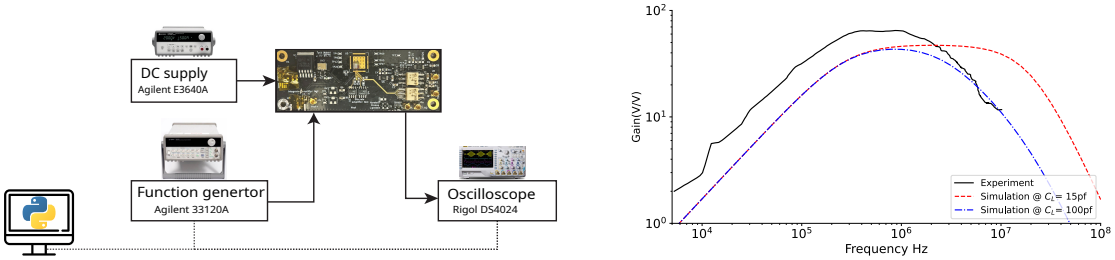
(a) (b)

Figure 2-11: 3D rendering of TC2 amplifier PCB trials (a) First trial which has a large grounded break out pad, differential signal generator and external instrumentation amplifer (b) Second trial that incorporated DC bias LDOs and bias current generator

2.3.2 TC2 amplifier characterization setup

Figure 2-12(a) shows a schematic diagram of the amplifier characterization setup. The circuit is powered using a single 5 V supply, as the regulators on the testbench take care of generating all required biasing voltages. An arbitrary function generator was used to generate a 1 V sinusoidal signal that will be attenuated on board and injected into the amplifier. A 200 MHz bandwidth oscilloscope is used to monitor the output. Both the function generator and the oscilloscope are connected to a computer through GPIB and USB cables, respectively, for experiment control and data acquisition. After switching on the power supply, a tuning step is required for the LM134 external resistors that, in turn, adjusts the bias current of the integrated amplifier as discussed in Section 2.2.1. The tuning happens visually by looking at the scope screen while rotating the knob of the resistor on the PCB until gain is maximized for a 100 KHz test signal.

A Python script was implemented to sweep the frequency output of the signal generator from 5 kHz to 10 MHz. The script also acquires data from oscilloscope which probes both input and output signal to the amplifier; these data are used to compute both gain and phase difference between input and output of the amplifier. Python scikit-learn library was used to process the phase information by means of a correlation function. Figure 2-12(b) depectis the result of this experiment and compares it with the cadence simulation results.



(a) (b)

Figure 2-12: TC2 amplifier characterization (a) Setup block diagram (b) Measurment results compared to Cadence simulation results with different load capacitance.

Ref.	Bandwidth	Noise	power	Gain
This work	9.52 MHz	2.7 pA_{rms}[5]	2.87 mW	70.4 V/V
[46]	0.5 MHz	20.4 pA_{rms}	20 mW	50 MΩ
[62]	1 MHz	24 pA_{rms}	5 mW	50 MΩ
Axopatch 200B [59]	0.1 MHz	9 pA_{rms}[6]	-	500 MΩ

Table 2.5: TC2 integrated amplifier compared to literature

Excellent agreement is exhibited up until the first pole, which occurs at 200 KHz. The second pole occurs at 1 MHz contradictory to 10 MHz simulated in cadence. This can be reasoned for the fact that Cadence simulation did not consider the stray capacitance of the wirebonding and low quality coaxial cables used. Another reason is that the gain is about 2x higher than simulated. Changing the load capacitance in the Cadence testbench to 100 pF results in a matched second pole. The result is still promising for the context of capturing translocation events in the microsecond range.

[5] for 1 MΩ of channel resistance

[6] According to [62] this value is extrapolated to 247 pA_{rms} to be compared for the same 1 MHz bandwidth

2.4 Conclusion

The performance of the TC2 amplifier is compared with similar integrated nanopore sensing amplifiers and the standard Axopatch 200B amplifier (Table 2.5). Although there is a wide spectrum of amplifiers targeted for ionic channel sensing, the amplifiers chosen for comparison are the closest scheme of nanopore integration to the TC2 platform. The TC2 amplifier is exceptionally well suited for sensing applications in CMOS nanofluidic platforms due to its bandwidth and noise performance. With a gain of 70.4 V/V, the TC2 amplifier ensures sufficient signal amplification to detect biomolecular events in a RPS scheme as it supports the high-frequency requirements needed to capture rapid transient signals often encountered in nanopore sensing. The simulated input-referred noise of 2.70 µVrms is particularly low, ensuring a correct read out for small signal fluctuations that is not possible with other sensing platforms, which is crucial for accurate detection and analysis in biosensing applications. Furthermore, the energy consumption, which is not optimized in this design, compares favorably with that of other amplifiers, making it good for development of other versions that integrate into portable or battery-powered sensing devices. Together, these specifications meet the stringent requirements of high-sensitivity and high-throughput nanopore sensing, ensuring reliable performance in the detection and analysis of single biomolecules.

This chapter summarized the TC2 chip design effort in [1] combining input from multi-physics modeling and geometry constraints of BCD55 technology. After the fluidic nanochannel was released, an electrical characterization was performed. A PCB was designed and fabricated to interface the chip via a COB scheme. Wire bonding was performed successfully and a setup was built around the PCB to characterize the amplifier. A performance match between results and simulation was concluded; however, the PCB design did not consider the fluidic packaging interface to which a Teflon seal to the PDMS coated chip. The design of such a mechanical package is still a challenge, taking into account the fragility of wireponding. Future work is planned to investigate this open chip-to-world problem.

Chapter 3

Characterization of the proposed CMOS Nanofluidcs Platform Integrated SPADs

The integration of optical modality in a biomolecule sensing platform was motivated in Section 1.4 due to the impact that fluorescence-based approaches had on key tools in life sciences such as DNA sequencing and the study of peptide sequencing by techniques like Edman degradation. The electrical characterization of a biomolecule using a nanopore can provide insights about the size and abundance of a certain molecule; however, in a scenario where a sample is provided with multiple analytes of near-molecular sizes, labeling becomes necessary for differentiating molecules. For example, two cytokines that are released in CAR-T cell production and play a crucial role in modulating the immune response, such as tumor necrosis factor alpha (TNF-α) and Interferon-gamma (IFN-γ) both have molecular weights of 17 kDa, suggesting that any size difference will be overshadowed by electrical noise in the readout amplifier. The CMOS nanofluidic platform introduced zero-change CMOS SPAD thanks to the different doping profiles offered in the GF 55BCDLite technology node, moreover the workflow of IC design using the PDK allows integration of these SPADs in the proximity of nanochannels making them as close as possible to the measured analytes.

SPADs are well-positioned to detect fluorescence-labeled biomolecules due to their inherent capability to detect low-photon count emissions; this fact coupled with their location on the silicon die as close as possiple to the nanopore suggests that reduced analyte volume is required for detection as the radiation collection solid angle increases near the SPAD surface, which in turn has the potential to unlock fluorescence spectroscopy schemes for labeled biomolecules.

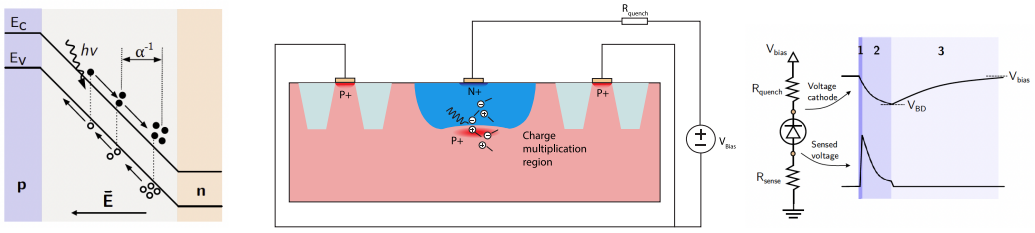
Integration of SPAD alongside the nanochannels involves a risk of reactive ion damage due to nano fabrication steps performed to release the channel. Initial experiments performed on this SPAD before and after post-processing indicate that the SPAD can survive these processing steps and still act in Geiger mode operation for photon counting and timing. This chapter starts with an introduction about the physics of SPAD devices and their operation. Section 3.2 explains in more detail the TC2 spad and the effect of nanochannels postprocessing on its performance. Section 3.3 introduces the characterization setup and main figures of merit measured for the nanofluidic platform SPAD to identify whether it is a good fit for use in FLIM techniques. Section 3.4 further compares the performance metrics for SPADs before and after nanochannel sacrificial layer etching to quantify the effect of RIE induced damage given the assumptions in the introduction. The chapter then concludes the advantages and limitations of SPAD in different FLIM setups.

3.1 SPAD Device Physics

SPAD is basically a phototodiode in reverse bias above its breakdown voltage. When a single photon incident on the photosensitive area (known as active area), an electron-hole pair is created. Under the condition that the depletion region ionization coefficient is greater than one for a certain bias voltage, an avalanche current is built up, resulting in a detectable signal. The avalanche build-up time is on the order of picoseconds and so the associated change in voltage is used to precisely measure the photon arrival time. This mode of operation is known as Geiger mode operation, derived from the Geiger-Müller radiation detector [90]. Figure 3-1(a) explains the dynamics of this process in terms of energy band diagram where an electron-hole pair is generated as a result of impact ionization, this generated carrier in the depletion region is accelerated by the reverse bias electric field, resulting in charge carriers transferring their energy to the lattice that impacts other carriers at an ionization rate α which can, under certain bias voltage, sustain noticeable current known as the avalanche current, thus marking the event of photon incidence.

3.1.1 Operating the SPAD

Once a photon is detected, the avalanche process needs to be extinguished to allow the SPAD to be ready for the next photon, which can be done by lowering the voltage across the SPAD and then restoring it to its initial value above the break down voltage. The simplest way to perform this action is with the aid of a series resistance, as shown in Figure 3-1(b). Next, the junction space charge region needs to be charged again to restore the SPAD to its initial condition, i.e., to reset the SPAD. In the series resistance configuration, SPAD can charge through the same path of quenching resistor. This scheme is known as passive quenching in contrast with a more complicated circuitry that actively reconnects the SPAD to different charging/discharging paths to perform the quenching and reset faster compared to passive circuitry.



(a) (b) (c)

Figure 3-1: Physics of the SPAD (a) Energy band diagram of SPAD PN junction illustrating the process of impact ionization where multiplcation is sustained for certain values of ionization coefficient α which is a function of reverse bias voltage applied to SPAD (b) External quench resistor is connected to the SPAD in what is known as current-mode sensing configuration (c) Tracing voltage and current through SPAD at the photon incidence event where first region depicts the avalanche current build up, second region shows the quenching process as a direct result for potential difference increase across R_{Quench} finally, the recharge process for which the SPAD is restored from V_{BD} to V_{bias}

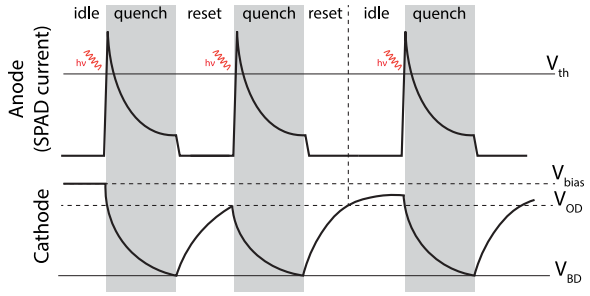


Figure 3-2: Photon detection cycles of the SPAD expressed in terms of cathode and anode voltage for the SPAD connection in Figure 3-1(c), Anode voltage reflects the value of SPAD current for small sense resistor, the SPAD is in ideal mode if it is fully charged above the specified V_{OD}.

Figure 3-1(c) shows the implementation of this scheme and the voltage and current traces of the passive quenching process. During the reset interval, the SPAD is blind to any incoming photon; it is not until the SPAD is fully reset that it is able to respond to another photon. Figure 3-2 shows an idealized typical counting cycle for an SPAD detector that illustrates the time slots where the SPAD is blind. Intuitively, reducing the quenching (blind) time would result in a higher counting efficiency. In addition, passive quenching is hindered by inherent noise sources in SPAD such as afterpulsing, where an avalanche is triggered not by a photon but rather by a trapped ion in certain defected energy levels. A discussion of this effect is detailed in Section 3.3.2.

3.1.2 Noise in SPADs

Lattice imperfections are inevitable in any solid state device and SPADs are no exception, they can lead to electron hole pairs generation by different mechanisms like thermal generation, field assisted Shockley-Read-Hall (SRH) generation, band-to-band tunnelling (BTBT), and trap assisted tunnelling (TAT). These loose charges often start an avalanche, hence false counts of photons, which are often referred to as dark counts. Field-assisted generation dominates the other mechanisms as far as dark counts are concerned [91]. Trap assisted tunneling results in another form of noise commonly known as afterpulsing, as it occurs following an avalanche where traps are filled during the avalanche and quenching phases and possibly leading to another avalanche following the primary one. Afterpulsing is particularly harmful as it extends the detector dead time. Both primary dark counts and after pulsing can be statistically described by a Poisson process, where the latter is correlated to the dark counts and tends to show up in bunches.

3.1.3 Optimal Operation of SPADs

There is a balance point that should be characterized in the operation of a SPAD for better readout fidelity. Increasing overbias voltage results in a higher photon detection probability as it boosts the avalanche initiation while it accelerates band-to-band tunneling and trap-assisted tunneling, therefore increasing the afterpulsing probability, which in turn increases the detector dead time. The combination of both SPAD and its quenching circuit is characterized to quantify its merits [92]: the photo-detection efficiency, which is expected to be less than 1 as a result of the blanking time needed for the SPAD reset process, the ratio between the number of detected photons to the actual number of incident photons is an important SPAD metric, and the inherent noise sources resulting from the DCR or after pulsing probability. In what follows is a description for the characterization that was performed and an estimate for those figures of merits trying to validate the TC2 SPAD in a photon timing application such as the TCSPC.

3.2 TC2 CMOS SPAD

The 55BCDLite foundry process used to build the nanofluidic platform offers vertically uniform doping profiles that were utilized to build the SPADs. A uniform PN junction is needed when reverse bias is applied whcih is pertinent to support the multiplication of avalanches in the event of photon absorption. To avoid premature junction breakdown, which occurs in these types of shallow-doped wells because of a high electric field, a guard-ring region is grown around the active area of the photodetector. This is achieved by shallow trench isolation (STI), an insulating SiO_2 zone that is typically grown to isolate nearby transistors. This layer, together with the round shape of the detector, eliminates sharp corners where the field increases locally, ensuring that the center of the junction breaks down at a lower reverse bias voltage value compared to corner breakdown [73]. Figure 3-3 depicts a schematic for the three variations of doping profiles implemented on the TC2 die. The devices have annotations PD4A, PD6C & PD6D. The motivation for adopting each profile was explained in [1] where those designs were implemented in an earlier version of the chip (TC1). In what follows, the focus is on the junction PD6D as it was chosen to be the junction constructed near the nanofluidic channel. It has the lowest junction breakdown owing to the retrograde P doping optimized to modify the depletion region so that peak electric fields occur away from the edge of the device without comprising the quantum efficiency. Figure 3-4 (a) shows a top view of the area of the nanofluidic variants in the TC2 die. Each of the channels annotated from A to J implements a certain arrangement of the SPADs and nanochannels

Integration of SPAD alongside with the nanochannel addresses multiple challenges, first the fact that deep submicron technologies do not offer efficient visible light absorber as the band gab is nearing the UV band, however, tweaking the doping profile in a high voltage devices-based process allows enlargement of the depletion region by excessive reverse bias tuning the band gab more toward the red and IR bands resulting in higher photon absorption efficiency in the visible range, the flip side of that is higher bias voltage results in a higher dark current, i.e. carriers resulting from ionization from photon sources other than light

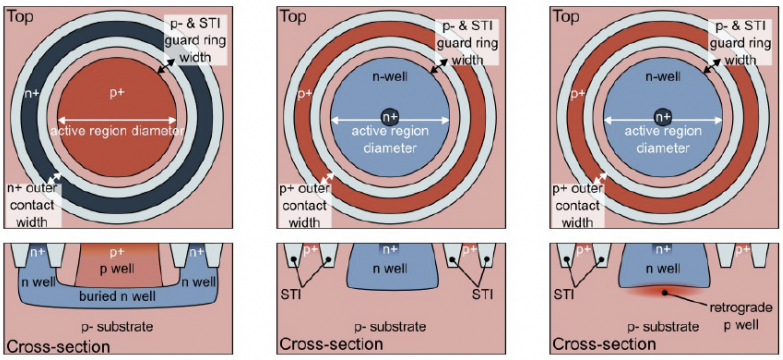
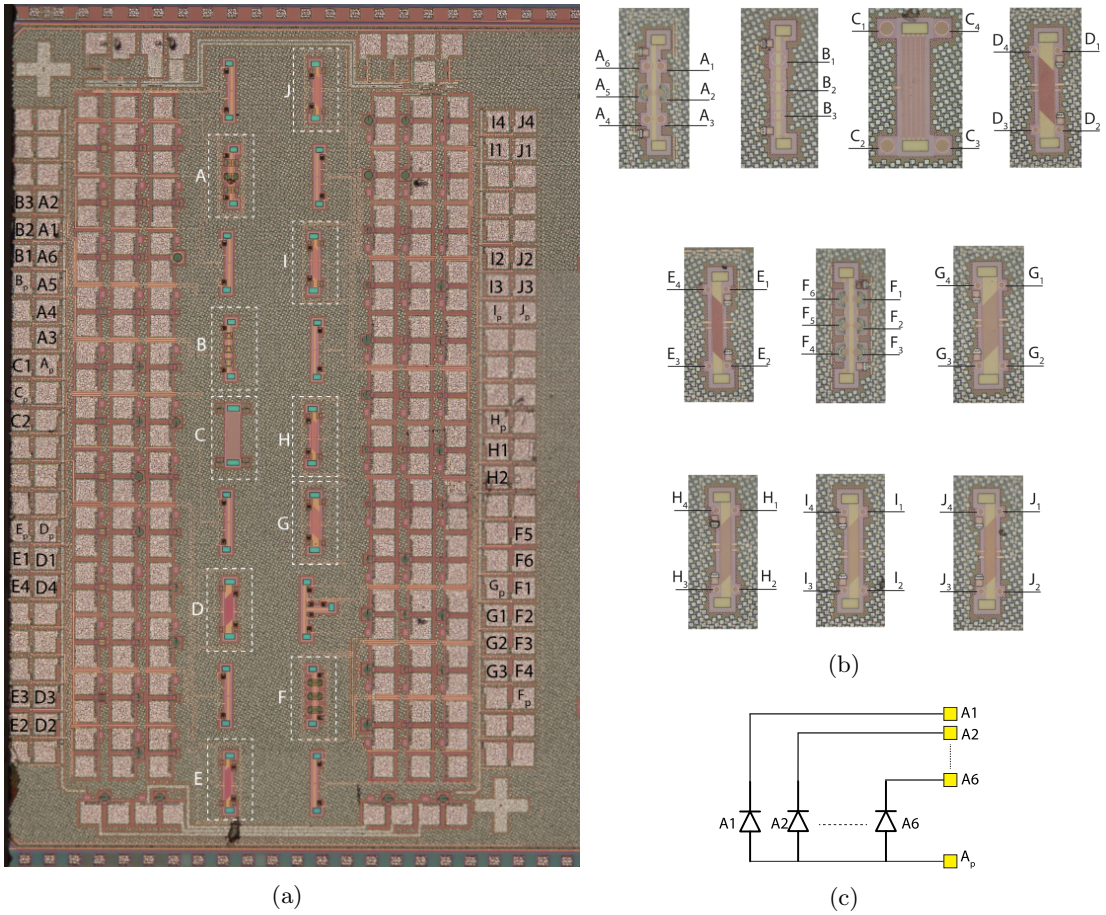


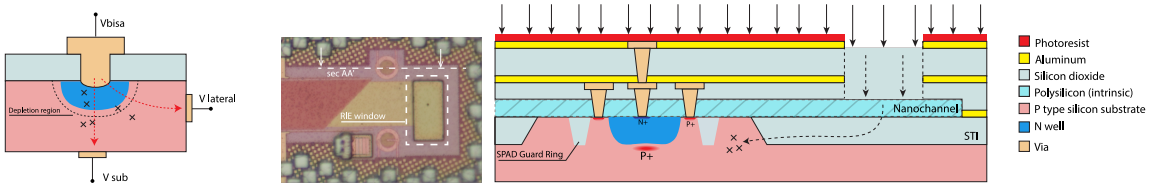
Figure 3-3: TC2 different SPAD junctions: doping profile from left to right: PD4A, PD6C and PD6D

which will be detailed later. Second, the post-processing that the die undergoes to etch away the sacrificial polysilicon and open nanofluidic channels. Those steps include: spin-coating the SU8 layer to pattern the microfluidic channel, spin-coating the photoresist to form reactive ion etching windows, Reactive Ion Etching (RIE) process to etch away dielectric layer above polysilicon, and finally, Xenon florid isotropic etching of poly silicon and completely opening the channel.These steps are described in detail in [1]. Reactive ion etching has a detrimental effect on PN junctions as the accelerated etchant ions can enter to the junction region, creating lattice defects, which in turn introduce undesired energy states that could act as what is known as trap states. Researchers investigated the plasma induced damage and its effect on heterogeneous junctions in an effort to understand the defect mechanisms and were able to confirm the existence of defects in both lateral and vertical directions [93] by measuring increased leakage current after plasma exposure through terminals shown in Figure 3-5(a). The RIE processing of the nanofluidic platform targets the nanochannel opening as seen in Figure 3-5(b) and so the rest of the chip is coated with thick photoresist including the SPADs, therefore we expect less plasma induced damage. Another argument can be made based on the RIE recipie listed in [1] where Reactive Ion Etching (RIE) was performed using Inductively Coupled Plasma (ICB) at RF power of 400 W and Bias of 100 V, comparing those parameters to the experiment in [94] performed on GaN junction assures that chosen parameters for nanofluidic chip processing is expected result in minimal degradation. The rigorous calculation that predicts the possibility that accelerated plasma ion etchant will cause defects in SPAD junction



(a) (b) (c)

Figure 3-4: Active area of the nanofluidic chip (a) Different variations of nanochannels and their annotations. Each group shares a common terminal for the anode that has the subscript (p), where the cathodes are wired separately to different pads, annotated by numbers mapping to each SPAD. Only SPADs with a cathode pad adjacent to the channel common anode can be tested using the GS probe; examples are A3, C1, C2, I3, J3. (b) Expanded view for the channels using 50x objective (c) Schematic showing the terminal connectivity of the SPADs associated with each channel



(a) (b)

Figure 3-5: (a) plasma deformation characterization Setup in [93] illustrating the current flow in lateral and vertical directions resulting from RIE defects (b) Cross section of nanofluidic platform (channel D) highlighting the SiO2 window etched to access the channel. Dashed arrows highlight the RIE reaction and possibility of lattice deformation due to ion dispersion

region can be performed by identifying formation energy which is a function of the silicon lattice energy and the chemical potential of the specific ion used in etching and can be approximated using Density Functional Theory (DFT) [95] which is a discussion outside the scope of this thesis. Finally, the removal of polysilcon sacrificial layer is expected to disturb the reverse biased junction electric field. The integrated SPAD junction has a doping profile that is optimized to concentrate the electric field around the center of space charge region to guarantee that avalanche breakdown starts in the center of active detector area, not from edges which impacts detection probability as will be seen later. The introduction of polysilicon with dielectric constant $\epsilon_r \approx 11.9$ in the vicinity of the detector is expected to pull some field lines resulting in change in the breakdown profile, so does removal of this polysilicon after etching the polysilicon sacrificial layer leaving an empty channel with a near unity dielectric constant such that less electric field intensity exists in this area compared to the surrounding SiO_2 which is the actual setup where this platform is supposed be used.

3.3 Characterization of SPAD

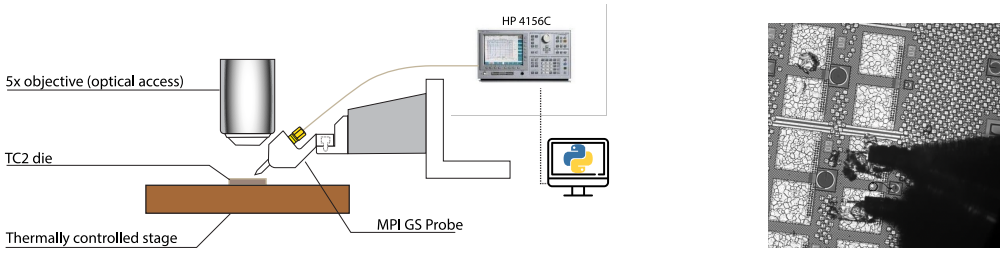
Initial assessment of the TC2 dies was performed by probing the die directly using GS probe. Figure 3-6 shows a schematic of this setup in which the probe connects the SPAD to the HP4156C parameter or any external circuitry through a coaxial cable. A green fiber laser source is used to provide 5 milli-watts of optical power at $\lambda = 520$nm. The optical setup depicted in Figure 3-7 serves to attenuate this power to the femto-watt level and direct through a low loss fiber to the probe station where the die stage and GS probe reside. Optical characterization for a single photon detector/counter requires such low power level of optical power that can be achieved by attenuating the laser source through a series of neutral density filters. The laser beam diverges as it is propagating for a distance so a collimatting lenses are placed to focus the attenuated laser beam to less than 4 microns spot size (effective area of the SPAD) and directed through the objective lens to shine the SPAD under test where there is a camera that helps with aligning the beam visually through the 90:10 beam splitter placed above the objective. The laser beam spot size was confirmed by capturing the a sample image and processing the intensity profile of pixels using imageJ software, where the $1/e^2$ width that reflects the spot size was estimated. Because of the extremely low level of optical power which is below the noise threshold of available optical power meters, a calibration process is performed by tapping part of the optical power before the neutral density filters and measuring the ratio between this power and the delivered optical power at the stage for each filter placed individually. The ratios are combined into one factor that is used to identify optical power incident on the SPAD side in terms of the tapped power before passing through the neutral density filters. The main reason for splitting the optical setup into two parts connected by a fiber is to avoid misalignment of attenuated beam with respect to SPAD active area after the neutral density filters are placed in position via mechanical sliders after visually hitting the SPAD active area with the non-attenuated version of the laser beam. Finally, a mechanical slider (S1) is used to switch between dark and light conditions during the experiment to avoid turning the laser off and guarantee optical power stability during the experiment time. Experiments were targeting SPADs near nanofluidic channels and this section lists the measurements of a die

that is not post processed to get a sense of the device performance and have a base line to which the performance of a processed die is compared.

3.3.1 IV Characteristics

IV measurements were performed to identify SPAD regions of operation and quantify the effect of post processing on the device performance. Figure 3-8 shows IV characteristics for two different SPADs, namely D_1 and I_3. Measurements performed in dark conditions shows that both junctions exhibit saturation current in the order of 10 pA. The effect of RIE processing is evident in all measurements where we can spot slight increase in the reverse bias saturation current and slight decrease in the reverse breakdown voltage value which marks the start of accelerated carrier multiplication. Both effects are naturally occurring as result of RIE introducing more defects in the junction region that are responsible for conduction of minority carriers leading to reverse bias current increase and creating regions where localized high-field facilitate early breakdown. We can argue however that the magnitude of change shown in results confirm that devices maintains its performance as the the active area is not exposed to RIE directly as discussed in Section 2.

Breakdown voltage is defined as the minimum reverse bias voltage at which an injected carrier in the space charge region produces an avalanche. However, practically measuring this value can follow many conventions, one being the voltage at which the logarithmic slope changes drastically; in this region the current is flowing at a rate that sustains the avalanche. The breakdown point should be accurately determined, as the percentage of excess bias (i.e. reverse bias applied beyond the breakdown voltage) is what governs the dynamics of photon detection using SPAD [96]. Both SPADs measured have the same diameter (4 μm) and the retrograde doping profile 6D exhibit breakdown voltage near 24.4 V (reduced to 23.9 V after RIE processing). The parameter analyzer was current limited to 1 mA to avoid destructive testing.



(a) (b)

Figure 3-6: Electrical characterization of SPADs (a)Connectivity through the GS probe to the semiconductor parameter analyzer: The GS probe is mounted on keinametic stage moving in x, y and z directions, so does the stage that mounts the die under test (b) Optical access confirming landing of the probe

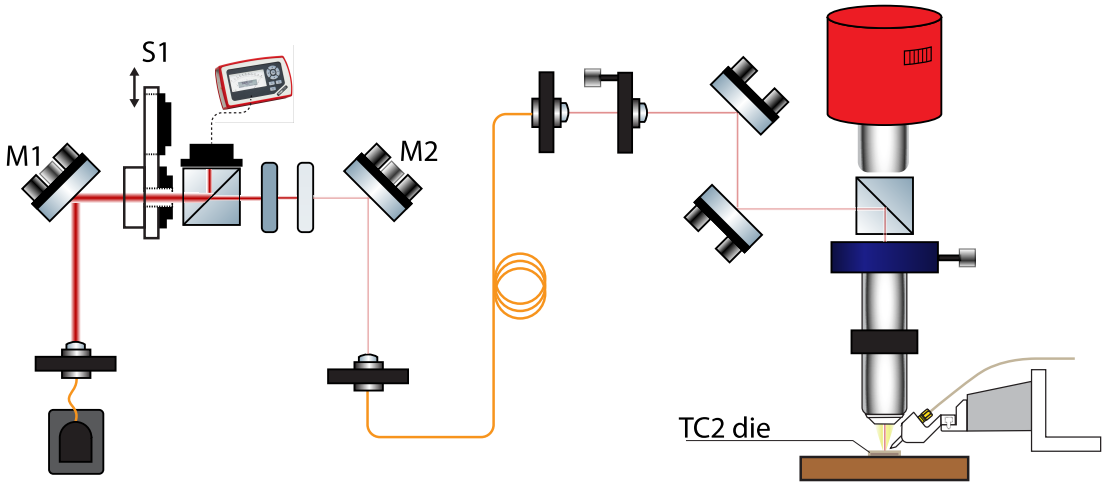
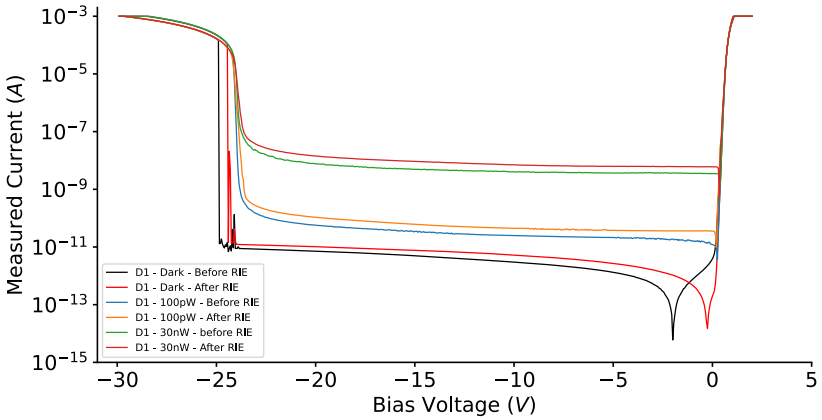
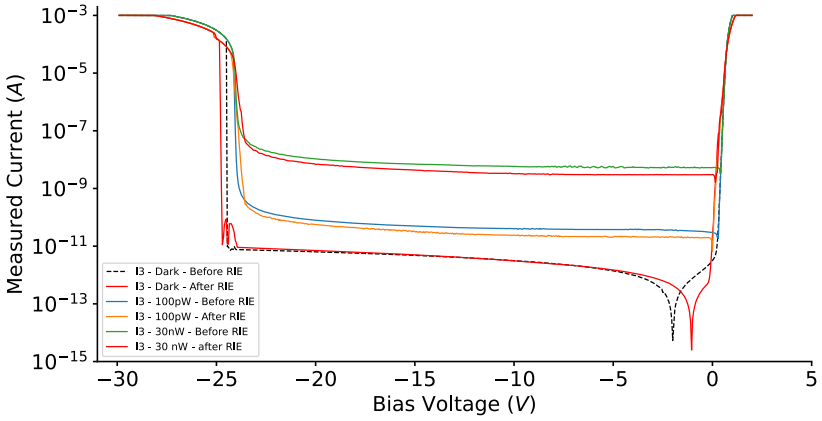


Figure 3-7: Optical characterization setup of the SPAD

These measurements, together with the saturation current value of each junction, can lead to an estimate of the doping profile concentrations of donor and acceptor atoms, which in turn can be used to calculate the capacitance of the depletion region (C_j). The slope of the IV curve beyond the break-down voltage is the junction resistance in the avalanche phase (R_j). Those parameters together with the parasitic capacitance formed by the cathode-substrate (C_{CS}) and anode-substrate (C_{AS}) interfaces can be used to build a lumped circuit model that captures the dynamics of the avalanche.



(a)



(b)

Figure 3-8: IV characterization of two SPADs near nano channels at Dark conditions and two level of optical power exposure, 100 pW and 30 nW. Results were acquired for devices on two different TC2 dies one of which has undergone post processing (RIE exposure) to release nanochannels as indicated in [1]. (a) SPAD: D_1 (b) SPAD: I_3

3.3.2 SPAD Events Readout

The SPAD front end circuit used for initial characterization is a simple passive quenching circuit followed by an amplifier circuit. The motivation to use of amplifier was made apparent after choosing the correct quenching resistor which can be done by performing a load-line analysis given the IV characteristics obtained, and the fact that current flows in series through the SPAD and resistor at the avalanche event. Figure 3-9(a) explains this concept by overlaying the IV characteristics of three different resistors with the measured IV curve of the SPAD of interest, illuminated I_3 SPAD in this case. The ideal resistor is one with a value that intersects the SPAD IV at a point slightly higher than the breakdown value, that is, the start of the Geiger mode operation (V_{BD}=24.6 V), to ensure that the SPAD remains in this mode of operation after the avalanche. A larger resistor value will place the SPAD in linear avalanche region, resulting in longer reset time, and a smaller value will operate the SPAD at a non-practical value of over bias. For this SPAD, a resistor of value 100 $K\Omega$ is therefore a feasible choice. The dynamics of avalanche can be traced on the zoomed-in version of the IV plot shown in Figure 3-9(b). Starting from point (1) where the SPAD is biased beyond its breakdown, here we chose overbias voltage V_{OB} = 26.5 V for a reason that will become apparent after analyzing the dark cont rate in Section 3.3. An incident photon causes an avalanche current to build up rapidly and the circuit now is at point (2), current flowing at this point has a value of $\frac{V_{OB}-V_{BD}}{R_J}$ where R_j is the space charge resistance that can be estimated from the slope of the SPAD IV characteristics in the Geiger mode region, for this case R_J = 4.83 kΩ. Because the voltage across R_Q is increasing, reducing the voltage across the SPAD, the current is reduced, i.e. quenched, and lies at the intersection point between the resistor load line and the characteristic curve of SPAD IV, which is marked (3). From points (3) to (4) the current further drops as the SPAD potential barrier is restored and the remaining current flowing at this point is charging the built-in capacitance of the SPAD to bias it back to V_{OB} for another detection cycle.

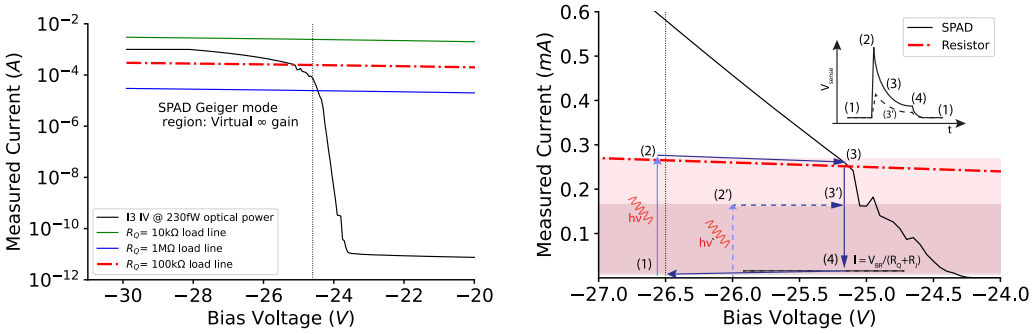
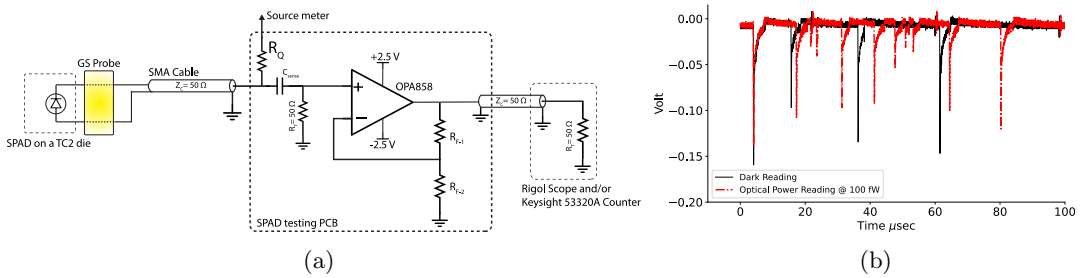


Figure 3-9: Analysis of the SPAD passive quenching circuit (a) Characteristic IV curve for an illuminated I_3 SPAD overlayed with three different load lines to estimate the correct biasing resistor that fixes SAPD operating point around the begining of Geiger mode region of operation, 24.4 V for this specific SPAD. Slope of each line = -1/R_Q. (b) Capturing the dynamics of avalanche events: the lightly shaded area is a photon induced avalanche for a fully reset SPAD defined by points (1),(2),(3),(4).Whereas the darker shaded area defines an avalnche for a partially reset SPAD which often occurs due to afterpulsing or high optical power beams with a large stream of photons. The region is defined by points (1), (2'), (3'), (4). The top right inset depects the time evolution of current pulse that maps aforementioned transitions

The maximum current swing that defines the peak-to-peak detection current pulse is defined by the lightly shaded area in Figure 3-9(b), it is approximately equal to $\frac{V_{OB}-V_{BD}}{R_J}$. Using a small sense resistance of 50Ω as in the arrangement in Figure 3-1(c) translates the current to ≈ 13 mV peak to peak pulse. In the characterization of the pulses and arrival times, a frequency counter is often deployed. In this setup, the keysight 53220a frequency counter is used, which features a sensitivity of 20 mV peak-to-peak from DC to 100 MHz. Weaker pulses are also expected, which are generated from re-triggering the SPAD before it is fully reset. This scenario is not uncommon and occurs as a result of after-pulsing, which is an avalanche initiated by an electron-hole pair held within a trap energy level during the main avalanche and affects the device before its fully reset. Other shorter pulses could occur when the optical power is high enough that the photon count is at a rate faster than the SPAD reset time. Ultimately, those pulses are even expected to show at a level below the fundamental 13 mV pulses. An amplitude amplification is necessary to bring those different pulses above the sensitivity level of the frequency counter.



(a) (b)

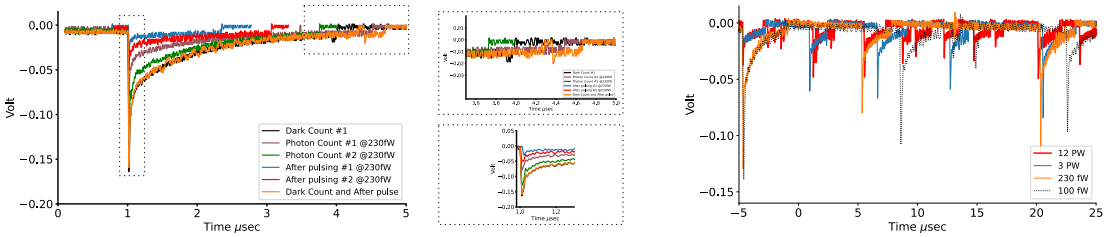
Figure 3-10: Time domain traces of quenching circuit: (a) Schematic of passive quenching pulses amplification circuit (b) Oscilloscope traces of the SPAD passive-quenched pulses

A 20 dB amplifier is built on a custom PCB using a Texas Instruments OPA858 high-speed operational amplifier. This choice was made based on the gain-bandwidth product value that this chip offers, 5.5 GHz, in addition to its relatively low input capacitance. Although the expected counts are in the megahertz range, the bandwidth offered is necessary to maintain the properties of the avalanche pulse leading edge and introduce minimal jitter. The PCB also has an Analog Devices LT3032, a fixed dual LDO to supply the bias rails ($\pm$2.5 V) of the amplifier in addition to the coaxial termination to connect to the GS probe. The PCB also has plated wireponding terminals bypassing the coaxial termination and connecting directly to the op amp for future testing schemes that improve the readout fidelity by eliminating the capacitance introduced by the GS probe and the coaxial cables. A schematic of this custom board is shown in Figure 3-10(a). The quenching resistor is connected in series with SPAD through a coaxial cable. In contrast to the placement of the sense resistor in the configuration depicted in Figure 3-1(c) the sense resistor is now moved to the input of the amplifier and the current pulse signal is AC coupled through a coupling capacitor C_{sense} for two reasons: First, the input of the operational amplifier OPA858 is sensitive to the DC level and ideally we would like to keep it at 0 V DC, which the charged C_{sense} guarantees independently of the SPAD DC bias. Second, a floating SPAD connected by the GS probe couples noise effectively through the die substrate capacitance that was simulated earlier showing that the floating SPAD arrangement will have an AC gain of 27 dB if a noise tone signal is injected through the substrate capacitance and measured across the sense resistor. In fact, a large noise magnitude was measured in one of the earlier

implementations of a quenching circuit with a floating SPAD arrangement. It is evident that grounding the SPAD is crucial in a setup where the connection is established by a GS probe. The sense capacitance will reverse the polarity of the sensed avalanche pulse, which is accounted for by the dual-polarity LDO supplying the operational amplifier. Finally, the feedback resistors R_{F1} and R_{F2} have values of 1 kΩ and 100 Ω, respectively, achieving a gain factor of 20.8 dB for a noninverting amplifier configuration, which is more suitable for the input signal source with a larger capacitive source impedance as is the situation with SPADs.

Figure 3-10(b) shows the readings obtained from the amplifier PCB when connected to the SPAD via the GS probe. Several points to observe from these traces, first dark count pulses peak to peak range from 110 to 150 mV, the amplifier gain together with the 13 mV peak to peak value deduced from the previous IV load line analysis indicated that we should expect pulses around 143 mV. The variance of pulse height can be attributed to the stochastic nature of scattering in a SPAD junction leading to variations in the latch current. These variations mean that point (2) in Figure 3-9(b) will slightly move up or down, affecting the peak to peak value of the detection current pulse. Second, illuminating the SPAD by a 100 fW 520 nm laser we can imminently spot the increase in resulting pulses. The amplitudes of pulses show more variance under illumination, which can be attributed to the slight shift in space-charge resistance, which disturbs the bias point bringing it a little higher as the slope of IV curve at Geiger mode region changes slightly under illumination. Third, a closer look at pulses under different lighting conditions is shown in Figure 3-11(a) where we can spot two sets of pulses: one of span 3.2 $\pm$ 0.4 μsec and the other is shorter pulses (less than 2μsec) with lower magnitude. The last set is what we refer to as afterpulsing.

Increasing the incident optical power to the picowatt level, we notice a reduction in the pulse amplitude level and its duration. The oscilloscope traces in Figure 3-11(b) show that at 12 pW of optical power the afterpulsing becomes dominant, at which level the photon detection probability is drastically reduced; moreover, we have no certainty that the observed avalanche event is the result of an incident photon. To mitigate this problem



(a) (b)

Figure 3-11: Stochastic nature of SPAD avalanche pulses: (a) Comparing different pulses from SPAD readout to highlight the difference between fully reset avalanche, afterpulsing and stochastic nature of avalanche scattering (b) Dominance of afterpulsing at higher optical power levels

in characterization with a passive quenching circuit we would keep the optical power as low as possible to the level that maintains a Poisson process with regard to photon arrival timing[97]. To specify the maximum power that SPAD can handle, the Keysight frequency counter is deployed in the setup depicted in Figure 3-11 where we primarily measure the distance between consecutive pulses. Later, these time intervals are sorted and plotted on a histogram which at a large number of pins converges to the probability density function (PDF) for the photon arrival frequency. Informed by the oscilloscope traces obtained earlier, a detection threshold is arbitrarily chosen so that it is most likely to avoid the afterpulsing with low amplitudes. We start with a 25 mV detection threshold up to 100 mV. This works in parallel with increasing optical power until the Poisson distribution is distorted, at which point the SPAD with a passive quenching resistor is no longer an efficient photon counter. Figure 3-13(b) shows the anticipated normalized distribution which is squeezed as we increase the optical power. However, in Figure 3-13(d) we show that the Poissoinian nature is lost at incident optical power of 30 pW as it converges to a narrow Gaussian distribution.

3.3.3 DCR measurements with passive quenching circuit

DCR defines the noise floor of the SPAD as a photon detector, it is an important figure of merit when comparing performance of multiple SPADs. In the context of the nanofluidic

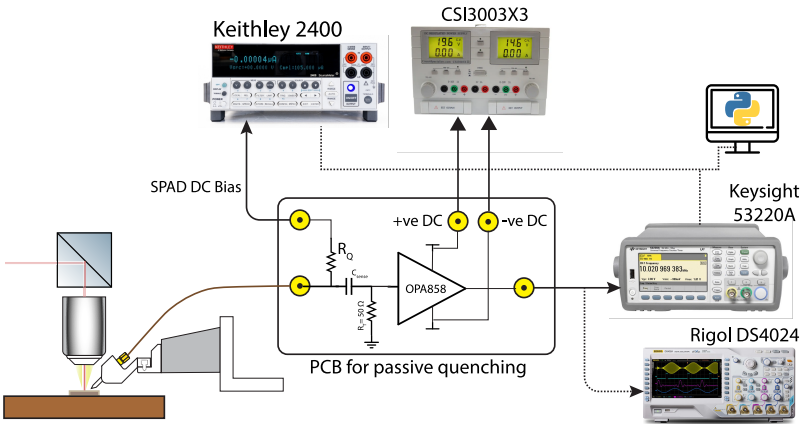


Figure 3-12: SPAD characterization setup for DCR and PDP

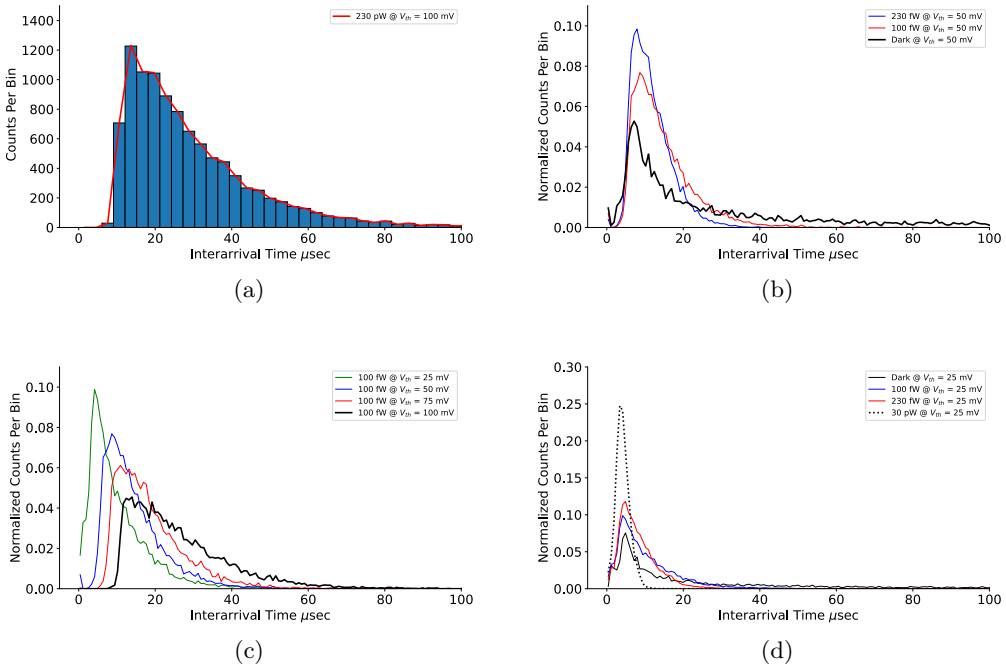


Figure 3-13: Sampling interarrival duration of pulses at different settings using a processed die, I_3 SPAD (a) Sampling and pinning histogram data (b) Comparing different normalized histograms obtained by biasing SPAD at 26.5 V and varying the incident optical power (c) Variation of V_{th}(d) Effect of 30 pico Watts of optical power on interarrival statistics where we can see total deviation of poissoin's process

platform, it will also serve to confirm the functionality of the SPAD after post-processing of the TC2 die. The implementation of the DCR characterization setup was performed using the setup in Figure 3-12 where we configure the frequency counter to the "Totalize" mode, which simply sums up the number of pulses that cross a certain voltage threshold. A variable current-limited power supply is added to the setup to characterize the DCR dependency on voltage overbias which was swept from 0 to 30%.

The current pulses start at weaker amplitudes as argued earlier in Section 3.2. Increasing the overbias ratio results in an exponential increase in dark counts shown in the results in Figure 3-14(a) and (d). There are three different exponential rates before 28 V that represent the dominance of avalanche initiating carriers. At lower overbias, the avalanche is dominated by direct band-to-band tunneling. As overbias increases, direct band thermal generation starts to dominate. The further overbias increases the faster the drift velocity, which lowers the avalanche probability as carriers now have less life time, which is apparent by slope decrease. Beyond 28 V all carriers experience the drift velocity effect even those trapped in defect states, hence, there is an apparent distinction between processed dies and normal dies in this region where we can clearly see that processed dies have a lower slope in this region as they have more defects as a result of processing. In fact, defects do not affect the moderate values of overbias (around 26 V) .Threshold dependency is also experimented following the guidelines to target the threshold at a level that maintains the Poisson properties of interarrivals.

The photon detection probability was characterized at two different optical power levels, 100 fW and 230 fW as we can guarantee from analysis of the photon interarrival that those levels will not saturate the detector.

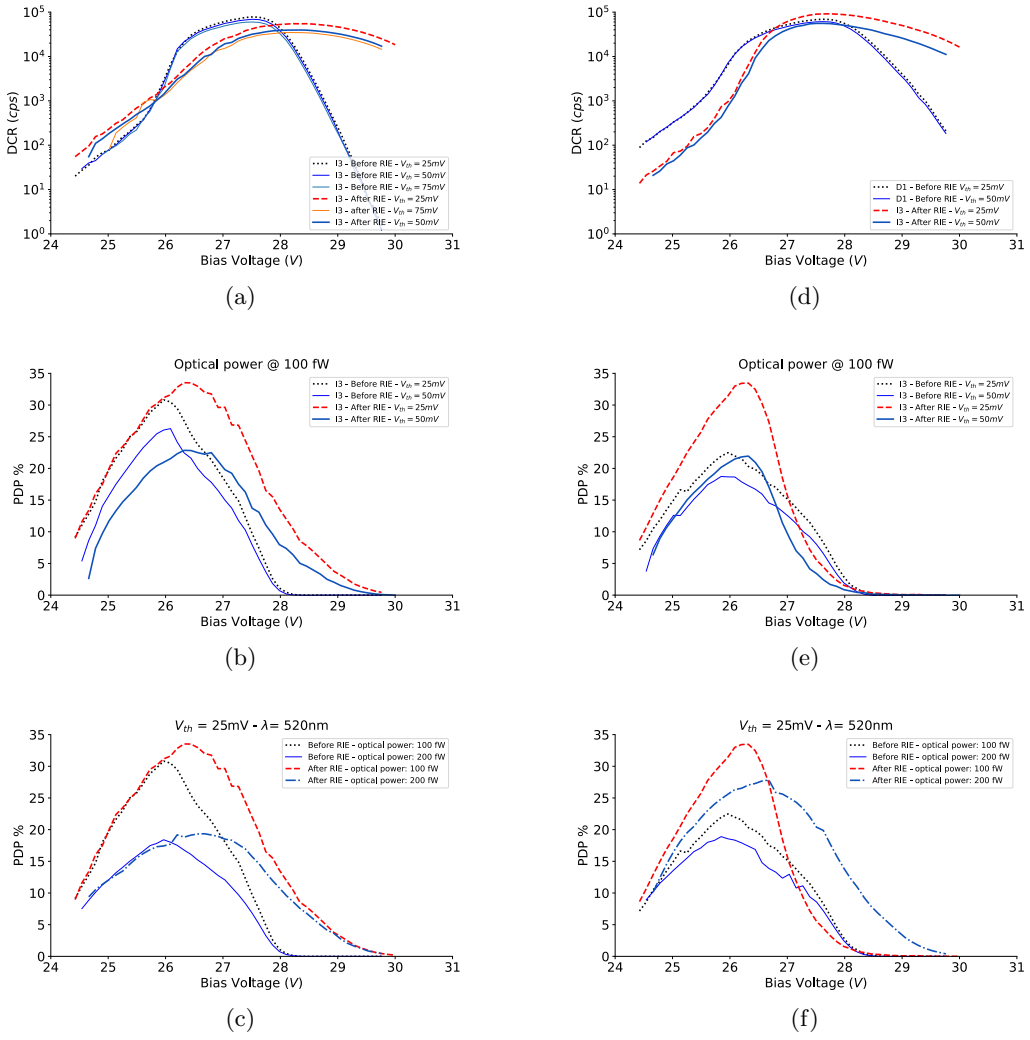
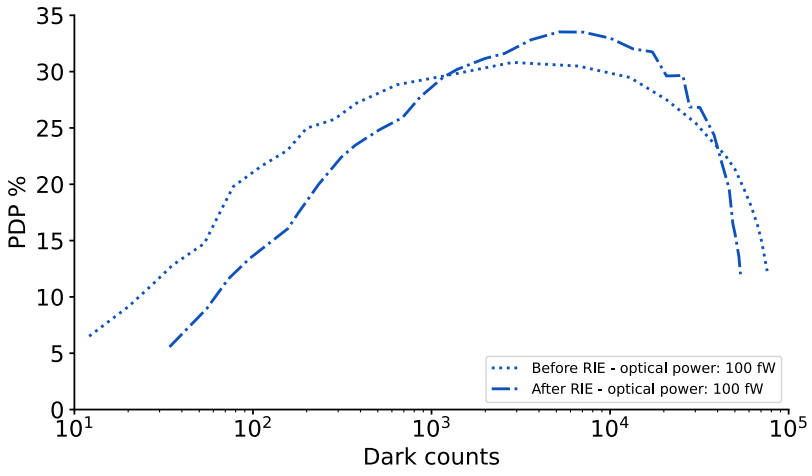
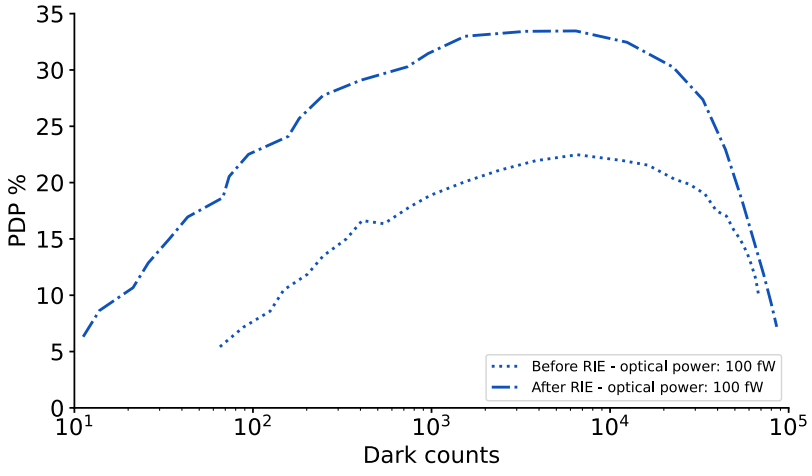


Figure 3-14: Characterization of DCR and PDP for two different SPADs before and after post processing. For SPAD I_3 we have (a) DCR at different values for threshold (b) Measurement of PDP at 100fW of optical power (c) Measurement of PDP at two different optical power levels. From (d) to (f) are same set of measurements for SPAD D_1



(a)



(b)

Figure 3-15: PDP vs. DCR before and after post processing for channel SPADs (a) I_3 (b) D_1

3.4 Conclusion

The chapter introduced the characterization of a novel SPAD junction integrated in the CMOS nanofluidics platform, highlighting their ability to detect single photons through avalanche multiplication when operated in Geiger mode. This operation mode was achieved even after the necessary post-processing steps needed to release the channels, as we conclude that RIE only affects the SPAD at higher overbias voltage values beyond the operation region of interest. The characterization results indicate that the SPADs could achieve values of PDP over 30%. This suggests that further optimization of the quenching and reset process is needed to enhance the efficiency of the detector. Despite these challenges, the work demonstrates the potential of CMOS nanofluidic SPADs to precisely detect minute changes in the optical properties of the analyte, facilitated by the successful integration of sensitive optical detectors with nanofluidic platforms.

Chapter 4

Passive Quenching - Active Reset Circuitry for Integrated CMOS SPAD

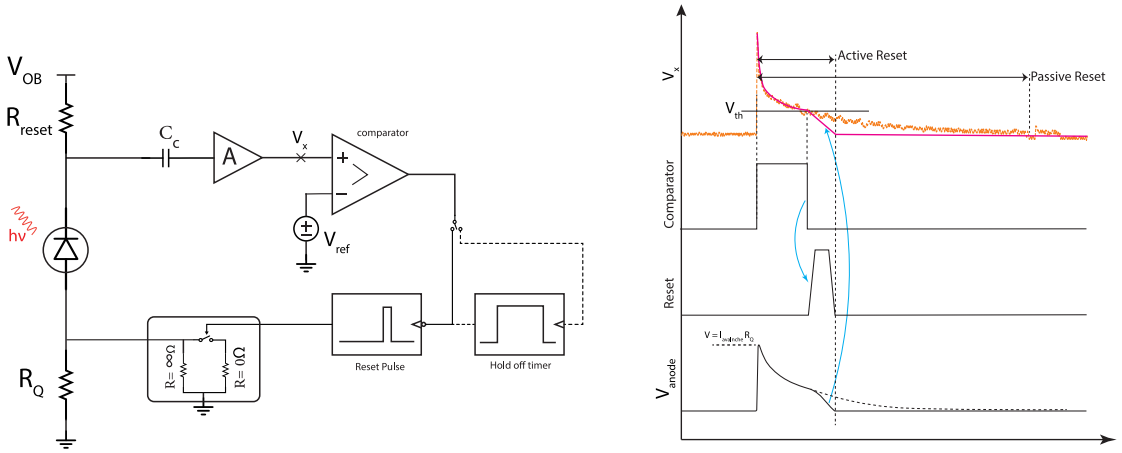
The SPAD characterization performed in Section 3.3.2 was based on the amplification of passive quenched pulses, which was useful as it gave insight about the operation of the Geiger mode, the bias point of the SPAD, the interarrival statistics and initial assessment of both DCR and PDP. The circuit shown in Figure 3-10(a) was simple to implement and granted stable operation in detecting pulses given the parasitics in such a setup where contact is always made by a GS probe followed by a 1 ft. coaxial cable to connect to the PCB. The downside of this setup (Figure 3-12) is that these parasitics contribute to the quenching time. The results in Figure 3-11 showed a pulse duration of ≈ 3.2 μsec. This time is detector dead time during which the SPAD is blind and cannot detect the arrival of another photon. For this detector to be used in a TCSPC setup, the dead time should be less than 1/10th of the shortest fluorescence decay time [70] which typically ranges from 1 to 10 nanoseconds. An active quenching circuit employ active components to reconfigure the quenching and reset paths so that it is not limited by the detector time constant. This approach is favored for interfacing with SPADs as it increases the maximum achievable

counts and reduces the probability of afterpulsing, thus enhancing the dynamic range of the detector.

In this chapter, we develop a prototype discrete circuit that reduces the reset time to less than 10 nanoseconds. This prototype is built to interface with TCSPC electronics to run initial life time measurement using the integrated detector, paving the way for the integration of a version of this circuit on the same CMOS nanofluidic chip. Section 4.1 of this chapter describes the top-level architecture of the discrete circuit implemented. In this architecture a modification was required for passive resistors used for quenching and reset, Section 4.2 revisits the PSPICE model of the SPAD and studies the effect of these connections on the SPAD operation. Section 4.3 covers the designs and challenges of each block of the active reset circuit. Section 4.4 discusses the results obtained using the discrete passive-quenching active reset circuit and concludes the chapter previewing room for improvement for this circuitry.

4.1 Passive Quenching Active Reset Topology

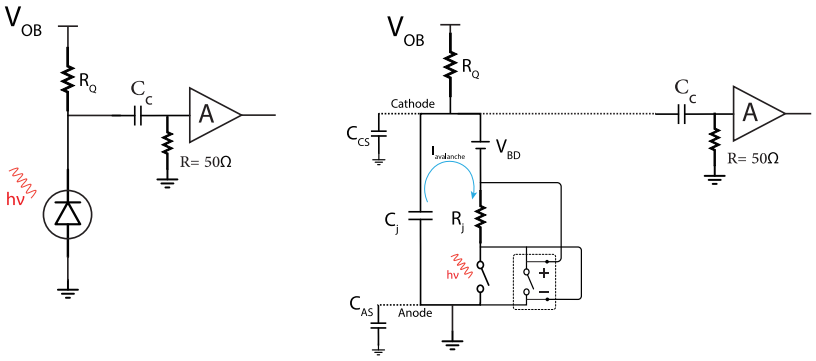
Active quenching and reset circuits are designed to create fast discharging/charging paths in the event of avalanche detection; thus the quenching and reset process no longer depends on the RC time constant of the SPAD connection. A common topology for such a system is depicted in Figure 1-12 where we can notice a comparator for event detection, a hold-off timer to add some delay for the clearance of the SPAD electron traps, which is necessary in the event of running SPADs at cryogenic temperatures, and a reset pulse generator that quickly charges SPAD to the overbias point. In what follows, we chose a passive quenching active reset topology, which still relies on a passive element for the detection and quenching of the avalanche, and employs active switches to reduce the reset time. The combination of passive quenching with active reset simplifies the circuitry compared to active quenching, which adds a level of complexity to the system. Although active quenching is superior in its temporal resolution, this prototyping SPAD dead time is dominated by its reset time. Figure 4-1(a) shows a block diagram for the implementation of passive quenching - active reset for TC2 SPAD where the avalanche pulse is DC decoupled and amplified to values that the discrete comparator can detect. The comparator output registers the count of the avalanche events, in addition, it triggers the reset pulse generator which, in turn, will switch the state of tri-state buffer block connected to the SPAD anode, thereby nearly shorting the anode to ground, which immediately discharges all remaining current from the avalanche event and biases the SPAD back to its overbias point. R_{reset} is usually much smaller than R_Q and is merely used for SPAD protection during the short reset time in which the series resistance is forcibly changed drastically, which results in a faster reset time compared to passive reset. Tri-state buffer implementation of resetting the SPAD is preferred to n-channel MOSFETs switch due to its low input / output capacitance which results in a shorter propagation delay, that is, a faster reset time. Figure 4-1 (b) depicts the timing diagram of this system overlayed on a SPAD passive reset trace from the characterization results previously reported in Figure 3-11 where the threshold position is exaggerated for the purpose of illustration. The circuit is configured so that the reset pulse is triggered at the falling edge of the comparator signal to avoid loop instability that may occur if the reset



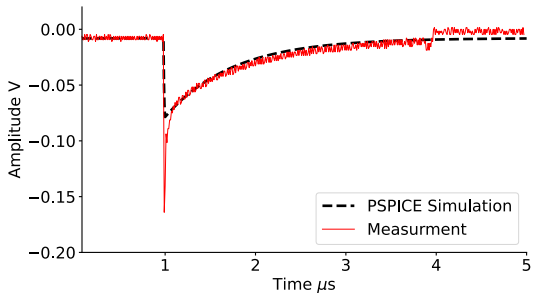
(a) (b)

Figure 4-1: (a)Top level diagram of passive quenching-active reset circuit (b) Timing diagram: the comparator signal duration is exaggerated for illustration. Dotted lines represent signal trace for passive reset process

pulse was faster than the fall-time limitation of the comparator used.



(a)



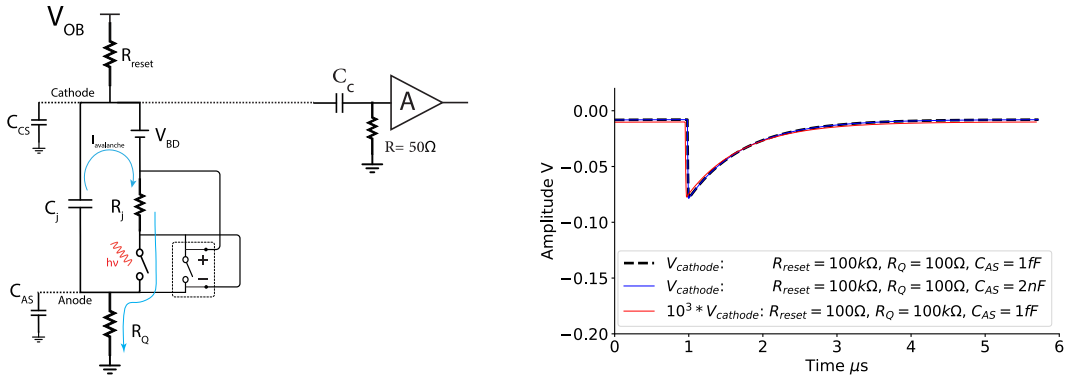
(b)

Figure 4-2: SPAD lumped circuit model: (a) Connection to passive quenching circuit (b) PSPICE simulation results vs. Measuments

4.2 PSPICE simulation of SPAD: Effect of rearranging resistors for active resrt

The passive quenching and reset circuit shown in Figure 3-10(a) introduced a simple and convenient SPAD connection where the cathode connecting the anode and the quenching resistor was probed using a decoupling capacitor to AC couple and amplify the avalanche pulse, while the anode was grounded. This is known as the current sensing configuration of passively quenched SPAD. The reason for the name convention becomes apparent when we look at the SPAD circuit model devised in [98] and depicted in Figure 4-2, the switch in series with space charge resistance R_j models the avalanche event occurring at the picosecond scale,with another parallel switch[1] that models the current latch mechanism occurring in the quench phase. As can be seen, the SPAD capacitance C_j is charged to V_{OB} and so once the switch closes instantaneously this capacitor will pump current through the now grounded R_j until it reaches V_{BD} ($V_{OB} > V_{BD}$). This lumped circuit model emulates the process explained in detail in Section 3.3.2. When a coupling capacitor is placed at the cathode terminal, the change in current is captured and amplified later. As in Figure 3-10 (a) the cathode is connected through a coaxial cable and the 50 ohm resistor serves as a matched back termination for the generated voltage pulses [80]. Figure 3-10(b) shows the PSPICE simulation results for SPAD lumped model where $R_j = 5$ kΩ obtained from the slope of IV characteristics in the Geiger mode region (Figure 3-9(b)) and C_j is 7.47 pF, which is the result of three capacitive components in parallel: SPAD capacitance = 0.17 pF, the microprobe (C_{probe}) $\approx$ 0.3 pF and capacitance and the capacitance of the coaxial cable (C_{coax}) $\approx$ 7 pF. The lumped model is not expected to model the rise and fall values of avalanche accurately as they occur on a much shorter time scale [99]. The parsitic capacitance from the cathode to the substrate is neglected as $C_{CS} \ll C_j$ where as the anode to substrate parasitic capacitance (C_{AS}) is grounded following the anode connection.

[1]Worth noting that PSPICE simulation of this voltage controlled switch uses a model that specifies two threshold values for control, which is the voltage connected across R_j in SPAD lumped model,: V_{off} at which the switch turns off and V_{on} at which the switch conducts current. The first is set to 0 while the latter is set to equal the product ($I_{avalanche,\ max}\ R_J$). The maximum value of $I_{avalanche}$ is obtained from SPAD IV measurements at V_{OB}=26 V and is $\approx$ 0.2 mA for the SPAD used in this discussion. So in away, this PSPICE model does not predict the avalanche current value but is rather informed by it



(a) (b)

Figure 4-3: SPAD lumped circuit model: (a) Arrangment suitable for active reset scheme (b) PSPICE simulation results where we vary the values of R_{reset}, R_Q and C_{AS} to study their effect, with reference to the simulation depicted in Figure 4-2(b) if we fix the resistor connected to cathode at 100 $k\Omega$ and introduced small resistance at the anode side (100 Ω) or varying the anode to ground capacitance from 1 fF to 2 nF, the AC coupled cathode voltage remains the same. When the resistor values are switched similar to the active reset circuit configuration in Figure 4-1(a) the cathode voltage is attenuated and still maintains its time constant.

Similar to the characterization experiment in Figure 3-9(a) the break down voltage and bias source in the lumped model are set at 24 V and 26 V, respectively.

Moving R_Q to the cathode terminal and introducing R_{reset} changes the quench mode to what is known as voltage mode sensing, and the reason is again apparent when this change is incorporated into the lumped model shown in Figure 4-3(a). The avalanche current now passes through the series combination of R_j and R_Q, were we to sense the avalanche from the anode side, we would be sensing some fraction of the voltage, hence the name "Voltage mode". This mode of detection is rarely used to avoid the filtering effect of C_{AS} that changes the timing of the edge of the avalanche pulse. However, in the proposed active reset scheme, the sensing is still performed through the cathode node. Because $R_{reset} \ll R_Q$ the peak of the detected avalanche pulse will be indeed reduced which is compensated by adjusting the amplifier gain, but the temporal properties of the pulse are not changed which can be verified by comparing the simulation results for each variation of cathode and anode resistors as shown in Figure 4-3(b)

4.3 Implementation of passive quenching active reset blocks

4.3.1 Pulse digital conversion: Threshold and Comparator

Figure 4-4 shows the implementation of the comparator block in Figure 4-1(a). The development of this block started by cascading Analog devices LT1711 comparator next to the OPA858 amplifier used earlier in the circuit shown in Figure 3-10 (a) in an open loop fashion. This comparator was chosen for its short propagation delay (4.5 ns). Two problems arise, first, the amplifier uses dual supply configuration where the rest of the system is set to single 5 V supply for compatibility with synchronization electronics in later deployment. This can be solved by DC-level shifting; one simple way is to capacitively coupling the output of the amplifier to a resistive divider network that defines the DC-level shift which was actually implemented in earlier trials but failed as the loading effect was not accounted for. The other way which worked well is to add a negative supply to the feedback network of the opamp. Dedicated LDO adjustable voltage source, Analog devices LT3904 was used for that purpose, with a potentiometer connected to its 'SET' pin, the value of DC shift can be tuned from 0.7 to 1 V. The reason for using negative LDO is the fact that the amplifier is configured in inverting mode for better bandwidth performance there, hence the negative voltage at the R_{F2} terminal will translate into a positive level shift.

The second terminal of the comparator is connected to a simple resistive divider, and one resistor of which is a potentiometer that gives a second knop for tuning. It was placed for convenience because the other knob, the LDO circuit, is a function of the amplifier gain governed by the R_{F1}/R_{F2} ratio so that one of the two threshold control knobs is independent. The resistor choice was made to guarantee a 500 mV tuning range that covers different counting thresholds set earlier in the characterization of SPAD (Figure 3-14 (a), (d)). The connection between the output and the negative input of the compartor is arbitrary and is chosen to convert the negative falling edge of avalanche signal to a positive rising edge that references the rest of the blocks, as shown in Figure 4-1(b).

Another issue arises when implementing the proposed circuitry on a PCB while connecting to SPAD through the microprobe, the parasitic C_{AS} that is no longer grounded due to

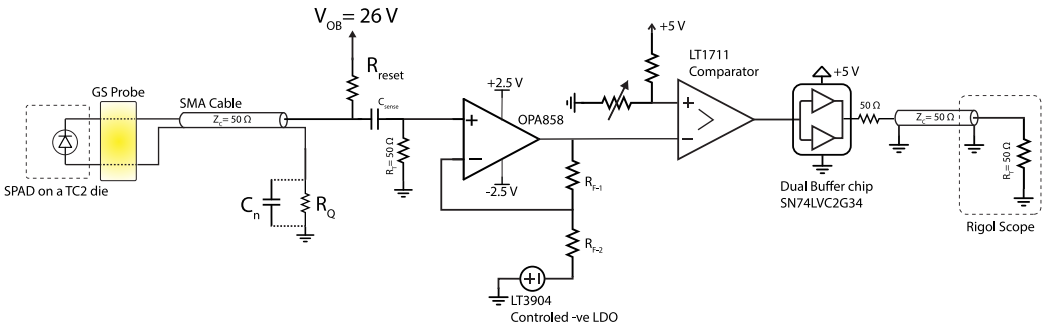
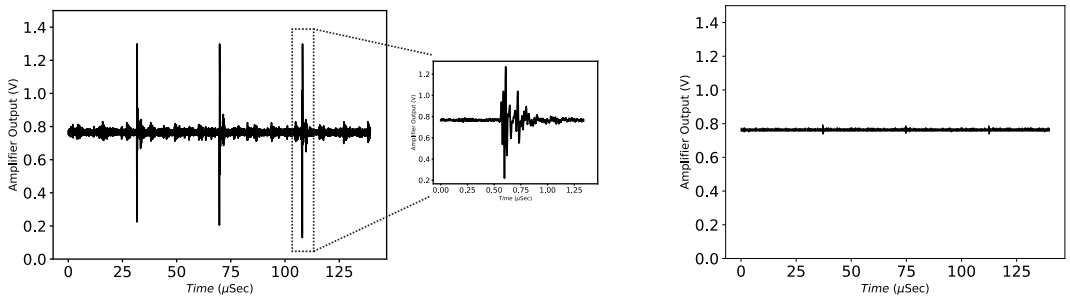


Figure 4-4: SPAD interface with LT1711 comparator

the introduction of R_Q between the anode and the ground combined with the capacitance of the coaxial termination and the self-inductance of the coaxial cable appears to exhibit ringing that is amplified, causing a periodic signal that interferes with SPAD pulses falsely triggering the comparator. This was fixed by introducing a 2 nF capacitor that filtered this ringing while maintaining the pulse characteristics of SPAD which was confirmed by the PSPICE simulation in Figure 4-3(b) where the SPAD pulses remain unchanged when measured from the cathode terminal in a current-mode measurement [2] (anode resistor R_Q $\ll$ cathode resistor R_{reset} and C_{AS} = 2 nF). This ringing signal and the effect of adding C_n on its magnitude are shown in Figure 4-5. In the wireponded version of this system, where the coaxial cable and the microprobe parasitics are removed, this ringing disappears, and eventually we discard this extra 2 nF capacitor.

Finally, the fast comparator cannot be tested directly by interfacing to a high impedance scope that will cause reflections for such high-speed transitions or a 50 ohm termination that requires drive current capability greater than 20 mA which is the current drive limit of LT1711; therefore, a dual channel buffer, Texas Instruments SN74LVC2G34, was used where combined channels, as the connection shows, can provide up to 100 mA load driving capability. This chip introduces a propagation delay of 4 ns, but it does not contribute to the total system delay, as it only buffers the output, and the comparator itself is what drives the next stage (whether it is the hold-off circuitry or the reset pulse generator). Event counts are registered through the output terminal of this buffer. Figure 4-6 shows

[2]For this simulation R_Q is 100 Ω, if that value increases to few kilo ohms the shape of the SPAD pulse changes, which is expected as this filter corner frequency increases



(a) (b)

Figure 4-5: Noise induced by the GS probe connection as seen at the amplifier output (a) Noise appears periodically (b) Noise magnitude reduced by introducing C_n, see schematic in Figure 4-4

the output of this block over two different time intervals.

4.3.2 Reset Pulse Generation Using Data Flip Flop (D-FF)

To realize the clocked operation of generating reset pulses at the negative edge of the comparator pulse, the Texas instruments SN74AUC1G74 D-FF was used with RC feedback network tying the complemented output $\overline{Q}$ to the 'data clear' input $\overline{CLR}$. This connection is shown in Figure 4-7(a). Inset (b) of the same figure explains the operation principle of this circuit by assuming an initial state of low state output at Q, naturally this means high state at $\overline{Q}$ where C_{pulse} is fully charged consequently, $\overline{CLR}$ pin is inactive as it is connected to high logic voltage. Once triggered, both Q and $\overline{Q}$ switch states, which in turn creates a discharging path for the capacitor through R_{pulse} having its terminal connected to low logic voltage. Once the voltage drops below the threshold voltage of the D-FF, the $\overline{CLR}$ pin resets the D-FF to its initial state where Q drops to zero volt and $\overline{Q}$ rises to a high logic voltage thus charging the capacitor again. This process repeats at each positive edge trigger. The time duration at which C_{pulse} discharges, which is governed by the time constant $\tau = R_{pulse}C_{pulse}$ determines the duration of the reset pulse. This timing is explained graphically in Figure 4-7(b). With the $R_{pulse} = 5$ kΩ and $C_{pulse} = 22$ pF we expect the generated pulse to have a width[3] $\approx 2\tau$, 220 nsec. This is more or less what we get when we look at the pulse

[3]In RC circuit a charged capacitor dissipates more than 70% of its charge through R in 2τ sec

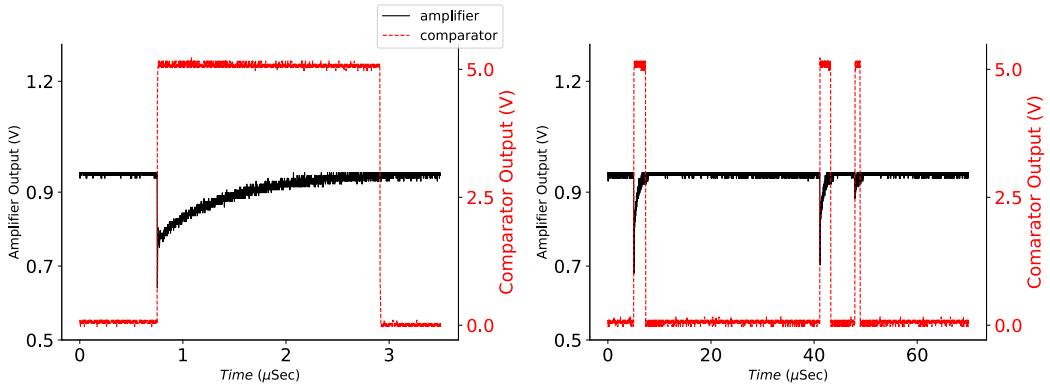
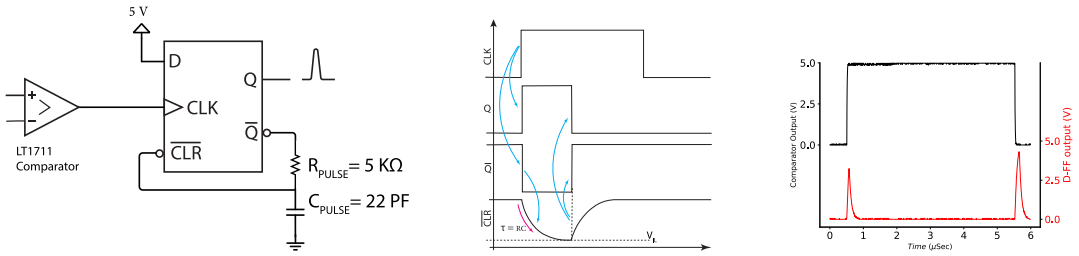


Figure 4-6: Oscilloscope traces of output of comparator circuit buffered using a dual buffer chip terminated a 50 Ω channel as shown in Figure 4-4, with reference to the same figure: R_{reset} = 100 KΩ, R_Q = 100 Ω, C_n = 2 nF, R_{F1}/R_{F2} = 1 kΩ/ 100 Ω. Comparator threshold is set to 25 mV and the operational amplifier output is DC shifted to 0.95 V (a) one passively quenched pulse (b) series of pulses

Full Width at Half Maximum (FWHM) value in the oscilloscope trace depicted in Figure 4-7(c). Sharp edges of the reset pulse are lost due to the filtering effect of the oscilloscope probes. Better signal probing can be performed if we used the same buffering technique as was followed in the comparator circuit. Unless continuous monitoring of the reset pulse is required, this initial assessment is practically sufficient.

The smallest pulse width that can be obtained by this D-FF configuration is the result of two limitation constraints on each component of the feedback network. R_{pulse} is limited by the current value that the chip could supply which is 9 mA, which means the least value is ≈ 560 Ω. The other limitation on the capacitance is the timing limitation set on the $\overline{CLR}$ signal, which according to the data sheet is 1 ns, which means that $2\tau = 2min\{R_{pulse}C_{pulse}\}$ = 1 ns. If we use the minimum value for R_{pulse} then C_{pulse} is ≈ 1 pF. The last consideration is the excitation edge, the D-FF clock input is connected to the complemented (inverted) output of the comparator to trigger at the negative edge of detection pulse.



(a) (b) (c)

Figure 4-7: Reset pulse generation using a data flip-flop (a) Schematic diagram (b) Timing diagram (c) Oscilloscope measurements for generated pulse in response to Compartor complemented output

4.3.3 Reset Switch Implementation: Non Inverting Tri-State Buffer For Reset Function

The final block in the proposed system is the tristate buffer that switches the anode resistance in response to the reset pulse to provide a faster charging path for C_j. Using On Semi NL17SZ125 noninverting tri-state buffer where its input is always connected to ground such that when the reset pulse triggers its enable bit ($\overline{EN}$) the output connected to the anode node switches from high impedance state to 0 ohm state[4], thus creating a path for C_j to recharge to the point of excess overbias faster, if R_{reset} is chosen to be significantly smaller than R_Q. This process can be understood by examining Figure 4-8 which incorporates the equivelent resistor of tri-state buffer when enabled for the reset time duration. Upon reset and during avalanche, the SPAD current flows through series combination R_j and R_Q. During passive reset, C_j charges from V_{BD} to V_{OB} through R_Q, on the contrary, the proposed reset configuration allows it to charge through R_{reset} and if we choose $R_{reset} \ll R_Q$ we can achieve a faster reset time that satisfies the timing in Figure 4-1(b).

Figure 4-9(a) depicts the connection of the tristate buffer having its enable bit connected to the D-FF output through an inverter, which is implemented by a NOR gate , On Semi SN74LVC1G02, with one input grounded and the other to the D-FF Q pin. To test the functionality and timing of this circuitry, the output of the tri-state buffer is bulled up to

[4]We refer to it as zero ohm "state" as it is not an ideal short circuit, rather a current sink. This buffer is rated to guarantee a current sink operation up to 50 mA, which is a value much higher than the SPAD avalanche current, therefore, the assumption of very low equivalent impedance is valid

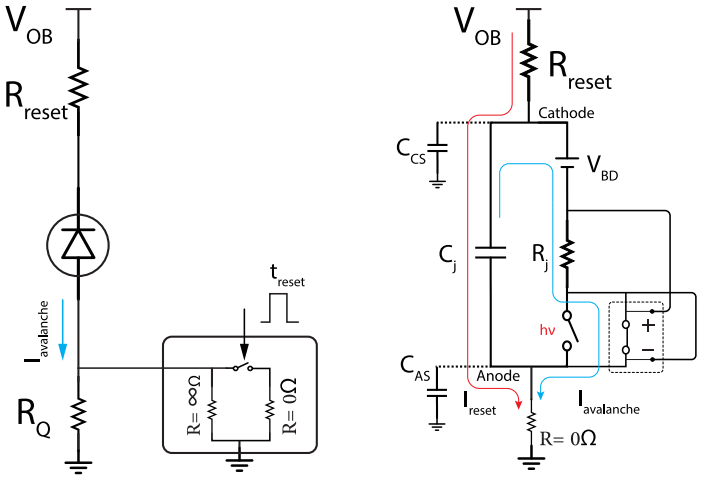


Figure 4-8: Tri-State Buffer: Reset Mechanism where the anode is shorted to ground for short time equal to t_{reset} such that the SPAD gets rid of residual avalanche current and C_j charges to excess overbias point through R_{reset}

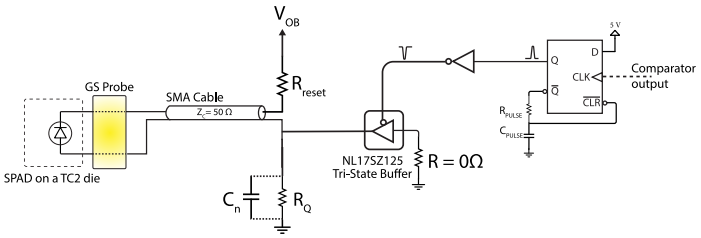
the logic high terminal through a 50 kΩ resistor. When enabled, the output switches to zero ohm, which in turn reflects on the signal going to 0 V at this time. Figure 4-9(b), (c) show this connection with the oscilloscope traces, where we can verify the correct timing performance, however, we notice the charging trace after the reset pulse duration that results from charging the capacitance of the 10 pF oscilloscope probe through the 50 kΩ pull up resistor.

4.3.4 Putting All Together: Passive Quenching/Active Reset PCB

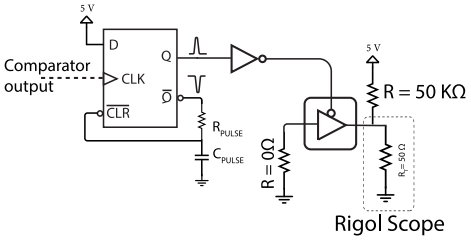
Figure 4-10(a) shows a schematic of the passive quenching active reset circuit realized using each block discussed earlier. After using the probe station setup for circuit development and verifying the functionality of each block, we eventually removed the coaxial cable and microprobe by directly wireponding the chip on the custom PCB shown in Figure 4-10(b). This indeed results in a stable system and presumably faster as we get rid of extra capacitance loading the junction capacitance and C_n added earlier to the anode node to stabilize the amplifier. The value of R_Q = 100 kΩ was decided based on the discussion in Section 3.3.2 to bias SPAD around 26 V which is the optimal point for PDP. The value of R_{reset} can be decided based on two factors: the value of excess bias and the maximum allowed current

to flow through SPAD without damaging the junction. This can be better explained by the model depicted in Figure 4-8 where the maximum current passes through SPAD when the tri-state buffer removes R_Q instantaneously from the circuit, This value is equal to $\frac{V_{OB}-V_{BD}}{R_{reset}}$. The SPAD near the channel tolerates 1 mA of continuous current, for excess bias of 1.5 V the minimum value of R_{reset} is 1.5 kΩ.

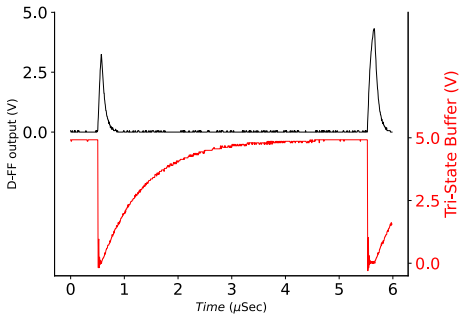
Having a fixed value for R_{reset} and C_j, which reduces from 7.47 pf to 1.4 pF after wire-bonding, sets the required value for reset pulse duration to 5 $R_{reset}C_j$ = 10.5 ns, which can be realized by a combination of R_{pulse} = 1 kΩ and C_{pulse} = 5.25 pF. In contrary to the passive quenching circuit used in Figure 3-10(a) where a 100 kΩ resistor was connected to the SPAD cathode terminal, the reduction of this value to 1.5 kΩ in this configuration will reduce the peak to peak value of the event detection pulses by nearly 70 times, which was compensated by reconfiguring the gain setting of the opamp by increasing the value of R_{F1}. Indeed this will reduce the amplifier bandwidth and a change in the LT3904 configuration resistor is made to maintain the same DC-level shifting values discussed in Section 4.3.1.



(a)

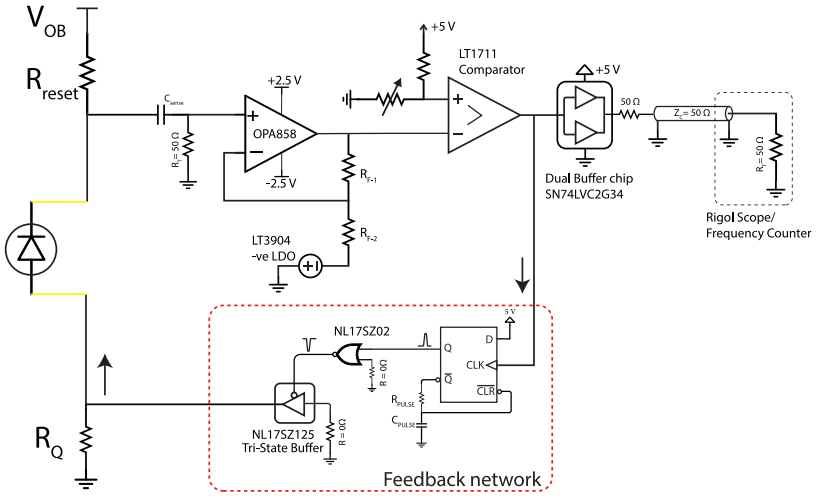


(b)

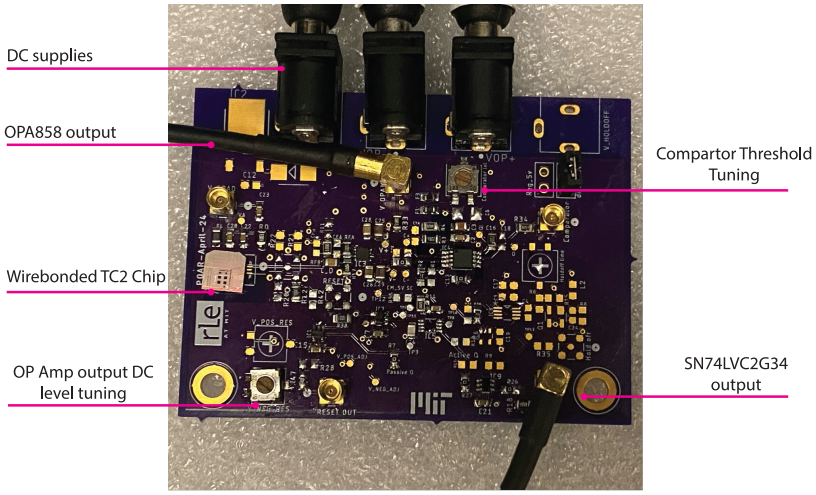


(c)

Figure 4-9: Implementation of reset switching block: (a) Schematic diagram of Tri-state buffer implementation (b) Buffer Testing circuitry (c) Oscilloscope traces for tri state buffer non-inverted enable signal vs. buffer output output showcasing the high impedance state



(a)



(b)

Figure 4-10: Passive Quenching Active Reset circuit implementation: (a) Full circuit that implements high level block diagram in Figure 4-1, yellow lines for off-chip wirebonding (b) PCB implementation with coaxial cables probing both the amplified avalanche signal and the digital output of event count signal

4.4 Results & Discussion

Results of actively resetting the SPAD are shown in Figure 4-11 obtained by probing the output of the amplifier, which was taken into account in the design of the PCB the result is in a fair agreement with the estimated dead time. Estimation of the dead time of SPAD using the active reset circuit can be performed by analyzing the propagation delay for each block in Figure 4-10. Table 4.1 lists the delay values that were calculated or obtained directly from the data sheet. The proposed circuit reduced the SPAD dead time by a factor of 150 compared to the passive reset case. The circuit works independently of V_{OB} values. It also offered flexibility in working with SPADs through probing on a chip through a coaxial cable with higher values of C_j. The dead time values compare favorably well to integrated quenching circuits, for example, work in [100] achieves a 12 ns dead time by employing a similar architecture integrated with a SPAD imager on a single CMOS die, another example in [76] which can go down to 3 ns by employing active quenching strategy. Achieving a 19.3 ns dead time with discrete components compares well with integrated structures and can be reduced by tolerating higher current values through the SPAD junction for faster reset, however, it will be challenging to use a system with such a dead time to measure the life time for fluorescent die with decay life time less than 200 ns using a time-correlated technique (10 times the detector deadtime [70]). It still serves well as a starting prototype for life-time imaging using a CMOS nanofluidic platform.

Following the discussion in Section 1.4.3, Figure 4-12 shows a cross section of one of the nanofluidic channels (channel B, refer to Figure 3-4 for annotations) which has SPAD junctions implemented beneath the nanochannel. Other variants like Channel A use stacked metal layers to act as reflectors. The active reset circuit discussed in this chapter needs to be modified by gating the dual buffer output so that it masks the counting process by the start/end trigger to implement the system depicted in Figure 1-13(c) where the

[5]That is a valid approximation for situations where transitions are very fast compared to the RC time constant of the circuit, here it is at least three orders of magnitude faster transition than 100pF $\times$ 50Ω

[6]This value is set by the D-FF feedback network

Block	Propagation delay
C_{sense} R_T section	negligible [5]
Opamp: OPA858	0.3 ns
Comparator: LT1711	4.5 ns
Data Flip Flop: SN74AUC1G74	10.5 ns [6]
Nor gate: SN74LVC1G02	2 ns
Tri-state buffer: NL17SZ125	2 ns
Total	19.3 ns

Table 4.1: Propagation delay of active reset circuit blocks

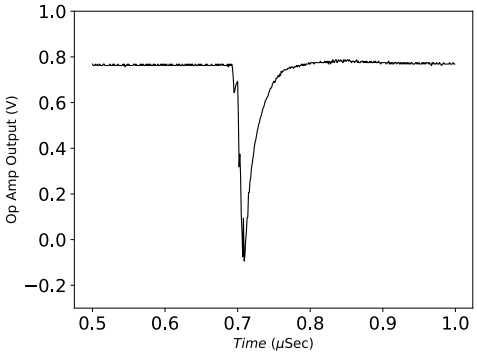


Figure 4-11: Amplifier output for actively quenched SPAD

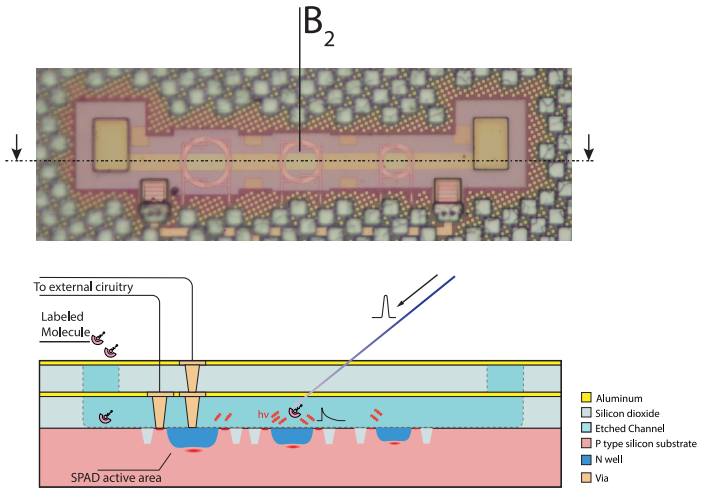


Figure 4-12: CMOS nanofluidic platform integrated SPADs in action: labeled biomolecules flowing through the nanochannel where laser pulse can excite the fluorescent label. The quenching circuit is connected externally (not all vias are shown in this cross section). Pulsed laser excite fluorescent dies and SPADs can identify the timing of photon emission

Chapter 5

Conclusion & Future work

The advances in microelectronic industry seems to offer a level of integration beyond Moore's law that ,when explored, could spur a plethora of applications such as personalized medicine tool that can tackle the single-cell proteomic challenge. In this thesis, we explore the biomolecule diffusion in tiny amounts of carrier fluid influenced by potential, which when confined in a nanopore can result in a measurable ionic current that can be tapped to identify molecules. On the same platform, an amplifier is built with careful consideration of the temporal aspects of this translocation. The system was characterized by the building of a custom PCB through which we could verify the operation of this integrated system. Each layer from nanopore to complete system attached to a PCB adds a different scheme of design challenge that we walked through both bottom-up, by utilizing multiphysics simulations and data from literature, or top-down, by building high-level blocks with design choices guided by the bottom-up approach and actual measurements performed on iterated version of the fluidic platform. There are still a number of challenges lying ahead for this platform that are left for future work, for example: fluidic packaging with a wiredbonded chip on a PCB, the relatively large pore and its implication, the use of packaged version of the platform to measure a flourescently labeled molecules.

The exploitation of optical detection by building an integrated CMOS SPAD was introduced with emphasis on effect of RIE post-processing on SPAD performance. Two custom PCBs

were built to interface with this detector. The new junction proved a photon detection efficiency that potentially fits FLIM schemes, adding a modality to the nanofluidic platform with zero change in the fabrication techniques.

Future work will further expand on those chip-to-world problems, in addition, refining integration techniques by optimizing the placement of channels and chip active area with respect to the efficient packaging to ensure functionality and efficiency. Integration of a SPAD active quenching and reset system is also planned to explore more fluorescent dies. This should position the platform for in-depth clinical validation for transitioning from a prototype to a practical application. By addressing these future directions, the CMOS nanofluidic platform can be evolved into a more robust tool, potentially revolutionizing how molecular diagnostics are performed and contributing to the advancement of personalized medicine. The integration of various sensing modalities and the refinement of the platform can open new avenues for research and application, making precise and real-time diagnostics more accessible and impactful.

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