

A PORTABLE EKG RECORDING SYSTEM

WITH DELAY BUFFERING

by

Peter A. Bonee, Jr.

Submitted in Partial Fulfillment

of the Requirements for the

Degree of Bachelor of Science

at the

Massachusetts Institute of Technology

May, 1979

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ABSTRACT

A portable EKG recorder has been designed which allows the tape recording of EKG waveforms, beginning with waves which occurred 32 seconds prior to the start of the recording process. The device is intended to be used by ambulatory patients who experience occasional, transitory symptoms which are thought to be possibly arrhythmia-related.

The analog EKG input is amplified and converted to 8-bit digital samples at a sampling rate of 250 Hz. Samples from the past 32 seconds are saved in a low-power 64K CCD shift-register type memory. The memory therefore provides a delay buffer for data to be recorded. Upon initiating the recording process, data is recorded in digital form, using PM encoding, on a miniature cassette recorder. The necessary playback electronics are also contained within the unit, so that playback by the physician is possible on existing EKG machines.

A prototype unit was built and tested using a commercially available miniature cassette recorder and common CMOS logic devices. The measured frequency response is flat ± 3 db from 0.16 Hz to 36 Hz, with no visible distortion in the playback waveform. Dimensions are 7-1/4 by 5-1/4 by 2-1/2 inches and the weight, with batteries, is 3 pounds, 5 ounces.

Thesis Supervisor: Dr. Stephen K. Burns

Title: Technical Director, Biomedical Engineering Center
for Clinical Instrumentation

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INTRODUCTION

The Medical Problem

Some alterations in the normal rhythm of the heart, known as arrhythmias, are believed to be significant indicators of heart disease.¹ Much interest has been expressed in the monitoring of arrhythmias in ambulatory patients. It is believed that the identification and treatment of arrhythmias in the population at large will reduce the incidence of fatal arrhythmias, which result in sudden deaths.²

The electrocardiogram (EKG) is a useful tool in the identification of patients with arrhythmias which may be manifestations of serious heart disease. However, such arrhythmias often occur infrequently and aperiodically. The recording of these low-probability events may require the continuous recording of a patient's EKG for an extended period of time and a careful search through the collected data for irregular activity.

Of particular concern in this thesis are infrequent arrhythmias which are associated with recognizable symptoms such as palpitations, dizzy spells, or chest pains. Such symptoms, though seldomly occurring and transitory, can alert the patient to the occurrence of the arrhythmia. It would be desirable, therefore, to allow the patient to initiate an EKG recording upon experiencing the symptom which is thought to be associated with abnormal heart function. To be useful to the

physician, the data collected would have to include the preliminary events which occurred before recording was started. A portable device which allows the recording of EKG data, starting with data which occurred about 30 seconds prior to the initiation of the recording process, is the subject of this thesis.

The Underlying Physiology

This section is not intended as a thorough discussion of the electrical activity of the heart, but rather as a very brief tutorial on the origins and significance of the EKG potentials on the body surface.

The heart intrinsically generates an excitation wave of electrical energy known as the action potential.³ The action potential propagates through heart tissue controlling muscle contraction. Normally, this excitation wave originates in a specialized group of cells in the upper portion of the right atrium known as the sinoatrial node. The sinoatrial node is often referred to as the primary pacemaker.¹ The action potential initiated by the sinoatrial node causes the atria to contract. At the same time, this action potential propagates to the atrioventricular node, a specialized group of cells which forms the conducting bridge between the atria and the ventricles.³ The action potential's propagation is slowed as it traverses the atrioventricular node. But the action potential is then rapidly conducted along the conducting

system of the ventricles, causing them to contract.

The mechanism by which this action potential propagates is the depolarization and subsequent repolarization of the myocardial (heart muscle) cell membranes. Consider the interface between a depolarized cell and a polarized cell shown in Figure 1.

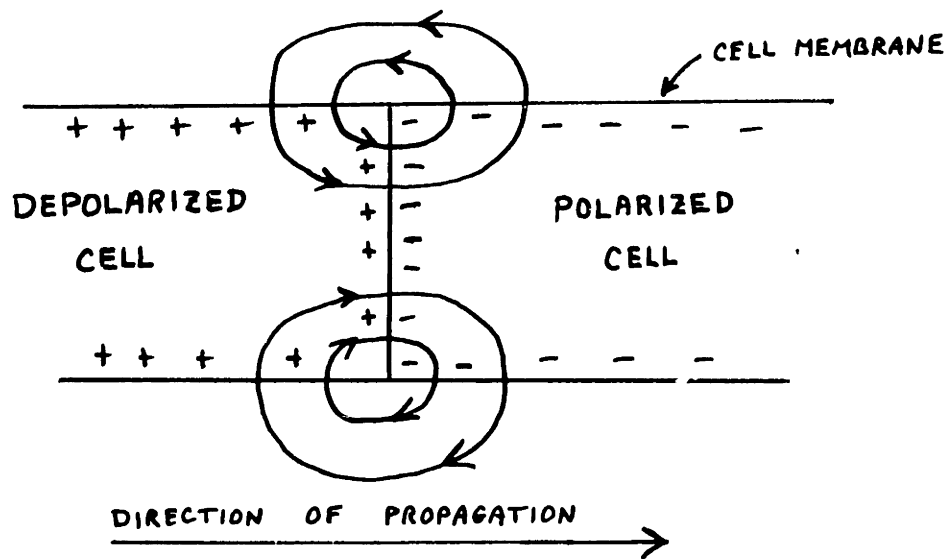


Figure 1: Propagation of Action Potential³

The potential difference at the interface gives rise to currents in the surrounding conducting medium. These currents are responsible for depolarizing the still-polarized membrane, thus causing the action potential to propagate. Since no net charge is produced by these currents, the current loops all close on themselves.

$$\bar{\nabla} \cdot \bar{J} = 0 \quad (1)$$

Each such interface between a depolarized cell membrane and a polarized cell membrane can thus be thought

of as a current dipole with a dipole moment vector pointing in the direction of propagation of the action potential. The vector summation of all such dipole moments corresponding to all the active myocardial cells of the heart is known as the heart vector. The magnitude and direction of the heart vector, as a function of time, describes the electrical cycle of the heart. As a result of the current density \bar{J} , described by the heart vector, an electric field is set up in the body. If we assume the body to be a linear isotropic medium with conductivity σ , then we can express the electric field and its corresponding potential gradient as a function of the heart vector.

$$\bar{J} = \sigma \bar{E} = -\sigma \bar{\nabla} \phi \quad (2)$$

By combining equations (1) and (2), Laplace's equation is obtained for the potential ϕ within the body.

$$\nabla^2 \phi = 0 \quad (3)$$

By solving Laplace's equation for ϕ as a function of position, the EKG potentials at different electrode positions can be obtained. One simplifying assumption which is often made is to consider the body surface as a sphere surrounding a current dipole described by the heart vector. By making such an approximation and specifying the appropriate boundary conditions, Laplace's equation can be solved for ϕ as a function of position. This model for the generation of body potentials forms

the theoretical basis of electrocardiography.

The electrocardiogram measures actual potentials on the body surface as a function of time. One cycle of a typical electrocardiogram pattern is sketched in Figure 2. On the same time scale, the corresponding variations in heart chamber volumes and pressures are sketched. The first peak seen in the cycle is known as the P wave and is present during the depolarization of the atria. During the PR interval which follows, the action potential is passing through the atrioventricular node. The waves which occur next are known as the QRS complex, and indicate depolarization of the ventricles. The remaining peak, known as the T wave, occurs when the myocardial cells of the ventricles become repolarized, in preparation for the next cycle.

The EKG is an important diagnostic tool because it allows the identification and analysis of arrhythmias. Arrhythmias usually indicate an abnormality in the generation or conduction of the action potential. The abnormality is often due to an "irritable" focus within the heart which generates an action potential of its own without being triggered through the normal conduction system. Such conditions may have connotations of serious consequences, and their presence justifies a careful search for heart disease.¹

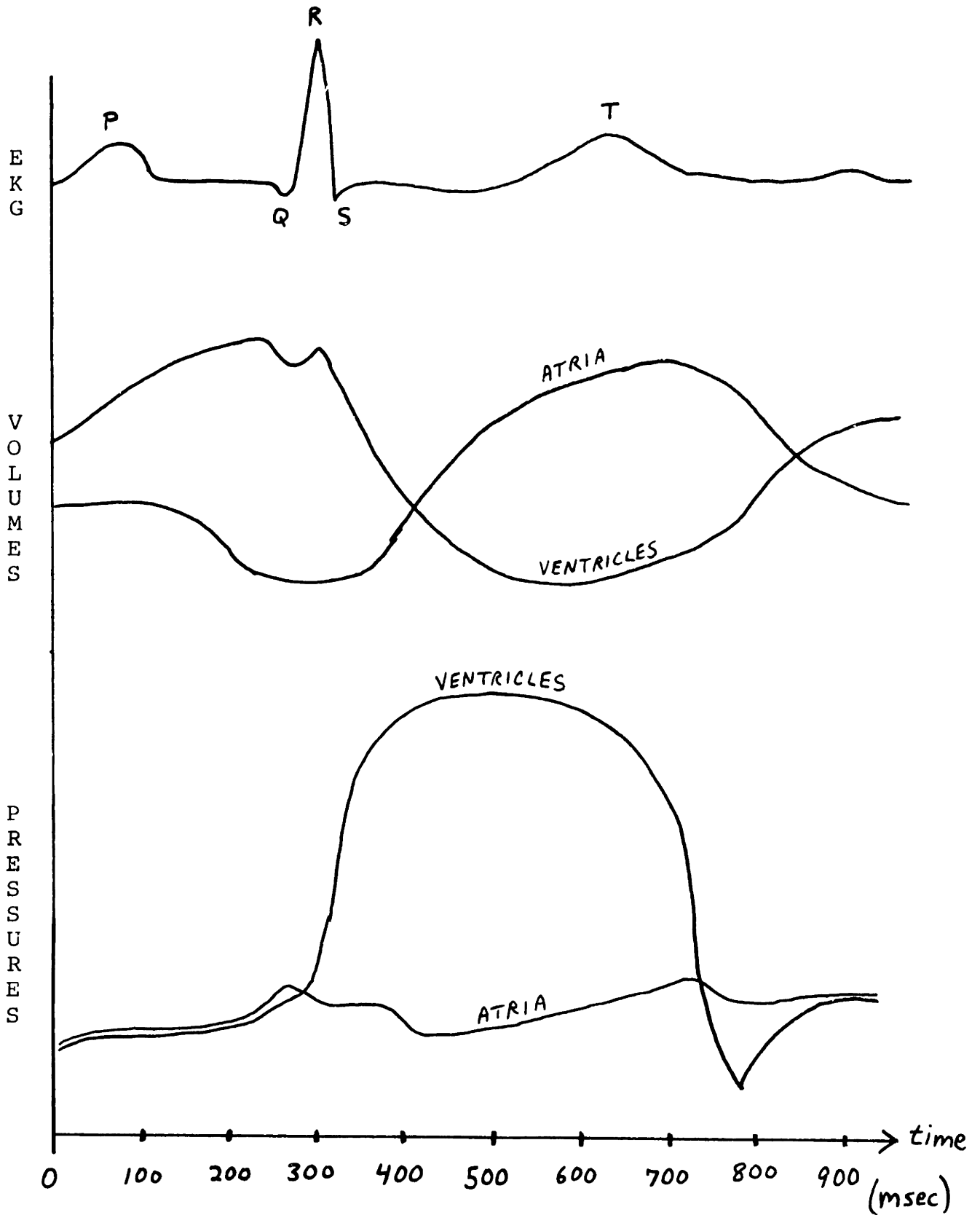


Figure 2: The Cardiac Cycle³

Present Technology

Currently, there exist two popular mechanisms for portable EKG monitoring. One mechanism provides a continuous 24-hour recording for later analysis and the other mechanism provides real-time analysis of the EKG with the capability of storing short waveform segments. Each of these efforts has been shown to be useful in the identification and analysis of arrhythmias in ambulatory patients. Some of the advantages and costs of each of these systems are summarized in this section.

The most popular system in use is a small, battery-operated tape recorder which continuously records EKG signals for a period of 24 hours. The tapes, known as Holter recordings, are later played back and analyzed by technicians on high-speed playback equipment. The typical result of the analysis is a statistical summary giving hourly counts of normal beats and irregular beats, trend recordings of heart rate and ST segment levels, and actual EKG waveforms showing the arrhythmias.⁴

The largest single problem with Holter recordings is one of cost. A very large investment is required in the high-speed playback equipment, and technicians are needed to perform the playback analysis and summarize their findings. This high cost prohibits the widespread use of the system by individual physicians. Other disadvantages are the possibility of errors in the analysis of the tapes by technicians and the limiting of recording

time to 24 hours.

A more recent innovation is the use of microprocessor technology to continuously monitor the ambulatory patient's EKG signal and maintain summaries of irregular activity in memory for later retrieval.⁵ An advantage of this system is its ability to provide real-time analysis of the signal and alert the patient to the occurrence of an arrhythmia.

Note, however, that this system only responds to heartbeats which its algorithm identifies as being irregular. In some cases, it would be more desirable to allow the patient to record segments of EKG data whenever an unusual symptom appeared such as palpitations or dizziness. Then, playback of the recorded segments by a physician would show conclusively whether there was any arrhythmia associated with the symptom. Other possible disadvantages of a microprocessor-controlled arrhythmia monitor are the difficulty of storing any appreciable length of EKG signal, the battery drain of the processor, and cost.

The goal of this thesis has been the development of a portable EKG recorder which is well suited to the problem of identifying and analyzing arrhythmias in patients who complain of occasional symptoms which may be arrhythmia-related. The system which was developed is described in the remainder of this thesis.

THE PORTABLE EKG RECORDER WITH DELAY BUFFERING

System Design Goals

The purpose of this device is to provide a means of reliably recording EKG signals corresponding to periods of time when a patient notices symptoms which may be indicative of abnormal heart function. In order to be useful, the recordings should include EKG signals from at least several seconds before the symptoms were noticed and recording was initiated. Thus, some type of delay buffering is necessary for incoming data being presented to the recorder. Providing this delay, while being constrained by other considerations such as portability, was the central issue in the design of the system.

Power consumption was another important consideration. Since the device will typically be used by one patient for a day or two, in an effort to record low-probability occurrences of arrhythmias, the device must have a battery lifetime of at least 24 hours. A much greater battery lifetime would be desirable. This device has an inherent advantage over 24-hour Holter recorders and the portable processor approach in that only the input circuitry and the delay buffer need be operated continuously; no power is continuously consumed by a tape drive or processor. The ultimate power consumption goal, then, has been to develop a device whose battery lifetime exceeds both that of the Holter recorder and that of the portable processor.

As with any portable system, the device's size and weight are important considerations. For the initial prototype unit, a goal was to design the device no larger than a typical portable cassette recorder (7" x 5" x 3") and to keep the weight of the unit below 5 pounds. A tradeoff between battery power and the device's weight and dimensions was recognized early in the design process.

Further requirements exist if the portable EKG recorder is to be used as a diagnostic tool. A flat frequency response from approximately 0.5 Hz. to 50 Hz. is required of most present portable EKG equipment.⁶ The recorded waveform should be reproducible with no apparent distortion to the rate or morphology of the waveform.

Finally, it would be most desirable for the physician to be able to play back the recordings on existing EKG equipment.

Design Procedure

This section gives a brief chronological account of the design process. A detailed hardware description follows in the next section.

Figure 3 shows a block diagram of the EKG recorder with delay buffering. The input signal is amplified and then digitized. The resulting samples are stored in sequential locations in a digital memory. As the memory is filled with data, the least-recent samples are taken out and applied to the tape recorder interface input. The

tape recorder therefore records data starting with samples from before the recording process was initiated. When data is later played back, the samples are used to reconstruct the analog signal.

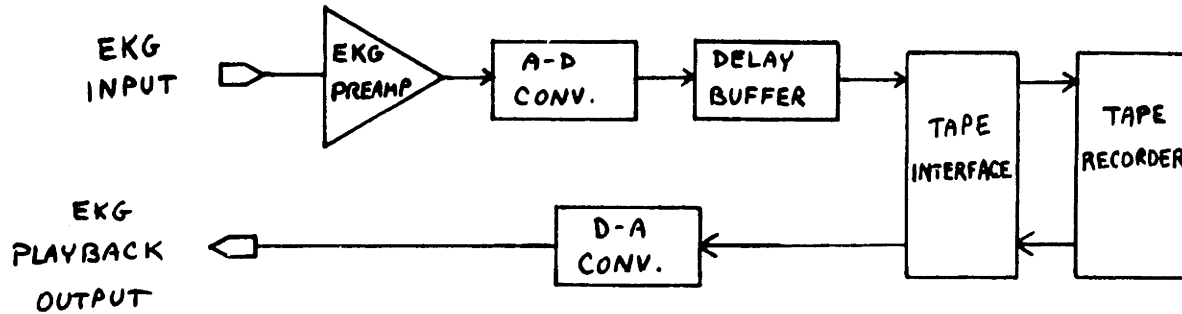


Figure 3: System Block Diagram

Since the specific implementation chosen for the delay buffer may dictate such design variables as the data word length, sampling rate, and tape interface operation, its design is central to the system design process. A memory was desired which would accommodate as much data as possible, yet operate with low power consumption. A further desire was to use a single integrated circuit memory.

The specific device chosen was a Texas Instruments TMS3064 charge-coupled device memory.⁷ This is a dynamic memory with a block-addressable serial organization. The specified power dissipation is only 25 milliwatts when no read/write operations are taking place. A continuous

two-phase clock is required.

The TMS3064 contains 16 addressable 4K shift registers. All 16 shift registers are constantly recirculating data, except during a read/write operation. During such an operation, a single bit may be read from or written into the addressed shift register; the other 15 shift registers simply recirculate their data. One of these read/write operations may take place per clock cycle.

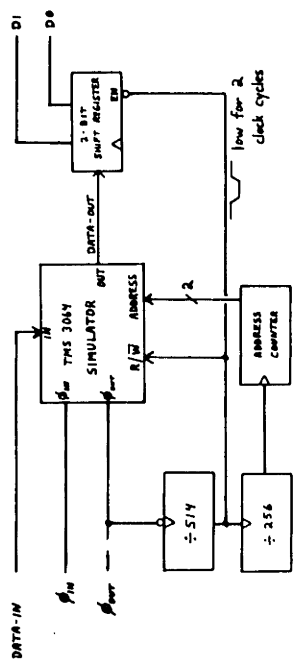
In order to more fully understand the TMS3064 memory a model was designed and constructed using commonly available logic devices. Due to the complexity of the TMS3064, as well as its scarcity and high cost, the design and use of this model was a valuable exercise. The logic diagram for this "TMS3064 simulator" is shown in Figure 4.

The memory device used in the simulator is a National Semiconductor MM5016.⁸ Note that this is a scaled-down model with only 4 shift registers, each 512 bits long. However, the simulator accepts clock and control signals analagous to those used by the TMS3064, and the structure of the simulator accurately reflects the internal organization of the TMS3064. The relevant timing information for the simulator also appears in Figure 4. During a given clock cycle, a single bit may be read out of the addressed shift register, and a single bit may be written into the addressed shift register. During this clock cycle, the data in the other shift registers is simply recirculated.

TMS 3064 SIMULATOR

LOGIC DIAGRAM

2-BIT WORD DELAY SYSTEM



TIMING DIAGRAM

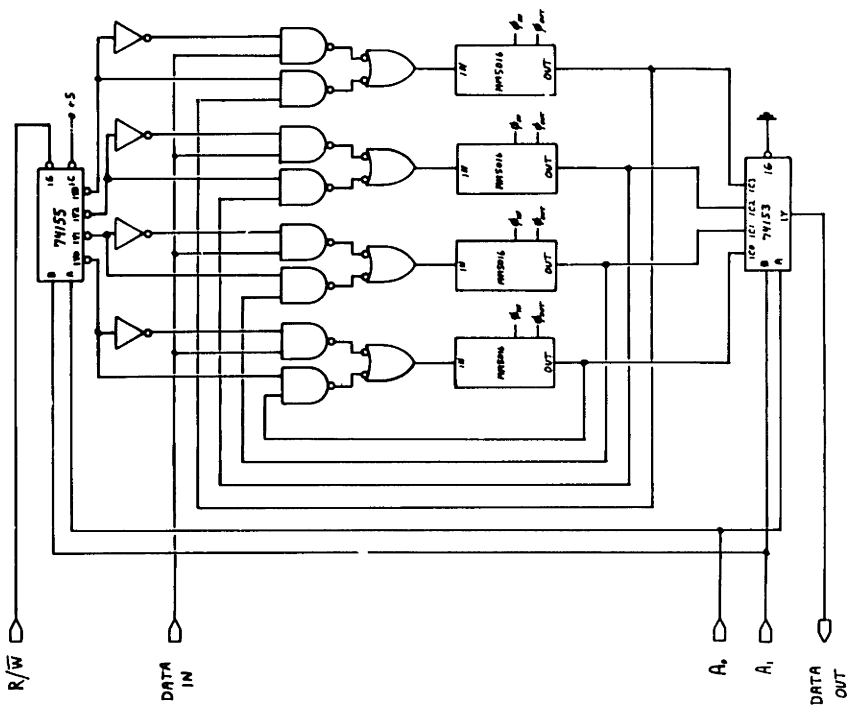
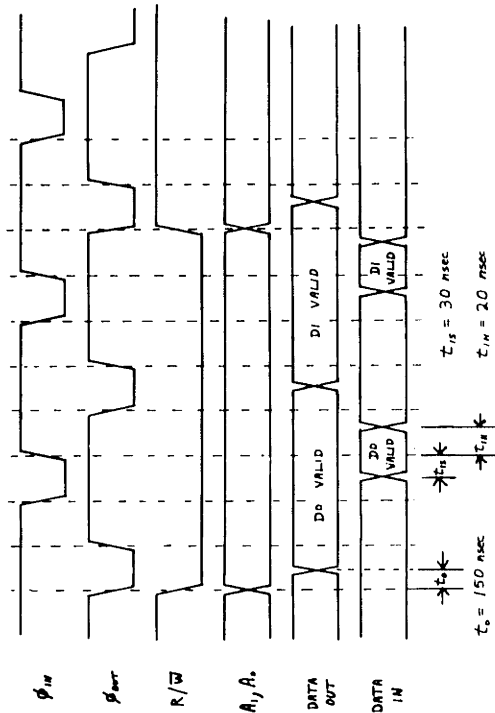


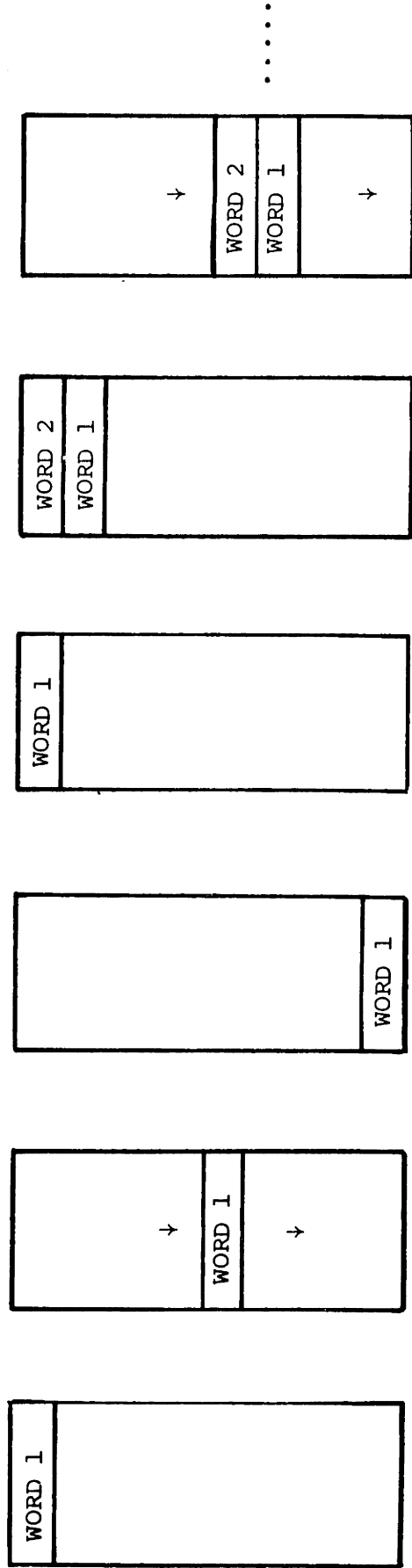
Figure 4

Another use of the TMS3064 simulator was in demonstrating the feasibility of using a shift register memory system as a delay buffer for data. The simulator was used as the memory element in a 2-bit word, 1K long data delay system as shown in the system block diagram of Figure 4. Every 514 clock cycles, a new data word was entered into the addressed shift register. Each data word was presented to the simulator input as a serial "burst" of 2 bits. Figure 5 illustrates this. After filling each shift register with 256 data words, a new shift register was addressed and filled in a similar manner, and so on. Thus, a total of 1K 2-bit words were accommodated. Prior to writing each bit into the simulator, the bit already occupying the bit position at the output of the addressed shift register was shifted into a separate 2-bit shift register.

We can calculate the number of clock cycles required to fill the entire simulator with data:

$$514 \times 256 \times 4 = 526,336$$

Therefore, the 2-bit output register always contained data presented to the data input 526,336 clock cycles ago. At a clock frequency of 526,336 Hz, for example, a delay of exactly 1 second was implemented. Data words were stored in and retrieved from the delay buffer every 514 clock cycles. In a delay system where the data represents samples of analog data, this would mean that the sampling



After 2 clock cycles After 256 clock cycles After 512 clock cycles After 514 clock cycles After 516 clock cycles And so on ...

FIGURE 5: Filling 512-bit Shift Registers with 2-bit Words

rate would have to equal the clock frequency divided by 514.

This exercise demonstrated the suitability of the TMS3064 CCD memory for delaying EKG data. When the TMS3064 is clocked at 1 Mhz and filled with 8-bit samples in the manner described above, a delay of approximately 32 seconds results. This is quite adequate for the portable EKG recording system. Since it takes approximately 4 milliseconds for 8-bit data bursts to circulate once through a 4K shift register at a clock frequency of 1 MHz, a new sample is required every 4 milliseconds. The required sampling rate is therefore 250 Hz. According to the sampling theorem, this rate is adequate since the EKG spectrum of interest lies below 50 Hz.

Keeping these considerations in mind, the design of the EKG preamplifier and analog-to-digital converter was relatively straightforward. The EKG preamplifier is required to amplify signals on the order of 1 millivolt peak-to-peak to a level suitable for accurate A-D conversion, while eliminating DC offsets characteristic of skin electrodes.⁶ The preamplifier also must have a differential high-impedance input and a high common-mode rejection ratio, and should include sufficient low-pass filtering to prevent aliasing. A circuit which meets these requirements was designed and built using commonly available operational amplifiers.

An 8-bit analog-to-digital converter was desired which required a minimum number of external components and a minimum of power. A commercially available monolithic charge-balancing A-D converter, the Teledyne 8703, was chosen.⁹ This device uses complementary MOS technology for low power consumption and requires only passive support components. The dynamic range available using 8-bit samples can be calculated as follows:

$$\begin{aligned} \text{dynamic range in db} &= 20 \log \frac{V_{\max}}{V_{\min}} \\ &= 20 \log 2^8 \\ &= 48 \text{ db} \end{aligned}$$

Another major design consideration was the choice of a tape recording scheme. The recording of digital information on a commonly available miniature tape recorder requires interface hardware. On the other hand, the recording of EKG signals in analog form requires either a tape recorder with a low-frequency response flat to below 1 Hz or a means of modulating a higher-frequency audio carrier signal with the EKG signal.

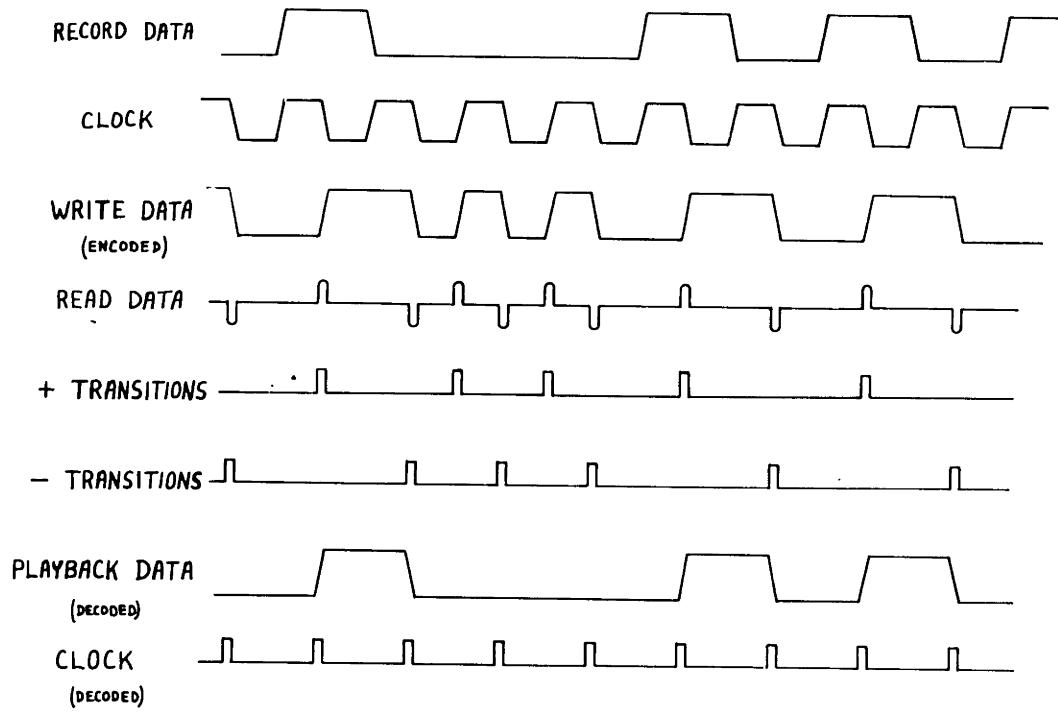
A digital tape recording scheme was chosen for its simplicity and freedom from adjustments. With properly calibrated A-D and D-A converters and a properly operating digital tape interface, the recorded and reproduced waveforms should be identical regardless of tape recorder

level adjustments, tape head adjustments, and tape noise. Furthermore, the additional hardware required for a digital tape interface is relatively straightforward and can be implemented with low-power CMOS logic.

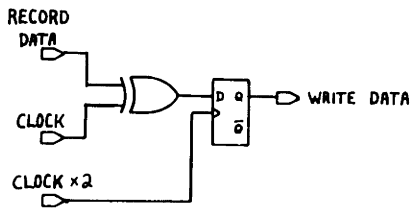
The specific digital recording standard chosen was the phase modulation (PM) or "Manchester" standard.¹⁰ PM recording encodes both the data and a corresponding clock signal into a square wave with a varying duty cycle. Figure 6 illustrates this technique. Logic circuits which perform the encoding and decoding are shown. The encoder generates a square wave with transitions occurring at frequencies of f_0 and $2f_0$ only, where f_0 is the data rate. This square wave signal is written onto the tape in the form of magnetic flux. When the tape is played back, a voltage proportional to the time derivative of flux detected by the tape head is present at the audio output jack of the tape recorder. Thus, a tape containing a square wave signal causes "impulses" of alternating polarity to appear at the recorder output jack when it is played. These positive-going and negative-going pulses may be converted to logic-level signals (+T and -T, respectively) and applied to the decoder shown in Figure 6 to recover the original data and clock.

The timing diagram in Figure 6 illustrates the encoding and decoding process for a sample data stream. Note that the encoded signal always has transitions at least once per bit time, even if the data bits do not

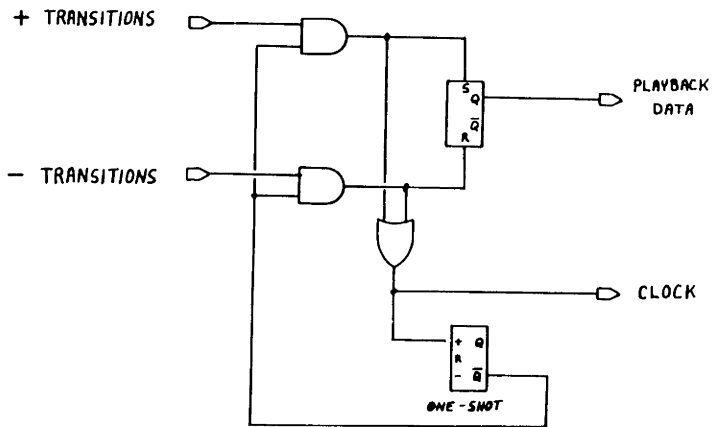
BI-PHASE (MANCHESTER) RECORDING



ENCODER



DECODER



One-shot duty cycle is $\frac{3}{4}$ bit time.

Figure 6

change. Therefore, it is possible to utilize the AC-coupled amplifier stages of the tape recorder without modification, as long as f_0 and $2f_0$ are within the frequency response range of the tape recorder.

A commercially available miniature cassette recorder was sought to provide the tape recorder function. A Sony model TC-150A cassette recorder was chosen for the prototype unit because of its small size and good performance.

The remaining block in Figure 3, the digital-to-analog converter driving the output, was implemented using an Analog Devices AD7520.¹¹ This is a low-power monolithic D-A converter using CMOS technology. It was decided that a high-level output and an EKG-level output should both be provided to allow playback on existing EKG machines as well as other devices.

Detailed Hardware Description

In this section, a detailed description of the portable EKG recorder's hardware is presented. Integrated circuits will be designated by their identification numbers, i.e. U28. A listing of integrated circuits by their identification numbers appears in Appendix A.

Figure 7 is a schematic diagram for the EKG preamplifier, A-D converter, delay buffer and associated control logic. The signal from the EKG electrodes is connected to the input of U25 via the front-panel connector J1. U25

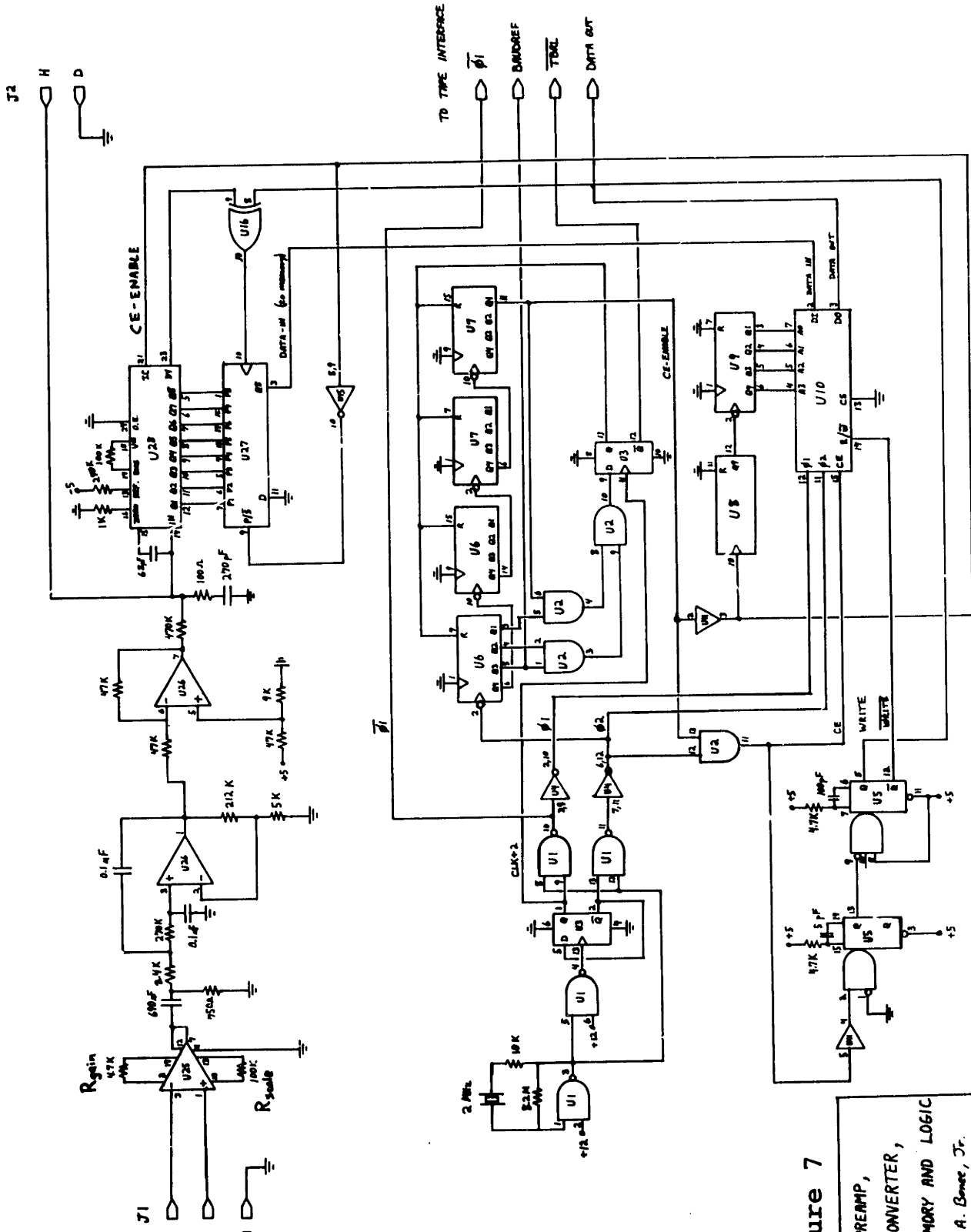


Figure 7

EKG PREAMP,
A/D CONVERTER,
BUFFER MEMORY AND LOGIC

Peter A. Bomer, Jr.

April, 1977

is an Analog Devices AD521 instrumentation amplifier providing a gain of approximately 20.¹¹ The gain of this amplifier is controlled by the ratio of the resistors R_{scale} and R_{gain} .

The output of U25 is AC-coupled to the following stage to eliminate the DC offset created by the chest electrodes. Since these offsets are typically in the 1 - 50 millivolt range, the amount of gain preceeding the AC-coupling had to be sufficiently small to prevent saturation.¹² This coupling capacitor and the 750 Ω resistor also provide a single-pole high-pass filter with a corner frequency of about 0.3 Hz.

U26, an LM358 dual operational amplifier, provides the remainder of the necessary amplification.¹³ The first section of U26 is connected as a two-pole active low-pass filter with a corner frequency of approximately 60 Hz and a Q of 0.79. This stage also provides the rest of the required gain. The second section of U26 provides buffering and shifts the signal so it is centered around 1 volt. The amplified EKG signal appears at pin H of connector J2 on the front panel to allow testing of the unit.

The A-D converter, U28, accepts input levels between 0 and 4.7 volts. No sample-and-hold circuit is necessary, as can be shown by the following calculation:

$$\text{maximum 1}^{\text{st}} \text{ derivative of input} = \frac{1 \text{ mV}}{.03 \text{ sec}} \quad (\text{QRS complex})$$

rated conversion time of U28 = 1.25 msec

$$\begin{aligned} \text{maximum possible error} &= \frac{1 \text{ mV}}{.03 \text{ sec}} \times 0.00125 \text{ sec} \\ &= 42 \text{ } \mu\text{volt} \end{aligned}$$

Note that this type of calculation is only meaningful for an integrating type converter. Neglecting the sample-and-hold function can be disastrous when successive-approximation type converters are used.

After each conversion, the result is strobed into a parallel-in serial-out register, U27. From U27 the data can be shifted into the memory data input upon command from the memory logic.

The two-phase clock, $\phi 1$ and $\phi 2$, is generated in the lower left-hand portion of the schematic of Figure 7. From this clock reference, two other signals necessary for read/write memory operations are generated. The chip-enable (CE) pulse and an accompanying WRITE pulse are both generated when CE-ENABLE is asserted high. CE-ENABLE goes high every 4104 clock cycles. During this time, CE and WRITE pulses will occur at the proper times to shift a new "burst" of 8 data bits into the memory. Counters U6 and U7 divide $\phi 2$ by 4104 and provide the CE-ENABLE signal. The CE-ENABLE line also initiates a new A-D conversion when it goes high.

The above process occurs 512 times before an entire shift register within the memory, U10, is filled. Therefore, the address specifying the current shift register

must be incremented on every 512 occurrences of CE-ENABLE. This is accomplished by counters U8 and U9. A timing diagram showing the interrelationships between $\phi 1$, $\phi 2$, CE-ENABLE, CE, $\overline{\text{WRITE}}$ and other signals appears in Figure 8.

During each occurrence of CE-ENABLE, 8 data bits are read out of the memory and sent to the tape interface. In addition, a control signal labelled $\overline{\text{TBRL}}$ is sent to the tape interface on the trailing edge of CE-ENABLE. $\overline{\text{TBRL}}$ tells the tape interface that the data byte is complete and should be transmitted onto the tape. Another signal, BAUDREF, is sent to the tape interface logic simply to provide a timebase from which the tape interface can derive its baud rate.

The tape interface logic is shown in Figure 9. Data from the memory is shifted into a serial-in parallel-out shift register, U14. The parallel outputs of U14 are connected to the transmitter buffer inputs of U13, a universal asynchronous receiver-transmitter (UART). When given a transmitter buffer register load ($\overline{\text{TBRL}}$) command, U13 takes in a data byte and initiates serial transmission of the data byte. This occurs at the sampling rate so a consistent spacing is maintained between data words on the tape. U13 adds a start bit and stop bit to the 8 data bits so each transmission consists of 10 bits. The serial output of U13 (TXDATA) is synchronized to the rising edge of TXCLOCK, the clock signal which sets the

SYSTEM TIMING DIAGRAM

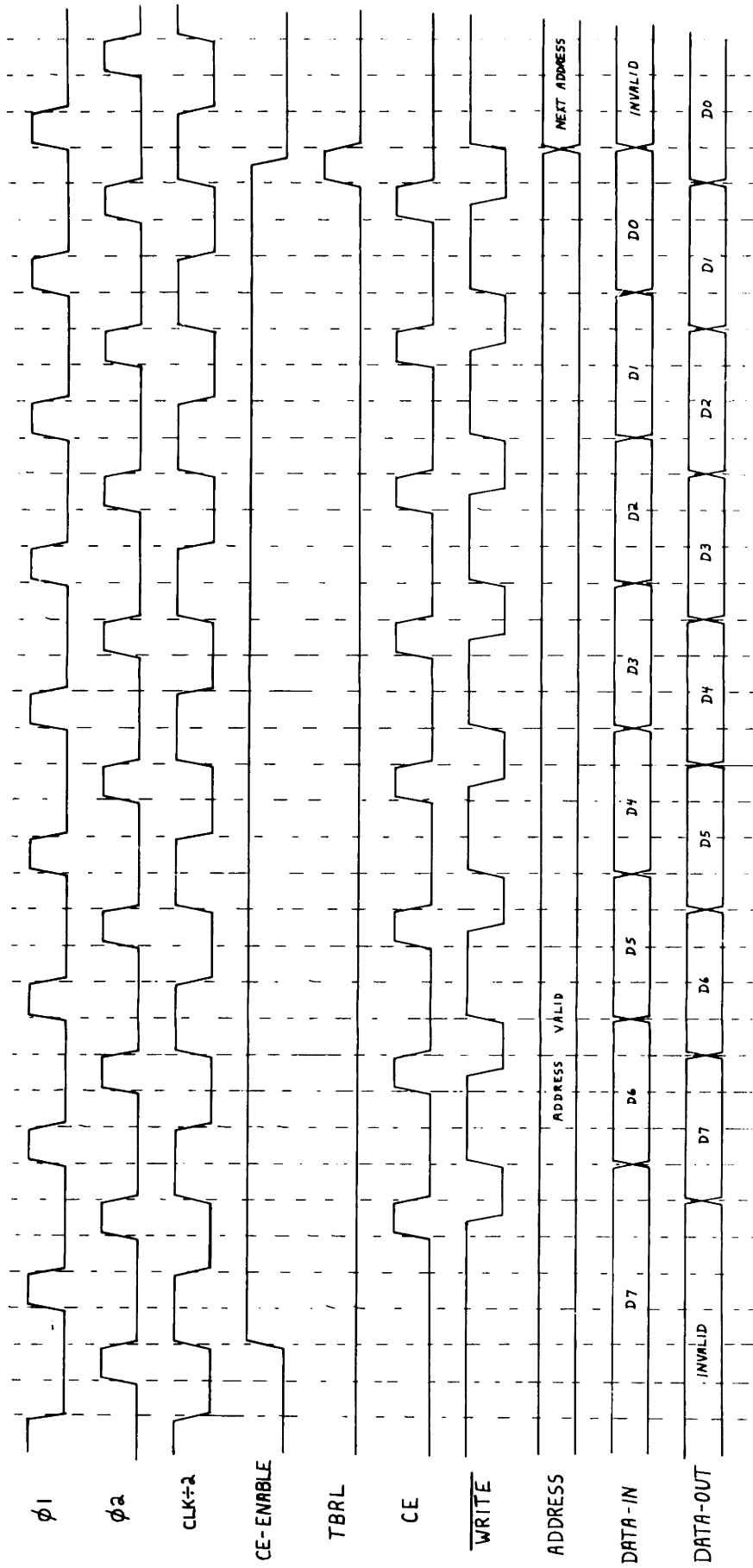


Figure 8

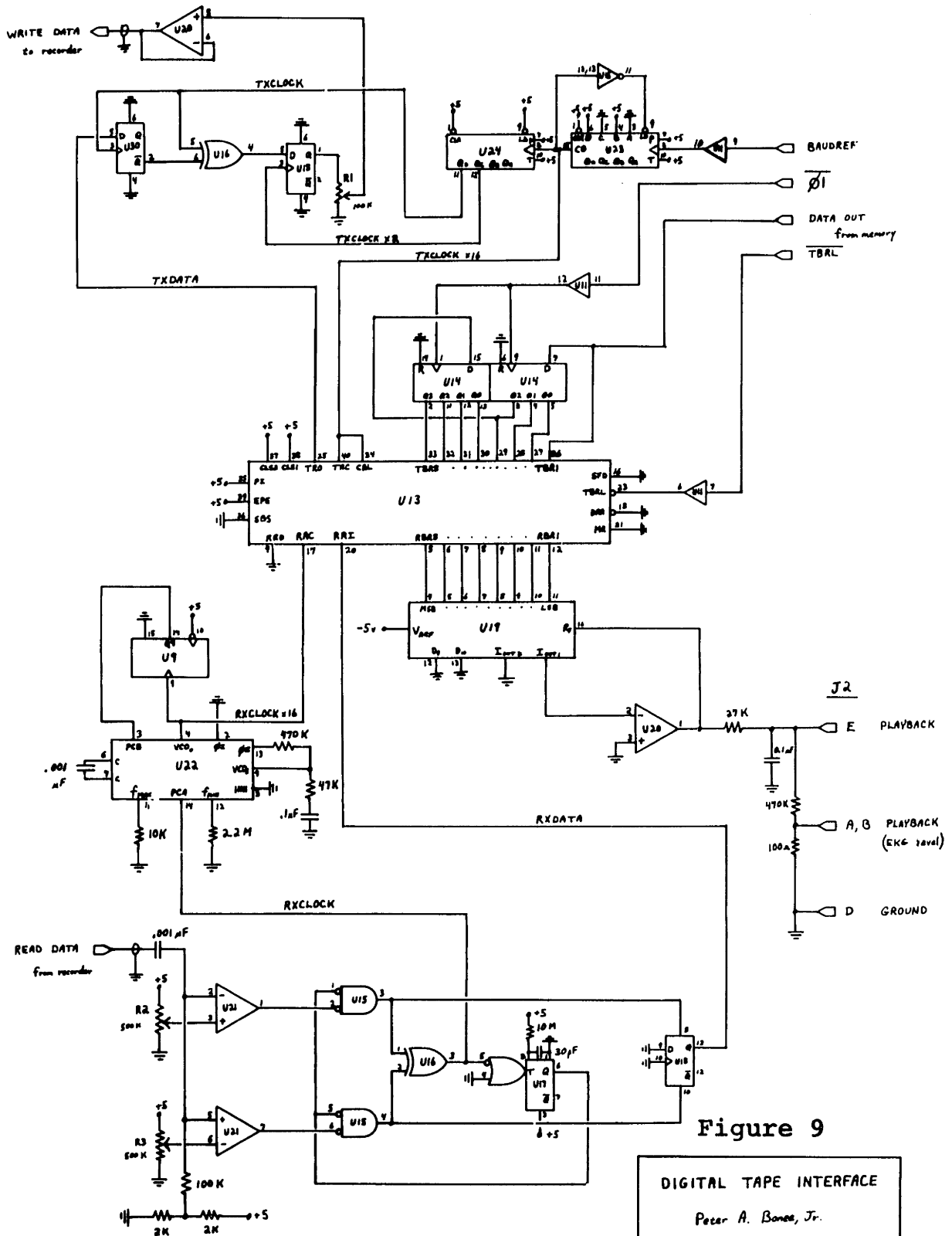


Figure 9

DIGITAL TAPE INTERFACE
 Peter A. Boney, Jr.
 April, 1979

transmitter baud rate. An encoder identical to the one shown in Figure 6 is used to encode the data and clock into a bi-phase signal. Counters U23 and U24 divide BAUDREF down to 2.6 KHz, 5.2 KHz, and 41.7 KHz square waves for TXCLOCK, TXCLOCKx2, and TXCLOCKx16, respectively. Note that the baud rate could be decreased if only 8 bits were transmitted every sample time. However, the start and stop bits facilitate proper synchronization during playback.

R1 is used to set the level of WRITE DATA, the signal recorded on tape. WRITE DATA is connected directly to the audio input of the tape recorder. No modifications were made to the tape recorder, so the tape recorder still operates as a linear AC-biased audio recorder. Studies have shown that linear AC-biased recording is quite suitable for digital recording.¹⁴ In fact, the tape interface and Sony TC-150A recorder of this design achieve a packing density of 1,387 bits per inch of tape, which is superior to many computer tape drives using saturation recording.¹⁰

The playback portion of the tape interface is slightly more complicated. The READ DATA from the recorder is high-pass filtered by a 0.001 μ F capacitor and 100 K resistor to ground. The upper section of U21 operates as a comparator and detects positive peaks above a threshold voltage set by R2. The lower section of U21 detects negative peaks below a threshold voltage set by R3. These

detected positive and negative peaks are converted to logic-level pulses by the comparators to create the +T and -T signals shown in Figure 6. These signals are then applied to a decoder of the type shown in Figure 6.

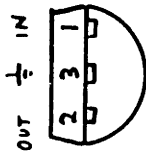
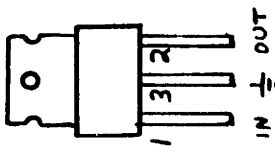
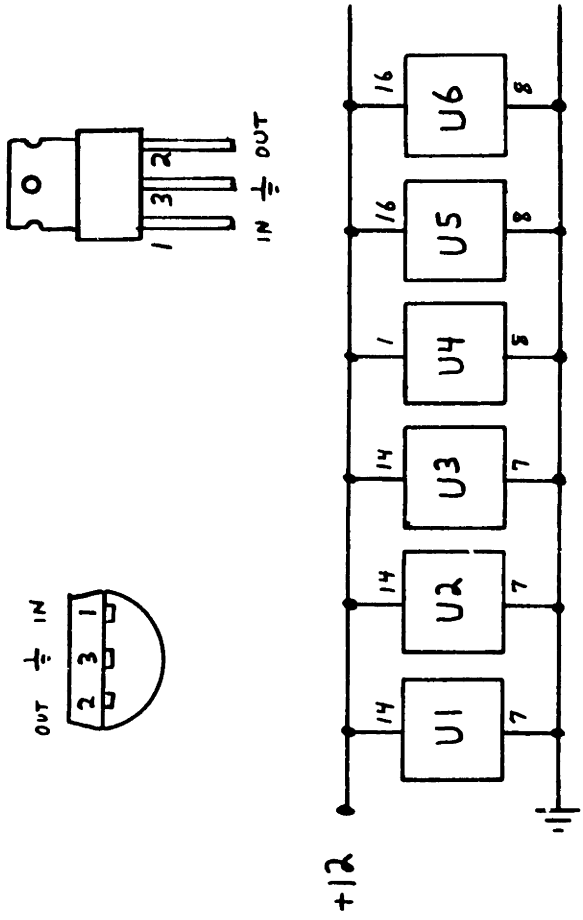
The decoded data (RXDATA) is applied to the serial receiver input of U13. When U13 recognizes a start bit in RXDATA, it accepts the next 8 data bits and presents them on the receiver buffer register output lines RBR1 - RBR8. Since U13 requires a receiver clock at a frequency of 16 times the received baud rate, the received clock (RXCLOCK) is applied to a frequency multiplier to generate the higher-frequency clock for U13. This frequency multiplier consists of U22, a phase-locked loop, with a $\div 16$ counter in its feedback loop.

The received data bits RBR1 - RBR8 are connected to the input of U19, a D-A converter. The D-A converter output appears at pins E and B of connector J2 on the front panel. The 0.1 μ F capacitor and the resistors provide low-pass filtering with a corner frequency of about 70 Hz. The output at pin E has a maximum amplitude of 5 volts peak-to-peak. The output at pin B has a maximum amplitude of 1 millivolt for playback on existing EKG equipment.

Figure 10 shows the power supply wiring of the portable EKG recorder. Power is provided by eight AA-type 1.5 volt cells and one 9 volt battery. U12 is a -5 volt regulator and U29 is a +5 volt regulator. The +12 volt

U12 - TOP VIEW

U12 - BOTTOM VIEW



8 1.5V
A" CELLS

9V
BATTERY

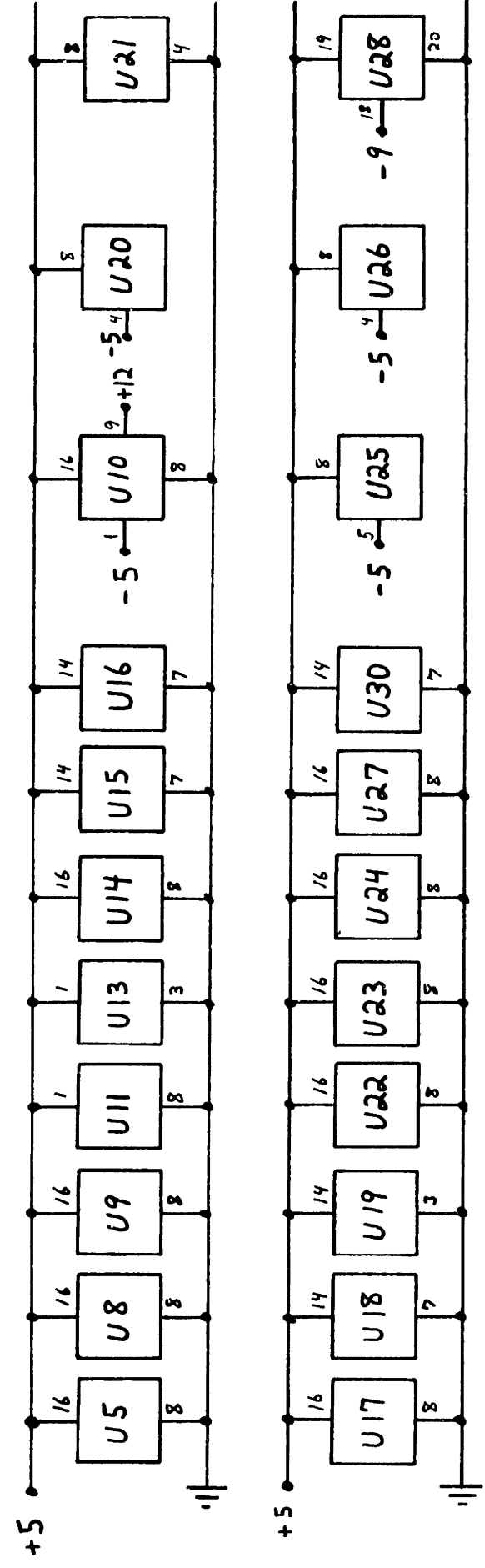


Figure 10: Power Supply Wiring

and -9 volt supplies are unregulated.

All components are mounted on a single $4\frac{1}{2}$ " x $6\frac{1}{2}$ " board. Figure 11 shows the location of integrated circuits on the board. Sockets are used for all integrated circuits and the interconnections are wire-wrapped. The board also accommodates the batteries. Figure 12 is a photograph of the interior of the unit.

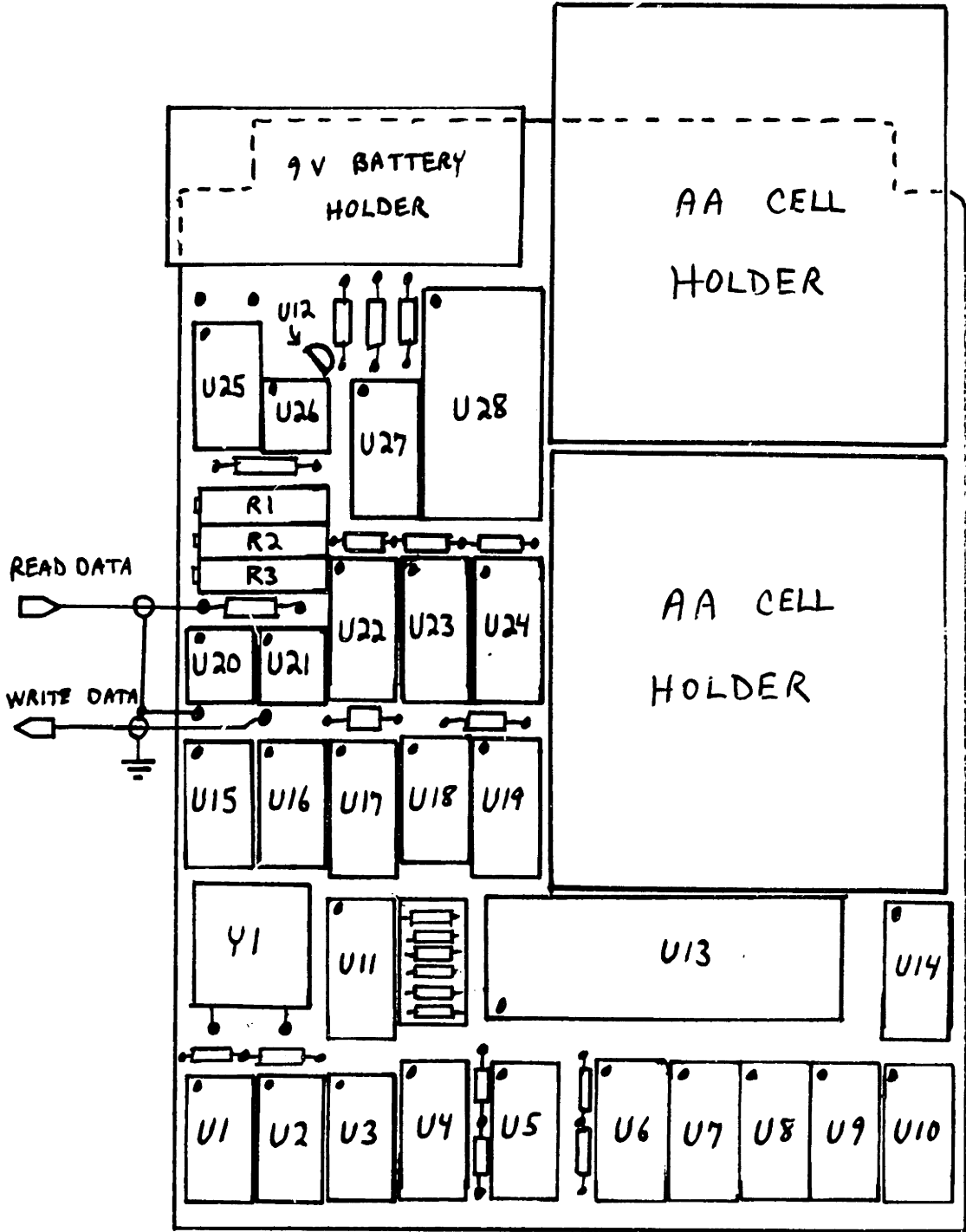
A photograph of the exterior of the unit appears in Figure 13. The input connector (J1) and the output connector (J2) appear on the left-hand portion of the front panel. The 3 adjustment holes to the right of the connectors are, from left to right, R1, R2, and R3. Appendix B explains these adjustments.

The dimensions of the prototype unit are $7\frac{1}{4}$ x $5\frac{1}{4}$ x $2\frac{1}{2}$ inches. The weight, with batteries and cassette, is 3 pounds, 5 ounces.

Testing and Evaluation

This section describes tests performed on the completed portable EKG recorder and relates the results to the original design considerations and goals.

After initial tests were performed to verify that the device was functional, various measurements were made of system performance. The first of these measurements was a frequency response test. Using a function generator to generate sine waves, it was found that the preamplifier had -3 db points at 0.16 Hz and 36 Hz. Sine waves of



Note: U29 and U30 are located on underside of board.

Figure 11: Board Layout

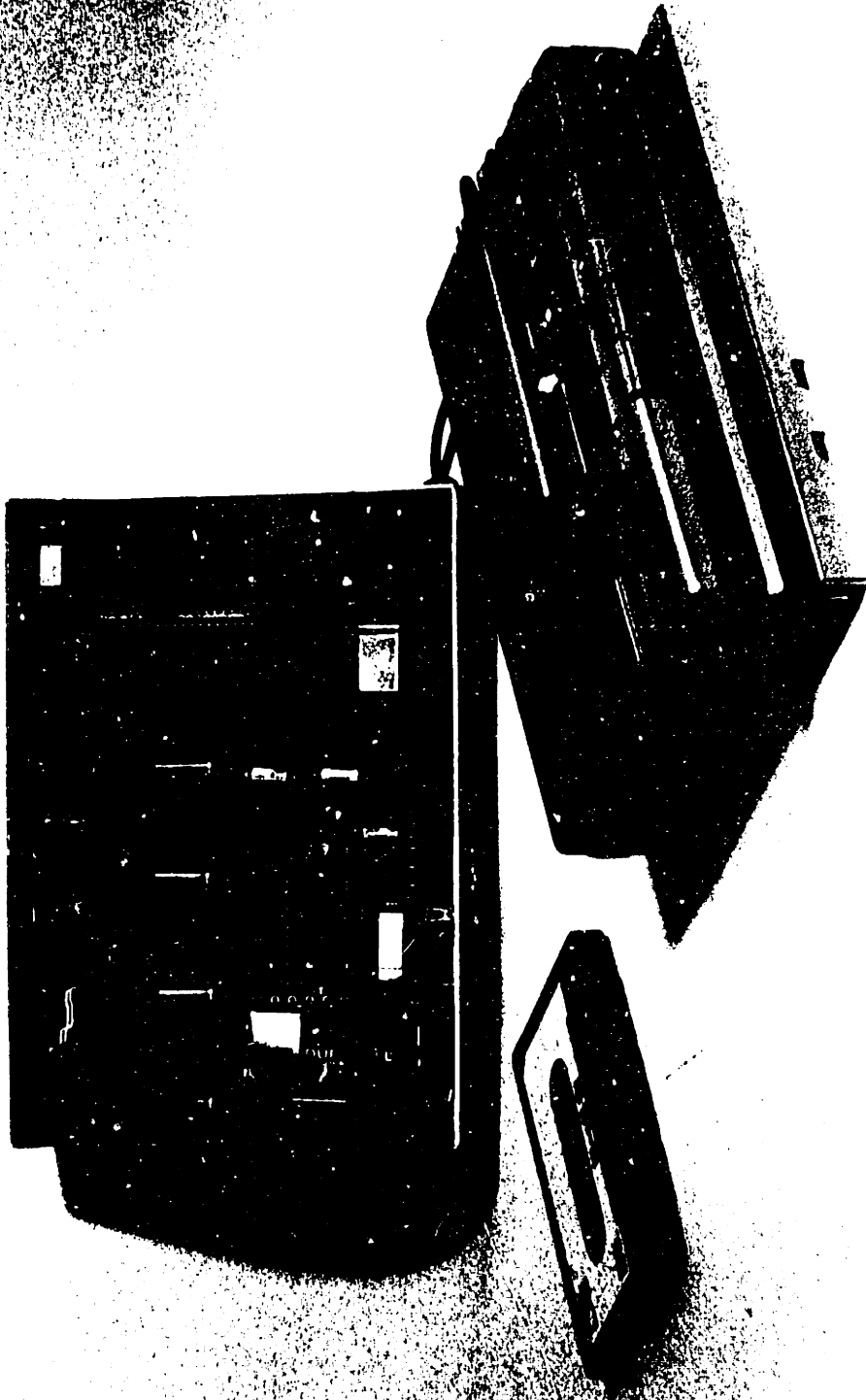


Figure 12: Interior View

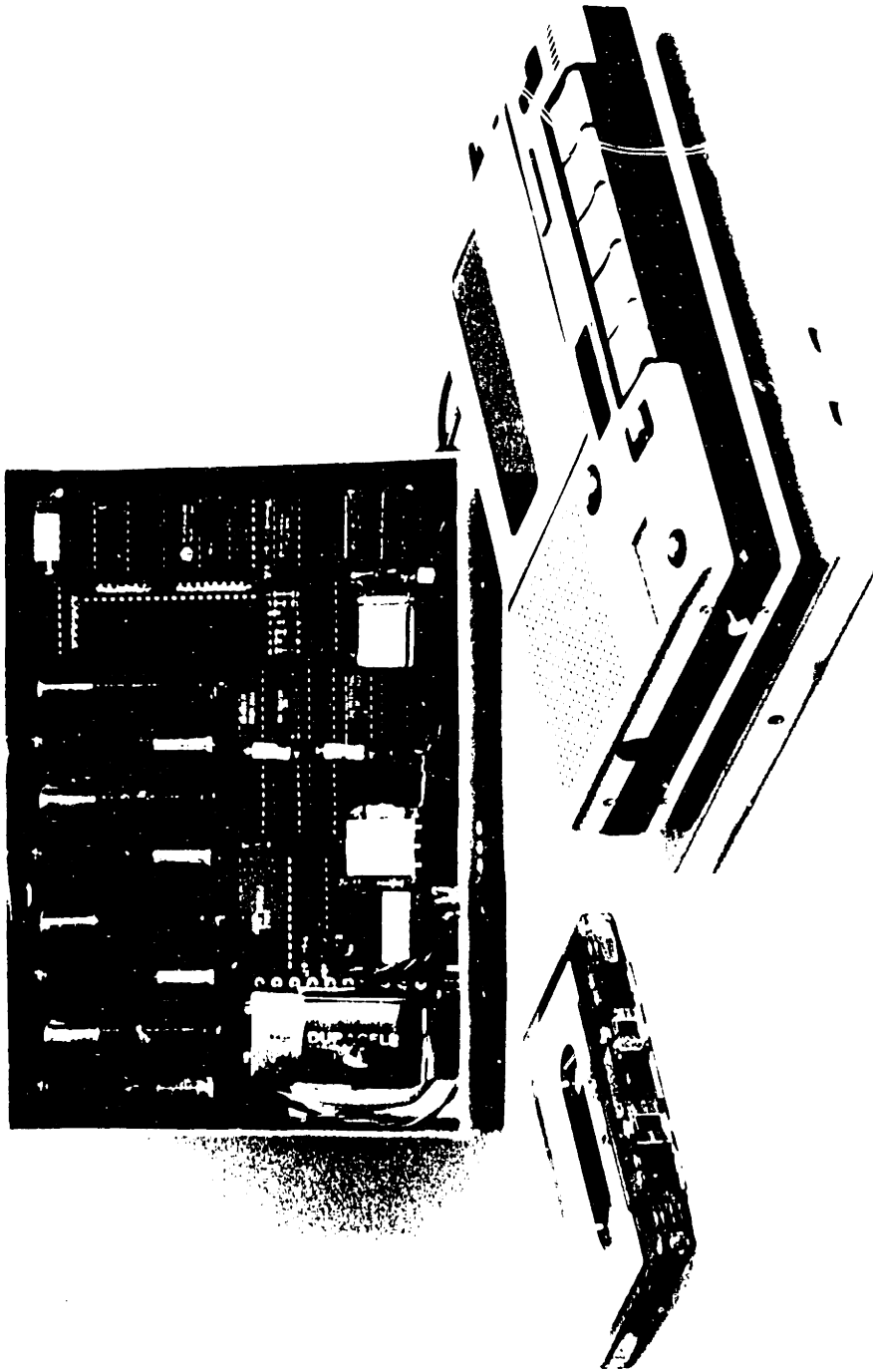




Figure 13: Exterior View



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various frequencies within this range were applied to the input and recorded 30 seconds later. The signals showed no signs of distortion on playback.

Operation of the tape interface was very satisfactory. The initial adjustments of the record and playback levels, U17 delay time, and peak-detection thresholds were not difficult and the tape interface never needed further adjustment. Further tests showed that reliable tape operation was possible even when the unit was shaken or struck lightly. This was determined by watching the recovered clock signal RXCLOCK on an oscilloscope and subjecting the unit to various motions and mechanical shocks. Clock jitter was very slight and never enough to affect the scope triggering action. This same type of experiment was performed while playing a tape which contained a sine wave from an earlier test, and no errors could be detected in the playback when the unit was shaken or struck lightly.

The device was further tested using actual EKG signals from a set of electrodes attached to the author. The preamplifier output and tape playback output both looked as expected. Various artifacts were introduced into the normal waveform by briefly tapping on the electrodes, coughing, etc. The tape recorder was then started about 20 seconds later to record the abnormal waveform segments. Later, playback of the recordings showed that the abnormal

waveform segments had been entirely recorded. A similar demonstration was performed by suddenly trying to exhale while holding the mouth closed and pinching the nostrils shut to block the flow of air. This is known as the Valsalva maneuver, and has the effect of causing an immediate slowing of the heart rate, as can be seen in Figure 14. A strip-chart recording of the preamplifier output appears on top and the corresponding playback (which was recorded on tape 30 seconds after the event actually occurred) appears below it.

To test battery lifetime, fresh batteries were installed and the unit was left running (except the tape recorder) until the batteries were drained beyond usefulness. Every hour during this experiment, about 10 seconds of EKG data were recorded on the tape. The tape was later played-through to see when the data became erroneous. This experiment was performed twice, once with inexpensive carbon-zinc batteries and once with alkaline batteries. The carbon-zinc batteries provided operation for 17 full hours and the alkaline batteries provided operation for 21 full hours.

These battery lifetimes clearly do not meet the initial goal of reliable operation over at least a 24-hour period. However, better batteries are available which would allow the portable EKG recorder to meet this design goal. The use of lithium cells, for example, could

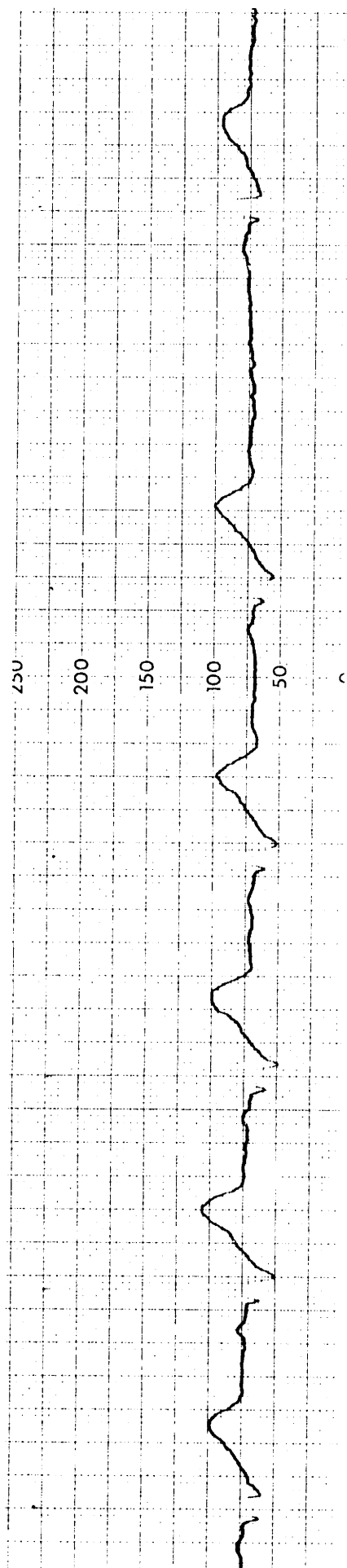
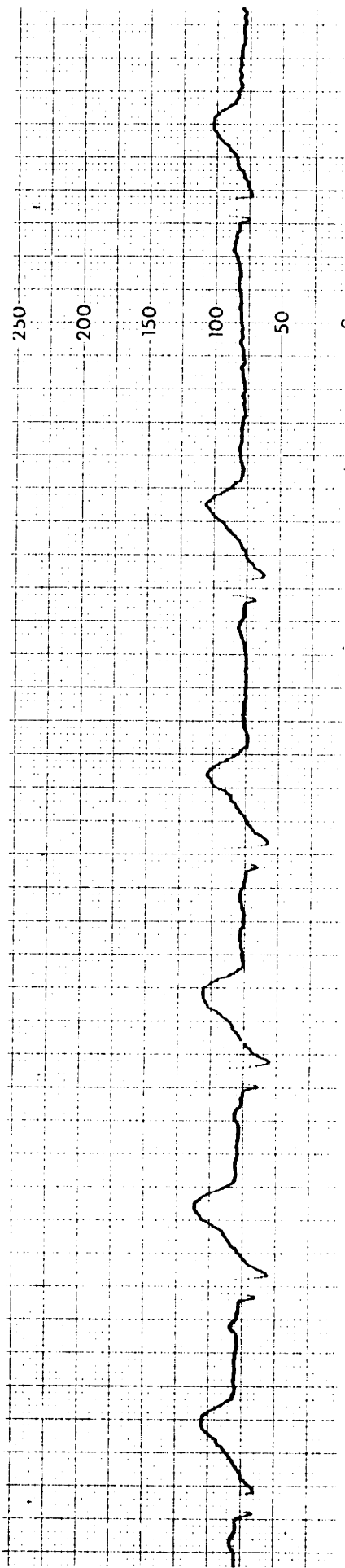


Figure 14: Original EKG Waveform (top) and Later Playback (bottom)

more than triple the battery lifetime of the +12 volt supply. Currently, the design calls for 8 size AA cells at 1.5 volts each to provide the +12 volt supply. Using lithium cells, only 5 size AA cells at 2.5 volts each would provide 12.5 volts, with approximately 3 times the capacity in ampere-hours.

A study was performed of the nature of the device's power consumption. Power consumed by each integrated circuit was measured while the system was running, and the results are tabulated in Appendix A. Total power consumption is almost 300 milliwatts. Of this total, about 50 milliwatts is used in the tape interface. Thus, future improvements to the portable EKG recorder should include switching-off the power to the tape interface when it is not in use, as well as the selection of superior batteries. Changes in circuit design, especially in the faster portions of the circuitry such as the clock generator, may also provide a savings in power consumption.

CONCLUSIONS

This project has shown the technical feasibility of the portable EKG recorder with delay buffering. With the exception of power consumption, all of the design goals were met by the initial design and prototype unit.

Commercially manufactured versions of this device would most likely be much less expensive than other systems in use, permitting the individual physician to invest in them.

Further efforts are needed, however, to solve the battery lifetime problem. The largest remaining task, of course, is to provide a clinical evaluation of the device.

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APPENDIX A

Integrated Circuits

Designation	Type	Supply	Pwr. Diss. (mW)
U1	MC14093B	+12	36.0
U2	MC14081B	+12	0.5
U3	MC14013B	+12	14.4
U4	MC14049B	+12	34.8
U5	74LS123	+ 5	55.0
U6	CD4520	+12	4.8
U7	CD4520	+12	10.8
U8	MC14040B	+ 5	2.0
U9	CD4520	+ 5	0.3
U10	TMS3064	+12,+5,-5	14.4
U11	MC14050B	+ 5	1.9
U12	79L05	- 5 volt regulator	
U13	IM6402	+ 5	10.0
U14	MC14015B	+ 5	1.0
U15	MC14001B	+ 5	0.3
U16	MC14070B	+ 5	0.4
U17	MC14528B	+ 5	1.0
U18	MC14013B	+ 5	0.3
U19	AD7520	+ 5	20.0
U20	LM358	+5,-5	7.0
U21	LM358	+ 5	2.1
U22	MC14046B	+ 5	11.0

<u>Designation</u>	<u>Type</u>	<u>Supply</u>	<u>Pwr. Diss. (mW)</u>
U23	MC14163B	+ 5	1.0
U24	MC14163B	+ 5	0.7
U25	AD521	+5,-5	9.0
U26	LM358	+5,-5	5.0
U27	MC14014B	+ 5	2.0
U28	8703C	+5,-9	40.0
U29	7805	+ 5 volt regulator	
U30	MC14013B	+ 5	0.2

APPENDIX B

Tape Interface Adjustment

It may be necessary to adjust certain tape interface parameters if a change is made in the tape recording system, such as a change in the quality of tape or a change in the tape recorder used.

Record Level: The level applied to the tape recorder input may be adjusted by means of R1. R1 is accessible through the first of the 3 adjustment holes on the front panel. The Sony TC-150A recorder was found to give best results when the level indicated on the VU meter was greater than 0 VU.

Playback Level: A level of about 3 volts peak-to-peak should be maintained for the audio signal READ DATA shown in Figure 9. This can be adjusted by means of the recorder volume control.

+T Threshold: The threshold above which a positive peak is detected during playback is adjusted by means of R2. R2 is accessible through the second of the 3 adjustment holes on the front panel. R2 should be adjusted for a +T signal similar to that shown in Figure 6, while watching the signal at pin 1 of U21 on an oscilloscope.

-T Threshold: The threshold below which a negative peak is detected during playback is adjusted by means of R3. R3 is accessible through the third of the 3 adjustment holes on the front panel. R3 should be adjusted for a -T signal similar to that shown in Figure 6, while watching the signal at pin 7 of U21 on an oscilloscope.