Monolithic Heteroepitaxial Integration of III-V Semiconductor Lasers on Si Substrates

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ABSTRACT

Monolithic optoelectronic integration on silicon-based integrated circuits has to date been limited to date by the large material differences between silicon (Si) and the direct-bandgap GaAs compounds from which optoelectronic components are fabricated. Graded Ge/GeSi buffer layers grown on standard Si substrates have been shown to produce near-lattice matched virtual substrates for GaAs integration on Si. This study investigated the crystal growth conditions and device fabrication techniques necessary for successful GaAs-based laser integration on Ge/GeSi buffer layers on Si substrates.

The nucleation conditions for GaAs on Ge/GeSi/Si substrates have been comprehensively examined. High-temperature ($\geq$ 700 ºC) initiation with properly chosen V/III gas flow ratio yields high-quality, stacking fault-free GaAs films on Ge/GeSi/Si substrates, but also encourages the vapor-phase transport of Ge from the substrate into the active regions of integrated GaAs devices. A new two-step GaAs nucleation process was developed that enabled the first demonstration of high-quality Ge-free GaAs light-emitting diodes on Ge/GeSi/Si substrates.

The large thermal expansion mismatch between Si, Ge, and GaAs introduces additional strain to integrated device layers on Ge/GeSi/Si substrates grown at high temperatures. This study conclusively demonstrated the link between thermal mismatch strain and increased misfit dislocation formation in $In_xGa_{(1-x)}As$/GaAs quantum well structures integrated on Ge/GeSi/Si substrates. The thermal mismatch strain was successfully countered by the introduction of compressive InGaAs graded buffer layers above the Ge/GeSi/Si substrate surface, and strain-free GaAs layers at growth temperatures suitable for laser integration have been demonstrated.

The integration of edge-emitting heterostructure lasers on Ge/GeSi/Si substrates introduces additional waveguide design issues addressed by this study. Low-index $Al_{0.6}Ga_{0.4}As$ cladding layers, along with a graded-index separate confinement heterostructure, were introduced to reduce photon losses. Interfacial roughness transmitted from the Ge/GeSi/Si substrate was reduced with a pre-growth chemical-mechanical polishing step, and smooth mirror facets on integrated devices were fabricated by cleaving thinned lasers parallel to the substrate offcut direction.

Continuously operating edge-emitting GaAs/AlGaAs quantum well lasers on Ge/GeSi/Si substrates were demonstrated at room temperature with an operating wavelength of 858 nm. Series resistance heating in early devices was reduced by the introduction of a top-contact geometry and optimized cladding layer structure, and

improved laser diodes had a differential quantum efficiency of 40%, a threshold current density of 269 A/cm^2, and a characteristic temperature of 129 K. Identical devices fabricated on GaAs substrates had similar performance characteristics. Lasers on Ge/GeSi/Si substrates fell below threshold after 4 hours of continuous operation−a dramatic improvement over early measured lifetimes of less than 20 minutes. Electroluminescence images of operating lasers taken before and after failure showed that dark line defects were present in the laser active regions after failure. Room-temperature 60 Å $In_{0.17}Ga_{0.83}As$ strained quantum well lasers have also been demonstrated on Ge/GeSi/Si with an operating wavelength of 897 nm; these lasers had shorter lifetimes (< 15 min) under continuous operation due to misfit dislocations in the strained quantum well active region.

While challenges remain for monolithic III/V optoelectronic integration on Si, it is clear that the demonstration of a successfully integrated GaAs-based laser on a Ge/GeSi/Si substrate represents a significant milestone on the path to the final goal of truly integrated high-speed optoelectronic devices and Si integrated circuits.

Thesis Supervisor: Eugene A. Fitzgerald
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I would like to dedicate this thesis to my grandfather, Dr. Raymond Wilson, who sparked my first interest in physics and encouraged me to never stop wondering how things work.

Chapter 1. Introduction

Silicon has become one of the world's most useful materials for a vast array of electronic applications. Silicon transistors can be found inside thousands of different consumer and manufacturing products where they provide efficient, high-speed calculating power at a fraction of the cost of other technologies. Silicon (Si) is an ideal material for microelectronic circuits for a variety of important reasons. Silicon has a stable, easily processed native oxide (SiO_2) that can be readily integrated on Si surfaces to form built-in circuit isolation layers and dielectric gate barriers. Silicon also benefits from almost 60 years of material research into the growth of elemental Si crystals. Si transistor manufacturing technology has built on these advances to the point where state-of-the-art fabrication facilities can produce billions of transistors per wafer at a rate of thousands of wafers per day. Considering the intense amount of investment which has gone into Si transistor technology in the last half century and the ubiquity of Si transistors in modern electronic equipment, it seems likely that Si wafers will continue to dominate the microelectronics industry for the foreseeable future.[1]

Despite its many strengths, Si is not a perfect material for large-scale transistor integration, and recent advances with increasing transistor speed and density on Si wafers have begun to expose some of the inherent limitations of traditional Si circuits for ultra-high-speed and high-density microelectronics applications. In particular, relatively low carrier mobility (compared to other inorganic semiconductors like Ge or GaAs) and the inability of Si crystals to form direct-gap optoelectronic devices have both begun to restrict the speed and data rates at which Si-based integrated circuits can operate. Crosstalk between neighboring circuits, coupled with RC signal delays in the metal interconnects that link individual Si transistors are unavoidable in present Si integrated circuit designs.[2,3]

Optical circuit interconnects offer an alternative model for high-speed microelectronics, in which individual Si circuits or devices on a wafer chip are connected by multiplexed optical waveguides, providing crosstalk-free data paths with exponentially higher data rates than current metal wire lines. The performance benefits offered by optoelectronic integration on Si circuits are in essence the same as those

offered by the fiber optic technology that replaced much of the traditional metal wiring in the world's telecommunications networks over the last 30 years. Individual fiber optic waveguide cables, capable of carrying trillions of bits of digital information per second through hundreds of discrete frequency channels, now carry nearly all of the long-distance voice and data traffic in the developed world.[4] Optoelectronic interconnects promise similarly revolutionary speed and bandwidth advances for Si integrated circuits if they can be successfully integrated into the mature Si transistor manufacturing infrastructure.

Si is an indirect-bandgap semiconductor and cannot be used to efficiently generate photons for optical communication applications. In contrast to Si, many of the compound semiconductors from groups III and V of the periodic table (such as GaAs or GaN) are direct-bandgap semiconductors. Alloys of GaAs, GaN, and InP have been used to fabricate a wide variety of commercially important light-emitting devices, including the high-speed semiconductor lasers which drive all modern fiber optic telecommunications circuits.[5] Ideally, a Si semiconductor circuit into which a compound semiconductor light-emitting device or detector could be easily and inexpensively integrated would offer the fast calculation speed, high device density, and low cost of modern Si circuit technology together with the high-speed data transfer capabilities of compound semiconductor optoelectronics. New integrated circuit designs may be imagined in which a collection of complimentary metal-oxide-semiconductor (CMOS) logic circuits on a Si wafer are linked to each other and to neighboring wafers by high-speed GaAs laser/detector modules integrated directly on the Si substrate wafer. A hypothetical example of one such circuit design is shown in Figure 1.1.

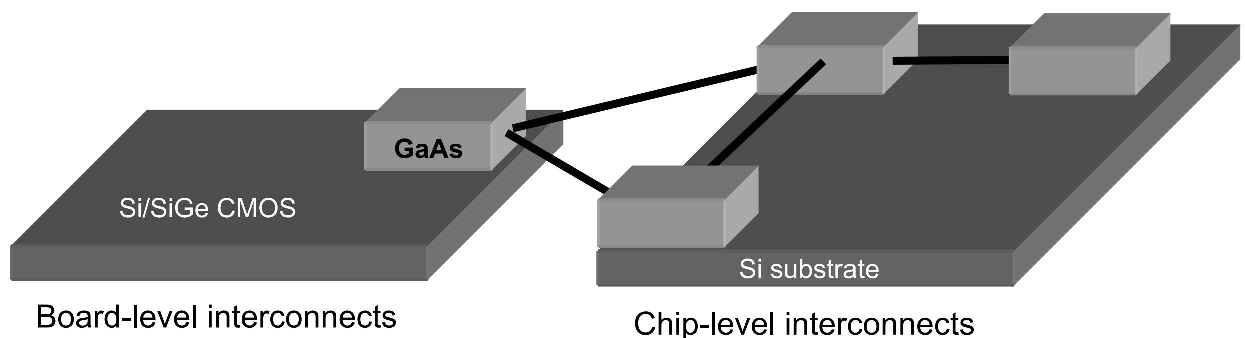

Figure 1.1: Hypothetical example of an integrated GaAs/Si optoelectronic circuit

The potential benefits of optoelectronic integration on Si integrated circuits have inspired hundreds of investigations into practical methods for achieving this goal by dozens of different research groups during the last three decades. While limited success has been reported for some complex hybrid integration schemes,[6] no group has yet demonstrated a commercially viable epitaxially integrated GaAs-based optoelectronic circuit on a Si CMOS logic platform. Monolithic epitaxial integration of III-V compound semiconductors on Si substrates will remain a key step for the economical production of optoelectronic integrated circuits. Only with compound semiconductor device layers deposited epitaxially at the beginning of the Si circuit fabrication process can manufacturers use the leverage of the mature Si production infrastructure to create truly high-speed and low-cost optoelectronic integrated circuits on Si wafers.

The monolithic epitaxial integration of III-V compound semiconductors on Si substrates is not a straightforward process, due to the significant differences in basic crystal properties that exist between elemental Si and the III-V semiconductor alloys. These differences include variations in the interatomic lattice spacing of the two materials, differences between their thermal expansion properties, and variations in the crystal structures due to the reduced symmetry of compound semiconductor lattices. Early attempts to deposit III-V semiconductor materials directly on Si substrates by a variety of crystal growth mechanisms led to unacceptably high densities of defects in the resulting films, as will be discussed in detail below. Recent work in this research group has suggested a new epitaxial integration procedure that can permit the successful epitaxial integration of III-V optoelectronic circuits on Si substrates via the use of relaxed graded Ge/$Ge_xSi_{(1-x)}$ buffer layers. Simple integrated optoelectronic devices including light-emitting diodes, solar cell structures, and photodetectors have been successfully demonstrated on Si substrates using this new integrated materials platform.

Although basic optoelectronic structures have been integrated on Si substrates via Ge/GeSi buffer layers, semiconductor laser structures remain the ultimate test for the quality of the integrated films because lasers operate at photon and minority carrier population densities that make them very sensitive to epitaxial defects from the integration process. The work presented in this thesis will focus on efforts to use relaxed

graded $Ge/Ge_xSi_{(1-x)}$ buffer layers to demonstrate high-quality III-V semiconductor lasers epitaxially integrated on Si substrates.

1.1. Barriers to Epitaxial III-V/Si integration

As mentioned above, there are a number of fundamental differences between the material characteristics of the III-V optoelectronic semiconductors and Si. A summary of the differences between Si, Ge, and GaAs is presented in Table 1.1.[7]

Table 1.1: Materials constants for Si, Ge, and GaAs

Semiconductor	Crystal structure	Lattice Constant (Å)	Coefficient of thermal expansion at 300K (K^{-1})
Si	Diamond cubic	5.430	2.6×10^{-6}
Ge	Diamond cubic	5.657	5.8×10^{-6}
GaAs	Zincblende	5.653	6.8×10^{-6}

It can be seen from this table that there are significant disparities in the crystal structure, lattice constants, and thermal expansion coefficients for all three semiconducting materials. Data is presented for germanium (Ge) along with Si and GaAs because of the importance of Ge as a natural intermediary material between Si substrates and III-V GaAs alloys, as will be explained below. The various differences between the three materials will be considered separately for each of the properties discussed above.

1.1.1. Differences in Lattice Constant

The lattice constant of bulk Si is 4.1% smaller than GaAs at room temperature. This mismatch in lattice constants means that a GaAs crystal deposited epitaxially on a Si substrate would require the periodic removal of a plane of Ga or As atoms every 25 atomic rows to match up coherently with the atoms of the Si crystal substrate below it. Unfortunately for experimentalists, there are few useful III-V semiconductor alloys with lattice mismatch on Si smaller than that of GaAs. A plot of common semiconductor lattice constants vs. bandgap energies is presented in Figure 1.2. It can be seen from this figure that GaAs is the closest match to Si of the direct-bandgap (light-emitting) binary compound semiconductors.

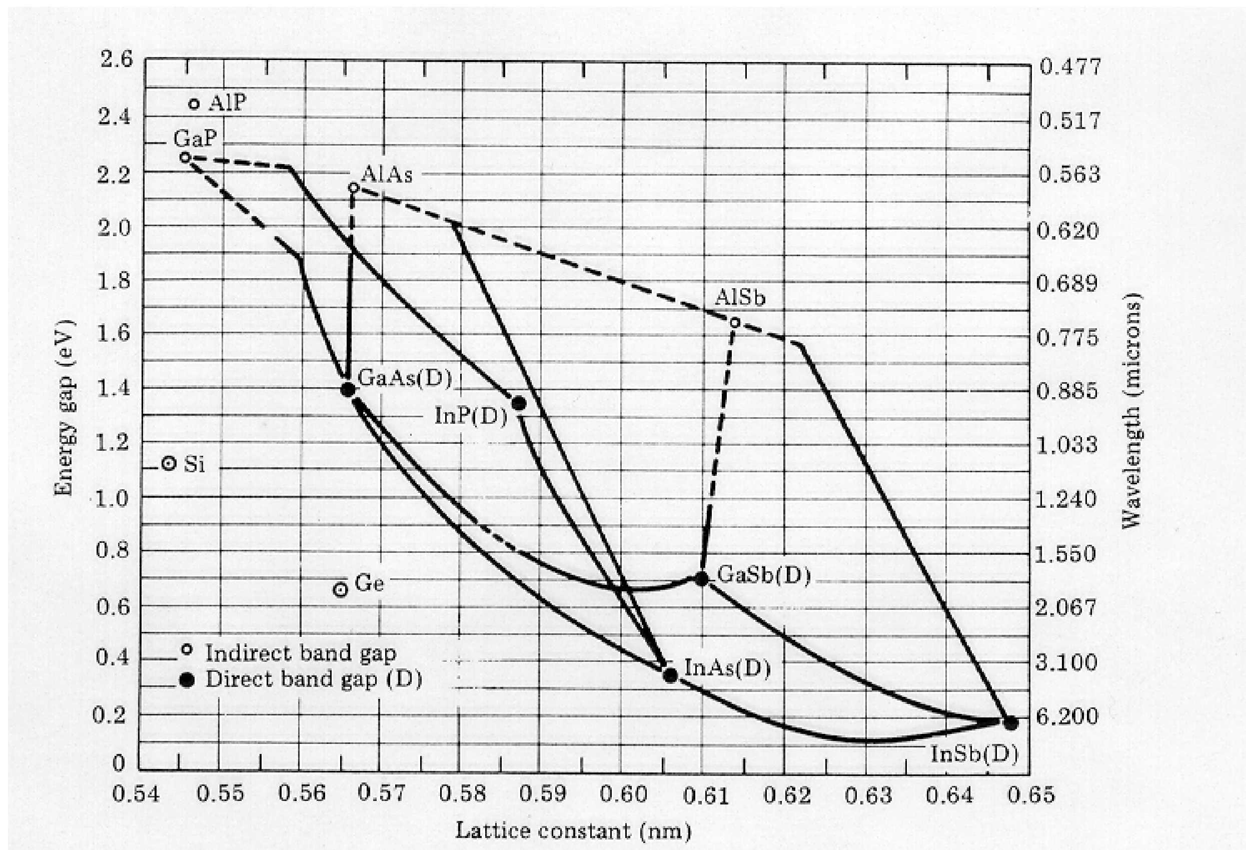

Figure 1.2: Bandgap energy vs. lattice constant for a variety of common semiconducting materials.

If lattice mismatch is unavoidable for III-V on Si epitaxy, it is important to consider how this mismatch will be accommodated during semiconductor crystal growth. When a semiconductor film with a lattice constant a_f is deposited on a semiconductor substrate with a lattice constant a_s, a misfit strain is developed which can be defined as:

$$f = \frac{a_s - a_f}{a_f}$$

For thin films with low amounts of mismatch, this misfit strain will be accommodated by an elastic deformation of the deposited film lattice. Epitaxial films with lattice constants larger than the substrate lattice will be compressively strained, while films with smaller lattice constants will undergo tensile strain. In either case, the film material will remain coherently linked to the substrate, with each substrate atom uniquely bonded to corresponding atoms in the film above it. With higher amounts of mismatch, or thicker epitaxial films, the misfit strain at the interface will increase until it exceeds the elastic strength of the coherent semiconductor-semiconductor bonds. At this point, the film will

undergo a plastic deformation resulting in the formation of broken bonds and non-coherent crystal defects at the substrate-film interface. A simplified cross-section showing the elastic and plastic stages of misfit strain accommodation for a compressive semiconductor film on a thick substrate is shown in Figure 1.3.

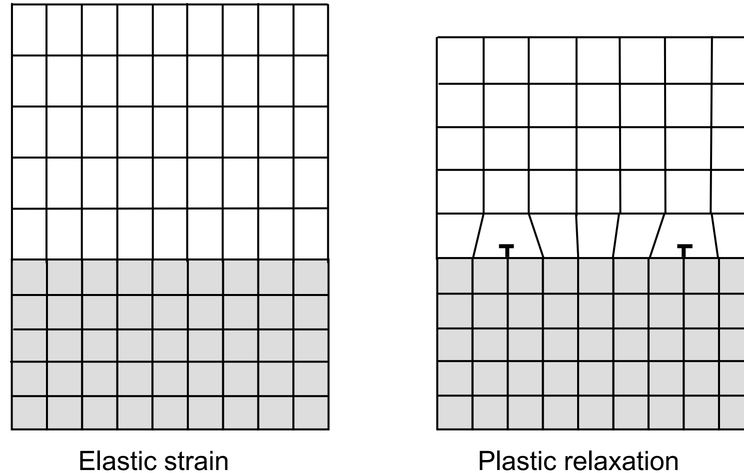

Figure 1.3: Elastic strain and plastic relaxation at a mismatched semiconductor interface. Note the two misfit dislocations at the mismatched interface after plastic relaxation.

It can be seen from the figure that the deposited semiconductor film will accommodate misfit strain plastically by forming a one-dimensional line of broken atomic bonds at the substrate-film interface. This one- dimensional defect structure is known as a misfit dislocation and will extend linearly along the interface to terminate at a free surface of the crystal. For the (001)-oriented surfaces typically used in semiconductor device epitaxy, the {111}<110> slip system of the mismatched crystal will encourage misfit dislocation lines to align themselves along the low-energy [110] and $[1\bar{1}0]$ directions. Once formed, dislocation lines can propagate by dislocation glide along a mismatched interface.

The formation and propagation of misfit dislocations is thermodynamically governed by a local energy balance between the misfit strain energy relieved by dislocation formation and the energy cost of extending an array of misfit dislocations along a coherent crystal interface. This energy balance can expressed mathematically by equating the misfit strain energy per unit area of a strained film,

$$E_s = \varepsilon^2 Y h$$

with the energy per unit area of an orthogonal array of misfit dislocations:

$$E_d = D\frac{b}{b_{eff}}\left(1-\nu\cos^2\theta\right)\left(f-\varepsilon\right)\left[\ln\left(h/b\right)+1\right]$$

The total strain in the epitaxial film is defined as $\varepsilon = f - \delta$, where f is the elastic misfit strain and δ is the accommodated plastic strain. Physically δ represents the strain which has been relieved by existing misfit dislocations. Y is the biaxial Young's modulus of the strained film, h is the film thickness, ν is Poisson's ratio in the epitaxial film, and b is the Burgers vector in the strained layer. The angle between the Burgers vector and the interface plane is θ, and D is the average shear modulus at the interface, defined as:[8]

$$D = \frac{G_f G_s b}{\pi\left(G_f + G_s\right)\left(1-\nu\right)}$$

where G_f and G_s are the respective shear moduli of the epitaxial film and the substrate.

The energy of misfit strain relaxation and dislocation array formation can be shown to be exactly balanced at a specific critical thickness, h_c. Mismatched films grown below this critical thickness should remain elastically strained without forming misfit dislocations, while films grown above this critical thickness can relax plastically by generating an array of [110] and $[1\bar{1}0]$ dislocation lines. Matthews has derived the following expression for critical thickness based on the material terms defined above:[9]

$$h_c = \frac{D\left(1-\nu\cos^2\theta\right)\left(b/b_{eff}\right)\left[\ln\left(h_c/b\right)+1\right]}{2Yf}$$

This expression gives the thermodynamic critical thickness for a mismatched film on a semiconductor substrate. As a point of reference, the thermodynamic critical thickness for GaAs grown on bulk Si is about 2 nm.

Kinetic factors also play a role in determining how misfit dislocations form in semiconductors. Kinetic activation barriers can inhibit the formation and glide motion of misfit dislocations, and lead to metastable super-critical strained films on mismatched substrates under certain growth conditions. Models explaining the kinetic factors involved in misfit strain relaxation have been developed but require extensive experimental fitting to be useful for predicting kinetic critical thickness values in real

systems.[10] It is therefore reasonable to treat the Matthews equilibrium critical thickness as a firm lower bound for misfit strain relaxation in strained layer systems, and to use this critical thickness relationship to better understand the formation and propagation of misfit dislocations in these systems.

All misfit dislocations must terminate at a free surface at the boundaries of a semiconductor wafer. While some dislocations will form or propagate at the edges of the wafer, most misfit lines will terminate in segments that originate at the semiconductor film surface. The misfit dislocation lines lying in the plane between the substrate and epitaxial film will connect to the surface via threading dislocation segments, which propagate by dislocation climb from the strained misfit interface along {111} planes in diamond-cubic or zincblende materials. Threading dislocations are one-dimensional crystallographic dislocations that do not relieve strain in a semiconductor. Importantly for epitaxial integration experiments, threading dislocations act as non-radiative recombination centers in optoelectronic devices and thus their presence is not welcome for III-V on Si heteroepitaxial structures.

Misfit and threading dislocation segments can be nucleated in a variety of ways in mismatched semiconductor films above the equilibrium critical thickness. At very high misfit strains, misfit dislocation loops can form spontaneously via homogenous nucleation, although this mechanism rarely occurs in practical growth systems. Much more common is heterogeneous nucleation of dislocation loops at surface imperfections or at point defects in the film. Misfit dislocation segments can also nucleate at pre-existing threading dislocations climbing upwards from the substrate. A schematic representation of the different ways dislocations can nucleate in a mismatched system is shown in Figure 1.4.

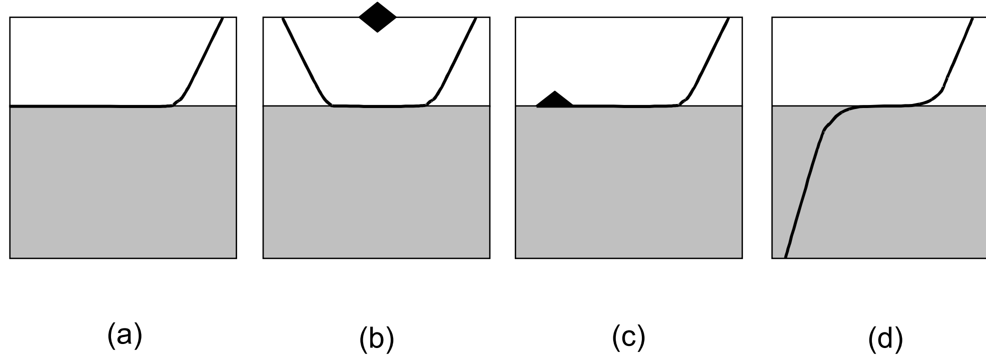

Figure 1.4: Options for dislocation nucleation at a mismatched semiconductor interface. (a.) Homogeneous nucleation, (b.) Heterogeneous nucleation at a surface defect, (c.) Heterogeneous nucleation at an interface defect, and (d.) Heterogeneous nucleation at a pre-existing thread. Heterogeneous mechanisms will dominate in practical growth systems.

Equilibrium thermodynamics can be used to estimate the total density of dislocations that will form for a mismatched semiconductor with a given misfit strain. For any strain state, the average spacing of an array of parallel misfit dislocations, *S*, can be estimated for a given amount of accommodated strain δ, as: [11]

$$S = \frac{b}{2\delta}$$

This equation assumes that all strain-relieving dislocations have Burgers vectors 60° from the [110] dislocation directions. For GaAs grown directly on Si, the complete relaxation of the 4.1% lattice mismatch would demand a dislocation spacing *S* = 100 Å. Equilibrium theory shows that some elastic strain will remain in a mismatched film after relaxation. Work by a number of authors has shown that the relaxation of a mismatched epitaxial film can be limited by kinetic barriers and dislocation-dislocation interactions.[12, 13]

Dislocation-dislocation interactions can play an important role in the relaxation behavior of mismatched epitaxial films. Gliding coplanar misfit dislocation lines can attract or repel each other depending on the sign of their respective Burgers vectors. Threading dislocations can also be attracted or repelled by the strain fields of adjacent dislocations, and research has shown that threading dislocation motion in a growing film can be easily impeded by the tangling of groups of threading dislocations into macroscopic dislocation pileups.[14] If threading dislocations are immobilized, their attached misfit segments cannot continue extending to relieve misfit strain and more

dislocations must be nucleated to relieve the remaining strain. Thus the total threading dislocation density in a mismatched epitaxial film will multiply rapidly if dislocations are able to interact and pin each other during growth. Dislocation multiplication is largely responsible for the observed rapid rise in threading dislocation densities with increasing lattice mismatch in real semiconductor systems.

Finding ways to reduce the density of threading dislocations at a given mismatch strain level is an important goal for successful strained-layer heteroepitaxy. As mentioned above, threading dislocations can act as non-radiative recombination centers in optoelectronic devices, because the localized mid-bandgap energy levels in the dislocation cores will act as highly efficient trap states for injected minority carriers. These traps can dramatically reduce the overall minority carrier lifetime in the material.[15] Localized mid-bandgap energy levels in threading dislocations (along with a tendency of these dislocations to getter metal impurity atoms) can lead to short-circuit behavior in active electronic junctions, and scattering from dislocation cores can lead to decreases in effective carrier mobility and transconductance for majority carrier devices.[16]

Reductions in minority carrier lifetime are especially detrimental for semiconductor lasers. A semiconductor laser requires a population inversion of minority carriers in the active layers of the laser structure before it can demonstrate a positive gain coefficient and lasing action. No other optoelectronic device requires such a high density of non-equilibrium carriers in its active region. If the minority carrier lifetime is reduced by dislocations in a laser structure, more and more of the injected minority carriers will recombine non-radiatively before they can reach the local densities necessary for population inversion. Early work with GaAs-based semiconductor lasers on GaAs substrates has shown that threading dislocation densities greater than 10^6 cm^{-2} can reduce minority carrier lifetimes in these materials enough to completely prohibit laser operation.[17] This requirement is not a problem for today's commercial GaAs substrates, which typically demonstrate total surface dislocation densities less than 100 cm^{-2}. However the threading dislocation densities for GaAs epitaxial films deposited directly on Si substrates are typically closer to 10^9 cm^{-2}, highlighting one of the chief issues facing any attempt to successfully integrate GaAs-based laser diodes on Si substrates.

Another unique issue for integrated laser structures on substrates with high dislocation densities is the potential movement of these dislocations during laser operation to form dark line defects in operating devices. Dark line defects (DLDs) have been reported by a number of authors as one of the chief failure mechanisms in operating GaAs-based semiconductor lasers.[18,19] These defects are composed of clusters of extended dislocation loops that propagate into the active regions of operating devices, where they increase the local rate of non-radiative recombination and thus produce dark lines visible in electroluminescence or electron beam induced current (EBIC) micrographs.[20] An EBIC image of a typical DLD dislocation cluster moving into a bright GaAs/AlGaAs laser active region is shown in Figure 1.5.

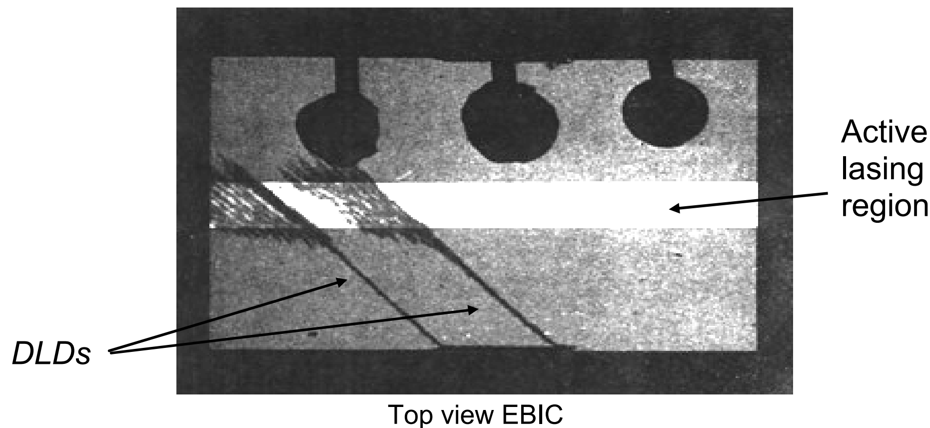

Figure 1.5: Representative EBIC image of a DLD dislocation cluster propagating from the edge of a GaAs/AlGaAs laser to the bright active region in the center. The three dark circles at the top of the image are metal contacts. (image courtesy of Yellen[18])

Two types of dark line defects are commonly found in failed lasers: <100> DLDs perpendicular to the interface planes, which climb from the edges of the cladding layer through the device layer, and <110> DLDs, which lie parallel to the interface planes and move into the active region by gliding from device edges. For both types of defect, the chief mechanism for the initial dislocation propagation and multiplication is believed to be recombination-enhanced defect reactions. As modeled by Weeks,[21] energy liberated by the non-radiative recombination of injected electrons and holes at pre-existing defect sites in an operating laser is converted into localized lattice vibrations. These local lattice vibrations are energetic enough to trigger new defect reactions, such as vacancy-interstitial pair formation and impurity or defect diffusion. Recombination enhanced

defect reactions (REDR) which occur at the newly created defect sites create additional defects in the same manner, and the cycle repeats in a positive feedback reaction as the DLDs climb or glide deeper into the device. At high densities, these dark line defects will lead to rapid increases in the threshold current for laser operation, and irreversible laser failure. Directly correlating the initial threading dislocation density in epitaxial laser structures with the dark-line defect density that develops in operating devices is difficult. While the initial nucleation of new dislocation loops will depend directly on the density of threading dislocation sites in the laser active region, the rapid multiplication of these loops into DLD structures will be controlled mostly by the temperature of the surrounding lattice and the injected carrier density in the operating device. Thus increasing threading dislocation densities in a semiconductor laser structure can be expected to increase the density of nucleated DLDs, but cannot be directly correlated to the final DLD density after failure without factoring in the kinetics of the defect multiplication reactions which follow nucleation.

Controlling DLD failure in operating GaAs lasers epitaxially integrated on Si substrates will place constraints on the maximum allowed threading dislocation densities in these devices, and will demand relatively low laser threshold current densities and low amounts of resistive self-heating in the operating devices fabricated on Si substrates.

Efforts to reduce the threading dislocation density, increase the minority carrier lifetime, and control dark line defect propagation in GaAs devices on Si by a number of different experimental methods will be discussed below.

1.1.2. Differences in Thermal Expansion Behavior

The thermal expansion coefficient of GaAs is almost 60% larger than the Si expansion coefficient at room temperature. This difference narrows only slightly at the elevated temperatures typical for semiconductor heteroepitaxy. The consequences of this thermal expansion mismatch can be significant. When a GaAs film is deposited on a thick Si substrate, it will relax at the growth temperature, forming an array of misfit and threading dislocations as detailed in the previous section. When the substrate is cooled after growth, the difference in thermal expansion coefficients will mean that the GaAs epilayers will shrink much more quickly than the Si substrate lattice below them.

Assuming that the mismatched GaAs film has completely relaxed at the growth temperature, a tensile thermal expansion strain will thus be developed in the cooling film which will be proportional to the total change in temperature of the system:

$$\varepsilon_t = \int_{T_0}^{T} \left[\alpha_s(T) - \alpha_f(T) \right] dT$$

where T and T_0 are the final and initial temperatures of the growth system, respectively, and α_s and α_f are the temperature-dependent coefficients of thermal expansion for the substrate and film. The actual dependence of the thermal expansion coefficients on temperature for GaAs and Si are small enough that they can be ignored to first order, leading to a simplified expression for the thermal mismatch strain as a function of the total change in reactor temperature ΔT:

$$\varepsilon_t = \left(\alpha_s - \alpha_f \right) \Delta T$$

For a GaAs film on a Si substrate at a typical reactor growth temperature of 700 °C, the total tensile strain developed on cooldown to room temperature will be 0.26%. This strain is significantly less than the total material mismatch strain for these two materials, but still significant enough to cause some important effects in heteroepitaxial layers. Because this strain develops as the epitaxial layers are cooled from the growth temperature, dislocation relaxation mechanisms are much less efficient at relieving the resulting tension. Dislocation glide velocity decreases exponentially with decreasing temperature, and thus the residual thermal expansion strain that remains in a heteroepitaxial film at room temperature can be as high as 90% of the total thermal mismatch.[22] This trapped tensile strain can lead to the formation of microcracks in the epitaxial film, with microcrack nucleation behavior governed by an effective critical cracking thickness similar to that discussed for misfit dislocation formation previously.[23] Thermal mismatch strain can also act to reduce the critical thickness of strained quantum well laser structures fabricated on Si substrates, as will be discussed in Chapter 4.

Some practical ways to account for thermal mismatch strain in the GaAs/Si materials system have been proposed. Slower cooling rates after growth can encourage additional tensile strain reduction by pre-existing misfit dislocations, although practical considerations limit how slowly temperature can be reduced.[24] Growth or device

fabrication on reduced areas can increase the total thickness of the epitaxial layers that can be grown without crack formation.[25,26] The deliberate inclusion of compressive material strain in an epitaxial layer at the growth temperature can act to balance the tensile thermal strain which develops in this layer during cooldown, resulting in a strain-free room-temperature structure.[27] This process has been demonstrated in the thermally mismatched Ge/Si system, but introduces potential complications for high-temperature post-growth device processing and also for the growth of additional epitaxial layers above the strain-balanced film layers.

1.1.3. Differences in Crystal Structure

In addition to the fundamental differences in lattice constant and thermal expansion coefficients that separate Si from GaAs-based semiconductor alloys, there is also the issue of the differing crystal structures of these two semiconductor materials. Because of its compound nature, a GaAs crystal unit cell cannot preserve the inherent symmetry of the Si diamond-cubic lattice. The different bonding energies of Ga and As atoms in relation to each other will give the GaAs crystal structure a more ionic character than Si, and will result in an asymmetric polarity that can cause problems when integrated on a non-polar Si substrate lattice. GaAs crystal structures deposited on Ge semiconductor substrates will face the same polarity problems, irrespective of the smaller lattice constant and thermal expansion mismatches that separate these materials. A complete understanding of polar-on-nonpolar epitaxy is a critical challenge for successful compound semiconductor integration.

The zincblende unit cell of a GaAs crystal can be imagined as two interpenetrating but chemically distinct face-centered-cubic (fcc) sublattices. This arrangement is different from the diamond-cubic Si or Ge unit cell, which can be simplified into two interpenetrating fcc sub-lattices that are functionally and chemically identical. When a GaAs unit cell is deposited on a Si substrate, the GaAs unit cell can therefore be aligned in one of two distinct and perpendicular orientations. Which orientation is produced will depend on the underlying arrangement of the Si substrate atoms and the growth environment of the GaAs film. A surface variation such as an atomic-level step on the Si substrate can cause the GaAs film above this step to rotate its

orientation, and thus lead to the formation of a propagating boundary layer between two distinct GaAs domains. The boundary that separates these adjacent domains will not consist of regular GaAs cation-anion bonds, but instead take the form of an electrically charged 2-dimensional plane of anion-anion or cation-cation bonds. This defective antiphase boundary (APB) plane can serve as a large-scale trapping site to reduce minority carrier lifetime in GaAs device layers,[28] and also act to increase majority-carrier scattering in electronic circuits which include APB defects.[29] A schematic drawing of an APB boundary formed by Ga-Ga bonds above a single-atom substrate step is shown in Figure 1.6.

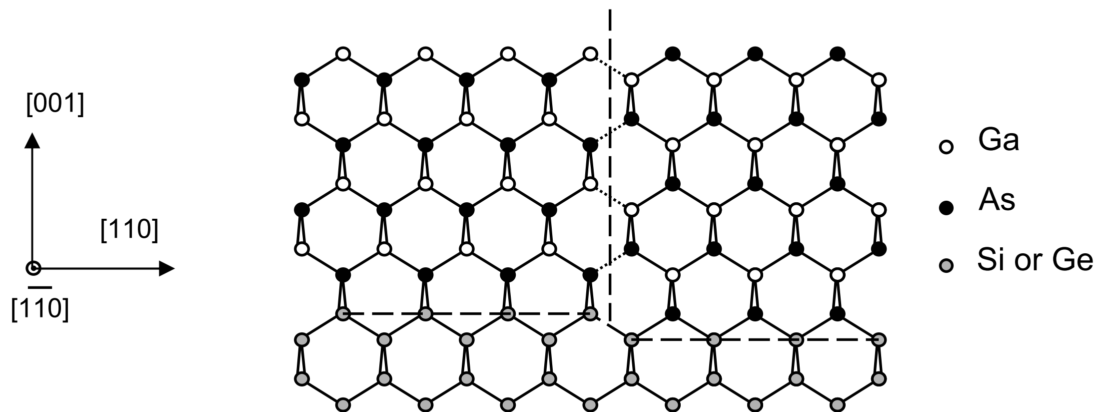

Figure 1.6: Antiphase boundary in GaAs formed by a single-atom step on the substrate surface.

Many authors have investigated substrate preparation recipes and nucleation conditions which can minimize or eliminate the formation of antiphase boundary defects for GaAs/Si and GaAs/Ge epitaxy.[30,31,32] Nucleating a GaAs film on an offcut substrate wafer at a high temperature and with a high ratio of As to Ga source gas flow rates in a chemical vapor deposition system has been shown to yield APB-free epitaxial GaAs on non-polar Ge substrates.[33] A more complete review of this work and a discussion of the key conditions for APB-free polar-on-nonpolar epitaxy will be presented in Chapter 3.

Additional difficulties may arise when atomic species are interchanged at a GaAs/Ge or GaAs/Si interface. Interdiffused Ga can act as a p-type electron acceptor in Ge or Si substrate layers, while As behaves as an n-type electron donor.[7] In GaAs epilayers, Ge or Si are amphoteric dopants, acting as either n- or p-type dopants depending on the lattice site on which they arrive.[34] Ga and As can move into a Ge or Si substrate via solid state diffusion during growth, while Ge or Si atoms can contaminate

GaAs epilayers through diffusion, surface segregation, or vapor phase transport during the deposition process. The autodoping of GaAs device layers during growth on heteroepitaxial substrates has long been recognized as a problem for materials integration experiments,[35] and surfaced as a serious issue for the laser integration experiments carried out for this work. Our efforts to reduce autodoping effects in integrated GaAs devices on Si, and the work of previous researchers facing similar challenges, will be reviewed in Chapter 3.

1.2. Strategies for III-V/Si Integration

Despite the significant differences in lattice structure, lattice constant, and thermal expansion characteristics that obstruct the successful integration of III-V semiconductors on Si, much work has been done to overcome or bypass these differences and achieve useful GaAs optoelectronic device layers on Si substrates. While many attempts have proven too costly or impractical, some have demonstrated limited success, and one strategy in particular, using relaxed compositionally graded buffer layer substrates, currently holds the greatest promise for realizing useful GaAs-based semiconductor lasers on Si substrates. It is possible to consider all of the previously published integration attempts by first separating them into two basic categories.

Hybrid integration schemes rely on separately grown and fabricated GaAs device structures that are attached via bonding or solder-bump metal layers to Si CMOS circuits. Monolithic integration techniques rely on the epitaxial growth or bonding of GaAs device layers onto Si substrates before any processing has taken place. Hybrid integration schemes have been used to successfully demonstrate integrated III-V optoelectronic devices on Si, including working GaAs-based semiconductor lasers.[6] Despite these successes, hybrid integration schemes remain limited due to their inherent expense and the complexity of the packaging-intensive methods that must be used to place and bond discrete optoelectronic devices on fabricated Si circuits. Monolithic integration techniques by contrast are self-aligned and easily scaled to high device densities and large-area processes.

Numerous techniques for monolithic III-V on Si integration have been proposed. Early work focused on the direct epitaxy of GaAs device layers on Si, while more recent work has investigated wafer-level bonding techniques along with a host of unproven epitaxial shortcuts. In all cases, the chief goal for integration has been to control the high threading dislocation densities that result from the large GaAs/Si lattice mismatch.

1.2.1. Dislocation Control Strategies for Monolithic Integration

As mentioned previously, the 4.1% lattice mismatch between a GaAs film and a (001) Si substrate will yield threading dislocation densities in the GaAs device layers on the order of 10^9–10^{10} cm^{-2}. Dislocation interactions can act to reduce this number slightly by annihilation reactions in which two dislocations with opposite Burgers vectors collide and cancel each other out.[36] Two glissile threading segments can also combine to form a single sessile segment, thereby reducing the overall threading dislocation density.[11] Thicker GaAs layers will increase the statistical likelihood of dislocation collisions, and thus early dislocation control experiments investigated the use of thick GaAs buffer layers to reduce surface dislocation densities.[37] Unfortunately, this technique can only reduce dislocations that remain mobile throughout the growth process and that are present in high enough densities to interact favorably with each other. Thermal expansion mismatch between GaAs and Si sets an upper limit on how thick a GaAs buffer on Si can be without cracking, and the best thick buffer experiments were therefore unable to reduce threading dislocation densities below 10^8 cm^{-2}.[38] Threading dislocations can be reduced slightly from this value by thermal cycle annealing, in which GaAs film growth steps are alternated with high-temperature (~800 °C) annealing steps to increase misfit and threading dislocation motion and encourage dislocation interactions at the interfaces of the annealed layers.[39] Strained layer superlattices, in which alternating layers of thin strained $In_xGa_{(1-x)}As$ or AlAs alloys are inserted between GaAs layers to encourage dislocation motion towards the wafer edges, have also been investigated but offer no apparent improvements to earlier threading densities.[40] The best efforts of the initial direct GaAs integration work on Si were able to reduce overall threading dislocation densities to 10^7 cm^{-2} in thick thermal-cycle-annealed GaAs epitaxial layers; a density

which was still at least an order of magnitude too high for useful minority carrier device integration.[38]

An alternate way to encourage dislocation reduction in mismatched heteroepitaxial films is to reduce the surface area available for epitaxial growth in relation to the perimeter of the resulting growth region. With increased perimeter length, and the proper growth conditions, there is an increased likelihood that misfit dislocations will glide to the edges of a mismatched film without nucleating threading dislocations. Pre-existing threading dislocations will also be more likely to terminate at the edges of the crystal instead of climbing all the way to the surface of the epitaxial film. Epitaxial films grown on reduced substrate areas can demonstrate dramatic reductions in threading dislocation densities,[41] but the associated reduction in the area available for device fabrication limits this technique's usefulness for all except certain optoelectronic structures with very small footprint areas. Epitaxial lateral overgrowth (ELO), in which mismatched films grown in artificially confined small areas are allowed to spread laterally over an oxide or nitride mask layer can increase the surface area available for device integration. But ELO techniques introduce their own complications including high defect densities at the interfaces between the laterally grown regions and sidewall dislocation nucleation from the masking layers.[42]

In recent years, certain authors have suggested epitaxial shortcut schemes in which a novel intermediary layer is inserted between GaAs epitaxial layers and the Si substrate to somehow absorb or neutralize the mismatch strain and stop dislocation propagation into the GaAs film.[43,44] To date, none of these techniques has been proven to conclusively reduce lattice mismatch strain or threading dislocation densities in GaAs device layers, and no practical integrated minority carrier devices have been demonstrated on these reported structures.

Wafer bonding of unprocessed GaAs device structures to Si has also been suggested as a potential technique for integration,[45] but will remain impractical for high-volume optoelectronic integration due to continuing difficulties with bonding yield, and poor mechanical strength and thermal stability at the wafer-bonded interfaces. Bonded wafer technology will also be limited by differences in the GaAs and Si wafer sizes available for bonding.

In contrast to other techniques, relaxed, compositionally-graded buffer layers have been shown to successfully reduce threading dislocation densities for integrated device structures to levels below those necessary for basic minority carrier device operation.[46] By incrementally introducing mismatch strain to an epitaxial layer during the growth process, and encouraging material relaxation at each incremental growth step, threading dislocations in the epitaxial layers can be recycled to avoid further nucleation or multiplication reactions. The individual layers in a compositionally graded buffer act to suppress dislocation interactions instead of promoting them, and high degrees of mismatch strain relaxation can be achieved without increasing the overall threading dislocation density. Unlike other techniques, graded buffer layers are not fundamentally limited in their potential reduction of threading dislocation densities for a set amount of material mismatch because they do not rely on a minimum dislocation density to ensure efficient dislocation interaction. A schematic diagram of a compositionally graded buffer layer on a mismatched substrate is shown in Figure 1.7. Note how a threading dislocation from the substrate extends its misfit length at each interface, increasing the strain relaxation without increasing the overall threading dislocation density.

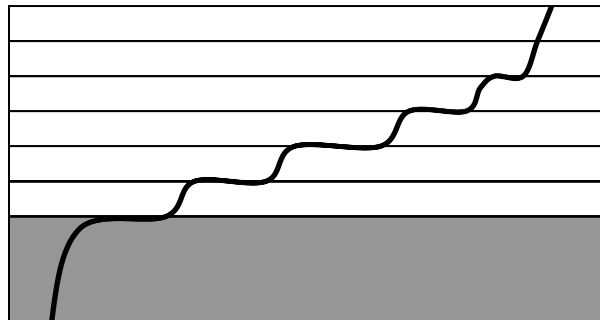

Figure 1.7: Cross-sectional schematic of a relaxed graded buffer layer grown on a mismatched substrate. A threading dislocation from the substrate is shown moving into the graded buffer and extending its misfit segment length without nucleating additional threads.

Relaxed compositionally graded buffer layers have been demonstrated in a number of strained, miscible alloy systems, including GeSi, InGaAs, and InGaP.[46,47,48] The GeSi materials system is a particularly interesting system for the potential integration of GaAs-based devices on Si substrates. The lattice constant of Ge is only 0.07% larger than the lattice constant of GaAs, and thus a compositionally graded $Ge_xSi_{(1-x)}$ buffer layer with a final Ge composition of x_{Ge}=1.0 could provide a high-quality, low

dislocation density virtual substrate for subsequent GaAs device epitaxy. Continuing research in this group has successfully produced relaxed graded Ge/GeSi/Si substrates suitable for monolithic III-V/Si integration, and these structures have acted as the foundation for the work reported in this thesis.

1.3. Relaxed $Ge_xSi_{(1-x)}$ Graded Buffers for III-V/Si Integration

Ge is an ideal intermediary material between GaAs and Si due to its close lattice match with GaAs and its complete miscibility with Si. Producing a high-quality, low dislocation density Ge/GeSi relaxed graded buffer layer on a Si substrate requires a comprehensive understanding of the dislocation dynamics acting throughout the graded buffer growth process and a growth system capable of generating the proper conditions to maintain low threading dislocation densities during the graded buffer growth process. Maintaining low threading dislocation densities requires maximizing the kinetics for dislocation glide in the buffer layers while minimizing the nucleation rate of new threading dislocations in the growing film. Both high growth temperatures and relatively low strain grading rates will serve to increase the effective dislocation glide velocity at graded buffer interfaces.[49] Increasing the overall dislocation glide velocity in a graded buffer will increase the total misfit segment lengths of the existing dislocations in relation to their threading lengths, and these dislocations will be thus be able to efficiently relieve large amounts of misfit strain before reaching the surface of the epitaxial film.

Minimizing the nucleation of new threading dislocations during the graded buffer growth process will require that pre-existing dislocations can move easily through the film without being pinned at localized dislocation pileups. Dislocation pileups have been shown to occur partly as a consequence of surface roughness, which occurs naturally in high-quality graded buffer layers.[14] This surface roughness usually takes the form of an orthogonal network of parallel ridges and troughs on the graded buffer surface and is commonly referred to as “crosshatch” surface roughness. Crosshatch roughness is caused by the low residual amounts of strain which remain in the top layers of a graded buffer during epitaxial growth.[50] At the growth temperature, this residual elastic strain attempts to relax by introducing gentle undulations in the film surface. These undulations remain

energetically favorable in the graded buffer despite the resulting increase in surface energy. The constant strain rate in a graded buffer film allows this corrugated surface pattern to propagate through the growing film to the top of the buffer, where it has been observed for a number of different epitaxial materials systems.[50,51,52] Work in this research group has shown that the crosshatch roughness pattern can have a negative effect on dislocation nucleation by acting to pin threading dislocations at the surface of a growing graded buffer film.[14] Once pinned, the misfit segments below these threading dislocations can no longer glide to relieve further mismatch strain, and additional dislocation segments must therefore be nucleated to continue the relaxation process.

One way to avoid dislocation pinning at surface crosshatch features is to remove this surface crosshatch roughness during the growth process. By halting the growth at intermediate graded buffer compositions and polishing the buffer surface with a chemical-mechanical polishing (CMP) process, dislocation pileup formation has been dramatically reduced in graded $Ge_xSi_{(1-x)}$ buffer structures.[53] Relaxed graded buffer structures produced using this procedure show only slight increases in threading dislocation density with increasing Ge fraction from 50–100%, indicating that threading dislocation nucleation has been effectively minimized in these optimized graded buffer layers.

To achieve the high growth temperatures and low growth rates necessary for optimal $Ge_xSi_{(1-x)}$ graded buffer growth on Si substrates, our group has developed a unique ultra-high-vacuum chemical vapor deposition (UHV-CVD) growth system. The characteristics of this system permit high-quality Ge/GeSi/Si graded buffer growths on multiple 4” or 6” Si substrates with grading rates of 10% Ge per micron and growth temperatures between 550°-800 °C. A cross-sectional transmission electron microscope (TEM) image of a GeSi graded buffer on Si with a 1 μm Ge cap suitable for III-V integration is shown in Figure 1.8.

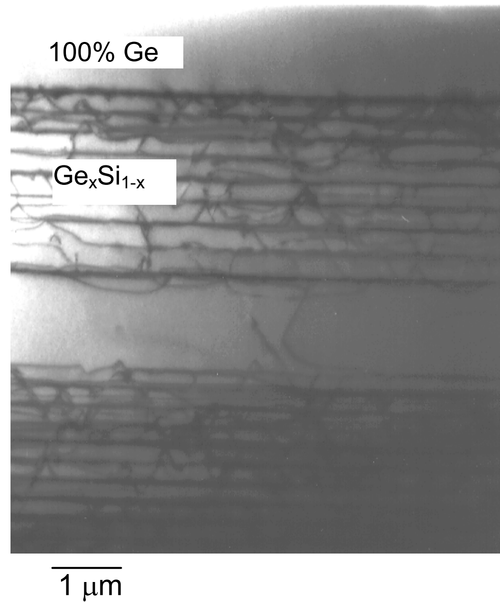

Figure 1.8: Cross-section TEM micrograph of a Ge/GeSi/Si graded buffer structure grown in the UHV-CVD growth reactor. The thick band in the center of the image is the CMP polished region at x_{Ge}=50%.

The cross-sectional image shows the network of misfit dislocations that exist along the graded buffer interfaces, but no obvious threading dislocations reaching the surface of the Ge cap layer. Cross-sectional TEM is a poor measurement technique for detecting low densities of threading dislocations however, and more accurate values for the actual threading dislocation density at the surface of a graded buffer structure can be arrived at with a combination of plan-view TEM imagery and defect-selective wet chemical etching of the surface. Studies of the graded Ge/GeSi layers on Si substrates used in this work have measured surface threading dislocation densities of 1×10^6 cm^{-2}. This number is an order of magnitude lower than any numbers previously reported for GaAs epitaxial integration on Si substrates (with nearly identical total lattice mismatch). Such a low dislocation density therefore offers a promising potential route for high-quality III-V/Si integration.

1.4. GaAs Integration on Ge/$Ge_xSi_{(1-x)}$ Buffers on Si

Integration experiments with GaAs films epitaxially integrated on optimized relaxed graded Ge/GeSi buffer layers on Si substrates have yielded promising results

pointing the way towards the ultimate goal of practical laser operation on Si. GaAs films grown via molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD) have both been demonstrated on Ge/GeSi/Si substrates, and the basic material characteristics of these integrated III-V/Si structures have been extensively characterized. Sieg was the first to report GaAs integrated directly on Ge/GeSi/Si substrates, which were grown under a high As flux rate in a standard MBE growth chamber.[31] These first films showed relatively high threading dislocation densities in the resulting GaAs films ($>10^7$ cm^{-2}) as well as high densities of APB defects originating at the GaAs/Ge interfaces. Improved growth recipes making use of migration-enhanced-epitaxy (MEE) were then reported by Carlin,[54] who measured surface threading dislocation densities for 3 μm-thick GaAs/$Al_{0.3}Ga_{0.7}As$ double heterostructure films on Ge/GeSi/Si substrates of 5×10^5–2×10^6 cm^{-2}. Carlin also measured minority carrier lifetimes in these integrated GaAs/Ge/Si structures by time resolved photoluminescence, and was able to report record long minority lifetimes of 10.5 ns, comparable to results for GaAs/AlGaAs structures on GaAs substrates. Transmission electron microscopy and secondary ion mass spectroscopy (SIMS) analysis of these films showed atomically sharp interfaces with little GaAs/Ge atomic intermixing and no evidence of antiphase boundary formation.

The minority carrier lifetimes recorded for these first GaAs/AlGaAs heterostructures on Ge/GeSi/Si are particularly important because they imply that minority carrier trapping at threading dislocations is no longer an overriding factor in these optimized III-V/Si materials. With lower threading densities and therefore larger average separation between threading dislocations in the surface GaAs/AlGaAs layers of these films, it is possible that minority carriers no longer diffuse far enough to reach a threading dislocation before recombining radiatively inside the GaAs/AlGaAs device structures. This change in carrier behavior will be critical for producing the minority carrier densities necessary to achieve laser operation in GaAs-based device layers. Longer minority carrier lifetimes should also mean a reduction in the carriers available to drive dark line defect propagation in laser active regions. A graph showing the measured minority carrier lifetimes for GaAs/AlGaAs heterostructures on Ge/GeSi/Si substrates as a function of the surface threading dislocation density is shown in Figure 1.9. The reported minority carrier lifetimes of previous work with GaAs structures grown directly

on Si are presented for comparison. Important to note is the saturation behavior for minority carrier lifetime that seems to occur for threading dislocation densities less than 10^5–10^6 cm^{-2}. If the effective minority carrier diffusion length is shorter than the mean dislocation spacing in GaAs epilayers with dislocation densities approaching 10^6 cm^{-2}, further reduction in substrate threading dislocation densities may not be necessary to achieve bulk-GaAs luminescence efficiency values on Ge/GeSi/Si substrates.

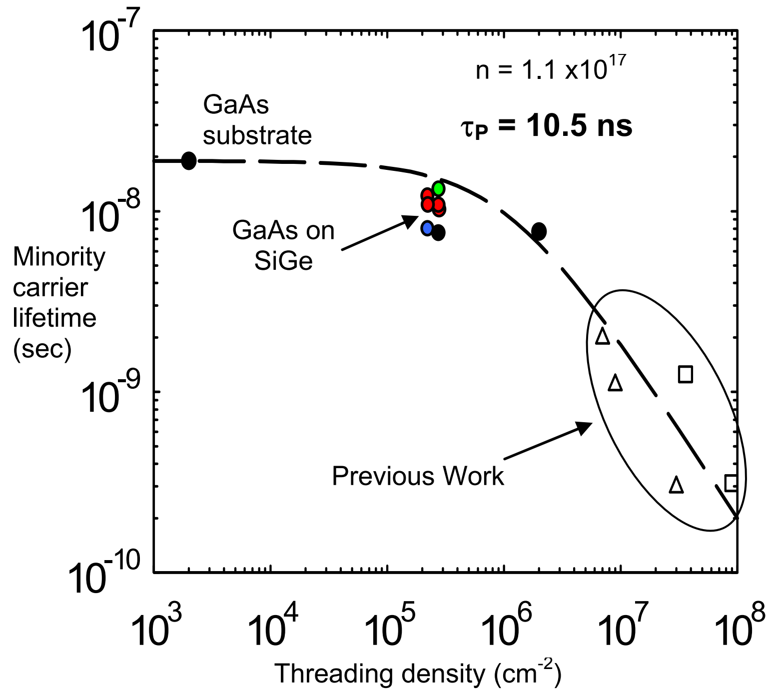

Figure 1.9: Minority carrier lifetime as a function of measured threading dislocation densities for a variety of GaAs heterostructures grown on Si substrates (courtesy of Carlin[54]). The points labeled "previous work" reflect reported data in the literature for GaAs growth directly on Si.

Similar work with GaAs device layers integrated on Ge/GeSi/Si substrates using an atmospheric MOCVD growth system has been reported by Ting.[55] Using a high growth temperature on a Ge/GeSi/Si substrate offcut 6° towards the [110] direction, Ting reported APB-free GaAs film growth with threading dislocation densities of 2×10^6 cm^{-2} measured by defect-selective wet chemical etching and plan-view transmission electron microscopy.[24] GaAs *pn*-junction diode materials fabricated on Ge/GeSi/Si substrates in the same manner showed good forward and reverse current–voltage characteristics, with reverse saturation currents as low as 2.6×10^{-5} A/cm^2 and diode ideality factors of 1.7.

Identical devices on GaAs substrates demonstrated essentially identical behavior, and calculated ideality factors of 1.8.

Recent work by Yang has detailed the first fabrication of integrated GaAs/AlGaAs optical links on Si substrates using relaxed graded Ge/GeSi buffer layers. [56] These optical link structures consisted of a matched GaAs *pin* light emitting diode and photodetector connected by an $Al_{0.15}Ga_{0.85}As$ waveguide layer grown on a Ge/GeSi/Si substrate. The successful operation of these potential data-link structures demonstrated LED operating efficiencies of 3 μA/W, and total waveguide losses of 144 dB/cm.

1.5. Goals and Scope of this Thesis

It is clear from the above review that GaAs integration on Ge/GeSi relaxed graded buffer layers on Si substrates holds great promise for the future demonstration of practical integrated III-V optoelectronic devices on a Si CMOS platform. This thesis has sought to continue the advances of the early integrated device reports while pursuing the ultimate objective of a practical GaAs-based semiconductor laser structure on Si. The goal of the work reported in this thesis was therefore to successfully demonstrate a GaAs-based edge-emitting laser diode on a Ge/GeSi/Si substrate, and to comprehensively characterize this laser in comparison to identical laser structures fabricated on standard GaAs substrates. Chapter 2 of this thesis discusses the experimental procedures and apparatus used to grow the III-V device layers used in this work. Chapter 3 details the optimized nucleation and growth procedures developed for GaAs MOCVD epitaxy on Ge/GeSi relaxed graded buffer layers, and the significant difficulties encountered with Ge autodoping behavior in the integrated GaAs device layers. Chapter 4 explains the work done in fine tuning the thermal expansion behavior of the integrated GaAs device layers on Ge/GeSi/Si substrates, and the issues encountered with defect-resistant $In_xGa_{(1-x)}As$ alloy layers grown on these Ge/GeSi/Si substrates. Chapter 5 covers the optical confinement and waveguide design optimization that was carried out to ensure that high-quality GaAs films on Ge/GeSi/Si substrates would also have the optical gain and waveguide loss characteristics necessary for laser operation. In Chapter 6, the fabrication and testing of actual integrated GaAs/AlGaAs and InGaAs/GaAs/AlGaAs laser structures

on Ge/GeSi/Si substrates is presented, along with comparisons to similar laser structures grown on standard GaAs substrates, and preliminary lifetime tests for all tested devices. Chapter 7 offers some conclusions and suggested directions for future work.

Chapter 2. Growth and Characterization of III-V films on Ge/GeSi/Si substrates

2.1. Introduction

All of the semiconductor device structures deposited for this work were grown in a metal-organic chemical vapor deposition (MOCVD) reactor. MOCVD is a particularly attractive technique for the fabrication of GaAs-based laser structures on a wide variety of semiconductor substrates due to its immense flexibility.[57] Deposition temperatures can be varied from 400 °C to 800 °C at operating pressures ranging from 76 millibar to atmospheric pressure. Rapid and precise changes in the composition and growth rate of deposited films are possible with simple changes in gas flow rates and chamber temperatures, and very low levels of incorporated impurities are easily achieved with modern purified sources.

This chapter details the application of MOCVD epitaxial deposition to the GaAs-based device structures grown for this work. Given the wide variety of process parameters that depend on the specifics of the CVD reactor chamber design, the particular configuration of the Thomas Swan MOCVD research reactor used for our experiments is described in detail. A brief discussion of the characterization methods used to investigate film quality after growth is also included.

2.2. Metal-Organic Chemical Vapor Deposition

The driving mechanism for metal-organic chemical vapor deposition is the pyrolytic decomposition of injected precursor gasses on a heated substrate surface. A single-crystal substrate surface acts as a template for pyrolysis reactions and the subsequent deposition of epitaxial film layers, at compositions set by the partial pressures of the precursor gasses and the reaction kinetics on the surface. In an MOCVD reactor, the Group III elements are typically carried to the substrate surface by metal-organic precursor gasses, while the Group V elements are carried by purified hydrides. As an example of the MOCVD reaction process, a simplified GaAs deposition reaction can be written as:

$$Ga(CH_3)_3[g] + AsH_3[g] \rightarrow GaAs[s] + 3CH_4[g]$$

In this reaction, the Ga precursor molecule is trimethylgallium (TMGa); other common metal-organic precursors include trimethylindium (TMIn), and trimethylaluminum (TMAl). The hydride gas that carries As to the surface is arsine, which can be replaced by phosphine (PH_3) or ammonia (NH_3) for GaP or GaN-based alloys. The reaction equation above is a simplified description of the actual pyrolysis reaction that takes place on the substrate surface. Closer investigations have shown that many intermediate reactions occur in the gas phase and at the growth surface before the final products are generated.[58]

Because the pyrolysis reactions that drive MOCVD growth are thermally activated, substrate temperature is one of the most important variables for controlling epitaxial deposition during film growth. At low temperatures (< 500 °C), pyrolysis reactions are slow and inefficient, while the sticking coefficient for impinging precursor gas molecules on the substrate surface is very high. This means that the limiting reaction rate in the multi-step pyrolysis process will limit the deposition rate at low substrate temperatures. The growth rate in the low-temperature, reaction-limited regime will thus be a superlinear function of growth temperature, and small local temperature variations on the substrate surface may lead to dramatic and unpredictable growth changes in the deposited film. By contrast, growth at higher temperatures will typically be mass-transport limited, as rapid reaction rates ensure that nearly every precursor molecule that diffuses to the surface and sticks undergoes a pyrolysis reaction. The precursor flow rates, along with the hydrodynamic boundary layer thickness above the substrate and the gas sticking coefficients at the surface will determine the deposition rate in the mass transport-limited regime. Transport-limited growth depends only weakly on substrate temperature and allows both growth rate and composition control via simple changes to the precursor gas flow rates. Most of the epitaxial growth done for this work took place under transport-limited growth conditions.

Another important variable for compound semiconductor growth via MOCVD is the ratio of the group V species to group III species at the substrate growth surface. The precursor gas V/III ratio at the surface has important effects on film stoichiometry, surface kinetics, and defect and impurity incorporation. In the mass transport-limited growth regime, the group III species are immediately incorporated into the growing film,

and the partial pressure of the group III species at the growth surface is essentially the vapor pressure of the solid. A large excess flow of group V species is typically used, so the actual V/III ratio at the growth interface is independent of the flow of the group III species and entirely dependent on the group V species flow.[57] Optimized V/III gas ratios for GaAs film growth on a variety of substrates have been reported in the literature, and different authors have reported V/III ratios varying over nearly two orders of magnitude for different MOCVD systems.[55,59,60] To understand the variance in the literature, it is important to recognize that these reported gas flow ratios are invariably calculated using the precursor flow rates into the reactor chamber, and not the measured V/III ratio at the film surface. Other growth process parameters, such as the substrate temperature, reactor chamber operating pressure, and carrier gas velocity will have strong effects on how much of each precursor species diffuses from the chamber atmosphere to arrive at the substrate surface. This means that an optimized V/III gas flow ratio will remain specific to the MOCVD chamber and growth conditions present during optimization, and will (in general) not be the same for different growth systems. The optimization of the V/III gas flow ratio for the Thomas Swan MOCVD reactor used in this work will be described in more detail in Chapter 3, and compared to the optimized V/III ratios reported by other authors.

The deliberate and the unintentional incorporation of impurities into epitaxial films during MOCVD growth both play important roles in the fabrication of practical optoelectronic devices from these epilayers. Intentional doping of film layers with donor and acceptor impurity atoms is vital for creating p- and n-type material for a diode or transistor active region, while the unintentional incorporation of atmospheric impurities such as oxygen or carbon can compensate deliberate doping levels and degrade operating device performance.

In a typical MOCVD reactor, donor and acceptor atoms are introduced to the growing film via dilute metal-organic or hydride carrier gasses. For the GaAs-based devices investigated in this work, p-type doping was achieved with dimethylzinc (DMZn) precursors, while n-type doping was introduced to the growing films with 1% dilute silane (SiH_4) in hydrogen. Doping with silane is relatively straightforward, since the extremely low vapor pressure of Si results in mass transport-limited doping.[61] N-doping

in MOCVD-grown GaAs films is thus directly proportional to the silane flow in the reactor chamber and inversely proportional to the growth rate. P-doping in GaAs films using dimethylzinc is slightly more complicated in MOCVD-grown GaAs, due to the high vapor pressure and fast diffusion rates of Zn.[62] P-doping levels in GaAs depend strongly on DMZn flow rates and growth temperature, as well as the effective partial pressure of the dimethylzinc precursor at the growth surface. Once incorporated, Zn is easily compensated by oxygen impurities, and can also move rapidly through device layers via solid-state interstitial diffusion.[63]

Unintentional incorporation of impurities during the MOCVD growth process may occur in many ways. The most studied atmospheric contaminant is oxygen, which is present in desorbed water vapor in the reactor chamber and as an impurity in the precursor sources themselves. Electrically active incorporated oxygen can compensate intentional dopants, leading to high intrinsic resistance in critical device layers, and has also been linked to increased surface roughness in growing GaAs films.[64] Oxygen incorporation is highest in alloyed films with high aluminum concentrations and can be reduced by increasing growth temperatures to sublimate aluminum-oxygen complexes before they can be incorporated in $Al_xGa_{(1-x)}As$ device layers. Published reports have shown direct links between the amount of oxygen incorporated in the AlGaAs cladding regions of a GaAs/AlGaAs quantum well laser structure and the laser threshold current of operating devices.[65] It will therefore be critical to minimize the incorporation of atmospheric oxygen in integrated epitaxial GaAs-based laser structures. High-temperature pre-growth bakeouts of the reactor chamber and growth susceptor, high $Al_xGa_{(1-x)}As$ layer growth temperatures of 750 °C, and certified high-purity precursor source gasses were all employed in this work to ensure low oxygen contamination levels in MOCVD-grown laser device layers.

Other unintentional contaminants which are typically found in epitaxial semiconductor films grown by MOCVD methods include carbon, nitrogen, and hydrogen. Carbon is a basic ingredient in the methyl groups of the metal-organic precursor gasses, and its ability to act as a p-type electron acceptor in GaAs films makes its unintentional incorporation troublesome at high concentrations. Proper choice of

growth temperatures and V/III ratios can both act to reduce carbon incorporation during deposition.[58]

2.3. Thomas Swan MOCVD Research Reactor

The MOCVD chamber used for this work was an atmospheric pressure cold-wall Epitor™ research reactor manufactured by Thomas Swan. The growth chamber is a horizontal quartz tube with an angled lamp-heated graphite susceptor that holds the semiconductor substrate. The top of the reactor chamber is water-cooled to reduce unwanted deposition reactions and precursor depletion across the substrate wafer. A schematic drawing of the reactor chamber is shown in Figure 2.1.

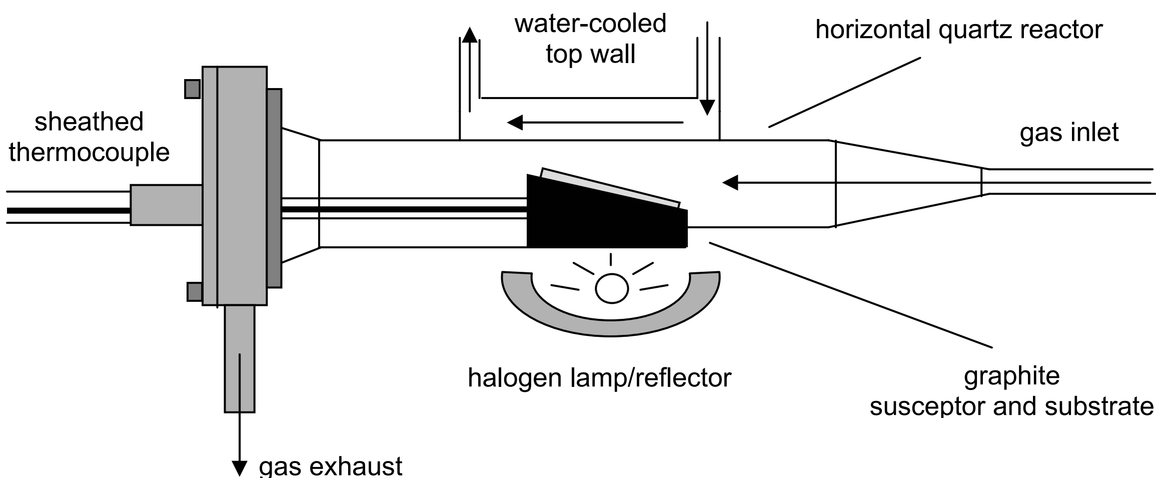

Figure 2.1: Schematic diagram of the Thomas Swan MOCVD growth chamber used in this work. The reactor operates at atmospheric pressure.

The temperature in the reactor is maintained via a thermocouple enclosed in a quartz sheath which is inserted into the back of the heated graphite susceptor. The thermocouple is connected through a temperature controller to a 1000W halogen lamp that provides rapidly variable radiant heating of the susceptor and thus maintains the desired substrate temperature. Source gasses are delivered at the inlet of the reactor tube, which flares out to a rectangular cross-section capable of holding substrate pieces as large as 1.5 × 2 cm. The source gasses are provided to the reactor by a fast-switching stainless steel gas manifold. All gas flow rates are controlled by high-precision mass flow controllers and are delivered to the reactor in steel lines held at slightly elevated

temperatures to reduce precursor condensation. The metal-organic source gasses are supplied to the manifold from liquid bubblers, through which H_2 carrier gas is forced at a controlled temperature and pressure to generate metal-organic vapor streams with precursor concentrations easily calculated from the known liquid vapor pressures and the ideal gas equation. The hydride sources are delivered from compressed gas cylinders stored in external gas cabinets.

The relatively small size and simple operation of this Thomas Swan research reactor enables easy maintenance and cleaning, and allows for unmatched flexibility in the types of structures and growth conditions available to the experimenter. A major drawback to this design, however, is the small size of the growth chamber and the constraint of atmospheric-pressure operation. The reduced area of the allowed semiconductor substrates exposes a large fraction of the total surface area to unwanted edge effects; non-uniform temperature gradients and shifts in the gas boundary layer thickness near the reactor walls can lead to sharp thickness and composition gradients across the deposited film surface, further reducing the useful area available for device fabrication and complicating film characterization efforts.

The MOCVD film deposition procedure used for the device structures grown in this work varied depending on the specific layer structures being grown, and more detailed descriptions of the particular growth recipes used for each experiment will be discussed in later chapters. A general summary of a typical GaAs growth procedure is presented below. To begin, a GaAs or Ge/GeSi/Si substrate wafer was cleaved into a suitably sized piece for the reactor chamber and cleaned with a wet chemical solution to remove the uppermost substrate layers and expose a fresh surface for deposition. GaAs substrates were cleaned for 1 minute in a 1:10 deoxidizing solution of HCl and de-ionized water (DI), followed by a 10-second dip in a 1:1:25 etching solution of H_2O_2:DI:H_2SO_4. The high concentration of sulfuric acid in this etch ensures that it remains diffusion-limited and etches relatively slowly. The samples were then dipped briefly in the deoxidizing solution before a final 2-minute rinse in de-ionized water. Ge/GeSi/Si substrates were prepared for growth by successive 30-second dips in 30% dilute H_2O_2 and HF acid solutions, separated by de-ionized water rinses. The final dip in the HF acid solution left the Ge surface hydrophobic and hydrogen-passivated for subsequent GaAs

nucleation. Before loading the cleaned substrate into the reactor, the reactor chamber and graphite susceptor were baked at a temperature of 850 °C for 15 minutes to drive out any adsorbed water in the chamber. After placing the cleaned substrate wafer on the baked susceptor, the reactor was closed and switched from a nitrogen to a hydrogen carrier gas ambient atmosphere and the temperature was raised to 200 °C for five minutes to desorb any residual water introduced during loading. For GaAs substrates, all further growth steps occurred under an arsine overpressure to prevent arsenic depletion at the substrate surface. Ge/GeSi/Si samples remained under a pure hydrogen atmosphere until the actual initiation of GaAs film growth. To prepare for film growth, the temperature of the substrate was then raised to 700 °C and held for at least five minutes to allow the surface to equilibrate with its proper surface reconstruction. The temperature and duration of the pre-growth annealing step are key variables for ensuring high-quality GaAs nucleation, as will be explained in Chapter 3. While the substrate was being annealed, the initial gas flows for nucleation were equilibrated in the manifold and passed into the reactor vent line. To begin growth, the equilibrated trimethyl and hydride gas flows were switched from the vent line to the reactor chamber, and growth proceeded with the growth rates and film compositions set by the precursor gas ratios.

2.4. Material Characterization

A wide variety of techniques were used to characterize the epitaxial films grown for this work. Information on surface morphology, layer thickness, defect density, residual strain, and intrinsic luminescence was gathered for many different device structures and aided the ultimate goal of producing a successfully integrated GaAs-based laser on Si.

2.4.1. Surface Morphology

The surface morphology of semiconductor structures can be evaluated with a wide variety of microscopic techniques. Differential interface contrast (DIC) optical microscopy can allow sensitive large-scale evaluation of surface microstructure features including crosshatch roughness, dislocation pileups, and surface step bunching. Vertical

surface features as small as a few nanometers can be observed at magnifications up to 1000X using DIC methods. For increased depth of field and higher overall resolution, scanning electron microscopy (SEM) can be used to evaluate film surfaces and facet edges. SEM systems can also be paired with spectrometers and x-ray detectors to enable enhanced surface characterization via cathodoluminescence or x-ray fluorescence spectroscopy. Nearly atomic-scale resolution of semiconductor surface features is possible with atomic force microscopy (AFM), which can be used to quantitatively study small-scale crosshatch roughness and surface step bunching behavior at length scales from 100 μm to less than 1 μm.

A Zeiss Axioplan optical microscope with a digital camera and differential interface contrast sliders was used for the optical characterization done in this work. The SEM used to study surface morphology and facet mirror roughness of fabricated laser structures was a tungsten-filament JEOL 5300. The AFM used to investigate crosshatch surface roughness on Ge/GeSi/Si substrates was a Digital Instruments Dimension 3000 Nanoscope IIIa AFM operating in tapping mode.

2.4.2. Device Structure

The internal structure of a semiconductor epilayer, including the quality of the various internal interfaces and the behavior of crystallographic dislocations at these interfaces can be observed with cross-section transmission electron microscopy (TEM). With properly prepared cross-sections, TEM can provide sub-nanometer resolution capable of accurately measuring thin quantum well structures and distinguishing individual misfit and threading dislocations. The preparation of useful TEM microscope samples and the proper alignment of the microscope electron beam optics to produce high-quality images is a complex process requiring extensive hands-on experience and has been reviewed in detail by Williams and Carter.[66] The high magnification of modern transmission electron microscopes results in relatively small sampling areas in prepared microscope samples, and thus limits the usefulness of cross-sectional TEM for accurate measurements of semiconductor threading dislocation densities at any levels below 10^8 cm^{-2}. This limit is important to consider when reviewing many of the early reports of reduced threading dislocation densities for integrated GaAs films grown on Si substrates.

In many reports the only characterization evidence offered as proof for the remarkably low measured density values are a series of cross-sectional TEM images.[37,67] More accurate dislocation density measurements are only possible with plan view TEM correlated with defect-selective etching, as will be detailed below.

The TEM used for this work was a JEOL 2000FX operating at 200kV. High-resolution lattice images of thin quantum well structures were taken with a JEOL 2010FX digital microscope capable of 1.2 MX magnification. Microscope samples were prepared by mechanical thinning to less than 50 μm, followed by mounting on a copper handling grid and further polishing to electron transparency thicknesses of 1 μm or less using a Gatan precision ion polishing system.

2.4.3. Crystallography and Strain

X-ray diffraction is the most direct and accurate way to characterize the crystallographic quality and residual strain in a deposited semiconductor epilayer. High-energy monochromatic x-rays diffracted off the epilayer surface will generate a pattern of diffraction peaks that can be measured and quantified to yield precise information on the symmetry, lattice spacing, orientation, and crystalline quality of the epilayer and substrate crystals. Triple-axis x-ray diffraction, in which the diffracted beam from the sample being measured is passed through an additional analyzer-collimator crystal before being measured, allows for the generation of unique three-dimensional reciprocal space maps of the diffracted x-ray beams at the sample surface and the precise measurement of residual strain, alloy composition, and crystallographic tilt in the most complex graded buffer structures. The theory and operation of x-ray diffractometers have been reviewed in detail by Bowen,[68] and strain and tilt characterization through triple-axis x-ray diffraction has been discussed in detail by van der Sluis.[69]

The X-ray diffraction system used to characterize the structures grown for this work was a Bede D^3 triple-axis x-ray diffractometer with dual-channel cut Si collimator crystals and a rotating Cu anode x-ray generator operating at 60kV and 200mA.

2.4.4. Dislocation Characterization

The characterization of misfit and threading dislocation densities is a key tool for heteroepitaxial integration experiments, and extra care must be taken to ensure accurate

dislocation density measurements for the highly mismatched epitaxial structures investigated in this work. As mentioned above, cross-section TEM is not useful for dislocation density characterization at densities less than 10^8 cm^{-2}. Plan-view TEM is slightly more sensitive to lower dislocation densities, due to the increased sample area visible in the low-magnification plan-view images. With careful thinning from the back of the deposited film, surface dislocation densities lower than 10^7 cm^{-2} can be accurately measured with this method. Even lower dislocation densities can be measured with defect-selective etching, in which a selective wet etching solution is used to preferentially attack the area of higher surface energy that surrounds each threading and misfit dislocation at the film surface. Molten potassium hydroxide has been used to successfully reveal threading dislocations on GaAs surfaces,[70] and photo-activated chromic acid etchant solutions have also been reported.[71] Defect selective etching can be sensitive to the local electrochemical environment at the film surface, and the presence of very high surface dislocation densities can actually reduce etchant selectivity to yield artificially low apparent threading dislocation densities. For this reason, threading densities measured via etch pit density methods should always be correlated with another defect-measurement technique to ensure complete accuracy.

Dislocation densities measured for this work were gathered via both plan-view TEM and defect-selective etching. Twenty or more plan-view images were taken at low magnifications ($<$ 10 kX) at random locations across each microscope sample to ensure good measurement statistics and low standard deviations. The etching chemistry used to reveal surface dislocations on GaAs and InGaAs surfaces was a solution of chromic acid, hydrofluoric acid, and water at a ratio of 2:1:8, which was exposed to the surface under a high-intensity tungsten lamp to drive the photo-activated etching process.[24] Multiple DIC micrographs were then taken of the etched surfaces and the total number of revealed threading dislocation pits were counted for each photograph.

2.4.5. Optical Characterization

Optical luminescence characterization techniques provide a fast, non-destructive method for evaluating the basic qualities of optoelectronic device structures without complex device fabrication steps. Photoluminescence (PL) uses a short wavelength laser

to create high densities of electron-hole pairs in the surface layers of a semiconductor film. These photogenerated carriers recombine in the active regions of the device structure by emitting photons at energy levels characteristic of the material bandgap, with intensities directly proportional to the overall film quality and the effective minority carrier lifetime in the material.[72] PL can be used to calculate the composition of thin or strained quantum well structures (assuming the well thickness is known) and to compare the luminescence efficiency of direct-bandgap films integrated on different substrate materials. Similar characterization data can be attained with cathodoluminescence (CL) techniques, in which carriers are injected with a focused electron beam in a scanning electron microscope, and the resulting emitted photons are collected and analyzed with an attached optical spectrometer.[73] The very small and tightly focused excitation spot of the SEM electron beam enables easy quantization of CL spectral data, and offers the potential of two-dimensional CL maps of surface luminescence by scanning the electron beam across the sample while recording the total emitted photon intensity.

Both PL and CL methods were used to characterize the integrated laser structures grown for this work. The photoluminescence system was a homemade apparatus with a 1W Ar-gas laser operating at a wavelength of 488 nm. Spectrum data was collected with a SPEX Compudrive 1702 spectrometer attached to a photomultiplier tube. Samples were mounted in a cryostat which enabled PL measurement at room temperature or liquid helium temperatures (4 K) to suppress thermal broadening. The CL system consisted of an integrated Oxford MonoCL spectrometer attached to a photomultiplier tube. Only room temperature measurements were possible with this system.

Chapter 3. Optimizing Epitaxy for GaAs/Ge/Si Integration

3.1. Introduction

The first requirement for successful GaAs epitaxy on Ge/GeSi/Si substrates is a high-quality GaAs/Ge interface. A good interface will be free from all types of material defects except for required misfit dislocations, and show a sharp material transition from the Ge substrate to the GaAs film above it. This chapter will discuss some of the epitaxial optimization steps which have been proven to control anti-phase boundary formation, as well as our experimental work investigating the effects of temperature and flow conditions on atmospheric MOCVD growth and Ge autodoping in GaAs films.

3.2. Background: GaAs Nucleation on Ge/GeSi/Si

3.2.1. Ge Substrate Surface

As mentioned in Chapter 1, Ge crystals have their atoms arranged in a diamond-cubic crystal structure which can also be imagined as two equivalent interpenetrating fcc unit cells. The reduced symmetry at the crystal surface encourages the top layers of Ge atoms to rearrange to minimize the number of dangling bonds. The surface of a clean on-axis (001) Ge wafer will actually consist of wide planar terraces of Ge-Ge dimer pairs separated by irregularly spaced single atomic layer steps.[74] The dimerization axis of the Ge-Ge bonds at a (001) Ge surface can be parallel or perpendicular to the [110] atomic step edges, depending on the orientation of the unit cell directly below them. At each step transition, the dimerization axis will rotate by 90 degrees, forming alternating terraces of parallel and perpendicular Ge-Ge dimers. A representation of a reconstructed Ge surface showing the rotated dimer axes is shown in Figure 3.1.

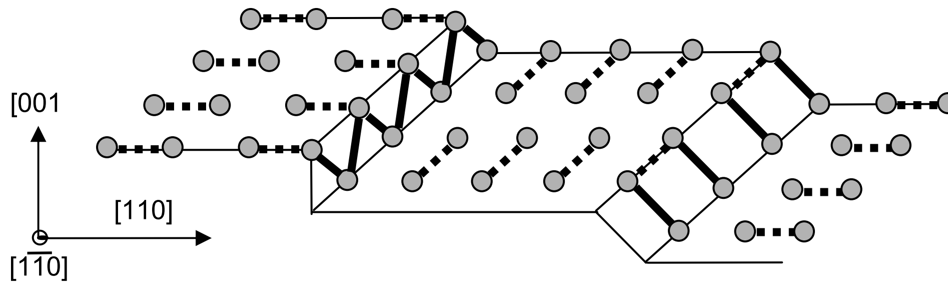

Figure 3.1: Schematic diagram showing single atomic layer steps on a (001) Ge surface. Note the rotation of surface dimers which occurs at the single steps.

3.2.2. GaAs Film Alignment on a Ge Substrate Surface

The atoms in a bulk GaAs crystal take the same positions as those in the diamond-cubic Ge lattice, but the GaAs compound structure, with its distinct anion and cation sites, reduces the symmetry of the unit cell. Exchanging the Ga anion positions with the As cations in the zincblende unit cell has the same effect as rotating the unit cell by 90 degrees. A representation of this effective cell rotation via cation-anion exchange is shown in Figure 3.2. When growing a GaAs film on Ge, the effective reduction of symmetry at the interface forces the GaAs unit cell to assume one of two distinct and perpendicular orientations. Which of these orientations occurs depends on the underlying orientation of the Ge substrate as well as the initiation conditions of the GaAs film. For example, the rotation of Ge-Ge dimer orientations across a single step on the Ge substrate surface can lead to a matching rotation of the GaAs unit cells above this step. The boundary which then forms between the adjacent rotated GaAs domains will not consist of regular cation-anion bonds; it will instead form a charged 2-D plane of anion-anion or cation-cation bonds. This anti-phase boundary (APB) will propagate through a growing GaAs film on Ge to form electrically active planar defects capable of significantly reducing minority carrier lifetimes in operating semiconductor devices and of increasing majority-carrier scattering.[29] A schematic drawing of an APB formed by Ga-Ga bonds above a single atom step is shown in Figure 3.3.

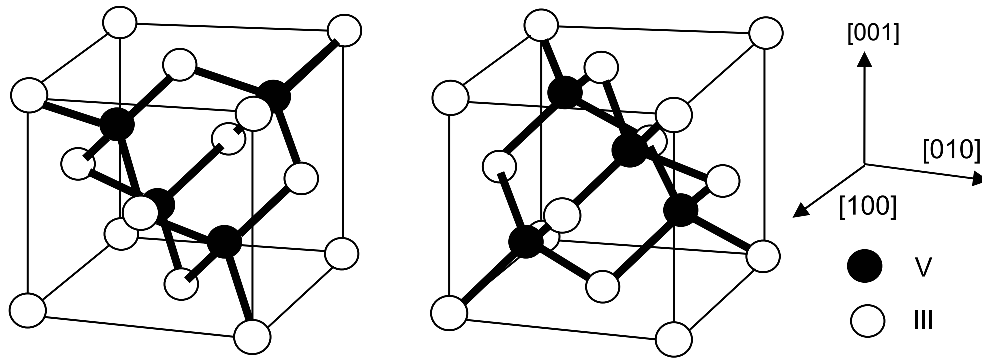

Figure 3.2: The two possible orientations of the GaAs zincblende unit cell.

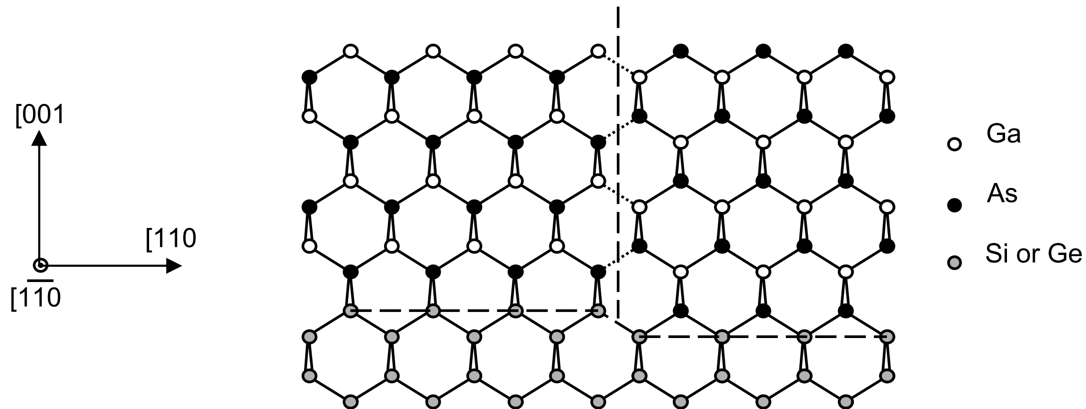

Figure 3.3: An antiphase boundary in GaAs formed by a single atom step on a Ge surface. Adjacent As-As and Ga-Ga bonds will create a charged planar defect propagating upwards from the interface.

3.2.3. Controlling Anti-phase Boundary Formation at the GaAs/Ge Interface

Controlling anti-phase boundaries requires controlling the structure of the Ge substrate surface before growth as well as controlling the nucleation environment during GaAs growth initiation.

A number of authors have investigated controlling the structure of the Ge substrate surface for APB-free GaAs nucleation. The goal of most work has been to achieve single-domain Ge-Ge dimer orientations across all surface step boundaries. Single-domain Ge surfaces, with all Ge-Ge dimers in the same orientation to the [110] step edges can be created by converting the single-steps of a native (001) Ge surface into double atomic steps. With all dimer pairs aligned the same way, GaAs films deposited on these Ge surfaces will no longer undergo domain rotation at Ge surface step edges, and anti-phase boundaries will not form.[55] This desired double-step arrangement is

illustrated in Figure 3.4. Surface step structure can be controlled macroscopically by introducing deliberate offcut to the (001) Ge wafer. When a (001) Ge wafer is offcut by a few degrees towards one of the [110] directions, the formerly irregular array of surface steps is converted to a regularly-spaced series of parallel single-atom steps in the offcut direction. The spacing of the steps w, is a direct function of the offcut angle θ, and step height d :

$$w = d \tan\theta$$

If the offcut angle is chosen properly, the single-step Ge surface structure will, when heated to temperatures typical for epitaxial growth, lower its surface energy by reordering into larger terraces separated by double atomic steps. Chadi has shown that a single-domain, double-step Ge surface structure is energetically favored for [110]-offcut substrates heated above 600 °C in high vacuum.[75]

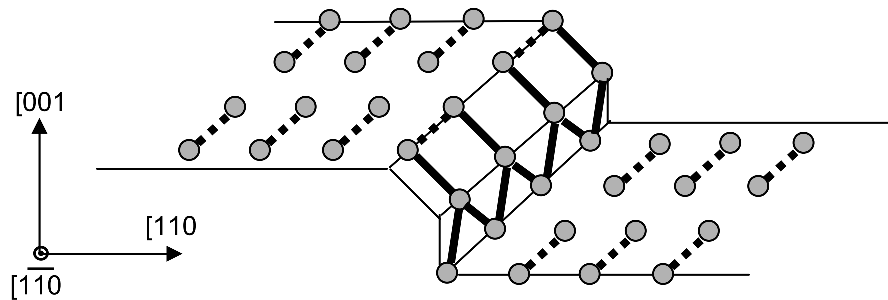

Figure 3.4: A double atomic layer surface reconstruction on a Ge surface. Note the parallel Ge-Ge dimers on both sides of the terrace. GaAs nucleated on this surface will not form an antiphase boundary at the step edge.

While a single-domain, double-step Ge surface is necessary for APB-free GaAs growth on Ge, it is not by itself sufficient. The nucleation environment during GaAs growth initiation will also affect anti-phase boundary formation. If different areas of a growing GaAs film encounter different initial Ga and As exposures, anti-phase boundaries can form where Ga-initiated films border As-initiated regions.[24] Due to the higher vapor pressure of As and its tendency to self-terminate with monolayer coverage on a Ge surface, short arsenic pre-exposures are typically used in MOCVD growth to ensure As-initiated nucleation across the Ge surface. When a clean single-domain Ge surface is exposed to As, the impinging As atoms form As-As dimer pairs on the surface.[76] However, depending on the nucleation conditions, the orientation of these As-As dimers can be rotated by 90°, conditional on whether the As adatoms form additive or

displacive bonded pairs with the underlying Ge atoms.[77] It is therefore clear that to achieve truly single-domain APB-free GaAs nucleation on Ge, careful attention must be paid to both the Ge surface preparation and the GaAs nucleation environment.

A number of authors have investigated the surface conditions and nucleation environment necessary for APB-free GaAs growth on Ge.[31,30,28,33] Li has shown that high-quality GaAs films can be nucleated by choosing a significant (> 3°) substrate offcut, high growth temperature (> 650 °C), relatively low growth rate (< 2μm/hr) and a high AsH_3/TMG gas ratio of 60:1, using AsH_3-initiated growth.[28] Other authors have confirmed these requirements, while pointing out some additional factors.[59,60] Pelosi has shown that for a growth temperature of 600 °C, the V/III gas flow ratio has a critical impact on the interface quality.[59] High V/III ratios were shown to produce As-rich initial films, with the excess Ga vacancies condensing to form high densities of planar stacking fault defects at the interface. Excessively low V/III ratios also caused problems in these experiments, yielding high densities of misfit and threading dislocations (which often split into Shockley partials separated by stacking faults) at the interface. Chen has investigated the effects of GaAs initiation temperature for atmospheric GaAs/Ge MOCVD growth.[60] His work showed the existence of a narrow temperature window (640 °C−680 °C) for optimal GaAs nucleation. Temperatures below this window produced high levels of surface roughness and low photovoltages in fabricated solar cells, while high temperatures yielded similar increases in roughness with falling photovoltages.

Work by Ting in our research group has demonstrated high-quality, APB-free GaAs nucleation on Ge/GeSi/Si substrates.[55] The optimized conditions for growth in our MOCVD reactor required (001) Ge/GeSi/Si substrates 6° offcut in the [110] direction. The MOCVD growth process began with a short pre-growth anneal at a temperature above 600 °C to promote double-step Ge surface ordering, followed by As-initiated GaAs deposition at a temperature less than 500 °C (which yields single-domain GaAs with steps parallel to the offcut axis) or greater than 600 °C (which yields single-domain GaAs with steps perpendicular to the offcut axis). A cross-section TEM micrograph of a high-quality GaAs film grown on a Ge/GeSi/Si substrate is shown in Figure 3.5.

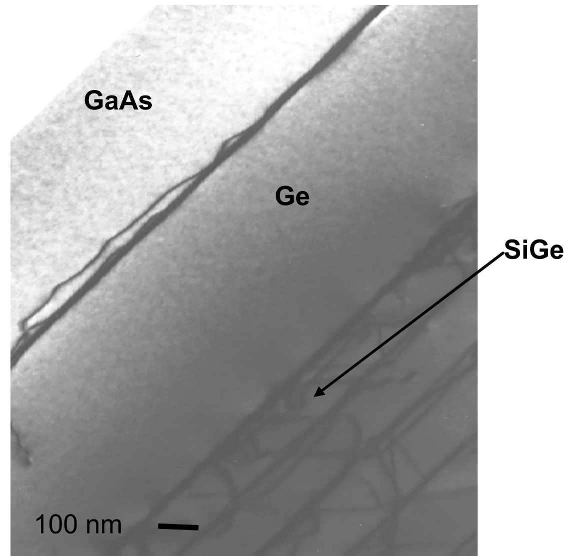

Figure 3.5: Cross-sectional TEM image of a GaAs film grown on a Ge/GeSi/Si substrate.

3.3. Low-Temperature Nucleation Experiments

As discussed above, the nucleation environment plays a key role in setting the quality of a GaAs film grown on a Ge substrate. Using our MOCVD reactor, Ting demonstrated specular, APB-free GaAs films on Ge/GeSi/Si nucleated at temperatures below 500 °C. However, upon closer inspection, these films were not defect-free. High densities of stacking faults (~10^6 cm^{-2}) forming inverted periods with their tips at the GaAs/Ge interface have been seen with plan-view TEM for many films grown using a low-temperature initiation step, as seen in Figure 3.6. A stacking fault is a planar defect caused by the introduction of an extra plane of atoms into an epitaxial lattice. Stacking faults are defined by the partial dislocations which bound them, and thus can be either Frank-type (**b** = 1/3<111>) or Shockley-type (**b**=1/6<121>), depending on how they are formed.[36] The stacking fault pyramids observed in the low-temperature nucleated GaAs appear to be sessile Frank-type stacking faults, and form characteristic "bow-tie" patterns when viewed from above with plan-view TEM with **g**=[022]. After observing the existence of these stacking faults at the interface of our GaAs/Ge films, we began a series of experiments to better understand the conditions that led to their formation.

Figure 3.6: Plan-view TEM image of a GaAs film on Ge/GeSi/Si substrate with a high density of pyramidal stacking fault defects. Depending on the orientation of the stacking fault planes with respect to the electron beam they will appear as squares or hourglass shapes in the plan-view microscope image.

All samples were grown in the atmospheric pressure MOCVD reactor described in the previous chapter. The substrates used were Ge/GeSi/Si relaxed graded buffer structures grown on standard Si substrates 6° offcut towards the [110]. MOCVD growth began with a 5 minute anneal under a H_2 atmosphere at a temperature of 650 °C, followed by a rapid temperature decrease to the nucleation temperature (between 400 °C-500 °C), and immediate initiation of AsH_3 and then TMG gas flows. The V/III gas ratio was varied from 275 to 1000, and the pre-growth annealing atmosphere was also varied by introducing small amounts of AsH_3 for certain samples.

The results of these experiments are summarized in Table 3.1:

Table 3.1: Low temperature GaAs/Ge nucleation experiments

Sample	Pre-growth anneal (5 minutes)	V/III gas flow ratio	Nucleation Temp (°C)	Stacking Fault density (cm^{-2})
0503vy1	5000 sccm H_2	550	400	3×10^6
0530vy2	10000 sccm H_2	550	400	1×10^7
0531mg195	5000 sccm H_2	550	450	4×10^5
0601vy1	5000 sccm H_2 and 25 sccm AsH_3	550	400	2×10^7
0602mg197	5000 sccm H_2	275	400	3×10^6
APCVD-8	5000 sccm H_2	1000	400	2×10^6
APCVD-11	5000 sccm H_2 then 10sec TMG first	550	400	8×10^8

It can be seen from the table that the density of the stacking fault pyramids remained high for all of the low-temperature initiation growths, despite their specular appearance and optically smooth surfaces. The lowest measured value of 4×10^5 cm^{-2} for sample 0531mg195 was the only sample nucleated at a higher temperature of 450 °C, but samples grown above this temperature showed considerable surface roughness, consistent with the earlier observations by Ting.[24] The most important variable for controlling stacking fault nucleation during low-temperature initiation appeared to be the pre-growth annealing environment. Adding additional gas to the mixture flowing over the sample surface, either in the form of increased H_2 carrier flows or small amounts of AsH_3, acted to increase the average stacking fault density by nearly an order of magnitude. The highest stacking fault density of 8×10^8 cm^{-2} was measured for a sample that included a brief 10-second TMG exposure at the end of the pre-growth anneal. In contrast, increasing or decreasing the AsH_3 gas flow after nucleation appeared to have almost no measurable effects on stacking fault densities.

It is clear from these results that the pre-growth annealing conditions are critical in defining the nucleation behavior of a low-temperature GaAs film on Ge. Work by Pelosi investigating atmospheric-pressure MOCVD growth of GaAs films on Ge may help us to understand why this is true.[59] Although growing at a much higher temperature of 600 °C, Pelosi showed that changes in the V/III gas flow ratio at nucleation can introduce surface non-stoichiometries which lead to stacking fault generation. He suggested that these stacking faults nucleate at the edges of GaAs islands at the earliest stages of GaAs growth. Work by Timo, also at higher temperatures, agreed that stacking fault nucleation in GaAs/Ge growth begins at the edges of GaAs islands before these islands coalescence into a uniform 2D film.[78]

Considering the low-temperature nucleation results measured in our experiments, it is possible to suggest some interpretations for this data. At the low temperatures at which our growths took place, epitaxy can be expected to proceed via surface reaction limited growth.[58] Under these conditions, the sticking coefficients for As and Ga atoms on the Ge surface will essentially be unity, with very little of the As desorption that characterizes growth at higher temperatures. This means that the 3D island growth of the initial GaAs monolayers will be very sensitive to local inhomogeneities or non-

stoichiometries. Microscopic defects or small islands of As-rich material will have strong effects on localized growth rates, and stacking faults will nucleate rapidly so long as Ga and As atoms do not have the thermal energy to relax to their lower-energy equilibrium lattice positions. The pre-growth Ge surface structure, including the presence or absence of metastable As-As dimer monolayers, will play a key role in determining whether or not stacking fault pyramids can form. Flowing AsH_3 or TMG during the pre-growth annealing step may change this surface structure or shift the surface stoichiometry enough to increase stacking fault nucleation, as we observed.

None of the samples measured in this work had a stacking fault density low enough to permit useful GaAs device integration on Ge/GeSi/Si, and thus it is clear that while acceptable for creating single-domain APB-free GaAs on Ge, low-temperature MOCVD GaAs nucleation is not capable of producing useful GaAs/Ge interfaces in the temperature regime below 500 °C.   For this reason we chose to focus on the high temperature (> 600 °C) nucleation of GaAs films on Ge for our next experiments.

3.4. High Temperature Nucleation Experiments.

Using our MOCVD reactor, Ting has demonstrated high-quality, APB-free GaAs films on Ge/GeSi/Si nucleated at temperatures above 600 °C.[55] Similar experiments by Li and Chen have confirmed the necessity of nucleation temperatures above 600 °C for optimal GaAs/Ge growth.[28,60] Chen in particular has shown that a narrow window of nucleation temperatures (640 °C−680 °C) offers the best conditions for atmospheric MOCVD GaAs/Ge growth. Nucleation temperatures outside this window showed increasing amounts of GaAs surface roughness as well as decreased device performance. The optimal nucleation temperature window was shown to be independent of the temperature of the pre-growth anneal step.[60] Atmospheric MOCVD growth by Pelosi, discussed above, has shown the importance of choosing a proper V/III gas flow ratio to avoid the generation of stacking fault structures at the GaAs/Ge interface.[59]

MOCVD growth of GaAs films on Ge/GeSi/Si substrates at temperatures between 625 °C-700 °C was performed for this work to investigate more carefully the optimal conditions for high-quality GaAs film nucleation on Ge surfaces. All samples were

grown on 6° offcut Ge/GeSi/Si substrates in the atmospheric MOCVD system described in Chapter 2. Nucleation temperatures and pre-growth anneal temperatures were varied from 620 °C-700 °C, and pre-growth annealing times were varied from 5 to 10 minutes. The V/III gas flow ratios were also varied from 60 to 225 for certain samples. The results of these high-temperature nucleation experiments are summarized in Table 3.2:

Table 3.2: High-temperature nucleation experiments

Sample ID	Pre-growth anneal temperature. (°C)	Growth temperature (°C)	V/III gas flow ratio	Surface appearance	Stacking faults (PV-TEM)
1111mg170	620 (5 minutes)	620	60	Very rough	
0122mg240	650 (5 minutes)	650	115	Very rough	
0114mg235	650 (5 minutes)	650	225	Very rough	9×10^7 cm^{-2}
0123mg243	675 (5 minutes)	675	225	slightly rough	$< 3 \times 10^3$ cm^{-2}
0125mg245b	650 (5 minutes)	700	225	Smooth	
0125mg245a	700 (5 minutes)	650	225	Very rough	
0302mg264	700 (5 minutes)	700	225	Smooth	$< 3 \times 10^3$ cm^{-2}
0125mg245c	700 (10 minutes)	700	225	slightly rough	

It can be seen from the table above that the best GaAs films on Ge were grown with high growth temperatures and high V/III ratios. Lower temperatures (< 675 °C) and V/III ratios produced very rough surfaces and high densities of interfacial stacking faults. The best conditions for high-quality films without interfacial defects were a 5-minute pre-growth anneal at 700 °C, followed by GaAs initiation at the same temperature with a V/III ratio of 225. As discussed by Chen, film quality appeared to be less dependent on pre-growth annealing conditions at high temperatures.[60] Films grown with lower annealing temperatures but high nucleation temperatures showed high surface quality, while low nucleation temperatures produced uniformly rough surfaces, independent of whether the pre-growth anneal temperatures were high or low. Extended high-temperature annealing (10 minutes at 700 °C) did appear to degrade surface morphology. This degradation sets an upper bound on the annealing time possibly due to background AsH_3 roughening of the Ge substrate.[33] Surface images and plan-view TEM photographs of sample 0114mg235, grown at 650 °C, are compared with images from sample 0302mg264, grown at 700 °C in Figure 3.7. There is a direct correlation between the presence of a rough surface morphology and high levels of defects at the GaAs/Ge interface. This correlation has been confirmed by other authors working in the GaAs/Ge system,[60,78] although our earlier experiments did not show an increase in surface

roughness with increasing stacking fault densities for low-temperature GaAs initiation. It is likely that the higher growth rates present in our high-temperature nucleation experiments act to magnify the roughness features due to material defects near the interface.[60] Plan-view TEM photographs were not taken for every sample because the correlation between surface roughness and interface quality is expected to hold, and our primary goal was simply to find the optimal conditions for high-quality GaAs/Ge high-temperature nucleation.

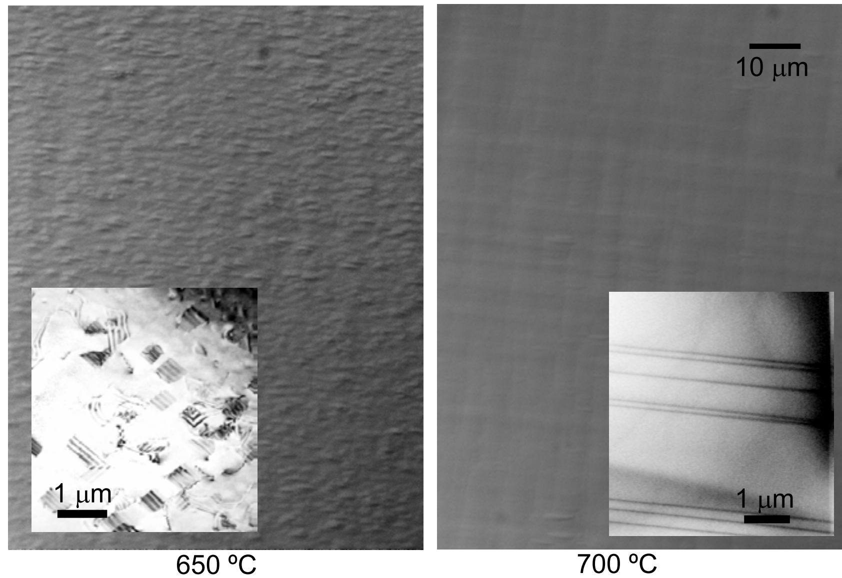

Figure 3.7: Optical micrographs and plan-view TEM images (inset) of GaAs films grown on Ge/GeSi/Si substrates at 650 and 700 ºC. Note the high density of stacking faults correlated with a visibly rougher GaAs film surface for the film nucleated at 650 ºC.

From the results of our high-temperature nucleation experiments it was apparent that high-quality GaAs film growth on Ge/GeSi/Si substrates is possible under specific optimized conditions. Similar to Li,[28] we have shown that high V/III ratios, high nucleation temperatures, and offcut substrates are necessary to avoid anti-phase boundary or stacking-fault formation at the GaAs/Ge interface and consequential surface roughness. Differences in gas flow patterns and temperature gradients in our MOCVD reactor make direct comparison of the ideal V/III ratios and nucleation temperatures calculated by other authors to our growth system difficult. However, the results of our low- and high-temperature nucleation experiments enabled us to define the optimum GaAs nucleation conditions for device-quality film integration on Ge/GeSi/Si substrates.

These nucleation conditions were used for all of the laser devices integrated on our Ge/GeSi/Si substrates, as will be described in later chapters.

3.5. Optimizing GaAs Nucleation to Control GaAs/Ge Interdiffusion and Autodoping

Atomic intermixing occurring at the GaAs/Ge interface has been recognized as a possible source of contamination for integrated GaAs/Ge device structures since the earliest attempts to fabricate such structures.[35] Early experimental work investigating GaAs device growth on Ge substrates via MBE was the first to quantify this intermixing behavior and its effects on device structures.[79,80] Chand showed that GaAs films grown at 500 °C on offcut Ge substrates show high levels of Ge contamination, an effect which was attributed to Ge diffusion and surface segregation during growth.[79] As a Group IV atom, Ge acts as an amphoteric dopant in GaAs, replacing Ga atoms to act as a n-type electron donor, or exchanging with As atoms to become an electron acceptor. Chand observed these doping effects in *np* diodes fabricated from this material, which showed *npnp* thyristor-like behavior due to Ge moving into deliberately n-doped GaAs layers to convert them to p-type layers, while As atoms diffused into the p-Ge to render it n-type. Later work with MBE GaAs/Ge growth also showed significant interfacial intermixing at growth temperatures of 600 °C.[80] Ge contamination of the GaAs overlayers was determined to arise chiefly from surface segregation, which occurs when Ge atoms exchange places with depositing Ga or As atoms and ride the growth front into the GaAs device layers. Solid-state diffusion of Ge into the GaAs was shown to play a minor role in the observed intermixing behavior, a result which was confirmed by Jaeger, who showed that the solid-state diffusion of Ge into GaAs is very slow, even at temperatures above 800 °C.[81] More recently, Sieg has shown that with the proper choice of MBE nucleation conditions, Ge segregation can be minimized to yield high-quality Ge-free GaAs device layers on Ge substrates.[31] Sieg used a migration-enhanced epitaxy process to nucleate the initial GaAs monolayers at low temperatures and was able to demonstrate Ge contamination levels in GaAs films below detectable limits when measured via SIMS depth profiling and Polaron C-V measurements. It is therefore clear that while GaAs/Ge

intermixing is a significant issue during MBE growth, proper choice of the GaAs nucleation conditions can control any long-range contamination effects of the Ge substrate atoms in GaAs device layers.

The growth of GaAs/Ge integrated device structures using MOCVD introduces additional pathways for Ge incorporation into GaAs films. The chief new pathway is Ge transport in the vapor phase, which can occur as a consequence of the much higher temperatures and pressures of the MOCVD growth method, combined with the high fluxes of reactive carrier gasses and pyrolysis by-products that are always present during MOCVD growth. Vapor-phase transport of substrate contaminants during epitaxy was first reported in halide-CVD experiments involving highly-reactive Cl-based carrier gasses.[34,82] Srinivasan reported autodoping behavior for As dopants carried in the vapor phase from Si substrates with both SiH_4 and $SiCl_4$ precursor gasses.[82] He showed that vapor phase transport was strongly dependent on the time and temperature of the pre-epitaxial annealing step, which controlled how much of the substrate dopant atom was carried into the vapor for later deposition. Kasano showed similar vapor-phase autodoping behavior for Ge in GaAsP films grown on Ge substrates, and was subsequently able to demonstrate reduced Ge contamination by passivating the back Ge surfaces of his wafers before growth.[34] Theoretical work by Carlson has investigated the thermodynamic driving forces for vapor phase transport during chemical vapor deposition, and has shown that both the growth temperature and the area of exposed source material will determine how much of the substrate material will be carried into the growing film during growth.[83]

More recent CVD growth experiments in reactor systems similar to our own have continued to explore the nucleation conditions that can lead to vapor-phase transport of Ge substrate atoms into growing GaAs films.[33,78,84,85] Timo has shown Ge incorporation in GaAs films grown using low-pressure MOCVD at growth temperatures of 700 °C.[78] Similar contamination effects were reported by Hudait with low-pressure growth at temperatures between 600 °C - 775°C.[33] Based on SIMS depth profiles, Hudait argued that the Ge was moving into the GaAs film chiefly by diffusion through Ga-vacancies, although this mechanism seems unlikely considering the slow diffusion rates of Ge in GaAs.[81] Hudait observed that the conditions necessary for high-quality, APB-free GaAs

nucleation on Ge (high temperatures, high V/III ratios, and low growth rates) are unfortunately also the best conditions to encourage GaAs/Ge intermixing and autodoping effects. Atmospheric MOCVD growth of GaAs/Ge solar cell structures by Tobin showed strong evidence of uniform vapor-phase contamination in 6 μm-thick GaAs device layers.[84] SIMS depth profiles showed Ge contamination levels higher than any of the deliberate doping levels at the solar cell junctions for MOCVD growth temperatures higher than 700 °C. Electrical characterization of fabricated devices confirmed that the incorporated Ge atoms were acting as electron donors in the GaAs. Tobin was able to show an order of magnitude reduction in the autodoping levels of Ge in GaAs devices by passivating the back sides of his Ge wafers with deposited GaAs films, thereby reducing the substrate area available as a source for vapor-phase transport. Autodoping via vapor-phase transport has also recently been reported by Azoulay for GaAs films grown on Si substrates by atmospheric pressure MOCVD. Azoulay has shown uniform Si contamination throughout 4 μm-thick GaAs diode structures grown on offcut Si substrates, and has suggested that the vapor phase transport of Si into the growing GaAs film occurs via surface reactions with the H_2 carrier gas:[85] $Si\ [s] + H_2\ [g] \leftrightarrow SiH_4\ [g]$

From this brief review of the literature it is therefore clear that GaAs/Ge intermixing will be a serious issue for the MOCVD growth of GaAs devices on Ge/GeSi/Si substrates, and experimental work in this group has confirmed that Ge autodoping does occur in our growth reactor and must be considered when optimizing GaAs nucleation on Ge/GeSi/Si.

3.6. Experiments to Control Autodoping in GaAs/Ge Growth

3.6.1. Characterizing GaAs/Ge Device Structures with Autodoping Contamination

InGaAs/AlGaAs light-emitting diode (LED) structures were grown on (001) Ge/GeSi/Si substrates offcut 6° towards the [110] direction. These LED structures were initiated at a growth temperature of 700 °C following a 5 minute pre-growth anneal at the same temperature. A 500 nm GaAs buffer layer was grown on the Ge surface, followed

by a 1.1 μm Si-doped $Al_{0.6}Ga_{0.4}As$ optical cladding layer grown at 750 °C to minimize oxygen incorporation into the AlGaAs. The temperature was then reduced to 650 °C over an interval of 5 minutes with all trimethyl sources turned off. A 100 nm undoped GaAs spacer was then grown, followed by a single 8 nm-thick $In_{0.2}Ga_{0.8}As$ quantum well active region, bounded on the other side by another 100 nm GaAs buffer. Growth was then halted for 5 minutes while raising the temperature to 750 °C for another 1.1 μm $Al_{0.6}Ga_{0.4}As$ cladding layer, this time doped with TMZn to yield p-type material. Growth was completed with a 100 nm heavily doped p-GaAs contact layer. Identical structures were grown using the same procedure on commercial n-doped (001) GaAs substrates to act as control samples. All samples were characterized with SIMS depth profiles using Cs^+ ion sputtering to provide accurate concentration vs. depth profiles with a detection limit of less than 10^{16} atoms/cm^3. Simple edge-emitting LED devices were also fabricated with these samples by contacting the p-GaAs cap with evaporated Ti/Au metal stripe contacts over an oxide mask and evaporating Au/Ge on the back of the sample to form backside contacts. The devices were then cleaved into bars and tested by varying the injected electron current while measuring the resulting diode voltage and emitted light intensity. A schematic of the LED structures after processing is shown in Figure 3.8.

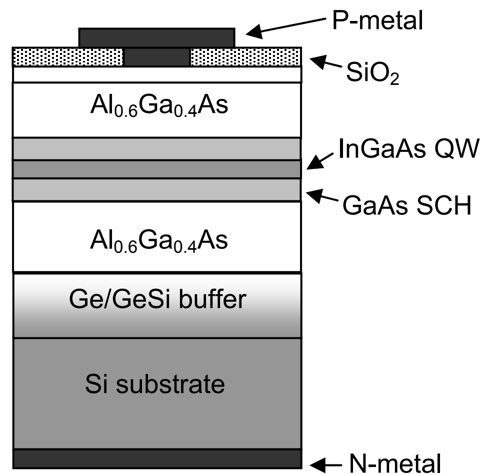

Figure 3.8: Schematic cross section of a GaAs/AlGaAs LED device structures grown on a Ge/GeSi/Si substrate. Identical devices were fabricated on n-doped GaAs substrates.

The SIMS depth profiles of the LED structures grown on the Ge/GeSi/Si substrate showed high levels of Ge incorporation completely through the device structure.

Decreasing from an initial peak value of 2 x 10^{19} cm^{-3} at the GaAs/Ge interface, the Ge contamination level remained essentially flat at about 4 x 10^{18} cm^{-3} through the AlGaAs cladding layers, with higher incorporation of nearly 1 x 10^{19} cm^{-3} in regions where the growth rate was reduced during growth, namely the region around the InGaAs active layer and in the final p-GaAs cap. A plot of the SIMS depth profile is shown in Figure 3.9. Noticeable in this plot is the absence of any significant decrease in the background Ge concentration with increasing distance from the substrate. Contamination behavior dominated by diffusion from the substrate would be expected to show an exponential decrease in concentration with distance.[86] Instead the flat concentration profile indicates a steady contamination source in the reactor environment that is not the Ge substrate surface (which is rapidly covered in the first moments of epitaxy). Vapor-phase transport from other parts of the MOCVD reactor is the most likely mechanism for the observed Ge incorporation, especially after observing that peaks in the Ge incorporation occur in regions where the growth rate was reduced by reducing the total Group III precursor flows. When the Group III precursor flows are reduced, the partial pressure of background contaminants will rise, and Ge-incorporation in the growing film will increase, assuming transport-limited film growth and a steady source of Ge-contamination in the reactor. The source of this Ge contamination is impossible to determine directly, but possible sources include the Ge/GeSi film on the back of the substrate wafer (an unavoidable consequence of the UHVCVD graded buffer growth process), the graphite susceptor beneath the substrate, or the walls of the reactor chamber.

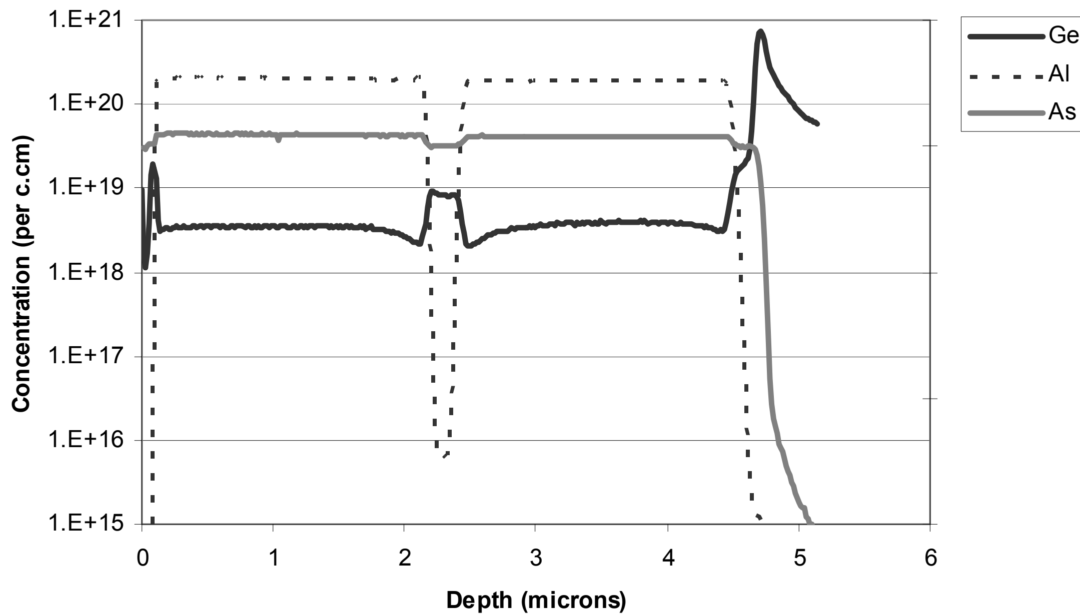

Figure 3.9: SIMS depth profile of InGaAs/GaAs/AlGaAs LED device structure on a Ge/GeSi/Si substrate. Note the high levels of Ge incorporation throughout all layers of the device. The dip in measured Al concentration in the center of the plot indicates the location of the GaAs device active region where growth was slowest. This is also where the Ge incorporation increases.

The direct effects of the Ge autodoping on device performance were observed when the fabricated LED structures on Ge/GeSi/Si were compared with identical Ge-free devices grown on GaAs substrates. Figure 3.10 shows a plot of injected current vs. measured luminescence intensity for the LED structures on both substrates. The slope of the current vs. optical power graphs can be used to calculate the differential quantum efficiency η_d of the LED structures according to the relationship:

$$\eta_d = \frac{q}{h\nu}\left[\frac{dP}{dI}\right]$$

Where q is the elemental electron charge, h is Planck's constant, ν is the frequency of the emitted light, and dP/dI is the measured slope. By this formula, the differential quantum efficiency of the LED structures on Ge/GeSi/Si substrates was 4×10^{-6}, while the same structure on a GaAs substrate had a measured η_d of 3×10^{-3}. The peak emission wavelength for all structures was measured to be about 915 nm. The diode voltage vs. injected current characteristics of the three devices was also measured, and these plots can be seen in Figure 3.11. The LED structure grown on a GaAs substrate showed the

expected rectifying characteristics, with a reverse leakage current of less than 0.01mA at a bias of –10V, and sharp turn-on behavior at +1V. In contrast to these results, the LED structures on Ge/GeSi/Si substrates showed strong deviations from ideality. The device on a Ge/GeSi/Si substrate showed rapid reverse breakdown at small negative voltages, with currents greater than 100mA at a bias voltage of –6 V. In forward bias, the Ge/GeSi/Si substrate device showed slow turn-on behavior and a very gradual rise in current with increasing positive voltage.

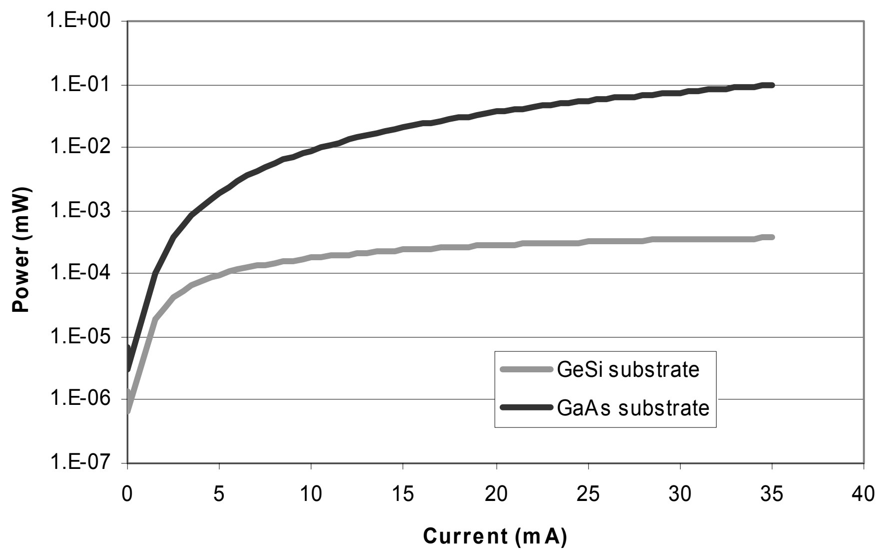

Figure 3.10: Diode current vs. measured optical power for LED structures on Ge/GeSi/Si and GaAs substrates. Note the much lower output power for the device on Ge/GeSi/Si.

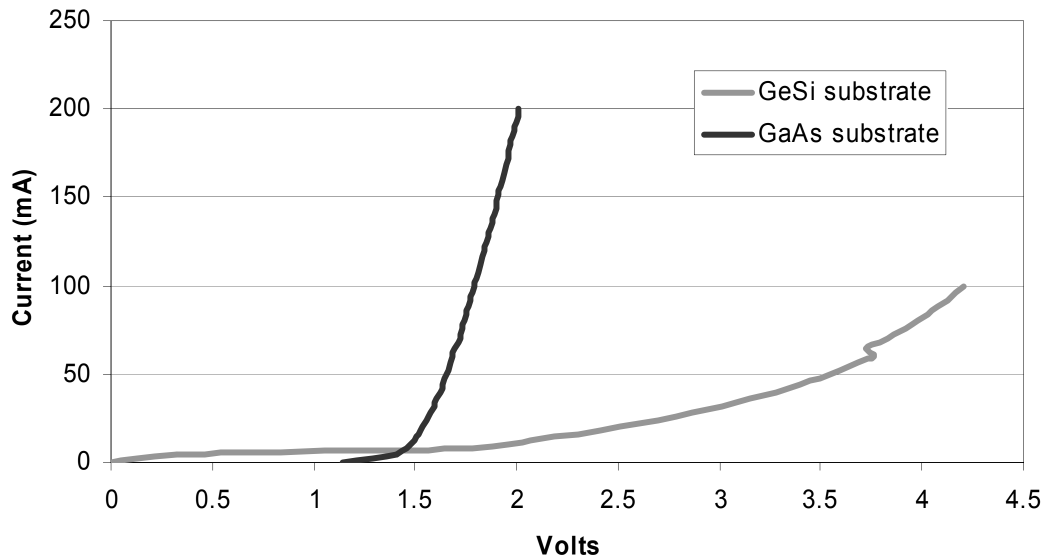

Figure 3.11: Voltage vs. current data for LED structures on Ge/GeSi/Si and GaAs substrates. The turn-on voltage and series resistance were much higher in the devices grown on Ge/GeSi/Si.

The behavior of the LED devices on Ge/GeSi/Si substrates confirms that Ge incorporation in these devices significantly impacts performance. For all of the LED structures, the deliberate p- and n-doping levels in the cladding layers were 5 x 10^{17} cm^{-3}. Ge contamination at concentrations greater than 10^{18} cm^{-3} throughout these layers would effectively swamp the deliberate doping levels, leaving the entire cladding and active-layer structure n-type. Only at the final p+ GaAs cap layer, where Zn-doping was increased to 1 x 10^{19} cm^{-3} to ensure good ohmic contact formation, would this deliberate doping be expected to balance the unintentional Ge autodoping to create a real *pn* junction. If the Ge autodoping does indeed shift the device junction up to the cladding/cap interface, very few injected holes from this junction will diffuse through the cladding layer to recombine radiatively with electrons in the InGaAs active region, while most will recombine non-radiatively in the indirect-bandgap cladding layer. Thus the compensated deliberate p-doping and shifted *pn* junction caused by Ge incorporation into all levels of the device will lead to the very poor differential quantum efficiencies we observed in the Ge/GeSi/Si substrate LEDs.

The electrical characteristics of these devices also confirm the effects of the unintentional Ge autodoping. The shifted asymmetric *pn* junction which results from Ge

incorporation in the device will produce a high series resistance, which is apparent in the much lower forward-bias slope of the voltage vs. current graph in Figure 3.11. Incorporated Ge will also contribute to reverse-bias generation current in the p-doped top AlGaAs cladding layer, explaining in part the large observed reverse bias currents. The top cladding layer, which is expected to be completely compensated by the unintentional Ge autodoping, can be expected to act more like the intrinsic region of a *pin* photodiode under negative bias conditions and thus allow large reverse currents with large reverse voltages.

From the results of the experiments discussed above, it is clear that integrated GaAs devices on Ge/GeSi/Si substrates will be impossible to achieve without finding a way to control the vapor-phase transport of Ge into the GaAs device layers during device growth. As Hudait observed, the obvious mechanisms for reducing vapor-phase transport of contaminants, namely by lowering the nucleation temperature or background pressure of reactive hydride gasses in the MOCVD chamber, are also those which most severely degrade the quality of the GaAs/Ge interface. The experimental results discussed in the previous section have proven that in our particular MOCVD growth system, high-quality GaAs nucleation on Ge/GeSi/Si offcut substrates cannot be achieved without nucleation temperatures of at least 700 °C and V/III gas flow ratios ~200. This indicates that another means of reducing the amount of Ge present in the reactor must be found to reduce autodoping behavior during GaAs growth on Ge/GeSi/Si. Our efforts to control Ge autodoping sources during MOCVD growth are described below.

3.6.2. Reducing Autodoping in GaAs/Ge Device Structures

Our experimental work to reduce the Ge autodoping of GaAs films in our MOCVD reactor focused on removing or passivating all possible Ge sources that were contributing to the background pressure of Ge in the reactor during growth. Previous work suggested that by undertaking steps to passivate possible Ge sources such as the backside of the wafer substrate, dramatic reductions in incorporated Ge in the GaAs epilayers could be achieved.[34,84]

For our initial passivation experiments, we investigated the ability of a low-temperature GaAs buffer layer to bury Ge contamination sources immediately after

nucleation. By nucleating a GaAs film on Ge/GeSi/Si at the standard high temperature/pressure conditions, but then lowering the temperature with all precursor gasses still flowing, it was hoped that slower Ge-desorption rates at low temperatures would enable Ge contaminants in the reactor environment to be buried under a passivating GaAs film. As with all samples, the growth was initiated at 700 °C with a V/III ratio of 225 following a 5-minute pre-growth anneal. The temperature was then reduced to 450 °C while continuing to flow all precursor gasses. After growing a 1 μm-thick buffer layer (measured growth rate = 3 μm/hr), the temperature was again raised to 700 °C, and an AlGaAs/GaAs test structure was grown, following the same recipe as the original LED structures described above, except without the InGaAs active region, to simplify compositional analysis. SIMS depth profiles of this sample are shown in Figure 3.12. It can be seen from the SIMS profile that the Ge concentration in the top layers of this passivated sample are indeed lower than in the original unpassivated GaAs films on Ge/GeSi/Si (Figure 3.9). Average Ge background levels fell to approximately 1×10^{17} cm^{-3} in the AlGaAs cladding layers, with slightly higher levels in the GaAs center region. Decreasing Ge incorporation in the GaAs is not the only effect of the low-temperature buffer; the SIMS data also shows a large increase in C contamination levels in the GaAs, particularly in the low-temperature buffer layer. This carbon contamination is most likely due to CH_3 from incompletely pyrolyzed TMG precursor gas, which is expected to have a cracking efficiency of approximately 80% at 450 °C.[58] Unfortunately C is an efficient p-type dopant in GaAs films, and this incorporated C contamination, with a measured maximum value of 1×10^{18} cm^{-3} in the low-temperature buffer layer would be expected to compensate deliberate n-doping in this lower layer and increase free-carrier absorption and reverse-bias leakage in diodes fabricated using this growth technique. Thus high temperature growth becomes necessary throughout the process of GaAs/Ge film growth, and the low-temperature buffer layer is not a practical means of passivating Ge/GeSi/Si substrates to avoid autodoping behavior in GaAs. For this reason we turned to alternative passivation strategies to remove possible Ge sources in the growth reactor before the high-temperature growth begins.

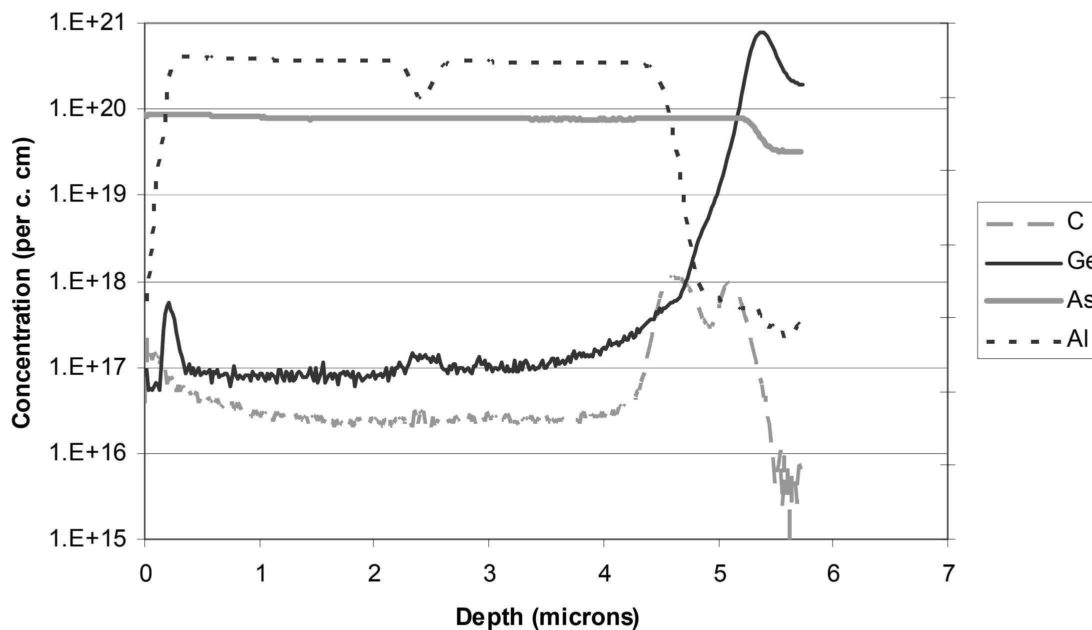

Figure 3.12: SIMS depth profile of GaAs/AlGaAs LED structure grown on a Ge/GeSi/Si substrate using a thick low-temperature GaAs buffer. Note the rapid increase in C contamination in the low-temperature buffer region.

As discussed above, possible sources for Ge contamination in the MOCVD growth chamber include the backside of the Ge/GeSi/Si substrate, the porous graphite susceptor on which the substrate rests during growth, and the walls of the growth chamber. Ge can be carried to the susceptor or reactor walls from the wafer during the high-temperature pre-growth anneal or from the back of the wafer during growth.[85] Our experiments focused on determining which of these possible sources play the strongest role in the observed Ge autodoping behavior, and to then find ways to control or reduce the effects of these sources. Three AlGaAs/GaAs LED test structures were grown on Ge/GeSi/Si substrates with different pre-growth steps to clean or passivate possible Ge contamination sources.

For the first growth, a standard high-temperature GaAs film was nucleated on the Ge/GeSi/Si substrate, followed by 500 nm of undoped GaAs at a temperature of 700 °C. Growth was halted, and the sample was allowed to cool under an AsH_3 overpressure. The sample was removed from the reactor chamber and set aside while the bare susceptor was reloaded into the reactor and heated up to 750 °C. The susceptor was then coated with approximately 1 μm of AlAs by flowing TMAl and AsH_3 for 15 minutes, which was

expected to cover any deposited Ge layers on the susceptor surface or the reactor walls. A switch from TMAl to TMG for the last 1 minute left a GaAs surface that would not oxidize upon removal from the reactor. The reactor was cooled down again under an AsH_3 overpressure. Meanwhile, the GaAs film on the Ge/GeSi/Si substrate was cleaned with a standard GaAs surface etch[47] of H_2O_2:H_2O:H_2SO_4 at a ratio of 1:1:25 for 10 seconds followed by a 2 minute deionized water rinse and blow dry. This etch was expected to remove 100-200 nm of Ge-contaminated GaAs and leave the surface smooth for further GaAs growth. The cleaned sample was then reinserted into the coated reactor chamber and the reactor was heated up to 700 °C under AsH_3 overpressure for a repeat of the AlGaAs/GaAs LED test structure growth described earlier. A SIMS depth profile of this sample is shown in Figure 3.13.

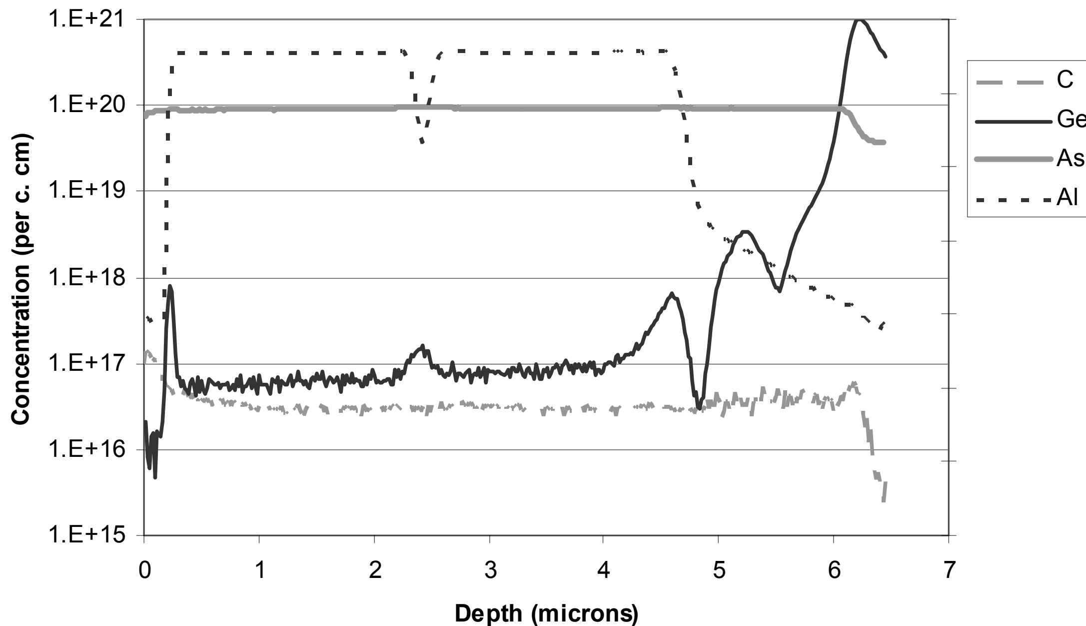

Figure 3.13: SIMS depth profile of GaAs/AlGaAs LED structure grown on a Ge/GeSi/Si substrate after a 15-minute AlAs coating of the susceptor and reactor walls. The overall Ge incorporation is lower, but a Ge spike remains in the central GaAs layer.

It can be seen from the SIMS profile that the use of an intermediate susceptor coating step reduced the overall Ge autodoping contamination level to 4 x 10^{17} cm^{-3} in the AlGaAs cladding regions. A peak at 1 x 10^{18} cm^{-3} was still present in the GaAs waveguide core at the center of the film, but the C contamination level remained flat

throughout the structure. The reduction in overall Ge contamination is nearly an order of magnitude over the original LED structures grown without susceptor coating, but the background level remained too high for practical device integration, and indicated that additional Ge sources remained in the reactor.

For our second experiment, a standard high-temperature GaAs film was nucleated on a Ge/GeSi/Si substrate followed by a 500 nm undoped GaAs buffer, as in the first growth. The sample was cooled down and removed from the reactor and the susceptor was again coated with a 15 minute AlAs growth. Unlike the first experiment, the Ge/GeSi/Si substrate with its epitaxial coating of GaAs was then mounted with heat-sensitive wax epi-side down on a hand-polishing chuck and mechanically polished to remove the backside Ge/GeSi layers. As discussed above, the UHVCVD growth of the Ge/GeSi buffer layers on a Si substrate deposits equal amounts of material on both sides of the Si wafer, and by mechanically removing the 10 μm-thick polycrystalline Ge/GeSi film on the back of the substrate we hoped to remove one more potential source for Ge vapor-phase transport in the MOCVD reactor. After mechanical polishing, the sample was heated then cleaned in acetone, methanol, and water to remove any remaining wax and then cleaned with the wet surface etch described above to prepare the GaAs surface layer for further growth. The sample was reinserted into the reactor and heated up to 700 °C under AsH_3 overpressure for a repeat of the AlGaAs/GaAs LED structure growth already described. A SIMS depth profile of this sample is shown in Figure 3.14.

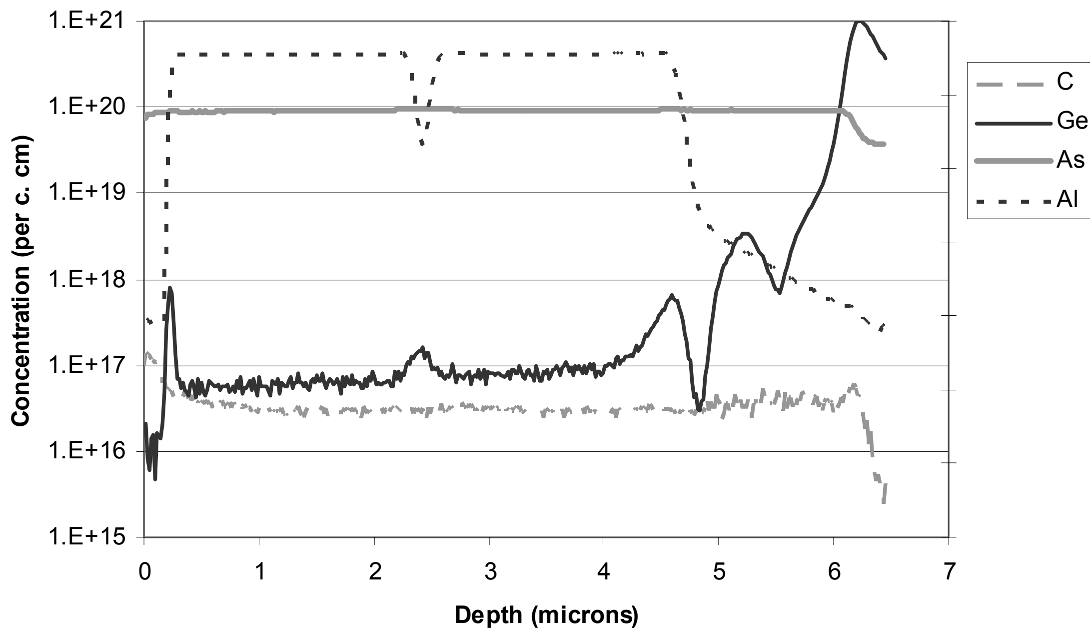

Figure 3.14: SIMS depth profile of a GaAs/AlGaAs LED structure on a Ge/GeSi/Si substrate grown after coating the susceptor and reactor walls and removing the Ge/GeSi back layers of the substrate wafer.

It can be seen from the SIMS profile that removing the backside Ge/GeSi layer from the Ge/GeSi/Si substrate further reduced the Ge incorporation in the GaAs/AlGaAs device structure. The background Ge contamination level in the AlGaAs cladding layers was lowered to about 9×10^{16} cm^{-3}, which was an additional 5X reduction from the previous sample grown with only a susceptor coating step. Carbon contamination remained low in all parts of the structure, and the Ge contamination in the GaAs center core layer, while slightly higher than the background level at 2×10^{17} cm^{-3}, was for the first time lower than the intentional Si- and Zn-doping levels of 5×10^{17} cm^{-3} necessary for useful device integration. As suggested by Tobin[84] it was thus clear that Ge on the back of the Ge/GeSi/Si substrate is a significant source for Ge transport in our MOCVD reactor.

A third experiment to create the cleanest possible environment for GaAs device growth on Ge/GeSi/Si in our MOCVD reactor chamber investigated the effects of cleaning the reactor walls and the susceptor on reducing incorporated Ge contamination levels. For this experiment, we followed the same procedures described earlier, depositing a 500 nm GaAs cap layer on Ge/GeSi/Si at high temperature, removing the

sample from the reactor and mechanically polishing the backside to remove all Ge/GeSi layers, and recleaning the sample to prepare it for GaAs epitaxy. However instead of coating the graphite susceptor and reactor walls with a AlAs passivating layer, we removed the quartz reactor tube and the graphite susceptor from the reactor and replaced them with a cleaned reactor tube and a new (unused) graphite susceptor. After leak-testing the reactor chamber, and baking the new susceptor in the chamber for 15 minutes at a temperature of 850 °C to drive out any water contamination, we reinserted the sample in the clean reactor chamber and grew an AlGaAs/GaAs LED structure as before. A SIMS depth profile of this sample is shown in Figure 3.15.

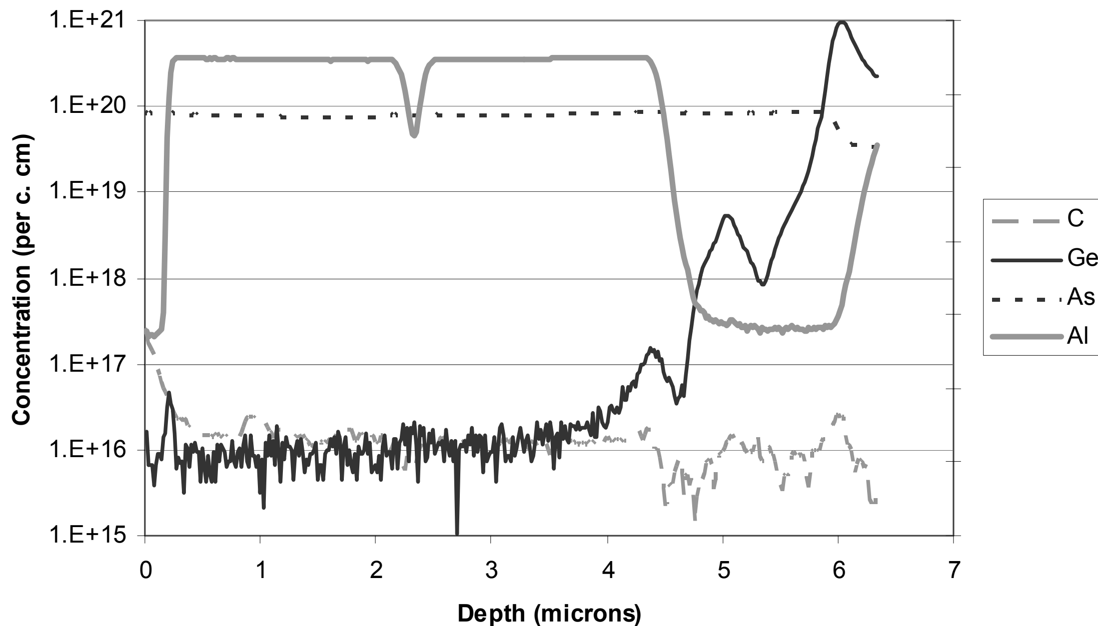

Figure 3.15: SIMS depth profile of a GaAs/AlGaAs LED structure on a Ge/GeSi/Si substrate grown on a new graphite susceptor in a cleaned reactor tube after mechanically removing the Ge/GeSi back layers. Note the very low Ge and C contamination levels, and the absence of any Ge peak in the GaAs waveguide core in the center of the device.

The SIMS profile of this sample shows the lowest Ge incorporation levels ever measured in our GaAs device layers on Ge/GeSi/Si substrates. The background Ge levels in the AlGaAs cladding layers were below the detectable limits of 1×10^{16} cm^{-3}, and no evidence of a Ge increase in the slow-growth rate GaAs center core region of the device was visible. Carbon contamination was also below detectable limits. From this data we concluded that all Ge sources in the MOCVD growth chamber had been removed by the

cleaning of the reactor chamber and graphite susceptor, in conjunction with backside polishing and regrowth on a previously nucleated and cleaned GaAs buffer layer. The previous experiments that used a 15-minute AlAs coating step to passivate the graphite susceptor and reactor walls were apparently unsuccessful in completely covering the desorbed Ge on these surfaces. It is clear that Ge is a very mobile species in the MOCVD reactor atmosphere, and all surface sources must be completely eliminated to allow Ge-free GaAs nucleation on our Ge/GeSi/Si substrates.

3.6.3. Characterizing Autodoping-free GaAs/Ge Device Structures

With undetectable Ge autodoping levels in the GaAs/AlGaAs device layers, it should be possible to successfully integrate practical AlGaAs/GaAs device structures on Ge/GeSi/Si substrates. To test this assertion, we fabricated LED test structures with our optimized GaAs/Ge nucleation procedure on Ge/GeSi/Si substrates and compared their optical and electrical characteristics to similar devices grown on commercial GaAs substrates in cleaned reactor tubes. The device structures began with 500 nm of GaAs buffer layer (n-doped on the GaAs substrate but undoped on the Ge/GeSi/Si in expectation of surface Ge autodoping in this buffer layer), followed by sample removal and reactor and sample cleaning as detailed above. The samples were then reinserted into the reactor and growth continued with symmetric n- and p-type 1.1 μm thick $Al_{0.6}Ga_{0.4}As$ cladding layers surrounding a 10 nm-thick undoped GaAs active region. The device structure was capped with a 50 nm highly p-doped GaAs cap layer for ohmic contact formation. An oxide mask followed by Ti/Au metal stripe evaporation defined the top contacts for these diodes, and evaporated Al on the Ge/GeSi/Si substrates or Ni/AuGe on the GaAs substrates formed the backside contacts. The devices were annealed for 20 seconds at 425 °C to alloy the metal layers, then cleaved into bars and tested. A plot of the current vs. optical power and diode voltage vs. current data for these devices is shown in Figure 3.16.

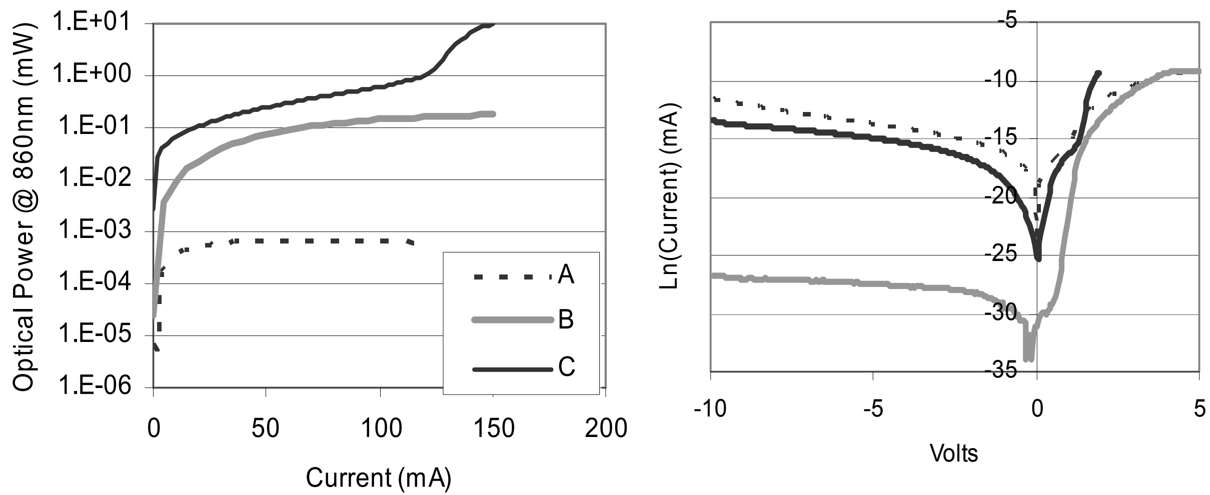

Figure 3.16: Current vs. optical power and diode voltage vs. current data for improved Ge-free GaAs/AlGaAs LEDs on Ge/GeSi/Si substrates (B) compared with identical devices fabricated on GaAs substrates (C). The original current vs. power and voltage data for the Ge-contaminated LED is also plotted for comparison (A).

It can be seen from the diode current vs. optical power measurements that the LEDs on Ge/GeSi/Si substrates showed performance almost equivalent to the devices on GaAs. The measured differential quantum efficiencies for these optimized devices were 1.2×10^{-3} on the Ge/GeSi/Si substrates compared with 4.7×10^{-3} on GaAs substrates. This is an improvement of nearly three orders of magnitude for the devices on Ge/GeSi/Si, confirming again the dramatic effect that unintentional Ge autodoping had on the original integrated LED devices. A similar improvement can be seen in the voltage vs. current curves for these new devices. The turn-on voltages and reverse-bias leakage currents are essentially identical for devices grown on GaAs and Ge/GeSi/Si substrates, and the device on Ge/GeSi/Si shows a very small decrease in slope at high voltages, indicating a slightly increased series resistance for these LEDs. It is possible to characterize the ideality of a semiconductor *pn* diode by measuring the behavior of the voltage vs. current graph above turn-on. The ideal diode equation predicts a forward bias current I defined by: [87]

$$I = I_0 \exp(\frac{qV}{nk_B T})$$

Where I_0 is the reverse leakage current, q is the fundamental electron charge, V is the applied voltage, k_B is the Boltzmann constant, T is the temperature, and n is the ideality factor. For an ideal diode, n should be close to 2 for high-level injection. If all other factors are assumed to be constants, the ideality of an actual device can be measured by plotting the natural log of the measured diode current as a function of voltage. The slope of this graph just above turn-on can then be used to estimate n according to the relationship:

$$\ln(I) = \frac{q}{nk_BT}V + \ln(I_0)$$

The calculated ideality for our control LEDs on GaAs substrates was 2.6. Identical devices on Ge/GeSi/Si substrates had an ideality $n = 2.1$. For comparison, the same structures on Ge/GeSi/Si substrates before the reduction of the Ge autodoping levels had an ideality factor of 4.9. This measurement confirms the optical data discussed above by showing that a reduction in the background Ge contamination of our integrated AlGaAs/GaAs devices on Ge/GeSi/Si substrates had a measurable effect on the performance of these devices and enabled them for the first time to approach the performance of identical devices grown on GaAs substrates.

3.7. Conclusions

From the experimental evidence presented in this chapter, it is clear that the nucleation of the initial GaAs monolayers on a Ge/GeSi/Si substrate will control the quality of the subsequent heteroepitaxial growth. During the initial nucleation step, efforts must be taken to minimize the formation of planar defects such as anti-phase boundaries and stacking fault pyramids. Attention must also be paid to the presence of undesired Ge sources in the reactor growth chamber, which have been shown to contribute directly to Ge autodoping behavior in GaAs devices and thereby degrade device performance. By investigating low-temperature GaAs nucleation on Ge/GeSi/Si substrates, we have shown that the generation of stacking fault pyramids in the initial GaAs film layers is unavoidable, and therefore prohibits useful device integration via low-temperature initiation layers. Our investigations of high-temperature nucleation on

Ge/GeSi/Si substrates have confirmed the assertions of previous authors that high temperatures, high V/III gas flow ratios, and offcut substrates are necessary for defect-free initiation layers on Ge. For our atmospheric MOCVD growth reactor we have extended the work of Ting to show that the ideal nucleation conditions for a GaAs film on a Ge/GeSi/Si substrate are a growth temperature of 700 °C, a V/III gas flow ratio of 225, and a 5-minute pre-growth anneal at a temperature of at least 650 °C. Our investigations of atomic intermixing between GaAs films and the Ge/GeSi/Si substrate material have shown the significant negative effects that unintentional Ge autodoping can have on GaAs device layers. We have confirmed that this Ge autodoping occurs via vapor-phase transport in the MOCVD growth chamber, and we have proven that the reactor walls, the wafer backside, and the graphite susceptor all act as Ge sources during the MOCVD growth process. By removing or passivating each of these sources, we have shown the ability to control Ge incorporation in GaAs films grown on Ge/GeSi/Si substrates, and thereby to rectify the dramatic decreases in LED device performance that this incorporation can cause. By controlling the GaAs/Ge interface through an optimized nucleation recipe, we have demonstrated AlGaAs/GaAs devices on Ge/GeSi/Si performance with nearly identical performance to matching devices fabricated on commercial GaAs substrates. This accomplishment is a significant one, and a large step toward the final goal of successful GaAs laser integration on Ge/GeSi/Si substrates.

Chapter 4. Optimizing Thermal Expansion Mismatch for Laser Integration

4.1. Introduction

This chapter investigates the details of thermal expansion mismatch in the GaAs/Ge/Si system and our work toward solutions enabling successful strained quantum well diode integration in highly mismatched materials systems.

The growth and optimization of Ge on relaxed graded $Si_xGe_{(1-x)}$ buffer layers on Si substrates was discussed earlier in Chapter 1, and by Currie,[27,53] who explained the details of the SiGe buffer and Ge cap growth process for all of the substrates used in this experiment. Surface microcracks induced by the large thermal expansion mismatch between the $Si_xGe_{(1-x)}$/Ge epilayers and the Si substrate below were eliminated with two growth modifications. First, the final grading layers from $Si_{0.25}Ge_{0.75}$ to 100% Ge were grown at a lower temperature (550 °C), and second, a deliberate composition jump was introduced at the final step from $Si_{0.08}Ge_{0.92}$ to 100% Ge. This compositional step introduces an intentional compressive strain in the Ge cap layer at the growth temperature that balances the tensile strain introduced upon cooling, while the lowered growth temperature prevents the strain in the cap layer from relaxing before it can be balanced by thermal mismatch strain. X-ray diffraction (XRD) of these 100% Ge graded buffer structures revealed no remaining tensile strain when the wafers were cooled to room temperature.

While the growth modifications described above have removed thermally induced tensile cracking during graded buffer growth, the deliberate compressive strain introduced by these modifications has negative effects on III-V strained-layer optoelectronic devices grown above these buffer layers. In particular, compressively strained quantum well diodes, which are the most resistant to threading dislocation-induced failure during operation (an important requirement for successful III-V on Si integration) will be more difficult to integrate on substrates that already contain a substantial amount of compressive strain at the growth temperature.

Work by Yellen[18] and Wang[88] has shown that $In_xGa_{(1-x)}As$ compressively strained quantum well devices are the most resistant of any III-V heterostructure device to failures due to <100> dark-line defects. As discussed in Chapter 1, dark-line defects (DLDs) are dense dislocation networks that form suddenly in the active regions of operating laser

diodes and lead to rapid increases in operating current and subsequent laser failure. These <100> DLD networks form when threading dislocations climb into laser active regions from other layers of the structure.[89] Given the fixed threading dislocation density (~10^6 cm^{-2}) present in all graded Si/SiGe/Ge substrates used for our integration studies, the proven resistance of $In_xGa_{(1-x)}As$ strained quantum well structures to the most common threading-induced failure mechanisms for operating GaAs-based lasers make these structures the best choice for optoelectronic integration on Si.

Compressively strained $In_xGa_{(1-x)}As$ quantum well lasers grown on Ge substrates have been demonstrated by D'Hondt,[90] but similar structures have not been successfully demonstrated on relaxed graded Si/SiGe/Ge substrates. As discussed above, the relaxed graded substrate structure has been optimized to include a deliberate compressively strained Ge cap layer to avoid the high crack densities caused by unequal contraction of Ge and Si upon cooling. While this deliberate compressive cap layer leads to nearly cubic room-temperature Ge, it also means that any additional III-V device layers grown above this substrate will contain this compressive strain at the growth temperature. Growth on a compressively strained Ge film would be expected to decrease the equilibrium critical thickness for strain relaxation in an $In_xGa_{(1-x)}As$ quantum well.

There are two approaches to avoid growing a super-critical strained quantum well on a compressively strained substrate. The quantum well may be thinned or the indium composition may be reduced to bring it below its critical thickness on the strained substrate. This approach will limit the accessible emission wavelengths and reduce electrical and optical confinement in the quantum well structure. A second, more flexible approach would be to relax the trapped compressive strain from the substrate during the epitaxial III-V growth process before this strain is able to relax in the quantum well active layer. In implementing this second approach care must be taken to avoid returning to the original problem of tensile thermal strain leading to microcrack formation.

4.2. Background: Thermal Expansion Mismatch

When a cubic semiconductor lattice is heated, it expands triaxially according to its coefficient of thermal expansion $\alpha(T)$. In general, this thermal expansion coefficient is a

function of temperature, but for small ΔT it can be assumed to be a constant. The thermal expansion coefficients of bulk GaAs, Ge and Si have been published by a number of authors.[91,93] When a thin heteroepitaxial film is deposited on a semiconductor substrate with a different thermal expansion coefficient, the thick substrate will dominate the thermal expansion behavior of the thin coherent film above it. As the deposited film is cooled from its growth temperature, it will therefore incorporate an additional biaxial strain due to the differing thermal expansion coefficients. Assuming no additional sources of plastic relaxation during cool-down, the total developed strain in such a system due to this thermal expansion mismatch could be estimated with the expression:

$$\varepsilon = \Delta\alpha\Delta T$$

To first order, the growth of a thin Ge (α = 5.8 x10^{-6} K^{-1}) film on a Si (α = 2.6x10^{-6} K^{-1}) substrate could be expected to introduce a tensile thermal expansion strain of approximately 0.18% assuming a Ge/GeSi growth temperature of 550° C. A GaAs (α = 6.8 x10^{-6} K^{-1}) film grown on Si at 700 °C would generate a thermal mismatch strain of approximately 0.26%. These strain estimations are close to those calculated more rigorously by Roos and Ernst[94] using complete expressions for thermal expansion coefficients as a function of temperature, and are therefore useful for understanding the order of magnitude of the strain expected to be introduced by thermal expansion mismatch.

The theoretical thermal strain calculated in this manner can be interpreted as the maximum elastic strain introduced to a heteroepitaxial system cooled from the growth temperature. As the deposited film is cooled from the growth temperature, it is important to confirm what if any relaxation mechanisms would operate to reduce this strain. A number of authors have investigated this question using materials systems with many parallels to this work.

Roos and Ernst[94] investigated the strain behavior of $Ge_{0.9}Si_{0.1}$layers grown on <111> Si substrates using liquid-phase epitaxy (LPE) at 820 °C. Their observations indicate that Ge-rich epilayers on Si relax a small amount of thermal mismatch strain when cooling above the brittle-ductile transition temperatures of bulk Si and Ge (~ 500 °C) but trap the remaining tensile strain when cooling below this temperature.

Lucas[95] investigated the behavior of thick (~ 2.5μm) GaAs layers grown on <100> Si with MBE at 600 °C. Samples were heated to temperatures from 30 to 430 °C while measuring the substrate and epilayer lattice constants with an *in situ* X-ray diffraction spectrometer. Lucas showed that the GaAs epilayers are forced by the underlying Si substrate to expand with linear thermal expansion coefficients matching those of the Si substrate below them. Measurements of the GaAs and Si lattice constants in both the parallel and perpendicular directions showed that GaAs epilayers distort tetragonally under the biaxial thermal mismatch strain and that the thermal expansion coefficient of GaAs in the direction perpendicular to the growth plane is larger than its bulk value by almost the same amount as the parallel thermal expansion coefficient is reduced. Thus the additional strain added by thermal expansion mismatch is not relieved by further dislocation nucleation or plastic deformation.

Lum[22] used atmospheric-pressure organometallic chemical vapor deposition (OMCVD) to grow thick (1 to 5μm) GaAs films on both oncut and 2° offcut <100> Si substrates at growth temperatures of 700 °C. The biaxial room-temperature tensile strain measured in these samples using XRD and wafer curvature measurements indicated that while a small amount of the thermal mismatch strain had been relaxed (or compensated by residual compressive strain due to the Si/GaAs misfit), more than 90% of the theoretical thermal expansion mismatch strain remained in the epilayer at room temperature.

In reviewing the previous work, it can be observed that while a small degree of additional plastic relaxation can be expected during cooling, a majority of the tensile stress induced by the mismatch between Si and Ge and GaAs thermal expansion coefficients will be trapped as strain in an epilayer film upon cooling. Conversely, compressive material mismatch strain that has been compensated by thermal expansion differences at room temperature can be expected to reappear if the sample is again heated to the growth temperature. It is the behavior on heating which motivates the strain relaxation work discussed in this chapter.

4.2.1. Theory of Critical Thickness

Before considering how the addition of thermal mismatch strain might modify the critical thickness of a heteroepitaxial strained quantum well, it is useful to briefly review the methods for calculating thermodynamic critical thickness in strained epilayers. The critical thickness of a strained layer is defined as the thickness at which dislocation line formation energy and dislocation strain energy in a film are equal. Many authors have investigated both thermodynamic and kinetic models for predicting the critical thickness at which a strained film begins to relax. For the InGaAs/GaAs system considered in this work, Fitzgerald[8] has shown how Matthews' energy balance[9] can be applied to anisotropic lattices with both 60° and 90° dislocation Burgers vectors to find the thermodynamic (equilibrium) critical thickness, h_c:

$$h_{c90} = \frac{D(1-\nu\cos^2\theta)[\ln(\frac{h_{c90}}{b})+1]}{2Yf}$$

$$h_{c60} = \frac{D(1-\nu\cos^2\theta)[\ln(\frac{h_{c60}}{b})+1]}{Yf}$$

Where following Fitzgerald,[8] D is the reduced shear modulus for InGaAs, Y is the modulus for [110] biaxial strain, b is the Burgers vector in InGaAs, and f is the mismatch. For an $In_xGa_{(1-x)}As$ film on bulk GaAs (a = 5.65315 Å) with x_{In} = 0.2, the calculated critical thickness for 60° dislocations at room temperature is 87Å. The critical thickness for 90° pure edge dislocations is slightly smaller, however in low-mismatch systems 60° dislocations will dominate the relaxation behavior due to their ability to glide along the primary {111}<110> slip system in cubic crystals.

The actual critical thickness for $In_{0.2}Ga_{0.8}As$ quantum well lasers on bulk GaAs has been measured experimentally at room temperature with EBIC and other methods to be approximately 120 Å.[96] The discrepancy between this actual value and the calculated equilibrium value is due to the kinetic barriers that impede dislocation nucleation and propagation and yield metastable super-critical films in most strained semiconductor materials. The equilibrium critical thickness remains useful as a firm lower bound on achievable strained layers. Films grown below the critical thickness will not relax

regardless of post-growth thermal annealing steps the device must undergo during processing.

4.2.2. Effect of Thermal Expansion Mismatch on Critical Thickness

It is possible to use the equilibrium critical thickness equation to understand how h_c will be modified by additional strain introduced by thermal expansion mismatch in the substrate material. Ignoring thermal expansion for a moment, and using the measured room-temperature substrate lattice parameter of the Ge cap layer of a relaxed graded Ge/GeSi structure (lattice parameters were measured using triple-axis X-ray diffraction as discussed by Currie[27]) the equilibrium critical thickness h_{c60} for an $In_{0.2}Ga_{0.8}As$ quantum well is 86 Å. This calculated value reflects the very close lattice match between GaAs (on which h_{c60} = 87 Å) and the nearly cubic room-temperature Ge cap layers produced by the relaxed graded buffer growth process.

While this calculation implies little strain difference between growth on GaAs and on Ge/GeSi/Si, it does not include the effects of thermal expansion. As the Ge/GeSi/Si substrate is raised to the growth temperature for GaAs/InGaAs deposition, the compressive strain balanced by the differing thermal expansion coefficients of the Si substrate and the Ge cap layer will return to the cap. One way to estimate the effects of this additional substrate strain on the critical thickness of an $In_xGa_{(1-x)}As$ film grown atop it is to modify the expression for mismatch (f) used in the critical thickness calculations detailed above. Assuming that the thermal expansion mismatch strain upon cooldown of the Ge/GeSi/Si substrate does not relax, this strain will be added back completely into the substrate as it is heated once again for III-V growth. The effective mismatch felt by the GaAs and InGaAs overlayers at the growth temperature will be,

$$f_{eff} = f + \varepsilon_{thermal} = f + \Delta\alpha\Delta T$$

Inserting this f_{eff} into the critical thickness calculations for an $In_{0.2}Ga_{0.8}As$ film grown on a Ge/GeSi/Si substrate with a thermal expansion mismatch strain $\varepsilon_{thermal}$ of 0.26% yields an equilibrium h_{c60} of 68 Å. This value is more than 20% thinner than the equilibrium value calculated for growth on bulk GaAs substrates, and shows the dramatic effect that thermal expansion mismatch will have on strained quantum wells.

With the issues introduced by thermal expansion mismatch understood, solutions to the unwanted strain contributions can be considered. Possible process modifications fall into two categories: modification of the substrate and modification of the III-V overlayers. Any action in the first category, namely modification of the Ge/GeSi/Si substrate, is necessarily constrained by the significant defect engineering that has already taken place with this substrate material (see Chapter 1). The growth recipe for the SiGe buffer layer is dominated by the need for slow grading rates at high growth temperatures for complete strain relaxation, and these layers cannot therefore be significantly thinned or cooled.

Consequently, the investigations presented in this chapter have focused exclusively on finding solutions within the III-V growth process. In particular we have explored the effects of intentional strain relaxation in the GaAs buffer layers below the central $In_xGa_{(1-x)}As$ quantum well layers. A straightforward way to introduce relaxation is to add additional compressive strain during the III-V growth process and reduce the effective critical film thickness. In the GaAs materials system additional lattice compression is achieved by adding small quantities of In. With our substrates, the built-in compression of the Ge/SiGe/Si substrate means that only a small amounts of additional indium should be needed to tip the energy balance towards relaxation in the initial GaAs buffer layers on Ge/GeSi/Si. In theory, a thin relaxed $In_xAl_yGa_{(1-x-y)}As$ buffer layer grown between the Ge/GeSi/Si substrate and the main device structure could return the device to a familiar phase space for strained quantum well diode design. By using InAlGaAs instead of InGaAs for this layer, the low index and high bandgap needed for optical and electrical confinement in the cladding region will be preserved. InAlGaAs lasers may also show increased operational lifetimes by inhibiting defect motion in the In-containing layers.

The addition of In to the lower layers of a GaAs/InGaAs quantum well device structure will introduce additional materials engineering issues that must be considered. One such issue is the possible nucleation of additional threading dislocation segments within InAlGaAs buffer layers. As discussed in the introduction, the Ge/SiGe/Si substrates used in this work have been optimized to achieve record low threading densities of less than 10^6 cm^{-2}, giving an average dislocation spacing below the typical

minority carrier diffusion length in GaAs-based devices.[54] The nucleation of new threading dislocations inside InAlGaAs buffer layers would remove all the advantages achieved by these revolutionary substrates and prohibit successful minority-carrier device (i.e. laser) operation. An optimized In concentration in our InAlGaAs buffer layers will avoid unwanted relaxation and subsequent dislocation nucleation, while providing enough compressive strain to relax the buffer layer to near-equilibrium GaAs lattice constants at the growth temperature.

The goal of the work presented below was to confirm the predicted effects of deliberate Ge compression on subsequent InGaAs/GaAs strained epitaxy, and to investigate possible strain-engineering solutions to enable misfit-free strained quantum well integration on Ge/GeSi/Si substrates.

4.3. Thermal Mismatch Experiments

As described in Chapter 2, all OMCVD growths were performed on a Thomas Swan horizontal research reactor operating at atmospheric pressure. Growth temperature for all films was 700 °C. Substrates used for all growths were cleaved pieces of the same Si/SiGe/Ge wafer.

Growth initiation was the same for all samples, beginning with a 5 minute anneal of the Si/SiGe/Ge substrate at 700 °C under H_2, after which the AsH_3 and TMG flows were turned on and a thin (1000Å) GaAs buffer layer was grown on the surface. Above this buffer layer 3500Å of $In_xAl_{0.55}Ga_{(0.45-x)}As$ was grown followed by a 1 μm thick Si-doped GaAs cap. The n-doping was included to permit later characterization with etch pit density (EPD) measurements.

To confirm the different relaxation behavior on GaAs and Si/SiGe/Ge substrates, three simple $In_{0.2}Ga_{0.8}As$ quantum well structures with different thicknesses (50Å, 75Å and 100Å) were grown on thick (5000Å) GaAs buffers on each substrate. Quantum well thicknesses were confirmed using cross-sectional TEM and the presence or absence of misfit dislocations in the quantum wells was observed using both plan-view and cross-sectional TEM.

To measure the effects of deliberate strain relaxation below the quantum well, seven samples were grown with varying In concentrations in their buffer layers. Strain and lattice constant measurements were made using a triple-axis high-resolution X-ray diffractometer. Lattice constants both perpendicular ($a_\perp$) and parallel ($a_{||}$) to the film growth direction were measured independently with (004) rocking curves and (224) glancing-exit reciprocal-space maps. Measured displacements of the film and substrate diffraction peaks were used to calculate all necessary lattice parameters and strain values according to the methods of van der Sluis.[69] Indium compositions were confirmed independently using thick (1.5 μm) $In_xGa_{(1-x)}As$ calibration samples grown directly on oncut GaAs wafers with identical growth settings. Threading dislocation density in the GaAs cap layers was measured using defect selective etching.

After the initial samples were grown, three additional structures in which the uniform 3500Å InAlGaAs buffer layer was replaced with an $In_xGa_{(1-x)}As$ graded buffer were also grown. The motivation behind these growths and their results will be discussed below. A cross-sectional schematic of the different buffer structures grown for this experiment is shown in Figure 4.1.

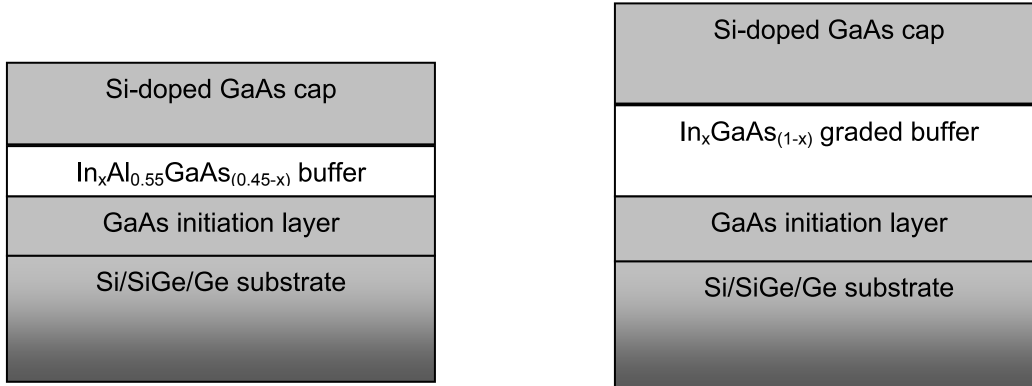

Figure 4.1: Schematic of the InAlGaAs and InGaAs buffer layers grown on Ge/GeSi/Si substrates. Both samples were n-doped with Si to increase the selectivity of the defect selective etching reaction.

4.3.1. Reduced Critical Thickness on Ge/GeSi/Si Substrates

The quantum well structures grown on GaAs and Si/SiGe/Ge substrates showed different relaxation behavior depending on the substrate on which they were deposited. For the 50Å $In_{0.2}Ga_{0.8}As$ quantum well grown on GaAs and on Si/SiGe/Ge, no misfit dislocations were observed in the wells of either sample, as would be expected from the

critical thickness calculations detailed previously. For both the 75Å and 100Å quantum wells, numerous misfit dislocations were observed in the quantum wells grown on Si/SiGe/Ge, whereas no misfit dislocations were found in the same structures grown on GaAs. Plan-view TEM micrographs of the 100Å samples are shown in Figure 4.2. These results confirm the theoretical critical thickness predictions discussed above, and show empirically that the critical thickness for compressively strained quantum wells on Si/SiGe/Ge relaxed graded substrates is significantly reduced by the thermal mismatch strain present in these structures at the growth temperature.

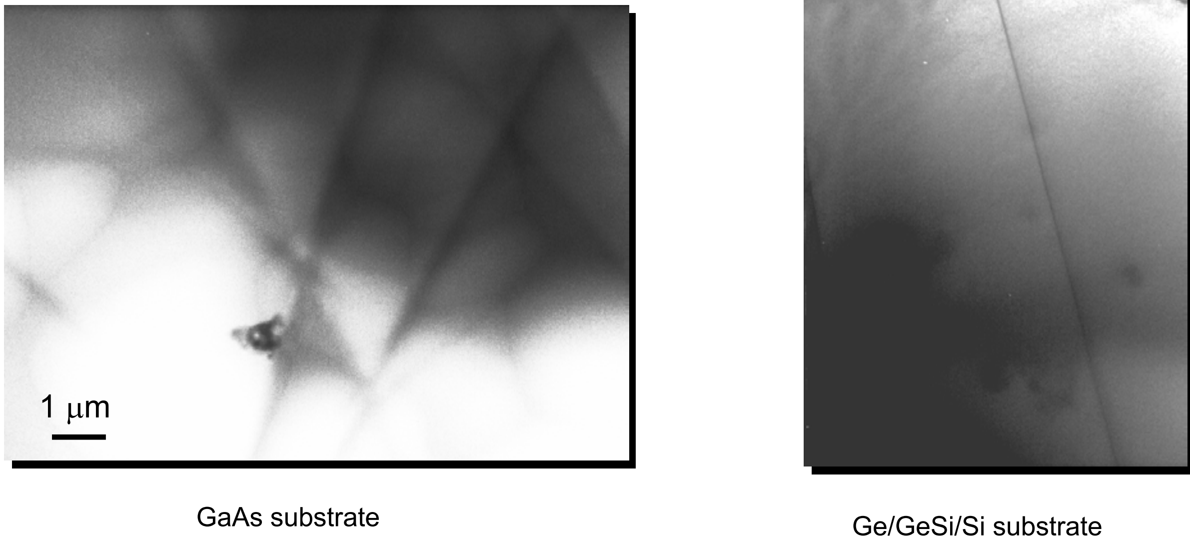

Figure 4.2: Plan view TEM micrographs of 100 Å InGaAs quantum wells grown on GaAs and Ge/GeSi/Si substrates. Note the presence of orthogonal misfit dislocation lines on the Ge/GeSi/Si substrate that are not present on the GaAs substrate

One significant difference between the Ge/GeSi/Si and GaAs substrates is the increased threading dislocation density in the Ge/GeSi/Si. Dodson and Tsao have argued that the initial relaxation of super-critical strained semiconductor films depends strongly on the substrate threading density.[10] The Ge/GeSi/Si substrates used in this work had threading dislocation densities at least 1000 times higher than the GaAs substrates used as controls. Work by Klem, *et al* investigated the effects of substrate threading dislocations on strained $In_{0.26}Ga_{0.74}As$ quantum wells on GaAs.[97] Their investigations

showed that while threading dislocation density increases misfit relaxation in wells grown above the thermodynamic critical thickness, it has no measurable effect for wells grown at or close to the critical thickness. It is therefore possible that some of the misfit relaxation seen in our thickest 100 Å quantum wells on Ge/GeSi/Si substrates is motivated in part by the higher density of misfit nucleation sources present in these substrates. However, these threading dislocation nucleation sites cannot be responsible for the misfit dislocations observed in thinner 75Å and 60Å $In_{0.2}Ga_{0.8}As$ quantum wells. Since these InGaAs quantum wells grown on our Ge/GeSi/Si substrates were below the equilibrium critical thickness for the substrates on which they were grown (calculated h_c = 86 Å), the increased threading dislocation density in the Ge/GeSi/Si substrates did not play a significant role in the increased misfit relaxation of InGaAs quantum wells grown on these substrates. Instead, as discussed above, the additional compressive strain introduced by thermal expansion mismatch was responsible for reducing the InGaAs quantum well critical thickness in all of the wells grown on these substrates.

4.3.2. Uniform $In_xAl_{0.55}Ga_{(0.45-x)}As$ Buffer Layer Experiments

Measured room-temperature in-plane lattice constants ($a_{||}$) of GaAs cap layers as a function of indium composition for seven $In_xAl_{0.55}Ga_{(0.45-x)}As$ buffer layer samples are shown in Figure 4.3. The bulk GaAs lattice constant at room temperature and at the growth temperature (700 °C) are plotted for reference. At each measured lattice constant value, an estimate of the lattice constant at the growth temperature is plotted as an error bar above the data point. These estimates were made using the linear thermal expansion coefficient of the Si substrate wafer ($\alpha = 2.6 \times 10^{-6}$ K^{-1}), which is expected to determine the thermal expansion behavior of the film in the (001) growth plane. It can be seen that the estimated in-plane GaAs lattice constant at 700 °C increases for In concentrations in the buffer layer and approaches the lattice constant of bulk GaAs at 700 °C at a buffer composition of about 9% In before leveling off . To examine the data another way, Figure 4.4 plots the measured room-temperature strain in the $In_xAl_{0.55}Ga_{(0.45-x)}As$ buffer layers and GaAs cap layers as a function of indium composition. [Uncertainties in strain measurements arise from the wide x-ray diffraction peaks in the ω direction due to incomplete strain relaxation and narrow film thicknesses.] The compressive strain in the

$In_xAl_{0.55}Ga_{(0.45-x)}As$ buffer layer on Ge/SiGe/Si increases with increasing amounts of In until reaching a threshold at about 6% indium. The GaAs layer above the buffer shows increasing tensile strain for increasing indium in the buffer until about 9% indium.

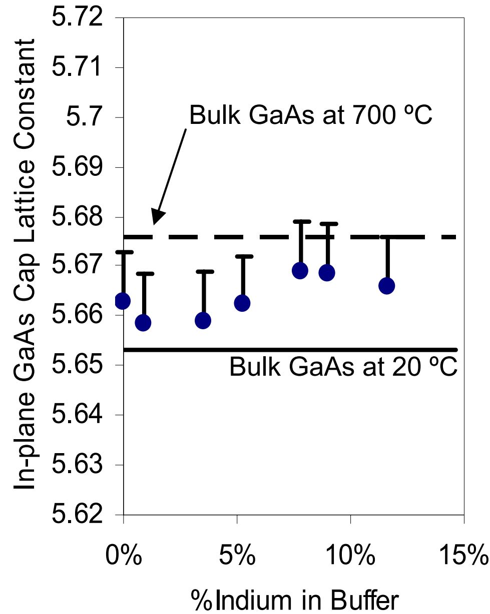

Figure 4.3: Measured room-temperature in-plane lattice constants of GaAs cap layers grown on InAlGaAs buffer layers on a Ge/GeSi/Si substrate. The plotted error bars indicate predicted in-plane lattice constants at the growth temperature.

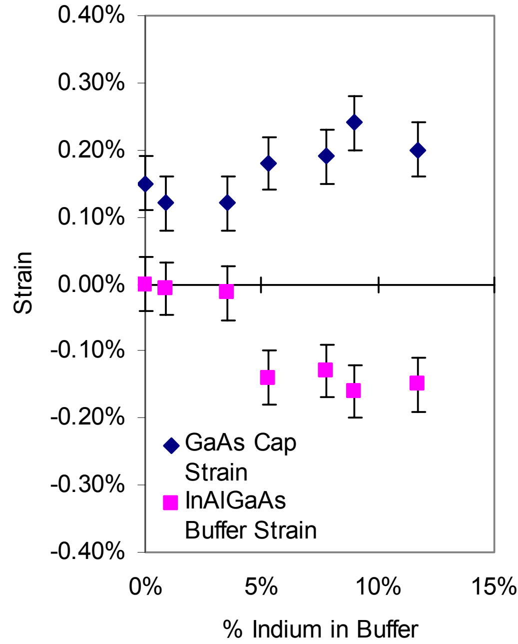

Figure 4.4: Measured room-temperature strain in an InAlGaAs buffer layer and GaAs cap layer grown on a Ge/GeSi/Si substrate at a variety of In compositions. Note the increase in tensile strain with increasing In for the GaAs buffer, which should result in lower compressive strain at the growth temperature.

It is important to consider how these strained layers actually behave during the film growth process when T_{growth} = 700°C. As shown by Roos[94] and Lum,[22] nearly all of the strain produced by the mismatched thermal expansion coefficients of a thin epitaxial film on a thick substrate would be expected to be trapped as elastic strain during film cool-down. Therefore strain measurements made after cool-down can be adjusted to reflect the approximate strain conditions during growth by subtracting out the thermal expansion mismatch strain generated for ΔT = (700°C – 20°C) = 680 °C. Figure 4.5 shows the estimated buffer and cap layer strains versus indium composition at the growth temperature. Strain at the growth temperature was estimated by multiplying the difference in thermal expansion coefficients (Δα) between the $In_xAl_{0.55}Ga_{(0.45-x)}As$ buffer and the GaAs cap and the Si substrate by ΔT, and subtracting this value from the measured room temperature strain.

$$\varepsilon_{GrowthTemp} = \varepsilon_{RoomTemp} - (\alpha_{film} - \alpha_{substrate}) \times \Delta T$$

Figure 4.5 shows that both the $In_xAl_{0.55}Ga_{(0.45-x)}As$ buffer and the GaAs cap layer should be under compressive strain at the growth temperature. When the indium in the buffer reaches about 9%, the compressive strain in the GaAs cap layer approaches its minimum value, indicating a nearly cubic GaAs surface at this temperature and buffer composition. This observation matches the data from Figure 4.3, which estimated an in-plane lattice constant very near the bulk 700 °C GaAs lattice constant for a buffer composition of about 9% In. Therefore an $In_{0.09}Al_{0.55}Ga_{0.36}As$ buffer would provide the right amount of tensile material strain in the GaAs structure above it to evenly balance the additional compressive strain due to thermal expansion mismatch for films of this thickness.

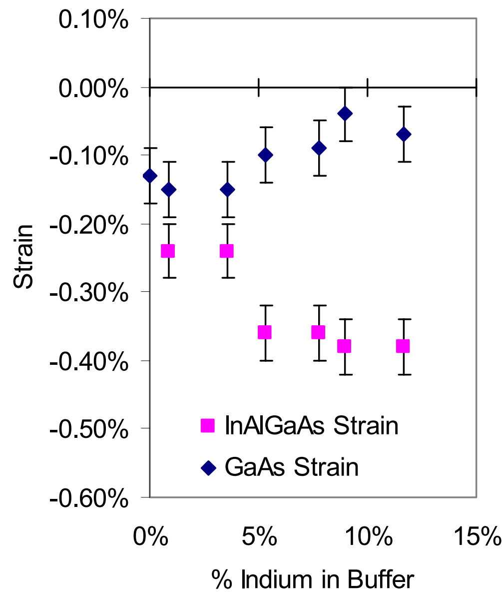

Figure 4.5: Calculated strain in InAlGaAs buffer layer and GaAs cap layer at the growth temperature on a Ge/GeSi/Si substrate as a function of In composition in the buffer layer. Note the minimized compressive strain in the GaAs cap for x_{In} = 9%.

Successful device integration requires that the insertion of an $In_xAl_{0.55}Ga_{(0.45-x)}As$ buffer layer does not increase the defect density in the GaAs cap above it. Etch pit density measurements of the threading dislocation density in the GaAs cap versus buffer indium composition are plotted in Figure 4.6. The threading density remains constant for low indium compositions, but rises rapidly above 6% indium. This measurement agrees with the increasing strain measurements in the buffer layer discussed earlier. As x_{In}

increases beyond 6%, misfit dislocations can no longer flow freely at the single interface to relieve additional strain, and new dislocations are nucleated to permit further relaxation. Many of these dislocations will terminate at the film surface as new threading segments. Although the sample with a 9% indium buffer layer showed the best strain balance at growth temperature for the GaAs layer grown above it, the threading dislocation density of 3×10^{6} cm^{-2} measured for this sample is too high for useful device integration. To avoid high dislocation densities while achieving the necessary thermal strain balance, a more efficient way of accommodating buffer layer strain is necessary.

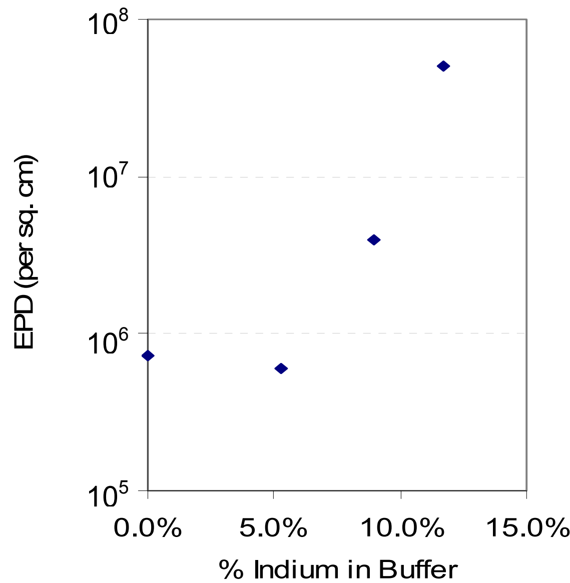

Figure 4.6: Etch pit density measurements of threading dislocation density in a GaAs cap above an InAlGaAs buffer on Ge/GeSi/Si as a function of In in the buffer. Note the rapid increase in threading density for $x_{In} > 6\%$.

4.3.3. Graded $In_xGa_{(1-x)}As$ Buffer Layer Experiments

Relaxed compositionally graded buffer layers are much more efficient at accommodating material strain than single uniform buffer layers of similar composition, yielding more completely relaxed layers with less nucleation of threading dislocations in the buffer layers. After observing the increasing threading dislocation density in the uniform $In_xAl_{0.55}Ga_{(0.45-x)}As$ buffer layers discussed above, we grew an additional series of samples on Ge/GeSi/Si substrates. In these three samples we replaced the thin uniform buffer with a relaxed graded $In_xGa_{(1-x)}As$ buffer structure. (Aluminum was removed from

the graded buffer to simplify compositional analysis, but could be reintroduced easily without dramatically affecting the results, due to the close lattice match between AlAs and GaAs.) All graded buffer layers were grown at the same growth conditions on the same substrates as the $In_xAl_{0.55}Ga_{(0.45-x)}As$ single layer structures described previously. Grading rates were kept constant for all samples at 7.2% In per micron, and the total buffer thicknesses varied from about 7000Å for the low-indium buffers to about 1.2μm for the buffers with the most indium. All samples were capped with 8000Å of Si-doped GaAs. A simple schematic of the complete structure is shown in Figure 4.1.

In Figure 4.7 the measured in-plane lattice constant ($a_{||}$) of the GaAs cap at room temperature is plotted as a function of indium composition in the buffer layer below it. The in-plane lattice constant at the growth temperature is estimated in the manner described previously for every room-temperature value as a positive error bar. The efficient relaxation provided by the relaxed graded buffer can be seen in the rapid increase in the estimated in-plane lattice constant, which approaches the bulk GaAs lattice constant at 700 °C for In concentrations less than 5%.

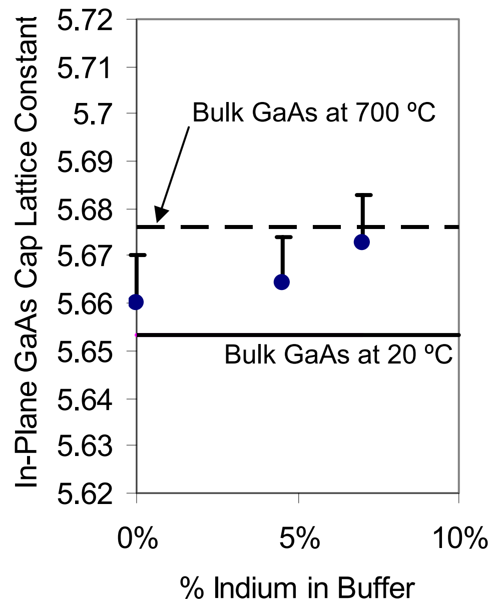

Figure 4.7: Measured in-plane lattice constant of a GaAs cap above an InGaAs graded buffer on Ge/GeSi/Si as a function of In in the buffer. The plotted error bars indicate the estimated in-plane lattice constant at the growth temperature.

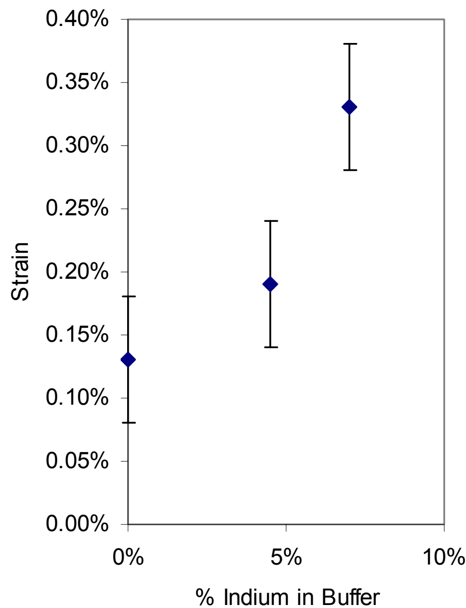

Figure 4.8: Measured room-temperature strain of a GaAs cap on an InGaAs buffer on Ge/GeSi/Si as a function of the final In composition of the graded buffer.

Figure 4.8 shows the observed room-temperature strain of the GaAs cap layer in relation to the indium composition in the buffer. Accurate strain measurements of the $In_xGa_{(1-x)}As$ buffer layers themselves were not possible with X-ray diffraction techniques due to the thinness of the stepped grading layers. Identical buffer structures with thick uniform $In_xGa_{(1-x)}As$ caps were grown on GaAs substrates and characterized with XRD to ensure accurate indium calibrations for these buffers grown on Si/SiGe/Ge. Due to the efficient strain relaxation provided by the graded $In_xGa_{(1-x)}As$ buffers in these samples, the tensile strain in the GaAs cap increased much more rapidly for smaller x_{In} than it did for the single uniform buffer layer. This rapid increase in strain is shown another way in Figure 4.9, which plots the calculated strain at the growth temperature as a function of indium concentration. The tensile material strain and the estimated thermal mismatch strain should be effectively balanced at the growth temperature for an Indium buffer composition around 6%, and the material strain should increase beyond the thermal mismatch strain for larger indium concentrations.

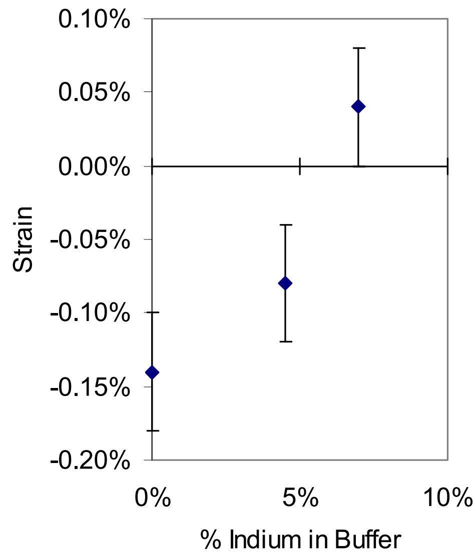

Figure 4.9: Calculated strain in the GaAs cap at the growth temperature on an InGaAs graded buffer on Ge/GeSi/Si. The strain in the cap at the growth temperature should be 0% for a graded buffer terminating at approximately 6% In.

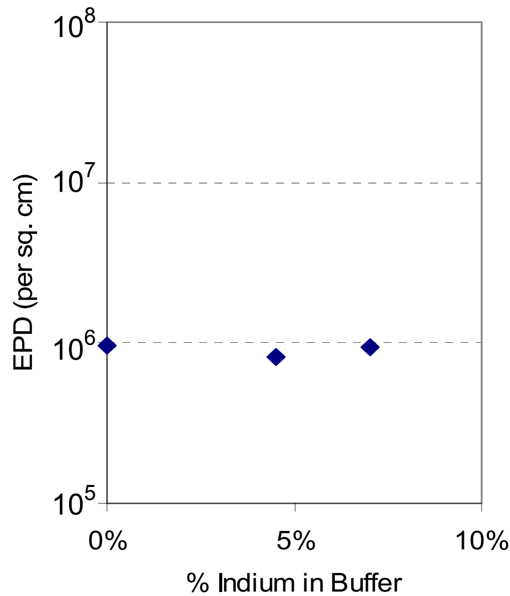

Figure 4.10: Measured threading dislocation density in a GaAs film above an InGaAs graded buffer on a Ge/GeSi/Si substrate as a function of In in the buffer layer. Note that the measured threading density does not increase with In fraction as it did for the uniform InAlGaAs buffer in Figure 4.6.

Figure 4.10 shows the surface threading defect density as a function of indium concentration. The threading dislocation density in the GaAs cap remained constant for

indium concentrations greater than 9%, holding steady at about 9×10^5 cm^{-2}, which was no larger than the measured substrate threading density before GaAs growth. This constant dislocation density implies that a relaxed graded $In_xGa_{(1-x)}As$ buffer layer with x_{In} ~ 6% should be capable of efficiently relaxing its compressive material strain without nucleating large amounts of new threading dislocations, and should therefore provide an effective virtual substrate for strained InGaAs/GaAs SQW device integration on Si/SiGe/Ge substrates.

The observation of empirical differences (as measured by x-ray diffraction and etch-pit density measurements) between the relaxation efficiency and the film quality of GaAs films grown on relaxed graded InGaAs buffer layers and single uniform buffer layers of identical composition is worth noting. Relaxed graded buffer layers provide an efficient means of material strain relief without the penalty of additional dislocation generation. The GaAs/InGaAs system explored in this experiment showed a reduction of nearly an order of magnitude in measured threading dislocation density compared to films grown above single uniform buffer layers. Empirical data such as that presented here will be are useful in building a better understanding of the benefits and the limits of mismatch accommodation via relaxed graded buffer structures for semiconductor heteroepitaxy.

4.4. Conclusions

The effects of thermal expansion mismatch strain on GaAs epilayers grown monolithically on Ge/GeSi/Si substrates were investigated. The significant differences between the thermal expansion behavior of GaAs, Ge, and Si introduces a thermal mismatch strain in GaAs films grown on a Ge/SiGe buffer layer above a standard Si wafer. This thermal mismatch strain has deleterious effects on the critical thickness of defect-resistant $In_xGa_{(1-x)}As$ strained quantum wells in the GaAs film, effectively prohibiting the direct integration of these useful device structures on Ge/GeSi/Si substrates for x_{In} values greater than 15%. We investigated strategies for removing all thermal strain at the growth temperature by using intentional material strain to balance the compression introduced by thermal mismatch. Single uniform buffer layers as well as

relaxed graded $In_xGa_{(1-x)}As$ buffer layers were used to deliberately introduce tensile strain in the GaAs layers grown above them, and this tensile strain was shown to balance the compressive thermal mismatch strain stored in the Ge cap layers at the growth temperature. $In_xGa_{(1-x)}As$ relaxed graded buffer layers in particular were shown to efficiently balance thermal strain without nucleating additional threading dislocations in the GaAs film.

Chapter 5. Optimizing Cavity Design for Laser Integration

5.1. Introduction

A semiconductor laser is a high-power minority carrier device. In addition to high material quality and demonstrated control over thermal mismatch issues, a successfully integrated III-V laser on a Ge/GeSi/Si substrate will require an optimized device design with a low laser threshold current, high optical confinement, and high mirror reflectivity.

5.2. Background: Laser Rate Equations

The operation of a semiconductor laser, and the chief differences between laser and light-emitting diode behavior, can be understood by considering the electron and photon rate equations in an optically active semiconductor. As a first approximation, consider a hypothetical two-level semiconductor system, with three possible paths for electron-photon interaction. Figure 5.1 shows these three possible mechanisms schematically.

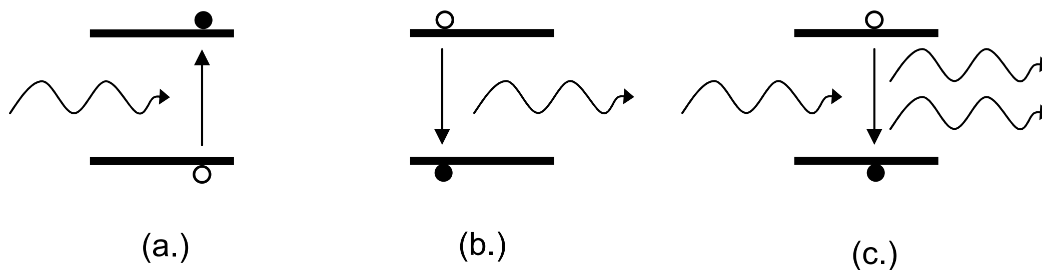

Figure 5.1: Three possible electron-photon interaction paths in a simple two-level semiconductor system: (a.) absorption, (b.) spontaneous emission, and (c.) stimulated emission.

An electron can be promoted from the low-energy level to the high-energy level by absorbing a photon with an energy $E = h\nu$ equal to the difference between the low and high energy levels. This process of photon absorption will depend on both the density of incident photons (N_p) and the density of electrons in the low-energy state (N_1). Once promoted to the high energy state, the electron can relax back to its original energy level spontaneously, by reemitting a photon with the same energy $E = h\nu$. The spontaneous emission rate will be proportional only to the density of electrons in the high energy state,

N_2. The electron can also relax when stimulated by another incident photon, falling back to its original energy level while releasing a photon with the same energy and phase as the incident photon. The stimulated emission rate will depend on both the density of high-energy electrons (N_2) and the incident photon density (N_p). A rate equation expressing all three possible electron transitions can thus be written as:

$$\frac{dN}{dt} = -R_{st}N_2N_p - R_{sp}N_2 + R_{ab}N_1N_p$$

where R_{st}, R_{sp}, and R_{ab} are rate constants for stimulated emission, spontaneous emission, and absorption, respectively. If the system is closed, then every electron relaxation will yield an emitted photon, and vice versa, so a matching photon rate equation can be written as:

$$\frac{dN_p}{dt} = R_{st}N_2N_p + R_{sp}N_2 - R_{ab}N_1N_p$$

These equations describe the electron and photon behavior for an ideal, closed two-level material system. A real semiconductor system introduces complications to this model in a number of ways. In a semiconductor crystal the energy levels are not two discrete levels but rather two continuous bands, separated by a characteristic bandgap. The bands provide many additional levels for electrons to be promoted to or relax from. Semiconductors are also subject to Pauli's exclusion principle, which forbids the population of any single energy level within a band by more than two electrons of opposite spins. A real semiconductor structure is also not a closed system, and accurate rate equations will have to account for electron injection into the device and photon losses from the system. More realistic rate equations can be written which maintain, however, the same basic form as the simple 2-level equations above:

$$\frac{dN}{dt} = -G(N)N_p - BN^2 + \frac{\eta_i I}{qV}$$

$$\frac{dN_p}{dt} = \Gamma G(N)N_p + \Gamma\beta_{sp}BN^2 - \frac{N_p}{\tau_p}$$

G(N) is the carrier-dependent gain, which measures the rate of stimulated emission and absorption as a function of the minority carrier density in the conduction band. B is the bimolecular recombination coefficient, which is directly related to the spontaneous

emission rate, R_{sp}, above. Because Pauli's exclusion principle demands that a spontaneously decaying electron must first have an empty valence-band energy level to relax into, the spontaneous emission factor is actually dependent on the carrier population in the conduction and valence bands, $NP = N^2$ (for low-level injection). The final term in the electron rate equation accounts for electron injection into the structure, and thus depends on the electron capture efficiency η_i (also known as the internal quantum efficiency), and the flux of injected electrons (I/qV). The photon rate equation is similar to the electron rate equation with the addition of a new term, Γ, which is the ratio of semiconductor volume with a positive gain coefficient (the active volume) to the total volume of illuminated material (the cavity volume). This term, also known as the confinement factor, measures how well the photons are confined in the lasing medium, and thus what fraction of the total photons are available to contribute to stimulated emission or absorption. The photon rate equation also includes a spontaneous emission factor, β_{sp}, which accounts for the large number of equivalent and non-interacting optical modes into which a photon can be emitted in a typical semiconductor crystal. The large number of possible modes (~10^5 for GaAs heterostructures) shows why spontaneous emission dominates at low current levels in light-emitting diodes. The last term in the photon rate equation introduces photon loss via an average photon lifetime τ_p. This lifetime is defined as a function of the photon group velocity, v_g, the internal non-radiative absorption α_i and the photon escape rate from the cavity, α_m:

$$\frac{1}{\tau_p} = v_g(\alpha_i + \alpha_m)$$

By considering the steady-state solutions to these electron and photon rate equations, it is possible to get a basic understanding of the behavior of a semiconductor laser structure. Under low-level injection, with low photon densities, $N_p \ll 1$ and the first terms in both the electron and photon rate equations can be ignored, leaving:

$$\frac{dN}{dt} = 0 = -BN^2 + \frac{\eta_i I}{qV}$$

$$\frac{dN_p}{dt} = 0 = \Gamma\beta_{sp}BN^2 - \frac{N_p}{\tau_p}$$

By rearranging the terms, it is possible to understand how the carrier density and photon density will change as a function of injected current, I:

$$N = \sqrt{\frac{\eta_i}{BqV} I}$$

$$N_p = \frac{\Gamma \beta_{sp} \eta_i \tau_p}{qV} I$$

Thus under steady-state low-level injection, the carrier density will scale as the square root of the injected current, while the photon density (and thus the photon flux from the device) will be linear with I. This behavior is typical for a light-emitting diode, which emits all of its light spontaneously with an emission efficiency dominated by the spontaneous emission factor β_{sp}.

The situation changes when the photon density is increased such that $N_p >> 1$. In this case, stimulated emission will dominate the electron and photon rate equations, and a similar analysis to that above yields:

$$N = N_{th}$$

$$N_p = \frac{\Gamma \eta_i \tau_p}{qV} I$$

At high photon densities, the carrier density will clamp at some fixed threshold density, N_{th}, while the photon flux will continue to increase linearly with I, although the removal of the spontaneous emission term β_{sp} from the slope will cause this increase to become much sharper. The physical reason for the disappearance of the spontaneous emission term is that photons emitted above threshold via stimulated processes are emitted into the same optical mode as the original stimulating photon, while the spontaneous photon flux is now clamped. If the photon density is then plotted vs. injected current for a typical semiconductor laser, the transition between the low-injection light-emitting diode behavior and the high-injection stimulated laser emission behavior with increasing current will be evident as a characteristic ‘kink’ in the slope of the graph. The current at which this kink occurs is referred to as the threshold current of the laser, I_{th}. A typical photon density vs. current graph for a semiconductor laser is shown in Figure 5.2.

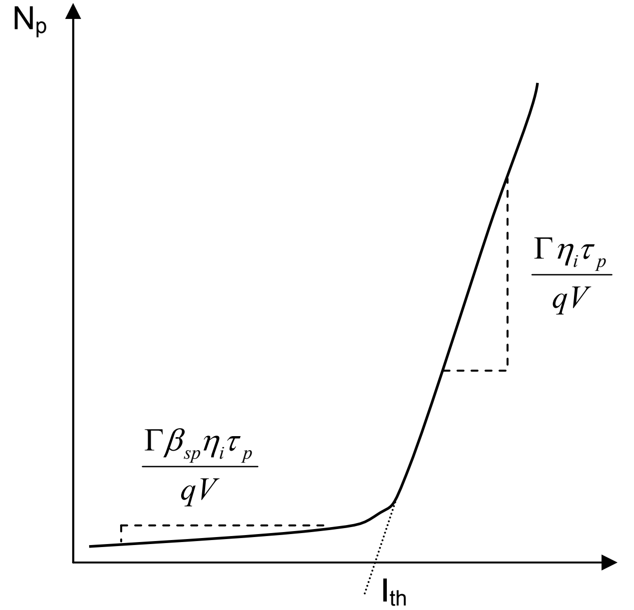

Figure 5.2: Typical photon-density vs. current graph for a semiconductor laser, showing the kink at the threshold current where stimulated laser emission dominates spontaneous LED emission.

A laser can reach its threshold only when the total rate of generated photons in the cavity equals that of the photons being lost by other processes. This will occur at steady state, when:

$$\frac{dN_p}{dt} = 0 \Rightarrow \frac{\Gamma G(N_{th})}{v_g} = \alpha_i + \alpha_m$$

Because almost all of the photons emitted by a semiconductor laser exit through the mirrors at the ends of the cavity, the photon escape rate α_m can be replaced with a distributed mirror loss to yield a threshold condition:

$$\frac{\Gamma G(N_{th})}{v_g} = \alpha_i + \frac{1}{2L}\ln\left(\frac{1}{R}\right)$$

L is defined as the optical cavity length, and R is the reflectivity of the semiconductor-air interface that serves as the facet mirror in a typical edge-emitting semiconductor laser.

From this equation, it is possible to understand what characteristic values must be optimized to produce the best performance for a real semiconductor laser. Ideally, an optimized laser will have a large confinement factor Γ, and a large positive gain at threshold $G(N_{th})$. A high-quality semiconductor laser will also have a small non-radiative

internal loss rate α_i , and a long optical cavity length L, with high mirror reflectivity, R. It must be noted that cavity length cannot be extended indefinitely because the resulting increase in active region volume will lead to unwanted increases in the laser threshold current.

The following sections will discuss the efforts of earlier authors and work in this group to maximize gain and confinement in integrated semiconductor lasers while minimizing non-radiative losses and maximizing mirror reflectivity.

5.3. Optimizing Optical Confinement

5.3.1. Introduction

The modern semiconductor laser is designed around a series of heterostructure layers that provide both electrical and optical confinement. A cross-section of a typical double-heterostructure laser is shown in Figure 5.3.

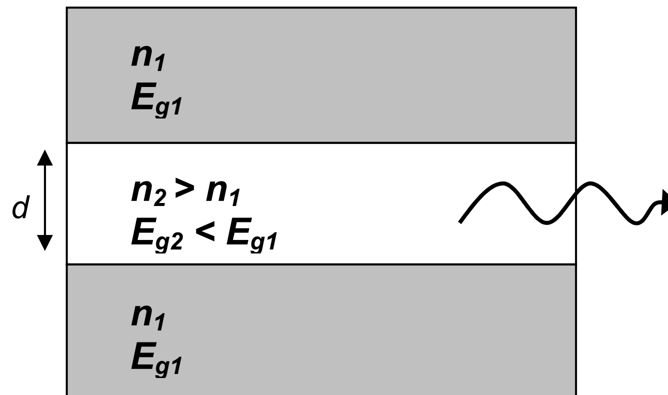

Figure 5.3: Cross section of a typical double-heterostructure laser. The outer cladding layers have a higher bandgap energy and a lower index of refraction than the inner active layer, thus serving to confine both the injected carriers and the generated photons.

As can be seen from the figure, the outer cladding layers surround an inner active layer with a lower energy bandgap and a higher index of refraction. The cladding layers thus serve to confine the injected carriers and guide the generated photons along the length of the cavity perpendicular to the layer structure. Coldren has shown how the allowed optical modes in a symmetric waveguide structure such as that in Figure 5.3 can

be solved analytically for a planar active region of thickness d with cladding and core indices of n_1 and n_2, respectively.[98]

To begin, Maxwell's equations can be used to suggest a wave equation that a guided electromagnetic wave must satisfy:

$$\nabla^2 \mathrm{E} = \mu\varepsilon \frac{\partial^2 \mathrm{E}}{\partial t^2}$$

E is the electric field in the cavity, μ is the magnetic permeability, and ε is the dielectric constant. For semiconductor materials, $\mu \approx \mu_0$, the permeability of free space, while ε is a complex number which includes both the gain and loss effects present in the material. Solutions to this equation are subject to the boundary conditions that tangential electric and magnetic fields must be equal across the dielectric boundaries on either side of the active region. Time-harmonic solutions to this wave equation exist with the form:

$$\mathrm{E}(x, y, z, t) = E_0 U(x, y) \exp^{j(\varpi t - \beta z)}\ \hat{r}$$

With transverse amplitude functions U(x,y):

$$U_2(x, y) = \begin{matrix} A\cos(k_x x) \\ A\sin(k_x x) \end{matrix}$$

for the symmetric and antisymmetric solutions in the core, respectively, and

$$U_1(x, y) = B\exp(\pm\gamma x)$$

for the solutions in the cladding layers above and below the core. Applying the boundary conditions leads to a transcendental equation that can be written for TE-polarized electromagnetic waves in terms of an effective index n_{eff} and the known waveguide characteristics n_2, n_1, and d:

$$\tan\left(\frac{k_0 d}{2}\left[n_2^2 - n_{eff}^2\right]^{1/2} - \frac{(m-1)\pi}{2}\right) = \left(\frac{n_{eff}^2 - n_1^2}{n_2^2 - n_{eff}^2}\right)^{1/2}$$

The mode index m = 1,2,3,… defines how many unique guided modes can exist in the waveguide. The free-space propagation constant k_0 is equal to 2π/λ. The effective index n_{eff} is a complex number that can be thought of as the total index of refraction felt by the guided electromagnetic wave, including both gain and loss terms. It is related to the transverse amplitude solutions U(x,y) by the relations:

$$k_x^2 = k_0^2 (n_2^2 - n_{eff}^2)$$
$$\gamma^2 = k_0^2 (n_{eff}^2 - n_1^2)$$

The transcendental equation can be solved graphically and the generated values for n_{eff} can be used to find the constants k_x, γ, A, and B, and thus the complete electromagnetic fields for the guided waves everywhere in the waveguide.

The optical confinement factor Γ is defined as the ratio between the active, positive gain volume of the core and the passive, negative-gain (absorbing) volume of the cladding that surrounds it. For confinement in the waveguide structure shown in Figure 5.3, this ratio can be expressed mathematically as:

$$\Gamma_x = \frac{\int_{-d/2}^{d/2} |U(x,y)|^2 \, dx}{\int_{-\infty}^{\infty} |U(x,y)|^2 \, dx}$$

The confinement factor can never be unity because some fraction of the electromagnetic field from the guided optical mode in the active region must leak across the dielectric barrier that separates this region from the passive waveguide structure surrounding it. In fact, the confinement factor in a standard semiconductor laser is often less than 0.1 due to additional design factors.

A number of authors have derived analytical expressions for the optical gain in a semiconductor material.[98,99,100] Casey has shown that in a simple double-heterostructure laser, gain is related to the current density (J) , internal quantum efficiency (η_i), and the thickness of the active region, d: [100]

$$G(N) \propto \frac{J\eta_i}{d}$$

This relationship implies that decreasing the thickness of the active region can increase laser gain (even though doing so will also reduce the laser confinement factor). By reducing the thickness of the active region to the order of the deBroglie wavelength in the semiconductor (~ 50Å in GaAs)[99] , the confinement factor will be reduced to less than 0.05, but the quantum effects that arise in this thin active region can yield dramatic gain improvements.

Reducing the active region thickness to quantum length scales (d = 50Å–100Å) will confine the propagating electromagnetic field in the out-of-plane (y) direction, reducing the allowed electron energies to a small number of discrete quantized levels. This quantization of the semiconductor energy bands will have the effect of reducing the number of unique electron states (because of the Pauli exclusion principle) available for electrons to populate in the active region. A reduction in the density of states will make it possible to fill the lowest conduction band and highest valence band to achieve minority carrier population inversion with a lower total level of injected carriers, and thus lower the threshold current for a laser using this material structure. A thin quantum-well active region will also produce a narrower laser gain spectrum, reduce the temperature dependence of the threshold current, and minimize the propagation of transverse magnetic (TM) polarized waves in the active region.[99] Most commercial edge-emitting semiconductor lasers now use quantum-well active structures to take advantage of their many benefits over the older double-heterostructure designs. To account for the very low confinement in quantum-well active layers, laser designers usually employ a separate confinement heterostructure (SCH). A diagram of a quantum-well SCH laser structure is shown in Figure 5.4.

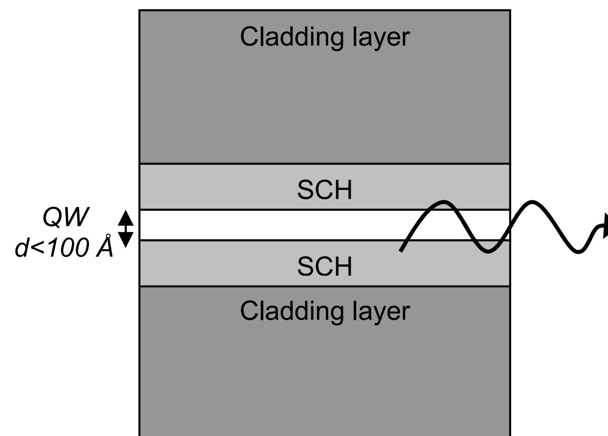

Figure 5.4: Schematic diagram of a single-quantum well separate confinement heterostructure laser. Injected carriers fall into the thin quantum well region in the center, while the surrounding SCH layers confine the generated photons.

The separate confinement heterostructure acts to confine the optical mode of the laser while the quantum well confines the electrons. An SCH structure can increase the

effective confinement of the active region and lower the laser threshold while also reducing the far-field divergence of the emitted laser beam.

Additional improvements in laser gain characteristics can be achieved using strained quantum well active regions. First proposed by Yablonovitch,[101] a strained quantum well structure uses an alloying atom with a larger lattice constant (such as In for GaAs lasers) to introduce deliberate compressive strain into the quantum well active region. This deliberate compression has three major effects: (1.) It increases the bandgap of the active region material, shortening the wavelength of the emitted light, (2.) it removes the valence band degeneracy, separating heavy holes from light holes and reducing the density of states in the valence band at the band edge, and (3.) it removes the symmetry of the valence band levels, reducing the in-plane effective mass of the carriers while increasing their out-of-plane masses. The last two effects in particular cause increased gain at lower current levels and thus lower laser threshold currents. Impressive results have been reported by a number of authors for compressively strained $In_xGa_{(1-x)}As$ quantum well lasers on GaAs substrates, and these lasers have also shown dramatic lifetime improvements.

5.3.2. Experimental Confinement Calculations

To understand the many factors at play in designing an optimum laser waveguide structure, we used the equations discussed above to estimate the confinement factors for a variety of proposed laser structures on Ge/GeSi/Si substrates. For all of the experiments in this work we focused on quantum-well active region lasers with separate confinement heterostructures. The lasers we investigated were InGaAs/GaAs/AlGaAs strained quantum well SCH devices, as well as GaAs/AlGaAs unstrained quantum well SCH devices. The InGaAs/GaAs/AlGaAs devices followed the work of previous authors[102] by beginning with an 80 Å $In_{0.2}Ga_{0.8}As$ single quantum well surrounded by a 200nm GaAs SCH layer, which was in turn surrounded by an $Al_xGa_{1-x}As$ cladding structure. The GaAs/AlGaAs quantum wells had 100Å GaAs quantum wells with 150 nm $Al_{0.2}Ga_{0.8}As$ SCH and thick $Al_xGa_{1-x}As$ cladding layers. Using the symmetric waveguide equations above, we simplified the problem to a three-level system by calculating the electromagnetic field strength in the SCH and cladding structures while ignoring the

small additional optical confinement of the quantum wells (expected to be less than 2% due to their extreme thinness).

Using the calculated electromagnetic field strengths and a calculated confinement factor Γ_x for the SCH, we were able to estimate the total energy leakage (which is proportional to the square of the field strength) at the edges of the cladding layer for a variety of cladding compositions and thicknesses. It is important to minimize the energy leakage out of the cladding layers, especially when integrating GaAs lasers on Ge/GeSi/Si substrates, because the Ge substrate layers directly beneath the cladding layer have a high index of refraction and large absorption coefficient ($n_{Ge} = 4$ and $\alpha = 2000\ cm^{-1}$ at $\lambda = 900nm$) and will rapidly absorb any optical energy that reaches the edge of the cladding layer.

A plot of the calculated electromagnetic energy in the cladding layer as a function of the $Al_xGa_{(1-x)}As$ cladding thickness for two different Al compositions ($x = 0.2, 0.6$) is shown in Figure 5.5 for the InGaAs/GaAs/AlGaAs laser structure. A similar plot for the GaAs/AlGaAs quantum well with a fixed $Al_xGa_{(1-x)}As$ composition of 60% but differing SCH thicknesses of 150 nm and 300 nm is shown in Figure 5.6.

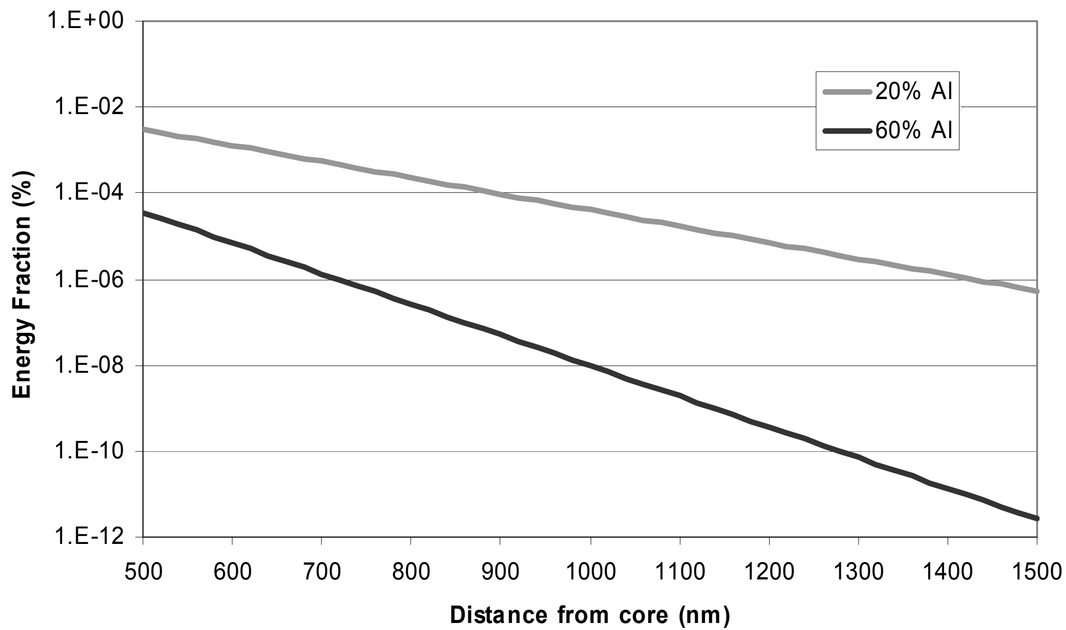

Figure 5.5: Calculated electromagnetic energy as a function of cladding thickness outside the SCH for xAl = 0.2, 0.6 for an InGaAs/GaAs/AlGaAs quantum well SCH laser structure.

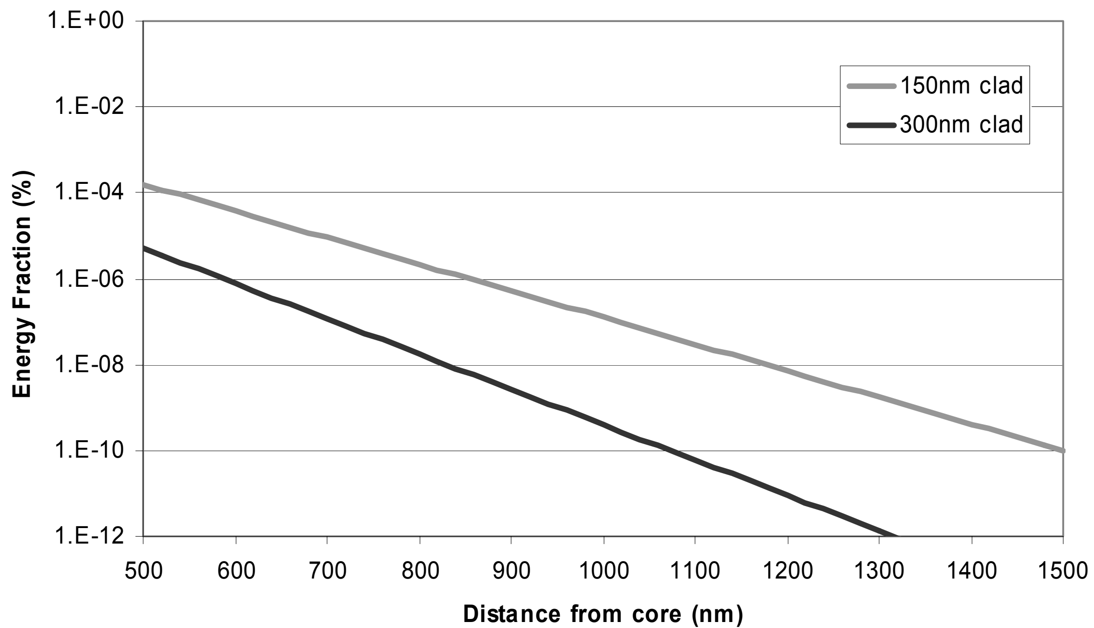

Figure 5.6: Calculated electromagnetic energy as a function of cladding thickness outside the SCH for a GaAs/AlGaAs quantum well SCH laser with d=150nm, 300nm

It can be seen from these figures that the electromagnetic energy in the cladding layer falls exponentially with distance from the core, as would be expected from the transverse amplitude function solutions described above. It is apparent that changing the Al concentration in the cladding layer has a dramatic effect on confinement, decreasing the optical energy in the cladding layer by more than two orders of magnitude when x_{Al} is raised from 20% to 60% (Figure 5.5). The thickness of the core layer also has a strong effect on the amount of energy that leaks into the cladding layer. Doubling the core thickness decreases the energy in the cladding layer by slightly more than an order of magnitude and shortens the characteristic decay length in the GaAs/AlGaAs structure evaluated in Figure 5.6. From these calculations, it is clear that ensuring low laser energy leakage into the Ge substrate layers of our Ge/GeSi/Si substrates will require high x_{Al} values and wide SCH regions. Liu has investigated the optimum cladding layer compositions and thicknesses for single quantum well InGaAs/GaAs/AlGaAs lasers on GaAs substrates.[103] Liu's work showed experimentally that InGaAs/GaAs SCH lasers with $Al_{0.6}Ga_{0.4}As$ cladding layers showed low threshold currents and high external quantum efficiencies for cladding thicknesses greater than 0.8 μm. Waveguide losses increased exponentially for thinner cladding layers and observed threshold currents climbed accordingly. From these graphs it is clear that we should expect similar results, with thicker cladding layers and x_{Al} values equal to or greater than 60% reducing waveguide losses to insignificant values 1 μm from the core.

Other material and device engineering factors will limit just how thick AlGaAs cladding layers can be. Liu has observed that thick cladding layers can contribute to increased thermal resistance and series resistance, especially for high Al-concentrations. More important to our integration experiments are issues with thermal expansion mismatch. As detailed in Chapter 4, thermal expansion mismatch between the Ge/GeSi/Si substrate and the GaAs/AlGaAs device layers can lead to large amounts of compressive strain in the GaAs layers at the growth temperature, which is converted to tensile strain upon cooling. The compressive strain at the growth temperature will relax by forming misfit dislocations, as described in the previous chapter, but the tensile strain during cooldown develops too quickly at too low of a temperature to be relieved by dislocation formation. If the tensile strain gets too large, it can trigger sudden crack

formation in the GaAs/AlGaAs device layers–a phenomenon that has been extensively investigated by Yang in our group.[104] Yang showed that there is an effective critical thickness for crack formation in GaAs/AlGaAs films grown on Ge/GeSi/Si substrates. Beyond this critical thickness, microcracks will nucleate on the surface during cooldown, with average spacings less than 100 cm^{-1}. Such microcracks will prohibit the integration of useful edge-emitting semiconductor lasers, which will have cavity lengths longer than the average crack spacing. A plot of the calculated and experimentally verified critical thickness for crack formation for GaAs/AlGaAs devices on a Ge/GeSi/Si substrate as a function of the difference between growth temperature and room temperature is shown in Figure 5.7.

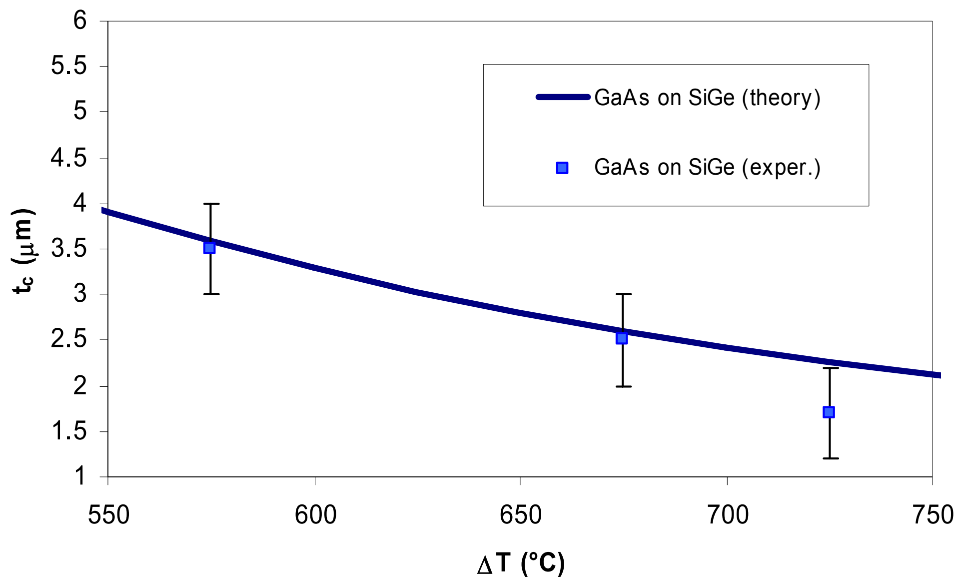

Figure 5.7: Theoretical and experimental critical crack thickness for GaAs epilayers grown on Ge/GeSi/Si substrates as a function of the difference between growth temperature and room temperature (courtesy of Yang[104])

It can be seen that for a typical growth temperature of 700 °C (ΔT = 700° − 25° = 675 °C) the expected critical cracking thickness is a little less than 3 μm. This means that the total thickness of the laser waveguide structure, including both cladding layers and the core, cannot exceed 3 μm without generating cracks in the GaAs/AlGaAs device layers. With this thickness limit in mind, a reasonable laser waveguide structure with 1μm-thick $Al_{0.6}Ga_{0.4}As$ cladding layers and a 200 nm SCH structure was chosen for our

initial laser structures as a good compromise, producing relatively high optical confinement without surpassing the cracking threshold thickness.

Additional improvements to the optical and carrier confinement of a laser waveguide structure can be achieved with the introduction of a graded-index separate confinement heterostructure (GRIN-SCH). This type of structure uses a graded compositional layer to change the index of refraction smoothly from a high value in the core to the lower value in the external cladding layer. GRIN structures have long been part of silica-based optical fibers, where they serve a similar purpose of increasing optical mode confinement without significantly increasing core or cladding diameters. A number of authors have shown how GRIN-SCH heterostructures can increase mode confinement and decrease threshold current in GaAs/AlGaAs device structures.[105,106,107,108] Zou has suggested a theoretical model for calculating the waveguide modes in a GRIN-SCH structure that uses a transfer matrix method to solve for the complex effective index n_{eff} at many discrete points in the graded waveguide structure subject to the boundary conditions of the adjacent layers.[107] With the effective index known, the complete electromagnetic field strength in the core and cladding layers can be calculated, and different GRIN-SCH structures can be compared to simple step-index SCH structures to quantify the benefits and optimize the grading parameters. Using the transfer-matrix method, Zou showed that an optimized GRIN-SCH structure will have a parabolic grading profile with a grading rate that depends on the final cladding composition. Experimental work by Aichmayr has suggested that GRIN-SCH lasers with linear grading profiles and high Al-concentrations in the cladding layers demonstrate much higher optical and carrier confinement than similar structures without GRIN layers.[105] Chinn has suggested that a GRIN-SCH with a linear grading profile provides the greatest confinement, especially at high gains and temperatures when the population of electrons at higher energy levels becomes significant.[106]

To test the benefits of a GRIN-SCH structure for our laser structures, we have followed the methods of Zou to model the electromagnetic field strengths in a GaAs/AlGaAs quantum-well SCH laser structure. To begin the analysis, a GRIN structure with a total thickness B was subdivided into N layers, with each layer having a

thickness $\Delta = B/N$ and a composition n_i determined by the shape of the grading profile. The guided wave in the ith layer must then satisfy the wave equation:

$$\frac{d^2E}{dy^2} = k_0^2(n_{eff}^2 - n_i^2)E_i$$

and will take the form:

$$E_i(y) = F_i \exp[K_i(y - y_i)] + G_i \exp[-K_i(y - y_i)]$$

where i = 0,1,2, …, N+1, F_i and G_i are propagation constants, and K_i is a pure imaginary or positive real number such that $K_i^2 = (n_{eff}^2 - n_i^2)k^2$. The index position y_i is equal to $d/2 + (i - 1)\Delta$. The problem can be simplified by considering only the fundamental TE mode, as all other modes will not propagate in a quantum-well laser. The normalized wave amplitudes in the core are set as $F_0 = G_0 = 1$, and by guessing a value for n_{eff} it is possible to calculate K_i and all of the F_i and G_i values via the expression:

$$\begin{bmatrix} F_i \\ G_i \end{bmatrix} = \begin{bmatrix} (K_i + K_{i-1})/2K_i & (K_i - K_{i-1})/2K_i \\ (K_i - K_{i-1})/2K_i & (K_i + K_{i-1})/2K_i \end{bmatrix} \times \begin{bmatrix} \exp(K_{i-1}\Delta) & 0 \\ 0 & \exp(K_{i-1}\Delta) \end{bmatrix} \begin{bmatrix} F_{i-1} \\ G_{i-1} \end{bmatrix}$$

At the final step in the GRIN, when i=N+1, the magnitude of the wave propagating into the core, F_{N+1} should be zero. By iterating n_{eff} until this condition is true, it is possible to then work backwards to find the electromagnetic field strength E_i at every point in the waveguide structure. Using this method with a small enough element size Δ, almost any GRIN-SCH grading profile can be investigated, including the degenerate case of a traditional step-index SCH. We have investigated linear graded-index SCH structures and compared them to our original step-index SCH heterostructures using this transfer matrix method. Linear grading profiles were chosen over other more complex alternatives because these were the simplest to implement experimentally in our MOCVD reactor system. The index of refraction in a GaAs/AlGaAs SCH waveguide structure is graded experimentally by gradually increasing the amount of TMAl flow in the reactor while holding all other flows constant.

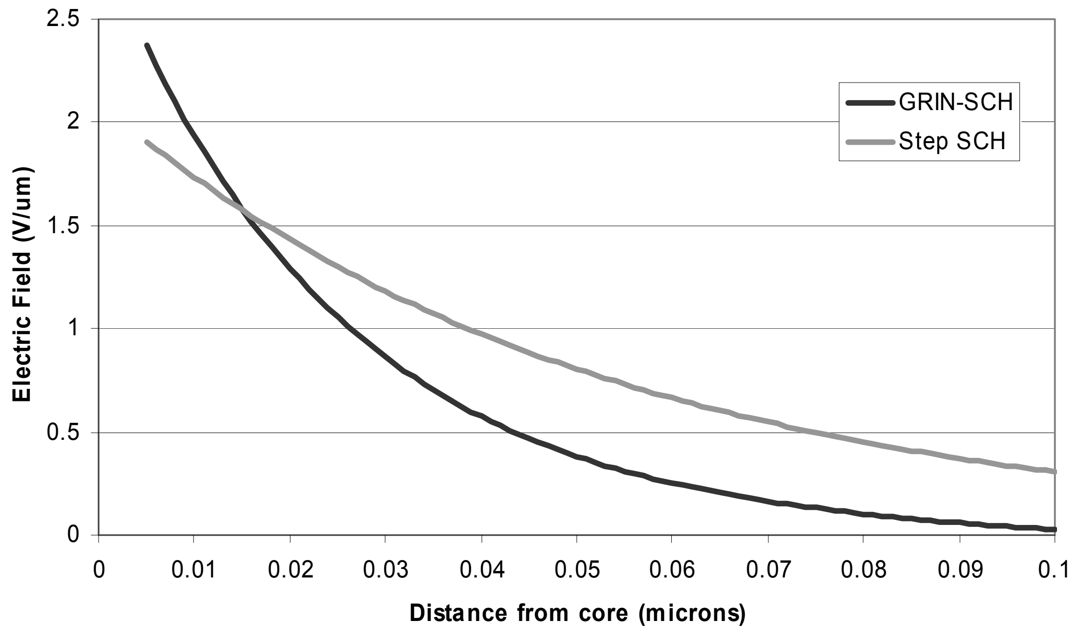

Figure 5.8: Calculated electromagnetic field strengths as a function of cladding thickness for a GaAs/AlGaAs step-index SCH compared with a GRIN-SCH waveguide structure. The core thickness is fixed for both waveguides at 100nm

A comparison between the calculated electromagnetic fields in the cladding layers of a step-index SCH and a GRIN-SCH waveguide structure is shown in Figure 5.8. Both waveguides had a core thickness of 100 nm, and the graded-index structure had a total thickness B = 200 nm. As expected, the graded index structure shows significantly increased optical confinement near the core and reduced field strength at the edge of the cladding layer. Increasing the thickness of the graded layer may increase this confinement, but Zou argues that there is a maximum GRIN-layer thickness (approximately 200 nm for an AlGaAs cladding structure) beyond which confinement will gradually decrease.

It is therefore clear from the calculations presented above that an optimized GaAs/AlGaAs laser structure for integration on a Ge/GeSi/Si substrate will have the following waveguide characteristics: (1.) a thick $Al_xGa_{(1-x)}As$ cladding layer with $x_{Al} \geq$ 60%, (2.) a wide SCH region with $d_{SCH} \geq 150$ nm, (3.) a linearly graded GRIN-SCH with $B \sim 200$ nm, and (4.) a total waveguide thickness less than 3 μm. By using these principles along with a quantum-well active region, it should be possible to achieve the highest gain and confinement values for a given laser structure, and thus the lowest

threshold currents for an integrated III-V semiconductor laser on a Ge/GeSi/Si substrate. As will be discussed in the following chapter, the actual laser devices we produced to experimentally demonstrate laser integration on our Ge/GeSi/Si substrates made use of all of the waveguide design principles detailed above to successfully create GaAs lasers on Si.

5.4. Minimizing Intrinsic Waveguide Losses

While increasing the gain ($G(N_{th})$) and confinement (Γ) of a laser structure are important goals for improving laser threshold, it is also important to reduce the waveguide losses (α_i and α_m) on the other side of the steady-state laser threshold equation, ensuring that generated photons are not absorbed or scattered before they can reach the densities necessary for lasing operation. The internal absorption coefficient α_i includes a number of factors that contribute to photon absorption in a semiconductor material. Photons can be absorbed by midgap states present at material defects (such as threading dislocations), or by intervalence band absorption between the light and heavy hole bands. Photons can also be lost via free-carrier absorption in the active region, or by scattering from the edges of the active region. Using high quality material with low defect densities and low free-carrier densities (typically achieved by setting back the doping levels in the cladding regions),[102] it is possible to reduce the internal absorption coefficient α_i to values between 3–5 cm^{-1} in standard GaAs/AlGaAs laser structures grown on GaAs substrates.[98] For integration on Ge/GeSi/Si substrates, the higher intrinsic threading dislocation density in the substrate material would be expected to increase the internal absorption. The minority-carrier lifetime measurements of GaAs devices on Ge/GeSi/Si discussed in Chapter 1 indicate, however, that non-radiative recombination does not have a large effect on minority carrier lifetimes for threading dislocation densities below 10^6 cm^{-2}. There are other photon losses that may occur for integrated GaAs lasers on Ge/GeSi/Si substrates that have not been encountered in previous work with GaAs substrate devices. Chief among these is the issue of built-in interfacial roughness from the Ge/GeSi buffer layer structure.

The graded Ge/GeSi buffer layer on a Si substrate that serves as the substrate for our laser integration experiments exhibits a characteristic surface roughness caused by the low-mismatch $Ge_xSi_{(1-x)}$ buffer layers. Small amounts of residual compressive strain that remain in the relaxed buffer layers during growth lead to the formation of surface undulations along the perpendicular [110] crystallographic directions of the (001) Si substrate.[50] This surface roughness has been described as 'crosshatch' roughness due to the distinctive pattern of perpendicular ridges that appear on inspection of a graded buffer film surface, and crosshatch patterns have also been reported for strained films on a variety of semiconductor substrates.[47,52] Relaxed graded buffer layers grown on offcut semiconductor surfaces have been shown to reflect the offcut angle in the development of their crosshatch patterns. For offcut films, the crosshatch surface ridges running parallel to the offcut direction separate into two subsets of crosshatch lines with an angle between them proportional to the wafer offcut angle.[51] Atomic force microscopy has been used to characterize crosshatch roughness, and measurements on Ge/GeSi buffers on Si substrates have shown rms roughness values averaging 13 nm for large (100 μm^2) scan areas.[27,50] The crosshatch roughness shows varying length scales, with longer period roughness ($L > 10$ μm) showing total height variations of 10 nm or more, and shorter period roughness ($L < 1$ μm) with roughness on the order of 1-3 nm. Atomic force micrographs have also been taken of GaAs device structures grown on Ge/GeSi/Si substrates, and confirmed that the Ge/GeSi surface roughness is transferred into the GaAs epilayers during MOCVD growth. A typical AFM scan of a Ge/GeSi/Si substrate surface is shown in Figure 5.9. Both the small- and large-period roughness on this surface is visible in the figure.

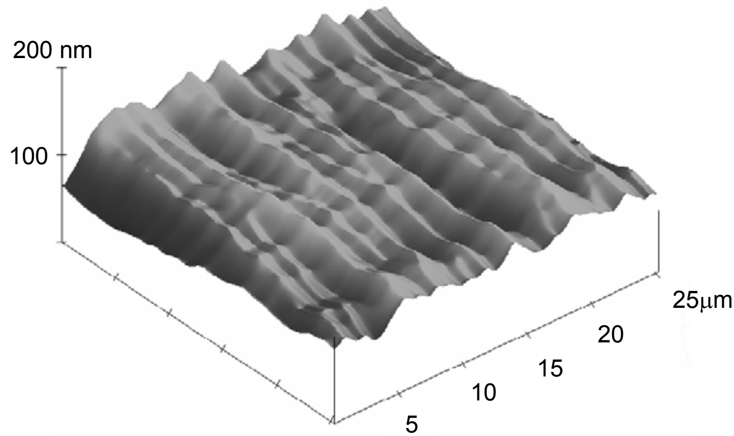

Figure 5.9: Atomic force micrograph of a Ge/GeSi/Si substrate surface. Note the periodic surface undulations that lead to crosshatch roughness.

The transfer of crosshatch roughness to the surface of an epitaxial GaAs film on Ge/GeSi/Si indicates that the waveguide interfaces in the interior of the GaAs structure are also subject to these crosshatch undulations. This conclusion suggests that waveguide interfacial scattering may be an important factor contributing to internal absorption losses for GaAs/AlGaAs waveguide structures grown on Ge/GeSi/Si substrates.

The effect of interfacial roughness on waveguide loss has been investigated by a number of authors.[109,110,111] Payne and Lacey have derived analytical expressions to estimate the effects of different types of waveguide roughness on optical mode loss.[109] They have shown that there is a rigorous upper limit to waveguide scattering loss, independent of the fabrication details or the form of the roughness:

$$\alpha \le \frac{\sigma^2}{2k_0 n_{core}} f(n_{eff})$$

where σ is the rms roughness, k_0 is the propagation constant, and n_{core} is the index of refraction of the waveguide core. The expression $f(n_{eff})$ is a function of the waveguide core thickness, d, the index of the cladding (n_{clad}) and core, and the square of the complex effective index:

$$f(n_{eff}) = \frac{k_0^4 (n_{core}^2 - n_{eff}^2)(n_{core}^2 - n_{clad}^2)}{1 + k_0 d (n_{eff}^2 - n_{clad}^2)^{1/2}}$$

From these two equations it can be seen that waveguide roughness scattering can be expected to increase rapidly with increasing rms roughness, and less dramatically with decreasing core thickness. Increasing the total index difference between the core and cladding layers will also increase the scattering loss. Two methods for decreasing interfacial scattering loss are apparent. Reducing the measured rms roughness will likely have the greatest effect, and possible methods for accomplishing this reduction will be discussed below. It should also be possible to reduce the magnitude of the scattering loss by increasing the effective index n_{eff} while keeping all other index values unchanged. One direct way to increase the effective index without changing the core or cladding index is by introducing a GRIN-SCH structure. In the calculations described in the previous section (see Figure 5.8), the real part of the effective index $\sqrt{n_{eff}^2}$ was increased from 3.28 to 3.34 by introducing a 200nm-thick linearly graded interface between the SCH and cladding layers in a GaAs/AlGaAs waveguide structure. With all other index values constant, the maximum waveguide scattering loss would be reduced by 36% by the introduction of this structure. The increased optical mode confinement of the GRIN-SCH will thus produce an additional benefit of reducing the sensitivity of an integrated GaAs/AlGaAs laser waveguide to interfacial scattering losses.

To reduce the interfacial rms roughness of the waveguide interfaces, it will be necessary to reduce the surface roughness introduced at the Ge/GeSi buffer layer. Since the crosshatch roughness is a natural feature of the graded $Ge_xSi_{(1-x)}$ buffer growth process, we investigated methods to reduce this roughness after the buffer growth step but before the integration of the GaAs/AlGaAs laser waveguide structure. Pitera in our group has investigated the chemical-mechanical polishing (CMP) of Ge/GeSi graded buffer structures on Si substrates.[112] Chemical-mechanical polishing uses a wet chemical etchant solution in conjunction with a mechanical abrasive (typically colloidal silica or alumina powder) to rapidly planarize a semiconductor surface. CMP processes have been evaluated for a wide variety of semiconductor materials,[113] and methods for planarizing Ge surfaces have been reported in the literature.[114] Pitera has shown that an adapted CMP process for Si-wafer planarization can be effective in reducing crosshatch roughness on Ge/GeSi buffer layers on Si substrates. Beginning with a Ge/GeSi buffer layer on a 6° offcut (001) Si wafer, Pitera measured the rms roughness at a variety of

length scales using atomic force microscopy. He then subjected the buffer layer to a short (10 minute) CMP planarization step to remove the top surface of the Ge cap layer. Transmission electron microscopy confirmed that this polishing step had removed approximately 50 nm from the Ge cap, and atomic force micrographs taken after the CMP step showed a reduced crosshatch roughness, especially at the shortest length scales. A summary of the averaged measured surface roughness measurements before and after planarization is presented in Table 5.1. It is important to note that rms roughness was reduced most drastically at a length scale of 1 μm. Scattering theory predicts that the highest degree of waveguide scattering will occur at roughness length scales near the wavelength of the light being scattered.[111] The operational wavelengths of our GaAs/AlGaAs or InGaAs/GaAs/AlGaAs lasers integrated on Ge/GeSi/Si substrates will vary from 0.85 μm–0.98 μm, which means that reductions in the shortest-period Ge/GeSi surface roughness will have the largest effect on interfacial scattering losses for these lasers. Using Payne and Lacey's method,[109] it is possible to estimate the maximum scattering losses due to the measured 1 μm-period Ge/GeSi surface roughness, assuming a 150 nm $Al_{0.2}Ga_{0.8}As$ SCH waveguide layer and a lasing wavelength of 860nm. The greater than threefold reduction in the post-CMP short-period surface roughness of the Ge/GeSi substrates should reduce interfacial scattering losses by more than an order of magnitude, as seen in Table 5.1.

Table 5.1: Average rms roughness and calculated maximum scattering loss of Ge/GeSi/Si wafer surfaces before and after CMP

sample	rms roughness at 10 μm	rms roughness at 1 μm	maximum scattering loss
Ge/GeSi/Si wafer before CMP	7.8 nm	1.4 nm	0.17 cm^{-1}
Ge/GeSi/Si wafer after CMP	3.2 nm	0.3 nm	0.005 cm^{-1}

The actual effects of the CMP planarization step on experimentally integrated GaAs/AlGaAs and InGaAs/GaAs/AlGaAs lasers on Ge/GeSi/Si substrates will be discussed in the next chapter.

5.5. *Minimizing Mirror Cavity Loss*

The other component of waveguide loss in a laser cavity besides the internal loss α_i is the loss due to photon escape through the laser mirrors, α_m. While some amount of photon escape is necessary to produce useful laser emission power, there must be a significant reflected component for the guided wave in the laser cavity to produce the positive feedback that drives the stimulated emission process. As stated earlier, the photon losses at the two ends of the laser cavity are divided into a distributed mirror loss throughout the cavity: $\alpha_m = 1/2L \times \ln(1/R)$, where L is the laser cavity length and R is the mean mirror reflectivity. For edge-emitting GaAs lasers, the cavity is often defined by a pair of mechanically cleaved facets, which behave as partial mirrors due to the sharp difference in index of refraction at the semiconductor-air interface.[98] Although chemically etched mirror facets have also been demonstrated,[115] it has been shown that simple mechanically cleaved GaAs surfaces provide the highest-quality mirror surfaces for edge emitting lasers. This fact is due to the fortuitous tendency of fractures in the GaAs zincblende crystal structure to propagate smoothly along the {110} slip planes, producing cleaved surfaces with near-atomic smoothness.

The theoretical optical power reflectivity, R, of a smooth GaAs mirror facet to a beam of perpendicularly incident light can be expressed as:

$$R = \left(\frac{n_{GaAs} - 1}{n_{GaAs} + 1} \right)^2$$

For optical wavelengths near the bandgap of GaAs, this reflectivity is 32%. For a typical laser cavity length of 0.5 mm, the total distributed mirror loss α_m is equal to 11 cm^{-1}. Distributed mirror losses can be decreased by increasing cavity length or by depositing high-reflectance (HR) coatings onto one or both of the cleaved facet mirrors.

Integrating a GaAs/AlGaAs laser structure onto a Ge/GeSi/Si substrate introduces additional issues that can have a negative impact on laser facet mirror performance. In particular, Si is a mechanically harder substrate material that does not cleave smoothly along {110} planes. The preferred cleavage planes for diamond-cubic Si crystals lie along the {111} faces of the unit cell.[116] For (001) Si wafers, deliberate fractures which are begun on a {110} plane (via mechanical scoring) will deviate onto alternating {111}

planes, often producing a rough, angled ‘hackle’ pattern with an average roughness of 10-100 μm on the newly cleaved surface.[117] A rough or off-angle facet pattern can dramatically reduce mirror reflectivity if it is allowed to propagate from the substrate to the mirrors of an integrated GaAs/AlGaAs laser cavity. Work on etched facet lasers has shown that power reflectivity will fall by more than an order of magnitude for mirror facets that are 2° misaligned to the waveguide axis and contain a surface roughness of more than 100 Å.[118]

Previous work on GaAs/AlGaAs lasers integrated directly on (001) Si substrates has suggested some ways to avoid the effects of substrate fracture roughening on GaAs mirror facets. Choi grew GaAs/AlGaAs quantum-well lasers on 2° offcut (001) Si substrates and produced working facet mirrors for these devices by mechanically thinning the Si substrate to a total thickness of 70 μm and cleaving mirrors from the top GaAs/AlGaAs surface.[119] The mirror cleave was encouraged to progress from the top surface by mechanically scoring a corner on the AlGaAs surface to ensure that the crack front began in the laser structure before it reached the Si substrate below. Similar methods involving mechanical thinning of the back substrate and cleaving from the top (device-side) of the wafer have been reported by a number of other authors.[120,121,122] Optical inspection of cleaved GaAs mirrors on Si substrates by Sakai has shown that the facet formed on the GaAs/AlGaAs epitaxial layer by this method appears smooth and flat, while the Si below shows a characteristic facet roughening as the crack deviates onto alternating {111} planes.[121]

The fracture behavior of GaAs/AlGaAs mirror cavities fabricated on offcut Ge/GeSi/Si substrates has not been previously characterized; however, this behavior will be important in determining whether or not cleaved-facet edge emitting lasers can be successfully integrated on our Ge/GeSi/Si substrate platforms. We have used optical and electron microscopy to investigate the microscopic fracture behavior of facet mirrors for a variety of GaAs/AlGaAs laser structures integrated on Ge/GeSi/Si substrates. To begin our experiments, we grew GaAs/AlGaAs LED devices with a total waveguide thickness of 2.5 μm on standard (001) Ge/GeSi/Si wafers 6° offcut towards the [110] direction. The waveguide structures were the same as those discussed for the autodoping studies described in Chapter 3. After fabricating ridge waveguide diode structures from these

samples in the MIT clean room, we mounted each device top side-down on a mechanical polishing chuck and removed varying amounts of the backside Si wafer surface with an alumina polishing paste. Each sample was polished for roughly 30 minutes and the sample thickness was measured after polishing with a digital micrometer accurate to ±1 μm. Three different final backside thicknesses were evaluated for their fracture behavior: 150 μm, 200 μm, and 300 μm. Because the samples were mounted to the polishing chuck with a hard wax compound, it was necessary to heat them to an approximate temperature of 150 °C after polishing to melt the wax and release the thinned devices from the chuck. This releasing step proved to be the limiting factor for samples thinned to total substrate thicknesses less than 200 μm. The samples with backside thicknesses reduced to 150 μm shattered into dozens of pieces while being heated for release from the polishing stage, and larger pieces that remained intact after release showed large amounts of visible bowing, forming convex curved surfaces that were quite brittle and broke easily with even the most careful handling. It is likely that the thermal expansion mismatch strain trapped in the GaAs/Ge/GeSi epitaxial layers that was discussed in Chapter 4 is responsible for the observed behavior of these thinned samples. With most of the backside Si removed, little mechanical strength remains in the substrate to counter the thermal mismatch strain trapped in the device and graded buffer layers, and thus the samples bend and break easily when heated, even to the relatively low temperatures necessary for wax release. Samples thinned to 200 μm remained intact during the wax release step, as did those with less Si removed. After successfully releasing the surviving test structures, all fracture experiments were carried out in the same way, with a diamond-tip scribe used to scrape a short (< 1 mm) notch on one corner of the top GaAs/AlGaAs epitaxial surface along one of the [110] directions. After scribing, the samples were turned over, and gentle pressure was applied to the back of the sample above the scribe with a razor blade. The new facet cleaved at the scribed notch and propagated along the axis of applied pressure until reaching the other edge of the sample to produce a thin bar of newly separated material. The thickest GaAs/Ge/GeSi/Si samples, with substrates thinned to 300μm showed relatively poor cleavage behavior when subjected to this cleaving procedure. Large amounts of applied pressure on the backside were required to force crack propagation, and the cleaved facets propagated

jaggedly, breaking into multiple cracks and reducing the scribed areas into collections of irregular rectangular pieces instead of the desired single bars. Samples thinned to 200 μm showed much better fracture behavior. Only light pressure with a razor blade was necessary to separate the scribed regions into rectangular bars, and the cleaved facets appeared to propagate cleanly along [110] directions, producing apparently parallel mirror facets. It was clear from these experiments then that there is an optimal thickness for cleaving integrated GaAs/AlGaAs laser structures on Ge/GeSi/Si substrates. Samples that are too thick will remain too strong mechanically and won't fracture without excessive amounts of applied pressure. Samples that are too thin will break upon release from the polishing chuck and remain too fragile to be scribed into useful devices. For our GaAs/AlGaAs test structures on Ge/GeSi/Si, the optimum thickness for the backside Si substrate was 200 μm.

Although our cleaved cavity mirrors appeared straight and smooth to the eye, it was important to characterize them microscopically as well. Especially important to note were any differences in the fracture behavior of the cleaved facets along directions parallel or perpendicular to the wafer offcut direction. Optical micrographs of the cleaved facets taken at magnifications of 1000X showed large amounts of visible roughness on the cleaved facets. The patterns of the roughness matched those observed on cleaved (001) Si facets[117] and reflected the progress of the crack front across the facet surface, moving diagonally from the top of the wafer near the scribed corner towards the bottom of the wafer on the opposite side. There was no apparent difference in either crystallographic cleaving direction, with facets cleaved parallel to the wafer offcut direction showing similar amounts of visible surface roughness to those cleaved perpendicular to the offcut direction. The resolution of the optical microscope was not high enough, however, to directly inspect the surface morphology of the facets in the thin GaAs/AlGaAs epitaxial layers, and so we examined these samples more carefully via scanning electron microscopy. Scanning electron micrographs at 20 kX magnification were taken of GaAs/AlGaAs cleaved surfaces on Ge/GeSi/Si surfaces along both perpendicular [110] directions. These images are shown in Figure 5.10.

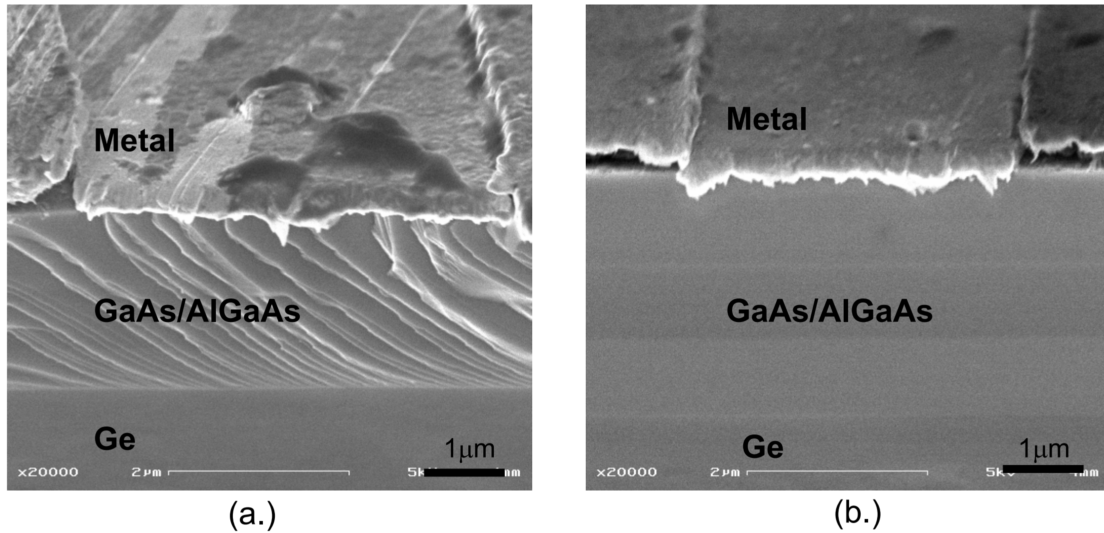

Figure 5.10: SEM image of GaAs/AlGaAs facet mirrors on a Ge/GeSi/Si substrate cleaved perpendicular (a.), and parallel (b.) to the direction of substrate offcut. Note the increased roughness on the mirror facet cleaved perpendicular to the offcut direction.

It can be seen from the SEM images that the surface produced by cleaving along the [110] direction parallel to the 6° offcut of the substrate wafer yielded a smooth facet in the GaAs/AlGaAs epitaxial layers, while the surface cleaved along the [110] direction perpendicular to the offcut showed a visible pattern of diagonal roughness. This result indicates that laser cavity mirrors on offcut substrates that are cleaved parallel to the offcut direction will be more likely to demonstrate high surface quality and higher mirror reflectivity. The reasons for this observed improvement in facet cleaving along the offcut direction are not immediately obvious. It has been shown that strained layers on offcut GaAs substrates will have a lower critical thickness for misfit relaxation along the offcut direction,[123] with misfit dislocations forming along the offcut direction at strain levels much below those required for misfit formation in the perpendicular direction. A similar behavior has been noted for cracks in GaAs caused by thermal expansion mismatch. Yang in our group has reported the earlier onset of crack formation in thermally strained GaAs layers on 6° offcut Ge/GeSi/Si substrates along the substrate offcut direction.[104] Similar results have been reported for InAlGaP tensile strained layers on InP substrates. [124] All of this evidence indicates that the resistance to microscopic and macroscopic defect propagation is reduced in offcut semiconductor wafers in the direction parallel to the wafer offcut. This reduced material strength is likely due in part to the broken

degeneracy of available slip systems that occurs along the offcut direction for misaligned wafers.[125] With fewer equivalent slip systems in the offcut direction, defects may be encouraged to move more quickly along the lowest-energy slip planes, which will have a slightly lower activation energy for breaking interatomic bonds than the equivalent slip planes in the oncut direction. Fracture that is initiated deliberately along the offcut direction will proceed smoothly and directly (as it does in the case of tensile thermal cracking) while fracture that is initiated perpendicular to the offcut direction may be encouraged during propagation to step laterally along the lower-energy offcut planes, leaving a jagged path through the crystal in its wake.

5.6. Conclusions

This chapter has presented the basic equations that govern semiconductor laser operation and waveguide cavity design. Through calculation and experiment it was shown that the best GaAs/AlGaAs laser waveguide structure for integration on a Ge/GeSi/Si substrate will maximize optical confinement and gain by making use of a quantum well active region surrounded by an optimized GRIN-SCH core and a thick AlGaAs cladding layer with a high aluminum concentration. The limit on the total laser waveguide thickness set by thermal expansion mismatch has been considered, and an optimized waveguide design for integration on our Ge/GeSi/Si substrates taking all of the optical and material factors into account has been proposed. In addition to discussing efforts to optimize optical gain and confinement, work to minimize the waveguide losses that are introduced by crosshatch surface roughness was discussed, and it was shown that a GRIN-SCH structure as well as CMP reduction of the total Ge/GeSi crosshatch roughness should improve the performance of lasers integrated on Ge/GeSi/Si substrates. Mirror facet cleaving has also been optimized by evaluating the steps necessary to produce optically smooth facet surfaces in GaAs/AlGaAs layers integrated on Ge/GeSi/Si substrates. Thinning the backside Si substrate to an optimum thickness of 200 μm, followed by the cleaving of a facet surface parallel to the substrate offcut direction has yielded reproducible high-quality mirror facets for integrated laser structures on Ge/GeSi/Si substrates. With an optimized MOCVD epitaxial growth process as well as a

proven waveguide structure and laser cavity fabrication process in place, it should now be possible to produce working GaAs/AlGaAs semiconductor lasers on Ge/GeSi/Si substrates. The demonstration of these lasers and work to improve upon their initial performance will be the subject of the next chapter.

Chapter 6. Laser Integration on Ge/GeSi/Si Substrates

6.1. Introduction

With the development of an optimized process for nucleating high-quality GaAs device layers on Ge/GeSi/Si substrates in our MOCVD growth chamber, and with a more complete understanding of the thermal expansion mismatch issues that will determine which laser structures can and can not be directly integrated onto these substrates, it should now be possible to grow and characterize heteroepitaxially integrated InGaAs/GaAs/AlGaAs laser structures on Ge/GeSi/Si substrates. The waveguide and facet mirror optimization process described in the previous chapter will guide us in choosing the laser structures most likely to produce laser operation on Ge/GeSi/Si substrates. By comparing devices grown on Ge/GeSi/Si substrates with similar structures grown on standard GaAs substrates we can understand the effects of integration on laser performance. This chapter will discuss our efforts to produce GaAs/AlGaAs and InGaAs/GaAs/AlGaAs quantum well lasers on GaAs and Ge/GeSi/Si substrates and to directly compare the performance of the resulting devices.

6.2. Background: Direct Laser Integration on Si

To understand the context of the laser integration experiments discussed in this chapter, it is useful to first review some of the previous work attempting to produce practical, monolithically integrated GaAs/AlGaAs and InGaAs/GaAs/AlGaAs lasers on Si substrates. All of this early work focused on the growth and fabrication of GaAs-based laser structures via MBE or MOCVD directly on Si substrates. The resulting GaAs and InGaAs device active layers had threading dislocation densities of 10^7–10^8 cm^{-2}, poor laser performance, and short operating lifetimes. Reports of these integrated lasers were rarely compared to identical non-integrated structures on GaAs substrates because of the enormous gap in performance that separated similar devices on different substrates.

Sakai reported a double heterostructure GaAs/AlGaAs laser grown on a 2º offcut Si substrate in a low-pressure MOCVD reactor.[121] A strained-layer superlattice structure of GaP/GaAsP was grown at the substrate interface to reduce the threading dislocation

density in the active region. No measured value for the GaAs threading density was reported. The simple transverse-junction stripe lasers that were fabricated from this material showed a high series resistance (13 Ω) and did not lase continuously. When operated under pulsed conditions with a duty cycle of 0.01% (100 ns pulses at 1kHz), the lasers turned on with a threshold current of 380 mA and a differential quantum efficiency of 2.2%.

Improved GaAs-based lasers on Si were reported by Egawa and Choi. Egawa used MOCVD and a thermal cycle annealing step to produce GaAs/AlGaAs quantum-well lasers on 2º offcut Si substrates.[126] These ridge waveguide devices had measured surface threading dislocation densities of 2×10^7 cm^{-2}. Continuous operation was recorded at an emission wavelength of 851 nm and a threshold current density of 2400 A/cm^2 at 27 ºC. The lasers had a differential quantum efficiency of 44%. Choi reported similar results for thermally cycled laser structures on offcut Si substrates that were fabricated into broad-stripe ridge waveguides.[119] These devices operated continuously with a threshold current density of 350 A/cm^2, and a differential quantum efficiency of 63%. Choi reported identical waveguide structures grown on GaAs substrates that demonstrated a threshold current density of 180 A/cm^2 and a differential quantum efficiency of 80%. The lasers reported by Egawa and Choi both failed after approximately 5 minutes of continuous operation.

Monolithically integrated GaAs/AlGaAs lasers on Si substrates with longer operating lifetimes have been reported by Deppe.[127] GaAs/AlGaAs quantum-well lasers were grown on 3º offcut Si using migration-enhanced epitaxy and a thick (2 μm) thermally cycled GaAs buffer layer. Narrow oxide stripe lasers operated continuously with a threshold current density of approximately 2000 A/cm^2. When driven at a very low optical power of 140 μW/facet, these lasers ran for approximately 17 hrs before failure, although the threshold current density increased by a factor of 3 during the first ten hours of operation.

Slightly better performance has been reported for monolithically integrated InGaAs/GaAs/AlGaAs lasers grown on Si substrates. Choi reported $In_{0.05}Ga_{0.95}As$ strained quantum well lasers grown directly on 2º offcut Si substrates above a thermally cycled GaAs buffer.[128] Narrow oxide stripe lasers operated continuously at a wavelength

of 855 nm with a threshold current of 50mA. After being bonded to copper heatsinks, these lasers operated continuously at room temperature for 56 hours at an output power of 2mW/facet. To our knowledge these are the longest lifetimes ever reported for GaAs-based lasers integrated directly on Si substrates. The dramatic improvement in operating lifetime over previous GaAs/AlGaAs quantum well devices was attributed by the authors to increased resistance of the strained InGaAs quantum well layers to dark line defect mechanisms.

It can be seen from this review that the first work on the growth and fabrication of GaAs-based lasers directly on Si substrates did not produce a practical solution for monolithic laser integration on Si. The reported threshold currents and quantum efficiencies for these early integrated lasers were much higher than similar devices on GaAs substrates, and the operating lifetimes for the best integrated devices did not exceed 60 hours. The key limiting factor in these devices for longer operating lifetimes and better laser performance remained the high threading dislocation density. By beginning with a much lower threading dislocation density in GaAs device layers grown on Ge/GeSi/Si substrates, and considering the much longer minority carrier lifetimes already measured in these layers, it seems likely that basic laser structures grown on Ge/GeSi optimized integrated substrates for this work will show dramatically better performance than the first integrated GaAs/Si lasers.

6.3. Experimental Procedure: Integrated Laser Growth and Fabrication

The basic description of the MOCVD growth reactor and epitaxial growth procedure were discussed in Chapter 2. This section will describe the specific steps that were followed for the growth and fabrication of InGaAs/GaAs/AlGaAs laser structures on both GaAs and Ge/GeSi/Si substrates.

The GaAs substrates used in our laser integration experiments were n+ Si-doped (001) GaAs wafers ($n = 1 \times 10^{18}$ cm^{-3}) that were offcut 2° toward the [110] direction. Offcut GaAs substrates have been shown to encourage smoother quantum well interfaces and higher optical efficiency in laser heterostructures.[129] The wafers we used were

surplus substrates donated by the LumiLEDs corporation and had measured surface threading dislocation densities of 10^3−10^4 cm^{-2}. The Ge/GeSi/Si substrates used in our laser integration experiments consisted of 1 μm n+ Ge cap layers grown on 10μm-thick relaxed graded $Ge_xSi_{(1-x)}$ buffer layers on n+ (001) Si wafers 6° offcut towards the [110] direction. The details of the graded buffer and cap growth process have been discussed previously.[27] The particular Ge/GeSi/Si wafers used for our experiments had measured surface threading dislocation densities of 2 x 10^6 cm^{-2} and measured rms surface roughness (with 100 μm^2 scan areas) between 10-15 nm.

To prepare substrates for MOCVD growth, they were cleaned in the MIT TRL Class 100 clean room laboratory and transported in sealed containers to the reactor chamber. The pre-growth cleaning recipes used for Ge/GeSi/Si and GaAs substrates were described in detail in Chapter 2. The Ge/GeSi/Si substrates with thin GaAs cap layers that were employed in a successful effort to stop Ge vapor-phase autodoping described in Chapter 3 were cleaned after removal from the MOCVD reactor using the same recipe as the standard GaAs substrates.

The growth nucleation procedure for the GaAs and Ge/GeSi/Si substrates differed significantly because of the very different initial surfaces presented by these two substrates. Before the growth on either substrate, the graphite susceptor and reactor chamber were baked in a nitrogen atmosphere for 15 minutes at 850 °C to drive out any adsorbed water in the chamber. Growth on GaAs substrates began with a 5 minute 200 °C anneal in H_2 to remove any remaining water from the GaAs surface. The reactor temperature was then raised to 700 °C under a flow of arsine (AsH_3) gas to maintain the necessary As-overpressure, while the TMG flow in the reactor was equilibrated by flowing into the reactor vent line for 5 minutes. With all initial flows stabilized, GaAs nucleation began with the switching of the TMG flow from the vent line to the reactor chamber, and proceeded with a typical V/III gas flow ratio of 112 and a growth rate of 26.5 Å/sec. As was described in Chapter 3, the optimized nucleation procedure for GaAs growth on Ge/GeSi/Si substrates required a 5-minute 700 °C anneal under H_2 carrier gas flow, followed by growth initiation at the same temperature. The typical V/III gas flow ratio during the initiation step on Ge/GeSi/Si was 225, and the initial growth rate remained similar to the rate on GaAs substrates. After nucleation on the Ge surface, the

V/III ratio was typically reduced to the standard GaAs value of 112 by reducing the AsH_3 flow rate.

The layer structures grown to create the laser waveguides for our experiments differed depending on the type of laser being grown. A typical GaAs/AlGaAs GRIN-SCH single quantum-well device began with an n+ doped 500nm GaAs buffer layer. This was followed by a 1 μm−thick $Al_{0.6}Ga_{0.4}As$ n-doped cladding layer (n = 5 x 10^{17} cm^{-3}). The GRIN structure consisted of a 200 nm-thick undoped $Al_xGa_{(1-x)}As$ layer in which x_{Al} varied smoothly from 0.6 to 0.2. This was followed by a thin (150 nm) undoped $Al_{0.2}Ga_{0.8}As$ SCH region with a 100Å GaAs quantum well active region at its core. A symmetric GRIN structure and p-doped $Al_{0.6}Ga_{0.4}As$ (p = 5 x 10^{17} cm^{-3}) cladding layer came next, followed at the end by a 50nm-thick p+ GaAs contact layer (p = 1 x 10^{19} cm^{-3}). Silane was used for n-doping and dimethylzinc provided the intentional p-doping in the cladding and cap layers. Slightly different waveguide structures, with additional quantum wells and $In_xGa_{(1-x)}As$ active regions, were also investigated and will be described in the text below. After growth, the lasers were returned to the MIT TRL laboratory for device processing. Two different laser processing recipes were used in our integration experiments. A simple oxide-stripe laser was fabricated on some samples using a basic two mask level recipe, while other samples were processed with a more complex four mask level broad ridge top-contact recipe. Cross-sections of typical laser structures after processing with both recipes are shown in Figure 6.1.

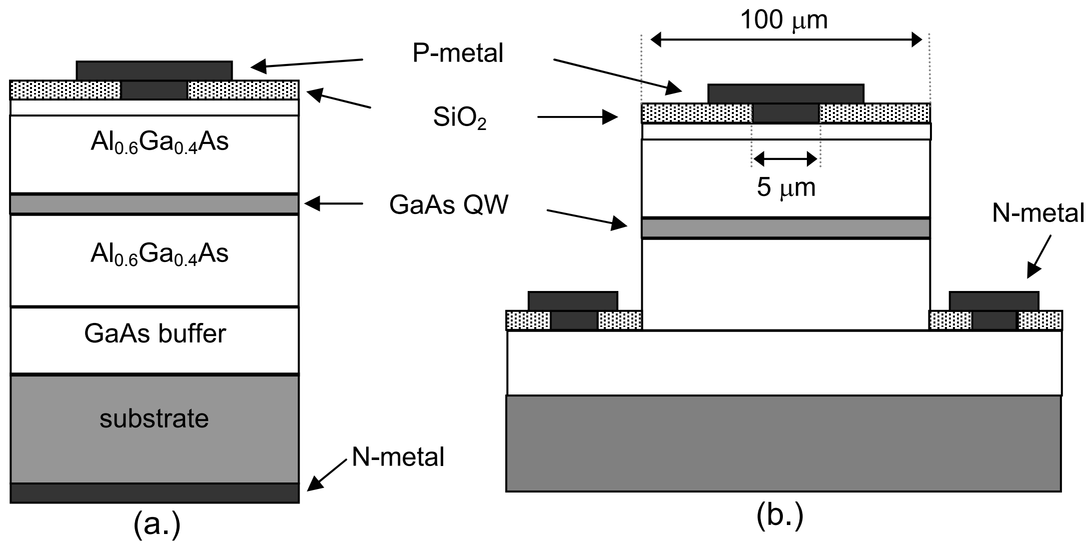

Figure 6.1: Cross-sectional schematic of a GaAs/AlGaAs quantum well laser processed with (a.) a basic two-level oxide stripe recipe and (b.) the more complex four-level top-contact recipe.

The oxide-stripe process began with the low-temperature deposition of a 3000Å-thick passivating SiO_2 oxide layer over the entire wafer. The wafer was then placed in a rapid thermal annealing (RTA) oven and raised to a temperature of 450 °C for 20 seconds to de-gas the deposited oxide layer. Laser samples where this de-gas step was not performed developed large bubbles leading to metal contact delamination during the RTA contact annealing step at the end of the fabrication process. After annealing, the lasers were coated with AZ image-reversal resist and a series of thin contact stripes (with stripe widths varied between 5−20μm in seven steps) were patterned on the oxide surface. These patterned stripes were etched in a 1:8 solution of buffered oxide etch (BOE) and water to produce contact trenches through the oxide. After this step the undeveloped resist was stripped in an acetone bath and the sample was re-coated with a new layer of resist for the metal contact liftoff patterning. The p-side (front) metal contacts were 100 μm-wide stripes centered on the oxide contact trenches and were deposited by high-vacuum e-beam evaporation. The p-metal layer consisted of a 50 Å Ti adhesion layer, followed by a 200Å Pt layer for work-function matching, which was then covered with 2500Å of Au. The samples were removed from the clean room and the back of each wafer was then removed mechanically in the manner described in Chapter 5, leaving a final substrate thickness of about 200 μm for both the GaAs and Ge/GeSi/Si

substrates. The polished backside was deoxidized in a 1:10 HCl:deionized water solution and then metallized in the e-beam evaporator to form an n-side contact. Si substrates were contacted with a 3000Å film of deposited Al, while GaAs substrates were contacted with a 500 Å Ni film followed by 2000Å of a eutectic AuGe alloy. The front and back contacts were annealed to form good ohmic contacts by placing the wafers into the RTA oven for 20 seconds at 425 °C.

A four-mask top-contact laser recipe was developed as an improvement to this basic laser fabrication recipe because it enabled the contacting of both the p- and n-sides of the GaAs/AlGaAs diode structure without passing current through the thick substrate layers. This top-contact geometry proved especially important for the devices on Ge/GeSi/Si, as will be discussed below. The improved top-contact recipe began with the etching of broad 100 μm-wide ridges through the GaAs/AlGaAs device epilayers with a 1:3:50 solution of phosphoric acid, hydrogen peroxide, and deionized water. This etch was selective for the Ge surface of the Ge/GeSi/Si substrate wafers and stopped automatically when it reached the Ge. The GaAs wafers were etched to the same depth by timing the etch after calibrating the solution with an identical structure grown on a piece of Ge/GeSi/Si. After stripe etching, the lasers were coated with a passivating oxide layer, and patterned with thin contact stripes as discussed previously. These stripes were etched in 1:8 BOE:H_2O until clear, and then metal contact layers were deposited above them in the e-beam evaporating chamber. The top (p-side) contacts were Ti/Pt/Au as before, but a new contact recipe had to be developed for the n-contact on the exposed Ge substrate material, because the n-GaAs contact recipe showed a tendency to alloy rapidly on the surface, forming discontinuous balls of non-wetted AuGe in the n-contact trenches. Making use of a contact metallization which was originally developed for GaAs/Ge solar cells reported by collaborators at Ohio State University,[130] our final n-Ge metallization recipe consisted of 300 Å of Au followed by 100 Å of Ni and then 2000 Å of eutectic AuGe, capped with a final 500 Å of Ni. The thin Au layer capped by Ni at the Ge substrate surface encouraged uniform AuGe alloy formation without de-wetting and produced smooth n-side contacts with negligible resistance along the contacts. The top-contact devices were then removed from the clean room, thinned mechanically, and cleaved into bars. Both the oxide stripe and top-contact lasers were cleaved in the

manner described in Chapter 5, by first scribing a corner of the top device layer along a [110] direction, then turning the wafer over and applying gentle pressure along the same [110] axis with a razor blade. The devices on Ge/GeSi/Si were cleaved parallel to the offcut direction, as discussed in the previous chapter, although some devices were also cleaved perpendicular to this direction to provide comparison samples, as will be discussed below.

After cleaving, the lasers were placed p-side up on a gold-coated copper block and contacted with probe tips to measure their electrical and optical properties. No direct attempt was made to heat-sink any of the devices tested here, although the stage on which they were placed was typically maintained at a constant temperature of 20 °C via a thermoelectric temperature controller. Without heat-sinking, it is expected that the temperature in the active regions of operating edge-emitting lasers can be as much as 130 °C hotter than the surface of the stage on which the substrate is resting.[131]

Power was provided to the mounted lasers via a Newport 5005 integrated laser diode power controller capable of providing continuous diode drive currents from 0.01−500mA at forward bias voltages between 0 V and 7 V. Optical power readings were collected at a single facet with an ILX Lightwave OMM-6810B optical multimeter connected to an integrating InGaAs photodetector with an operational wavelength range of 800−1600 nm. Wavelength spectra of the operating lasers were recorded by a fiber-coupled Hewlett Packard 70950B optical spectrum analyzer with a minimum resolution bandwidth of 0.08 nm and a 600nm−1700nm spectral range.

6.4. Results and Discussion

6.4.1. GaAs Substrate Devices

Our initial experiments focused on growing optimized GaAs/AlGaAs and InGaAs/GaAs/AlGaAs lasers on standard GaAs substrates to prove that the waveguide and laser fabrication recipes that had been worked out theoretically would yield operational lasers in practice. Working lasers on GaAs substrates can also provide useful

benchmarks for comparison against similar structures grown on Ge/GeSi/Si substrates and fabricated in the same manner.

The first laser on a GaAs substrate made use of the GaAs/AlGaAs GRIN-SCH quantum well structure described in detail in the experimental section above. Lasers with this structure were grown and fabricated into top-contact devices with cavity lengths of approximately 1000 μm. The lasers operated continuously (cw) at a wavelength of 853 nm with a threshold current of 127 mA, and an estimated threshold current density of 636 A/cm^2. A plot of the laser optical power vs. injected current is shown in Figure 6.2.

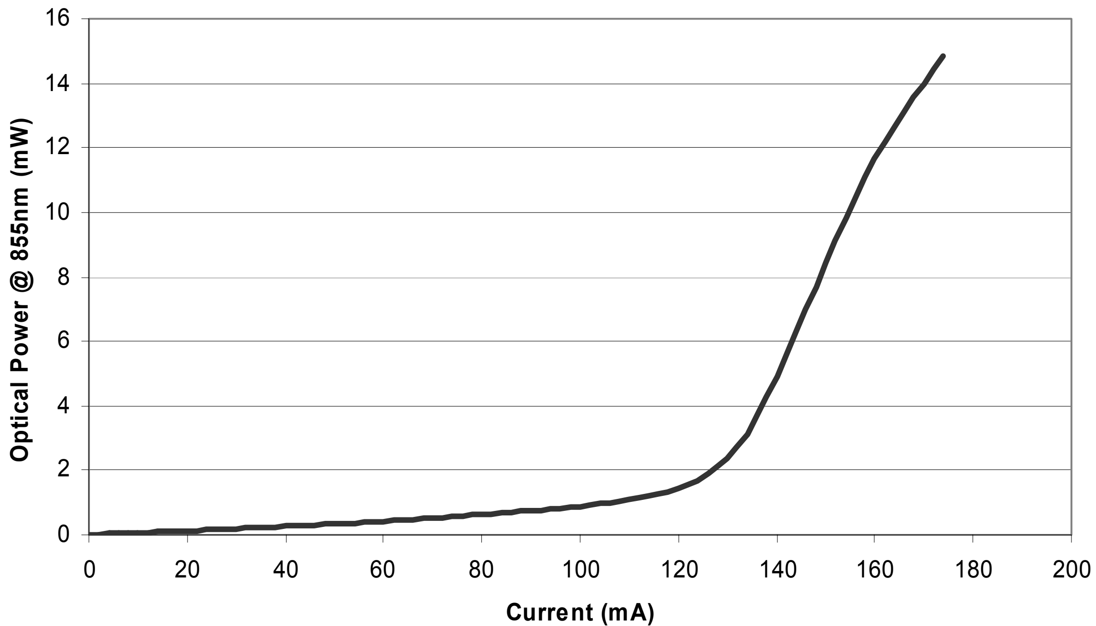

Figure 6.2: Plot of laser optical power vs. injected current for the initial GaAs/AlGaAs GRIN-SCH quantum-well laser on GaAs. The laser reached threshold at a current of 127mA.

By measuring the slope of the power vs. current graph above threshold, it is possible to calculate the differential quantum efficiency η_d per facet:

$$\eta_d = \frac{q}{h\nu}\left(\frac{dP}{dI}\right)$$

as described in Chapter 3, which for these initial GaAs/AlGaAs lasers was 24% per facet. Considering that an uncoated edge-emitting laser emits equal amounts of light from both facet mirrors, the total differential quantum efficiency was therefore 48%. The current-voltage characteristics of these lasers showed good diode behavior, with a turn-on voltage

of 1.6 V and a measured series resistance of 3.3 ohms. A graph of laser diode current as a function of bias voltage is shown in Figure 6.3. The series resistance was calculated from the current-voltage data via the method of Neudeck,[87] which involves measuring the voltage increase from ideality (ΔV) as a function of diode current at high current levels, and then using the slope of the current vs. ΔV graph to estimate the total diode series resistance. The diode series resistance can also be estimated directly by taking the inverse slope of the voltage vs. current graph at large forward biases, where series resistance is assumed to be the only source of impedance for current flow. Both methods yielded identical results for our GaAs/AlGaAs laser diodes, and so all further series resistance estimates were made using the more rapid inverse-slope method. The calculated ideality factor of this diode structure was 2.9, slightly higher than the simple GaAs/AlGaAs diode structures tested in Chapter 3, which had an ideality value of 2.6. It is likely that some of this increase is due to additional series resistance introduced by the top-contact laser geometry, which requires lateral current conduction through the n-GaAs buffer layer and introduces an effective turning resistance for the carriers injected through the n-contacts.

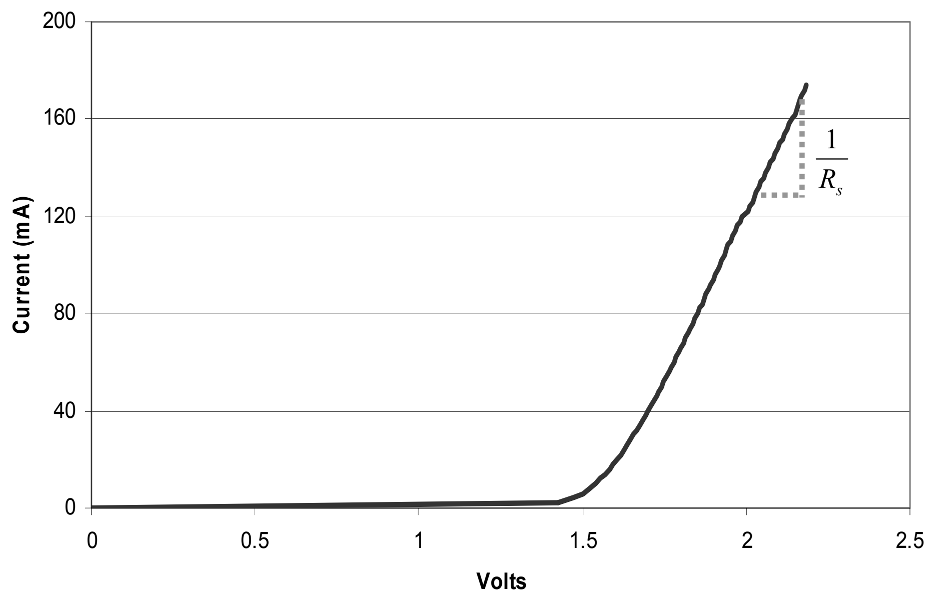

Figure 6.3: Injected current vs. voltage characteristics of initial GaAs/AlGaAs GRIN-SCH laser diode on GaAs. The series resistance (R_S) in the diode was 3.3 ohms.

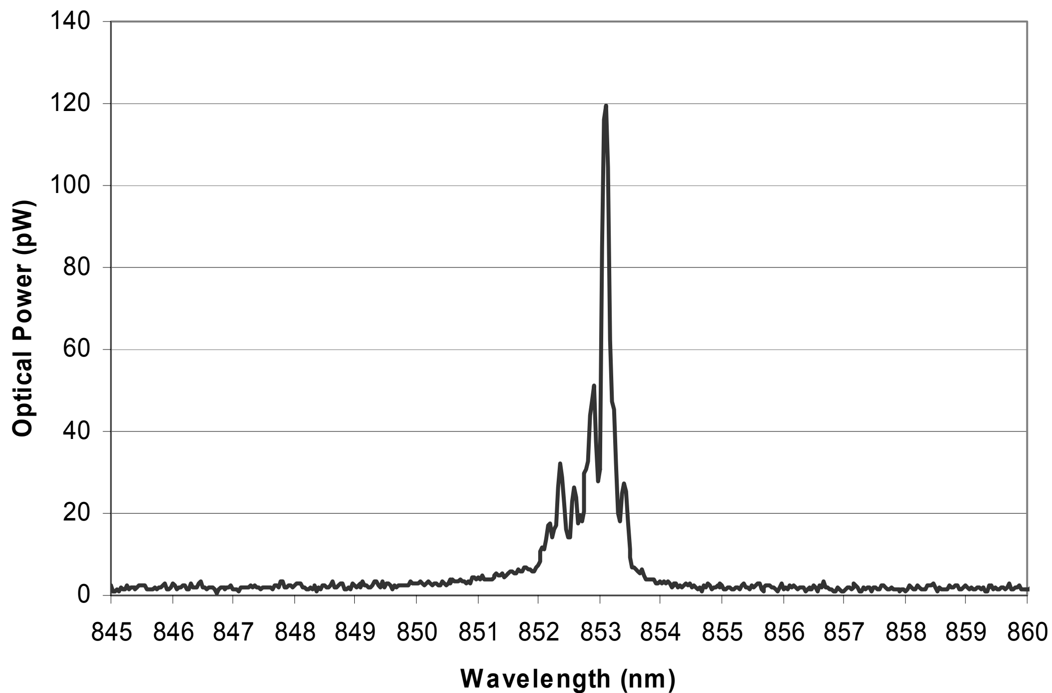

Figure 6.4: Wavelength spectrum of the initial GaAs/AlGaAs laser diode at an operating current above threshold. The laser emission wavelength shows a peak at 853.2 nm with surrounding low-intensity cavity modes.

The wavelength spectrum of the GaAs/AlGaAs laser diode above threshold is shown in Figure 6.4. The spectrum graph shows a distinctive narrow peak of the primary optical mode at 853.2 nm (FWHM < 0.1 nm), surrounded by smaller peaks from nearby cavity modes. As the current was increased above threshold, the primary laser wavelength increased as well, hopping to longer-wavelength modes as the laser active region heated up. This red-shift effect with increasing injection current has been documented in other GaAs/AlGaAs lasers[131] and is linked to the decrease in the fundamental energy bandgap in the active region as a function of temperature. The performance of a semiconductor laser as a function of temperature can also be characterized by measuring how the laser threshold current changes with external device heating. It is expected that increased carrier leakage and Auger recombination will combine to exponentially increase the total carrier density necessary for laser threshold as the temperature of an operating laser is increased.[98] The threshold current will thus be expected to increase with temperature such that:

$$I_{th} = I_0 e^{T/T_0}$$

where the characteristic temperature T_0 typically varies from 50 K for narrow-bandgap InGaAsP/InP lasers to values greater than 200 K for optimized strained-layer InGaAs quantum well devices. By measuring the threshold current of our GaAs/AlGaAs laser as the temperature of the laser stage was varied from 15–55 °C it was possible to estimate T_0 by taking the inverse slope of a plot of $\ln(I_{th})$ vs. temperature. The characteristic temperature of the GaAs/AlGaAs laser measured in this way was 127 K. Optimized GaAs/AlGaAs quantum well diodes with higher carrier confinement and reduced heating due to series resistance typically demonstrate characteristic temperatures between 150–180 K.[98] A plot showing the observed change in laser threshold current as a function of temperature for our GaAs/AlGaAs GRIN-SCH quantum-well laser is shown in Figure 6.5.

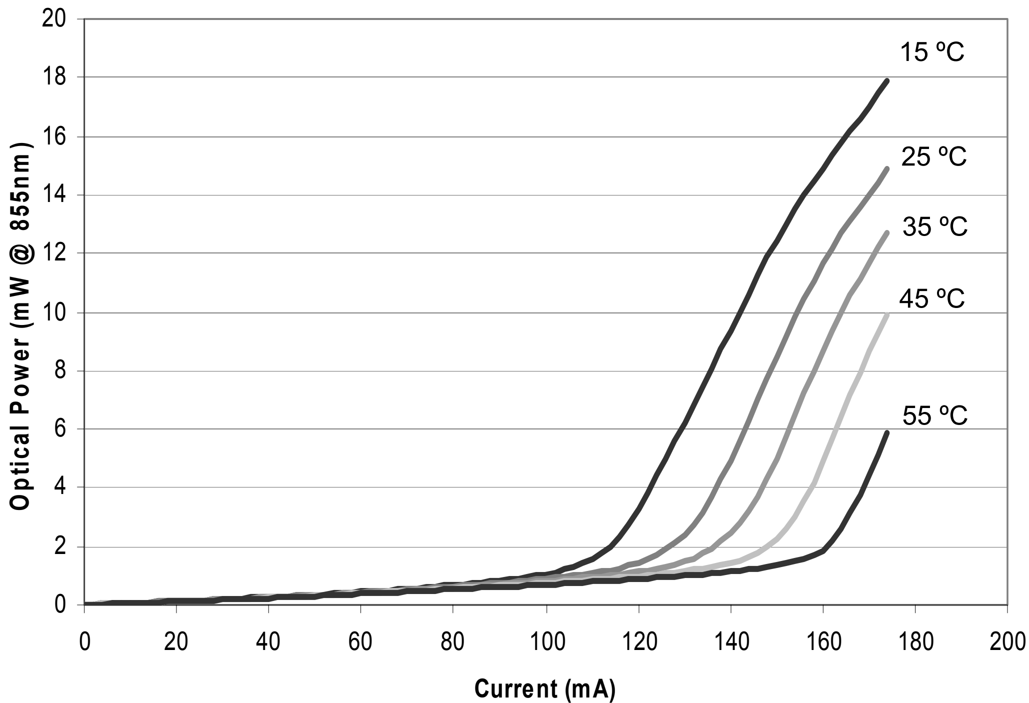

Figure 6.5: Laser power vs. current as a function of increasing temperature for the initial GaAs/AlGaAs GRIN-SCH quantum well diode on GaAs. Note the increasing threshold current with increasing test stage temperature.

Adding deliberate compressive strain to the quantum well active region of a laser by introducing an $In_xGa_{(1-x)}As$ alloy should increase the laser quantum efficiency and reduce the threshold current, as was discussed in Chapter 5. To confirm this expectation for our experimental devices, we grew an $In_{0.2}Ga_{0.8}As$ strained quantum well GRIN-SCH laser on a GaAs substrate for comparison with the initial GaAs quantum well device detailed above. The strained quantum well device had a similar waveguide structure, with 1 μm-thick $Al_{0.6}Ga_{0.4}As$ cladding layers and a 200 nm GRIN layer with x_{Al} varied smoothly from 0.6 to 0.2. A 200nm GaAs SCH layer was grown to surround the strained quantum well, which was 80Å thick. The laser was processed in the same manner as the GaAs/AlGaAs laser, with etched top contacts and an oxide mask defining narrow laser stripes for p-side metallization. These lasers were tested under cw operating conditions, and showed laser operation at a wavelength of 1009 nm. A comparison of the optical power vs. injected current characteristics of the InGaAs and GaAs quantum well lasers on our GaAs substrates is shown in Figure 6.6.

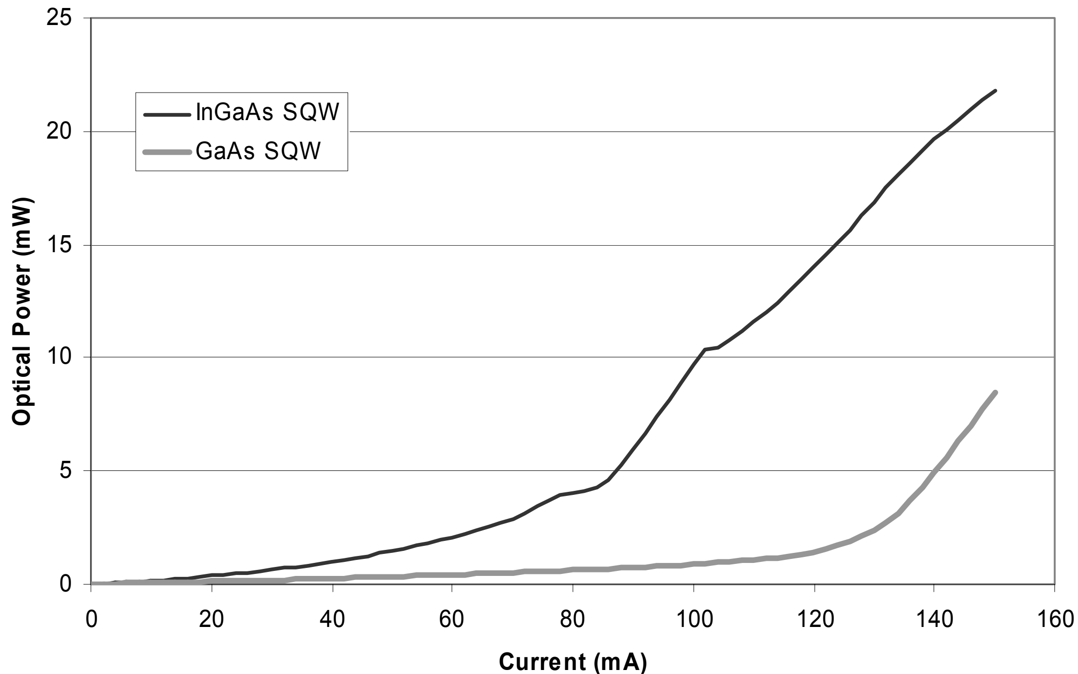

Figure 6.6: Side-by-side comparison of the optical power vs. current characteristics for GaAs and InGaAs quantum well devices on GaAs substrates. The optical power readings are normalized to take into account the different emission wavelengths. The InGaAs quantum well device shows lower threshold current density and slightly better differential quantum efficiency.

The lasers with $In_{0.2}Ga_{0.8}As$ strained quantum well active regions showed dramatic performance improvements, particularly for the threshold current density, which decreased to 370 A/cm^2 (threshold current of 74 mA) from the GaAs quantum well device threshold density of 636 A/cm^2. The differential quantum efficiency also improved to 54% from a value in the GaAs quantum well of 48%. An inspection of the graph shows kinks in the optical power curve for the $In_{0.2}Ga_{0.8}As$ quantum well device and inspection of the optical wavelength spectrum confirmed that these kinks were due to wavelength mode shifts caused by cavity heating. The cause of this cavity heating was suggested by injected current vs. voltage data for the InGaAs quantum well devices. The series resistance in these devices was 3.9 ohms, slightly higher than the GaAs active region lasers. The calculated ideality factor was 3.0, also slightly higher than the GaAs quantum well structures.

It was clear from the InGaAs/GaAs/AlGaAs quantum-well device results on a GaAs substrate that the strained-quantum well structure, with a much lower threshold current and a larger differential quantum efficiency, would be a strong candidate for integration on Ge/GeSi/Si substrates. The series resistance and relatively high ideality factors for all of the top-contact lasers initially tested encouraged us to seek an optimized InGaAs/GaAs/AlGaAs laser structure with better electrical characteristics and improved optical efficiencies. To achieve this goal we grew a double-quantum well $In_{0.2}Ga_{0.8}As$/GaAs SCH laser on a GaAs substrate and processed it with the two-mask simple oxide stripe laser process described in the experimental section above. The laser structure began with a 200 nm n+ GaAs buffer layer followed by an n-doped 1 μm $Al_{0.3}Ga_{0.7}As$ cladding layer. The concentration of aluminum (x_{Al}) was lowered slightly in this device in an effort to decrease the amount of oxygen incorporation in the cladding layers. The laser structure continued with a 200 nm GaAs SCH structure centered on two 80 Å $In_{0.2}Ga_{0.8}As$ quantum wells separated by a 100Å GaAs spacer layer. The addition of an extra quantum well to a laser active region will effectively double the optical confinement factor, Γ, although it will also increase the total threshold current by increasing the injected minority carriers necessary to achieve population inversion for both quantum wells. The laser structure was completed with a p-doped 1 μm

$Al_{0.3}Ga_{0.7}As$ top cladding layer and a 50 nm p+doped GaAs cap. The lasers were patterned and cleaved into bars with cavity lengths of approximately 1000 μm.

The combination of an additional quantum well and reduced Al concentration in the cladding regions led to the best performance characteristics yet recorded for our InGaAs/GaAs/AlGaAs quantum well devices on GaAs substrates. The double-quantum well laser turned on with a wavelength of 982.7 nm and a threshold current of 56 mA, which translated into a threshold current density of 781 A/cm^2 (or 390 A/cm^2 per well). The differential quantum efficiency was 62%, and the current-voltage characteristics also improved, demonstrating a calculated ideality factor of 2.03, and a measured series resistance of 0.8 ohms. A graph of the optical power vs. current characteristics of our best $In_{0.2}Ga_{0.8}As$ double quantum well laser on a GaAs substrate is shown in Figure 6.7.

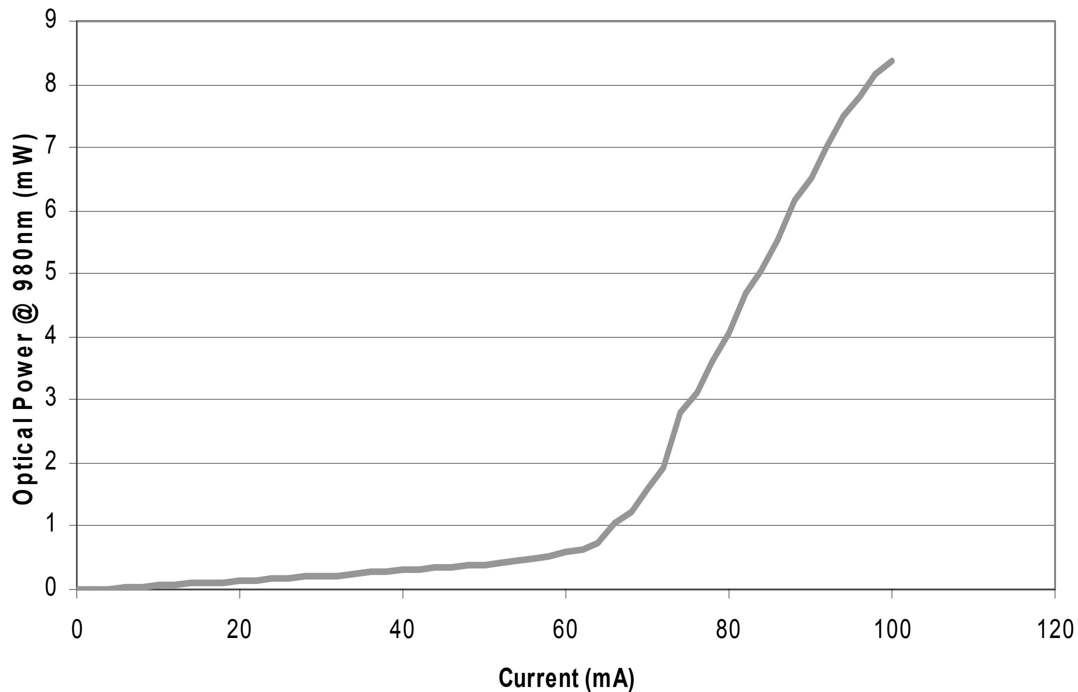

Figure 6.7: Optical power vs. current for an InGaAs double quantum well laser on a GaAs substrate. This device had the best operating characteristics of all the lasers fabricated on GaAs substrates.

6.4.2. Ge/GeSi/Si Substrate Devices

After demonstrating and comparing the performance of GaAs/AlGaAs and InGaAs/GaAs/AlGaAs quantum well lasers on standard GaAs substrates, our next step

was to investigate the performance of similar structures fabricated on Ge/GeSi/Si substrates. It would seem logical to choose the device design with the best performance on GaAs as the first candidate for integration on our Ge/GeSi/Si substrates, considering the additional challenges any integrated laser will face on the Ge/GeSi/Si substrate platform. These challenges will include the increased density of non-radiative threading dislocations in the active region of the device, the additional amount of interfacial waveguide roughness due to the Ge/GeSi crosshatch pattern, increased built-in strain from the GaAs/Ge/Si thermal expansion mismatch, and issues with smooth facet mirror formation on Si substrates. The thermal expansion mismatch issues discussed in Chapter 4 will present a particular challenge for the integration of compressively strained $In_xGa_{(1-x)}As$ active regions on Ge/GeSi/Si substrates, although these strained quantum well structures promise the greatest performance and device lifetime benefits. Taking the promised benefits into consideration, along with our earlier demonstration of dramatically improved lasers on GaAs substrates making use of $In_{0.2}Ga_{0.8}As$ strained active layers, we decided to attempt our first integration experiment on a Ge/GeSi/Si substrate using a $In_xGa_{(1-x)}As$/GaAs/AlGaAs SCH heterostructure. To account for the expected decrease in the effective critical thickness for strained $In_xGa_{(1-x)}As$ layers on Ge/GeSi/Si substrates, we reduced the concentration of In in the active layer to 12%, and chose to include only one quantum well instead of the two-well structure demonstrated on GaAs. All other aspects of the GaAs/AlGaAs waveguide structure remained the same as those for our most successful GaAs-substrate device, with 1 μm-thick $Al_{0.3}Ga_{0.7}As$ cladding layers and a 200 nm GaAs SCH surrounding an 80 Å InGaAs quantum well. The lasers were patterned with the same recipe, forming simple oxide-stripe cavities with cavity lengths of 1000 μm.

The electrical and optical characteristics of our first integrated InGaAs/GaAs/AlGaAs laser structures on Ge/GeSi/Si substrates were quite poor. A graph of the optical power vs. current data from the best of these initial devices is shown in Figure 6.8, where it is compared to curves from the similar device on a GaAs substrate discussed above. A plot of the measured current vs. voltage data for the device on Ge/GeSi/Si is compared to the GaAs-substrate device on a semi-log scale in Figure 6.9.

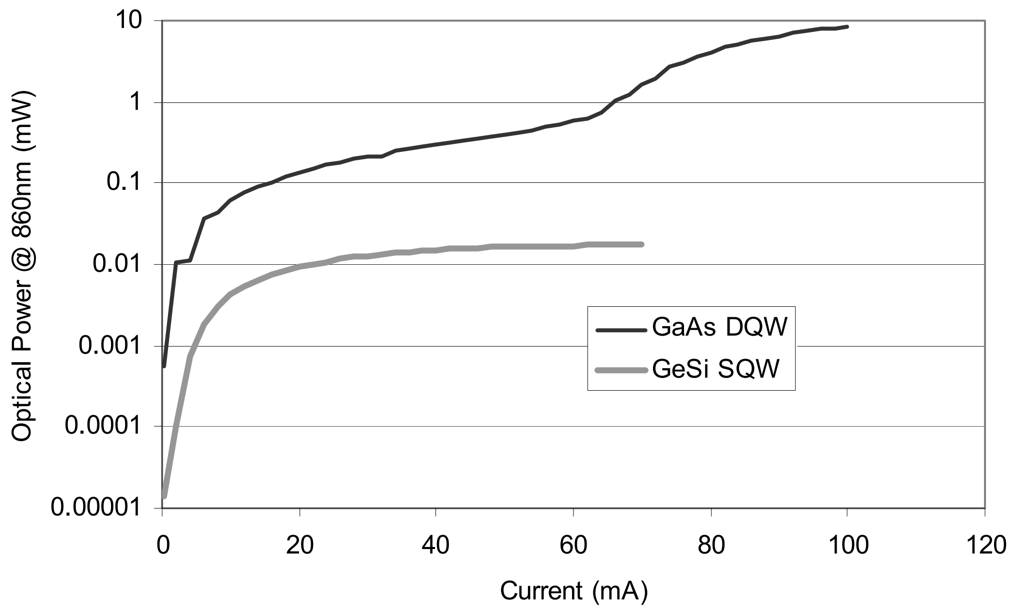

Figure 6.8: Optical power vs. current for the first InGaAs/GaAs/AlGaAs quantum well laser structures integrated on Ge/GeSi/Si substrates. A plot of the power vs. current data for a similar device on GaAs is shown for comparison. The laser structure on Ge/GeSi/Si shows much lower emission efficiency and never turns on.

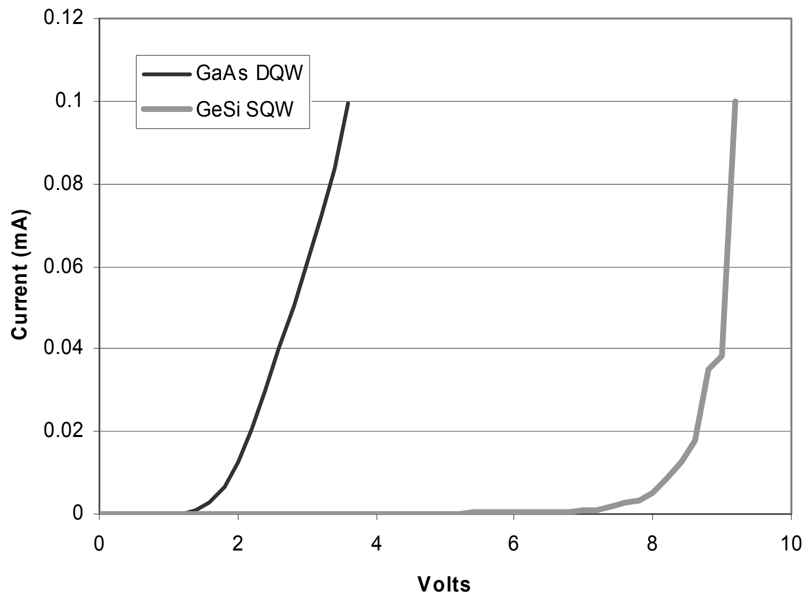

Figure 6.9: Measured diode current vs. voltage for the first InGaAs/GaAs/AlGaAs laser structures integrated on Ge/GeSi/Si. The current-voltage characteristics of a similar device on GaAs are shown for comparison. Note the much higher turn-on voltage for the device on Ge/GeSi/Si.

It can be seen from the optical power curve that the waveguide structure on Ge/GeSi/Si never achieved laser operation, and in fact demonstrated total output optical power more than two orders of magnitude lower than the similar device on GaAs. Measurements of the sub-threshold slope of the optical power vs. current graph allowed us to estimate the differential quantum efficiency of the device on Ge/GeSi/Si to be 0.015%. The sub-threshold quantum efficiency of the laser structure on GaAs was 1.6%. A similarly large gap in performance was noted in the current-voltage data, where the device on Ge/GeSi/Si had a calculated ideality factor of 3.4 and an estimated series resistance of 12.7 ohms. The same device on GaAs had an ideality factor of 2.03 and a series resistance of 0.8 ohms.

There are a number of possible explanations for the poor performance of this first integrated InGaAs/GaAs/AlGaAs laser on a Ge/GeSi/Si substrate. The reduction in the number of InGaAs quantum wells and the fraction of In in the quantum well reduced both the optical confinement factor and the injected carrier confinement. The higher threading dislocation density and increased interfacial roughness from the Ge/GeSi/Si substrate increased the effective internal absorption coefficient (α_i) . But the chief and most significant reason that these first integrated devices on Ge/GeSi/Si did not lase was Ge autodoping in the InGaAs/GaAs active regions. These first integrated devices were grown before the discovery of the dominant role played by vapor phase transport of Ge in the MOCVD growth system, and thus did not make use of the two-step optimized growth recipe discussed in Chapter 3 to remove all Ge sources from the reactor environment. It is certain that these initial integrated InGaAs/GaAs/AlGaAs lasers contained unintentional concentrations of Ge in the active and cladding layers of at least 1×10^{18} cm^{-3}. As discussed in Chapter 3, this amount of Ge contamination leads to compensation of intentional dopants in the cladding layers and increased free-carrier absorption in the active layers of a laser structure. The performance of these first laser structures on our Ge/GeSi/Si substrates is a direct illustration of the dramatic negative effect that Ge autodoping can have on actual InGaAs/GaAs/AlGaAs integrated laser structures, and confirms the importance of the steps described in Chapter 3 to minimize this Ge autodoping behavior.

Our next integration experiments for lasers on Ge/GeSi/Si substrates focused on eliminating Ge vapor phase transport into the GaAs heteroepitaxial layers. As was detailed in Chapter 3, we showed that a two-step GaAs nucleation procedure, in which a thin GaAs passivating layer is nucleated on the Ge/GeSi/Si substrate and the substrate and reactor chamber are then cleaned before regrowing the GaAs/AlGaAs device structure, will eliminate almost all detectable Ge transport into the device layers. GaAs/AlGaAs LEDs grown on Ge/GeSi/Si substrates following this improvement in the GaAs/Ge nucleation recipe showed 100X improvements in their differential quantum efficiencies and much better current-voltage characteristics.

After demonstrating successful control of Ge incorporation in our integrated structures on Ge/GeSi/Si, we attempted again to demonstrate a functioning laser structure on a Ge/GeSi/Si substrate. To avoid any possible complications from thermal mismatch-induced misfit relaxation in a compressive InGaAs active layer, we decided to begin with a simple GaAs/AlGaAs GRIN-SCH quantum well structure similar to the first laser structure successfully demonstrated on a GaAs substrate. This laser structure began with a 500nm-thick n-doped GaAs buffer layer that included the initial passivating GaAs layer grown for autodoping control as well as an additional thin GaAs layer grown after the reactor cleaning step. The buffer was followed by an n-doped 1 μm $Al_{0.6}Ga_{0.4}As$ cladding layer and a 200 nm GRIN graded layer with x_{Al} varying smoothly from 0.6 to 0.2. A 150 μm $Al_{0.2}Ga_{0.8}As$ SCH layer surrounded a 100Å GaAs quantum well, which was followed by a matching GRIN and p-doped $Al_{0.6}Ga_{0.4}As$ cladding layer. The structure was terminated with a 50nm p+ GaAs cap. A cross-section TEM image of the laser structure on a Ge/GeSi/Si substrate is shown in Figure 6.10.

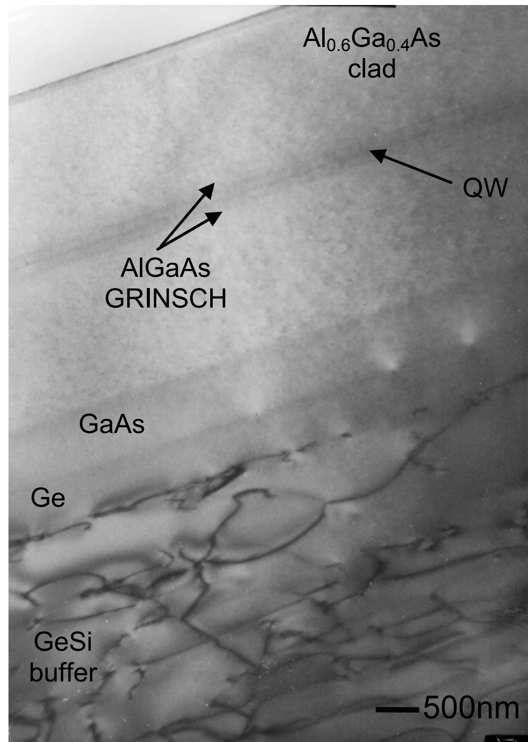

Figure 6.10: Cross-section TEM image of a GaAs/AlGaAs GRIN-SCH quantum well laser on Ge/GeSi/Si.

Laser bars were fabricated using the top-contact mask set and to investigate the effects of cleaving direction on laser performance, identical lasers were fashioned with mirrors cleaved parallel to the substrate offcut direction and also rotated perpendicular to the offcut direction. To enable a direct comparison of the effects of the Ge/GeSi/Si substrate on laser performance, identical devices were grown and fabricated in parallel on standard GaAs substrates.

All fabricated lasers were mounted p-side up and tested as before. The integrated GaAs/AlGaAs GRIN-SCH quantum well devices showed the first continuous room-temperature laser operation ever observed on Ge/GeSi/Si substrates. The lasers with mirrors cleaved parallel to the offcut axis of the substrate wafer turned on at a threshold current of 86 mA and a resulting threshold current density of 577 A/cm^2. Identical lasers on GaAs substrates turned on with a slightly lower threshold current density of 529 A/cm^2. The emission wavelength for both lasers was 858 nm. The laser structures on Ge/GeSi/Si with mirrors cleaved perpendicular to the offcut direction of the substrate wafer did not turn on, despite being grown and processed in exactly the same way as the working lasers on Ge/GeSi/Si. These rotated lasers had similar sub-threshold differential

quantum efficiencies to the laser cavities cleaved perpendicular to them, indicating that internal absorption losses in the different devices were not the limiting factor for reaching threshold. Instead it is most likely that the reduced reflectivity of mirrors cleaved perpendicular to the substrate offcut direction was responsible for the inability of these lasers to reach threshold. As discussed in Chapter 5, reflectivity is a strong function of mirror facet roughness, and reduced mirror reflectivity can increase the distributed mirror loss coefficient and raise the minimum threshold gain to unattainable levels. A plot of the measured optical power vs. current data for integrated devices on both Ge/GeSi/Si and the GaAs substrate control sample is shown in Figure 6.11.

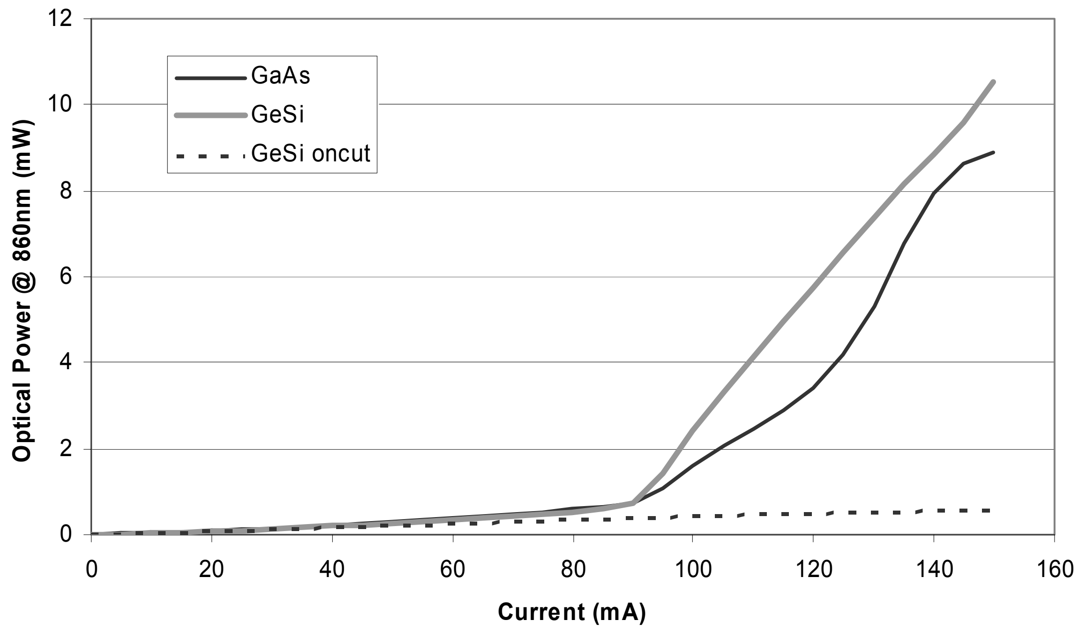

Figure 6.11: Optical power vs. current for GaAs/AlGaAs GRIN-SCH quantum well lasers integrated on Ge/GeSi/Si substrates with mirror facets cleaved parallel and perpendicular to the substrate offcut direction. Also included for comparison is the optical power vs. current data for an identical laser structure grown on a standard GaAs substrate and processed in parallel.

The measured differential quantum efficiency for the integrated GaAs/AlGaAs laser on Ge/GeSi/Si was 24%. The control laser on GaAs had a differential quantum efficiency of 32%. Measurements of the current-voltage characteristics for both devices showed slightly better performance in the control devices on GaAs substrates. The measured series resistance on the GaAs substrate was 3.9 ohms, with a turn-on voltage of 1.3 V, while an identical device on a Ge/GeSi/Si substrate showed a series resistance of

6.3 ohms and a turn-on voltage of 1.6 V. A plot of the current vs. voltage data for both substrates is shown in Figure 6.12.

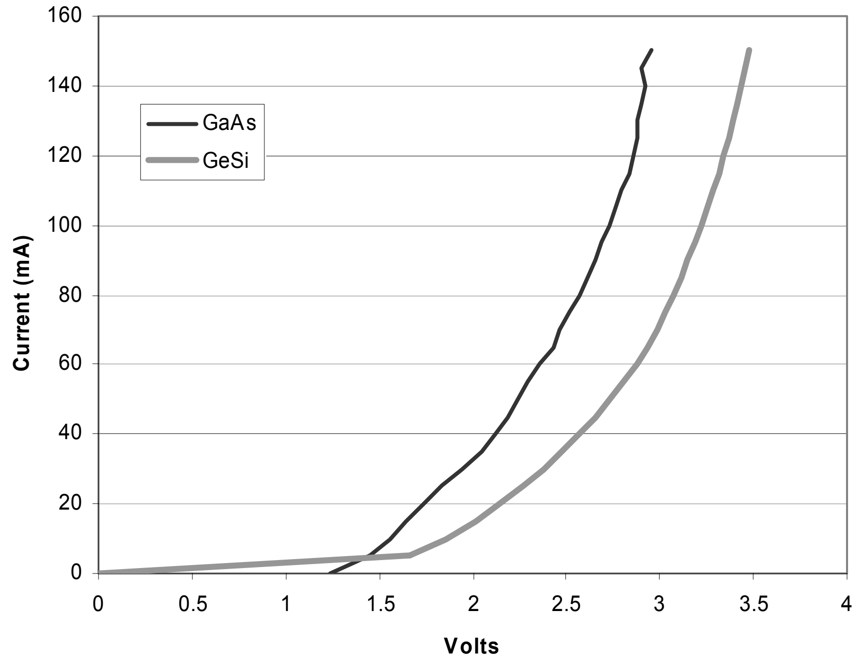

Figure 6.12: Measured current vs. voltage data for the first GaAs/AlGaAs GRIN-SCH top-contact quantum well lasers on Ge/GeSi/Si substrates compared with data for the same device fabricated on a standard GaAs substrate. The first devices on Ge/GeSi/Si show slightly higher turn-on voltages and series resistances.

Measurements were also made of the characteristic temperature for both the integrated lasers on Ge/GeSi/Si substrates and the control devices on GaAs substrates. For temperatures between 15 °C−60°C, the characteristic temperature for the laser on Ge/GeSi/Si was 61 K, while the laser on GaAs showed a characteristic temperature of 128 K.

It is clear from these results that while successful cw laser operation was achieved on Ge/GeSi/Si substrates, significant differences remain between these integrated GaAs/AlGaAs GRIN-SCH quantum well lasers and identical structures fabricated on standard GaAs substrates. Higher turn-on voltages, increased series resistance, reduced characteristic temperatures and lower differential quantum efficiencies in the devices on Ge/GeSi/Si all indicated that further improvement was possible for our first integrated devices. It is likely that many of the observed limits on operating performance in these

first devices sprang from the same root cause, namely higher barriers to current flow in the integrated devices on Ge/GeSi/Si substrates. Higher resistance through these devices would lead to resistive heating and rapid increases in threshold current with increasing external temperature, along with reduced quantum efficiency due to increased internal absorption losses. To understand the factors that may be responsible for the additional resistance in our integrated GaAs/AlGaAs devices on Ge/GeSi/Si, it is helpful to return to the consideration of Ge autodoping effects discussed in Chapter 3. The two-step GaAs nucleation procedure that was used to demonstrate Ge-free GaAs device layers on our Ge/GeSi/Si substrates does not remove Ge incorporation from the initial GaAs passivation layer grown before the reactor and sample cleaning steps. This GaAs nucleation layer, which is grown at a high temperature and a high V/III ratio to encourage a defect-free GaAs/Ge interface, will contain vapor-transported Ge at concentrations exceeding 1×10^{19} cm^{-3}. While this unintentional Ge contamination will have no direct effect on the Ge-free device layers grown above it, it can be expected to have a significant effect on current transport across the GaAs/Ge interface. This is because the high mobility of Ga atoms at the MOCVD growth temperature typically results in a thin diffused layer of electrically active p-type Ga doping in the top of a GaAs-coated n-Ge substrate.[33] When coupled with the high levels of Ge in the adjacent initial layers of the deposited GaAs passivating layer, the intermixed Ge/As boundary will form a reverse *pn*-junction at the interface that will significantly impede carrier transport across the interface.[79] Although exact measurements of the height of the reverse junction energy barrier for a diffused GaAs/Ge diode are difficult to make, it is expected that the insertion of a reverse-biased diode in the laser equivalent circuit will increase the overall turn-on voltage and the series resistance of the device. By fabricating an integrated GaAs/AlGaAs laser structure that avoids direct current injection across the GaAs/Ge interface, it should therefore be possible to observe improved diode performance and better laser characteristics.

To avoid current injection across the GaAs/Ge interface for our integrated GaAs/AlGaAs devices on Ge/GeSi/Si, we chose to adjust the growth and contacting procedure for the n+ GaAs buffer layer below the laser waveguide structure. Beginning with a GaAs-passivated Ge/GeSi/Si substrate, we grew a thick 1 μm n-doped GaAs

buffer layer, above which was grown a GaAs/AlGaAs GRIN-SCH quantum well waveguide structure identical to the previous integrated GaAs/AlGaAs laser on Ge/GeSi/Si. The laser was processed using the top-contact laser recipe as before, except an adjustment was made to the wet etching step that defined the n-contact trenches. The phosphoric acid solution that had been previously used to selectively etch through the GaAs/AlGaAs device layers and stop at the Ge substrate surface was replaced with a 1:8 solution of hydrofluoric acid and water. Hydrofluoric acid etches AlGaAs alloys selectively without etching GaAs. By using this etch chemistry we could adjust the depth of the n-contact trenches so that the ohmic n-contact metal was deposited at the boundary of the lower AlGaAs cladding layer and the thick n+ GaAs buffer instead of at the GaAs/Ge interface. This new contacting scheme reduced the total distance the injected electrons had to travel to reach the GaAs quantum well active layer, but more importantly acted to ensure that no injected carriers had to pass through the interfacial GaAs/Ge reverse junction. A plot of the current-voltage characteristics for these improved GaAs/AlGaAs laser structures compared to earlier devices with the original Ge contact metallization is shown in Figure 6.13.

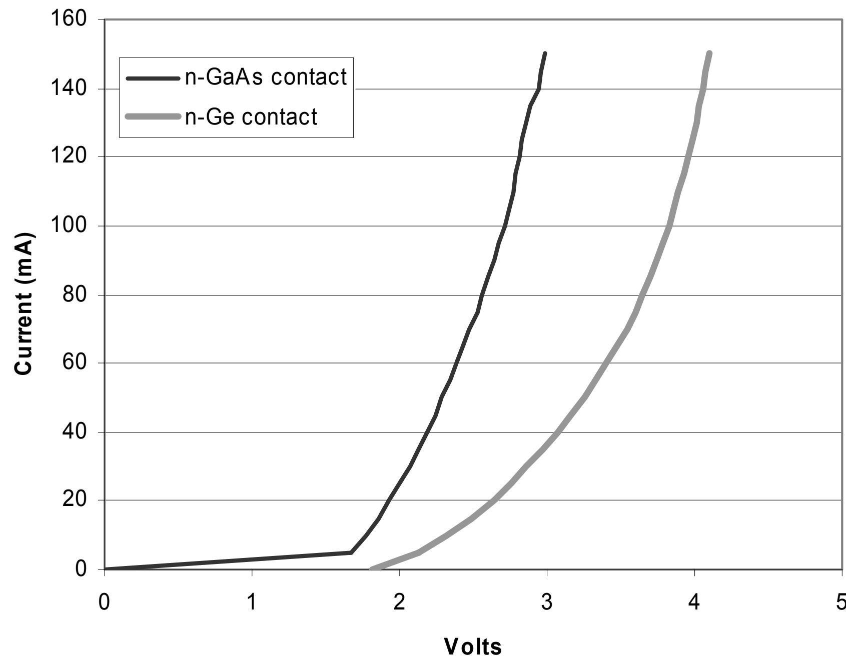

Figure 6.13: Current-voltage characteristics of GaAs/AlGaAs laser diodes integrated on Ge/GeSi/Si substrates with improved contact metallization layers deposited at the AlGaAs/GaAs waveguide interface (labeled "n-GaAs contact") compared with similar structures contacted at the lower GaAs/Ge interface ("n-Ge contact"). The n-GaAs contacted devices turned on earlier and showed lower series resistance at high current levels.

It can be seen from the current-voltage data that the turn-on characteristics of the devices using the new top-contact structure improved dramatically over the original GaAs/Ge contacted devices. By removing the reverse junction energy barrier from the equivalent diode circuit, the improved n-GaAs contact geometry reduced the forward bias voltage needed to reach turn-on. The calculated ideality factor for these devices also improved, from 7.85 in the devices that included the reverse GaAs/Ge diode in the n-contact layer to 3.61 in devices that avoided this layer. Laser performance increased also in the improved contact devices, with laser emission at 853 nm and a threshold current of 67 mA, resulting in a threshold current density of 337 A/cm^2. This compares well to the threshold current density of 577 A/cm^2 measured for the first-generation GaAs/AlGaAs top-contact lasers on Ge/GeSi/Si. The measured differential quantum efficiency was slightly lower than the value for the original integrated devices on Ge/GeSi/Si, with η_d values of 16% compared to the first-generation differential quantum efficiencies of 24%.

Although the improved n-GaAs contact geometry for the second generation of integrated lasers on Ge/GeSi/Si substrates produced some performance improvements, it was clear that room remained for increasing laser performance on these substrates. A third-generation laser with a number of additional design improvements was therefore grown to attempt to match the performance of the original GaAs/AlGaAs laser diodes grown on GaAs substrates. The improved structure began with a CMP-polished Ge/GeSi/Si substrate with reduced surface crosshatch roughness, following the methods detailed in Chapter 5. The average rms roughness of the Ge/GeSi/Si substrate at length scales of 1μm was reduced from 1.4 to 0.3 nm by the CMP polishing step. The laser structure consisted of a 1μm n+ doped GaAs buffer layer, over which was grown a 200 nm-thick smoothly graded $Al_xGa_{(1-x)}As$ cladding structure followed by 1 μm of n-doped $Al_{0.6}Ga_{0.4}As$. The graded $Al_xGa_{(1-x)}As$ structure between the GaAs buffer layer and the $Al_{0.6}Ga_{0.4}As$ cladding layer was added to further reduce the series resistance at the GaAs/AlGaAs heterointerface. A symmetric 200 nm $Al_xGa_{(1-x)}As$ GRIN layer was grown above the cladding layer, followed by a 150 nm $Al_{0.2}Ga_{0.8}As$ SCH surrounding a 90 Å GaAs quantum well active layer. The waveguide structure above the SCH followed a similar plan, with a 200 nm GRIN layer, a 1 μm-thick p-doped $Al_{0.6}Ga_{0.4}As$ cladding and 200 nm graded top layer, with a final 50 nm cap of p+ GaAs. The laser bars were patterned as before, with a top-contact geometry that included the improved n-GaAs contact arrangement above the GaAs/Ge substrate interface.

The third-generation of lasers on our Ge/GeSi/Si substrates showed the best performance yet recorded for GaAs/AlGaAs devices on these substrates. The lasers on Ge/GeSi/Si had an emission wavelength at threshold of 858 nm, and a threshold current of 51 mA, which resulted in a threshold current density of 269 A/cm^2. This threshold density was almost half that of the first-generation GaAs/AlGaAs quantum well lasers on Ge/GeSi/Si, which turned on at a current density of 577 A/cm^2. The differential quantum efficiency of the third-generation devices was also significantly higher than the original integrated devices, with measured η_d values of 40%, compared to the initial device values of 24%. A plot of the optical power vs. current curves for the third-generation lasers on Ge/GeSi/Si substrates is shown in Figure 6.14. The power vs. current data for the first-generation devices on Ge/GeSi/Si and GaAs substrates is shown for comparison. It can

be seen from the graph that the improved devices on Ge/GeSi/Si have performance equal to or even slightly better than the original control lasers grown on GaAs substrates. A similar story is told by the current vs. voltage data, which is presented in Figure 6.15. The improved contact geometry and symmetrically graded $Al_xGa_{(1-x)}As$ cladding layers have contributed to produce current-voltage characteristics in the third-generation devices on Ge/GeSi/Si matching those of the original lasers grown on GaAs substrates. The series resistance for the improved laser diode on Ge/GeSi/Si is 4.0 ohms, almost the same as the device on GaAs, which showed a series resistance of 3.9 ohms, and much better than the first-generation GaAs/AlGaAs laser on Ge/GeSi/Si, which had a series resistance of 6.3 ohms.

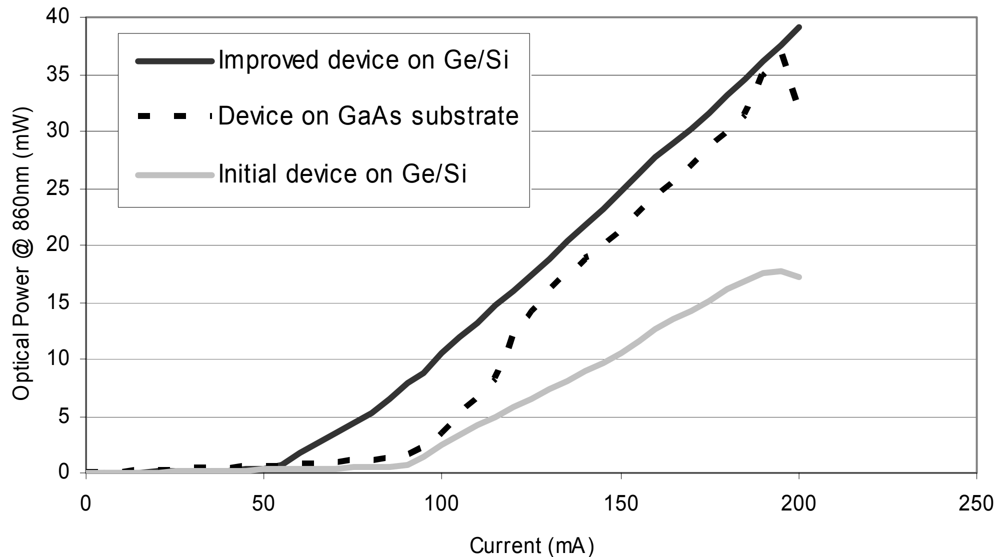

Figure 6.14: Optical power vs. current data for improved GaAs/AlGaAs laser structures grown on CMP-polished Ge/GeSi/Si substrates. The original optical power vs. current data for the first GaAs/AlGaAs lasers on Ge/GeSi/Si and GaAs substrates are included for comparison.

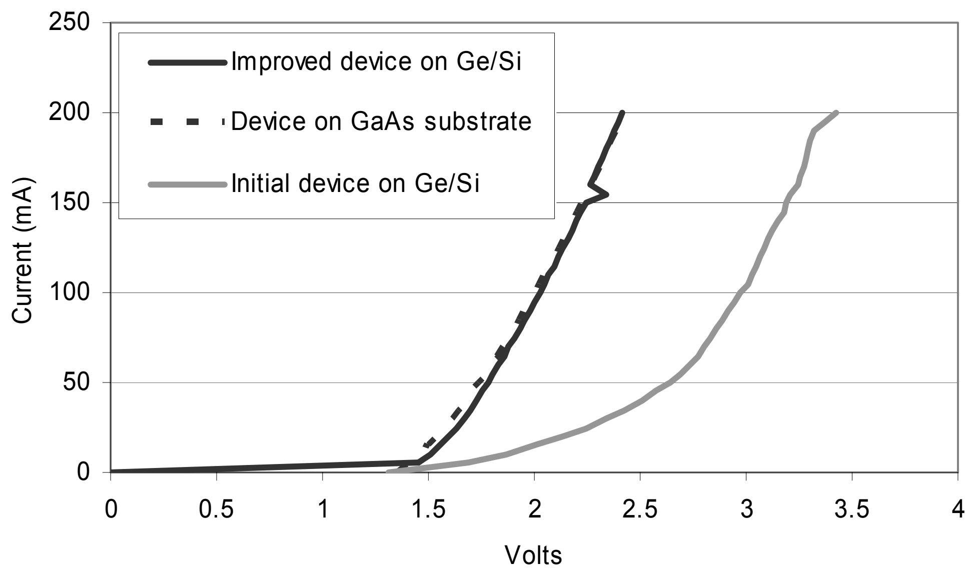

Figure 6.15: Current vs. voltage characteristics of improved GaAs/AlGaAs lasers on Ge/GeSi/Si substrates compared to the current-voltage characteristics of the original GaAs/AlGaAs devices grown on Ge/GeSi/Si and GaAs substrates. Note that the improved devices show identical diode characteristics to the devices grown on GaAs.

Improvements in these new GaAs/AlGaAs laser structures on Ge/GeSi/Si were also observed in the measured characteristic temperatures for laser threshold. The third-generation devices on Ge/GeSi/Si substrates had a calculated T_0 of 129 K, identical to the characteristic temperature of the first GaAs/AlGaAs lasers on GaAs substrates. It is clear from these results that our optimized GaAs/AlGaAs devices integrated on Ge/GeSi/Si substrates have demonstrated performance equivalent in all respects to similar devices grown on GaAs substrates. This achievement is significant considering the many additional materials integration challenges that had to be addressed to achieve successful laser diode integration on the Ge/GeSi/Si materials platform. The achievement of equivalent laser performance on Ge/GeSi/Si and GaAs substrates will be an important step in the integration of commercially useful optoelectronic circuits on Si CMOS substrates.

Significant performance improvements from our original GaAs/AlGaAs quantum well lasers on standard GaAs substrates were achieved by incorporating $In_xGa_{(1-x)}As$ compressively strained quantum well layers into the laser active regions. Our work with

material compression introduced by thermal expansion mismatch, which was described in Chapter 4, convinced us that the effective critical thickness for strained $In_xGa_{(1-x)}As$ layers on Ge/GeSi/Si substrates will be significantly reduced from the expected critical thicknesses of the same layers on GaAs substrates. As explained in Chapter 4, the addition of deliberate compressive strain below the active region of a $In_xGa_{(1-x)}As$/GaAs/AlGaAs quantum well laser structure can act to relax the effective compression of the substrate surface at the growth temperature (through controlled material relaxation in the compressive buffer layers) and recover (theoretically) the critical thickness of a familiar $In_xGa_{(1-x)}As$ strained quantum well layer on a GaAs substrate. The addition of deliberate compressive strain to a GaAs/AlGaAs waveguide structure integrated on Ge/GeSi/Si introduces additional material and device design difficulties however, the most serious of which is the increased tensile strain after cooling to room temperature. This tensile strain can lead to the formation of microcracks in the laser active regions and to difficulties during processing caused by crack multiplication or substrate fracture during the backside removal step (as discussed in Chapter 5). Because it is unclear whether the benefits of a deliberately compressed buffer layer integrated below the laser waveguide on a Ge/GeSi/Si substrate outweigh the inherent drawbacks of this more complicated structure, we chose to focus initially on simpler $In_xGa_{(1-x)}As$ strained quantum well laser designs integrated on Ge/GeSi/Si. By reducing the In concentrations in the quantum wells and growing thinner quantum well layers it was expected that a strained well structure could be grown on Ge/GeSi/Si that remained below the reduced critical thickness for strained $In_xGa_{(1-x)}As$ on this substrate. To test this assumption, we grew and processed a series of $In_xGa_{(1-x)}As$/GaAs/AlGaAs compressively strained quantum well lasers, with thicknesses less than 80Å and In concentrations varying from 15%−20%.

All of the $In_xGa_{(1-x)}As$/GaAs/AlGaAs laser structures tested for this work had similar waveguide structures, with symmetrically graded $Al_{0.6}Ga_{0.4}As$ cladding layers and a 150 nm SCH structure surrounding a single $In_xGa_{(1-x)}As$ quantum well. The devices were processed into top-contact lasers with cavity lengths between 700 and 1000 μm. Cross-section and plan-view TEM micrographs were taken for many of the devices to

check for misfit dislocations in the InGaAs quantum wells. A summary of the laser test results is presented in Table 6.1.

Table 6.1: Summary of results for InGaAs/GaAs/AlGaAs laser structures on Ge/GeSi/Si substrates

Sample	% In in the quantum well	Quantum well thickness	Misfit dislocations in quantum well?	Laser operation?	Differential quantum efficiency
0226mg328	15%	60 Å	Likely	No	0.11%
0224mg327 (CMP substrate)	17%	60 Å	Likely	Yes	28%
0226mg329	19%	50 Å	Yes	No	0.29%
0225mg326	20%	50 Å	Yes	No	0.14%
0229mg331 (bare Si substrate)	18%	50 Å	Yes	No	0.003%

It can be seen from the data presented in the table that only one of the structures with an $In_xGa_{(1-x)}As$ quantum well active region produced cw laser operation. It is significant that this was also the only one of these devices grown on a CMP-polished Ge/GeSi/Si substrate. Almost all of the $In_xGa_{(1-x)}As$ quantum well structures showed evidence of misfit dislocations at the $In_xGa_{(1-x)}As$/GaAs interfaces. The two laser structures with the lowest In concentrations in the active regions were not observed directly with TEM micrographs, but similar structures grown previously on Ge/GeSi/Si substrates showed misfit dislocations in quantum wells with similar thicknesses and In concentrations (although at much lower average misfit spacings than those observed for the $In_xGa_{(1-x)}As$ lasers with higher x_{In} values). It is likely that the misfit dislocations played a role in prohibiting laser operation in the non-CMP-polished $In_xGa_{(1-x)}As$ devices, and it is interesting to note that the best (sub-threshold) quantum efficiencies for these non-lasing devices remained about an order of magnitude below the sub-threshold differential quantum efficiency reported for the early $In_{0.2}Ga_{0.8}As$ quantum well laser fabricated on GaAs (η_d = 1.6 %). The $In_xGa_{(1-x)}As$ quantum well structure that did reach threshold on the Ge/GeSi/Si substrate was the first room-temperature cw InGaAs/GaAs/AlGaAs laser to be demonstrated on this substrate system. The lasing wavelength was 892nm, and the threshold current for a 1000 μm-cavity device was 128 mA (J_{th} = 709 A/cm^2). The differential quantum efficiency was 28%. A plot of the optical power vs. current data for this laser is shown in Figure 6.16.

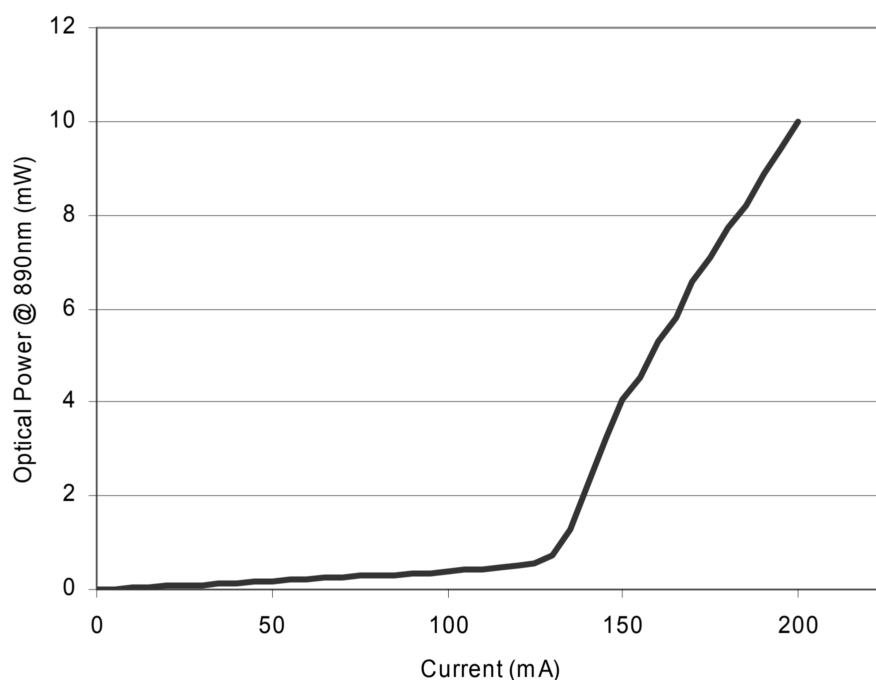

Figure 6.16: Optical power vs. current data for the first InGaAs/GaAs/AlGaAs laser to be demonstrated on a Ge/GeSi/Si substrate. The laser turned on at 128mA.

The demonstrated difficulty of achieving cw laser operation of $In_xGa_{(1-x)}As$ quantum well devices on Ge/GeSi/Si substrates confirms the conclusions made in Chapter 4 that the thermal mismatch between GaAs, Ge, and the Si substrate will complicate the lattice matching necessary for useful strained-layer quantum well integration on Si substrates. The fact that all of these initial $In_xGa_{(1-x)}As$ quantum well structures showed evidence of misfit formation in the quantum well indicates that simple reductions in the In fraction or quantum well thickness may not be sufficient to enable practical strained-layer device integration on Si substrates. It seems more likely that one of the methods discussed in Chapter 4 for forcing misfit dislocation formation below the quantum well active region will be necessary to permit $In_xGa_{(1-x)}As$ quantum well integration on Ge/GeSi/Si. The implications of this conclusion will be discussed in the section covering future work.

6.4.3. Device Lifetime Measurements

As discussed in Chapter 1, demonstrating long lifetime in integrated GaAs-based lasers on Si substrates is a key goal for enabling practical optoelectronic device integration on a Si wafer platform. Laser lifetimes approaching the typical values for device lifetime on standard GaAs substrates (10,000+ hrs) will need to be demonstrated before monolithic heteroepitaxial integration of GaAs/AlGaAs lasers on Ge/GeSi/Si substrates will become practical for commercial applications. Earlier work with GaAs lasers grown directly on Si substrates faced non-radiative threading dislocation densities greater than 10^8 cm^{-2} in the laser active regions and consequently never demonstrated room temperature cw lifetimes longer than 56 hours.[128] The significant reduction in substrate threading dislocation density offered by a relaxed, lattice-matched Ge/GeSi graded buffer layer on a Si substrate offers the potential for significantly improved device lifetimes for lasers that can be successfully integrated on these substrates. To test this expectation, we completed a series of lifetime experiments on the GaAs/AlGaAs and InGaAs/GaAs/AlGaAs lasers demonstrated on our Ge/GeSi/Si substrates to evaluate their operating lifetimes and potential failure mechanisms.

The lifetime characteristics of three different laser structures on Ge/GeSi/Si substrates were measured by mounting several of each device p-side up on a gold-coated copper block held at a temperature of 18 °C by an integrated thermoelectric cooler. A small amount of silicone heat-conducting paste was applied to the back of the mounted laser stripes to provide a degree of thermal conductivity between the cooled laser stage and the backside of the operating devices. As discussed in the experimental section above, it is expected that the active regions of the operating lasers will reach significantly higher temperatures than the surface of the laser stage below them. The lifetime of a GaAs/AlGaAs GRIN-SCH quantum well laser on a standard GaAs substrate was measured to provide a benchmark for the devices on Ge/GeSi/Si substrates. The three laser structures on Ge/GeSi/Si substrates that were tested for this experiment were: a first-generation GaAs/AlGaAs GRIN-SCH quantum well laser structure (including the high-impedance n-Ge top contact geometry), an improved third-generation GaAs/AlGaAs GRIN-SCH quantum well (with improved n-GaAs contacts and a CMP

polished Ge/GeSi/Si substrate), and the $In_{0.17}Ga_{0.83}As$ strained quantum well GRIN-SCH laser that was the only strained-well device to operate on Ge/GeSi/Si.

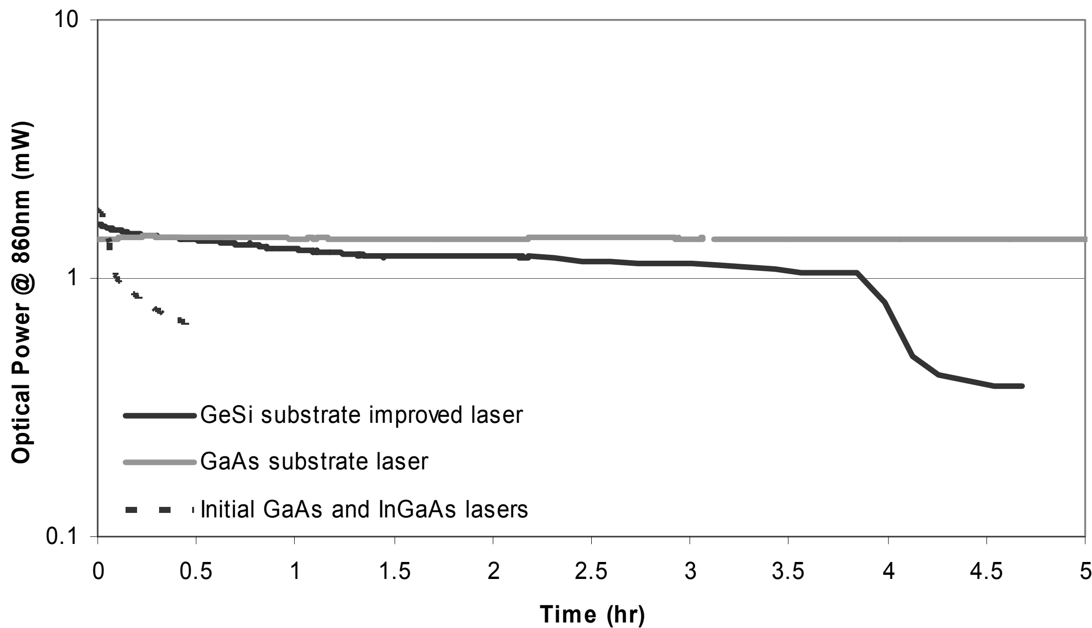

Figure 6.17: Laser power as a function of time at a fixed current for sample lasers on Ge/GeSi/Si and GaAs substrates. The optical power at threshold was slightly less than 1mW/facet for all devices.

A plot of the measured lifetime characteristics for all of the tested laser devices is shown in Figure 6.17. All lasers were operated continuously at a fixed current slightly over threshold, which corresponded to an optical power density of roughly 1mW/facet. When individual lasers failed, the output optical power fell rapidly below threshold, and could not be recovered by turning off the current and turning it back on. It can be seen from the lifetime plot that the GaAs/AlGaAs device on a GaAs substrate showed no evidence of failure behavior at any time scale. The output optical power varied by less than 0.1% over the entire length of the lifetime test, matching earlier observations of GaAs/AlGaAs lasers on GaAs substrates, for which other authors have demonstrated average cw operating lifetimes greater than 8000 hrs.[18] The lasers on Ge/GeSi/Si substrates show much less stable behavior, with both the first-generation GaAs/AlGaAs laser and the $In_{0.17}Ga_{0.83}As$ strained quantum well laser dropping below threshold after less than 10 minutes of continuous operation. The improved third-generation GaAs/AlGaAs quantum well laser on Ge/GeSi/Si showed much better behavior, with a

gradual decrease in optical power followed by a final sharp fall below threshold after almost 4 hours of continuous operation. From the results of this lifetime test it was clear that the improvements in laser threshold current and characteristic temperature demonstrated for the third-generation GaAs/AlGaAs lasers on Ge/GeSi/Si translated into direct improvements in laser operating lifetime. It is likely that the biggest factor underlying this observed improvement in laser lifetime with lower threshold density and threshold temperature sensitivity was the lower resistive heating in the active regions of these devices. Previous work has suggested that the dark-line-defect mechanism in operating lasers is thermally activated and that the propagation velocity of DLD clusters is exponentially dependent on temperature.[89] By lowering the temperature in the active region where dark line defects do the most damage, it is apparent that the improved GaAs/AlGaAs lasers on Ge/GeSi/Si demonstrated dramatically improved lifetimes. For our third-generation devices, a more than 2X reduction in the threshold current density compared to the first-generation devices, along with a twofold increase in the laser characteristic temperature, resulted in a greater than 10X improvement in device lifetime. It is likely that further improvements to the laser threshold parameters would translate into additional dramatic improvements in laser operating lifetime.

Observations of the integrated lasers on Ge/GeSi/Si substrates before and after laser failure indicated that some clues as to the mechanisms driving their failure behavior could be drawn from a more careful study of the electroluminescence patterns of operating laser cavities. Early work with GaAs double-heterostructure lasers integrated directly on Si used microscopic images of the electroluminescence patterns of operating laser cavities to understand the appearance and multiplication of dark spot defects in these short-lived lasers.[126] A similar system was arranged for our lasers, with a Si charge- coupled device (CCD) camera mounted to an optical microscope positioned directly above an operating laser. The camera provided magnified top-down electroluminescence images of the laser cavity during operation and was used to observe changes in the cavity luminescence patterns for all four laser structures during laser lifetime tests. Electroluminescence images taken of the GaAs/AlGaAs lasers on GaAs substrates showed even illumination across the laser cavity, with no visible changes after continuous operation for more than 5 hours. Similar images of the GaAs/AlGaAs

structures on Ge/GeSi/Si substrates showed even cavity illumination across the devices when they were first turned on, but then showed narrow dark lines parallel to the facet mirrors appearing after a few minutes of continuous laser operation. These narrow dark features appeared to be randomly distributed across the cavity and grew gradually wider as the lasers continued to operate. The longest lifetime third-generation GaAs/AlGaAs laser on Ge/GeSi/Si generated narrow dark lines that grew into wide dark bands obscuring more than 50% of the total cavity area after laser failure. Electroluminescence images taken before and after failure of a third-generation GaAs/AlGaAs quantum well laser on Ge/GeSi/Si are shown in Figure 6.18.

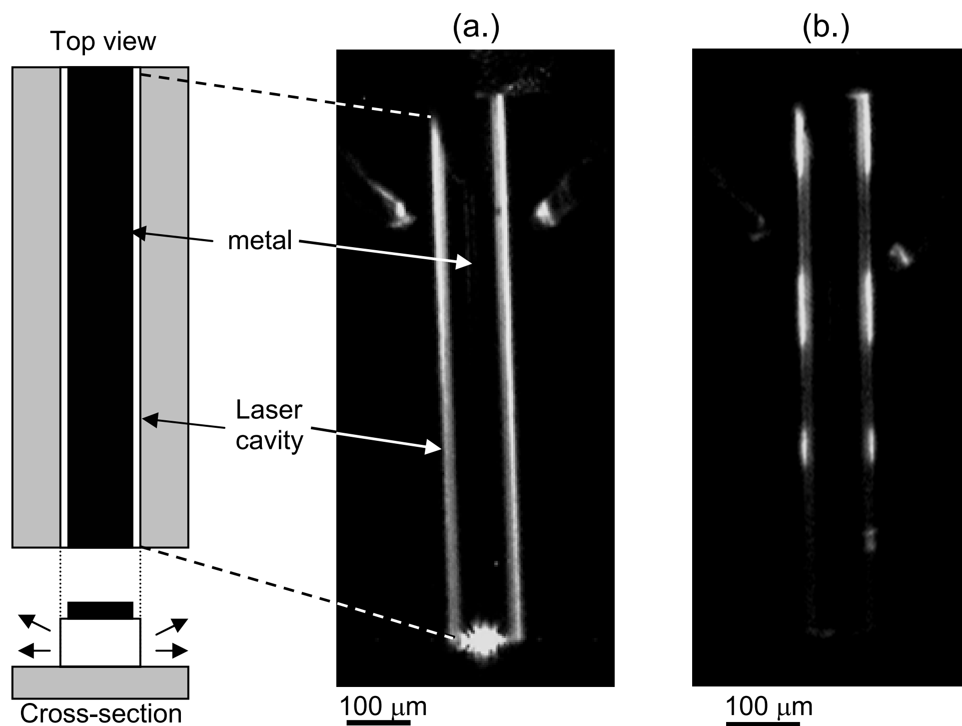

Figure 6.18: Plan-view electroluminescence image of a GaAs/AlGaAs laser on Ge/GeSi/Si (a.) before and (b.) after laser failure. The active region is obscured by the p-metal layer on the top of the device, but the two bright stripes on either side allow observation of the luminescence pattern inside the cavity, and the appearance of wide, dark bands stretching across the laser cavities in image (b.) after laser failure.

It can be seen from the electroluminescence images that all of the dark bands in the laser cavity lie parallel to the cleaved facet mirrors and therefore parallel to the substrate offcut direction. As mentioned in Chapter 5, previous work on strained semiconductor heterostructures has shown that misfit dislocation and tensile microcrack

formation are both favored along the [110] directions parallel to substrate offcut. Optical inspection of the failed lasers showed no evidence of visible microcracks associated with the dark areas in the electroluminescence images, and previous work on GaAs/Si lasers indicates that tensile microcracks are usually apparent even at low magnifications in operational devices.[127] Dark line defects seem to be a more likely cause for the observed banding in the post-failure electroluminescence images, and the fact that all of the observed dark areas are parallel to the substrate offcut direction may simply reflect the lower energy barrier for dislocation glide in this direction. DLDs will appear in electroluminescence (or EBIC) images as rapidly widening dark bands in the active region of the operating laser and will be accompanied by a matching decrease in the laser output efficiency. This is indeed the type of behavior observed in our GaAs/AlGaAs laser diodes on Ge/GeSi/Si substrates, and it appears to point toward dark-line-defect propagation as the root cause for the observed failure behavior for our GaAs/AlGaAs laser diodes integrated on Ge/GeSi/Si substrates.

Previous work has shown that the inclusion of compressively strained $In_xGa_{(1-x)}As$ quantum wells in laser waveguides can dramatically reduce the propagation of existing dark line defects through the active regions of semiconductor laser structures.[18,20] With this fact in mind, it seems surprising that our $In_{0.17}Ga_{0.83}As$ strained quantum well lasers integrated on Ge/GeSi/Si substrates had some of the shortest operating lifetimes observed on these substrates. Examination of the electroluminescence images taken before and after the failure of these devices suggested some possible explanations for this behavior. Electroluminescence images for a 60 Å $In_{0.17}Ga_{0.83}As$ quantum well laser on Ge/GeSi/Si before and after laser failure are shown in Figure 6.19.

Figure 6.19: Electroluminescence pattern of an InGaAs laser cavity on Ge/GeSi/Si (a.) before and (b.) after device failure (average lifetime for these devices was < 10 minutes). A pattern of dark areas at the cavity edges is visible in both images.

It can be seen from the electroluminescence images that even when the $In_{0.17}Ga_{0.83}As$ strained quantum well laser first turned on, it contained an array of dark areas in the active region similar to those observed in the failed GaAs/AlGaAs laser structures. These dark areas did not seem to grow or increase in density in the devices after they failed. The presence of apparent dark line defects in the active regions of these integrated laser structures before they were first turned on may coincide with the probable presence of misfit dislocations in the active regions of these strained quantum well devices. As mentioned above, misfit dislocations were observed via TEM in similar quantum well structures on Ge/GeSi/Si substrates, and misfit dislocations are known to propagate at low dislocation densities primarily along the substrate offcut direction. While misfit dislocations may not by themselves be responsible for the observed failure behavior of our integrated $In_{0.17}Ga_{0.83}As$ quantum well lasers, they may act as extended nucleation sites for other radiatively enhanced defect reaction mechanisms and thereby contribute directly to the observed laser failure behavior. Most of the work with dark line

defect propagation and inhibition in strained layer $In_xGa_{(1-x)}As$ quantum well lasers has focused on <100> dark line defects, which typically propagate by climbing from the edges of the laser cladding layers through the device active layer. Less work has been done to investigate <110> dark line defects, which move much more slowly in operating lasers by gliding sideways along [110] directions from the edges of operating devices.[132] Previous work has suggested that strained $In_xGa_{(1-x)}As$ quantum wells are less effective in prohibiting the propagation of these <110> DLDs in operating lasers,[20] and it is even possible that the top-contact laser process used for this experimental work, which involves an etch through the active regions of the laser stripes to form the n-GaAs contacts, may provide new potential edges for <110> DLD nucleation. If <110> DLD nucleation is a factor for our integrated GaAs/AlGaAs lasers on Ge/GeSi/Si, it may not be inhibited by the presence of an $In_{0.17}Ga_{0.83}As$ strained quantum well in the laser active region, and this fact might then help to explain why these strained layer devices showed no apparent improvement in device lifetime over similar unstrained quantum well lasers.

6.5. Conclusions

This chapter has presented the work done to investigate the integration of optimized GaAs/AlGaAs and InGaAs/GaAs/AlGaAs laser structures on Ge/GeSi/Si substrates. A variety of laser test structures were first demonstrated on standard GaAs substrates; these devices confirmed that edge-emitting lasers with reasonable operating characteristics could be grown in our MOCVD growth reactor. The working laser structures on GaAs served as models for the first successful demonstration of GaAs/AlGaAs quantum well lasers on Ge/GeSi/Si substrates. The initial integrated devices showed threshold current densities and differential slope efficiencies slightly below those of identical devices on GaAs substrates, and further experiments with improved contact geometries, improved cladding layer interfaces, and better Ge/GeSi/Si surface preparation methods enabled the demonstration of dramatically improved third-generation GaAs/AlGaAs lasers integrated on Ge/GeSi/Si substrates. These improved devices showed functionally equivalent performance to similar lasers grown on standard GaAs substrates and represented an important milestone for practical optoelectronic integration on Si substrates. Further work with $In_xGa_{(1-x)}As$ strained quantum well

structures illustrated the lattice and thermal mismatch issues that will complicate attempts to demonstrate practical strained-layer active layers on Ge/GeSi/Si substrates. Despite these integration issues, the first continuous operation of an $In_{0.17}Ga_{0.83}As$ strained quantum well laser on a Ge/GeSi/Si substrate has been demonstrated by making use of a CMP polished Ge/GeSi/Si substrate wafer to reduce the interfacial waveguide scattering losses at the quantum well and SCH interfaces.

Lifetime measurements have been performed on all of the laser structures on Ge/GeSi/Si and show a direct trend of increasing operating lifetime with decreasing threshold current density and increasing characteristic temperature. This trend, coupled with electroluminescence images of the integrated laser cavities before and after device failure have led us to the conclusion that the observed failure behavior in the integrated GaAs/AlGaAs lasers on Ge/GeSi/Si is dominated by thermally activated dark line defect formation. Electroluminescence images of the $In_{0.17}Ga_{0.83}As$ strained quantum well lasers on Ge/GeSi/Si before and after failure have suggested that misfit dislocations in the quantum well play a role in the very rapid failure of these devices, and that <110> dark line defects propagating from the edges of the laser active region may also have a role in the observed failure of all of the GaAs lasers on Ge/GeSi/Si substrates.

Chapter 7. Conclusions

7.1. Summary of Experimental Findings

This work has demonstrated the first compound semiconductor lasers monolithically integrated on Ge/GeSi buffer layers on Si substrates. The demonstration of epitaxially grown GaAs-based lasers on Si has remained one of the key materials integration challenges for practical optoelectronic circuit fabrication on standard Si logic circuits. The work presented in this thesis builds upon extensive earlier optimization of Ge/GeSi graded buffer layers on Si to prove the ultimate flexibility of the GaAs/Ge/Si integration platform for all types of optoelectronic device integration on low-cost Si wafers.

A number of important insights into the challenges of semiconductor laser integration have been developed in the course of demonstrating the first GaAs-based lasers on Ge/GeSi/Si substrates. A study of the proper nucleation conditions for defect-free GaAs film growth on offcut Ge surfaces has shown that high temperatures, high V/III gas flow ratios, and proper pre-growth annealing conditions are necessary to suppress APB and stacking fault defects at the GaAs/Ge interface. Further work has shown that these optimized nucleation conditions lead to vapor phase transport of Ge substrate atoms into growing GaAs/AlGaAs device layers. Vapor-phase Ge autodoping significantly affects the electrical and optical performance of GaAs devices grown on Ge/GeSi/Si substrates. With the proper cleaning procedures to remove Ge sources in the reactor environment, Ge contamination in GaAs/AlGaAs device layers was reduced to undetectable levels, and dramatic improvements in device performance were realized.

The effects of thermal expansion mismatch on the critical thickness of defect-resistant InGaAs strained quantum well structures integrated on Ge/GeSi/Si substrates were shown to effectively prohibit the direct integration of these useful device structures on Ge/GeSi/Si. Theoretical and empirical observations have confirmed the effective reduction in critical thickness for compressively strained InGaAs quantum wells grown above compressive Ge/GeSi graded buffer layers on Si. Thermal mismatch strain has been removed from GaAs films grown on compressive Ge/GeSi graded buffer layers via uniform InAlGaAs buffers placed between the Ge/GeSi and GaAs layers. Increases in overall threading dislocation density introduced by these first InAlGaAs buffers have

been eliminated by replacing them with thin graded InGaAs buffer layers. With the introduction of InGaAs buffer layers on Ge/GeSi/Si substrates, the thermal mismatch strain responsible for misfit dislocations in strained InGaAs quantum wells grown on these substrates has been removed.

Careful evaluation of the rate equations and threshold conditions governing semiconductor laser behavior showed that an optimized device structure for integration on Ge/GeSi/Si substrates consisted of a graded index separate confinement heterostructure surrounding a thin quantum well active region. Increased optical losses on Ge/GeSi/Si substrates due to substrate crosshatch roughness and poor cleaving at mirror facets was accounted for with pre-growth chemical mechanical polishing steps and a perfected cleaving procedure aligned with the substrate offcut direction. These design optimization steps permitted the first continuous, room-temperature demonstration of GaAs/AlGaAs GRIN-SCH quantum well lasers on Ge/GeSi/Si substrates. The first integrated devices showed only slightly worse performance than identical devices grown and fabricated on standard GaAs substrates. Resistive heating in the first-generation integrated lasers was believed to play a significant role in the observed short operating lifetimes and higher threshold current densities. Improved GaAs/AlGaAs lasers on Ge/GeSi/Si with n-GaAs top contacts and CMP-polished substrates showed dramatic improvements in threshold current density, characteristic threshold temperature, and operating lifetimes over the first-generation devices. Electroluminescence imaging has shown that laser failure on Ge/GeSi/Si substrates is associated with the appearance of dark bands in the operating laser cavities parallel to the [110] mirror facets.

Making use of the design improvements demonstrated in the third-generation GaAs/AlGaAs lasers integrated on Ge/GeSi/Si, the first $In_{0.17}Ga_{0.83}As$ strained quantum well laser was then successfully fabricated on a Ge/GeSi/Si substrate. The likely presence of misfit dislocations caused by thermal expansion mismatch in the GaAs/Ge/Si substrate platform restricted the performance and operating lifetime of the first strained-well integrated devices. Dark line defects observed in these lasers via electroluminescence showed similar behavior to those observed in the integrated GaAs/AlGaAs lasers on Ge/GeSi/Si, suggesting the potential activation of a <110> DLD

failure mechanism in these devices that is not impeded by the deliberately strained InGaAs quantum well layer.

Despite the limited operating lifetimes of the first integrated GaAs/AlGaAs and InGaAs/GaAs/AlGaAs lasers on Ge/GeSi/Si substrates, these primitive device structures hold great promise for future improvement. Unlike earlier work with GaAs-based device structures grown directly on Si substrates, which only showed continuous laser operation and quite short operating lifetimes after extensive, decade-long engineering of the laser cavity and mounting structure designs, the designs of the first integrated lasers on Ge/GeSi/Si substrates demonstrated in this work were simple and un-optimized. Minority carrier lifetime measurements and side-by-side comparisons with identical laser structures grown on GaAs substrates both indicate that no fundamental differences exist between the electrical and optical characteristics of GaAs laser structures grown on Ge/GeSi/Si and those grown on standard GaAs substrates. The rapid improvements in laser performance and device lifetime noted for the second and third generation GaAs/AlGaAs lasers on Ge/GeSi/Si, made with only a few simple adjustments to the device fabrication process, indicate that further dramatic improvements in performance will not be long in coming.

7.2. Suggestions for Future Work

A straightforward way to improve laser performance on Ge/GeSi/Si substrates would be to apply some of the laser design improvements developed for devices on GaAs substrates in the last two decades to the integrated structures on Ge/GeSi/Si. Ridge waveguide structures can be used to increase lateral optical confinement and reduce laser threshold. High-reflectivity facet coatings can dramatically decrease mirror losses at the cleaved mirror facets, while a copper heat sink bonded via indium solder to the substrate could significantly reduce self-heating in the laser active region. By reducing threshold current and internal device heating, the thermally-activated recombination reactions that drive dark line defect propagation in the operating lasers will more effectively be suppressed.

It is clear from the electroluminescence data presented for the first failed laser cavities on Ge/GeSi/Si substrates that further research will be needed to understand the exact mechanisms that drive this failure behavior. Plan-view and cross-section TEM of the observed dark regions in failed laser cavities could help to understand the kinds of dislocations involved and how they spread through the failed active regions. With direct TEM analysis of the failed laser active regions it should be possible to determine if <100> or <110> dark line defects are responsible for the dark bands observed in the electroluminescence images. A more comprehensive analysis of laser failure behavior, with statistically significant numbers of tested devices and a variety of different laser structures, could also help to understand the dominant factors governing laser failure on Ge/GeSi/Si substrates.

Work remains to be done in the integration of strained-layer quantum well structures on Ge/GeSi/Si substrates. The work presented in this thesis suggests that while very thin, low-strain wells can be coaxed into laser operation, realistic quantum well compositions and dimensions will require the demonstration of a truly effective method of accommodating the thermal expansion mismatch strain that has limited strained-well integration to this point. The relaxed graded $In_xGa_{(1-x)}As$ buffer structure suggested in Chapter 4 may be one option, although the increased thickness of this buffer layer can also lead to increased microcrack formation, particularly if it cancels the deliberate crack-compensating compressive strain at the growth temperature. Integrated GaAs/Ge/GeSi growth in a single CVD reactor chamber could provide another possible solution to the thermal expansion mismatch between these materials. If a complete InGaAs/GaAs laser structure could be grown in the same growth chamber at the same high growth temperature as the Ge/GeSi graded buffer layer on a Si substrate, it would remove the need for a deliberately compressive Ge cap layer in between the InGaAs/GaAs device layer and the Si substrate. Instead of a deliberately compressive Ge cap layer, the compressive InGaAs active region could provide the necessary balance to the tensile thermal mismatch strain that would develop as the laser structure was cooled. Strained quantum well structures with high indium concentrations could thus be integrated on Si substrates without concern for misfit dislocation formation or microcrack formation in room-temperature devices. Single-chamber growth may introduce other integration

complications however, including increased autodoping effects in GaAs device layers grown immediately after the thick Ge/GeSi graded buffer layers.

The continued optimization of the Ge/GeSi relaxed graded buffer platform on Si would also be expected to yield direct improvements for GaAs laser structures integrated on this proven substrate platform. Continued work to reduce the Ge/GeSi surface threading dislocation density below 10^6 cm^{-2}, as well as new substrate structures involving graded buffer growth in patterned areas, have both been investigated by members of this group. Recent demonstration of thin, low defect density Ge layers directly bonded to Si substrates offers another potentially promising platform for epitaxial GaAs device integration.

With lasers successfully integrated on Ge/GeSi/Si substrates, the next step for demonstrating useful optoelectronic integrated circuits will be to combine an integrated laser structure with other simple integrated devices, such as modulators, waveguides, or photodetectors fabricated in the GaAs/Ge epilayers, or with signal processing or diode driver circuitry fabricated in the Si substrate beneath these layers. A host of integration issues with Si CMOS logic circuitry remain to be addressed, including the thermal budget available for CMOS processing on Si substrates integrated with GaAs/Ge device structures, and the challenge of electrical interconnect fabrication through the thick Ge/GeSi graded buffer structure that separates the substrate from the optically active device layers. Dielectric encapsulation may be necessary for passivation of GaAs/Ge device layers during high-temperature Si CMOS processing, but solid-state diffusion at high temperatures may continue to affect thin quantum well structures and Zn doping profiles in the encapsulated GaAs/AlGaAs device layers.

While many challenges for monolithic III/V optoelectronic integration on Si remain, it is clear that the demonstration of a successfully integrated GaAs-based laser on a Ge/GeSi/Si substrate represents a significant milestone toward the final goal of true integration of high-speed optoelectronic devices with Si CMOS circuits.

References

1 Semiconductor Industry Association, "International Technology Roadmap for Semiconductors." International SEMATECH, (2001).

2 A. K. Stamper, M. B. Fuselier and X. Tian, "Advanced wiring RC delay issues for sub-0.25-micron generation CMOS." Proceedings of the IEEE 1998 International Interconnect Technology Conference, San Francisco, CA, 62 (1998).

3 R. H. Havemann, M. K. Jain, R. S. List, A. R. Ralston, W. Y. Shih, C. Jin, M. C. Chang, E. M. Zielinski, G. A. Dixit, A. Singh, S. W. Russell, J. F. Gaynor, A. J. McKerrow and W. W. Lee, "Overview of process integration issues for low k dielectrics." Proceedings of the MRS: Low-Dielectric Constant Materials IV, San Francisco, CA, **511**, 3 (1998).

4 D.K. Mynbaev and L.L. Scheiner, *Fiber-Optic Communications Technology*. Columbus, OH, Prentice Hall (2001).

5 J.E. Midwinter and Y.L. Guo, *Optoelectronics and Lightwave Technology*. New York, NY, John Wiley & Sons (1992).

6 W. Hunziker, W. Vogt, H. Melchior, P. Buchmann and P. Vettiger, "Passive Self-Aligned Low-Cost Packaging of Semiconductor Laser Arrays on Si Motherboard." IEEE Photonics Technology Letters **7**, 1324 (1995).

7 S.M. Sze, *Physics of Semiconductor Devices*. New York, Wiley-Interscience (1981).

8 E. A. Fitzgerald, "Lattice mismatch and dislocations in InGaAs/GaAs strained heterostructures." *Properties of Lattice Matched and Strained Indium Gallium Arsenide*. Ed. P. Bhattacharya. London, INSPEC. **8:** 6 (1992).

9 J. W. Matthews, S. Mader and T. B. Light, "Accommodation of misfit across the interface between crystals of semiconducting elements or compounds." Journal of Applied Physics **41**, 3800 (1970).

10 B.W. Dodson and J. Y. Tsao, "Relaxation of strained-layer semiconductor structures via plastic flow." Applied Physics Letters **51**, 1325 (1987).

11 R. Hull and J.C. Bean, "Misfit dislocations in lattice-mismatched epitaxial films." Critical Reviews in Solid State and Materials Sciences **17**, 507 (1992).

12 V. Krishnamoorthy, Y. W. Lin, L. Calhoun, H. L. Liu and R. M. Park, "Residual strain analysis of InGaAs/GaAs heteroepitaxial layers." Applied Physics Letters **61**, 2680 (1992).

13 D. J. Dunstan, P. Kidd, P. F. Fewster, N. L. Andrew, R. Grey, J. P. R. David, L. González, Y. González, A. Sacedón and F. González-Sanz, "Plastic relaxation of metamorphic single layer and multilayer InGaAs/GaAs structures." Applied Physics Letters **65**, 839 (1994).

14 E.A. Fitzgerald, S.B. Samavedam, Y.H. Xie and L.M. Giovane, "Influence of strain on semiconductor thin film epitaxy." Journal of Vacuum Science and Technology A **15**, 1048 (1997).

15 M. Yamaguchi and C. Amano, "Efficiency calculations of thin-film GaAs solar cells on Si substrates." Journal of Applied Physics **58**, 3601 (1985).

16 A. Bartels, E. Peiner and A. Schlachetzki, "The effect of dislocations on the transport properties of III/V compound semiconductors on Si." Journal of Applied Physics **78**, 6141 (1995).

17 S.D. Lester, F.A. Ponce, M.G. Craford and D.A. Steigerwald, "High dislocation densities in high-efficiency GaN-based light-emitting diodes." Applied Physics Letters **66**, 1249 (1995).

18 S. H. Yellen, A.H. Shepard, R.J. Dalby, J.A. Baumann, H.B. Serreze, T.S. Guido, R. Soltz, K.J. Bystrom, C.M. Harding and R.G. Waters, "Reliability of GaAs-based semiconductor diode lasers: 0.6-1.1 microns." IEEE Journal of Quantum Electronics **29**, 2058 (1993).

19 G.R. Woolhouse, "Degradation in injection lasers." IEEE J. of Quantum Elec. **QE-11**, 556 (1975).

20 R.G. Waters, "Diode laser degradation mechanisms: a review." Progress in Quantum Electronics **15**, 153 (1991).

21 J.D. Weeks, J.C. Tully and L.C. Kimerling, "Theory of recombination-enhanced defect reactions in semiconductors." Physical Review B **12**, 3286 (1975).

22 R. M. Lum, J. K. Klingert, R. B. Bylsma, A. M. Glass, A. T. Macrander, T. D. Harris and M. G. Lamont, "Effects of misfit dislocations and thermally induced strain on the film properties of heteroepitaxial GaAs on Si." Journal of Applied Physics **64**, 6727 (1988).

23 R.T. Murray, C.J. Kiely and M. Hopkinson, "General characteristics of crack arrays in epilayers grown under tensile strain." Semiconductor Science and Technology **15**, 325 (2000).

24 S.M. Ting, "Monolithic integration of III-V semiconductor materials and devices with silicon," Ph.D, MIT (1999).

25 J. De Boeck, C. Van Hoof, K. Deneffe, R. P. Mertens and G. Borghs, "Relief of thremal stress in heteroepitaxial GaAs on Si by mesa release and deposition." Applied Physics Letters **59**, 1179 (1991).

26 A. Ackaert, L. Buydens, D. Lootens, P. Van Daele and P. Demeester, "Crack formation and thermal stress relaxation of GaAs on Si growth by metal organic vapor phase epitaxy." Applied Physics Letters **55**, 2187 (1989).

27 M. T. Currie, S. B. Samavedam, T. A. Langdo, C. W. Leitz and E. A. Fitzgerald, "Controlling threading dislocation densities in Ge on Si using graded SiGe layers and chemical-mechanical polishing." Applied Physics Letters **72**, 1718 (1998).

28 Y. Li, G. Salviati, M. M. G. Bongers, L. Lazzarini, L. Nasi and L. J. Giling, "On the formation of antiphase domains in the system of GaAs on Ge." Journal of Crystal Growth **163**, 195 (1996).

29 D.B. Holt, "Antiphase boundaries in semiconducting compounds." Journal of Physical Chemistry of Solids **30**, 1297 (1969).

30 P. Modak, M. K. Hudait, S. Hardikar and S. B. Krupanidhi, "OMVPE growth of undoped and Si-doped GaAs epitaxial layers on Ge." Journal of Crystal Growth **193**, 501 (1998).

31 R.M. Sieg, S.A. Ringel, S.M. Ting, S.B. Samavedam, M. Currie, T. Langdo and E.A. Fitzgerald, "Toward device-quality GaAs growth by molecular beam epitaxy on offcut Ge/SiGe/Si substrates." Journal of Vacuum Science and Technology B **16**, 1471 (1998).

32 S. Strite, M.S. Unlu, K. Adomi, G.B. Gao, A. Agarwal, A. Rockett, H. Morkoc, D. Li, Y. Nakamura and N. Otsuka, "GaAs/Ge/GaAs heterostructures by molecular beam epitaxy." Journal of Vacuum Science and Technology B **8**, 1131 (1990).

33 M. K. Hudait, P. Modak, S. Hardikar and S. B. Krupanidhi, "Photoluminescence studies on Si-doped GaAs/Ge." Journal of Applied Physics **83**, 4454 (1998).

34 H. Kasano, "Autodoping Effects of Ge in Vapor-Grown GaAsP layers on the Ge Substrates." Solid State Electronics **16**, 913 (1973).

35 L.C. Bobb, H. Holloway and K.H. Maxwell, "Oriented growth of semiconductors. III. Growth of gallium arsenide on germanium." Journal of Applied Physics **37**, 4687 (1966).

36 D. Hull, *Introduction to Dislocations*. Elmsford, NY, Pergamon Press, Inc. (1981).

37 P. Demeester, A. Ackaert, G. Coudenys, I. Moerman, L. Buydens, I. Pollentier and P. Van Daele, "Relaxed lattice-mismatched growth of III-V semiconductors." Progress in Crystal Growth and Characterization **22**, 53 (1991).

38 H. Kroemer, T.Y. Liu and M. Petroff, "GaAs on Si and related systems: problems and prospects." Journal of Crystal Growth **95**, 96 (1989).

39 M. Akiyama, T. Ueda and S. Onozawa, "MOCVD Growth of GaAs on Si." Materials Research Society Conference, Boston, MA, **116**, 79 (1988).

40 M. Yamaguchi, M. Sugo and Y. Itoh, "Misfit stress dependence of dislocation density reduction in GaAs films on Si substrates grown by strained-layer superlattices." Applied Physics Letters **54**, 2568 (1989).

41 E.A. Fitzgerald, G. Watson, R. Proano, D. Ast, P. Kirchner, G. Pettit and J. Woodall, "Nucleation mechanism and the elimination of misfit dislocations at mismatched interfaces by reduction in growth area." Journal of Applied Physics **65**, 2220 (1989).

42 Z.I. Kazi, P. Thilakan, T. Egawa, M. Umeno and T. Jimbo, "Realization of GaAs/AlGaAs Lasers on Si Substrates Using Epitazial Lateral Overgrowth by Metalorganic Chemical Vapor Deposition." Japanese Journal of Applied Physics **40**, 4903 (2001).

43 K. Eisenbeiser, J. Finder, R. Emrick, S. Rockwell, J. Holmes, R. Droopad, Z. Yu, J. Ramdani, L. Hilt, A. Talin, J. Edwards, W. Ooms, J. Curless, C. Overgaard and M. O'Steen, "RF devices implemented on GaAs on Si substrates using a SrTiO3 buffer layer." IEEE GaAs IC Symposium, Baltimore, MD(2001).

44 C. W. Pei, B. Turk, W. I. Wang and T. S. Kuan, "Mechanism of the reduction of dislocation density in epilayers grown on compliant substrates." Journal of Applied Physics **90**, 5959 (2001).

45 F.E. Ejeckam, C.L. Chua, Z.H. Zhu and Y.H. Lo, "High performance InGaAs photodetectors on Si and GaAs substrates." Applied Physics Letters **67**, 3936 (1995).

46 E.A. Fitzgerald, "GeSi/Si nanostructures." Annual Review of Materials Science **25**, 417 (1995).

47 M.T. Bulsara, "Materials issues with the integration of lattice mismatched InGaAs devices on GaAs," Ph.D, MIT (1998).

48 A.Y. Kim, W.S. McCullough and E.A. Fitzgerald, "Evolution of microstructure and dislocation dynamics in InGaP graded buffers grown on GaP by metalorganic vapor phase epitaxy:

Engineering device-quality substrate materials." Journal of Vacuum Science and Technology B **17**, 1485 (1999).

49 E.A. Fitzgerald, "Dislocations in strained layer epitaxy: theory, experiment, and applications." Materials Science Reports **7**, 87 (1991).

50 J.W.P. Hsu, E.A. Fitzgerald, Y.H. Xie, P.J. Silverman and M.J. Cardillo, "Surface morphology of related GeSi films." Applied Physics Letters **61**, 1293 (1992).

51 K.P. Giannakopoulos and P.J. Goodhew, "Striation development in CBE-grown vicinal plane InGaAs layers." Journal of Crystal Growth **188**, 26 (1998).

52 H. Dumont, L. Auvray, J. Dazord, V. Souliere, Y. Monteil and J. Bouix, "Strain-induced surface morphology of slightly mismatched InGaAs films grown on vicinal (100) InP substrates." Journal of Applied Physics **85**, 7185 (1999).

53 M. T. Currie, "SiGe virtual substrate engineering for integration of III-V materials, microelectromechanical systems, and strained silicon MOSFETs with silicon," Ph.D, MIT (2001).

54 J.A. Carlin, S.A. Ringel, E.A. Fitzgerald, M.T. Bulsara and B. M. Keyes, "Impact of GaAs buffer thickness on electronic quality of GaAs grown on graded Ge/GeSi/Si substrates." Applied Physics Letters **76**, 1884 (2000).

55 S.M. Ting and E.A. Fitzgerald, "Metal-organic chemical vapor deposition of single-domain GaAs on Ge/GeSi/Si and Ge substrates." Journal of Applied Physics **87**, 2618 (2000).

56 V.K. Yang, M.E. Groenert, G. Taraschi, C.W. Leitz, A.J. Pitera, M.T. Currie, Z. Cheng and E.A. Fitzgerald, "Monolithic Integration of III-V Optical Interconnects on Si Using SiGe Virtual Substrates." Journal of Materials Science: Materials in Electronics **13**, 377 (2002).

57 G.B. Stringfellow, "Fundamental aspects of organometallic vapor phase epitaxy." Materials Science and Engineering B **B87**, 97 (2001).

58 G.B. Stringfellow, *Organometallic vapor phase epitaxy: theory and practice*. San Diego, CA, Academic Press, Inc. (1989).

59 C. Pelosi, G. Attolini, C. Bocchi, P. Franzosi, C. Frigeri, M. Berti, A.V. Drigo and F. Romanato, "The role of the V/III ratio in the growth and structural properties of metalorganic vapor phase epitaxy GaAs/Ge heterostructures." Journal of Electronic Materials **24**, 1723 (1995).

60 J.C. Chen, M.L. Ristow, J.I. Cubbage and J.G. Werthen, "GaAs/Ge heterojunction grown by metal-organic chemical vapor deposition and its application to high efficiency photovoltaic devices." Journal of Electronic Materials **21**, 347 (1992).

61 N. Bottka, R.S. Sillmon and W.F. Tseng, "Silicon and beryllium doping of OMVPE grown AlGaAs using silane and diethylberyllium." Journal of Crystal Growth **68**, 54 (1984).

62 K. Kurishima, T. Koayashi, H. Ito and U. Goesele, "Control of Zn diffusion in InP/InGaAs heterojunction bipolar transistor structures grown by metalorganic vapor phase epitaxy." Journal of Applied Physics **79**, 4017 (1996).

63 S. Yu, T.Y. Tan and U. Goesele, "Diffusion mechanism of zinc and beryllium in gallium arsenide." Journal of Applied Physics **69**, 3547 (1991).

64 T.F. Kuech, S. Nayak, J.W. Huang and J. Li, "Chemical and physical effects in oxygen incorporation during the metalorganic vapor phase epitaxial growth of GaAs." Journal of Crystal Growth **163** (1996).

65 Y. Mihashi, M. Miyashita, N. Kaneno, M. Tsugami, N. Fujii, S. Takamiya and S. Mitsui, "Influence of oxygen on the threshold current of AlGaAs multiple quantum well lasers grown by metalorganic chemical vapor deposition." Journal of Crystal Growth **141**, 22 (1994).

66 D.B. Williams and C.B. Carter, *Transmission Electron Microscopy: a textbook for materials science*. New York, NY, Plenum Press (1996).

67 H. Kakinuma, T. Ueda, S. Gotoh and Yamagishi, "Reduction of threading dislocations in GaAs on Si by the use of intermediate GaAs buffer layers prepared under high V-III ratios." Journal of Crystal Growth **205**, 25 (1999).

68 D.K. Bowen and B.K. Tanner, *High Resolution X-ray Diffratometry and Topography*. London, UK, Taylor & Francis (1998).

69 P. van der Sluis, "Determination of strain in epitaxial semiconductor layers by high-resolution x-ray diffraction." Journal of Physics D: Applied Physics **26**, A188 (1993).

70 A.R. Clawson, "Guide to references on III-V semiconductor chemical etching." Materials Science and Engineering **31**, 1 (2001).

71 J. Weyher and J. Van de Ven, "Selective etching and photoetching of {100} gallium arsenide in Cr03-HF aqueous solutions." Journal of Crystal Growth **63**, 285 (1983).

72 K. Akimoto, M. Kamada, K. Taira, M. Arai and N. Watanabe, "Photoluminescence killer center in AlGaAs grown by molecular beam epitaxy." Journal of Applied Physics **59**, 2833 (1986).

73 B.G. Yacobi and D.B. Holt, "Cathodoluminescence scanning electron microscopy of semiconductors." Journal of Applied Physics **59**, R1 (1985).

74 J.E. Griffith and G.P. Kochanski, "The atomic structure of vicinal Si(001) and Ge(001)." Critical Reviews in Solid State and Materials Sciences **16**, 255 (1990).

75 D.J. Chadi, "Stabilities of single-layer and bilayer steps on Si(001) surfaces." Physical Review Letters **59**, 1691 (1987).

76 P.R. Pukite and P.I. Cohen, "Suppression of antiphase domains in the growth of GaAs on Ge(100) by molecular beam epitaxy." Journal of Crystal Growth **81**, 214 (1987).

77 R.D. Bringans, D.K. Biegelsen and L.E. Swartz, "Atomic-step rearrangement on Si(100) by interaction with arsenic and the implication for GaAs-on-Si epitaxy." Physical Review B **44**, 3054 (1991).

78 G. Timo, C. Flores, B. Bollani, D. Passoni, C. Bocchi, P. Franzosi, L. Lazzarini and G. Salviati, "The effect of the growth rate on the low pressure metalorganic vapour phase epitaxy of GaAs/Ge heterostructures." Journal of Crystal Growth **125**, 440 (1992).

79 N. Chand, J. Klem, T. Henderson and H. Morkoc, "Diffusion of As and Ge during growth of GaAs on Ge substrate by molecular beam epitaxy: Its effect on the device electrical characteristics." Journal of Applied Physics **59**, 3601 (1986).

80 H. Kawai, H. Yonezu, H. Yoshida and K. Pak, "Ge segregation and its suppression in GaAs epilayers grown on Ge(111) substrate." Applied Physics Letters **61**, 1216 (1992).

81 H. Jaeger and E. Seipp, "Epitaxial deposition of GaAs and GaAsP on Ge substrates." Journal of Applied Physics **49**, 3317 (1978).

82 G.R. Srinivasan, "Autodoping Effects in Silicon Epitaxy." Journal of the Electrochemical Society **127**, 1334 (1980).

83 J.O. Carlsson, "Thermochemical modelling of interfacial reactions and selective depositon at growth from the vapor." Journal of Vacuum Science and Technology A **6**, 1656 (1988).

84 S.P. Tobin, S.M. Vernon, C. Bajgar, V.E. Haven and S.E. Davis, "MOCVD growth of AlGaAs and GaAs on Ge substrates for high efficiency tandem cell applications." 18th IEEE Photovoltaic Specialists Conference, Las Vegas, Nevada, 134 (1985).

85 R. Azoulay, N. Draidia, Y. Gao, L. Dgrand and G. Leroux, "Autodoping of GaAs grown by organometallic vapor phase epitaxy on silicon substrates." Applied Physics Letters **54**, 2402 (1989).

86 R.W. Balluffi, S.M. Allen and W.C. Carter, *Kinetic Processes in Materials*. New York, NY, John Wiley & Sons (2002).

87 G.W. Neudeck, *The pn Junction Diode*. Reading, MA, Addison-Wesley (1989).

88 H. Wang, A. A. Hopgood and G. I. Ng, "Analysis of dark-line defect growth suppression in InGaAs/GaAs strained heterostructures." Journal of Applied Physics **81**, 3117 (1997).

89 P. M. Petroff, "Physics and materials issues behind the lifetime problem in semiconductor lasers and light emitting diodes." Proceedings of the SPIE: Fabrication, Testing and Reliability of Semiconductor Lasers **2683**, 52 (1996).

90 M. D'Hondt, Z.-Q. Yu, B. Depreter, C. Sys, I. Moerman, P. Demeester and P. Mijlemans, "High quality InGaAs/AlGaAs lasers grown on Ge substrates." Journal of Crystal Growth **195**, 655 (1998).

91 H. P. Singh, "Determination of thermal expansion of germanium, rhodium, and iridium by x-rays." Acta Crystallographa **24A**, 469 (1968).

92 Y. Okada and Y. Tokumaru, "Precise determination of lattice parameter and thermal expansion coefficient of silicon between 300 and 1500K." Journal of Applied Physics **56**, 314 (1984).

93 R. Feder and T. Light, "Precision thermal expansion measurements of semi-insulating GaAs." Journal of Applied Physics **39**, 4870 (1968).

94 B. Roos and F. Ernst, "Thermal-stress-induced dislocations in GeSi/Si heterostructures." Jounral of Crystal Growth **137**, 457 (1994).

95 N. Lucas, H. Zabel, H. Morkoc and H. Unlu, "Anisotropy of thermal expansion of GaAs on Si(001)." Applied Physics Letters **52**, 2117 (1988).

96 K. J. Beernink, P.K. York, J.J. Coleman, R.G. Waters, J. Kim and C.M. Wayman, "Characterization of InGaAs-GaAs strained layer lasers with quantum wells near the critical thickness." Applied Physics Letters **55**, 2167 (1989).

97 J.F. Klem, W.S. Fu, P.L. Gourley, E.D. Jones, T.M. Brennan and J.A. Lott, "Role of substrate threading dislocation density in relaxation of highly strained InGaAs/GaAs quantum well structures." Applied Physics Letters **56**, 1350 (1990).

98 L.A. Coldren and S.W. Corzine, *Diode Lasers and Photonic Integrated Circuits*. New York, NY, John Wiley and Sons, Inc. (1995).

99 B.E. Saleh and M.C. Teich, *Fundementals of Photonics*. New York, NY, John Wiley and Sons, Inc. (1991).

100 H.C. Casey and M.B. Panish, *Heterostructure Lasers*. Boston, MA, Academic Press, Inc. (1978).

101 E. Yablonovitch and E.O. Kane, "Reduction of lasing threshold current density by the lowering of valence band effective mass." Journal of Lightwave Technology **LT-4**, 504 (1986).

102 R.L. Williams, M. Dion, F. Chatenoud and K. Dzurko, "Extremely low threshold current strained InGaAs/AlGaAs lasers by molecular beam epitaxy." Applied Physics Letters **58**, 1816 (1991).

103 D.C. Liu, C.P. Lee, C.M. Tsai, T.F. Lei, J.S. Tsang, W.H. Chiang and Y.K. Tu, "Role of cladding layer thickness on strained-layer InGaAs/GaAs single and multiple quantum well lasers." Journal of Applied Physics **73**, 8027 (1993).

104 V.K. Yang, "Integration of III-V Optical Devices and Interconnects on Si using SiGe Virtual Substrates," Ph.D, MIT (2002).

105 G. Aichmayr, M.D. Martin, H. van der Meulen, C. Pascual, L. Vina, J.M. Calleja, F. Schafer, J.P. Reithmaier and A. Forchel, "Carrier and light trapping in graded quantum-well laser structures." Applied Physics Letters **76**, 3540 (2000).

106 S.R. Chinn, P.S. Zory and A.R. Reisinger, "A model for GRIN-SCH-SQW diode lasers." IEEE J. of Quantum Elec. **24**, 2191 (1988).

107 W.X. Zou, Z.M. Chuang, K.K. Law, N. Dagli, L.A. Coldren and J.L. Merz, "Analysis and optimization of graded-index separate-confinement heterostructure waveguides for quantum well lasers." Journal of Applied Physics **69**, 2857 (1991).

108 I. Kim, B.D. Choe and W.G. Jeong, "An improved approach for the wave equation solution of graded-index waveguide." Journal of Applied Physics **78**, 3514 (1995).

109 F.P. Payne and J.P.R. Lacey, "A theoretical analysis of scattering loss from planar optical waveguides." Optical and Quantum Electronics **26**, 977 (1994).

110 K.K. Lee, D.R. Lim, H.C. Luan, A. Agarwal, J. Foresi and L. Kimerling, "Efect of size and roughness on light transmission in a Si/Si02 waveguide: experiments and model." Applied Physics Letters **77**, 1617 (2000).

111 F. Ladouceur, J.D. Love and T.J. Senden, "Measurement of surface roughness in burried channel waveguides." Electronics Letters **28**, 1011 (1992).

112 A. Pitera. personal communication (2002).

113 H. Hocheng, H.Y. Tsai and Y.T. Su, "Modeling and experimental analysis of the material removal rate in the chemical mechanical planarization of dielectric films and bare silicon wafers." Journal of the Electrochemical Society **148**, G581 (2001).

114 W. Kern, "Chemical etching of silicon, gremanium, gallium arsenide, and gallium phosphide." RCA Review **39**, 278 (1978).

115 S.C. Horst, S. Agarwala, O. King, J.L. Fitz and S.D. Smith, "GaAs/AlGaAs ridge lasers with etched mirrors formed by an inductively coupled plasma reactor." Applied Physics Letters **71**, 1444 (1997).

116 A. Misra and I. Finnie, "On the scribing and subsequent fracturing of silicon semiconductor wafers." Journal of Materials Science **14**, 2567 (1979).

117 T. Cramer, A. Wanner and P. Gumbsch, "Dynamic crack propagation in single-crystalline silicon." Fracture and ductile vs. brittle behavior - theory, modeling, and experiment, Boston, MA, **539**, 181 (1999).

118 C.F. Lin, "The influence of facet roughness on the reflectivities of etched-angled facets for superluminescent diodes and optical amplifiers." IEEE Photonics Technology Letters **4**, 127 (1992).

119 H.K. Choi, C.A. Wang and J.C.C. Fan, "Room-temperature continuous operation of GaAs/AlGaAs lasers grown on Si by organometallic vapor-phase epitaxy." Journal of Applied Physics **68**, 1916 (1990).

120 X. Liu, H.P. Lee and S. Wang, "Double-heterostructure AlGaAs/GaAs lasers grown on the mesas of trenched Si substrate by molecular beam epitaxy." Electronics Letters **26**, 590 (1990).

121 S. Sakai, X.W. Hu and M. Umeno, "AlGaAs/GaAs transverse junction stripe lasers fabricated on Si substrates using superlattice intermediate layers by MOCVD." IEEE J. of Quantum Elec. **QE-23**, 1085 (1987).

122 J.H. Kim, G. Radhakrishnan, A. Nouhi, J.K. Liu, R.J. Lang and J. Katz, "High-power AlGaAs/GaAs DH stripe laser diodes on GaAs-on-Si prepared by migration-enhanced molecular beam epitaxy." Japanese Journal of Applied Physics **28**, 791 (1989).

123 X.W. Liu, A.A. Hopgood, B.F. Usher, H. Wang and N. Braithwaite, "Formation of misfit dislocations during growth of InGaAs/GaAs strained layer heterostructures." Semiconductor Science and Technology **14**, 1154 (1999).

124 R.T. Murray, C.J. Kiely and M. Hopkinson, "Crack interactions in tensile-strained epilayers." Institute of Physics Conference, 169 (1997).

125 C.W. Leitz, "High Mobility Strained Si/SiGe Heterostructure MOSFETs: Channel Engineering and Virtual Substrate Optimization," Ph.D, MIT (2002).

126 T. Egawa, T. Jimbo, Y. Hasegawa and M. Umeno, "Optical and electrical degradations of GaAs-based laser diodes grown on Si substrates." Applied Physics Letters **64**, 1401 (1994).

127 D.G. Deppe, D.C. Hall, N. Holonyak, R.J. Matyi, H. Shichijo and J.E. Epler, "Effects of microcracking on AlGaAs-GaAs quantum well lasers grown on Si." Applied Physics Letters **53**, 874 (1988).

128 H.K. Choi, C.A. Wang and N.H. Karam, "GaAs-based diode lasers on Si with increased lifetime obtained by using strained InGaAs active layer." Applied Physics Letters **59**, 2634 (1991).

129 S. Martini, A.A. Quivy, A. Tabata and J.R. Leite, "Influence of the temperature and excitation power on the optical properties of InGaAs/GaAs quantum wells grown on vicinal GaAs(001) surfaces." Journal of Applied Physics **90**, 2280 (2001).

130 R.M. Sieg, J.A. Carlin, J.J. Boeckl, S.A. Ringel, M.T. Currie, S.M. Ting, T.A. Langdo, G. Taraschi, E.A. Fitzgerald and B.M. Keyes, "High minority-carrier lifetimes in GaAs grown on low-defect-density Ge/GeSi/Si substrates." Applied Physics Letters **73**, 3111 (1998).

131 D.C. Hall, N. Holonyak, D.G. Deppe, M.J. Ries, R.J. Matyi, H. Shichijo and J.E. Epler, "Low-temperature operating life of continuous 300-K AlGaAs-GaAs quantum well heterostructure lasers grown on Si." Journal of Applied Physics **69**, 6844 (1991).

132 O. Ueda, *Reliability and Degradation of III-V Opitical Devices*. Boston, MA, Artech House Publishers (1996).