A Superconducting Bandpass Delta-Sigma Modulator for Direct Analog-to-Digital Conversion of Microwave Radio

by

John Francis Bulzacchelli

B.S. Electrical Engineering
Massachusetts Institute of Technology, 1990

M.S. Electrical Engineering and Computer Science
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Electrical Engineer
Massachusetts Institute of Technology, 1991

Submitted to the Department of Electrical Engineering and Computer Science
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Author ..... John F. Bulzacchelli
Department of Electrical Engineering and Computer Science
March 28, 2003

Certified by ..... Hae-Seung Lee
Professor of Electrical Engineering and Computer Science
Thesis Supervisor

Certified by ..... Mark B. Ketchen
Manager, Design/Technology Integration, IBM Research
Thesis Supervisor

Accepted by .....
Arthur C. Smith
Chairman, Committee on Graduate Students
Department of Electrical Engineering and Computer Science

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Abstract

Direct analog-to-digital conversion of multi-GHz radio frequency (RF) signals is the ultimate goal in software radio receiver design but remains a daunting challenge for any technology. This thesis examines the potential of superconducting technology for realizing RF analog-to-digital converters (ADCs) with improved performance. A bandpass delta-sigma ($\Delta\Sigma$) modulator is an attractive architecture for digitizing narrowband signals with high linearity and a large signal-to-noise ratio (SNR). The design of a superconducting bandpass $\Delta\Sigma$ modulator presented here exploits several advantages of superconducting electronics: the high quality factor of resonators, the high sampling rates of comparators realized with Josephson junctions, natural quantization of voltage pulses, and high circuit sensitivity.

Demonstration of a superconducting circuit operating at clock rates in the tens of GHz is often hindered by the difficulty of high speed interfacing with room-temperature test equipment. In this work, a test chip with integrated acquisition memory is used to simplify high speed testing in a cryogenic environment. The small size (256 bits) of the on-chip memory severely limits the frequency resolution of spectra based on standard fast Fourier transforms. Higher resolution spectra are obtained by "segmented correlation", a new method for testing ADCs. Two different techniques have been found for clocking the superconducting modulator at frequencies in the tens of GHz. In the first approach, an optical clocking technique was developed, in which picosecond laser pulses are delivered via optical fiber to an on-chip metal-semiconductor-metal (MSM) photodiode, whose output current pulses trigger the Josephson circuitry. In the second approach, the superconducting modulator is clocked by an on-chip Josephson oscillator.

These testing methods have been applied in the successful demonstration of a superconducting bandpass $\Delta\Sigma$ modulator fabricated in a niobium integrated circuit process with 1 kA/cm^2 critical current density for the Josephson junctions. At a 42.6 GHz sampling rate, the center frequency of the experimental modulator is 2.23 GHz, the measured SNR is 49 dB over a 20.8 MHz bandwidth, and a full-scale (FS) input is -17.4 dBm. At a 40.2 GHz sampling rate, the measured in-band noise is -57 dBFS over a 19.6 MHz bandwidth.

Thesis Supervisor: Hae-Seung Lee
Title: Professor of Electrical Engineering and Computer Science

Thesis Supervisor: Mark B. Ketchen
Title: Manager, Design/Technology Integration, IBM Research

In memory of Robert V. Bulzacchelli

Acknowledgments

If, in the future, readers of this thesis are impressed by the scope of this project, they should understand that this work was only made possible by the embarrassment of riches I received in support from myriad groups of people. Without their generous assistance, I could never have completed a project which turned out to be far more ambitious than I initially thought. I therefore humbly share my success in this project with them.

First, I want to thank my thesis supervisor at M.I.T., Professor Hae-Seung Lee, who encouraged me to find a thesis topic which would challenge and excite me. His high expectations for me were the biggest reason I joined his research group and remained a constant source of inspiration for me throughout this project. His expert technical guidance and imaginative suggestions were instrumental in making this project a success. I will always appreciate the faith he showed in me, even at times when the technical obstacles seemed insurmountable. He continues to be a great professional role model for me.

Next, I wish to thank my other thesis supervisor, Mark Ketchen, who was my manager during my stay at IBM, where I conducted all of the experiments described in this thesis. Mark's support of this project can only be described as heroic. Even when IBM decided to reduce the size of its effort in superconducting electronics, he made sure that my project would have the necessary resources to continue. Without his support at several key junctures, this project could not have succeeded. In addition to providing the material resources needed to carry out this work, he supplied this project with an optimistic enthusiasm which always lifted my spirits. Mark's extensive experience in Josephson technology also made him an invaluable source of technical information.

Jim Misewich was my mentor at IBM, and most of the experiments described in this thesis were conducted in his laser laboratory. Jim patiently shared with me his knowledge of optics and lasers, which was a wonderful learning experience. He unselfishly donated his time to maintaining the laser systems I was using and helped write laboratory automation software for my experiments. I also enjoyed sharing technical ideas with Jim on all aspects of my project, from the design of the optical clocking setup to the layout of the modulator test chip. Jim was also a great source of conversation on non-technical subjects, including the history of railroads, Lionel trains, classical music, vintage telephones, and classic cars. His friendship made my long hours in the lab a lot more enjoyable.

I am also grateful to Professor Terry Orlando at M.I.T., whose graduate class provided me with a solid foundation in applied superconductivity at the beginning of this project, and who served as a thesis reader at the end. His kind words of encouragement throughout the course of the project are also appreciated.

Sotiris Alexandrou was a post-doc at IBM who worked with me on the design and construction of the optical clocking setup. His expertise in lasers and optics was the perfect complement to my background in electronics, and together we made terrific progress during the nine months he was at IBM. Our passionate but always friendly technical discussions were stimulating and profitable.

I also wish to extend thanks to Merit Hong at Motorola for his collaboration in applying his sinusoidal signal analysis technique to the binary output codes produced by the experimental modulator. The results of his analysis were useful in interpreting the segmented correlation data presented at the end of Chapter 12.

Several people donated Josephson circuit layouts that were incorporated in the design

of various test chips. They are Vasili Semenov and Jao Ching Lin at the State University of New York (SUNY) Stony Brook, and Oleg Mukhanov, Sergey Rylov, Alex Kirichenko, and Steve Kaplan at HYPRES, Inc. I also received helpful technical advice about Josephson technology from Konstantin Likharev at SUNY Stony Brook, and from Alan Kadin and Masoud Radparvar at HYPRES. Alan Kadin also helped review some of the chapters in this thesis. Stas Polonsky gave me an excellent tutorial on using the RSFQ design software developed at SUNY Stony Brook. All of the Josephson circuits discussed in this thesis were fabricated at HYPRES. John Coughlin at HYPRES was very helpful in baking some of the test chips described in Chapter 6 so that the junction critical currents were reduced to an acceptable range.

Many people at the IBM T. J. Watson Research Center assisted me in this project and made my stay there an enjoyable one. Jonathan Sun was a great person to bounce technical ideas off of, and his suggestions for innovative laboratory techniques were often an immense benefit. In addition, he provided me with LabWindows/CVI code which became the starting point for the test system software described in Chapter 11. I also enjoyed his company and conversation over countless dinners. Jim Glownia was always helpful in providing me with optical equipment and technical advice. I also had fun talking to him about vintage radios and stereo equipment, automobiles, and baseball, though as a Yankees fan I'll never understand his sadistic affection for the Red Sox. Jungwook Yang was helpful in letting me run some of my longest circuit simulations on his workstation, and I enjoyed our conversations about analog circuit design. Roger Koch taught me a lot about modeling the noise of Josephson junctions and trustfully loaned me some of his most expensive test instruments. Alan Kleinsasser gave me useful advice about testing Josephson circuits in the early phases of this work. Ray Robertazzi helped me when I was designing the modulator test chip with important tips about designing circuits in the HYPRES process. Several people at IBM were involved in the fabrication of the microstrip circuits used in the optoelectronic sampling experiments of Chapter 4. Kevin Stawiasz helped define the fabrication sequence and was responsible for the overall process flow, Dave McInturff and Manjul Bhushan deposited the oxide dielectrics for the microstrip lines, and Carol Jessen, Dan Lathrop, and John Connolly performed photolithography. I am also grateful to Dan Grischkowsky, who let me work in his laser laboratory during my first year at IBM. Prior to this project, I had never even touched an optical setup, and the members of Dan's group gave me essential lessons on optics and the use of lasers. In particular, Josh Rothenberg taught me how to conduct an optoelectronic sampling experiment with picosecond photoconductors, Nir Katzenellenbogen generously maintained the laser system that I used in the earliest phase of this work, and Hoi Chan provided useful information on test chip preparation. I am also indebted to John Chi, who let me finish the optoelectronic sampling experiments of Chapter 4 in his laser laboratory after Dan Grischkowsky left the company. Finally, I want to thank Bill Gallagher, Jim Rozen, George Keefe, David Abraham, Steve Brown, and Dick Matick, who provided important technical advice on a wide variety of subjects.

During my stay at IBM, I shared a three-person office with several different individuals who helped create a friendly work environment and sometimes gave me a hand in the lab, including Russ Allen, Anelia Delcheva, Meng Ding, Hur Koser, Jin Song, and Li Ji. As my tennis partner, Anelia provided me a welcome diversion from my thesis which gave me much needed exercise and helped clear my mind. Another person who occasionally assisted me in the lab is Jin-Seo Noh, whose friendship and comradery as a fellow graduate student

made late nights at IBM less lonely.

I also received valuable technical information from several other people at M.I.T. during the course of this project. I first learned what a Josephson junction was from Ted Tewksbury, whose M.I.T. area exam was on superconducting ADCs. Our discussions about implementing a delta-sigma modulator in superconducting technology were the seeds from which this thesis project grew. Will Aldrich kindly invited me up to the M.I.T. Haystack Observatory, where he explained how special-purpose correlation hardware is employed in radioastronomy; this information proved helpful in developing my ideas on segmented correlation. Jen Lloyd, Joe Lutsky, and Andy Karanicolas gave me helpful advice on simulating and testing ADCs, and their friendly encouragement helped sustain me during what seemed at times a long ordeal. Jen and Joe also provided me with housing when I came to M.I.T. for several Registration Days, and Andy gave me a place to stay when I visited San Francisco.

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Finally, I come to the two people for whom my gratitude is too deep to be expressed in mere words, my parents. While almost all successful graduate students are indebted to their parents for their love and encouragement, the support I have received from them is unimaginable to anyone who does not know them. They not only provided me love, encouragement, and financial support, but even made direct contributions to this project at critical times. When I was facing an urgent deadline, Dad saved me valuable time by making mechanical drawings from which the IBM machine shop constructed protective housings for the optical clocking setup. More impressively, Dad later learned enough about the Cadence design system to help check all the power supply wiring for the modulator test chip and even did some of the power supply routing himself! When time was critical, Mom prepared dinners for me to take to work so that I would not have to waste time getting food outside IBM. Needless to say, I will forever cherish the love and support they have provided me during this project.

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Biography

John F. Bulzacchelli was born in New York, New York, on September 29, 1966. He attended Edgemont High School in Scarsdale, New York from 1980 to 1984. He entered the Massachusetts Institute of Technology (M.I.T.) in September 1984. As a member of M.I.T.'s VI-A co-op program, he was an internship student at Analog Devices, Wilmington, Massachusetts in the summers of 1986 and 1987, and from June 1988 to January 1990. His research conducted at Analog Devices on new techniques for high speed clock recovery circuits formed the basis of a joint B.S./M.S. thesis entitled *A Delay-Locked Loop for Clock Recovery and Data Synchronization*. He received both the B.S. and M.S. degrees from the Department of Electrical Engineering and Computer Science (EECS) at M.I.T. in June 1990. He received the degree of Electrical Engineer from the EECS department at M.I.T. in February 1991. In the fall of 1990 and the fall of 1991, he was a Teaching Assistant in the EECS department at M.I.T. for the undergraduate class *Solid-State Circuits* and the graduate class *Advanced Circuit Techniques*. From January 1991 to the present, he has been a Research Assistant at the M.I.T. Microsystems Technology Laboratory under the supervision of Professor Hae-Seung Lee. Since June 1992, he has conducted the doctoral research described in this thesis at the IBM T. J. Watson Research Center, Yorktown Heights, New York, in a joint study program between IBM and M.I.T. His present research interests include the design of analog and mixed-mode circuits in conventional and exploratory technologies, optoelectronics, high speed testing methods, and signal processing techniques. He has been a member of Tau Beta Pi and Eta Kappa Nu since 1987, a member of Sigma Xi since 1991, and a member of IEEE since 1992. He received the National Merit Scholarship from 1984-1988, the National Science Foundation Fellowship from 1988-1992, and the IBM Cooperative Fellowship from 1995-1997. His paper describing the design and testing of a superconducting bandpass delta-sigma modulator was recently recognized with the Jack Kilby Award as the Outstanding Student Paper at the 2002 IEEE International Solid-State Circuits Conference.

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Part I

Overview

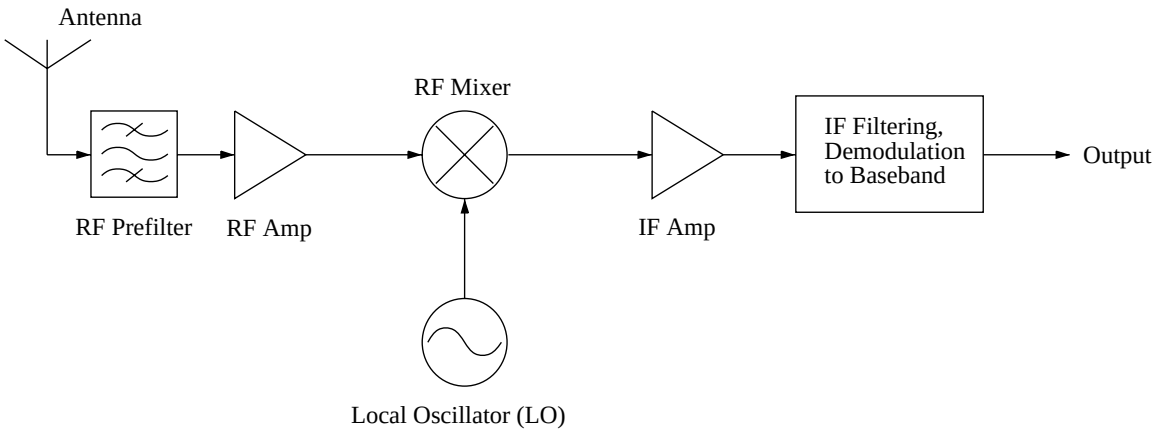
Chapter 1

Introduction

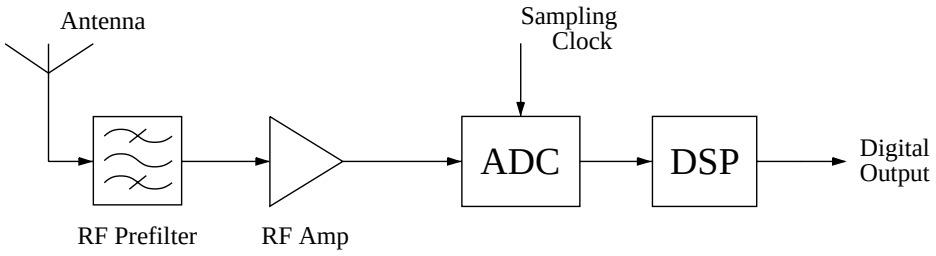
1.1 Motivation

A dominant theme in the evolution of electronic systems over the past few decades has been the increasing use of digital signal processing techniques in applications where analog techniques were once dominant. Digital techniques are now commonly employed in the processing of audio, video, speech, image, geophysical, biomedical, sonar, and radar signals [1]. Driving this shift toward digital implementation is the steady advancement of very large scale integrated (VLSI) technology. Because digital circuits benefit more from technology scaling than do analog ones [2], digital implementations which were once considered prohibitively complex and expensive eventually become not only practical, but even less costly than traditional analog solutions. System performance is fundamentally improved by the use of digital signal processing, which is inherently immune to the noise, distortion, and parameter uncertainties that limit the accuracy and stability of analog signal processing [3]. Another vital advantage of digital signal processing is enhanced flexibility. As best exemplified by the microprocessor of a general-purpose computer, a single piece of digital hardware can be programmed with software to perform a wide range of sophisticated functions. In comparison, analog hardware is usually hard-wired for a given function and has only limited capacity for reconfiguration.

In a touch of irony, one of the last applications to succumb to the onslaught of digital technology is also one of the oldest: radio signal reception. While digital signal processing is often applied to baseband signals and sometimes to intermediate frequency (IF) signals, radio frequency (RF) signals in the GHz range are still processed in the analog domain [4]. The front ends of most radio receivers employ the classic superheterodyne architecture, shown in Figure 1-1(a). A bandpass filter known as the RF prefilter (or preselector) protects the RF amplifier and RF mixer from being overloaded by out-of-band signals and suppresses the spurious response due to the image frequency. The RF mixer translates the amplified RF signal to a lower IF frequency, where the signal is further amplified, filtered, and processed by analog and digital circuitry. While the example shown in the figure uses only one mixer and one IF frequency, modern high performance receivers often employ multiple mixers and IF conversions. After more than 70 years of development, superheterodyne receivers achieve a high level of performance which sets the standard by which all other receiver architectures are judged. On the other hand, the flexibility of these complex analog receivers is limited.



(a)



(b)

Figure 1-1: Radio receiver architectures. (a) Superheterodyne receiver. (b) Software radio receiver.

The selection and arrangement of the analog components in a radio receiver are carefully optimized for a specific frequency band and signal standard. In order to receive a signal with a different standard, the analog signal processing chain must be reconfigured, usually by switching in and out different discrete components. This hardware-intensive approach only allows the reception of a few different signal standards.

The increased system flexibility offered by digital processing of radio signals is a major motivation behind recent research on software radio receivers [5, 6, 7]. As illustrated in Figure 1-1(b), the ultimate goal in software radio receiver design is to digitize directly the RF signal from the antenna with an analog-to-digital converter (ADC). In this architecture, virtually all of the signal processing functions of a radio, such as mixing, channel filtering, equalization, and demodulation, are performed in the digital domain. The power and flexibility of the digital signal processor (DSP) make the system ideal for the simultaneous reception of multiple channels with different signal standards – an important advantage in wireless infrastructure applications such as cellular base stations [6]. Military communication systems also benefit from this ability to handle multiple standards [8, 9]. The programmability of the DSP lengthens the service lifetime of the radio receiver. If a new signal standard is adopted in the future, the functions of the receiver can be redefined with

a download of new software, without requiring costly hardware modifications [10]. Finally, the dramatic simplification of the analog circuitry largely eliminates the need for expensive adjustment procedures during manufacturing and improves system robustness [11].

These benefits are obtained at the cost of demanding performance requirements on the ADC and the DSP. At the present time, neither ADC technology nor DSP technology is adequate for the software radio application [12]. In the long run, the feasibility of software radio systems will likely be limited by ADC technology, as analog circuits improve in performance more slowly than digital circuits. The computing power of digital processors continues to double every 18 months [13], following the exponential growth curve originally predicted by Moore [14]. A comprehensive survey compiled by Walden [15] shows much slower growth in the performance of recent ADCs. At any given sampling rate, the signal-to-noise ratio (SNR) of ADCs has improved by only about 1.5 bits in 8 years. Spurious-free dynamic range (SFDR), a critical specification of ADCs for radio applications [16], has improved by only about 1 bit in 8 years. This slow growth in performance is stimulating interest in alternative architectures and technologies for ADCs. This dissertation examines the potential of superconducting technology for direct analog-to-digital conversion of RF signals in the GHz range.

1.2 ADC Requirements

The high frequency and large dynamic range of RF signals make their direct digitization difficult. Typical carrier frequencies of the RF input are in the low GHz range (e.g., 0.9–3 GHz). Satisfactory reception of weak or badly faded signals in the vicinity of strong interference demands a receiver front end with a high dynamic range. The dynamic range of unfiltered signals from the antenna can be enormous. Interfering signals may be as large as 10 V rms, more than 140 dB larger than the minimum desired signal (< 1 μV rms) [17]. Such a large dynamic range is far beyond the capability of any high frequency ADC demonstrated to date, including the superconducting one discussed in this thesis. In order to reduce the out-of-band interference and relax the dynamic range requirement on the ADC, some RF prefiltering will be required in practical implementations of software radio receivers, as implied in Figure 1-1(b). If the bandwidth of the RF prefilter is too narrow, though, the fundamental advantage of the software radio receiver – its flexibility – will be lost. The prefilter must pass to the ADC *the entire band for which the receiver is designed.* For base station receivers, this means an entire cellular band (covering all subscriber channels), with a bandwidth typically between 12.5 and 60 MHz [18]. Since the RF prefilter passes to the ADC many channels with widely varying signal strength, the dynamic range required of the ADC is still large. For cellular systems based on the Global System for Mobile Communications (GSM) standard, the required dynamic range exceeds 90 dB; for most other standards, the required dynamic range is about 10 dB lower [19].

It is worth pointing out that the SNR of the ADC in a software radio receiver does not have to be as large as the dynamic range of the RF signals that it digitizes. The noise described by the SNR specification of the ADC is spread over a bandwidth much greater than that of a single channel. Therefore, much of the noise can be removed from the desired signal with digital filtering by the DSP. As an example, consider digitizing the 890–915 MHz GSM cellular band with an ideal 8-bit ADC sampling at 4 GHz. The SNR of an ideal 8-bit ADC is only about 50 dB [20]. Provided that the input of the ADC is "busy"

enough[1], the quantization noise has a white spectrum, with power evenly distributed in frequency between dc and half the sampling rate (2 GHz in this example). Applying a digital bandpass filter to the ADC output eliminates most of this out-of-band noise and increases the SNR of the received signal. If the digital filter limits the signal bandwidth to 25 MHz (the width of the entire cellular band), the quantization noise is reduced by $10\log_{10}(2\times10^9/25\times10^6)$=19 dB, and the SNR is increased to 69 dB. If the digital filter limits the signal bandwidth to 200 kHz (the width of a single GSM channel), the SNR is increased further to 90 dB. Thus, the SNR of an ideal 8-bit ADC with a sampling rate of 4 GHz is almost high enough to meet the dynamic range requirement of a GSM system. The SNR improvement achieved by spreading the quantization noise power over a frequency band wider than the band of interest is a well-known benefit of oversampling (sampling the signal at a rate higher than twice its bandwidth). In radio applications, the SNR improvement due to oversampling is often called "processing gain" [21].

On the other hand, oversampling and digital filtering do not reduce the amplitudes of in-band intermodulation (IM) distortion products generated by nonlinearities in the ADC. In order to avoid generating IM distortion products which block the detection of weak signals in the vicinity of strong interferers, the ADC must have very high linearity. The linearity of an ADC used for digitizing radio signals is often characterized in terms of its SFDR, defined as the ratio of total signal power[2] to the power of the largest in-band spurious product in the output spectrum of the ADC [16]. The SFDR of the ADC must be at least comparable to the dynamic range of the RF signals being digitized, with a minimum required value usually between 80–105 dB [12, 22].

In summary, the RF ADC in a software radio receiver must digitize GHz signals with a moderately high SNR (over a bandwidth encompassing all its channels) and an extremely high SFDR. These requirements strongly constrain the choice of architecture for the ADC. Traditionally, flash ADCs with resolutions between 3 and 8 bits have been used to digitize signals above 1 GHz. Because the linearity of a flash ADC is limited by component matching tolerances, its SFDR is not usually much higher than its stated resolution (without oversampling) [15] and is far below that required in a software radio receiver.

Oversampling ADCs known as bandpass delta-sigma ($\Delta\Sigma$) modulators digitize narrowband signals with a high SNR [23]. If single-bit quantization is employed, a bandpass $\Delta\Sigma$ modulator has inherently high linearity, without precise component matching. Bandpass $\Delta\Sigma$ modulators implemented in semiconductor technology are now a popular choice for digitizing IF signals in the MHz range [11, 24, 25], but even in the most advanced technologies, their performance at GHz frequencies is limited by comparator delays and the low quality factor (Q) of integrated inductors. The fastest reported semiconductor bandpass $\Delta\Sigma$ modulator [26], implemented in silicon-germanium (SiGe) technology, digitizes RF signals with a center frequency of 1 GHz at a sampling rate of 4 GHz. For sake of comparison, the center frequency and sampling rate of the superconducting bandpass $\Delta\Sigma$ modulator demonstrated in this project are higher by factors of approximately 2 and 10, respectively. The SNR (49 dB) of the superconducting modulator is limited by the frequency resolution of the measurement but still exceeds the SNR of the SiGe modulator by 3 dB, after accounting for the difference in reported bandwidths (4 MHz for the SiGe circuit versus 20.8 MHz for

[1]The large number of RF signals passed to the ADC in a software radio receiver ensures that the ADC input is busy at all times.

[2]In a multi-tone IM distortion test, the total signal power equals the combined power of all input tones.

the circuit investigated here).

Superconducting technology based on Josephson junctions [27, 28, 29, 30] has several advantages for implementing a bandpass $\Delta\Sigma$ modulator with high performance in this frequency range. The low loss of superconductors allows for resonators with very high values of Q. Very fast comparators can be realized with Josephson junctions, whose fast switching speed allows sampling rates in the tens of GHz. Josephson junctions generate naturally quantized voltage pulses, which can be utilized for effecting fast and precise feedback within the modulator. The high sensitivity of Josephson circuits simplifies the design of the RF amplifier by reducing the required gain in front of the ADC. On the other hand, superconducting technology also has important limitations. Because there are no high gain linear amplifiers analogous to op-amps, it is difficult to implement more complex $\Delta\Sigma$ modulator structures, such as bandpass modulators with more than one resonator inside the feedback loop. The need to maintain cryogenic temperatures limits application of this technology to ground-based systems such as base stations, where installation of a compact cryocooler may be practical [10]. It is worth noting that ground-based systems are the best candidates for early adoption of the software radio architecture since the power dissipation of the DSP may be too high for portable units – at least for the near future [6].

The superconducting bandpass $\Delta\Sigma$ modulator implemented and experimentally demonstrated in this project achieves record-setting performance which represents noteworthy progress toward the goal of direct analog-to-digital conversion of multi-GHz RF signals. Nonetheless, even higher performance is needed to meet the requirements of most software radio systems. According to simulations, the SNR and SFDR of the current modulator design should be improved by at least 15 dB and 20 dB, respectively. The prospects for achieving such improved performance with more advanced modulator designs are examined in the final chapter of the thesis.

1.3 Testing Challenges

The very high operating frequencies (potentially, in the hundreds of GHz [31]) of superconducting circuits make Josephson technology attractive for implementing oversampling ADCs but complicate their testing. Conventional test instruments such as logic analyzers do not presently operate at clock rates in the tens of GHz [32]. Even if faster instrumentation were available, high speed testing of superconducting circuits would be limited by the capacity of the input/output (I/O) interface. The long coaxial cables used to connect the Josephson circuit to room-temperature test equipment have significant loss and dispersion at high frequencies. In the case of the test setup for the superconducting bandpass $\Delta\Sigma$ modulator, the cable bandwidth is only about 2–3 GHz. Such cables are adequate for delivering a 2 GHz microwave input to the modulator, but not for delivering the 20–45 GHz sampling clock, nor for reading out the 20–45 Gbit/s output of the modulator. High speed detection of the output data is further complicated by the small voltage levels (0.1 to 3 mV) produced by most Josephson circuits. The highest rate at which digital data have been transferred from a Josephson circuit to room-temperature electronics is 10 Gbit/s [33], but that demonstration used a standalone interface circuit fabricated in an experimental process with a high critical current density (and therefore low capacitance) for the Josephson junctions. For Josephson circuits fabricated in a conventional process, a readout rate of a few Gbit/s is more typical [34, 35].

These experimental challenges have been overcome in this project not by improving conventional electrical testing methods in an evolutionary manner but by developing new strategies and techniques for high speed testing of multi-GHz circuits. The foremost example of a new testing method is the use of optical clocking to bypass the bandwidth bottleneck of the electrical interface. Optoelectronic techniques have been used in the past to generate electrical signals which are faster than those produced by any other method [36, 37]. In this work, such techniques have been extended in developing a highly versatile optical clocking system, in which picosecond optical pulses are delivered via optical fiber to a superconducting chip, on which an integrated photodiode generates fast electrical pulses with subpicosecond timing accuracy. The system is capable of triggering superconducting circuits with a variety of pulse patterns and repetition rates.

On the other hand, optoelectronic *readout* of superconducting circuits was not investigated in this project. The small electrical signals produced by Josephson circuits are usually inadequate for driving optoelectronic devices such as laser diodes, electro-optic modulators, or magneto-optic modulators. Despite much research [38, 39, 40], an optical output interface for superconducting circuits is not yet practical. Instead of increasing the speed with which data can be read out from the superconducting chip, an alternative strategy was adopted. A popular method [41, 42, 43, 44] of relaxing the bandwidth requirements for readout when testing multi-GHz superconducting circuits is to capture the output data with an on-chip acquisition memory, which can be later uploaded to room-temperature electronics at a relatively low speed (over coaxial cables). The test chip used here to demonstrate the superconducting bandpass $\Delta\Sigma$ modulator includes a 256-bit acquisition memory. The small size of the acquisition memory is set by integration limits of current Josephson technology. Conventional methods of testing $\Delta\Sigma$ modulators require longer record lengths than 256 bits, as the spectral resolution of a 256-point Fast Fourier Transform (FFT) is too low for accurate measurement of ADC performance. This dissertation introduces a new ADC testing method based on "segmented correlation", which yields high resolution estimates of the output spectrum, even when data record lengths are limited by small on-chip memories. While demonstrated here with the superconducting bandpass $\Delta\Sigma$ modulator, the segmented correlation technique is applicable to a wide range of ADCs.

Another example of simplifying high speed testing with suitable on-chip circuitry is clocking of the superconducting bandpass $\Delta\Sigma$ modulator by a Josephson oscillator instead of the optical clock source mentioned above. This use of a Josephson oscillator as an internal clock source for superconducting circuits is a well-known technique [45, 46, 47, 48]. When testing the modulator with the Josephson clock source, the highest frequency signal delivered to or from the superconducting chip is the analog input near 2 GHz.

1.4 Thesis Organization

This thesis is divided into four major parts so that readers can focus on the topics of most interest to them. Part I continues with Chapter 2, which provides background material relevant to this research project. The basic concepts of $\Delta\Sigma$ modulation as a technique for analog-to-digital conversion are reviewed, and a brief tutorial on superconducting electronics is presented. Part II, comprising Chapters 3 through 6, covers the work on optical clocking of superconducting circuits. Chapter 3 is a survey of standard optoelectronic techniques that are used to generate and detect electrical pulses on the picosecond time scale.

The important characteristics of available laser sources and the performance tradeoffs of different photodetectors are discussed. The measurement of picosecond pulses by optoelectronic sampling methods is also explained. Chapter 4 describes optoelectronic sampling experiments that were conducted to study the propagation of picosecond pulses along the superconducting microstrip lines commonly used for signal transfer in Josephson circuits. Particular attention is given to the suppression of transmission line reflections, which become a problem at high clock frequencies. The lessons learned from these optoelectronic sampling experiments guided the design of the optoelectronic interface used in later experiments with Josephson circuits. Chapter 5 presents the optical setup used for multi-GHz clocking of superconducting circuits. The design, operation, alignment, and calibration of this complex but versatile optical system are covered. The triggering of simple Josephson circuits by this optical clocking system is demonstrated in Chapter 6.

Part III, comprising Chapters 7 through 12, is the heart of this thesis and covers the work on the superconducting bandpass $\Delta\Sigma$ modulator. The basic operating principles of the modulator are introduced in Chapter 7. Major design issues are discussed, and modulator output spectra and ADC performance are predicted with a linearized model. At the end of the chapter, the modulator described in this thesis is compared with other superconducting bandpass $\Delta\Sigma$ modulators reported in the literature. Chapter 8 presents the results of detailed circuit simulations of the modulator. Signal-dependent jitter due to delay modulation in the comparator of the modulator is shown to be the main limiting factor in the SNR achieved by the circuit. Chapter 9 explains how the segmented correlation technique can be used to estimate the output spectrum of an ADC with fine frequency resolution when the data record lengths are limited by small acquisition memories. The basic concept of segmented correlation, the accuracy of the spectral estimation, and some practical details of using the technique are discussed. Chapter 10 presents the design of the test chip used to demonstrate the superconducting bandpass $\Delta\Sigma$ modulator. The overall test chip architecture and key implementation details of several circuit blocks are described. Important layout considerations are examined at the end of the chapter. The room-temperature electronics that interface with the modulator test chip are discussed in Chapter 11. The use of current sources with optically-isolated grounds for reducing magnetic coupling to the Josephson circuits is highlighted. The experimental results on the superconducting bandpass $\Delta\Sigma$ modulator are presented and examined in Chapter 12. High speed operation of the modulator is demonstrated with both the optical clock source and the on-chip Josephson clock source. The measured output spectra and SNR of the modulator are shown under different test conditions. The results of segmented correlation measurements are discussed at the end of the chapter. The thesis draws to a close in Part IV, which comprises Chapter 13 and four appendices cited in the text of earlier chapters. Chapter 13 summarizes this work and suggests directions for future progress in this field.

Chapter 2

Background

This chapter briefly reviews the fields of $\Delta\Sigma$ modulation and superconducting electronics at a level necessary for understanding the concepts, analyses, and experiments described in this dissertation. More information on $\Delta\Sigma$ modulation as a technique for analog-to-digital conversion can be found in a textbook [49] and an anthology of classic papers [50] on the subject. Readers desiring a more thorough introduction to superconducting devices and circuits are referred to a few excellent textbooks [27, 28, 29, 30] and to a well-known review article [31] on rapid single flux quantum (RSFQ) logic, the family of Josephson digital circuits employed in this work.

2.1 $\Delta\Sigma$ Modulation

2.1.1 Basic Concept

ADCs which employ noise shaping and oversampling for resolution enhancement are popularly known as $\Delta\Sigma$ (or $\Sigma\Delta$) data converters. The block diagram of a general $\Delta\Sigma$ data converter is presented in Figure 2-1. The data converter consists of two major subsystems: an analog noise shaping feedback loop, called the $\Delta\Sigma$ modulator, and a digital decimation filter (decimator). The $\Delta\Sigma$ modulator samples the analog input at a rate f_s, which is higher than the Nyquist rate f_N by a factor called the oversampling ratio (OSR). According to the Nyquist sampling theorem [1], f_N is equal to twice the bandwidth (Δf) of the analog input signal, so

$$\mathrm{OSR} \equiv \frac{f_s}{f_N} = \frac{f_s}{2\Delta f}. \tag{2.1}$$

Because the input signal is oversampled, its value changes slowly relative to the sampling rate of the $\Delta\Sigma$ modulator. The N-bit ADC produces an N-bit approximation that rapidly oscillates about the input signal. The N-bit digital-to-analog converter (DAC) in the feedback path of the modulator is used to compare this N-bit approximation with the analog input, and the resulting error signal is applied to the analog loop filter in the forward path. In the case of a low-pass $\Delta\Sigma$ modulator used to digitize baseband signals, the analog loop filter contains at least one integrator, which forces the dc error between the analog input and the N-bit approximation to zero. In the frequency domain, the spectral density of the quantization error tends to be small near dc and rises with increasing frequency (hence the

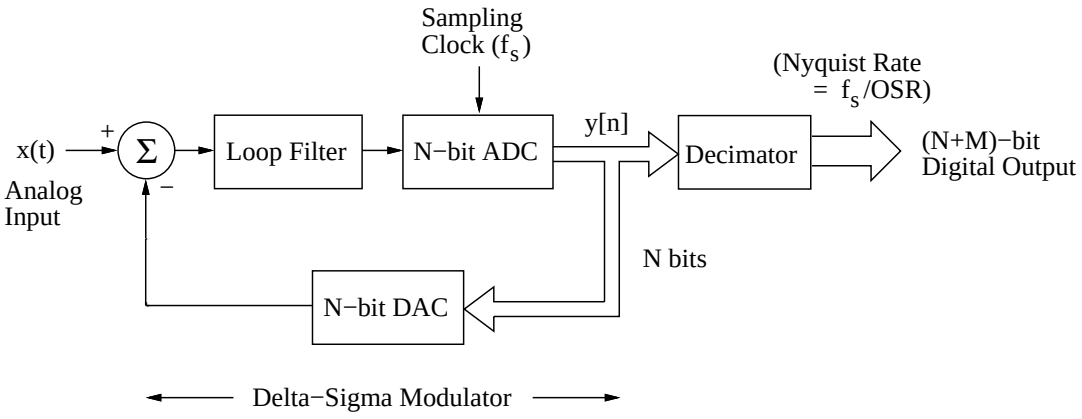


Figure 2-1: General $\Delta\Sigma$ data converter.

term "noise shaping"); the aim is to push the quantization error outside the band of interest, assumed[1] (for now) to be near dc. The decimator then digitally low-pass filters the N-bit approximation, limiting its bandwidth to Δf prior to dropping the sampling rate. The high frequency quantization noise above the band of interest is eliminated in the process[2]. In the time domain, the decimator interpolates between the levels of the N-bit approximation, producing a higher resolution $(N+M)$-bit digital representation of the analog input at the Nyquist rate.

In many practical $\Delta\Sigma$ modulators, the quantizer inside the feedback loop is a simple 1-bit ADC, more commonly known as a comparator. An example of a low-pass $\Delta\Sigma$ modulator with single-bit quantization is illustrated in Figure 2-2. The modulator is first-order because there is only one integrator in its loop filter. The popularity of $\Delta\Sigma$ modulators with single-bit quantization is due to the simplicity of the 1-bit DAC in the feedback path; because a 1-bit DAC is inherently linear (after all, two points define a line), component mismatches in the DAC cause only gain and offset errors, not distortion. If necessary, gain and offset errors can be easily eliminated through calibration. This inherent linearity is particularly valuable for implementing high resolution ADCs in technologies which have relatively poor component matching, such as digital CMOS and Josephson integrated circuits. The superconducting modulator studied and demonstrated in this project employs single-bit quantization.

The analog loop filter of a $\Delta\Sigma$ modulator can be implemented with either discrete-time circuitry, such as switched-capacitor circuits, or continuous-time circuitry, such as active or passive RC circuits. Switched-capacitor circuits are the most popular choice for $\Delta\Sigma$ modulators implemented in CMOS technology. Continuous-time $\Delta\Sigma$ modulators operate at higher sampling rates and provide some implicit anti-alias filtering but are more sensitive to clock jitter and to waveform distortion in the feedback DAC. The superconducting modulator presented here is an example of a continuous-time design.

[1]This assumption is dropped in a later section of the chapter when the operation of bandpass $\Delta\Sigma$ modulators is explained. This introductory discussion focuses on low-pass $\Delta\Sigma$ modulators because their operation is easier to understand intuitively.

[2]It is important to filter the output of the modulator *before* dropping the sampling rate in order to prevent the high frequency quantization noise from aliasing into the baseband.

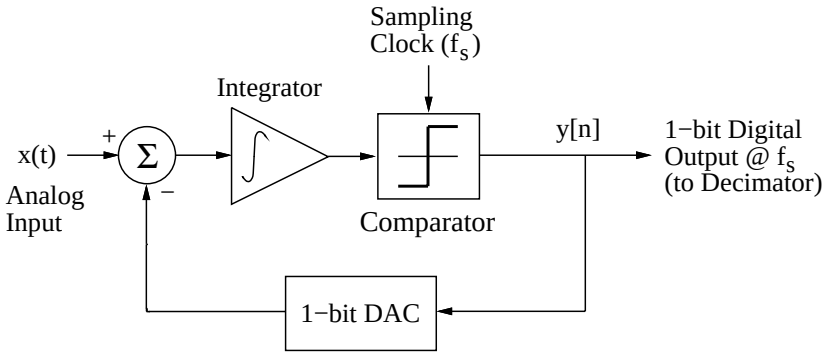


Figure 2-2: First-order low-pass $\Delta\Sigma$ modulator with single-bit quantization.

2.1.2 Linearized Model

Because the quantizer, which is a nonlinear element, is inside the feedback loop, exact analysis of a $\Delta\Sigma$ modulator is often intractable. Faced with this difficulty, most circuit designers have linearized the problem by approximating the quantizer as a source of additive independent white noise with z-transform $E(z)$, as shown in Figure 2-3. $H(z)$ is the transfer function of the loop filter, and K represents the effective gain of the quantizer. For a single-bit quantizer, this gain depends on the joint statistics of its input and output [51, 52] and can be estimated from long computer simulations of the modulator. According to the linearized model of Figure 2-3, the z-transform of the output equals the superposition of the response due to the input and the response due to the source of quantization noise:

$$Y(z) = \mathrm{STF}(z)X(z) + \mathrm{NTF}(z)E(z), \tag{2.2}$$

where the signal transfer function (STF) equals

$$\mathrm{STF}(z) = \frac{KH(z)}{1 + KH(z)}, \tag{2.3}$$

and the noise transfer function (NTF) equals

$$\mathrm{NTF}(z) = \frac{1}{1 + KH(z)}. \tag{2.4}$$

For a low-pass $\Delta\Sigma$ modulator with one or more integrators in the loop filter, $KH(z) \gg 1$ at low frequencies. Therefore, low frequency input signals are passed to the output largely unchanged, while low frequency quantization noise is attenuated by a factor close to $1/KH(z)$. In this way a high SNR in the baseband is obtained. The STF and NTF of a typical low-pass $\Delta\Sigma$ modulator are sketched in Figure 2-4.

The resolution enhancement achieved through noise shaping is well illustrated by the performance of the first-order low-pass $\Delta\Sigma$ modulator shown above in Figure 2-2. Assuming that the quantization error added by the comparator can be modeled as white noise[3],

[3]For a low-order $\Delta\Sigma$ modulator such as the first-order low-pass modulator being discussed here, this white noise assumption is often inaccurate since the quantization error may be highly correlated with the input and may have a periodic structure which appears in the digital output code as "idle tones" [53]. However,

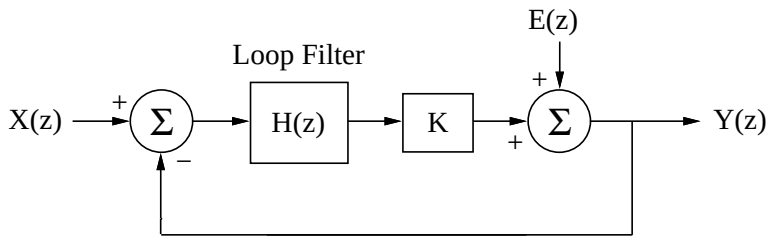


Figure 2-3: Linearized model for $\Delta\Sigma$ modulator loop.

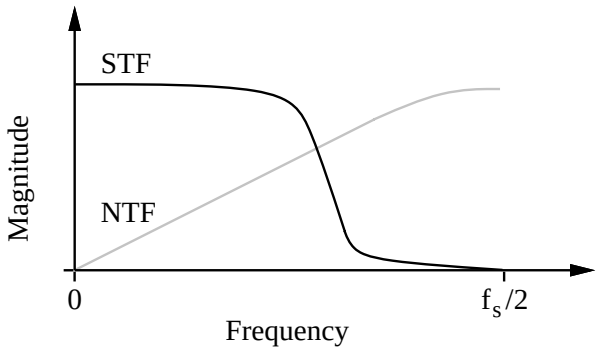


Figure 2-4: Comparison of STF and NTF for a typical low-pass $\Delta\Sigma$ modulator.

and the OSR is large ($\gg 1$), the power spectral density of the quantization noise in the baseband rises quadratically with increasing frequency. The integrated in-band noise power is proportional to the cube of the signal bandwidth Δf, and the peak SNR of the modulator can be expressed (in power) as [20]

$$\text{SNR} = \lambda(\text{OSR})^3, \tag{2.5}$$

where λ is a multiplicative constant typically less than unity. Because of noise shaping, the first-order low-pass $\Delta\Sigma$ modulator gains resolution faster than it trades off speed. For a given sampling rate, a one-octave reduction in signal bandwidth doubles the OSR and improves the SNR by 9 dB, which corresponds to 1.5 bits of resolution. In comparison, doubling the OSR of an ADC that does not employ noise shaping improves the SNR by only 3 dB (0.5 bits) [55]. If many octaves of oversampling are used, the resolution advantage of a $\Delta\Sigma$ data converter over an ADC without noise shaping may amount to several bits.

Higher-order $\Delta\Sigma$ modulators which use loop filters with more than one integrator can achieve even greater SNRs for a given oversampling ratio. Such modulators are not treated in this review, as their implementation is difficult in superconducting technology, which lacks a high gain linear amplifier analogous to a semiconductor op-amp. Without linear amplification, the loop filter in a superconducting $\Delta\Sigma$ modulator is purely passive, and the insertion loss of a higher-order loop filter reduces signal levels to the point where operation of the quantizer (i.e., comparator) becomes unreliable. Researchers developing superconducting second-order low-pass modulators [56, 57, 58, 59] have tried to compensate for

the quantization error in a low-order $\Delta\Sigma$ modulator can be *whitened* with the application of appropriate dither [20, 54], in which case the analysis presented here is reasonably accurate.

the insertion loss of the loop filter by adding power gain to the feedback circuit which implements the 1-bit DAC, but the complexity of such feedback compromises modulator robustness and dramatically reduces the maximum sampling rate, to only 2 GHz for some designs [59]. The reduced sampling rate of such circuits is a major drawback since the SNR of a $\Delta\Sigma$ modulator is a strong function of the OSR.

2.1.3 Bandpass $\Delta\Sigma$ Modulators

Up to this point, the examples used to illustrate the basic concept and analysis of $\Delta\Sigma$ modulation have been low-pass modulators, which were historically the first type developed and are now commonly used in applications such as digital audio. A more recent development has been the invention of bandpass $\Delta\Sigma$ modulation [60, 61, 62], in which the principles of oversampling and noise shaping are applied to digitizing signals with center frequencies much greater than their bandwidths. Such narrowband signals are prevalent in many radio communication systems.

The first-order low-pass $\Delta\Sigma$ modulator of Figure 2-2 can be transformed into a bandpass modulator by replacing the integrator in the forward path with a resonator, as shown in Figure 2-5. The resonant frequency (f_0) is selected to match the center frequency of the analog input signal. The noise shaping of a bandpass modulator can be analyzed with the linearized model presented in the last section. The z-transform of the modulator output is still given by Equations 2.2 through 2.4, but the STF and NTF differ significantly from those of a low-pass modulator because the transfer function $H(z)$ of the loop filter now has a maximum at f_0 instead of at dc. The large loop gain near resonance suppresses quantization noise in the frequency band of the input signal so that a high in-band SNR is obtained. The STF and NTF of a typical bandpass $\Delta\Sigma$ modulator are sketched in Figure 2-6. The large amount of quantization noise outside the band of interest can be removed by a digital bandpass filter in the decimator.

The performance of a bandpass $\Delta\Sigma$ modulator using a single resonator is similar to that of a first-order low-pass modulator. Assuming that the band of interest is defined to lie between the frequencies $f_0 - \Delta f/2$ and $f_0 + \Delta f/2$, the OSR is still given by Equation 2.1, and the peak SNR of the modulator is again given by Equation 2.5. Thus, the SNR improves by 9 dB for each doubling of the OSR. Since the SNR does not depend on the value of f_0, the center frequency of the analog input signal can be a substantial fraction of the sampling

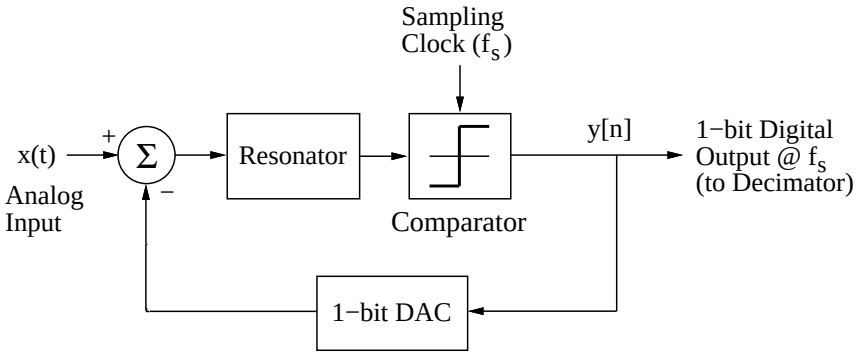


Figure 2-5: Basic bandpass $\Delta\Sigma$ modulator with single-bit quantization.

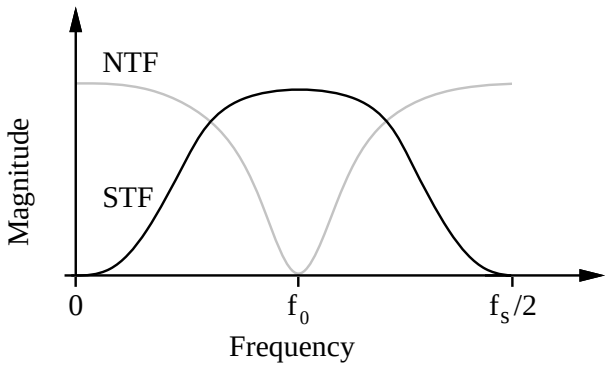


Figure 2-6: Comparison of STF and NTF for a typical bandpass $\Delta\Sigma$ modulator.

rate, often as high as $f_s/4$. Direct analog-to-digital conversion of multi-GHz RF signals can be achieved by implementing a bandpass $\Delta\Sigma$ modulator in a technology that supports sampling rates in the tens of GHz. One such technology is superconducting electronics, on which a brief tutorial is now presented.

2.2 Superconducting Devices and Circuits

2.2.1 Josephson Junction

The basic element of superconducting electronics is the Josephson junction, which consists of two superconducting electrodes separated by a region of weakened superconductivity known as a weak link. In a niobium (Nb) integrated circuit process, which is currently the low temperature superconductor (low-T_c) technology most suitable for implementing Josephson circuits of moderate complexity (such as ADCs), the weak link is a thin layer of insulator, usually aluminum oxide (AlO_X) [63]. Such a structure, shown conceptually in Figure 2-7(a), is called a tunnel junction, as current flows through the junction by tunneling across the insulating barrier. Figure 2-7(b) shows the circuit symbol for a Josephson junction.

Two distinct tunneling mechanisms are responsible for current flow. The tunneling of normal electrons can be modeled as a nonlinear resistive channel, while the tunneling of Cooper pairs (which are the carriers of the lossless currents in superconductors) results in

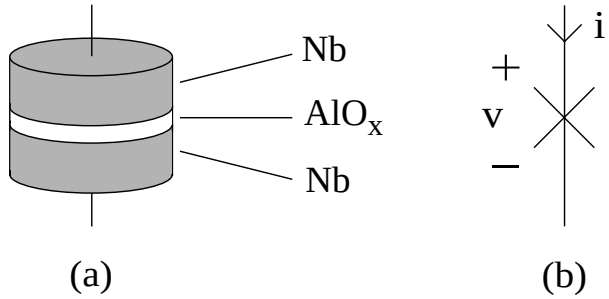


Figure 2-7: Josephson tunnel junction. (a) Physical structure in niobium technology. (b) Circuit symbol.

a Josephson supercurrent described by

$$i_s = I_c \sin\phi, \tag{2.6}$$

where I_c is the critical current of the Josephson junction, and ϕ is the gauge-invariant phase difference of the electron wave function across the junction. The time derivative of the phase difference is proportional to the voltage drop across the junction:

$$\frac{d\phi}{dt} = \frac{2e}{\hbar}v = \frac{2\pi}{\Phi_0}v, \tag{2.7}$$

where the magnetic flux quantum $\Phi_0 \equiv h/2e \approx 2.07 \times 10^{-15}$ Wb. In addition to the two tunneling currents, tunnel junctions have appreciable displacement current since the two electrodes and the insulator form a parallel plate capacitor. Hence, the total current flowing through a Josephson junction can be expressed as the sum of three terms,

$$i = I_c \sin\phi + vG(v) + C\frac{dv}{dt}, \tag{2.8}$$

where $G(v)$ is the nonlinear conductance due to normal tunneling, and C is the junction capacitance. Together, Equations 2.7 and 2.8 form the constitutive relations of the Josephson junction.

A fundamentally important property of the Josephson junction is its ability to pass dc current with zero resistance. For applied currents less than the critical current ($|i| < I_c$), Equations 2.7 and 2.8 allow stationary solutions of the form

$$\phi = \sin^{-1}\left(\frac{i}{I_c}\right), \tag{2.9}$$

$$v = \tfrac{\Phi_0}{2\pi}\tfrac{d\phi}{dt} = 0. \tag{2.10}$$

This effect, known as the *dc Josephson effect*, is especially useful in digital applications, where the persistent currents flowing in superconducting loops of Josephson junctions can represent bits of information.

If the applied current is larger than the critical current, the junction develops a nonzero voltage, the phase difference continually evolves, and the Josephson supercurrent oscillates. This behavior, called the *ac Josephson effect*, is most easily understood by examining the response of a Josephson junction when a dc voltage V_0 is applied. In that case, Equation 2.7 can be directly integrated to give

$$\phi(t) = \phi_0 + \frac{2\pi V_0}{\Phi_0}t, \tag{2.11}$$

so that the supercurrent (Equation 2.6) oscillates sinusoidally:

$$i_s = I_c \sin\left(\frac{2\pi V_0}{\Phi_0}t + \phi_0\right) = I_c \sin(2\pi f_J t + \phi_0). \tag{2.12}$$

The Josephson frequency f_J is directly proportional to the dc voltage on the junction:

$$f_J = \frac{V_0}{\Phi_0} \approx 483.6 \times 10^{12} V_0 \quad \text{(in Hz)}. \tag{2.13}$$

This Josephson voltage-frequency relation has been shown to hold to better than 2 parts in 10^{16}, independent of weak link structure or materials [64].

Further insight into the dynamics of Josephson junctions can be gained by simplifying the junction model. In the resistively shunted junction (RSJ) model, shown in Figure 2-8, the nonlinear conductance due to normal tunneling is treated as a linear resistance R. Replacing $G(v)$ with $1/R$ in Equation 2.8, and using the voltage-phase relation of Equation 2.7, one obtains the following expression relating the total junction current to the phase difference ϕ and its time derivatives:

$$i = I_c \sin\phi + \frac{\Phi_0}{2\pi R}\frac{d\phi}{dt} + \frac{\Phi_0 C}{2\pi}\frac{d^2\phi}{dt^2}. \tag{2.14}$$

While still nonlinear, this equation is a familiar one from elementary mechanics, for it describes the motion of a driven pendulum. A study of this mechanical analog provides rich insight into the dynamics of many circuits using Josephson junctions [65].

Consider a pendulum of mass m and length l driven by an external torque I. The applied torque balances the gravitational torque and the forces of drag and inertia:

$$I = mgl\sin\phi + D\frac{d\phi}{dt} + M\frac{d^2\phi}{dt^2}, \tag{2.15}$$

where D is the damping constant, M the moment of inertia, and ϕ the angular displacement of the pendulum from rest. A comparison of Equations 2.14 and 2.15 shows that the pendulum is an exact analog of the RSJ model of the Josephson junction. The applied torque corresponds to the applied junction current, and the angular velocity to the voltage across the junction. The damping and rotational inertia model the effects of the resistive and capacitive channels, respectively. The moment arm of the pendulum, mgl, can be considered the "critical torque" since a pendulum initially at rest will start rotating only if the applied torque exceeds mgl. For applied torques less than mgl, the gravitational torque balances the externally applied torque, and the pendulum remains stationary – corresponding to the superconducting state of the Josephson junction.

Once the pendulum has been set in motion by an applied torque larger than mgl, its inertia tends to keep it rotating even when the applied torque is reduced. If the pendulum is very lightly damped, the minimum torque needed to maintain rotation is much less than mgl. In an underdamped Josephson junction, the analogous behavior is observed in a hysteretic dc current-voltage characteristic, as shown in Figure 2-9(a). Once the junction has been switched into the voltage state by an applied current above the critical current,

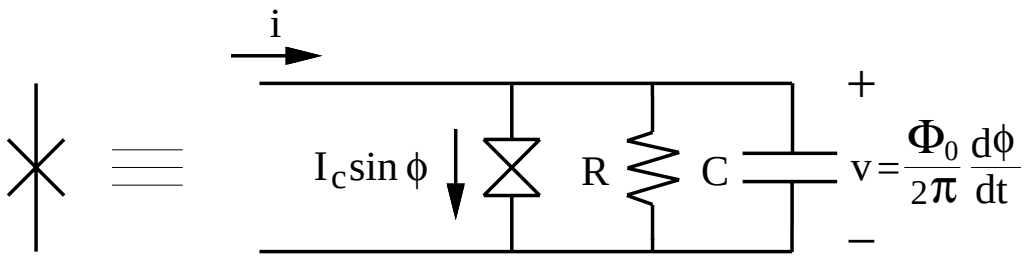


Figure 2-8: Resistively shunted junction (RSJ) model.

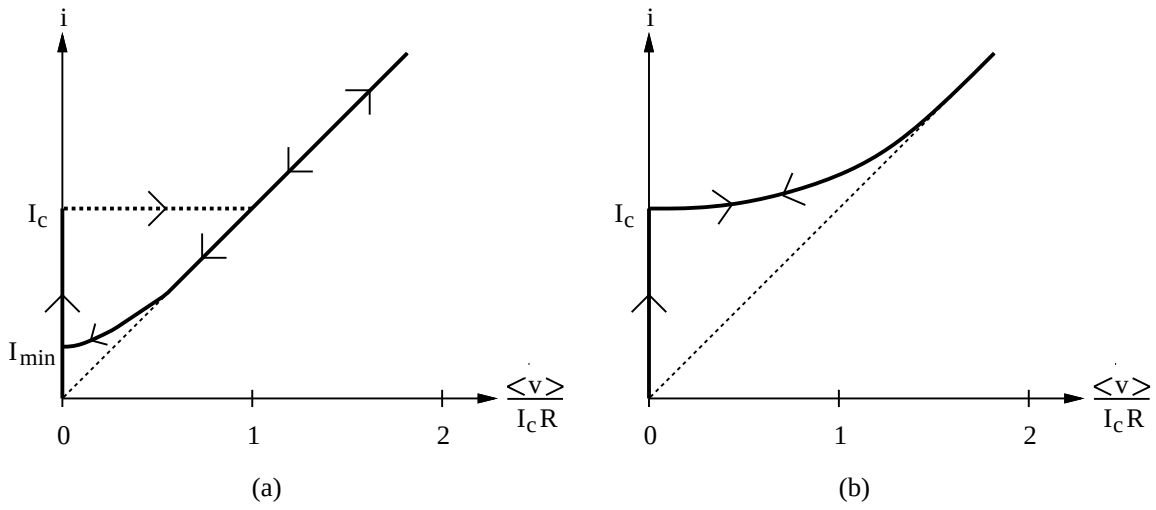


Figure 2-9: Current i versus dc voltage $\langle v(t) \rangle$ characteristic for (a) underdamped junction ($\beta_c \gg 1$) and (b) overdamped junction ($\beta_c \ll 1$).

the current must be decreased to a value I_{min} well below I_c in order to reset the junction to its superconducting state. On the other hand, if the pendulum is heavily damped, inertial effects are negligible, and the pendulum stops rotating as soon as the applied torque is reduced below mgl. Correspondingly, the dc current-voltage characteristic of a heavily overdamped Josephson junction, shown in Figure 2-9(b), is not hysteretic. The degree of damping in a Josephson junction is characterized by the Stewart-McCumber parameter β_c, given by

$$\beta_c = \frac{2\pi I_c R^2 C}{\Phi_0}. \tag{2.16}$$

The boundary between overdamped and underdamped behavior is usually taken to be $\beta_c = 1$. For $\beta_c > 1$, the junction is considered underdamped and exhibits appreciable hysteresis. For $\beta_c < 1$, the junction is considered overdamped and exhibits little or no hysteresis.

All of the superconducting circuits discussed in this dissertation require that the Josephson junctions be overdamped. Because resetting an underdamped junction to the superconducting state by reducing the bias current below I_{min} is a relatively slow process (on the Josephson junction time scale), circuits which use junctions in a hysteretic, or "latching", mode have maximum clock frequencies on the order of 1 GHz [31]. In contrast, circuits which use overdamped junctions in a nonhysteretic mode offer clock speeds which are orders of magnitude higher. Present-day niobium integrated circuit technology produces tunnel junctions which are naturally underdamped because of the substantial capacitance inherent to the device structure. In the circuits to be discussed, the junctions are made nonhysteretic by shunting them with an external resistor, which lowers the effective value of R in Equation 2.16. Typically, the shunt resistance is selected so that β_c is near unity. Because the conductance of the linear shunt resistor usually dominates the nonlinear conductance due to normal tunneling, the RSJ model is a good approximation in circuits employing overdamped junctions. Since every circuit discussed in this dissertation is based upon over-

damped junctions, the external shunt resistors are not explicitly shown in circuit schematics, *but their existence is always assumed.*

The pendulum analogy is also useful for visualizing single flux quantum events. Consider an overdamped Josephson junction biased at a current near but below its critical current. In the mechanical analog, this corresponds to a pendulum raised by an externally applied torque to an angle ϕ just below the critical angle of $\pi/2$. If now a short kick is delivered to the pendulum that drives it past the critical angle, the pendulum will flip over the top. Since the pendulum is overdamped, the pendulum will come to a stop after one full revolution. Analogously, an impulse of current of the right magnitude will trigger a 2π change in the junction phase. By the Josephson voltage-phase relation, a 2π leap in phase is accompanied by the generation of a voltage pulse across the junction with area

$$\int_{\phi=\phi_0}^{\phi=\phi_0+2\pi} v(t)dt = \frac{\Phi_0}{2\pi}\int_{\phi=\phi_0}^{\phi=\phi_0+2\pi} \frac{d\phi}{dt}dt = \Phi_0, \tag{2.17}$$

so that a 2π leap in junction phase corresponds to a single flux quantum (SFQ) event. The notion of an SFQ event is an important one in SFQ logic circuits, which process, transfer, and store binary information as SFQ pulses; these circuits are covered later in the chapter. Equation 2.17 shows that the area of an SFQ pulse is defined by quantum mechanics and is independent of junction parameters such as critical current, resistance, or capacitance[4]. The natural quantization of the SFQ pulse is exploited in the design of many superconducting ADCs [10, 56, 58, 66, 67, 68], including the bandpass $\Delta\Sigma$ modulator described in this thesis.

2.2.2 Superconducting Quantum Interference

When one or more Josephson junctions are connected in a superconducting loop, a superconducting quantum interference device (SQUID) is formed. Since SQUIDs are the basic building blocks of many superconducting circuits, knowledge of their basic operation facilitates the understanding of more complex circuits. Because the entire loop in a SQUID is superconducting, the current flowing through the loop may be described in terms of a macroscopic electron wave function possessing both magnitude and phase. Single-valuedness of the wave function dictates that the change in phase around the SQUID loop be an integral multiple of 2π, a requirement which can be expressed as the quantum-phase relation

$$\sum_i \phi_i + 2\pi\sum_j \frac{\Phi_j}{\Phi_0} = 2\pi n, \tag{2.18}$$

where ϕ_i is the gauge-invariant phase difference across the ith junction in the loop, Φ_j is the flux in the jth inductor in the loop, and n is an integer. By applying the quantum-phase relation of Equation 2.18, Kirchhoff's current law (KCL), and the constitutive relations of the Josephson junction, the circuit response of any SQUID can be calculated[5].

[4]These junction parameters affect the height, width, and shape of an SFQ pulse, but not its area.

[5]Experienced circuit designers may be wondering what happened to Kirchhoff's voltage law (KVL). KVL is still valid! Since the time derivative of the junction phase is proportional to the junction voltage (Equation 2.7), and the inductor voltage equals the time rate of change of flux, KVL can be derived for the superconducting loop by differentiating Equation 2.18 with respect to time. However, Equation 2.18 is a stronger statement than just an integral form of KVL since the constant of integration is restricted to integral multiples of 2π.

Because the junction phases are coupled by the superconducting loop, macroscopic interference effects occur in multi-junction devices. The most famous example of this is the critical current modulation of a double-junction (DJ) SQUID, which consists of two Josephson junctions connected in a superconducting loop, as shown in Figure 2-10. Assuming that the junctions are in the superconducting state, the resistive and capacitive components of the junction currents can be neglected, and the total current through the DJ SQUID is the sum of the two Josephson supercurrents,

$$i = i_1 + i_2 = I_c \sin\phi_1 + I_c \sin\phi_2. \tag{2.19}$$

For simplicity, the junctions are assumed to have identical critical currents. The relation between the junction phases ϕ_1 and ϕ_2 is found by applying Equation 2.18 to the DJ SQUID loop, which yields

$$\phi_1 - \phi_2 + 2\pi\frac{\Phi}{\Phi_0} = 2\pi n, \tag{2.20}$$

where Φ is the total magnetic flux penetrating the superconducting loop. The negative sign in front of ϕ_2 merely reflects the opposite directions around the loop defined for i_1 and i_2. The total flux penetrating the loop is the sum of the externally applied flux Φ_{ext} and the flux generated by the circulating current flowing in the loop:

$$\Phi = \Phi_{ext} + Li_{circ}, \tag{2.21}$$

where

$$i_{circ} = \frac{1}{2}(i_1 - i_2). \tag{2.22}$$

The critical current of the SQUID, defined to be the largest dc current that can flow through the SQUID with zero resistance, can be determined by maximizing Equation 2.19 under the constraints given by Equations 2.20–2.22. The critical current of a DJ SQUID with $LI_c = \Phi_0/2$ is plotted as a function of Φ_{ext} in the threshold curve of Figure 2-11. Each lobe of the threshold curve is known as a "mode boundary" and corresponds to a different value of n in Equation 2.20.

When no external flux is applied, the difference in junction phases $\phi_1 - \phi_2 = 0$, and

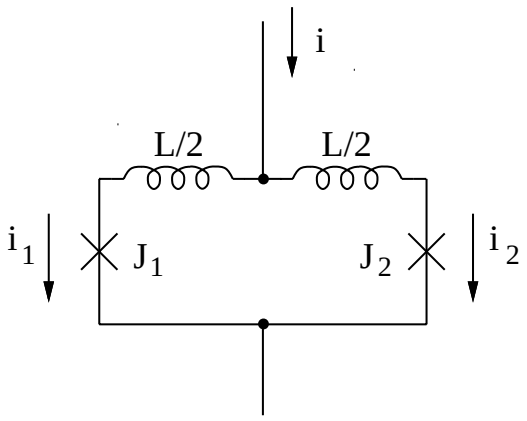


Figure 2-10: Double-junction (DJ) SQUID.

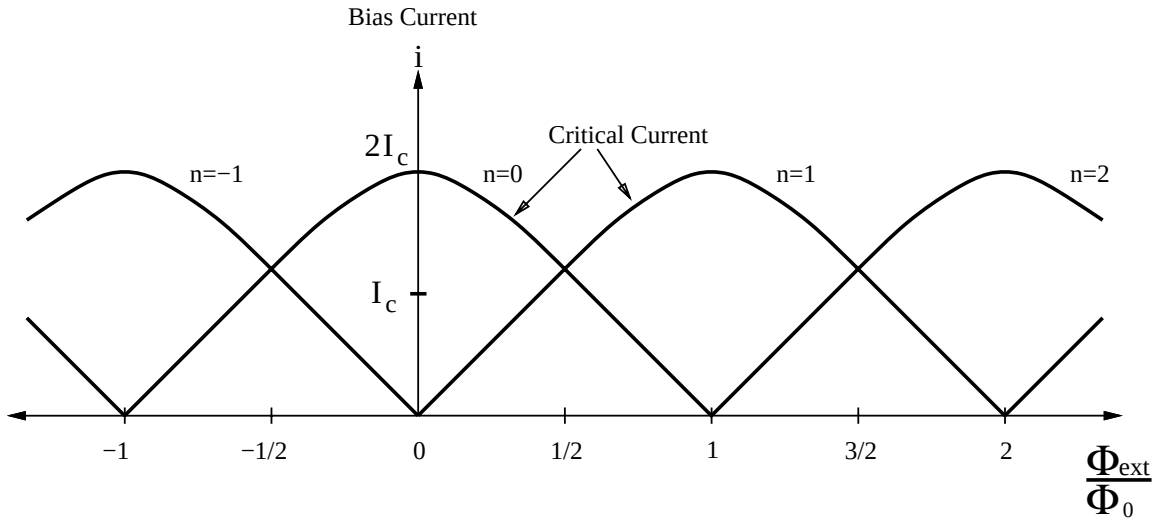


Figure 2-11: Threshold curve for a DJ SQUID with $LI_c = \Phi_0/2$.

the maximum current that can flow through the SQUID is $2I_c$, with each junction carrying its critical current. As the applied flux Φ_{ext} increases, circulating currents form in the loop which produce an opposing flux. As the circulating current i_{circ} increases, less of the junctions' supercurrent is available to carry the bias current, and the critical current of the SQUID decreases, as illustrated by the $n = 0$ mode boundary of Figure 2-11. Other values of n permit additional solutions. For instance, when $n = 1$ and $\Phi_{ext} = \Phi_0$, the junction phases ϕ_1 and ϕ_2 are equal, and the maximum current that can flow through the SQUID is $2I_c$. Because of these other solutions, the threshold curve is periodic in the applied flux, with a period equal to the magnetic flux quantum Φ_0.

When used as part of an SFQ logic circuit, a SQUID is biased at a low enough current that its junctions never enter the voltage state, except on a transient basis when the SQUID loop switches between different states, each of which corresponds to a different mode boundary in the threshold curve. As an example, consider driving the DJ SQUID of Figure 2-10 along the operating points indicated in Figure 2-12. The bias current of the SQUID is fixed at $I_c/2$, while the external flux is increased from zero to Φ_0 and then decreased back to zero. Initially, the applied flux is zero, and the bias current divides equally between the two junctions of the SQUID. As the external flux is increased, a clockwise circulating current develops, which decreases i_1 and increases i_2. The circulating current keeps increasing until, at point 3 in the figure, i_2 equals I_c, and the $n = 0$ mode becomes unstable. Assuming that the junctions are overdamped, the circuit switches from the $n = 0$ mode to the $n = 1$ mode with an SFQ voltage pulse generated across junction J_2, and the circulating current reverses direction. (In the $n = 1$ mode, the circulating current attempts to maintain the total flux in the loop at one flux quantum; therefore, after the SQUID switches at point 3, the circulating current enhances the applied flux instead of opposing it.) As Φ_{ext} is increased further to point 4, the junction currents return to their original values, with the bias current equally divided. If now the applied flux is decreased, a counterclockwise circulating current develops, which increases i_1 and decreases i_2. At point 2 in the figure, i_1 equals I_c, and the $n = 1$ mode becomes unstable. The circuit switches back into the $n = 0$ mode with an SFQ voltage pulse generated across junction J_1, and the circulating current again reverses

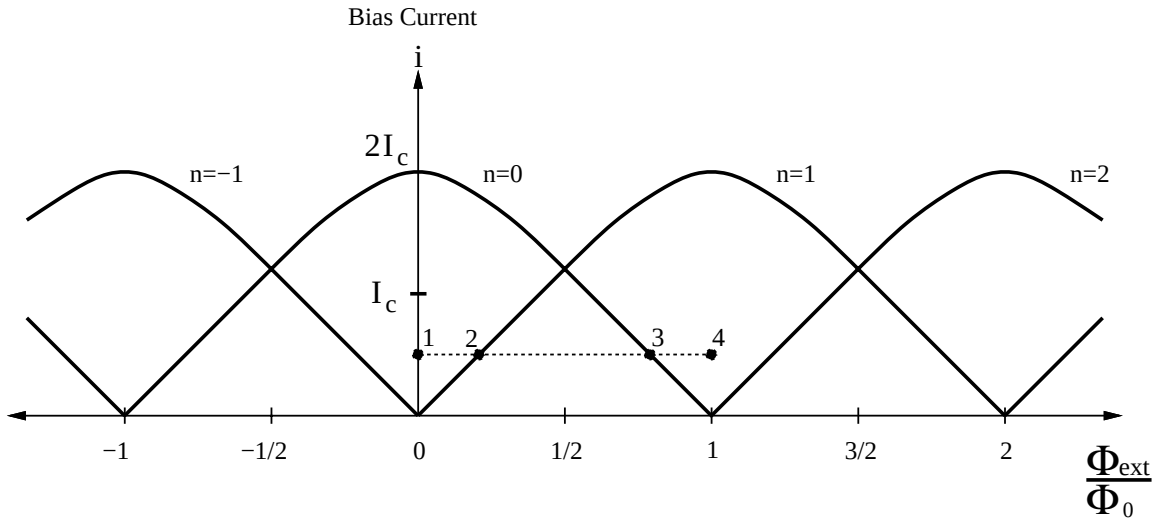


Figure 2-12: Operating points along the threshold curve of a DJ SQUID with $LI_c = \Phi_0/2$ as Φ_{ext} is varied between 0 and Φ_0 at a bias current $i = I_c/2$.

direction. In summary, every time an increase in the external flux crosses the right-hand side of a mode boundary, an SFQ voltage pulse is generated across junction J_2; every time a decrease in the external flux crosses the left-hand side of a mode boundary, an SFQ voltage pulse is generated across junction J_1.

The switching of a SQUID between different dc operating modes can also be viewed in terms of magnetic flux quanta entering and leaving the loop through its Josephson junctions. In the case of the previous example, when junction J_2 switches to produce an SFQ voltage pulse, one flux quantum (Φ_0) of magnetic field passes through J_2 and enters the SQUID loop, where it is stored as a circulating current. When junction J_1 later switches to produce an SFQ voltage pulse, this flux quantum of magnetic field leaves the SQUID loop through J_1, and the circuit returns to its original state.

This use of Josephson junction switching to regulate the flow of magnetic flux quanta into and out of SQUID loops is the basis behind SFQ logic circuits. The most successful SFQ logic family shown to date is known as rapid single flux quantum (RSFQ) logic, originally proposed by Likharev, Mukhanov, and Semenov [69]. All of the superconducting digital circuits employed in this work belong to this logic family, the basic operation of which is now illustrated with a set of circuit examples.

2.2.3 Josephson Transmission Line

The representation of binary information as SFQ voltage pulses with quantized area has important consequences for the design of RSFQ logic circuits. The role of interconnect inductance is critical. If one logic gate generates an SFQ output pulse, the current delivered to the input of the next gate equals Φ_0/L, where L is the inductance of the wiring between the two logic gates[6]. If L is too large, this current will be too small to switch a Josephson

[6]Technically, the inductance L also includes contributions from the small nonlinear inductances of the Josephson junctions in the circuit. Such details are not important to the present discussion.

junction reliably, and logical errors will occur. Thus, RSFQ circuits are not tolerant of excessive interconnect inductance between logic gates, *even if high speed operation is not required*. (In contrast, traditional semiconductor logic circuits such as static CMOS are adversely affected by excessive capacitance only at high operating frequencies.) In order to avoid problems with excessive inductance, logic gates which are more than about 50–100 μm apart are usually connected together not with long wires but with active circuits known as Josephson transmission lines (JTLs).

Figure 2-13 shows the schematic of a two-stage JTL. (The number of stages equals the number of junctions in the JTL.) Current sources I_{b1} and I_{b2} are used to bias junctions J_1 and J_2 close to their critical currents (e.g., at $0.75I_c$). When an SFQ pulse arrives at the input, it increases the current through inductor L_1 so that J_1 is momentarily driven above its critical current and switches. The SFQ pulse generated across J_1 reduces the current through L_1 back toward its original value and increases the current through inductor L_2 so that J_2 is momentarily driven above its critical current. When J_2 switches, an SFQ pulse appears on the output of the JTL. The inductances in a JTL are small enough (typically, $\leq \Phi_0/2I_c$) that no magnetic flux quanta can be trapped between any of its stages. Therefore, a JTL acts as an SFQ pulse "repeater", transferring each input pulse to the output after a short propagation delay. Because the SFQ pulse is actively regenerated by each junction in the circuit, JTLs with a large number of stages can be used to transfer SFQ pulses between logic gates which are physically far apart.

JTLs have other valuable uses in RSFQ logic circuits as well. Circuits based on two-terminal devices such as Josephson junctions offer relatively limited isolation, and undesirable interactions between different logic gates may hinder their proper operation. Inserting a couple of JTL stages between logic gates reduces the strength of such interactions and often improves the operating margins of the circuit. The use of JTLs as standardized loads for RSFQ logic gates also saves design time by reducing the need to modify circuit cells for specific load conditions. A JTL can provide current gain (and therefore power gain) if the junction critical currents are scaled upward in the direction of pulse propagation. A common guideline used in designing such an "amplifying JTL" is to increase the critical currents by a factor of $\sqrt{2}$ per stage [31]. The current gain of an amplifying JTL allows it to drive a load with a low impedance.

On the other hand, the use of active JTL circuits for signal transmission has some significant drawbacks. In present-day niobium integrated circuit technology (with 1 kA/cm^2 critical current density for the Josephson junctions), each stage of JTL adds about 4-8 ps of delay, depending on load conditions and the current gain required of the JTL. Even a short JTL with only a few stages has a propagation delay comparable to that of a typical RSFQ

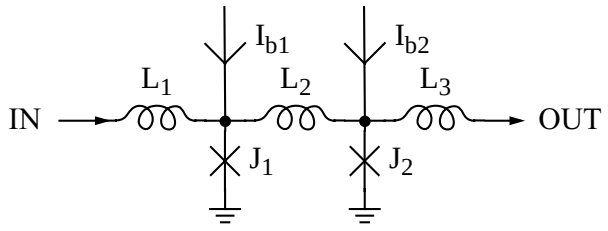


Figure 2-13: Two-stage Josephson transmission line (JTL).

logic gate, so JTL delays can significantly diminish the maximum clock frequency of an RSFQ circuit. In some cases, the delays of long JTLs are avoided by transferring SFQ pulses over purely passive superconducting microstrip transmission lines [70, 71, 72], but the space consumed by such wide (20 μm) microstrip lines and the need for special driver and receiver circuits matched to the line impedance usually restrict their use to signal transmission over long distances (e.g., $>$ 1 mm). Because good impedance matching is needed to minimize signal reflections, the transfer of SFQ pulses over microstrip transmission lines is relatively sensitive to circuit parameters and is not used in any of the RSFQ circuits implemented for this thesis project. In this work, all RSFQ logic gates are connected together with the more robust JTL circuits, and the delays added by the JTLs are carefully minimized through custom design and layout, some of which is detailed at the end of Chapter 10.

The power and chip area consumed by JTLs are substantial, often comparable to those of the logic gates that they connect. The layout of a JTL can be made more compact by modifying the points at which bias currents are injected into the circuit. Each current source in an RSFQ circuit is implemented as a calibrated resistor connected from the power supply line (with a typical supply voltage of 2–3 mV) to the current injection point (where the dc voltage is much smaller than 2–3 mV). If, as shown in Figure 2-13, the bias currents are injected directly into the junctions, one bias resistor is needed for each stage in the JTL. However, two JTL stages can be powered from a single bias resistor if the current is injected into the middle of the inductors that connect the stages, as shown in Figure 2-14. Two inductive current dividers are used to split the currents from sources I_{b1} and I_{b2}. The inductance ratios L_{2A}/L_{2B} and L_{4A}/L_{4B} are selected so that each junction in the JTL is biased at the desired current. The performance and power dissipation of the JTL are unaffected by this modification to its biasing. While the use of only one bias resistor for every two JTL stages does allow more compact layouts, the overhead of a JTL in terms of chip area and power dissipation is never small.

2.2.4 SFQ Splitter

The SFQ splitter shown in Figure 2-15 is used to provide fanout in RSFQ circuits. The circuit is a straightforward extension of an amplifying JTL. As stated in the last section, each junction in an amplifying JTL is capable of driving another junction whose critical current is about $\sqrt{2}$ times larger than its own. In the SFQ splitter circuit, the output junctions J_2 and J_3 are switched in parallel by the input junction J_1. If the critical currents of the three junctions are scaled so that $I_{c2} = I_{c3} = \sqrt{2}I_{c1}/2$, the loading of J_1 by J_2 and J_3 is equivalent to the loading by a single junction with critical current equal to $\sqrt{2}I_{c1}$. Since I_{c1} is only $\sqrt{2}$ times larger than I_{c2} and I_{c3}, each output of the SFQ splitter can drive the

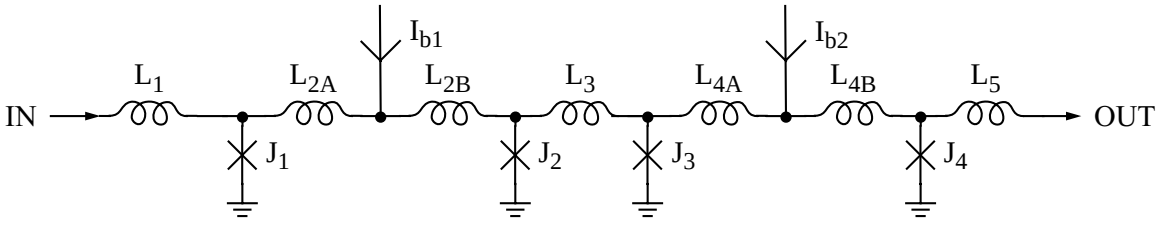


Figure 2-14: Four-stage JTL with alternative injection points for bias currents.

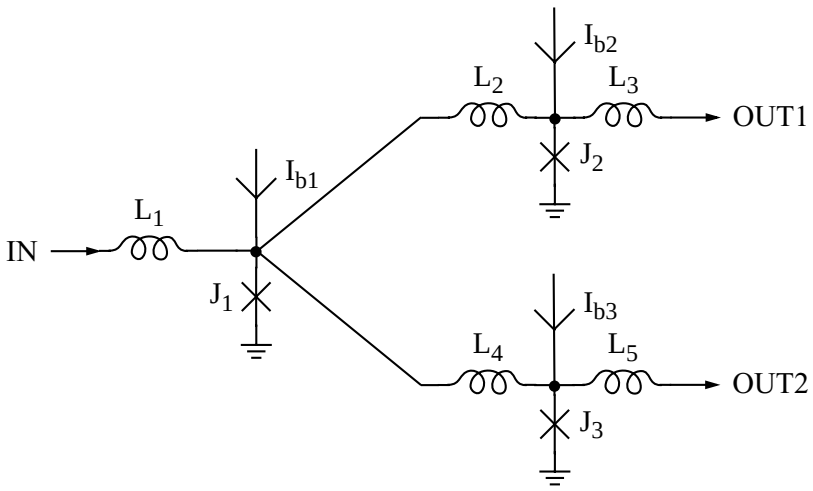


Figure 2-15: SFQ splitter with fanout of two.

input of another SFQ splitter, and SFQ splitters can be cascaded to provide fanouts greater than two.

2.2.5 Unidirectional Buffer

Because of its symmetric structure, a JTL allows SFQ pulse propagation in both directions. As with a passive transmission line, the direction of signal flow is dictated not by the characteristics of the JTL itself but by the manner in which it is driven by the circuits connected to its two ends. In some situations (e.g., see Section 10.2.5), isolation is necessary to protect driving circuitry from backward propagating SFQ pulses. Such isolation can be achieved with the unidirectional buffer shown in Figure 2-16. When an SFQ pulse arrives at the input terminal, it increases the current through inductor L_1 and switches junction J_1. Since junction J_2 does not switch and remains in the superconducting state, the SFQ pulse generated across J_1 is passed to the output terminal. On the other hand, if a backward propagating SFQ pulse is applied to the output terminal, it induces current to flow through L_2, J_2, and J_1. Because the critical current of J_2 is smaller than that of J_1, J_2 is driven above its critical current first. Due to the switching of J_2, the applied SFQ pulse is dropped across J_2 instead of J_1 and does not reach the input terminal.

2.2.6 Confluence Buffer

The confluence buffer shown in Figure 2-17 is used for merging SFQ pulses from two input lines onto a common output line. When an SFQ pulse arrives at the IN1 input, it switches junction J_1. Since junction J_2 does not switch and remains in the superconducting state, the SFQ pulse generated across J_1 is applied to inductor L_3. The resulting current pulse through L_3 switches junction J_5, and an SFQ pulse appears at the output of the circuit. In addition, junction J_4 switches so that the SFQ pulse does not reach the IN2 input. An SFQ pulse arriving at the IN2 input is transferred to the output of the circuit in a completely symmetric manner. In this case, the junctions that switch are J_3, J_5, and J_2. A potential weakness of the confluence buffer is that it may not operate reliably if the IN1 and IN2

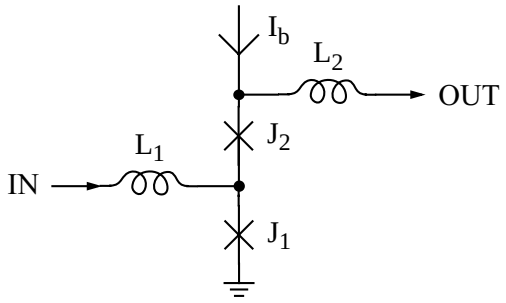


Figure 2-16: Unidirectional buffer.

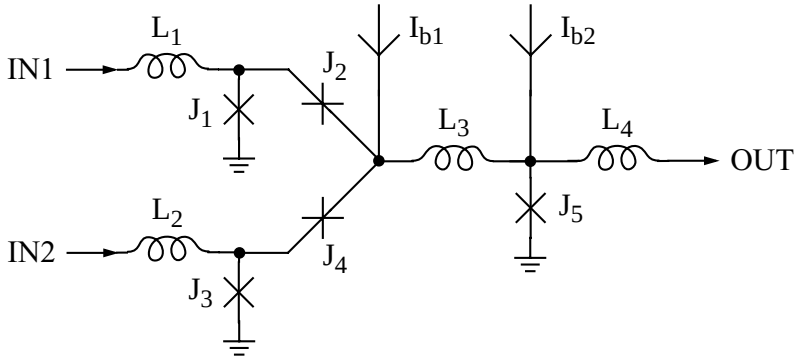


Figure 2-17: Confluence buffer.

input pulses arrive too close in time. Such "pulse collision" problems can be avoided with proper design of the digital system timing.

2.2.7 RSFQ Basic Convention for Representing Binary Information

The previous few sections have described the circuits used to transfer SFQ pulses from one RSFQ logic gate to another. Before examining some of the RSFQ logic gates which accomplish the actual processing and storing of binary data, it is helpful to define the SFQ representation of information more precisely. As illustrated in Figure 2-18, each elementary logic cell of the RSFQ family receives SFQ pulses on a number of signal lines $S_1, S_2, \ldots, S_n$ and on a clock line T. The clock pulses mark the boundaries between adjacent clock periods, during which SFQ pulses can arrive on the signal lines (Figure 2-18(b)). *According to the RSFQ basic convention, the arrival of an SFQ pulse on a signal line during the current clock period represents a binary 1, and the absence of an SFQ pulse during this period represents a binary 0.* Information about the arrival of the SFQ pulses on the signal lines is stored in the internal state of the cell until an SFQ pulse arrives on the clock line T, at which time the cell generates SFQ outputs determined by the logical inputs (i.e., which signal lines received SFQ pulses during the period), and the cell is reset for the next clock period.

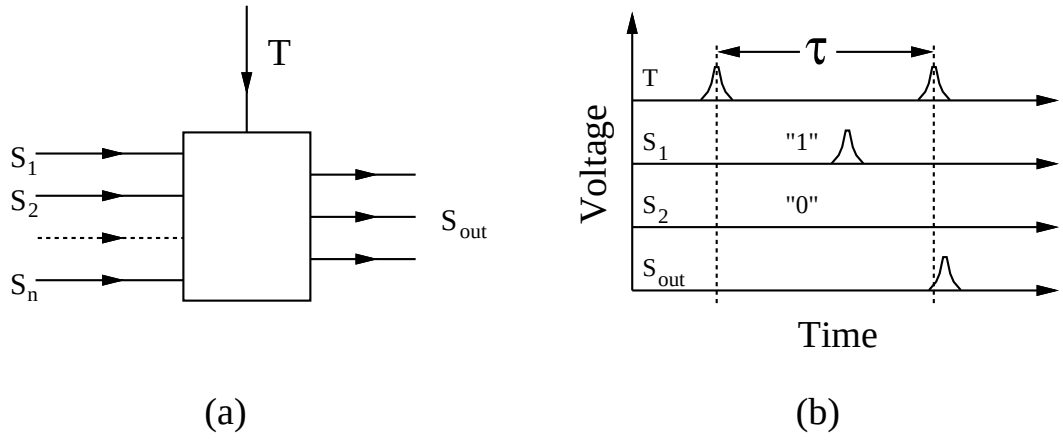


Figure 2-18: RSFQ representation of binary information. (a) General elementary logic cell. (b) Signal timing.

2.2.8 D Latch

A simple circuit cell which exemplifies the operation of an RSFQ logic gate is the D latch, whose schematic and circuit symbol are shown in Figure 2-19. The heart of the circuit is the DJ SQUID loop formed by J_1,J_3, and L_q. The circuit has two stable states with different circulating currents. The circulating current is counterclockwise in the "0" state, clockwise in the "1" state. At the beginning of each clock period, the circuit is in the "0" state, and junction J_1 is biased close to its critical current. When an SFQ pulse arrives at the D input (representing a binary 1), it induces a 2π leap of phase (SFQ pulse generation) in J_1, and the circuit switches to the "1" state. The value of the storage inductor L_q is selected so that the clockwise circulating current now biases junction J_3 close to (but not above) its critical current. When an SFQ clock pulse subsequently arrives at the CLK input, it induces a 2π leap of phase in J_3; the SFQ pulse appearing at the output represents a binary 1. The switching of J_3 also resets the circuit to the "0" state, so readout of the cell is *destructive*.

On the other hand, if no SFQ pulse arrives at the D input during the clock period (representing a binary 0), the circuit is still in the "0" state when the clock pulse arrives at the CLK input. In this case, junction J_3, which carries little dc current in the "0" state, does not switch. Instead, the clock pulse switches junction J_2, whose critical current is smaller than that of J_3. (Because the state of the circuit is detected by the switching of either J_2 or J_3, such a pair of junctions is often given the term "decision-making pair".) The switching of J_2 leaves the state of the circuit unchanged, and the absence of an SFQ output pulse represents a binary 0. Thus, the circuit functions as a clocked register in RSFQ logic. An incoming SFQ data pulse is stored in the SQUID loop until the next clock pulse, when it is released to another RSFQ circuit.

2.2.9 T Flip-Flop

A basic building block of many counter circuits is the toggle (T) flip-flop, whose schematic and circuit symbol are shown in Figure 2-20. This circuit toggles back and forth between two stable states. The circulating current flowing through the DJ SQUID loop formed by

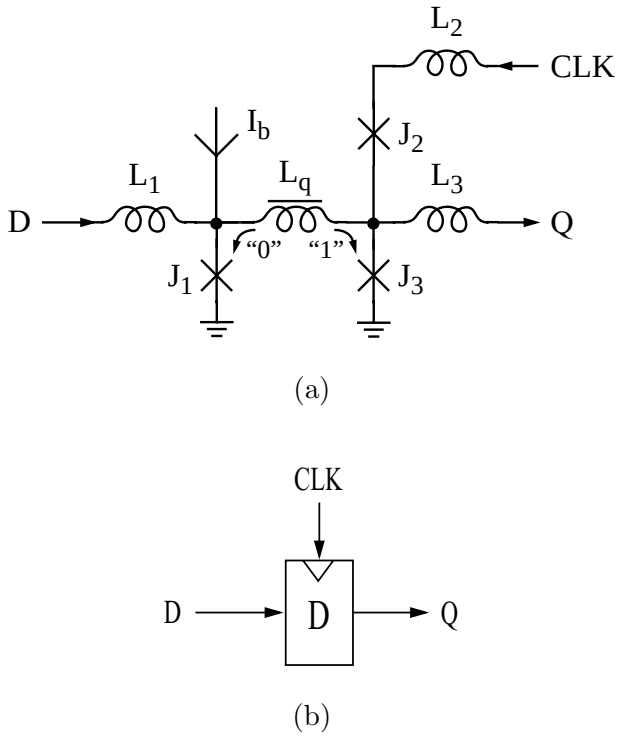


Figure 2-19: D latch. (a) Schematic. (b) Circuit symbol.

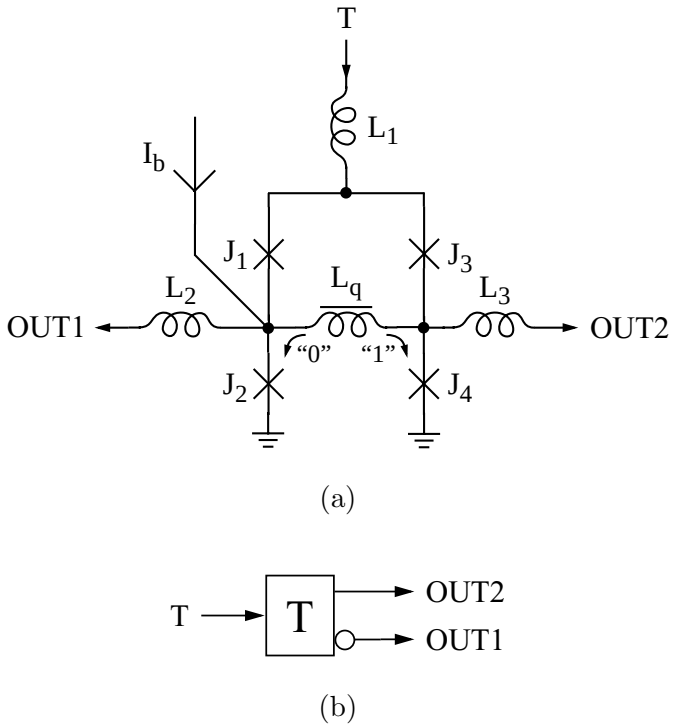


Figure 2-20: T flip-flop with complementary outputs. (a) Schematic. (b) Circuit symbol.

J_2, J_4, and L_q is counterclockwise in the "0" state, clockwise in the "1" state. Because the bias current I_b is applied to the left side of the DJ SQUID, the circuit is in the "0" state before the first SFQ clock pulse is applied to the T input. When an SFQ clock pulse does arrive at the T input, it triggers decision-making pairs J_1–J_2 and J_3–J_4. Because the circulating current adds to the dc current through J_2 and subtracts from the dc current through J_4, the junctions that switch are J_2 and J_3. The switching of these junctions sets the circuit to the "1" state, and an SFQ pulse appears on the OUT1 output. Since the circulating current now flows in the opposite direction, the next SFQ clock pulse arriving at the T input induces the switching of the other junctions in the decision-making pairs – namely, J_1 and J_4. The switching of these junctions resets the circuit to the "0" state, and an SFQ pulse appears on the OUT2 output.

The two outputs of the cell are complementary, producing SFQ pulses on alternate cycles of the clock input. A simple N-bit ripple counter may be realized as a cascade of N T flip-flops. If complementary output signals are not needed, one of the output terminals shown in Figure 2-20 can be left unconnected. While the lack of loading on that output affects the operating margins of the cell, such effects can be compensated with appropriate modification of the circuit parameters.

2.2.10 Timed Inverter

Logical signal inversion in RSFQ logic is accomplished not with a combinational circuit (such as a two-transistor CMOS inverter) but with a clocked circuit having internal state. The schematic and circuit symbol of a timed inverter are presented in Figure 2-21. Junctions J_1 and J_2 form a unidirectional buffer through which an SFQ pulse arriving at the D input is transferred and applied to junction J_3. The SFQ pulse generated across J_3 establishes a circulating current through inductor L_q which biases junction J_4 close to its critical current. The timed inverter is now in the "1" state. When an SFQ clock pulse subsequently arrives at the CLK input, it induces a 2π leap of phase in the upper junction of decision-making pair J_4–J_5. The SFQ pulse generated across J_4 annihilates the circulating current, resetting the cell to its original "0" state. Since junction J_5 does not switch, no SFQ pulse appears on the $\overline{Q}$ output.

On the other hand, if no SFQ pulse arrives at the D input during the clock period, no circulating current through L_q is set up before an SFQ clock pulse arrives at the CLK input. In this case, junction J_4, which carries little dc current in the "0" state, does not switch. Instead, the clock pulse switches junction J_5, and an SFQ pulse appears on the $\overline{Q}$ output. In addition, junction J_2 switches so that no SFQ pulse reaches the D input. After the switching of J_5 and J_2, the circuit remains in the "0" state. According to the RSFQ basic convention, the output of the cell is the logical complement of its D input. The inverter produces an SFQ output pulse when there is no SFQ input pulse, and vice versa.

2.2.11 Clock Pulse Distribution

Clock pulses are distributed to RSFQ logic gates with networks of JTLs and SFQ splitters. Figure 2-22 presents an illustrative example of four D latches clocked by a four-stage JTL. Together, the four D latches and the four-stage JTL form a simple four-stage shift register. Since the propagation delay of the clock JTL is not negligibly small compared to the gate delays of the D latches, the clocking of the four D latches cannot be considered simultaneous

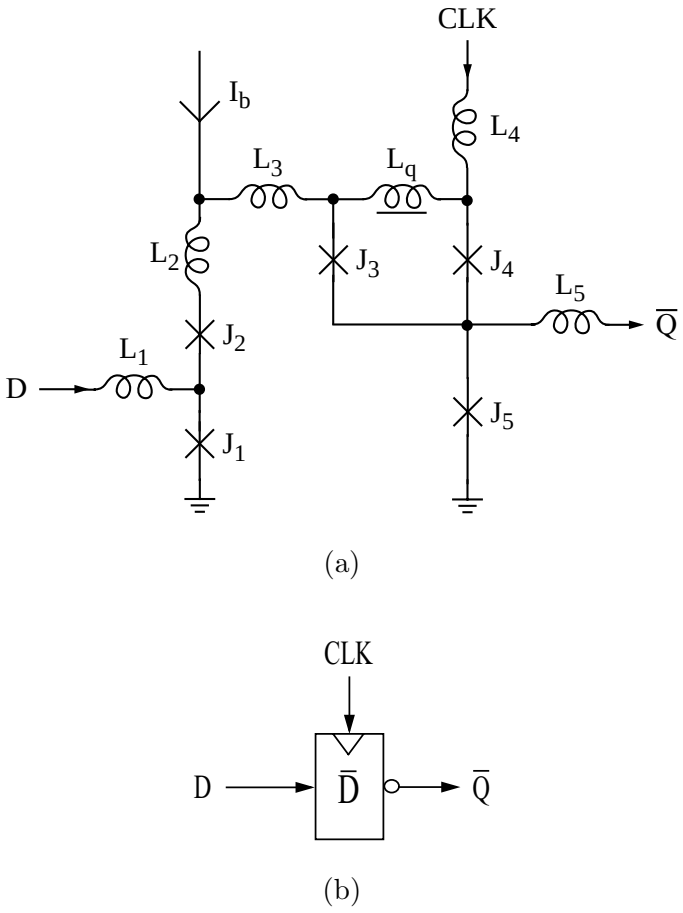


Figure 2-21: Timed inverter. (a) Schematic. (b) Circuit symbol.

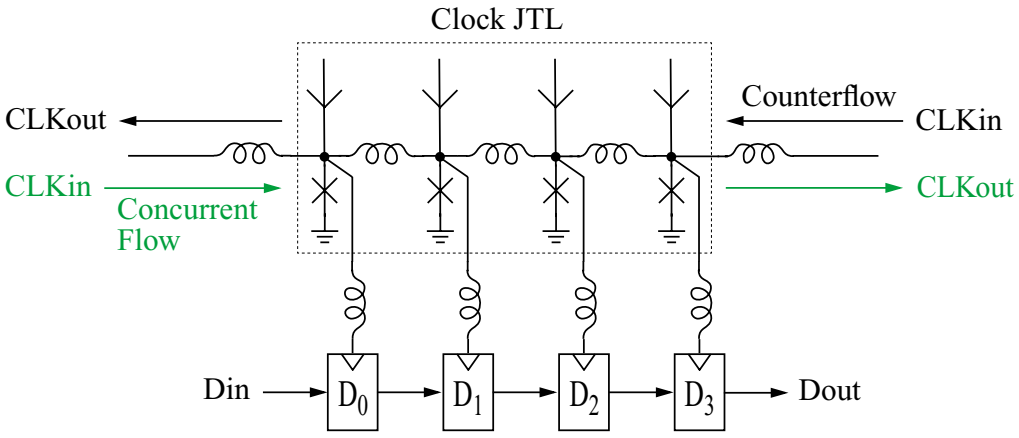


Figure 2-22: Comparison of counterflow and concurrent flow clocking for the case of a four-stage shift register.

(with zero skew). A more realistic picture of the circuit timing is that the D latches are clocked in succession as the advancing front of a "clock pulse wave" passes through the structure. The propagation direction of this clock pulse wave may be the same as or opposite to the direction in which the data bits are shifted.

In a "counterflow" clocking scheme, the clock and data pulses travel in opposite directions. Counterflow clocking is inherently robust and immune to racing problems. For proper circuit operation, each stage of the shift register should be destructively read out before being loaded with a new data bit. This timing requirement is easily satisfied with counterflow clocking, as each stage of the shift register is clocked earlier in time than the previous one (i.e., the one from which it receives a data bit).

In a "concurrent flow" clocking scheme, the clock and data pulses travel in the same direction. Concurrent flow clocking is less robust than counterflow clocking because it is sensitive to racing between the clock and data pulses. In most designs, including the shift register discussed here, the circuit delays are adjusted so that the clock pulses arrive at each logic gate before the data pulses[7]. Provided that the difference in arrival times is at least equal to the hold time of the D latch [73], each stage of the shift register is read out early enough that it is ready to receive the new data bit from the previous stage. While requiring more careful design, concurrent flow clocking of an RSFQ circuit allows higher frequency operation than does counterflow clocking. Both counterflow and concurrent flow clocking schemes are employed in the RSFQ circuits described in later chapters.

[7]Another type of concurrent flow clocking, in which the data pulses race *ahead* of the clock pulses, is considered in Section 10.2.3.

Part II

Optical Clocking

Chapter 3

Optoelectronic Techniques

The use of optoelectronic techniques for generating and detecting electrical pulses on the picosecond time scale is well-established [74, 75, 76, 77]. A comprehensive review of optoelectronics and its many applications is well beyond the scope of this thesis. This chapter focuses on the standard optoelectronic techniques most relevant to this research project. The important characteristics of the optical pulses produced by available laser sources are first described, and the use of harmonic generation for wavelength conversion is discussed. A passive optical technique for pulse rate multiplication is also introduced. Next the performance tradeoffs of different photodetectors for converting picosecond optical pulses into fast electrical pulses are examined. The final sections of the chapter explain how ultrashort optical and electrical pulses can be measured with subpicosecond time resolution.

3.1 Generation of Picosecond Optical Pulses

3.1.1 Characteristics of Mode-Locked Laser Pulses

Lasers operating in a "mode-locked" regime are capable of generating optical pulses on the picosecond and even femtosecond time scales [78, 79, 80]. No attempt is made here to describe the physics of mode-locked lasers. (For an explanation of mode-locking in lasers, see [78].) In this section, a mode-locked laser is treated as a "black box" which can be characterized in terms of its optical output. The emphasis of the discussion is on commercially available laser systems, not research results reported in the literature.

When all the resonant modes of a laser cavity are locked with fixed amplitude and phase relationships to each other, a laser produces a regularly spaced train of optical pulses. The period of this pulse train is determined by the round trip delay of an optical pulse circulating within the laser cavity. If the laser cavity is realized as a short (mm-scale) waveguide integrated on the same chip as a semiconductor laser diode, very high pulse repetition rates can be achieved, easily exceeding 100 GHz [81]. Such monolithic mode-locked lasers are not yet commercially available and have not been used in this work. (Even if these lasers had been available, the long wavelength and low energy of their output pulses would have been unsuitable for the experiments presented in this thesis. These same limitations apply to mode-locked erbium-doped fiber lasers [82].) The two mode-locked lasers used during the course of this project are large benchtop systems which have long been standard tools in the

field of ultrafast optoelectronics: the colliding-pulse, mode-locked (CPM) dye laser [79] and the more recently developed mode-locked titanium-doped sapphire (Ti:sapphire) laser [83]. The laser cavities in these systems are constructed from bulk optical components mounted on a rigid platform. The round trip path length followed by an optical pulse circulating within the laser cavity is a few meters, so the pulse repetition rate is on the order of 100 MHz, and the temporal spacing between consecutive pulses is on the order of 10 ns.

The time duration of individual laser pulses is much shorter than their spacing. The gain media employed in these systems (an organic dye solution in the case of the CPM laser and a crystal rod in the case of the Ti:sapphire laser) have broad lasing bandwidths which support the generation of pulses with widths below 100 fs. Such ultrashort optical pulses act as ideal impulse excitations for the photodetectors used in this project, which all have response times longer than 500 fs (0.5 ps). Consequently, the optoelectronic experiments to be described are sensitive only to the areas (i.e., energies) of the optical pulses, not their exact widths. Because the optical pulse train has a very low duty cycle, the peak power of the emitted laser beam is four to five orders of magnitude higher than its average power.

Historically, the CPM laser was the first widely available source of optical pulses with widths below 100 fs. Its operating wavelength is typically fixed at 620 nm (visible red light). This laser emits its optical pulses in two synchronized output beams, each of which has an average power of about 20 mW. The stability of the CPM laser, while better than that of earlier mode-locked lasers, is fundamentally limited by its use of organic dyes which slowly degrade over time and must be replaced every few weeks. Because the organic dyes are toxic, they require considerable care in handling and disposal. Even when functioning well with fresh dyes, a CPM laser requires attention from a skilled operator on an hourly basis. The optoelectronic sampling experiments described in the next chapter were conducted with femtosecond optical pulses generated by a home-built CPM laser.

During the last decade, the mode-locked Ti:sapphire laser has supplanted the CPM laser as the source of ultrashort optical pulses in most laboratories. The Ti:sapphire laser has a number of advantages which contribute to its popularity. Like the CPM laser, it is capable of generating optical pulses with widths below 100 fs. Because the gain medium is a solid-state crystal rod whose properties are unaffected by usage or aging, this laser is inherently more stable in operation and requires much less maintenance than the CPM laser. Once its pump laser (either an argon ion laser or a diode-pumped solid-state laser) has finished warming up, the Ti:sapphire laser may be operated "hands-free" for several hours at a time. Its optical output is also tunable over a broad range of wavelengths in the near infrared (IR), from below 700 to above 1000 nm. Over most of this range, the average output power exceeds 1 W, almost two orders of magnitude higher than that provided by the CPM laser. The peak output power of this laser can exceed 150 kW. As discussed in the next section, optical pulses with high peak powers can be converted to shorter wavelengths by second-harmonic generation in a nonlinear crystal. Since the wavelength is inversely related to the optical frequency, second-harmonic generation reduces the wavelength by a factor of two (e.g., from 940 to 470 nm). Even with only modest energy conversion efficiencies such as 10%, the second-harmonic pulses produced in this way are more powerful than the pulses directly emitted from the CPM laser. Thus, Ti:sapphire laser systems are useful for generating not just near IR optical pulses, but shorter wavelength pulses as well. A Spectra-Physics Tsunami (model 3960) mode-locked Ti:sapphire laser is a major component of the optical setup presented in Chapter 5 for multi-GHz clocking of superconducting circuits.

Since the output of a mode-locked laser is not a continuous wave but a pulsed wave, its optical spectrum cannot be arbitrarily narrow but must have a nonzero bandwidth $\Delta\omega$. (In the preceding paragraphs, the term "wavelength" refers to the wavelength at the center of this spectrum.) According to the Fourier transform theorem known as the "uncertainty principle", the product of $\Delta\omega$ and the pulse width Δt must obey the inequality [78]

$$\frac{\Delta\omega\Delta t}{2\pi} \geq K, \tag{3.1}$$

where K is a constant on the order of unity, with a value depending upon the detailed shape of the optical pulses and the precise mathematical definitions[1] of $\Delta\omega$ and Δt. Equation 3.1 places a lower limit on the obtainable pulse width for a given spectral bandwidth. Optical pulses which meet this limit are described as being "transform-limited". When properly tuned, both the CPM laser and the mode-locked Ti:sapphire laser can generate nearly ideal transform-limited pulses.

Because of the uncertainty principle, optical pulses with time durations below 100 fs have broad spectral bandwidths corresponding to several nm in wavelength. A broad spectral bandwidth is a disadvantage in some applications. In the optical clocking setup described in Chapter 5, the Josephson chip under test sits near the bottom of a magnetically shielded liquid helium dewar. Short laser pulses are delivered over several meters of optical fiber to a photodiode on the Josephson chip. Because the fiber has significant linear dispersion near the 470 nm (center) wavelength of the pulses, the different frequency components of the pulses travel with unequal group velocities, and the pulses are broadened (in time) as they propagate through the fiber. Because the differences in group velocity are larger across wider spectral bandwidths, shorter pulses suffer more broadening than longer pulses. For the length of fiber used in the optical clocking setup, a pulse with a (transform-limited) width of 100 fs would be broadened to a width above 20 ps, while a pulse with a (transform-limited) width of 1 ps would only be broadened to a width less than 3 ps. As with many practical optical fiber links [84], the shortest input pulse does not yield the shortest pulse delivered to the on-chip photodetector. For this reason, the Spectra-Physics Tsunami mode-locked Ti:sapphire laser in the optical clocking setup is operated not in its "femtosecond configuration" but in its "picosecond configuration" so that it generates nearly ideal transform-limited pulses with a width just over 1 ps and a repetition rate near 80.6 MHz. The lower peak power of the pulses produced in the picosecond configuration also reduces pulse broadening due to nonlinear effects in the optical fiber [85].

Other important characteristics of mode-locked laser pulses include their energy fluctuations, timing jitter, and polarization. In optoelectronic sampling experiments (such as those presented in the next chapter), optical pulses with small energy fluctuations decrease measurement times because less signal averaging is needed to achieve the desired SNR. Small energy fluctuations are even more critical in the optical clocking system, as error-free triggering of a Josephson circuit requires current pulses of fairly uniform size from the on-chip photodetector[2]. According to its specifications [86], the Tsunami mode-locked Ti:sapphire laser generates optical pulses with less than 2% rms noise and less than 5% long-term drift. The CPM is also capable of generating optical pulses with less than 2% rms noise, but

[1] The most commonly used definition for $\Delta\omega$ and Δt is the full-width-at-half-maximum (FWHM).

[2] To a good approximation, the current pulses produced by the photodetector are proportional to the energies of the incident optical pulses.

the long-term drift in its average output power can exceed 10% or more, depending on the condition of its organic dyes. Because of its superior stability, the Ti:sapphire laser is a much better choice for a reliable optical clocking system. A mode-locked laser pulse train with low jitter and highly stable repetition rate is valuable for optical clocking of ADCs. Optical correlation measurements of the type discussed in Section 3.3.1 show that the pulse-to-pulse timing jitter of the Ti:sapphire laser used in the optical clocking system is smaller than 200 fs rms. The drift in the repetition rate of this laser is less than 10 parts per million (ppm) over a timespan of several hours. Such timing accuracy is more than adequate for clocking the superconducting bandpass $\Delta\Sigma$ modulator studied in this work. Typically, the output of a mode-locked laser is linearly polarized to a high degree ($>$ 500:1 in the case of the Ti:sapphire laser).

3.1.2 Wavelength Conversion

As explained later, the on-chip photodetector whose current pulses trigger the Josephson circuitry has the fastest response when illuminated by short wavelength light such as 470 nm (visible blue light). In the optical clocking setup described in Chapter 5, 940 nm optical pulses from the mode-locked Ti:sapphire laser are converted to 470 nm optical pulses by second-harmonic generation (also called "frequency-doubling") in a nonlinear crystal. Only the basic concepts of second-harmonic generation are presented here. The mathematical analysis and implementation details of second-harmonic generation can be found in several books and papers [78, 87, 88, 89, 90].

Figure 3-1 shows a typical optical setup for second-harmonic generation. The key component is a crystal with significant second-order nonlinearity in its susceptibility, such as KH_2PO_4 (KDP), LiB_3O_5 (LBO), and β-BaB_2O_4 (BBO). Because of this nonlinearity, an incident laser beam with optical frequency ω induces a polarization inside the crystal which has a component at frequency 2ω. The oscillating dipoles responsible for this polarization act as a source of coherent radiation with frequency 2ω, and a second-harmonic beam is emitted in the same direction as the fundamental (i.e., incident) beam. Optical power is only efficiently converted from the fundamental frequency to the second harmonic if the phase velocities at ω and 2ω are equal. In practice, such "phase-matching" is usually achieved in birefringent crystals by carefully adjusting the orientation of the crystallographic axes with respect to the direction and polarization of the incident laser beam [87, 88]. The time duration of the pulses in the second-harmonic beam is about $\sqrt{2}$ times shorter than in the fundamental beam, with the spectral bandwidth increased by the same factor [78]. Because the group velocities at ω and 2ω are not usually equal under phase-matching conditions,

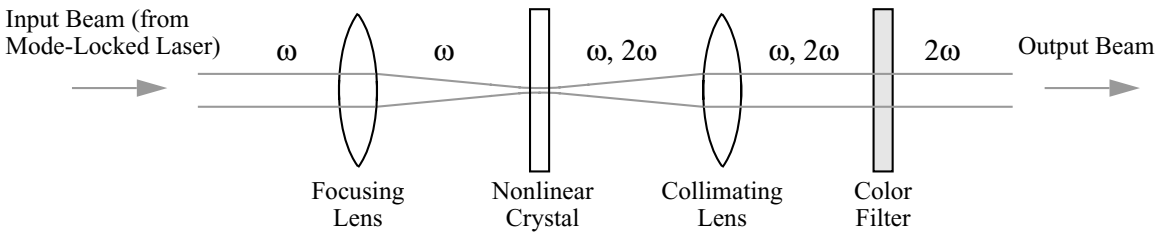


Figure 3-1: Typical setup for second-harmonic generation with nonlinear crystal.

efficient frequency-doubling of picosecond pulses only occurs in the crystal over a short distance proportional to their time durations. For this reason, thinner crystals are used for second-harmonic generation with 100 fs pulses than with 1 ps pulses.

Since second-harmonic generation is a nonlinear effect, high optical intensities inside the crystal increase the conversion efficiency. The high peak powers of the pulses produced by the Tsunami mode-locked Ti:sapphire laser are therefore favorable to frequency-doubling. The conversion efficiencies that can be achieved in the picosecond and femtosecond configurations of this laser are comparable. While the lower peak power in the picosecond configuration reduces conversion efficiency, the greater thickness of the crystal used for second-harmonic generation with 1 ps pulses enhances conversion efficiency. Focusing of the incident beam with a convex lens is typically used to obtain very high peak intensities ($> 10^9$ W/cm^2) inside the crystal. If the focusing is too tight, though, the strong beam divergence away from the focal point compromises phase-matching, and the conversion efficiency is reduced. In practice, the focusing needs to be optimized. Some crystals, such as KDP and BBO, permit tighter focusing of the incident beam in one transverse direction than in another. The conversion efficiency with these crystals can often be improved by focusing the incident beam with a pair of orthogonal cylindrical lenses with different focal lengths [89], rather than the spherical lens indicated in Figure 3-1. In this case, the focal spot inside the crystal is elliptical instead of circular. Cylindrical focusing is used with a BBO crystal in the setup described in Chapter 5.

The fundamental and second-harmonic beams leaving the nonlinear crystal are recollimated with a convex lens (or a pair of cylindrical lenses if cylindrical focusing is employed). Since the conversion efficiency is usually modest (e.g., 10%), the fundamental beam leaving the crystal is more powerful than the second-harmonic beam. This fundamental beam is removed from the second-harmonic output with highly selective color filters such as dichroic beamsplitters [91] and Schott glass [92].

3.1.3 Pulse Rate Multiplication

While pulse repetition rates on the order of 100 MHz are convenient for most optoelectronic sampling experiments (including those described in the next chapter), much higher repetition rates are needed for multi-GHz testing of superconducting circuits. In this work, higher repetition rates have been obtained by splitting each pulse from the Ti:sapphire laser into a train of pulses with equal spacing T_1, as depicted in Figure 3-2. Such a "pulse splitter" can be realized with various arrangements of beamsplitters and optical delay lines [93, 94]. Since the pulse splitter is purely passive, its operation unavoidably reduces the pulse energies. The high power of the Ti:sapphire laser source makes such reductions in pulse energies

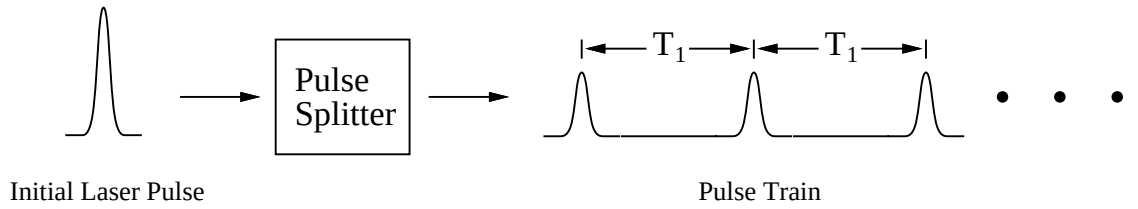


Figure 3-2: Increasing the repetition rate by pulse splitting.

affordable in the present application.

An uninterrupted stream of uniformly spaced pulses is needed for clocking the superconducting bandpass $\Delta\Sigma$ modulator. In order to achieve a seamless transition between the pulse trains produced by the pulse splitter, T_1 should be an exact submultiple of the fundamental period T of the mode-locked laser. If M is the number of pulses in each train produced by the pulse splitter, T_1 should equal

$$T_1 = \frac{T}{M}. \tag{3.2}$$

For the pulse splitter constructed in this project, $T \approx 12.41$ ns, and M=256, so $T_1 \approx 48.5$ ps. Thus, the 80.6 MHz repetition rate of the laser is multiplied up to 20.6 GHz. The design, operation, alignment, and calibration of this pulse splitter are detailed in Chapter 5. That chapter also explains how more complex pulse patterns and lower repetition rates can be selected by blocking various beams within the pulse splitter. Some of these more complex pulse patterns are useful for high speed testing of superconducting digital circuits.

3.2 Generation of Picosecond Electrical Pulses

3.2.1 Optical-to-Electrical Conversion

Picosecond (or femtosecond) optical pulses can be converted to picosecond electrical pulses with a fast photodetector. The cleanest electrical pulses are generated if the wires connected to the photodetector are arranged as on-chip transmission lines with well-defined impedances. Figure 3-3 shows a typical circuit configuration in which the photodetector bridges a gap between two sections of transmission line with characteristic impedances $Z_{0,1}$ and $Z_{0,2}$. While $Z_{0,1}$ and $Z_{0,2}$ are often chosen to be equal for reasons of simplicity and convenience, such matching does not bear any special advantage for circuit operation. The left section of transmission line provides the bias voltage for the photodetector. Prior to optical excitation, no current flows through the photodetector, and the voltage across the load resistor R_L is zero. When an optical pulse strikes it, the photodetector conducts for a short period of time, and an electrical pulse is transferred down the right section of transmission line toward the load. Assuming that load resistor R_L is matched to $Z_{0,2}$, no reflection occurs, and a single voltage pulse is generated across the load.

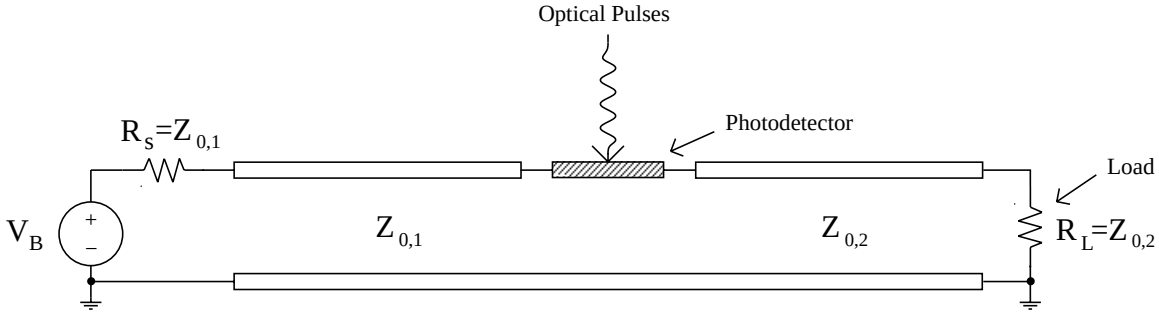


Figure 3-3: Biased transmission line configuration for optical-to-electrical conversion of picosecond pulses.

Since the photodetector draws current from the biased (i.e., left) section of transmission line, an electrical pulse also propagates along that section toward the bias voltage source V_B. Provided that source resistance R_s is matched to $Z_{0,1}$, this pulse is completely absorbed at the left end of the line and never affects the load. In practice, however, controlling the source impedance of the externally supplied bias voltage is difficult at the high frequencies contained within a picosecond pulse. The large pad structures used for off-chip connections have complex impedances which cannot be effectively matched to an on-chip transmission line, so the reflections from the pads are substantial. A more practical technique for suppressing reflections along the biased section of transmission line is to make this section lossy by increasing its series resistance per unit length. In this scheme, a pulse traveling along the biased section is dissipated before it reaches the pads at the end of the transmission line. The need for and effectiveness of this scheme are demonstrated experimentally in the next chapter.

With proper termination of the transmission lines, the performance of the optoelectronic interface is primarily limited by the speed of the photodetector. A fast photodetector can be implemented with several different semiconductor devices, including p-i-n photodiodes, Schottky photodiodes, avalanche photodiodes, and multiple-quantum-well detectors [95]. Some of these devices are not well-suited to operation at cryogenic temperatures, however. Devices whose operation depends critically on doping of the semiconductor are particularly vulnerable at low temperatures to incomplete ionization of dopants and carrier freeze-out effects [96]. The two types of photodetectors used during the course of this project, the picosecond photoconductor [36] and the metal-semiconductor-metal (MSM) photodiode [97, 98], have the important attribute that they function as well at cryogenic temperatures as at room temperature. The simple structures of these devices and their compatibility with silicon substrates are advantageous for integration with Josephson circuits [38, 39]. The operation and performance of these two types of photodetectors are now described.

3.2.2 Picosecond Photoconductors

One of the simplest types of photodetectors is the photoconductor, which is formed by depositing two metal electrodes on a piece of semiconductor, as shown in Figure 3-4. A bias voltage is applied between the electrodes so that an electric field is set up inside the semiconductor. Because virtually all of the carriers in the semiconductor are frozen out at cryogenic temperatures, the semiconductor is insulating, and no current flows through the photoconductor in the absence of light. When the area between the electrodes is illuminated by an optical pulse, the photogenerated carriers in the semiconductor experience the electric field due to the bias voltage, and a drift current begins to flow. The rise time of the photocurrent is extremely fast ($\ll$ 1 ps with a femtosecond optical pulse) and does not limit the speed of the electrical pulse that is produced on the transmission line. Instead, the electrical pulse width is limited by the fall time of the photocurrent. In a picosecond photoconductor (also called an "Auston switch"), the fall time is minimized by intentionally decreasing the carrier lifetimes inside the semiconductor [36]. Once the carriers disappear through recombination, the photocurrent terminates. One method of reducing the lifetimes dramatically is to bombard the semiconductor with ions so that a large number of defects are created inside the crystal. With enough defects acting as traps and recombination centers, carrier lifetimes below 1 ps can be achieved [37]. Because the response time of

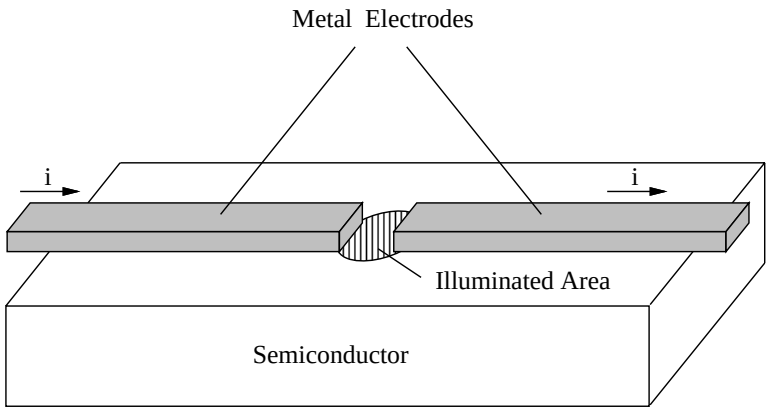


Figure 3-4: Structure of picosecond photoconductor.

a picosecond photoconductor is limited by carrier lifetimes and not by the transit time between the electrodes, the physical dimensions of the device have little effect on its speed.

Ohmic contacts are easily made to semiconductors with high defect densities [36]. With good ohmic contacts, the photocurrent is proportional to the bias voltage applied across the electrodes:

$$i(t) = G(t)v(t). \tag{3.3}$$

In pulse generation applications, the bias voltage $v(t)$ is usually a dc voltage (such as V_B in Figure 3-3). More generally, though, $v(t)$ can be time-dependent. Assuming that the picosecond photoconductor is struck at $t=0$ by an optical pulse with negligible width ($\ll$ 1 ps), the time-dependent conductance $G(t)$ can be modeled by a simple exponential response function [37],

$$G(t) = \begin{cases} 0 & \text{if } t < 0, \\ G_0 e^{-t/\tau_c} & \text{if } t \geq 0, \end{cases} \tag{3.4}$$

where τ_c is the carrier lifetime[3]. The peak conductivity G_0 is proportional to the energy of the optical pulse. Equations 3.3 and 3.4 show that the bias voltage affects only the amplitude of the photocurrent pulse, not its time duration.

Reducing the carrier lifetimes by introducing high defect densities into the semiconductor has one major disadvantage. Scattering from the defects decreases the carrier mobilities substantially [36]. Consequently, the sensitivity of a picosecond photoconductor is much lower than that of other photodetectors. Even at bias voltages just short of breakdown, the photocurrent is typically smaller than that of a quantum efficient photodetector[4] by more than three orders of magnitude. The very low sensitivity severely limits the utility of the picosecond photoconductor for multi-GHz clocking of superconducting circuits. Since the average optical power scales with the pulse repetition rate, high optical pulse energies are not practical at repetition rates in the tens of GHz. According to circuit simulations, a picosecond photoconductor would require over 100 mW of average optical power to switch a Josephson junction at 20 GHz. Such high average optical power would cause excessive

[3]The carrier lifetimes of electrons and holes are assumed to be equal in this simple model.

[4]An ideal quantum efficient photodetector is one for which each incident photon contributes one electron charge to the photocurrent.

chip heating – enough, in most cases, to destroy the superconductivity altogether. For this reason, the slower but much more sensitive MSM photodiode described below was chosen for the optical clocking application. In this project, picosecond photoconductors were only employed in the optoelectronic sampling experiments presented in the next chapter. With the moderate repetition rate ($\approx$ 90 MHz) used in those experiments, the average incident optical power was only a couple mW, and no problems due to chip heating were encountered.

When ion bombardment is used to create defects inside the semiconductor material, it is important that the radiation damage be physically distributed so that the carrier lifetimes are short throughout the entire active region of the picosecond photoconductor. This is more easily accomplished if the semiconductor is a thin film rather than bulk material. A popular substrate for fabrication of picosecond photoconductors is silicon-on-sapphire [99]. Because the thickness (e.g., 0.5 μm) of the silicon layer is less than the penetration depth of the light at most wavelengths, a significant fraction of the incident photons are not absorbed. This effect reduces the sensitivity even further.

3.2.3 Metal-Semiconductor-Metal (MSM) Photodiodes

Like a picosecond photoconductor, an MSM photodiode is formed by depositing two metal electrodes on a piece of semiconductor. In this device, however, the metal-to-semiconductor contacts are Schottky barriers which inhibit injection of carriers from the metal electrodes into the semiconductor. Once all of the carriers generated by a picosecond optical pulse are swept out by an applied electric field to the metal electrodes, the photocurrent terminates. Therefore, the fall time of the photocurrent is limited by the carrier transit time between the electrodes, not the carrier lifetimes, which are long since the semiconductor crystal is left virtually defect-free. (As in the case of the picosecond photoconductor, the rise time of the photocurrent is extremely fast and does not limit the electrical pulse width.) The quantum efficiency of an MSM photodiode is typically high, as most of the photogenerated electron-hole pairs are collected at the metal electrodes. Unlike the case of the picosecond photoconductor, the time duration of the photocurrent pulse is affected by the bias voltage. The fastest response is obtained when the MSM photodiode is biased at a high enough voltage that its carriers reach saturation velocity [98].

Because it is limited by the carrier transit time, the speed of an MSM photodiode improves as the separation between the metal electrodes is reduced. The simple gap geometry shown in Figure 3-4 is not practical with very small interelectrode spacings since a minute active area hinders efficient coupling to incident light. A usefully large active area with small interelectrode spacing can be obtained if the electrodes are laid out in an interdigitated pattern, as illustrated in Figure 3-5. If the width and spacing of the interdigitated fingers are equal, about half of the incident light is reflected off the metal electrodes, and the quantum efficiency of the photodetector is close to 50%. Even with interelectrode spacings as small as 0.1 μm, MSM photodiodes are not as fast as picosecond photoconductors [98]. Furthermore, submicron lithography is not yet available in Josephson integrated circuit processes. The silicon MSM photodiode used in this work has interdigitated fingers with width and spacing both equal to 1 μm, and the active area of the photodetector is 20 μm $\times$ 20 μm. At these dimensions, the capacitance of the interdigitated electrodes has a negligible effect on device performance [98, 100]. Optoelectronic sampling experiments conducted at the University of Rochester [101] have shown that at cryogenic temperatures a silicon MSM photodiode with these dimensions generates electrical pulses with a full-width-at-half-maximum (FWHM)

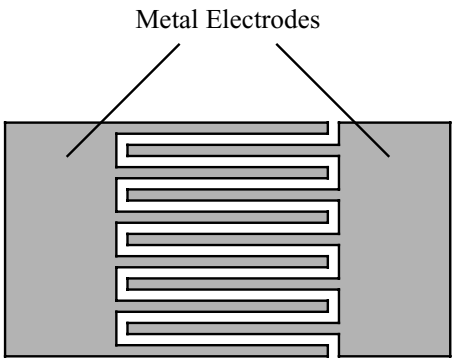


Figure 3-5: Interdigitated electrode layout for MSM photodiode.

below 10 ps, and its recovery to the nonconducting state is fast enough for operating frequencies close to 40 GHz. In this project, such a photodetector has been used to clock superconducting circuits at frequencies up to 20.6 GHz with only about 1 mW of average incident optical power, approximately half of which is absorbed and contributes to chip heating.

The MSM photodiode is fabricated on bulk silicon because that is the substrate commonly used in Josephson integrated circuit processing. A silicon MSM photodiode has the fastest response when illuminated by short wavelength light such as 470 nm. The penetration depth of light in a semiconductor typically increases with wavelength [96]. At longer wavelengths, carriers are generated at depths which exceed the spacing between the interdigitated fingers. Since the electric field due to the bias voltage is weaker away from the surface, deep carriers experience increased transit times which add a slow "tail" to the photocurrent pulse. Marked degradation of speed due to deep carrier generation has been observed experimentally in a silicon MSM photodiode at wavelengths of 725 nm and longer [102]. Short wavelength excitation is especially important for high speed operation at low temperatures, where penetration depths are longer than at room temperature [96]. The need for short wavelength light was an important consideration in choosing the laser source for the optical clocking system.

3.3 Measurement of Picosecond Pulses

Even the fastest oscilloscopes do not have bandwidths adequate for accurate measurement of picosecond (or femtosecond) pulses. Several specialized techniques have been developed for measuring ultrafast optical and electrical signals [103, 36, 76]. The next couple of sections describe two popular measurement techniques which were used during the course of this project. The first technique is used for measuring ultrashort optical pulses, the second for measuring ultrashort electrical pulses. While the details of implementation differ, both techniques are based on measuring the correlation between two ultrashort pulses whose relative timing is controlled with subpicosecond accuracy.

3.3.1 Optical Correlation

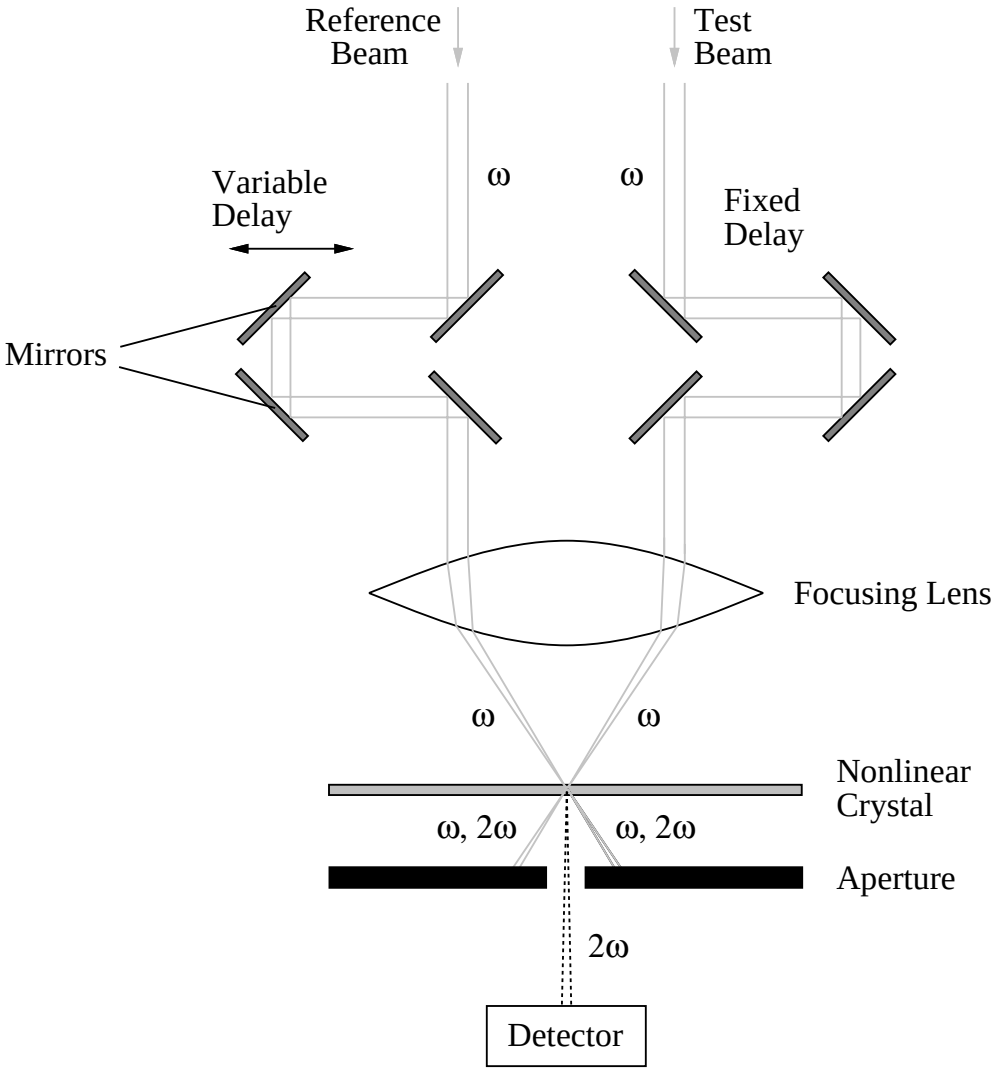
A standard experimental technique for determining the time duration of a mode-locked laser pulse is to measure its autocorrelation [104, 105]. The measurement is made by dividing the laser pulse into two beams with a beamsplitter and then passing the two beams to an optical correlator, an implementation of which is shown in Figure 3-6(a). The beam paths before the correlator have balanced delays so that the pulses in each beam enter the correlator at approximately the same time. The relative delay between the pulses in the reference beam and the test beam is varied by mechanically changing a path length within the correlator[5]. For automated measurements, mirrors are placed on a precision translation stage driven by a computer-controlled stepping motor. Since the speed of light in air is known, the movement of the mirrors is easily converted to a time delay with an accuracy much better than 1 ps. The reference and test beams are focused with a lens to the same spot on a nonlinear crystal of the type discussed in Section 3.1.2. Due to the nonlinearity, some of the laser power incident upon the crystal is converted from optical frequency ω to 2ω. A noncollinear arrangement [106] of the reference and test beams is used so that the beams that are emitted in response to either incident beam acting alone can be blocked with an aperture. The only beam passed to the detector is produced by a nonlinear interaction between the reference and test beams and has a direction between theirs. The strength of the nonlinear interaction depends on the temporal overlap of the pulses in the reference and test beams. The average intensity of the detected beam is a maximum when the pulses are coincident and decreases with relative delays further from zero. The measurement is background-free, as no signal is detected in the absence of temporal overlap [103]. Mathematically, the average intensity that is measured as a function of relative delay represents the autocorrelation function of the laser pulse shape. The autocorrelation trace of a typical mode-locked laser pulse is sketched in Figure 3-6(b).

The nonlinear crystal in an optical correlator is optimized more for low dispersion than for high conversion efficiency. If the pulses in the reference and test beams have only moderate intensities, the average intensity of the beam measured by the detector is very low. For this reason, the detector is usually a highly sensitive photomultiplier tube. If necessary, the effects of room light and other low frequency noises can be suppressed by modulating either the reference or test beam with a mechanical chopper and synchronously demodulating the detector output with a lock-in amplifier.

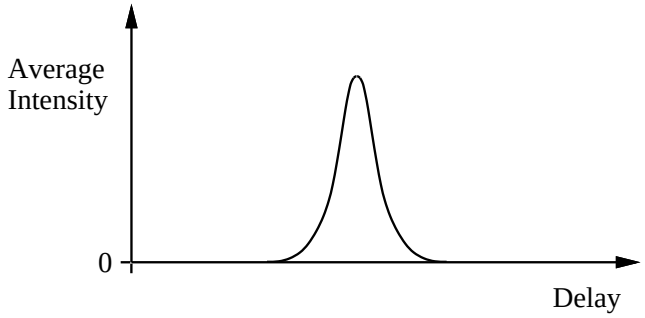
Measurement of the autocorrelation does not uniquely determine the shape of a laser pulse. For instance, the asymmetry of a laser pulse is not revealed in its autocorrelation, which is always a symmetric function. The laser pulse shape can be uniquely determined by measuring higher-order correlation functions [103], but such detailed knowledge of a laser pulse is not required in most experiments. Often the width Δt of a laser pulse is directly estimated from the width $\Delta\tau$ of its autocorrelation by assuming a pulse shape for which the ratio $\Delta\tau/\Delta t$ is known. A commonly assumed pulse shape is sech^2, for which $\Delta\tau/\Delta t = 1.55$ (with both $\Delta\tau$ and Δt defined as FWHMs).

An optical correlator has other uses besides estimating the time duration of a laser pulse. The timing jitter in the mode-locked laser pulse train can be evaluated by measuring the

[5]For the autocorrelation measurement being discussed here, the names "reference beam" and "test beam" are completely arbitrary, as the roles of the two beams are identical. These names have more meaning for cross-correlation measurements, which are discussed later in this chapter, as well as in Chapter 5.



(a)



(b)

Figure 3-6: Measurement of optical pulses by correlation. (a) Implementation of optical correlator. (b) Autocorrelation trace of typical mode-locked laser pulse.

cross-correlations between different pulses. The experimental setup shown in Figure 3-7 allows the cross-correlation between consecutive laser pulses to be compared easily with the autocorrelation of a single pulse. The test beam is split into two beams and then recombined[6] into one by means of two beamsplitters. The mirror positions are adjusted so that the difference in delays between paths A and B precisely equals T, the period of the mode-locked laser pulse train. An autocorrelation of a single laser pulse is measured by blocking path B so that the test beam only passes through path A. A cross-correlation between consecutive laser pulses is measured by blocking path A so that the test beam only passes through path B. If the mode-locked laser pulse train is perfectly periodic without any jitter, adding one period of delay to the test beam has no effect on the measurement, and the cross-correlation matches the autocorrelation exactly. However, if the pulse-to-pulse timing jitter of the mode-locked laser is appreciable, the cross-correlation is wider (and shorter) than the autocorrelation, as illustrated in Figure 3-8(a). This experimental technique was used in this work to evaluate the timing jitter of the Tsunami mode-locked Ti:sapphire laser when operating in its picosecond configuration. The measured pulse-to-pulse cross-correlation was found to be no wider than the measured autocorrelation. Based on the accuracy of the measurements, the pulse-to-pulse timing jitter of this laser must be less than 200 fs rms.

Optical cross-correlation measurements are also useful for precise calibration of path delays. If, for instance, the difference in delays between paths A and B in Figure 3-7 is slightly larger than T, the position of the cross-correlation is shifted from that of the autocorrelation, as illustrated in Figure 3-8(b). The magnitude of the shift is a precise measurement of the delay error. Chapter 5 explains in detail how optical cross-correlations were used to calibrate the path delays within the pulse splitter used for repetition rate multiplication.

3.3.2 Optoelectronic Sampling of Fast Electrical Signals

Fast electrical signals can be measured with subpicosecond time resolution by optoelectronic sampling [36, 37, 107, 76, 77]. All optoelectronic sampling methods operate by probing an electrical quantity such as a voltage or electric field with an ultrashort optical pulse from a mode-locked laser. What distinguishes one optoelectronic sampling method from another is how the probing is implemented. A photoconductive sampling gate [36] is realized by connecting a picosecond photoconductor to the circuit under test. The voltage being sampled acts as the bias voltage for the picosecond photoconductor. (As mentioned earlier, this bias voltage can be time-dependent.) When struck by an optical pulse, the picosecond photoconductor generates a current pulse which is proportional to the voltage being sampled. The time resolution of the photoconductive sampling gate is determined by the time duration of the photoconductance ($G(t)$ in Equation 3.3). With a femtosecond laser pulse and short enough carrier lifetimes in the photoconductor, subpicosecond time resolution is achievable.

If the electrical signal being measured is optoelectronically generated with the same

[6]Some optical power is lost upon recombining the beams, but the transmission efficiency of the setup is not important to the present discussion. As explained in Chapter 5, the transmission efficiency of splitting and recombining beams is a major consideration in the design of the pulse splitter used for repetition rate multiplication.

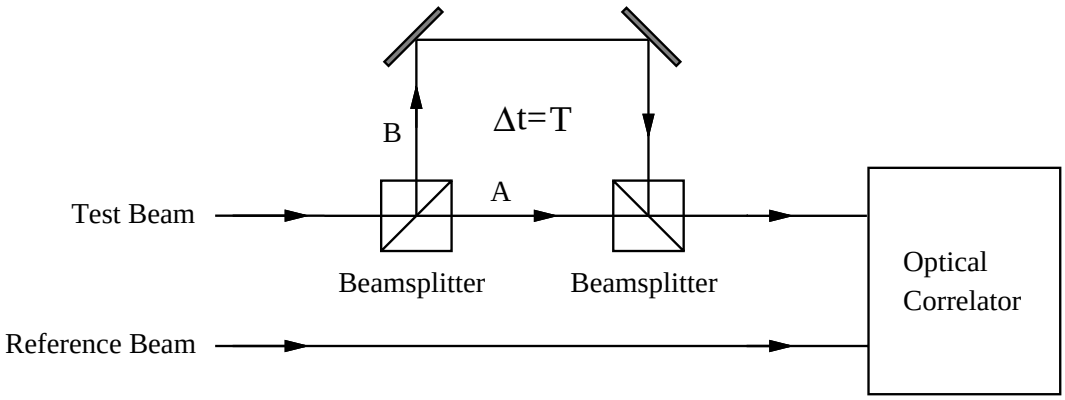
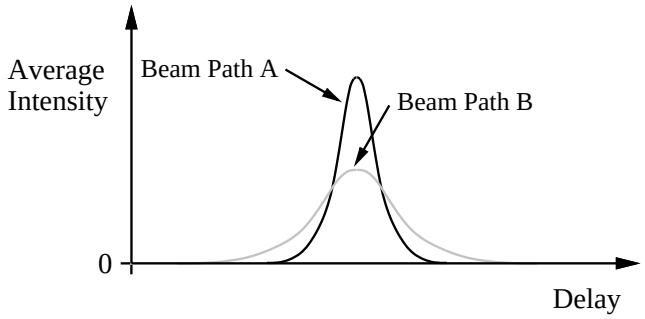
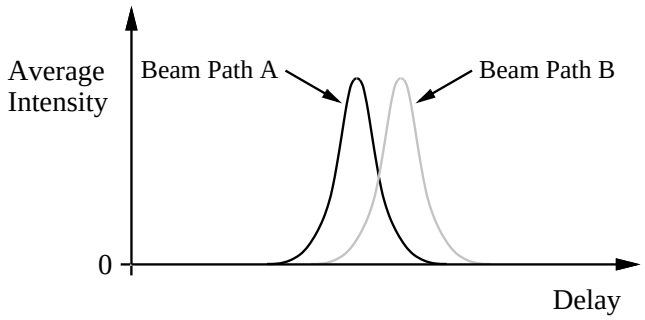


Figure 3-7: Experimental setup for comparing pulse-to-pulse cross-correlation with autocorrelation of single pulse.



(a)



(b)

Figure 3-8: Comparisons of pulse-to-pulse cross-correlation (beam path B) and autocorrelation of single pulse (beam path A). (a) The mode-locked laser pulse train has appreciable pulse-to-pulse timing jitter. (b) The difference in delays between paths A and B is slightly larger than T.

laser pulse used for the sampling gate, virtually jitter-free sampling can be accomplished. As an example, Figure 3-9 presents a microstrip transmission line circuit used for generating and sampling electrical pulses on the picosecond time scale. The term "photoconductive gap" is shorthand notation for a picosecond photoconductor which bridges a gap between transmission line sections. A mode-locked laser pulse is divided with a beamsplitter into the exciting and sampling beams which illuminate the two photoconductive gaps. The gap illuminated by the exciting beam is biased by a dc voltage. As explained in Section 3.2.1, each laser pulse striking this gap launches a short positive voltage pulse on the main transmission line and a short negative voltage pulse on the bias line. The main transmission line is long enough that the reflection from its end is not observed within the time window of the measurement. The photoconductive gap illuminated by the sampling beam is used as a sampling gate to detect the pulse propagating along the main transmission line. The delay of the laser pulse in the sampling beam relative to the one in the exciting beam is varied by moving mirrors placed on a computer-controlled translation stage similar to that used in an optical correlator. With a repetitive train of mode-locked laser pulses, the voltage sampled at a given value of relative delay can be determined by measuring the dc current through the sampling gate with an ammeter. By measuring this dc current as a function of the relative delay between the exciting and sampling beams, the time response of the electrical pulse on the transmission line is obtained. Mathematically, the time response measured in this way equals the cross-correlation of the electrical pulse on the transmission line with the time-dependent photoconductance of the sampling gate [36].

Since the sensitivity of a picosecond photoconductor is very low, the average current flowing through the sampling gate is quite small. For this reason, the ammeter is implemented as a low-noise current amplifier in most experimental setups. Often the exciting beam is modulated with a mechanical chopper, and the current amplifier output is synchronously demodulated with a lock-in amplifier so that the measurement is not affected by dc offsets and low frequency noises [36, 37].

Other types of photodetectors can be substituted for the picosecond photoconductor which generates the electrical pulse on the main transmission line. Such a hybrid arrange-

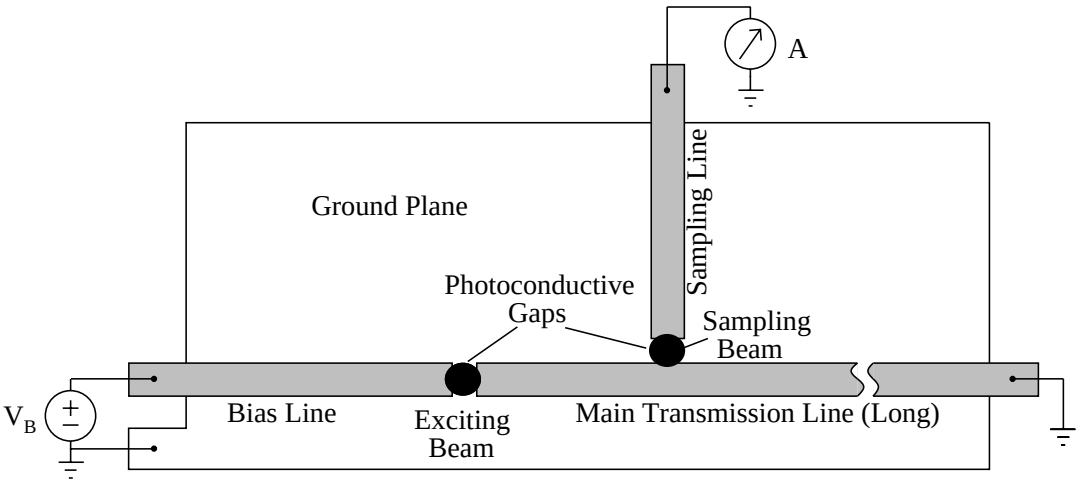


Figure 3-9: Microstrip transmission line circuit with picosecond photoconductors for generating and sampling fast electrical pulses.

ment, with different types of photodetectors generating and detecting the electrical pulses, has been used for high speed characterization of various photodetectors, including p-i-n photodiodes [36] and MSM photodiodes [97]. On the other hand, most photodetectors (including MSM photodiodes) are not suitable substitutions for the picosecond photoconductor which samples the electrical pulse, as their photocurrents are not linear with bias voltage, except at low voltages where their speed of response is degraded.

An alternative to photoconductive sampling is electro-optic sampling [76, 77], in which the electric field due to the pulse on the transmission line is probed with a nonlinear crystal placed in close proximity to the circuit. Due to the Pockels effect, the electric field changes the birefringence in the crystal so that the polarization of the sampling beam propagating through it is altered. By measuring the change in polarization as a function of the relative delay between the exciting and sampling beams, the time response of the electrical pulse is determined. The time resolution (less than 200 fs [108]) achieved with electro-optic sampling is even finer than that achieved with photoconductive sampling. The practical details of electro-optic sampling are not covered here, as only photoconductive sampling was used in this work.

Chapter 4

Optoelectronic Sampling Experiments

4.1 Introduction

While the optoelectronic techniques described in the last chapter for generating picosecond electrical pulses are well-established, in the past little attention has been paid to the suppression of transmission line reflections. In most optoelectronic sampling experiments, the transmission line lengths are chosen so that no reflection occurs within the time window of the measurement. As long as the reflections die out due to dissipation before the next laser pulse launches another electrical pulse on the transmission line, they have no effect on the measured result. At the modest pulse repetition rates (100 MHz or less) usually used in such experiments, this condition is easily satisfied, even with the low loss of a superconducting transmission line. The suppression of transmission line reflections becomes essential, however, at the high pulse repetition rates used for multi-GHz clocking of superconducting circuits. To study the effectiveness of termination techniques, optoelectronic sampling experiments were conducted on the propagation and reflection of picosecond pulses on superconducting microstrip transmission lines. This chapter describes these experiments and presents their main results. Measurements demonstrate the importance of dampening the bias line of the photodetector used for optical-to-electrical conversion so that reflections do not generate spurious responses. The effective suppression of reflections with matched resistive loads is shown up to frequencies approaching 1 THz. The lessons learned here influenced the design of the optoelectronic interface used in later experiments with Josephson circuits.

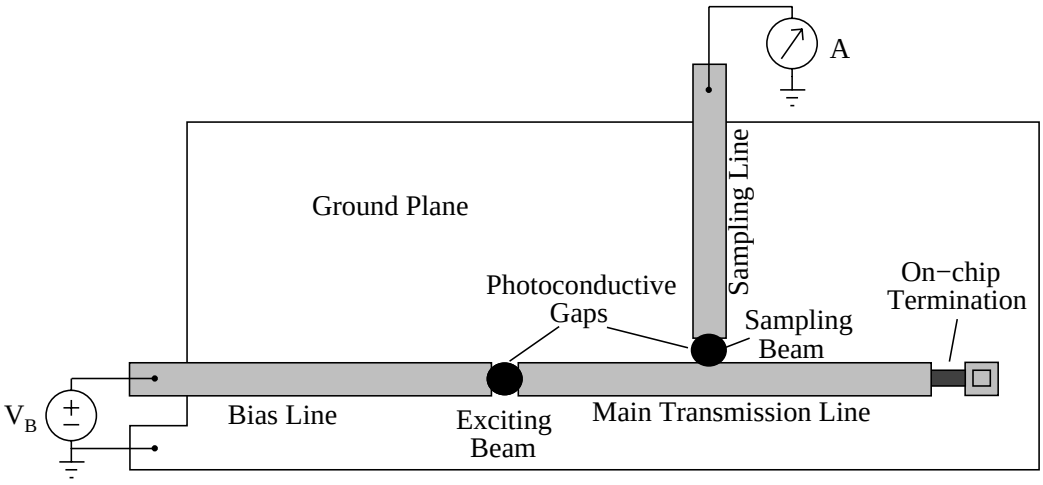
While studying transmission line reflections and techniques for their suppression was the original motivation behind these experiments, valuable data were also acquired on the high frequency performance of the superconducting microstrip lines themselves. The ability to pass SFQ pulses of picosecond duration along superconducting microstrip lines with negligible distortion is often cited as a key feature of Josephson digital technology [31, 71]. Theoretical calculations performed by Kautz [109] show that picosecond pulses can propagate along Nb microstrip lines with little broadening over distances exceeding typical chip dimensions. Such calculations, however, represent an idealized situation; for instance, the dielectric between the conductors is assumed to be lossless and dispersionless. Prior to this work, the performance of real Nb microstrip lines was never rigorously tested. Optoelectronic sampling experiments were used to study the propagation of picosecond pulses along

Nb coplanar transmission lines [107]. While low attenuation and dispersion were demonstrated for frequencies below the gap frequency of Nb ($\approx$ 0.7 THz), the relatively high characteristic impedance ($Z_0 \approx 100\ \Omega$) of coplanar lines makes them unsuitable for transferring SFQ pulses generated by low impedance (1–10 Ω) Josephson junctions. Because low impedance microstrip lines differ significantly from these coplanar lines in geometry and dielectric, it is difficult to infer the performance of microstrip lines from such measurements. The experimental results presented here represent the first direct measurements of picosecond pulse propagation along the Nb microstrip lines used for signal transfer in Josephson logic circuits. The results confirm that real Nb microstrip lines are suitable for transferring picosecond SFQ pulses over distances (up to several mm) comparable to the dimensions of the largest Josephson chips. Since attenuation is shown to be negligibly small below the gap frequency, the high frequency performance of these lines is limited not by dielectric loss but almost entirely by the frequency-dependent loss of Nb.

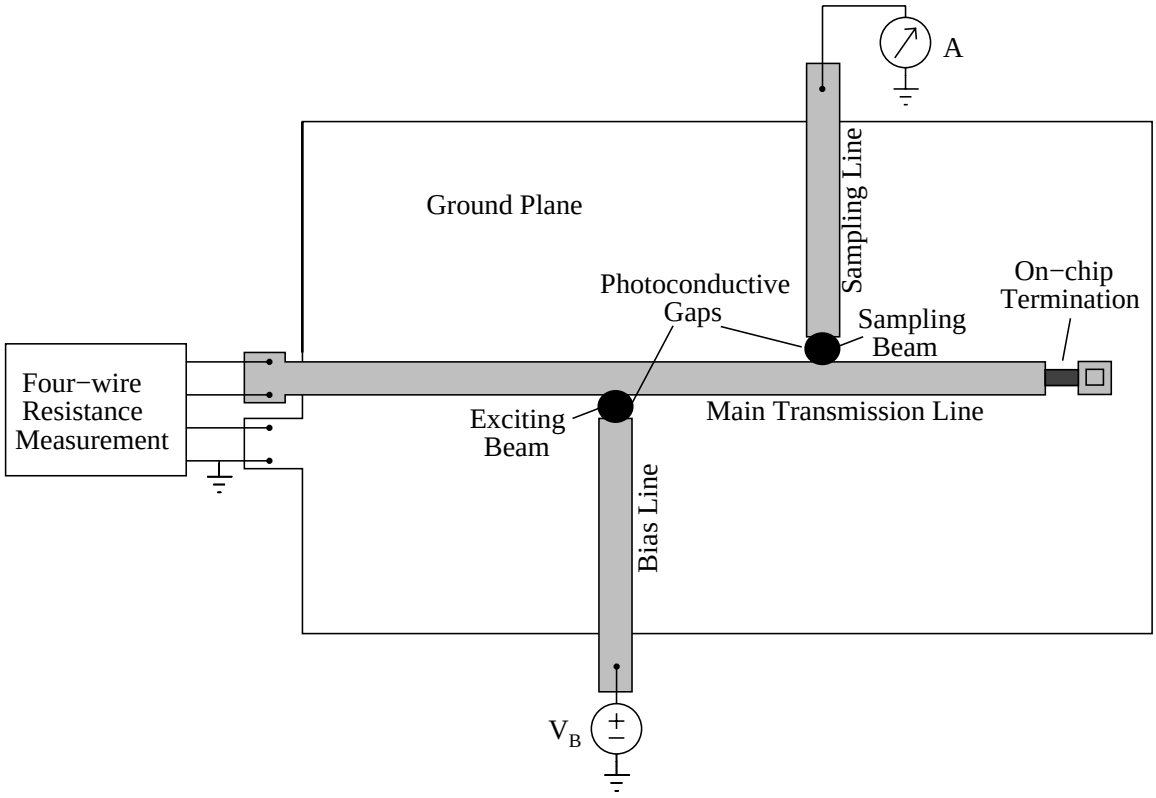
4.2 Description of Experiments

Picosecond photoconductors were used for generating and sampling the electrical pulses along the Nb microstrip lines. The basic circuit configurations employed in the experiments are illustrated in Figure 4-1. (Since the microstrip lines are only a couple μm wide and up to several mm long, the drawings in the figure are far from scale.) The circuit configuration shown in Figure 4-1(a) is similar to that depicted earlier in Figure 3-9, with the only difference being that the main transmission line is shortened so that the reflection from an on-chip termination can be observed within the time window of the measurement. Figure 4-1(b) shows an alternative circuit configuration in which the electrical pulse is generated with a photoconductive side gap instead of series gap. When the exciting beam illuminates a biased side gap, each laser pulse generates two electrical pulses on the main transmission line, one traveling to the left and one to the right. Because the injected current splits between the two arms of the transmission line, excitation with side gaps produces pulses only half as large as those produced by biased series gaps. On the other hand, the circuit configuration shown in Figure 4-1(b) has one important advantage over series gap excitation. Because the superconducting line to which the on-chip termination is connected is not broken with a series gap, the dc resistance of termination resistors can be easily measured with a four-wire measurement, as shown in the figure. The left arm of the main transmission line is sufficiently long that reflections of the leftward propagating pulse do not interfere with the measurement of the rightward propagating pulse and its reflection from the on-chip termination. In order to facilitate measuring their resistances, the reflections from all termination resistors were measured with the circuit configuration of Figure 4-1(b).

Figure 4-2 shows a cross-section of the Nb microstrip lines fabricated for the experiments. Test chips were cut from two separate wafer runs, which differed primarily in the choice of dielectric and the film thicknesses, which are listed in the figure caption. In each run, a Nb ground plane layer was first deposited on commercial silicon-on-sapphire substrates (with 500 nm thick silicon). After being patterned by reactive ion etching (RIE) in CF_4, the ground plane layer was covered with a dielectric. In the first run, SiO_2 was deposited by plasma-enhanced chemical vapor deposition; in the second, SiO was deposited by evaporation. Next a PtRh film was evaporated onto the oxide surface and defined by liftoff to make resistors with a sheet resistance close to 5 $\Omega/\Box$. Contact holes were then



(a)



(b)

Figure 4-1: Experimental microstrip circuit configurations with photoconductive gaps for generating and sampling picosecond electrical pulses. (a) Generation via series gap and sampling via side gap. (b) Generation and sampling via side gaps.

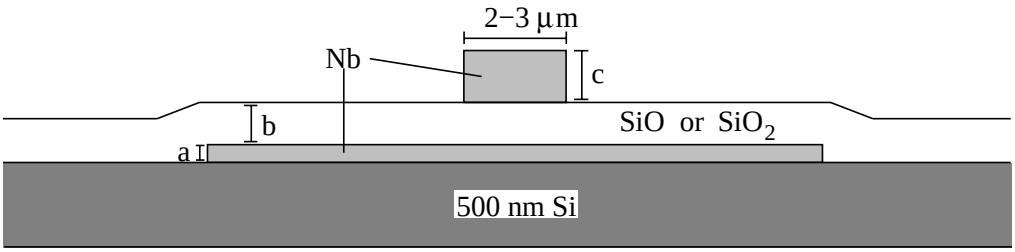


Figure 4-2: Cross-section of main transmission line. For the first wafer run, the dielectric was SiO_2, and the layer thicknesses were: a = 90 nm, b = 200 nm, and c = 300 nm. For the second wafer run, the dielectric was SiO, and the layer thicknesses were: a = 130 nm, b= 300 nm, and c = 450 nm.

formed by RIE in CHF_3 with a selectivity greater than 3:1 over Nb or Si. Finally, Nb was deposited on the wafer and patterned by CF_4 RIE to form the top level wiring. Minimum feature sizes were typically 2–3 μm. After the circuit structures were completed, the entire surface was implanted with two doses of O^+ ions, $10^{15}/cm^2$ at an energy of 200 keV and $10^{15}/cm^2$ at an energy of 100 keV. The dosages and energies were chosen to match those used in earlier work by Ketchen and his co-workers at IBM [37], who showed that such ion bombardment reduces the carrier lifetimes in the silicon layer of the substrate to less than 1 ps.

Since the photoconductive silicon layer is underneath the transmission line structure, holes in the ground plane and oxide layers are needed to make a photoconductive gap between the upper conductors of two microstrip lines. The layout of a typical side gap is presented in Figure 4-3. Because of its small size (18 μm$\times$18 μm) relative to the electromagnetic wavelength, the ground plane hole affects circuit dynamics minimally. Nonetheless, the photoconductive gap design shown in Figure 4-3 does have one important drawback. Because the ground plane is in contact with the silicon layer of the substrate, photocurrents flow not only between the microstrip lines (as intended), but also to the ground plane. Even when the focused laser beam is aimed at the center of the gap, the photoconductance between one microstrip line and the ground plane is about three times the photoconductance between the two microstrip lines. In the absence of parasitic coupling between microstrip lines, photocurrents to the ground plane do not affect the generation and detection of pulses on the main transmission line. As discussed later, though, if the bias line and sampling line are coupled, the spurious responses due to such coupling are magnified by photoconductivity to the ground plane.

Following dicing and wire bonding, the test chips were mounted on an insert inside a variable temperature dewar (Janis Research model 8DT) with an optical access window[1]. By adjusting the flow of cold helium vapor over the sample, the temperature was maintained at 3.6–4.2 K. The dewar was placed on an optical table with the home-built CPM

[1]The lack of magnetic shielding in this dewar was not a problem in these experiments since the picosecond photoconductors and the superconducting microstrip lines are not sensitive to the earth's magnetic field. Because the Josephson circuits discussed later in this thesis are very sensitive to magnetic field, they had to be tested with a magnetically shielded dewar without an optical access window.

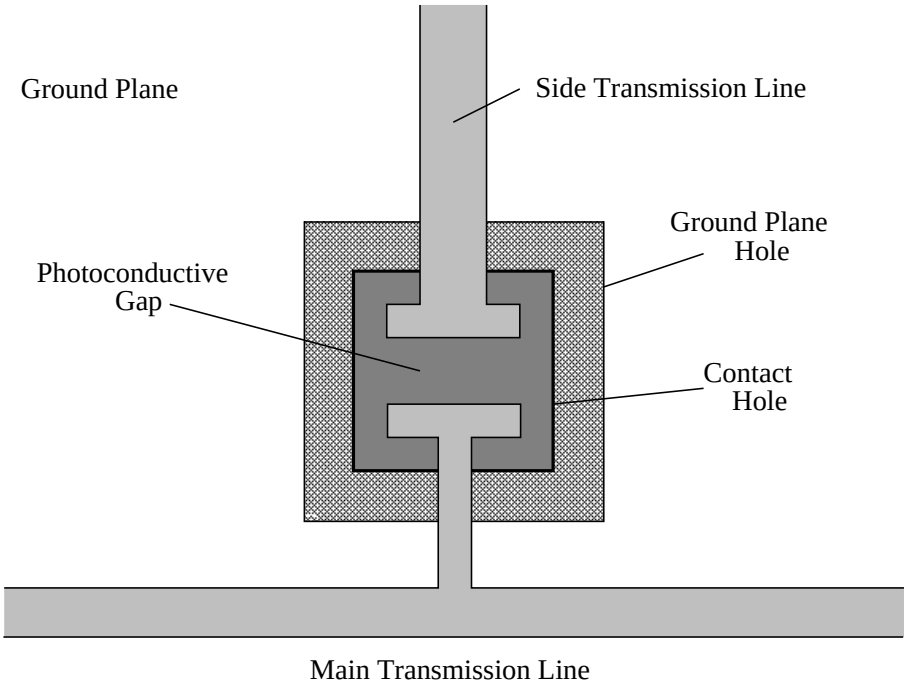


Figure 4-3: Layout of photoconductive side gap.

laser mentioned earlier in Section 3.1.1. This laser produced femtosecond ($\approx$ 100 fs) optical pulses with a wavelength of 620 nm at a repetition rate near 90 MHz. A non-polarizing 50/50% beamsplitter [92] was used to divide the laser pulses into the exciting and sampling beams, the delay between which was mechanically scanned by moving mirrors (specifically, an air-spaced retroreflector [92]) placed on a computer-controlled translation stage. The exciting and sampling beams were focused on the photoconductive gaps with lenses positioned just outside the optical window of the dewar. The exciting beam was modulated with a mechanical chopper (from Scitec Instruments Ltd.) at a frequency in the range of 0.4–1 kHz. To minimize heating of the superconducting chip, the average power in the exciting and sampling beams was attenuated to 0.7–0.8 mW and 1.4–1.7 mW, respectively[2]. A Hewlett-Packard 6115A precision power supply provided the bias voltage (typically 4–5 V) for the photoconductive gap generating the electrical pulses. The low frequency components of the current flowing through the sampling line were detected with an Ithaco 1211 current preamplifier, whose output was demodulated with a Stanford Research Systems SR510 lock-in amplifier synchronized to the mechanical chopper. The output of the lock-in amplifier was recorded with an IBM proprietary data acquisition card installed inside the same laboratory computer (IBM PC/AT) used to control the optical delay between the exciting and sampling beams. This delay was scanned several times over the time window of interest so that the SNR of the measurement could be improved by signal averaging; the total measurement time was typically in the range of 5–30 minutes. The test software running on the computer was not written for this project but was the legacy of several

[2]The laser pulses in the two attenuated beams had approximately equal energies. The exciting beam had a lower average power because it was chopped with a 50% duty cycle, while the sampling beam was not.

earlier experiments conducted at IBM, including those reported in [37, 107, 110, 111].

4.3 Experimental Results

Because of adhesion problems with the resistors on the first wafer run, many of the circuits with the SiO_2 dielectric could not be tested. With the exception of some results on pulse propagation (discussed next), all of the data presented in this chapter were taken on circuits with the SiO dielectric.

4.3.1 Pulse Propagation

Figure 4-4 demonstrates a 0.8 ps full-width-at-half-maximum (FWHM) pulse generated and detected by two photoconductive side gaps (Figure 4-1(b)). In the circuit tested, the two side gaps are located at the same position along the main transmission line, directly opposite each other. This arrangement permits measurement of the electrical pulse right at the point of excitation. The dielectric in this case is SiO.

The effect of propagation on pulse shape can be observed by testing circuits with different distances between the photoconductive gaps used for excitation and sampling. Figure 4-5 presents measurements of the picosecond pulses after various distances of propagation along microstrip lines with (a) SiO and (b) SiO_2 dielectrics. Even after only 200 μm of propagation, some pulse broadening is observed (1.0 ps FWHM for the circuits with SiO). After 6.5 mm of propagation, the pulse widths have increased to 1.8 and 2.7 ps FWHM for the microstrip lines with SiO and SiO_2, respectively. The greater dispersion of the microstrip lines with SiO_2 does not indicate inferiority of the SiO_2 dielectric; rather, it illustrates the effects of using thinner layers for the microstrip. For microstrip lines with dimensions typically used in Josephson integrated circuits, dispersive effects are smaller with thicker dielectric and superconducting layers [109]. The ground plane layer below the SiO_2 dielectric is particularly thin, with a thickness (90 nm) which is barely one London penetration depth for Nb [28]. As a picosecond pulse propagates along a microstrip line, a long oscillatory tail develops. This tail is due to strong dispersion at frequencies approaching the gap frequency of the superconductor [109].

4.3.2 Spurious Responses

Some of the initial experiments suffered from spurious responses which obscured the desired signals; an example of such an experiment is depicted in Figure 4-6. In this case, a biased side gap is used to generate pulses on the main transmission line. Because the main transmission line is long, the reflection of the rightward traveling pulse is not observed within the time window of the measurement. The leftward traveling pulse and its reflection off an unused series gap are sampled with another side gap. Since the unused series gap acts like an open circuit, the reflection coefficient should be near unity. The measured result is shown in Figure 4-7(a). The reflected pulse can be seen 17 ps after the incident pulse; since the unused series gap is 1 mm from the gap used for sampling, this delay corresponds to a propagation velocity of 118 μm/ps. To compare with theory, the inductance (per unit length) of the microstrip line was estimated with SC2D [112, 113], a two-dimensional inductance calculation tool for superconductors, and the capacitance (per unit length) was estimated with C2D [114], a two-dimensional capacitance calculation tool.

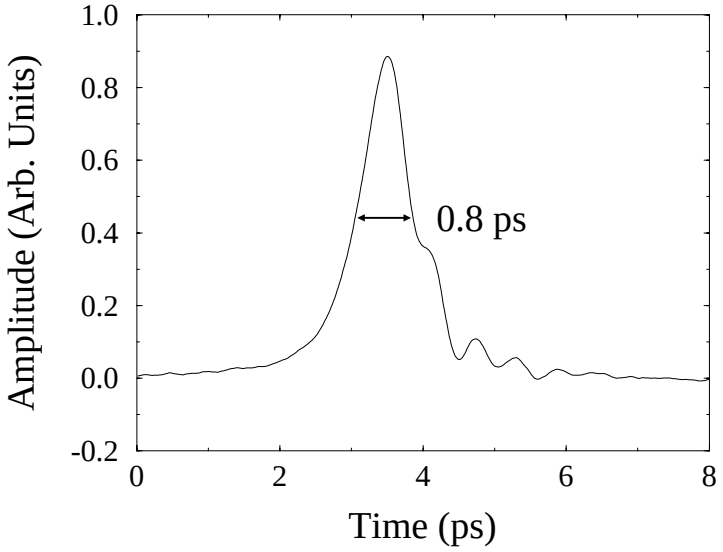


Figure 4-4: Electrical pulse detected at the point of excitation, before propagating along a microstrip line with SiO dielectric.

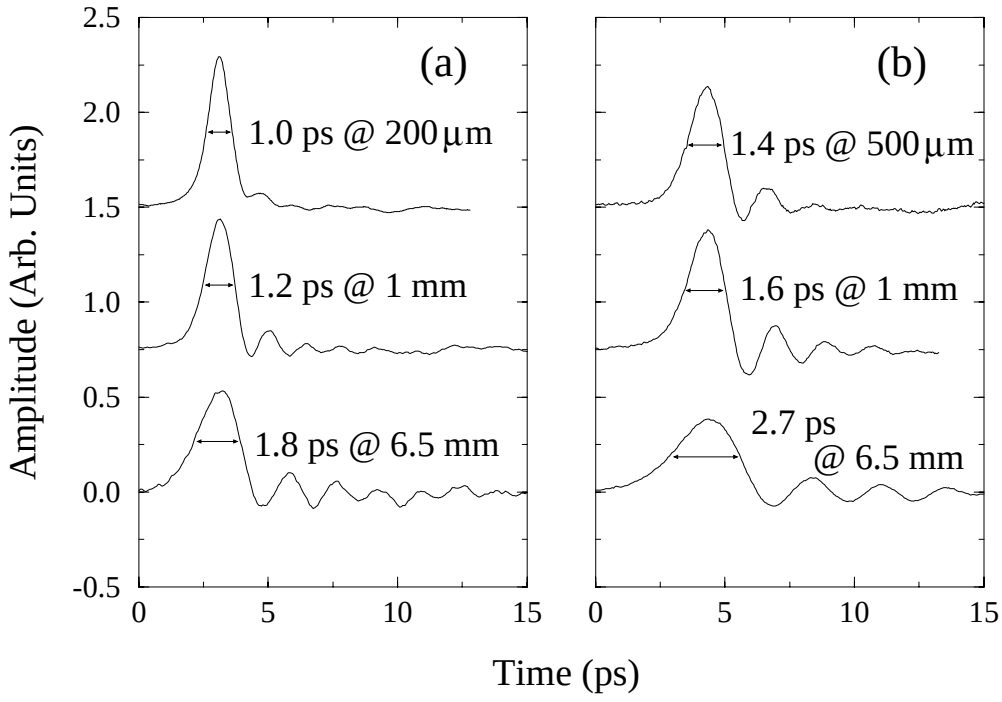


Figure 4-5: Electrical pulses after propagating along microstrip lines with (a) SiO and (b) SiO_2 dielectrics. For clarity, the waveforms are offset, and the time origins are shifted.

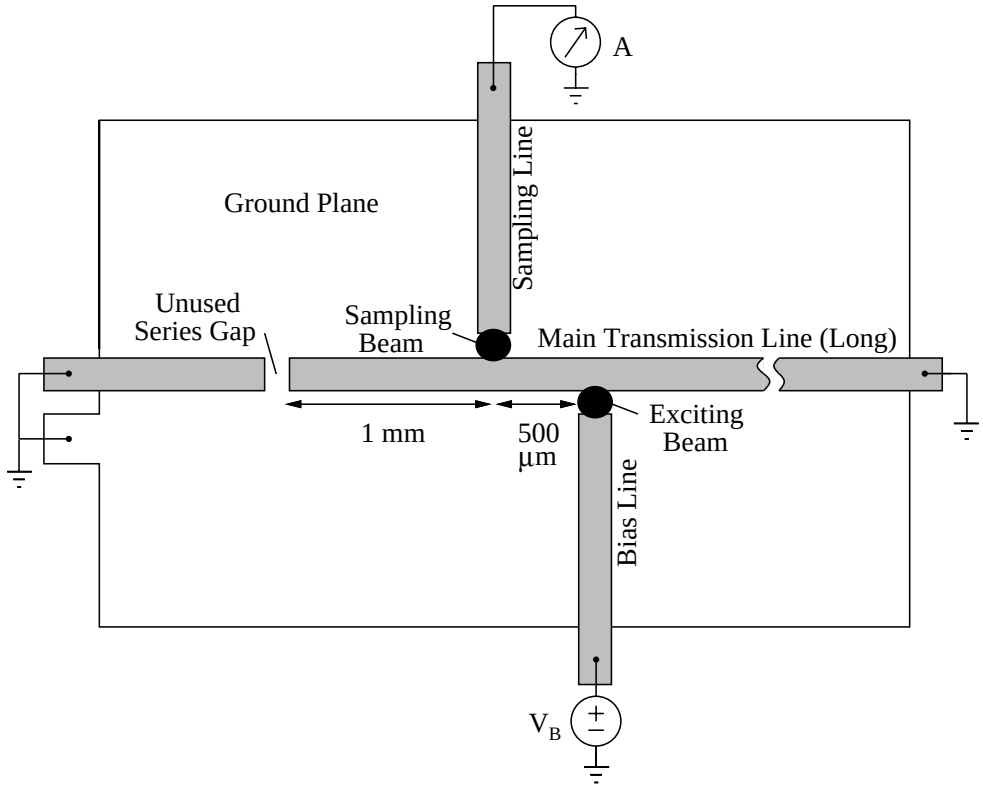


Figure 4-6: Microstrip circuit configuration exhibiting spurious response.

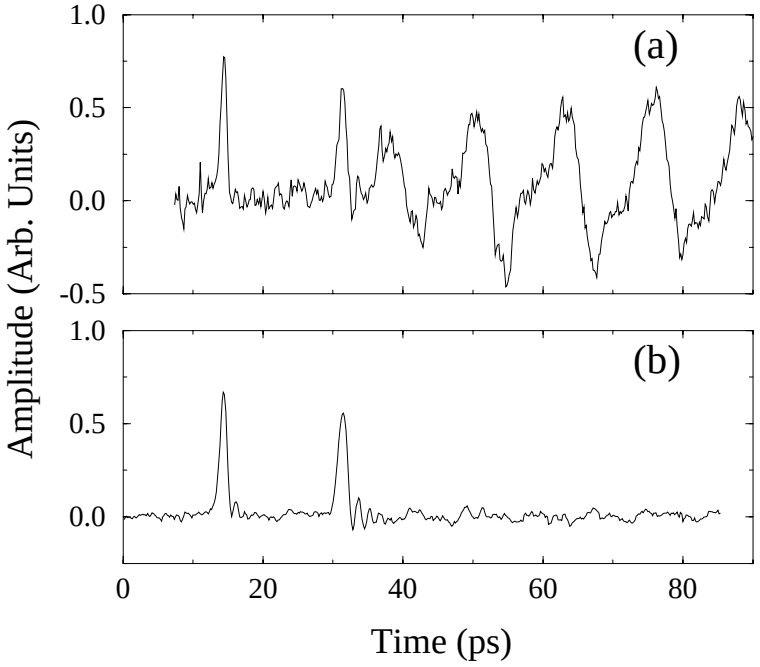


Figure 4-7: Measured response of the circuit of Figure 4-6 with (a) superconducting bias and sampling lines and (b) resistive bias and sampling lines.

Assuming a relative permittivity of 5.6 for the SiO dielectric, the propagation velocity of a 2 μm wide microstrip line was calculated from the estimated inductance and capacitance to be 117 μm/ps, within 1% of the measured value.

Unfortunately, the details of the reflection are obscured by a large, oscillatory signal; this oscillatory signal is a spurious response and results from unwanted coupling between the bias and sampling lines. When the biased side gap is struck by a laser pulse, a short negative pulse is launched on the bias line. Because the bond pad and wire at the end of the line are poorly matched to the line impedance, this pulse bounces back and forth along the bias line. The round trip delay expected for a pulse propagating up and down the bias line closely matches the period (13 ps) of the oscillation seen in Figure 4-7(a). Because the capacitance of the photoconductive gap is small, little of this signal is coupled onto the main transmission line. Instead, this signal is coupled to the sampling line *radiatively*; at these frequencies, the bonding pads and wires act as effective antennas. The coupling was particularly large in this experiment because the bias and sampling lines had identical lengths and therefore the same resonant frequencies. Photoconductivity to the ground plane, mentioned earlier, also increases the relative strength of the spurious response – in two ways, in fact. When a photoconductive gap is used for pulse generation, approximately three times more photocurrent is dumped to the ground plane than injected into the main transmission line; consequently, the negative pulse bouncing back and forth on the bias line is significantly larger than the positive pulse on the main transmission line. When a photoconductive gap is used as a sampling gate, the relatively large photoconductance between the sampling line and the ground plane makes the sampling gate more sensitive to voltage on the sampling line than to voltage on the main transmission line (by about a factor of four). Because photoconductivity to the ground plane both increases the amplitude of the pulse launched on the bias line and makes the sampling gate preferentially sensitive to voltage on the sampling line, even a moderate amount of coupling between the bias and sampling lines can produce a spurious response as large as the desired signal.

To study the details of transmission line reflections, it is necessary to suppress the spurious oscillations seen in Figure 4-7(a). An effective solution to the problem is to dampen the bias and sampling lines by making them resistive. The result of replacing the Nb bias and sampling lines with ones formed from PtRh is shown in Figure 4-7(b). Because of the loss due to resistance, the negative pulse on the bias line is dampened before it even reaches the bond pad and wire, and the spurious oscillations are no longer seen. This technique of dampening the bias line to avoid spurious responses was incorporated in the design of the optoelectronic interface used in later experiments with Josephson circuits.

4.3.3 Reflections from Terminations

The incident and reflected pulses for an open circuit termination and a short circuit termination are shown in Figures 4-8(a) and (b), respectively. The open circuit termination is tested with side gap excitation (Figure 4-1(b)), while the short circuit termination is tested with series gap excitation (Figure 4-1(a)). In both cases, the bias and sampling lines are formed from the resistive PtRh layer, and the distance between the termination and the side gap used for sampling is 500 μm. With a measured propagation velocity of 118 μm/ps, each reflected pulse is detected 8.5 ps after the incident pulse. As theory predicts, the reflection coefficient for the open circuit is 1, and the reflection coefficient for the short circuit is -1. Because of dispersion and attenuation at high frequencies, the reflected pulses are some-

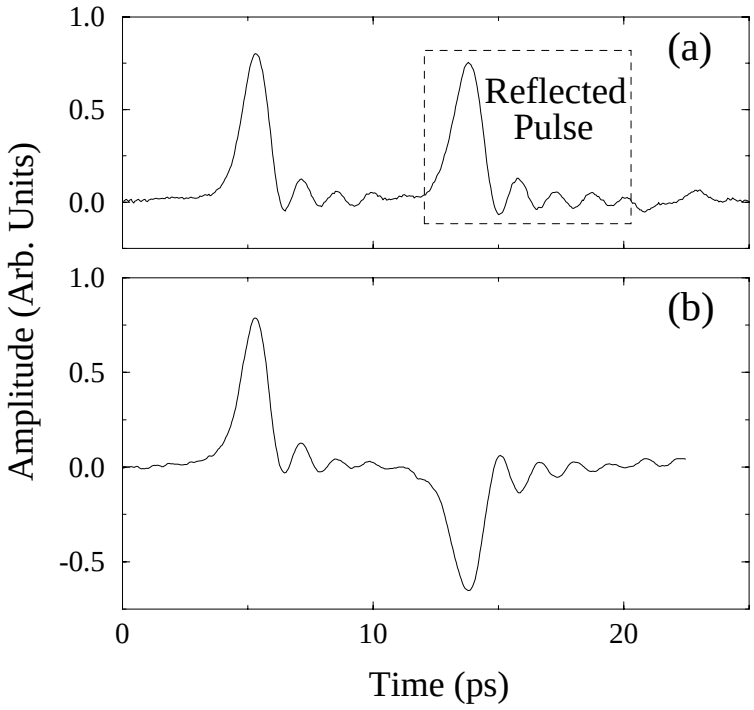


Figure 4-8: Incident and reflected pulses for (a) open and (b) short circuit terminations.

what broader than the incident pulses. Indeed, by comparing the Fourier transforms of the incident and reflected pulses, the frequency-dependent attenuation of the Nb microstrip line can be calculated; the result for the data of Figure 4-8(a) is plotted in Figure 4-9. (The time windowing used to define the reflected pulse is pictured in Figure 4-8(a) as a dotted box; the small oscillations after the dotted box represent a different reflection on the transmission line and are not included in the calculation.) The attenuation is seen to be small up to about 0.7 THz, which corresponds to the gap frequency of Nb. As predicted by theory [109], attenuation increases rapidly above the gap frequency of the superconductor. The drop in attenuation at 0.8 THz is not real, for at this frequency, the spectral amplitudes of the incident and reflected pulses are small enough to be dominated by measurement noise. The ripple in the attenuation curve below 0.6 THz is an artifact of time windowing. (Time windowing of the pulses assumes that the pulses do not overlap, which is only an approximation here.) It is worth noting that calculating attenuation from reflection measurements has one advantage over calculations based on measuring a propagating pulse at different locations along a transmission line, which was the method employed previously in [107]. Because the same photoconductive gap is used for sampling the incident and reflected pulses, variations in the sensitivity and speed of the picosecond photoconductors do not affect the accuracy of the calculation.

Finally, measurements of the reflections from various termination resistors are presented in Figure 4-10. Because the dc resistances of the termination resistors can be accurately measured (cf. Figure 4-1(b)), such reflection data provide a convenient way of determining the characteristic impedances of Nb microstrip lines. In all the experiments with termination resistors, the configurations and lengths of the microstrip lines were identical to those used to test the open circuit termination; consequently, each reflection is sampled 8.5 ps after

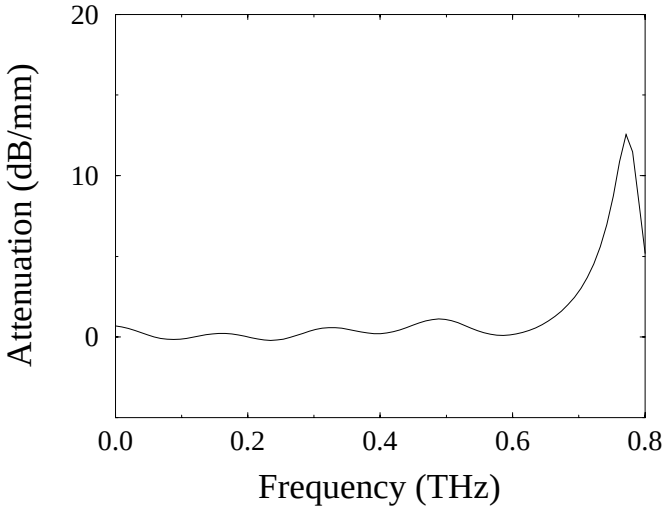


Figure 4-9: Frequency-dependent attenuation of Nb microstrip line.

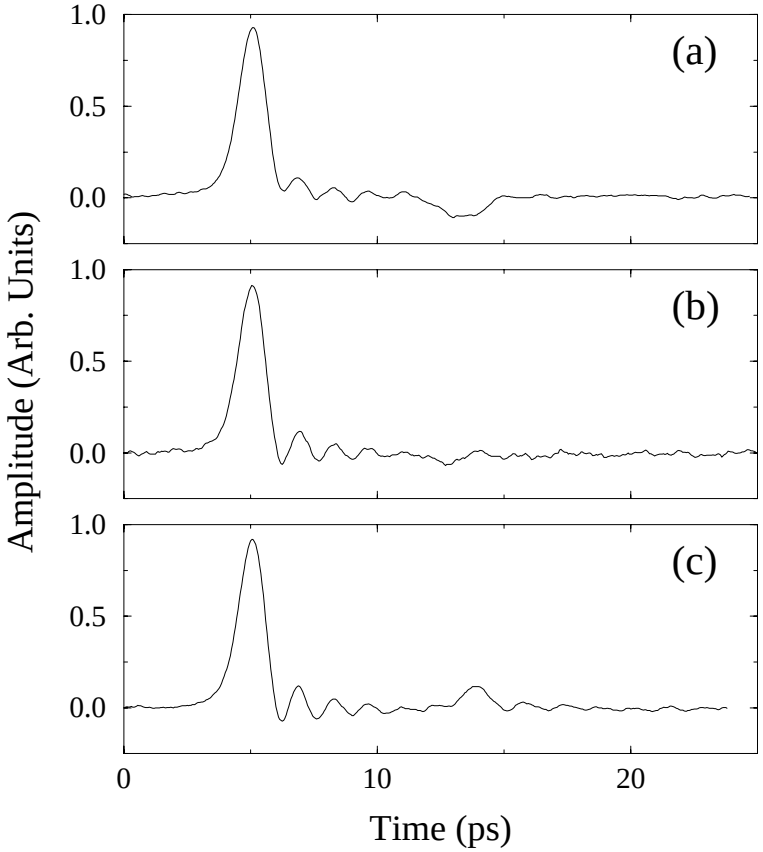


Figure 4-10: Incident and reflected pulses for resistive terminations. The measured values of the load resistors (R_L) and the widths (w) of the microstrip lines are: (a) $R_L = 16.4\ \Omega$ and w = 2 μm, (b) $R_L = 21.5\ \Omega$ and w = 2 μm, (c) $R_L = 22.0\ \Omega$ and w = 3 μm.

the incident pulse. For the data shown in Figures 4-10(a) and (b), the microstrip line is 2 μm wide. Calculations with SC2D and C2D show that the characteristic impedance Z_0 of such a line is close to 21 Ω. Accordingly, the reflection from a 16.4 Ω load resistor (smaller than Z_0) is a negative pulse, as shown in Figure 4-10(a). Better suppression of reflections is demonstrated in Figure 4-10(b); here the load resistor is 21.5 Ω, much closer to the line impedance. Because of its small size (12 μm long and 3 μm wide), the resistor behaves as a lumped element even at frequencies approaching 1 THz, and reflections due to reactance are minimal. For the data shown in Figure 4-10(c), the microstrip line is 3 μm wide. Since this wider line has a lower characteristic impedance ($Z_0 \approx 15.5$ Ω), the 22.0 Ω load resistor is larger than Z_0, and the reflected pulse is positive.

Chapter 5

Optical Clocking Setup

A major effort in this research project was the development of a highly versatile optical clocking system for testing superconducting circuits at multi-GHz frequencies without encumbrance by bandwidth limitations of the electrical interface to room-temperature electronics. This chapter presents the optical setup that was constructed for generating picosecond optical pulses at repetition rates up to 20.6 GHz and for delivering these pulses to the superconducting chip, on which an integrated MSM photodiode converts the optical pulses to fast electrical pulses that trigger the Josephson circuits with subpicosecond timing accuracy. The first two sections of the chapter describe the basic structure and functional capabilities of the optical clocking system. The remaining sections of the chapter then cover the detailed implementation, alignment, and calibration of this complex optical setup. The next chapter demonstrates triggering of simple Josephson circuits with the optical clocking system. The optical clocking system was later used for external triggering of the superconducting bandpass $\Delta\Sigma$ modulator whose experimental results are discussed in Chapter 12.

5.1 Overview of Optical Clocking System

The major components of the optical clocking system are depicted in Figure 5-1. Because of its abundant power and excellent stability, a Spectra-Physics Tsunami (model 3960) mode-locked Ti:sapphire laser is used to generate picosecond ($\approx$ 1 ps) optical pulses with a wavelength of 940 nm at a repetition rate near 80.6 MHz. As discussed in Section 3.3.1, the pulse-to-pulse timing jitter of this laser is less than 200 fs rms. Since the silicon MSM photodiode integrated with the Josephson circuitry provides the fastest response when illuminated by short wavelength light, the 940 nm optical pulses emitted by the laser are converted to 470 nm optical pulses by second-harmonic generation (SHG). As explained in Section 3.1.3, the 80.6 MHz pulse repetition rate of the laser is multiplied up to 20.6 GHz by an optical "pulse splitter". The basic operation of this pulse splitter, which is realized with an arrangement of beamsplitters and optical delay lines, is described in the next section. By blocking and unblocking different beam paths in the pulse splitter, a variety of pulse patterns and clock rates can be synthesized.

The output of the pulse splitter is coupled into a single-mode optical fiber, which delivers the optical pulses to the Josephson chip at the bottom of a magnetically shielded liquid

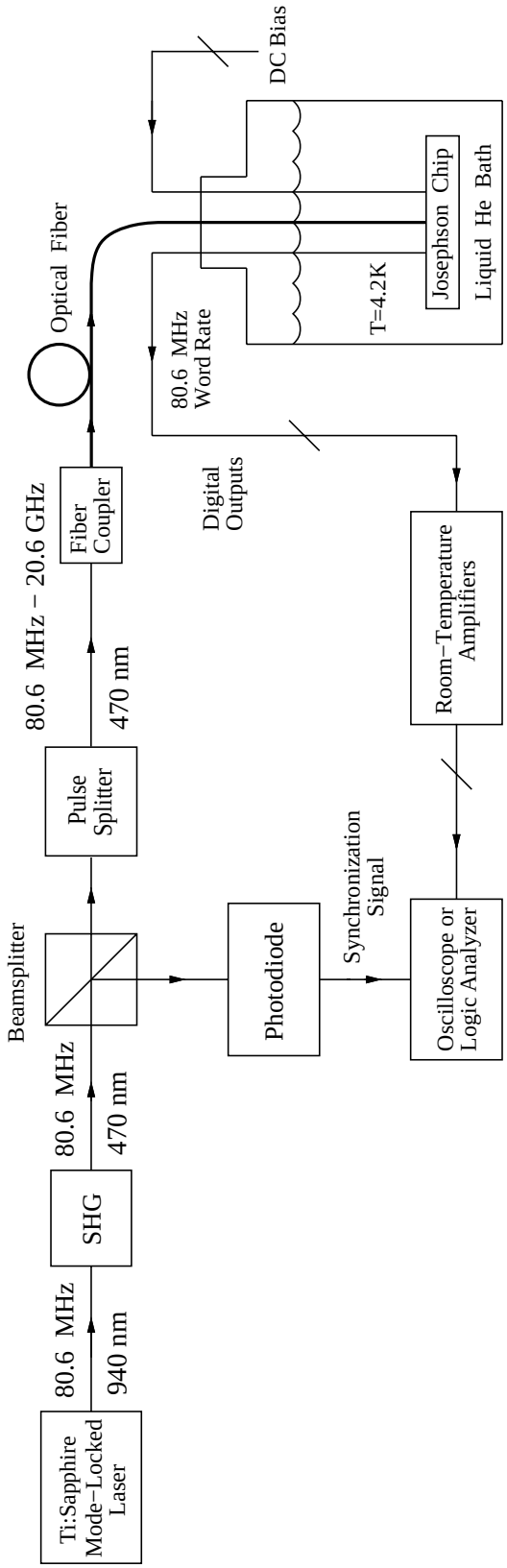


Figure 5-1: Block diagram of optical clocking system.

helium dewar. A crucial advantage of optical over electrical interfacing is the low loss and dispersion of this fiber; even after 7.5 meters of fiber, each optical pulse is only broadened to 3 ps full-width-at-half-maximum (FWHM). On the Josephson chip, the MSM photodiode converts the optical pulses into picosecond electrical pulses, which trigger RSFQ circuitry.

To evaluate its operation, the outputs of the circuit under test are read out electrically over coaxial cables at a relatively slow rate: 80.6 MHz in the example of Figure 5-1, and twice that (161 MHz) in the case of the optically triggered bandpass $\Delta\Sigma$ modulator demonstrated in Chapter 12. The modest readout rates reduce the bandwidth requirements on the room-temperature amplifiers that boost the small output voltages of the Josephson circuits up to signal levels which are easily measured with standard test instruments such as oscilloscopes or logic analyzers. For testing a Josephson circuit which is purely digital in function, the pulse splitter may be operated in "burst mode" (explained in the next section), in which optical triggering is disabled for a large fraction of each laser period so that readout of circuit states can be performed. Because all timing in the optical clocking system is derived from the laser repetition rate, an electrical signal suitable for synchronizing test instruments can be obtained by dividing the original laser beam with a beamsplitter and illuminating a high speed photodiode with one of the separated beams.

5.2 Basic Operation of Pulse Splitter

The basic operating principle of the optical pulse splitter can be appreciated by examining a simple pulse rate doubler, shown in Figure 5-2. In this scheme, the beam from the mode-locked laser is split into two beams and then recombined into one by means of two non-polarizing beamsplitters [92]. The beamsplitters are selected to have 50% transmittance and 50% reflectance so that the optical power is divided equally between the two beam paths, and the pulses in the recombined output beam have equal energies. If the mirror positions are adjusted so that the difference in delays (Δt) of the two paths is exactly half of the laser period T, the recombined beam forms a periodic pulse train with a repetition rate twice that of the incoming laser beam.

This design for an optical pulse rate doubler is not, however, power efficient. Each of the beams arriving at the second beamsplitter is divided equally into two beams following paths A and B. Since the beam along path B is not used (blocked, for instance, by a beamstop), half of the optical power is lost upon recombining the beams to form the output beam. Ignoring the reflection losses of real optical components, this pulse rate doubler has an ideal transmission efficiency of only 50%. Such low efficiency precludes cascading pulse rate doublers to achieve much higher pulse rate multiplication factors. For a cascade of N pulse rate doublers, the transmission efficiency from input to output would only be 2^{-N}, which is unacceptably low in many applications, including the optical clocking system considered here (with N=8).

A pulse rate doubler with much better transmission efficiency is obtained by replacing the non-polarizing beamsplitters with polarizing beamsplitters [92], as suggested in Figure 5-3. A polarizing beamsplitter separates the two orthogonally polarized components (traditionally named s and p) of an incident laser beam into two perpendicular output beams. The s-polarized component is completely reflected at a 90° angle, while the p-polarized component is completely transmitted through the beamsplitter without deviation of direction. As mentioned earlier in Chapter 3, the output of a mode-locked laser is typi-

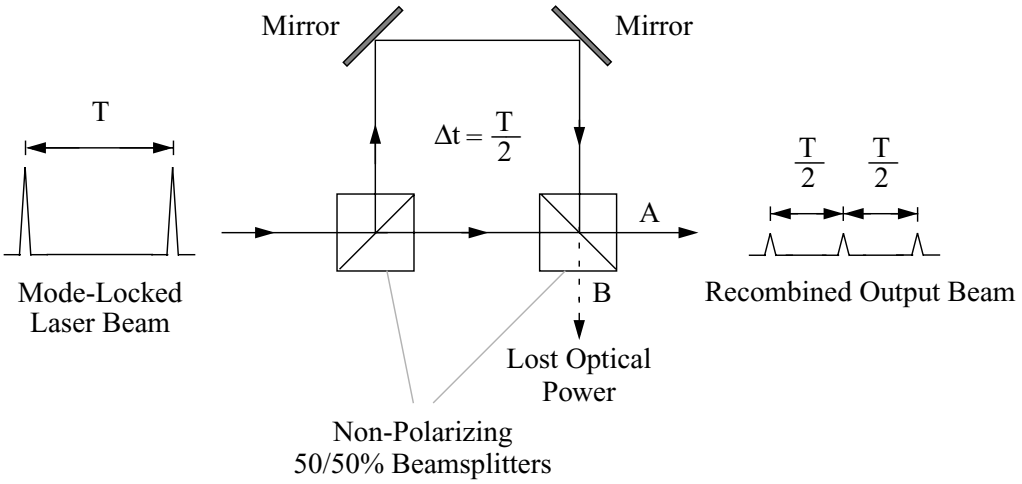


Figure 5-2: Optical pulse rate doubler.

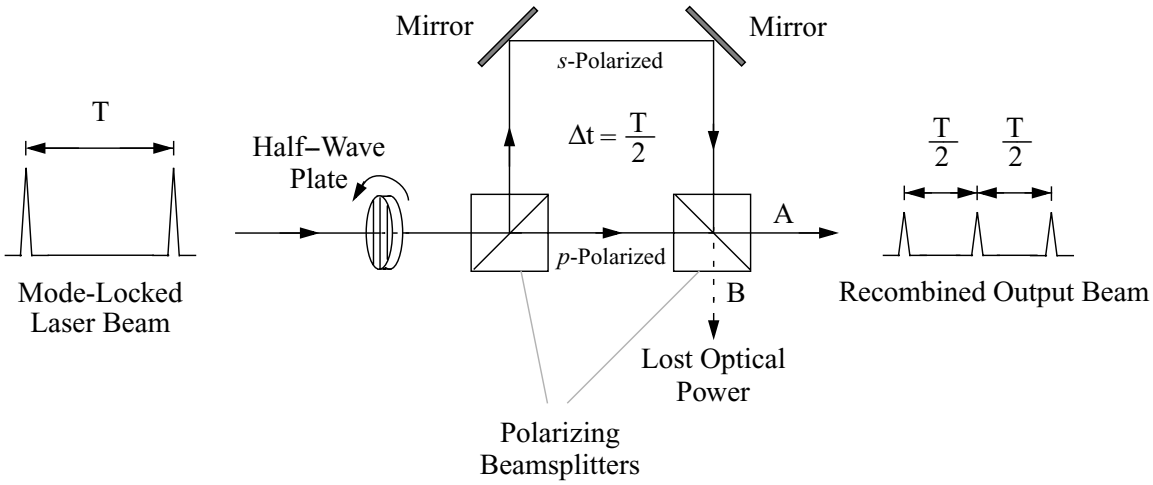


Figure 5-3: Optical pulse rate doubler with polarizing beamsplitters for higher transmission efficiency.

cally linearly polarized. The division of optical power between the two beam paths can be varied by rotating the polarization of the incoming laser beam with a half-wave plate [92]. Equal division of power is obtained when the polarization of the incident light is oriented at a 45° angle with respect to the polarizing axes of the beamsplitter. The advantage of using polarizing instead of non-polarizing beamsplitters is the high power efficiency with which the separated beams can be recombined. Since the beam following the longer path is *s*-polarized, it is completely reflected by the second polarizing beamsplitter in the direction of the output beam (path A). Similarly, the *p*-polarized beam following the shorter path is completely transmitted through the second polarizing beamsplitter in the direction of the output beam (path A). Ignoring the imperfections of real optical components, no beam is emitted along path B, no optical power is wasted, and the ideal transmission efficiency of this pulse rate doubler is 100%. In practice, the output beams of a real polarizing beamsplitter are highly but not perfectly polarized, so some optical power is emitted in the direction of path B and lost. This type of loss can be minimized by using polarizing beamsplitters with high polarization purity, commonly specified as an "extinction ratio". With an extinction ratio greater than 200:1, less than 0.5% of the optical power is lost through path B, which is low enough that the transmission efficiency of the pulse rate doubler is usually limited by the reflection losses of its optical components.

The high transmission efficiency of pulse rate doublers based on polarizing beamsplitters allows them to be cascaded to make more complex pulse splitters. Figure 5-4 depicts in simplified form the pulse splitter constructed for the optical clocking system. (More detailed descriptions of its implementation are given in later sections of this chapter.) Eight cascaded stages of pulse rate doublers are used to multiply the pulse repetition rate by 2^8=256 (from 80.6 MHz to 20.6 GHz). Because of the pulse rate doubling achieved by each stage, the path delay differences $\Delta t_1, \Delta t_2, \ldots, \Delta t_8$ are binary scaled. To ensure subpicosecond timing error for each of the pulses produced by the pulse splitter, the path delays of the optical setup must be calibrated very precisely. Section 5.5 explains how the path delay differences $\Delta t_1, \Delta t_2, \ldots, \Delta t_8$ were each calibrated to better than 0.1 ps accuracy through a series of optical cross-correlation measurements. Sections 5.4 and 5.6 discuss the procedures used for optical alignment of the pulse splitter and the details of adjusting the half-wave plates so that the optical power is divided nearly equally among the various beam paths.

If all of the beam paths in the pulse splitter are used, a continuous 20.6 GHz pulse train is generated. Alternatively, some of these pulses can be suppressed by blocking one or more of the beam paths. For example, if one of the divided beams in stage 8 is blocked, as suggested in Figure 5-4, every other pulse is eliminated, and the clock rate effectively falls to 10.3 GHz. More generally, if the last K stages of the pulse splitter are disabled in this fashion, the clock rate drops by a factor of 2^K. The pulse splitter also permits burst mode operation. If stage 1 is disabled by blocking one of its beams, a burst of 128 pulses at a 20.6 GHz clock rate is produced, after which no pulses occur for about 6.2 ns (the remainder of the laser period). During the time between pulse trains, relatively low speed readout operations can be performed. Shorter pulse trains can be realized by blocking more beam paths.

The following shorthand notation is used to specify the configuration of the pulse splitter. For each stage, the beam configuration is denoted by one of three letters. An "S" denotes that only the shorter of the two beam paths is used (i.e., the longer is blocked), an "L" denotes that only the longer is used, and an "X" denotes that both the longer and shorter

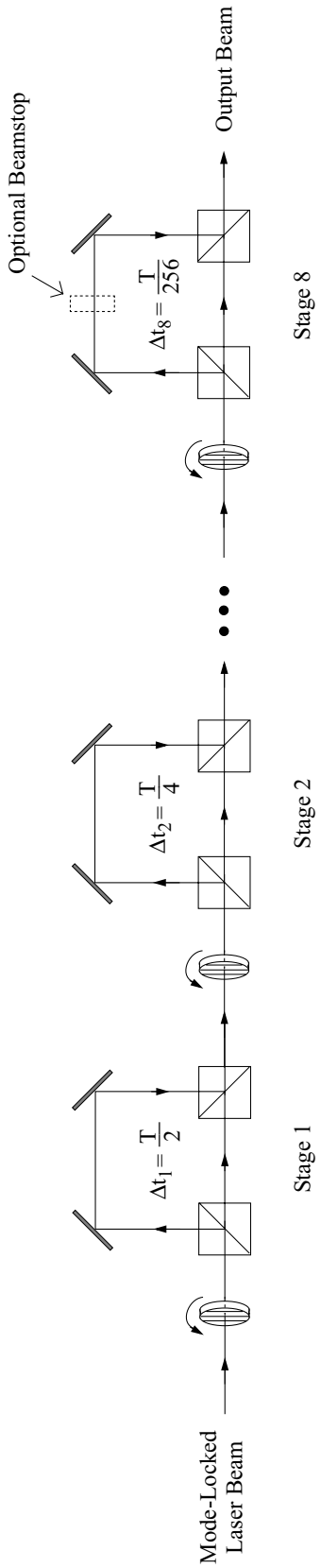


Figure 5-4: Implementation of pulse splitter as a cascade of pulse rate doublers.

are used. The configuration of the entire pulse splitter is then described by a code of eight letters. For instance, SSSSSXSX indicates that both the shorter and longer beam paths are unblocked in stages 6 and 8, but only the shorter beam paths are used in the rest of the stages. If, according to the RSFQ basic convention described in Section 2.2.7, the arrival of a pulse during a period of the 20.6 GHz clock represents a "1" bit, and the absence of such a pulse represents a "0" bit, the output of each stage of the pulse splitter can be described as a 256-bit word repeating at the laser repetition rate. Moreover, these words can be easily calculated from the pulse splitter configuration by noting the following relationship between the words generated by successive stages:

$$Y_n = \begin{cases} Y_{n-1} & \text{if } n\text{th stage} = \text{S}, \\ Y_{n-1} >> 2^{8-n} & \text{if } n\text{th stage} = \text{L}, \\ Y_{n-1} + (Y_{n-1} >> 2^{8-n}) & \text{if } n\text{th stage} = \text{X}, \end{cases} \tag{5.1}$$

for $1 \leq n \leq 8$, where Y_n is the word generated by the nth stage, and $Y_{n-1} >> 2^{8-n}$ signifies Y_{n-1} bit-shifted to the right by 2^{8-n} bits. Y_0 is the word corresponding to the laser pulse train itself: $1000\ldots0$. Equation 5.1 can be applied iteratively to obtain the output pattern for any pulse splitter configuration. As an example, for a configuration of SSSSSXSX, Y_1=Y_2=Y_3=Y_4=Y_5=$1000\ldots0$, Y_6=Y_7=$1000100000\ldots0$, and Y_8=$1100110000\ldots0$. Note how the pulse splitter can produce short bursts of pulses with nonuniform spacing between pulses.

5.3 Implementation Details

5.3.1 Second-Harmonic Generation Optics

Figure 5-5 shows in detail the second-harmonic generation optics used for converting the 940 nm laser pulses to 470 nm optical pulses. The 470 nm (visible blue) light is generated inside a BBO crystal, which was purchased from CSK Optronics, Inc. and has dimensions of 5 mm × 5 mm × 2 mm (with the last dimension being its thickness). As discussed in Section 3.1.2, the conversion efficiency with the BBO crystal is improved by focusing the incident beam more tightly in one transverse direction than in another. In this case, the incident beam is focused in the horizontal direction by cylindrical lens CL1 with a focal length of 100 mm and in the vertical direction by cylindrical lens CL2 with a focal length of 25.4 mm. Both CL1 and CL2 are placed on micrometer-driven translation stages (from Newport Corporation) so that their distances from the BBO crystal can be precisely adjusted for optimum focusing.

The other cylindrical lenses are used for collimating the light emitted from the BBO crystal. The output beam is collimated in the vertical direction by cylindrical lens CL3 and in the horizontal direction by cylindrical lenses CL4 and CL5. These last two lenses form a compound lens having an effective focal length f_{eff} given by [115]

$$f_{eff} = \frac{f^2}{2f - d}, \tag{5.2}$$

where f is the focal length (75.6 mm) of both CL4 and CL5, and d is the distance between them. A long effective focal length is achieved if $d \approx 2f$. The distance from the BBO

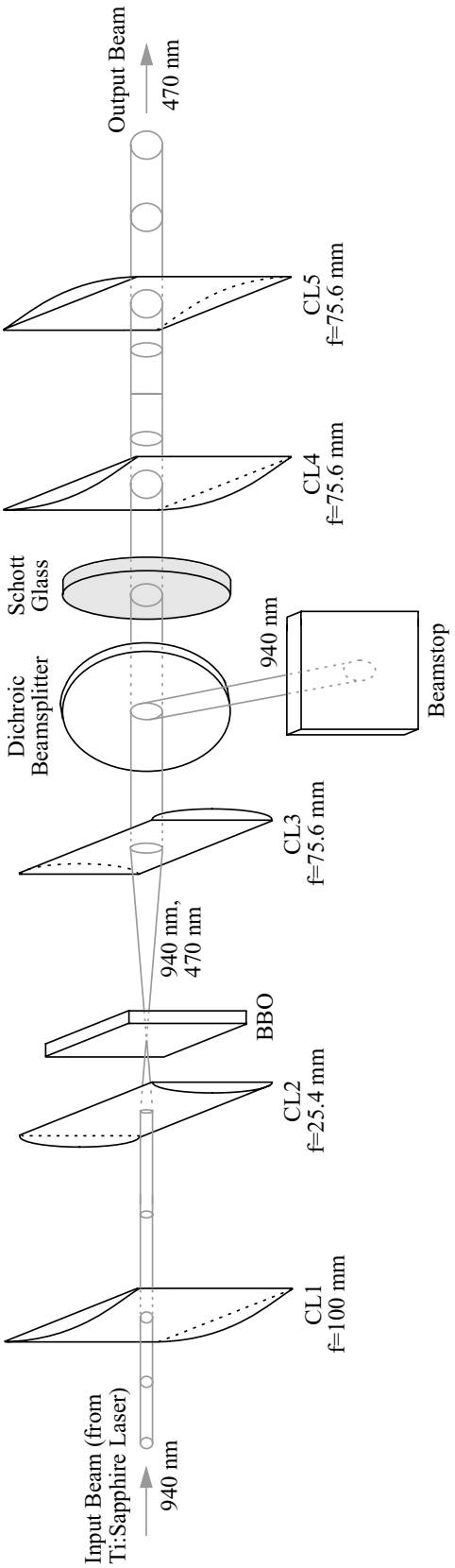


Figure 5-5: Experimental arrangement of second-harmonic generation optics.

crystal to this compound lens is set so that the recollimated output has a symmetric beam shape (i.e., with equal vertical and horizontal dimensions). Even with optimum placement of the lenses, though, the output beam profile is not perfectly round but appears somewhat triangular in shape when viewed with a CCD camera. Such poor spatial quality of the output beam, often encountered when the input beam is focused for highest conversion efficiency [116], reduces the efficiencies with which the various beams of the optical clocking setup can be coupled into a single-mode optical fiber[1]. To facilitate adjustment of output beam collimation, CL3 and CL5 are placed on micrometer-driven translation stages (from Newport Corporation).

All of the cylindrical lenses were purchased from Newport Corporation. To maximize the optical output power, they were ordered with anti-reflection coatings covering the following wavelength ranges: 650–1000 nm for CL1 and CL2, and 430–700 nm for CL3, CL4, and CL5. Similar anti-reflection coatings were applied to the hermetically sealed housing for the BBO crystal.

The fundamental beam is removed from the second-harmonic output with two stages of color filtering. Over 99.5% of the fundamental beam power is rejected with a dichroic beamsplitter (from CVI Laser), which has high reflectance at 940 nm and high transmittance at 470 nm. The fundamental beam power transmitted through the dichroic beamsplitter is low enough that it can safely be absorbed with Schott glass (Newport FSR-BG40) having a blue bandpass characteristic. After passing through all the collimating lenses and color filters, the output beam has a maximum average power of about 80 mW when the average input power is about 1 W. The conversion efficiency is therefore about 8%.

Since the focal length of CL3 and the effective focal length of compound lens CL4–CL5 are greater than the focal lengths of the focusing lenses CL1 and CL2, the recollimated output beam has a diameter (6 mm) which is about three times the input beam diameter (2 mm). The expansion in beam diameter is advantageous in reducing the effects of diffraction. Because of diffraction, the diameter of a collimated laser beam slowly increases with distance of propagation. For a laser beam with a Gaussian transverse intensity distribution, the beam radius[2] w increases with distance z as [118]

$$w(z) = w_0 \sqrt{1 + \left(\frac{z}{z_R}\right)^2}, \tag{5.3}$$

where w_0 is the radius of the beam at its "waist" (i.e., at $z = 0$, before spreading has

[1] In retrospect, better output beam quality could probably have been achieved by using a different nonlinear crystal for second-harmonic generation. Most of the distortion in the output beam profile is due to birefringence, which causes the fundamental and second-harmonic beams to separate spatially as they propagate through the crystal, a phenomenon known as "walk-off" [116]. Better output beam quality could be obtained with a crystal such as LBO, which has smaller walk-off than BBO [117]. While the smaller nonlinear susceptibility coefficient of LBO [88] might moderately decrease the conversion efficiency of second-harmonic generation, the improvement in beam quality would likely increase the fiber coupling efficiencies enough that the maximum optical power that could be delivered to the superconducting chip would be at least as high as in the present setup.

[2] For a Gaussian beam, the radius w is commonly defined to be the distance from the center of the beam at which the optical intensity has fallen to $1/e^2$ of its value at the center. The diameter, of course, equals $2w$.

occurred), and z_R is the "Rayleigh range", defined for a given wavelength λ to be

$$z_R \equiv \frac{\pi w_0^2}{\lambda}. \tag{5.4}$$

Equation 5.3 shows that the beam spreading due to diffraction is small over distances less than z_R. Since z_R is proportional to w_0^2, expanding the beam diameter increases the distance over which diffraction effects are negligible. This advantage is particularly important for achieving good performance with the optical pulse splitter. Since the various beam paths within the pulse splitter differ substantially in length, diffraction must be minimal for the beams in the recombined output to have the same diameters and divergences. Because of its inferior beam quality, the second-harmonic output beam is a poor approximation to an ideal Gaussian beam, and its spreading due to diffraction cannot be accurately calculated with Equations 5.3 and 5.4. Nonetheless, the expansion in beam diameter does help reduce undesirable diffraction effects.

5.3.2 Pulse Splitter Stage Layouts

Figure 5-6 presents the optics layout used for pulse splitter stages 2 through 4. A couple of practical advantages justify the extra complexity of this optical arrangement compared with that shown in Figure 5-3. The use of four mirrors instead of two in the longer beam path allows its delay and its output beam alignment to be adjusted nearly independently. The delay of this path is manually varied by displacing mirrors M1 and M2, which are placed on a micrometer-driven translation stage, while its output beam is aligned with the one from the shorter "straight-through" path by turning mirrors M3 and M4. Since the orientations of M1 and M2 are always fixed at a 45° angle of incidence, displacing them a short distance (up to a few mm) has little effect on output beam alignment.

The addition of half-wave plates HW2 and HW3 to the stage provides an extra degree of freedom in balancing the optical power in the shorter and longer paths. In the absence of alignment errors, diffraction effects, and optical component imperfections, this extra degree of freedom would not be needed, as equal division of power between the two paths could be achieved by rotating the polarizations of the optical pulses in the input beam with half-wave plate HW1. A point that needs to be stressed here is that the optical pulses in the input beam do not have a single polarization. Optical pulses which followed the shorter beam path in the previous stage are *p*-polarized while those which followed the longer beam path in the previous stage are *s*-polarized. Nonetheless, if HW1 is adjusted so that both input polarizations are rotated by 45°, each optical input pulse would ideally be divided equally between the shorter and longer beam paths. In practice, however, the optical pulses following the shorter and longer paths may suffer different reflection losses and, due to diffraction or minor beam misalignment, may be coupled with different efficiencies into the single-mode fiber which delivers the pulses to the superconducting chip. The resulting variations in the energies of the optical pulses reaching the chip often cannot be compensated by readjusting HW1 alone. For instance, assume that the reflection losses of mirrors M1 through M4 reduce the energies of all the pulses following the longer beam path. If one turns HW1 so that the input polarizations are rotated by more than 45°, a *p*-polarized input pulse would be divided so that more of its energy is delivered to the longer path and less to the shorter path (which is the desired effect), but an *s*-polarized input pulse would

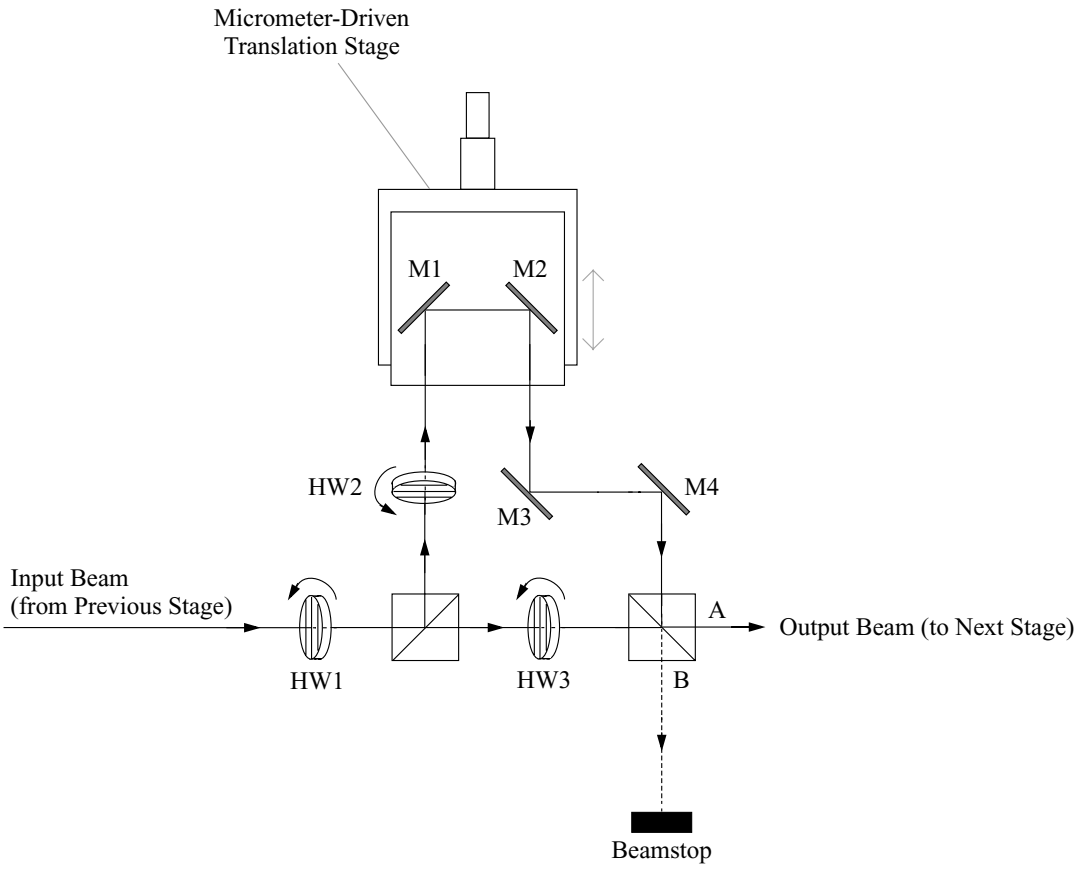


Figure 5-6: Optics layout used for pulse splitter stages 2 through 4.

be divided so that less of its energy is delivered to the longer path and more to the shorter path (which is the *opposite* of the desired effect). Thus, adjusting HW1 is not helpful for compensating this type of power imbalance. The degree of freedom needed to accomplish such compensation is obtained by turning HW2 and HW3.

HW2 and HW3 operate as variable attenuators for the two beam paths. If both of these half-wave plates are turned so that they do not rotate the polarizations of the beams passing through them, they have no effect on the power balance of the stage. If HW2 is turned so that it does rotate the polarization of the beam following the longer path, this beam is no longer purely s-polarized. Since its p-polarized component is transmitted through the second polarizing beamsplitter of the stage (along path B) and dumped to a beamstop, this beam is attenuated. Similar attenuation can be applied to the beam following the shorter path by turning HW3 so that the beam is no longer purely p-polarized. The attenuation accomplished with HW2 and HW3 is independent of the input pulse polarization. Returning to the example of the last paragraph, one can easily compensate for the reflection losses of mirrors M1 through M4 by turning HW3 so that the beam following the shorter path is attenuated by a factor equal to the mirror losses. In general, HW2 and HW3 are never both turned to provide polarization rotation at the same time, as adding attenuation to both beam paths is not necessary for power balancing and merely reduces the transmission efficiency of the stage. Since it was not known prior to operation of the pulse splitter which

half-wave plate would not be needed for polarization rotation, both HW2 and HW3 were included in the construction of each stage. Inserting a half-wave plate in one of the beam paths on an "as needed" basis is not practical because it alters the optical path delay.

The optical components of each pulse splitter stage were carefully selected to maintain high transmission efficiency. The mirrors (from Melles Griot) are a multilayer dielectric type optimized for wavelengths near 470 nm and a 45° angle of incidence. The minimum reflectance of these mirrors is 99.3% for p-polarized light and even higher for s-polarized light. The polarizing beamsplitters (Spindler & Hoyer model 335651) have a transmittance in excess of 99% for p-polarized light, a reflectance in excess of 99% for s-polarized light, and an extinction ratio greater than 200:1. The half-wave plates (Special Optics model 8R-9015) are an achromatic type with anti-reflection coatings covering a wavelength range of 400-700 nm. The transmittance of each half-wave plate is specified as greater than 98%.

Other layouts of the optical components are more convenient for constructing pulse splitter stages in which the difference in delays of the two beam paths is particularly large or small. In the layout shown in Figure 5-6, all of the extra distance of the longer path is in a direction perpendicular to that of the shorter "straight-through" path. Such a layout becomes awkwardly wide and occupies excessive area on the optical table if used for the first pulse splitter stage, in which the difference in path lengths must be almost 1.9 meters to achieve a delay difference of $T/2$ (≈ 6.2 ns). A more compact layout of stage 1 is obtained without increasing the mirror count by "folding" the longer path so that much of its extra distance is in a direction parallel to the shorter path, as shown in Figure 5-7. Because the beam entering the first stage of the pulse splitter only has a single polarization, just one half-wave plate (HW1) is needed to balance the optical power in the shorter and longer paths.

The physical size of bulk optical components prevents them from being arranged very close to each other and places a lower limit on the path delay differences that can be realized with the optics layouts shown so far. As shown in Figure 5-8, smaller path delay differences are achieved by increasing the length of the shorter path with the addition of four mirrors (M5 through M8). Arbitrarily small differences in delay can be obtained with this arrangement, which is used for pulse splitter stages 5 through 8.

5.3.3 Interstage Fiber Link

An important implementation detail not mentioned earlier is the use of an optical fiber link between stages 4 and 5 of the pulse splitter. This interstage fiber link, shown in Figure 5-9, provides a couple of important benefits. Since the output beam from the fiber link has a direction which is unrelated to the direction of its input beam, stages 1–4 can be aligned independently of stages 5–8. This dramatically simplifies the task of aligning the pulse splitter. Since the number of different paths along which an optical pulse can travel is 16 for four pulse splitter stages and 256 for eight pulse splitter stages, it is much easier to align two independent groups of four stages than a single group of eight stages. The interstage fiber link also allows more flexible placement of the optics. In this case, stages 1–4 and stages 5–8 are located on different optical tables.

Lenses L1 and L2 form a telescopic beam compressor which reduces the diameter of the input beam from about 6 mm to 3 mm so that it fits within the clear aperture of a 10X microscope objective. To minimize reflection losses, these lenses were ordered from Newport Corporation with anti-reflection coatings covering a wavelength range of 430–700 nm. The

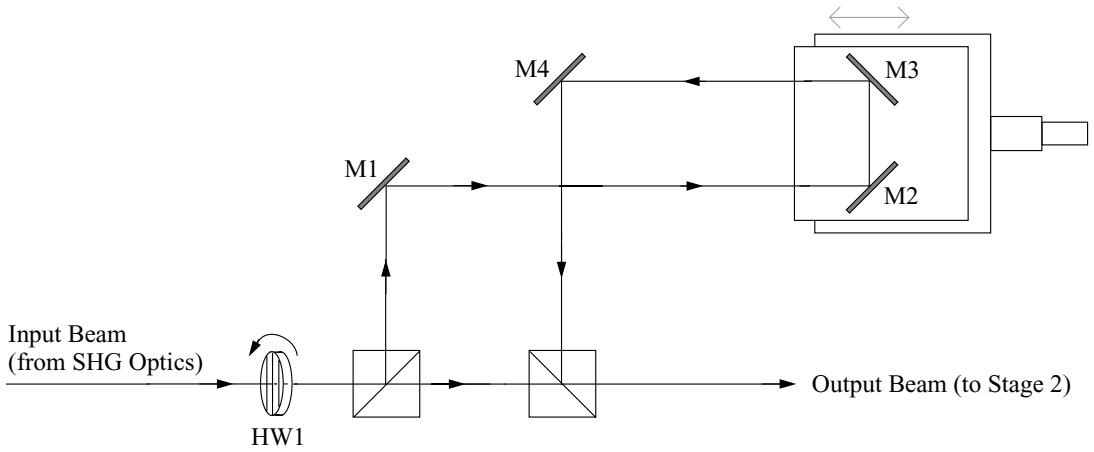


Figure 5-7: Optics layout used for pulse splitter stage 1.

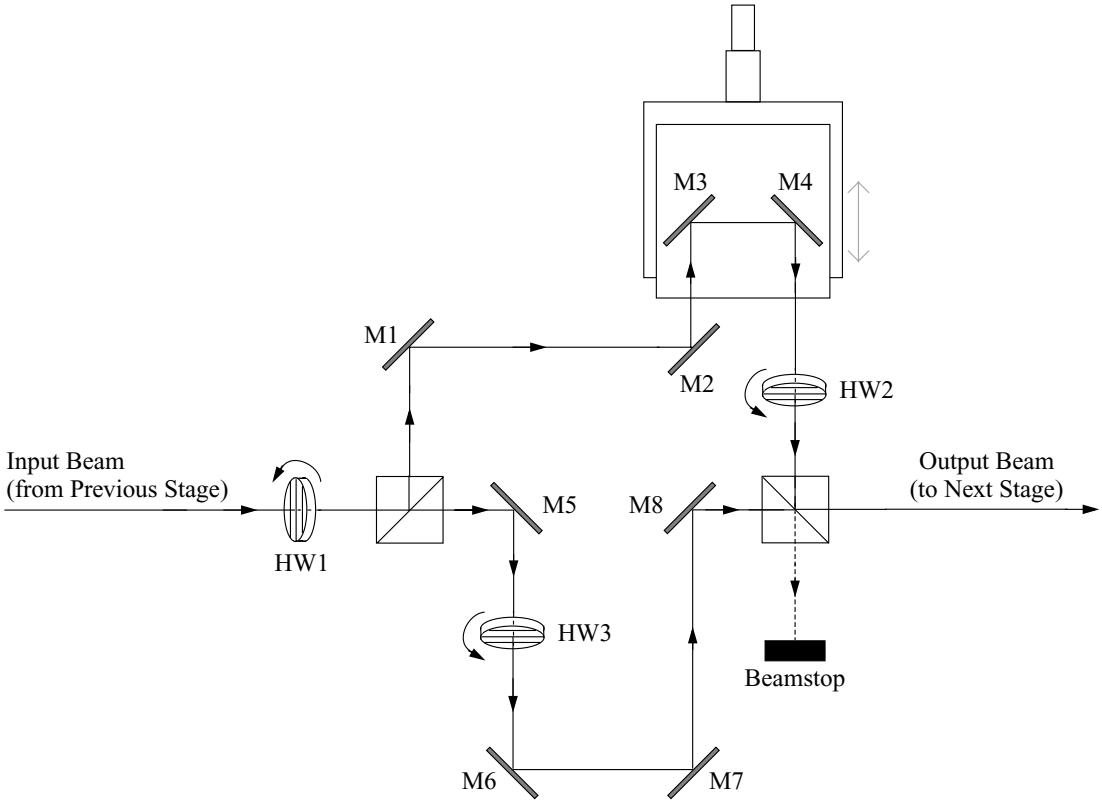


Figure 5-8: Optics layout used for pulse splitter stages 5 through 8.

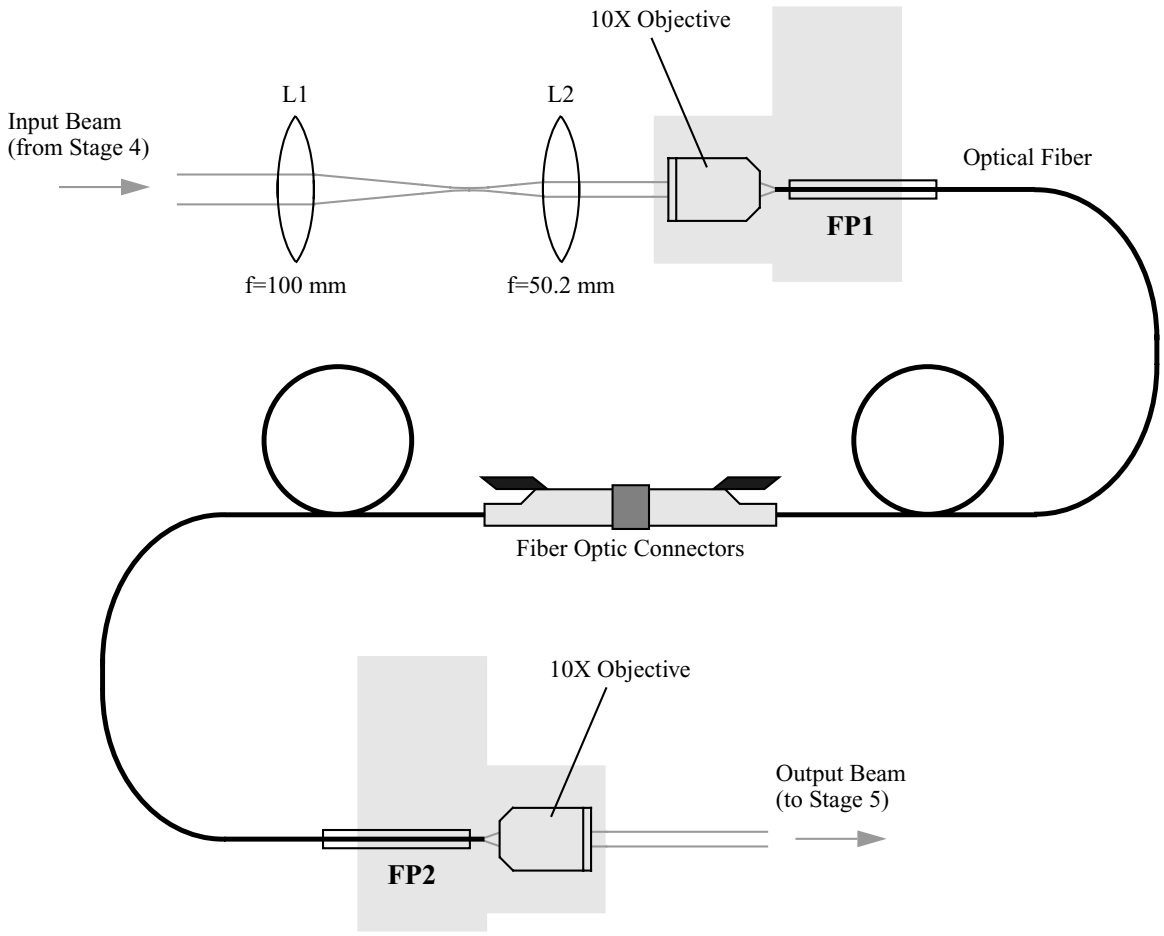


Figure 5-9: Optical fiber link connecting pulse splitter stages 4 and 5.

10X microscope objective is mounted on fiber positioner FP1 (New Focus model 9091) so that its focused output can be aligned with submicron accuracy to the tip of a single-mode fiber (Newport type F-SA). At the other end of the link, the light coupled into the fiber is recollimated back into a free-space beam with another 10X microscope objective mounted on fiber positioner FP2 (also New Focus model 9091). The diameter (3 mm) of the output beam is not expanded back to the input beam diameter (6 mm). Since the path delay differences of stages 5–8 are relatively small, beam spreading due to diffraction is not significant, and a smaller beam diameter can be used in these stages. Fiber optic connectors (Diamond E2000) allow the fiber link to be disconnected and reconnected easily. As explained in Section 5.4, these connectors are particularly helpful when the pulse splitter is being optically aligned. The insertion loss of these connectors is relatively small (< 0.5 dB). The dominant transmission loss of the interstage fiber link is the low power efficiency (39%) with which the input beam is coupled into the optical fiber. As mentioned earlier, the poor spatial quality of the beam produced by second-harmonic generation is responsible for this low coupling efficiency. Measured from input beam to output beam, the overall transmission efficiency of the interstage fiber link is about 33%. Since the fiber only supports a single mode of propagation, the output beam from the interstage fiber link has excellent spatial quality.

The same types of microscope objective and precision fiber positioner are used to couple the output beam from stage 8 of the pulse splitter into the fiber which delivers the optical pulses to the superconducting chip. (No telescopic beam compressor is needed here, as the output beam from stage 8 already has a diameter of 3 mm.) Because of the large improvement in beam quality effectuated by the interstage fiber link, the light is coupled into this single-mode fiber with much better power efficiency (about 70%). This fiber is also fitted with fiber optic connectors so that the piece of fiber threaded through the cryogenic sample holder can be disconnected from the piece aligned to the beams on the optical table.

Both the fiber used in the interstage fiber link and the fiber used to deliver the optical pulses to the superconducting chip have a length of about 3.75 meters. With a total fiber length of 7.5 meters used in the optical clocking setup, the 1 ps optical pulses from the mode-locked Ti:sapphire laser are broadened to almost 3 ps (FWHM) by the linear dispersion of the fiber at a 470 nm wavelength. Because the interstage fiber link is preceded by four stages of pulse splitting, the peak power of the optical pulses propagating through the fiber is low enough that pulse broadening due to nonlinear effects [85] is not excessive. (Nonlinear effects in the fiber which delivers the optical pulses to the superconducting chip are completely negligible, as these pulses have been divided by eight stages of pulse splitting.) The significance of such nonlinear effects was evaluated by performing autocorrelation measurements of the type discussed in Section 3.3.1. Figure 5-10 presents the autocorrelation traces of the optical pulses at the output of the optical clocking setup (i.e., after propagating through all 7.5 meters of fiber) for five different pulse energies coupled into the interstage fiber link. For these measurements, the pulse splitter configuration was SSSSSSSS, and the pulse energies were varied by turning the half-wave plates in stages 1–4 so that more or less optical power was delivered to the shorter beam paths. For pulse energies of 1.18 pJ and 2.36 pJ, nonlinear effects are insignificant, and almost all of the pulse broadening is due to linear dispersion of the fiber. The additional pulse broadening due to nonlinear effects is clearly visible at higher pulse energies. For a pulse energy of 18.6 pJ, the measured autocorrelation has a width of 7.7 ps, which is over twice that (3.7 ps) measured with a pulse energy of 1.18 pJ. A pulse energy of 4.66 pJ is close to the maximum that can be coupled into the interstage fiber link during "normal operation" of the pulse splitter, when the half-wave plates are adjusted so that the optical power is divided nearly equally among all beam paths. At this pulse energy, nonlinear effects broaden the pulse only moderately, and the measured autocorrelation has a width of 4.7 ps. Assuming a pulse shape of sech^2, the FWHM of the output pulse is 3.0 ps.

5.4 Optical Alignment of Pulse Splitter

Careful alignment of the pulse splitter is critical for coupling the optical pulses efficiently (and with approximately equal energies) into both the interstage fiber link and the fiber which delivers the light to the superconducting chip. This section first describes the procedure used to align the laser beam entering the pulse splitter so that it passes through the shorter paths of the stages in a uniquely defined manner. Then the alignment of the longer beam paths to the shorter ones is explained. While the discussion focuses on the alignment of pulse splitter stages 1–4, the same procedures are used to align stages 5–8.

The most common method used for aligning a laser beam is to center it on a pair of widely spaced apertures. Such a method is based on the simple principle that a line is

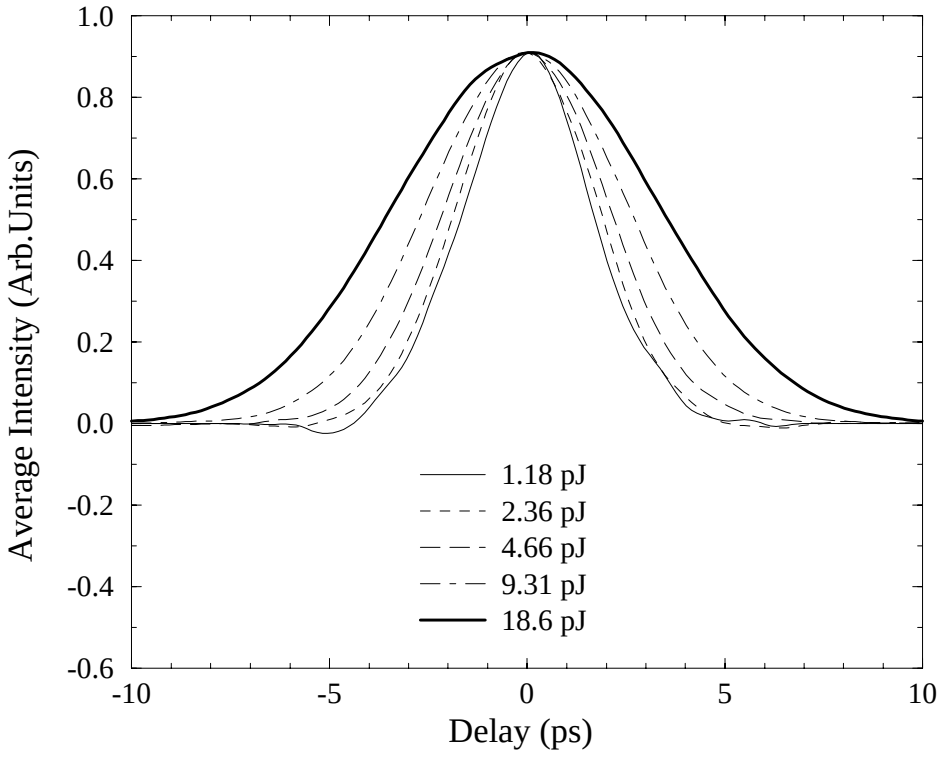


Figure 5-10: Autocorrelation traces of optical pulses at output of optical clocking setup, measured with five different pulse energies coupled into fiber link between pulse splitter stages 4 and 5.

uniquely defined by two points through which it passes. The method used for aligning the laser beam entering the pulse splitter is based on a different principle – namely, that a line is uniquely defined by one point through which it passes and by its direction. As shown in Figure 5-11, the alignment of the input beam is adjusted by turning two mirrors (M1 and M2) in front of the first pulse splitter stage. First, M1 is turned so that the input beam is centered on an aperture in close proximity to M2. Next, with the longer beam paths of all the stages blocked, the light coupled into the interstage fiber link is monitored with an optical power meter, and the angular orientation of M2 is adjusted to maximize the coupling efficiency to the fiber. This effectively fixes the direction of the beam passing through the shorter paths of the stages, as even a minute change in beam direction moves the focal spot of the microscope objective away from the core of the fiber held in fiber positioner FP1, decreasing the coupling efficiency. Since turning M2 slightly affects the alignment of the beam to the aperture, the angular orientation of M1 must be readjusted, and the whole process is therefore repeated. Typically, two iterations are sufficient for accurate alignment of the input beam.

The procedure just described only achieves consistent alignment of the input beam if the location of the fiber tip inside FP1 is precisely fixed with respect to the microscope objective. While the model of fiber positioner (New Focus model 9091) used for FP1 has excellent long-term stability, periodic readjustment of the fiber positioner (on the order of once a month) is performed to return the fiber tip to its original location in the focal

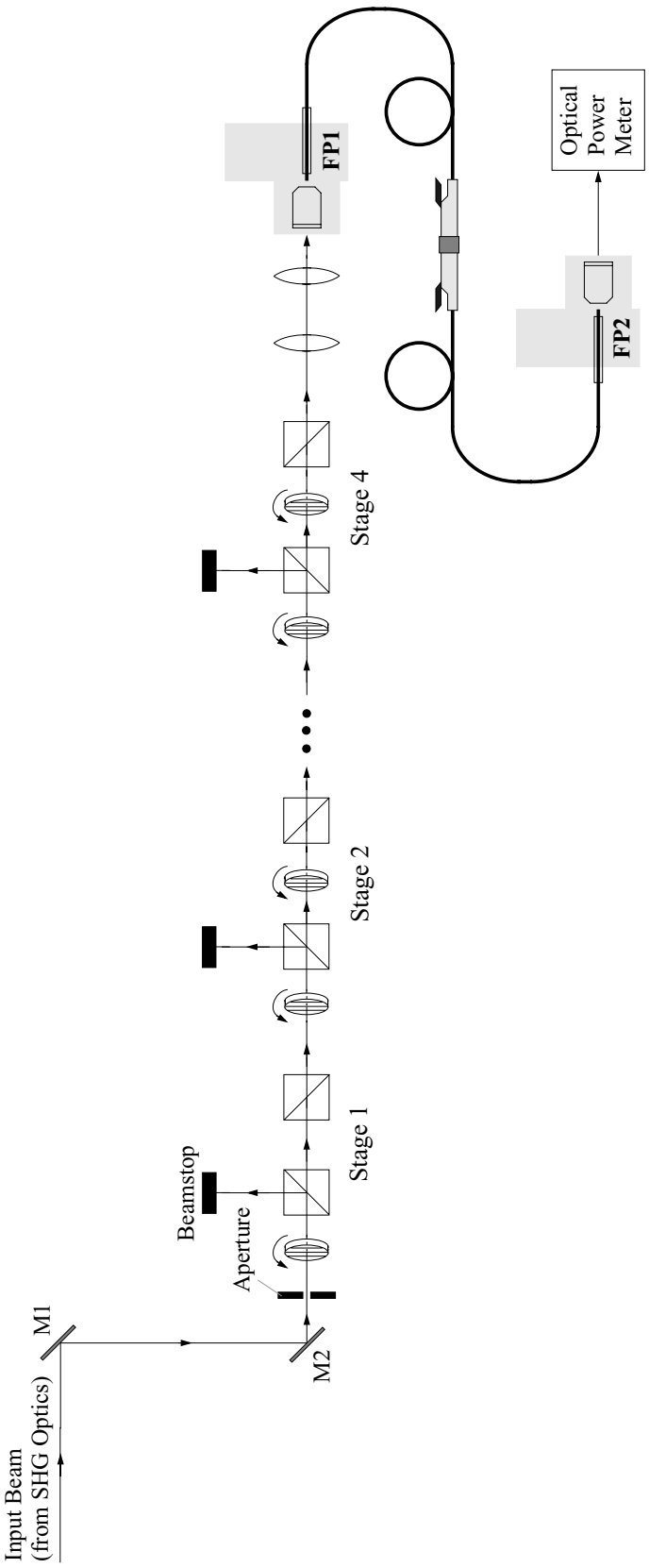


Figure 5-11: Alignment of laser beam entering pulse splitter.

plane of the objective. The location of the fiber tip in the focal plane is checked by sending light *backwards* through the interstage fiber link so that it is emitted from the fiber tip and propagates in a reverse direction through the shorter paths of the pulse splitter stages, as shown in Figure 5-12. Since the location of the fiber tip determines the direction of this backward propagating beam, readjusting FP1 so that this beam is centered on the aperture between M2 and stage 1 is an effective technique for returning the fiber tip to its original location. The use of detachable fiber optic connectors simplifies the task of sending light backwards through the interstage fiber link. For backward beam propagation, the piece of fiber held in FP1 is disconnected from the piece held in FP2 (through which the optical pulses are ordinarily delivered to stages 5–8) and connected to a piece held in FP3. The input beam is redirected into the microscope objective mounted on FP3 by inserting mirror M3 in its path. A telescopic beam compressor is not needed in front of this objective because high coupling efficiency is not important during this alignment procedure.

Once the input beam has been aligned so that it passes through the shorter paths of the stages in a uniquely defined manner, the longer path of each stage can be aligned to the shorter one. Proper beam recombination requires that the output beams from the longer and shorter paths be parallel and spatially overlapped with each other. The first step in the alignment of the longer path is to adjust the angular orientation of a mirror such as M4 in Figure 5-6 so that its output beam is coupled with high efficiency into the interstage fiber link (or, in the cases of stages 5–8, into the fiber which delivers the light to the superconducting chip). This adjustment ensures that the output beams from the longer and shorter paths are parallel. (Recall that the direction of the beam passing through the shorter paths has been optimized for highest coupling efficiency to the fiber.)

In principle, the output beam from the longer path has the highest coupling efficiency to the fiber when it is not just parallel but also overlapped with the one from the shorter path. In practice, however, it is difficult to detect a small lateral displacement error between the beams by measuring a minor drop in coupling efficiency. A more reliable method of detecting beam displacement errors is to place a CCD camera in the beam path, as shown in Figure 5-13. Because this camera has no lens in front of its CCD array, the change in position of the imaged beam when the shorter and longer paths are alternately blocked and unblocked is a direct measure of the displacement error. The angular orientation of mirror M3 is then adjusted until the measured displacement error is eliminated. Since turning M3 alters the direction of the output beam from the longer path, the angular orientation of M4 must be readjusted, and the whole process is therefore repeated. After several iterations, the alignment of the longer path to the shorter path is complete. All eight stages of the pulse splitter were aligned with this procedure.

5.5 Calibration of Pulse Splitter Path Delays

The general idea of using optical cross-correlation measurements for precise calibration of path delays was introduced in the last paragraph of Section 3.3.1. This section explains in detail how such measurements were used to calibrate the path delays of all eight pulse splitter stages.

Figure 5-14 shows the experimental setup employed for calibrating the path delays of the pulse splitter. The output beam of the second-harmonic generation optics is divided with a non-polarizing beamsplitter into two beams, which are then passed through two separate

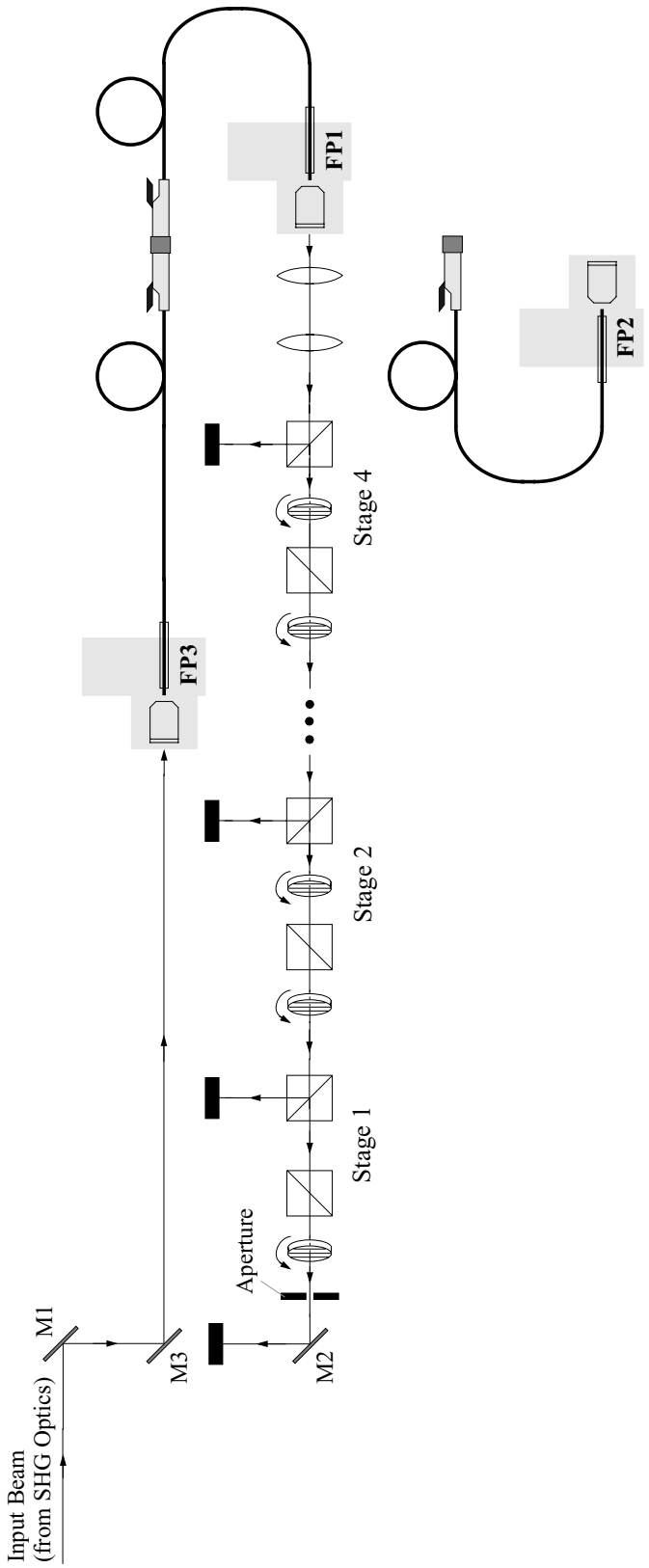


Figure 5-12: Use of backward beam propagation for setting location of fiber tip inside fiber positioner FP1.

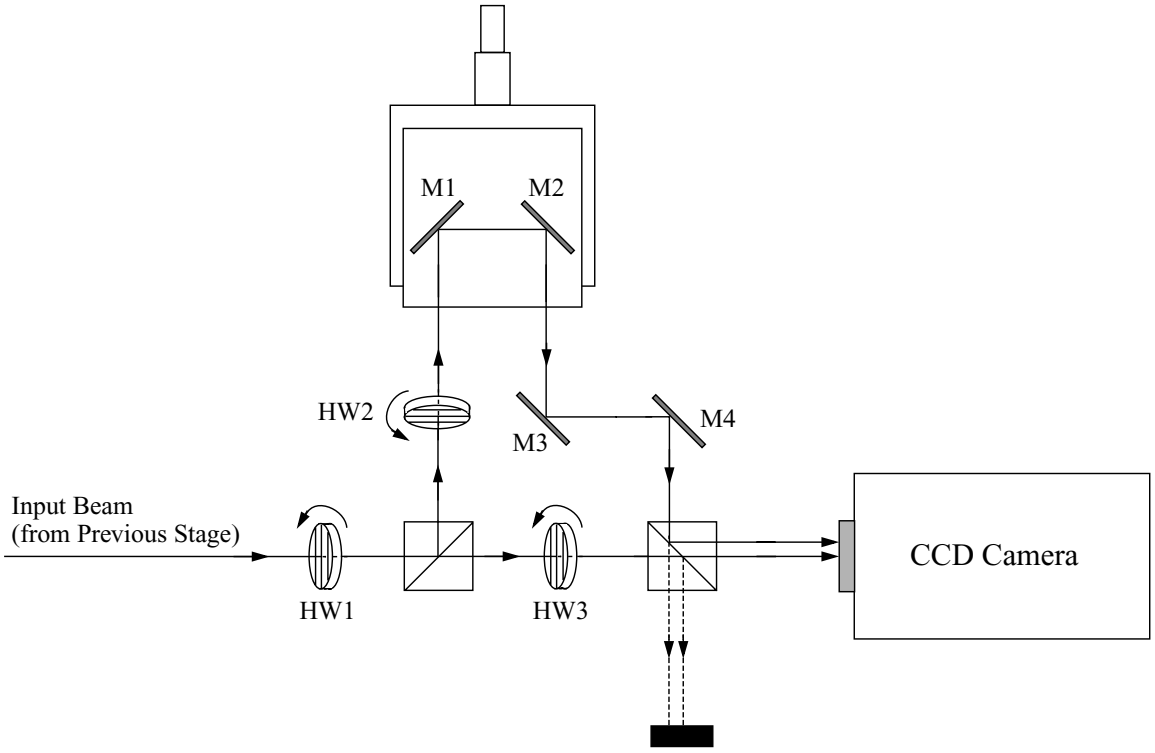


Figure 5-13: Measurement of beam displacement errors with CCD camera.

paths to an optical correlator. The test path contains the pulse splitter whose delays need to be calibrated. During the calibration, the pulse splitter is configured so that only one path in each stage is unblocked at a time. The output of the pulse splitter is coupled into the same piece of fiber through which the optical pulses are ordinarily delivered to the superconducting chip. Through the use of fiber optic connectors, this piece is disconnected from the piece of fiber threaded through the cryogenic sample holder and connected to a piece whose output is collimated and aligned to one input of the optical correlator. As in the case of the interstage fiber link, the output of the fiber is collimated by an objective mounted on a fiber positioner. Because the alignment of the output beam to the optical correlator is not as critical as the alignment of the beams passing through the pulse splitter, a less expensive fiber positioner (Newport F-915T) is used here. The optical pulses which arrive at the other input of the correlator provide a common "reference" in time against which the delays of the test path can be compared. The delay of the reference path (which also includes a piece of single-mode fiber) must be stable, but its exact value is not critical. The only requirement is that the difference in delays between the test and reference paths not exceed the scanning range (e.g., $\pm$400 ps) of the optical correlator.

The basic concept of calibrating the pulse splitter delays is now illustrated by describing the calibration of stage 8, for which the path delay difference (Δt_8) must equal $T/256$, or 48.49 ps. First, the pulse splitter is placed in a configuration of SSSSSSSS, and the cross-correlation between the pulses from the test and reference paths is measured. Next, the pulse splitter is placed in a configuration of SSSSSSSL, and another cross-correlation is measured. Because of the extra delay introduced by using the longer path instead of the

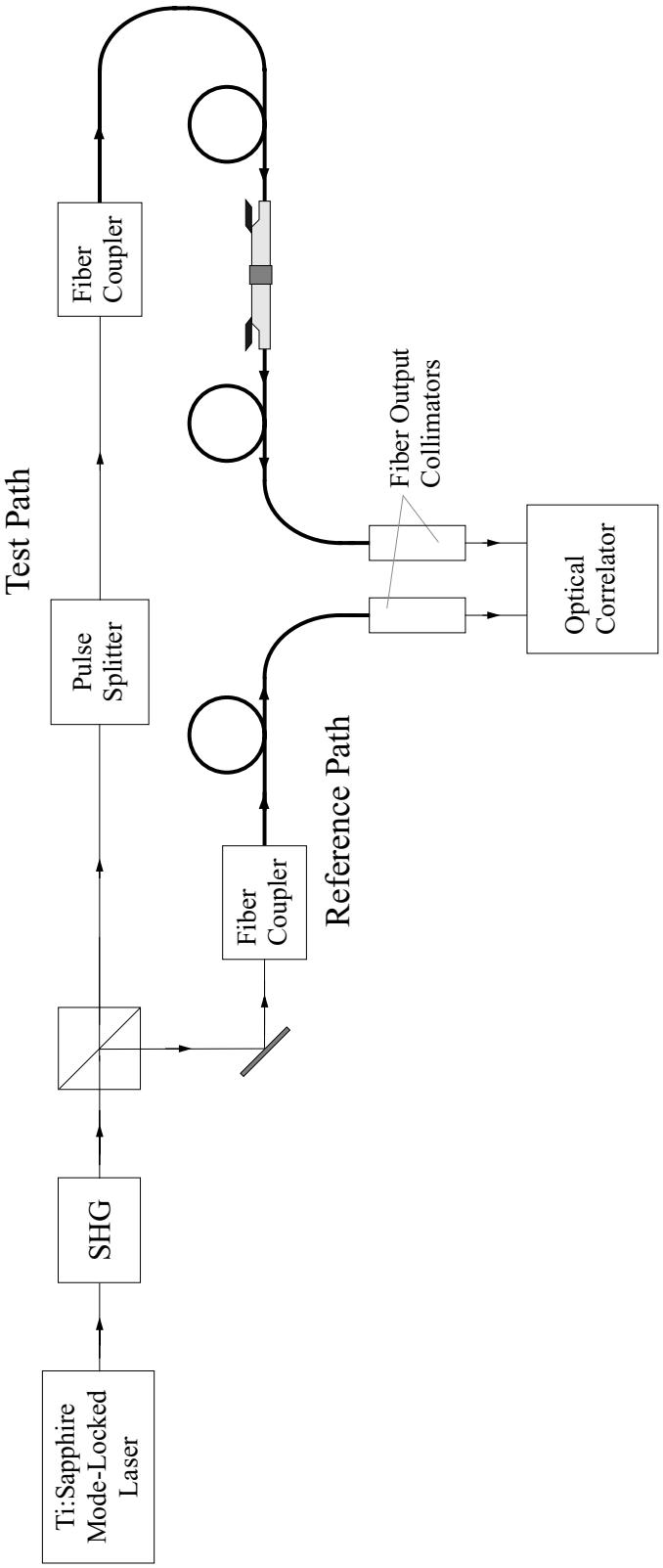


Figure 5-14: Experimental setup for calibrating path delays within pulse splitter by optical cross-correlation.

shorter path in stage 8, the peak of the cross-correlation is now shifted from that of the first cross-correlation. The magnitude of the shift is a precise measure of the path delay difference Δt_8. If Δt_8 does not equal 48.49 ps, the error in path length is corrected by moving the mirrors placed on the micrometer-driven translation stage. The path delay difference is then measured again by optical cross-correlation. After just two or three iterations, the path delay difference is calibrated to an accuracy better than 0.1 ps.

While small path delay differences in the pulse splitter can be directly calibrated in this manner, a different approach must be applied to calibrating path delay differences which exceed the scanning range of the optical correlator. For instance, the path delay difference of the first pulse splitter stage must equal exactly half of the laser period T. To calibrate a path delay difference of $T/2$ ($\approx$ 6.2 ns), which is *much* greater than the correlator scanning range, a "dummy" stage is added to the pulse splitter, as shown in Figure 5-15. (To avoid unnecessary clutter in the figure, the beam paths of the stages are represented in simplified form. The extra complexity of the real stage layouts described in Section 5.3.2 has no bearing on the present discussion.) The path delay difference of the dummy stage is chosen to match that of the first stage. The delays of the first stage and the dummy stage are calibrated with the following steps. First, the longer paths of all the stages (including the dummy stage) are blocked so that only the shorter paths are used, and the cross-correlation between the pulses from the test and reference paths is measured with the setup of Figure 5-14. Next, the shorter paths of the first stage and dummy stage are blocked, the longer paths of these two stages are unblocked, and another cross-correlation is measured. Since the pulse-to-pulse timing jitter of the mode-locked Ti:sapphire laser is negligible, the second cross-correlation will match the first if

$$\Delta t_1 + \Delta t_D = T. \tag{5.5}$$

If the sum of Δt_1 and Δt_D does not satisfy this condition, the peak of the second cross-correlation will be shifted from that of the first (by an amount equal to the error in the sum). If necessary, the lengths of the longer paths in these two stages can be adjusted (and readjusted) until Equation 5.5 is satisfied.

The cross-correlation measurements just described do not ensure that Δt_1 and Δt_D both equal $T/2$, as an error in Δt_1 might be compensated by an equal and opposite error in Δt_D. To check that Δt_1 and Δt_D equal each other (and therefore, by Equation 5.5, equal $T/2$), other cross-correlation measurements are performed. First, the pulse splitter is configured so that only the longer path in the first stage is used, and only the shorter paths in the rest of the stages are used. After increasing the delay through the reference path by about $T/2$ so that the difference in delays between the reference and test paths is again within the scanning range of the optical correlator, a cross-correlation is measured. Next, the pulse splitter is configured so that only the longer path in the dummy stage is used, and only the shorter paths in the rest of the stages are used. If Δt_1 and Δt_D are equal, the cross-correlation measured with this pulse splitter configuration will equal the previous one. If Δt_1 and Δt_D are not equal, the peaks of the two cross-correlations will be shifted from each other (by an amount equal to $\Delta t_1 - \Delta t_D$). If necessary, the lengths of the longer paths in these two stages can be changed by equal and opposite amounts so that $\Delta t_1 = \Delta t_D$. For highest accuracy, the cross-correlations discussed in the previous paragraph are then repeated in order to check if Equation 5.5 is still satisfied. After a few iterations back and forth, both Δt_1 and Δt_D are calibrated to an accuracy better than 0.1 ps.

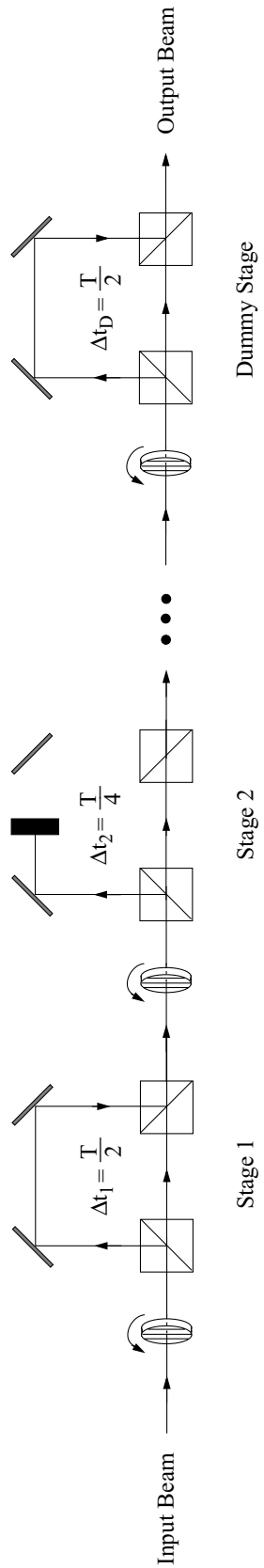


Figure 5-15: Pulse splitter with dummy stage added for calibrating path delays of stage 1.

After the calibration of Δt_1 is complete, a similar approach is applied to calibrating Δt_2, the path delay difference of the second stage. Since the original dummy stage is no longer needed, it is replaced by a new dummy stage with a path delay difference Δt_D close to $T/4$. Cross-correlation measurements are performed to check whether the sum of Δt_2 and Δt_D equals Δt_1, which has already been calibrated to be extremely close to $T/2$. The first cross-correlation is measured with the pulse splitter configured so that only the longer path in the first stage is used, and only the shorter paths in the rest of the stages are used. The second cross-correlation is measured with the pulse splitter configured so that only the longer paths in the second stage and the dummy stage are used, and only the shorter paths in the rest of the stages are used. These two cross-correlations will be equal if

$$\Delta t_2 + \Delta t_D = \Delta t_1 = T/2, \tag{5.6}$$

where the last equality assumes that Δt_1 has been calibrated with negligible error. Other cross-correlations, analogous to those described in the previous paragraph, are then performed to check that Δt_2 and Δt_D are equal to each other. Once this equality has been established, it follows from Equation 5.6 that Δt_2 equals the desired value of $T/4$. Calibration of the other pulse splitter stages proceeds by iteration. The path delay differences of stage 3 and its matching dummy stage are calibrated against Δt_2, the path delay differences of stage 4 and its matching dummy stage are calibrated against Δt_3, and so on. The path delays of the first seven pulse splitter stages were calibrated with this dummy stage technique. Only the path delay difference of stage 8 was calibrated with the more direct method described in the third paragraph of this section.

After the path delays of all eight stages were calibrated, other cross-correlation measurements were performed to check the accuracy of the time intervals between the pulses produced by the pulse splitter. With all its beam paths unblocked, the pulse splitter generates a train of 256 pulses for each pulse emitted by the mode-locked Ti:sapphire laser. A particularly critical time interval is the one between the 128th and 129th pulses in the train. The 128th pulse follows the beam paths used in pulse splitter configuration SLLLLLLL, and the 129th pulse follows the beam paths used in pulse splitter configuration LSSSSSSS. Because these two pulses do not share the same beam path in any of the eight stages, the time interval between them is sensitive to a linear combination of the errors in the delay calibration of all eight stages. Mathematically, the challenge of making this time interval accurate is analogous to the difficulty of maintaining uniformly spaced output levels at the "half-scale" point of a DAC based on a simple binary-weighted architecture [119]. To check the accuracy of this time interval, the difference in delay through the pulse splitter in its SLLLLLLL and LSSSSSSS configurations was measured by optical cross-correlation. The measured difference was 48.54 ps, only about 50 fs (0.05 ps) larger than the ideal value of 48.49 ps. Another demanding test of the delay calibration is to measure the time interval between the last (256th) pulse in one train and the first pulse in the next train (due to the next laser pulse). Such a test checks whether $\Delta t_1 + \Delta t_2 + \cdots + \Delta t_8$ is smaller than the laser period T by the correct amount ($T/256$). Optical cross-correlation measurements similar to those discussed earlier showed that the time interval between these pulses was 48.50 ps, only about 10 fs larger than the ideal value (48.49 ps). The measured accuracy of these time intervals strongly suggests that the path delay differences $\Delta t_1, \Delta t_2, \ldots, \Delta t_8$ were each calibrated to an accuracy *substantially* better than 0.1 ps.

5.6 Optical Power Balancing of Pulse Splitter Beam Paths

The adjustment of half-wave plates to balance the optical power in various pulse splitter beam paths is first demonstrated for the example of a two-stage pulse splitter shown in Figure 5-16. The mode-locked laser pulses entering the pulse splitter are assumed to be p-polarized. The pulses at the output of each stage have alternating p and s polarizations. Ideally, the pulses at the output of each stage have equal energies if the half-wave plates are turned so that HW1_1 and HW1_2 rotate the polarizations of the pulses passing through them by 45°, and HW2_2 and HW3_2 do not rotate the polarizations of the pulses passing through them. However, as already discussed in Section 5.3.2, this energy balance between the output pulses may be degraded by miscellaneous imperfections of the optical setup. The resulting variations in the energies of the output pulses are compensated by turning the half-wave plates slightly away from their nominal settings. Determining the proper adjustments to make requires knowledge of how small rotations of the various half-wave plates affect the energy of each output pulse.

Each pulse arrives at the output of the second stage from one of four beam paths. Using the shorthand notation introduced in Section 5.2, the four beam paths are those selected in pulse splitter configurations SS, SL, LS, and LL. Turning HW1_1 so that the polarization of the input beam is rotated by slightly more than 45° alters the division of optical power in the first beamsplitter of stage 1 so that less power is delivered to the shorter path and more to the longer path. Therefore, the output beam power is decreased (↓) in pulse splitter configurations SS and SL and increased (↑) in pulse splitter configurations LS and LL. These results are summarized in the first row of Table 5.1. The results of increasing the polarization rotation through HW1_2 were described previously in the second paragraph of Section 5.3.2 and are summarized here in the second row of the table. As explained earlier, HW2_2 and HW3_2 operate as variable attenuators for the longer and shorter paths of stage 2. Hence, increasing the polarization rotation through HW2_2 decreases (↓) the output beam power in pulse splitter configurations SL and LL and has no effect (–) on pulse splitter configurations SS and LS, while increasing the polarization rotation through HW3_2 decreases (↓) the output beam power in pulse splitter configurations SS and LS and has no effect (–) on pulse splitter configurations SL and LL. These results are summarized in the third and fourth rows of the table.

Table 5.1: Effect of rotating various half-wave plates on output beam power with two-stage pulse splitter in four different configurations.

	Pulse Splitter Configuration			
Half-Wave Plate	SS	SL	LS	LL
HW1_1	↓	↓	↑	↑
HW1_2	↓	↑	↑	↓
HW2_2	–	↓	–	↓
HW3_2	↓	–	↓	–

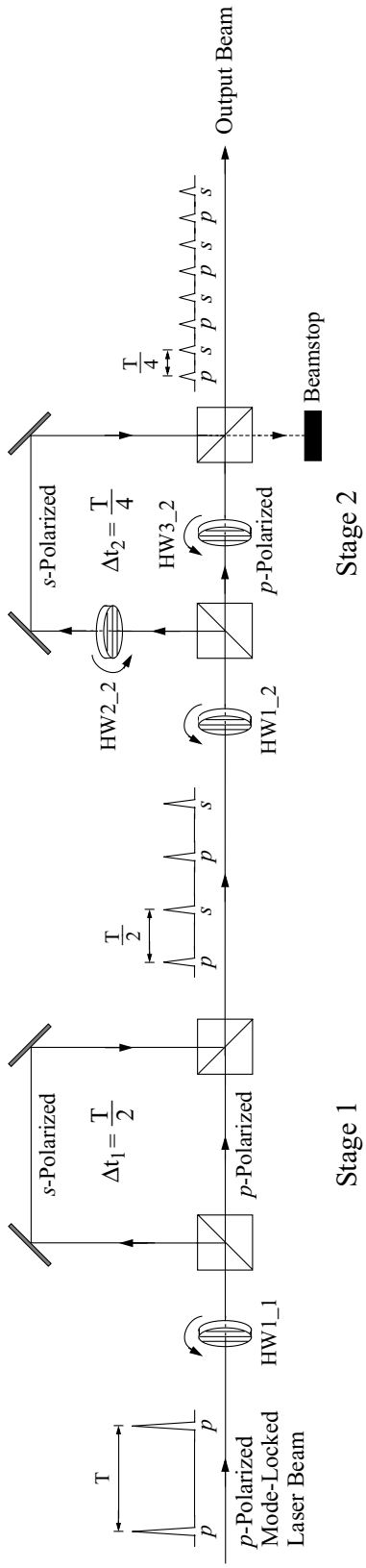


Figure 5-16: Example of two-stage pulse splitter illustrating polarization of optical pulses at output of each stage.

For the two-stage pulse splitter, the degrees of freedom obtained by adjusting these four half-wave plates are sufficient that the energy of an output pulse from one of the four beam paths can be reduced without any net change in the energies of the output pulses from the other beam paths. Consequently, the energy of an output pulse which is too strong can always be reduced to match the energies of the others. As an example, assume that the output pulse following the beam path used in pulse splitter configuration SS is 4% more powerful than the output pulses from the other three beam paths. Such an imbalance can be corrected with the following combination of adjustments. First, the polarization rotations through both HW1_1 and HW1_2 are increased by equal amounts so that the output beam power is decreased by 2% in pulse splitter configuration SS and increased by 2% in pulse splitter configuration LS. (With equal adjustments made to HW1_1 and HW1_2, there is no net change in the output beam power in pulse splitter configurations SL and LL.) Next, HW3_2 is turned so that the shorter path in stage 2 is attenuated by 2%. With this adjustment, the output beam power in pulse splitter configuration LS is restored to its original value, and the output beam power in pulse splitter configuration SS is 4% lower than its original value, which is the desired correction. In a similar manner, other combinations of adjustments can be used to reduce the energy of an output pulse from any of the other three beam paths. The task of balancing the optical power in the various beam paths can be expedited by writing a simple software program which calculates the combination of adjustments needed to compensate for a given imbalance (as measured with an optical power meter).

The results of Table 5.1 are easily generalized to the case of the eight-stage pulse splitter implemented in this thesis project. Let the half-wave plates of the stages be numbered with the same convention used in Figure 5-16. If HW1_1 is turned so that the polarization of the input beam is rotated by slightly more than 45°, the output beam power is decreased in every pulse splitter configuration beginning with the letter "S" and increased in every pulse splitter configuration beginning with the letter "L". An alternative way of expressing this is that such an adjustment decreases the power in all the beam paths used in pulse splitter configuration SXXXXXXX and increases the power in all the beam paths used in pulse splitter configuration LXXXXXXX. The effects of adjusting the other half-wave plates can be described similarly. Increasing the polarization rotation through HW1_2 decreases the power in the beam paths used in pulse splitter configurations SSXXXXXX and LLXXXXXX and increases the power in the beam paths used in pulse splitter configurations SLXXXXXX and LSXXXXXX. Increasing the polarization rotation through HW2_2 decreases the power in the beam paths used in pulse splitter configuration XLXXXXXX and has no effect on the beam paths used in pulse splitter configuration XSXXXXXX. Increasing the polarization rotation through HW3_2 decreases the power in the beam paths used in pulse splitter configuration XSXXXXXX and has no effect on the beam paths used in pulse splitter configuration XLXXXXXX. (Note the obvious relationship to the results of Table 5.1.) The effects of adjusting the half-wave plates in stages 3–8 follow a pattern similar to that set in stage 2. The only difference is that with each successive stage, the "S" and "L" letters in the codes describing the affected pulse splitter configurations are shifted one position to the right (with each of the remaining positions filled with an "X"). As an example, increasing the polarization rotation through HW1_6 decreases the power in the beam paths used in pulse splitter configurations XXXXSSXX and XXXXLLXX and increases the power in the

beam paths used in pulse splitter configurations XXXXSLXX and XXXXLSXX.

The eight-stage pulse splitter contains a total of 22 half-wave plates. The degrees of freedom obtained by adjusting these half-wave plates are *not* sufficient for balancing the energies of the output pulses from all 256 beam paths through the pulse splitter[3]. While perfect energy balancing between the output pulses is not attainable, the imbalance can be minimized by careful adjustment of the half-wave plates. The adjustment procedure follows naturally from the discussion of the previous paragraph. HW1_1 is adjusted so that the average output power (due to all beam paths) in pulse splitter configuration SXXXXXXX equals the average output power in pulse splitter configuration LXXXXXXX. HW1_2 is adjusted so that the sum of the average output powers in pulse splitter configurations SSXXXXXX and LLXXXXXX equals the sum of the average output powers in pulse splitter configurations SLXXXXXX and LSXXXXXX. Either[4] HW2_2 or HW3_2 is adjusted so that the average output power in pulse splitter configuration XLXXXXXX equals the average output power in pulse splitter configuration XSXXXXXX. The adjustment of the half-wave plates in stages 3–7 proceeds similarly.

After the adjustment of the half-wave plates is complete, the strongest output pulse is typically 25–30% more powerful than the weakest output pulse. Most of the residual imbalance is due to differences in the efficiencies with which the various beams can be coupled into both the interstage fiber link and the fiber which delivers the optical pulses to the superconducting chip. Such differences in coupling efficiencies are exacerbated by the poor spatial quality of the beam produced by second-harmonic generation.

Since much of the compensation for variations in output pulse energies is accomplished by adding attenuation to various beam paths, the overall transmission efficiency of the pulse splitter (averaged over all its beam paths) is reduced when the half-wave plates are adjusted for optimum power balancing. In general, the more compensation is needed, the greater will be the drop in transmission efficiency. For the eight-stage pulse splitter constructed for the optical clocking system, the reduction in transmission efficiency due to compensation (about 15–20% per stage, depending on the quality of optical alignment) exceeds that due to reflection losses (about 10% per stage) and is comparable to the transmission losses associated with coupling the free-space beams into the optical fibers used in the setup (Section 5.3.3). The combined effect of these losses is substantial. When the average power of the second-harmonic beam entering the pulse splitter is turned up to about 70 mW, the average power of the 20.6 GHz optical pulse train delivered to the superconducting chip is only 1.1–1.6 mW. The overall transmission efficiency is therefore 1.6–2.3%. Note, though, that this *measured* transmission efficiency is more than four times greater than the *ideal* transmission efficiency of eight cascaded pulse rate doublers based on non-polarizing beamsplitters (Figure 5-2). The experimental results presented in the next chapter demonstrate that the optical power delivered to the superconducting chip is more than sufficient for reliable optical triggering of a Josephson circuit at frequencies up to 20.6 GHz.

The insertion of the interstage fiber link between stages 4 and 5 does not require modifications to the procedure used to balance the optical power in the pulse splitter beam paths.

[3]This is an inevitable consequence of increasing the number of pulse splitter stages. While the number of beam paths that an optical pulse may follow grows exponentially with the number of stages, the number of half-wave plates available for compensation of power imbalances grows only linearly.

[4]As noted earlier, attenuation is never added to both the longer and shorter paths of the same stage.

However, because of small birefringence changes in the single-mode fiber caused by stress and temperature variations, the optical pulses at the end of the interstage fiber link have polarizations which slowly drift over time. To maintain the desired division of optical power in the first beamsplitter of stage 5, half-wave plate HW1_5 had to be readjusted fairly often (about every 30 minutes). In retrospect, more stable operation of the pulse splitter could have been achieved if the single-mode fiber used in the interstage fiber link were replaced with a "polarization-preserving" type [120].

Chapter 6

Experiments with Optically Clocked Josephson Circuits

The last chapter described an optical clocking system capable of triggering Josephson circuits with a variety of pulse patterns, at clock frequencies from 80.6 MHz up to 20.6 GHz. This chapter presents two different experiments which were performed to evaluate the system. In the first, an RSFQ T flip-flop was optically triggered at frequencies up to 1.3 GHz with a variety of bit patterns, and its output was directly observed on a digital oscilloscope. In the second, a JTL was optically triggered at frequencies up to 20.6 GHz with a variety of bit patterns, and correct operation was verified by precise measurement of the Josephson voltage.

6.1 Optically Triggered T Flip-Flop Experiment

6.1.1 Circuit Description

The functionality of the optical clocking system was first established by optically triggering an RSFQ T flip-flop. The circuit used in this experiment is presented in Figure 6-1; all of the cells shown are standard elements of the RSFQ logic family [31]. A three-junction DC/SFQ converter [121], the parameter values of which are listed in the figure caption, transforms each picosecond electrical pulse from the MSM photodiode into an SFQ pulse, which is picked up and transferred by a JTL to a T flip-flop, whose state is then toggled. The SFQ/DC converter[1] senses the state of the flip-flop and generates a small output voltage ($\approx 100\ \mu$V) which can be detected with a room-temperature amplifier and observed on an oscilloscope. In proper operation, each arrival of an optical pulse is reflected in a transition of the output voltage. Purely electrical triggering of the circuit is also possible; if sufficient current is passed through resistor R_A, the DC/SFQ converter generates an SFQ pulse, which toggles the T flip-flop. This is useful for checking the functionality of the Josephson circuits before proceeding to high speed testing with the optical clocking system.

[1] In most circuit implementations, including the one used in this experiment, the T flip-flop and SFQ/DC converter are combined to form a single RSFQ cell [31]. The representation of this circuitry in Figure 6-1 as a T flip-flop connected to a separate SFQ/DC converter is chosen to highlight the two distinct functions (toggling and SFQ/DC conversion) being performed. In the description of more complex RSFQ circuits presented in later chapters of this thesis, this circuit combination is called a "T-type SFQ/DC converter".

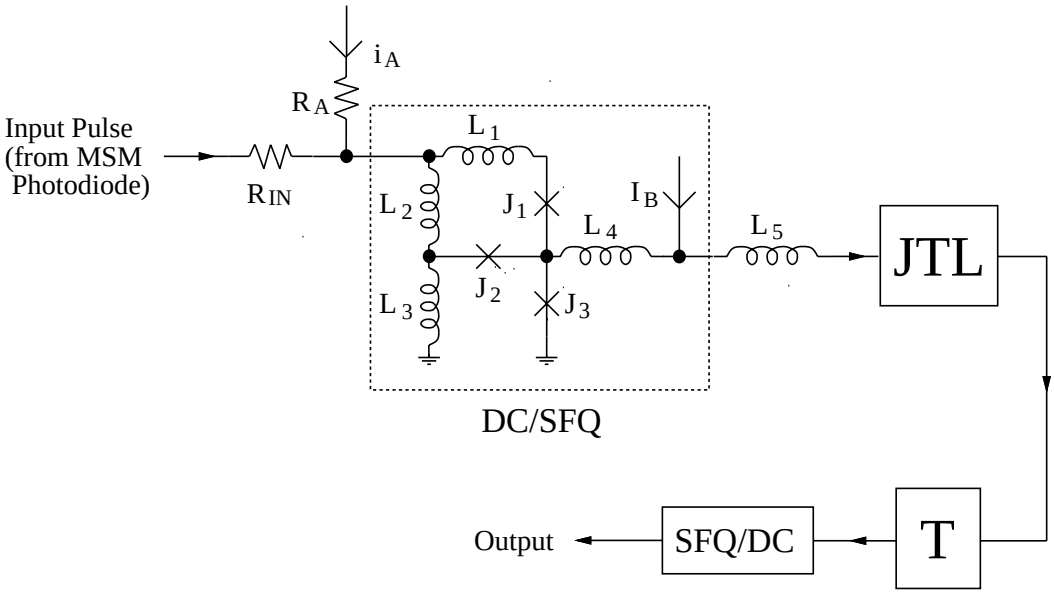


Figure 6-1: Circuit for optically triggered T flip-flop experiment. The nominal parameters of the input circuitry are: R_{IN}=10 Ω, R_A=50 Ω, L_1=L_2=1.3 pH, L_3=3.4 pH, L_4=1.1 pH, L_5=1.6 pH, I_{c1}=I_{c3}=171 μA, I_{c2}=147 μA, and I_B=375 μA.

An important design issue in this experiment is the sensitivity of the input circuitry to variations in the amplitude of the current pulse generated by the MSM photodiode. As explained in the last chapter, the optical pulses delivered to the Josephson chip do not have equal energies. Even after adjusting the half-wave plates for optimum power balancing of the pulse splitter beam paths, the strongest optical pulses delivered to the Josephson chip are 25–30% more powerful than the weakest ones. At the modest optical power levels used in the experiment, each current pulse generated by the MSM photodiode is proportional to the optical pulse energy, so the amplitudes of these current pulses vary by 25–30%. To study the effects of such variations, the triggering of the DC/SFQ converter by picosecond current pulses from the MSM photodiode was simulated with JSIM [122], a SPICE-like simulation tool for superconducting circuits. In the simulation, the shape and duration of the current pulse from the MSM photodiode were modeled on data taken at the University of Rochester [101]. These simulations showed that the DC/SFQ converter has an input margin of ±72% when triggered by picosecond pulses from the MSM photodiode. Such a large input margin easily accommodates the amplitude variations of the photocurrent pulses.

All of the RSFQ cells shown in Figure 6-1 were donated to this project by Semenov and Lin at the State University of New York (SUNY) Stony Brook and had been laid out for the standard HYPRES niobium process [123] with 1 kA/cm^2 critical current density for the Josephson junctions. The layout of the optoelectronic interface to the circuit is shown in Figure 6-2. To protect the Josephson circuitry from heat generated by the incident light, the MSM photodiode is located 500 μm away from the DC/SFQ converter. On-chip reflections are suppressed with techniques whose effectiveness was demonstrated in the optoelectronic sampling experiments of Chapter 4. The superconducting microstrip transmission line which connects the MSM photodiode to the DC/SFQ converter is terminated with a resistor R_{IN}

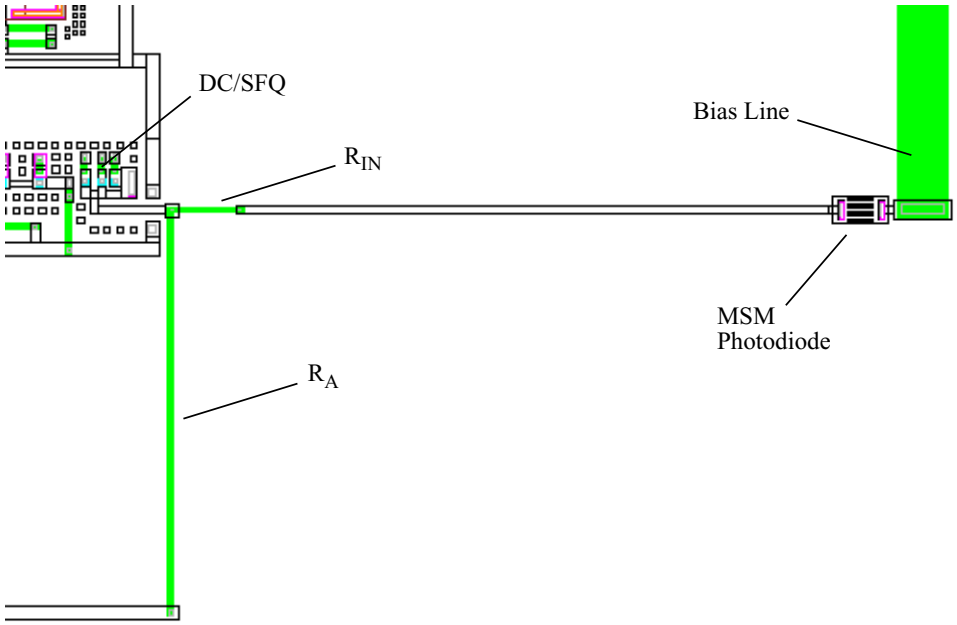


Figure 6-2: Layout of optoelectronic interface showing an MSM photodiode connected by a microstrip transmission line to the DC/SFQ converter.

matched to its characteristic impedance ($Z_0 = 10\ \Omega$). The input impedance of the DC/SFQ converter itself is much less than 10 Ω and only has a minor effect on the quality of the termination. The bias voltage for the MSM photodiode is supplied over a long (> 1 mm), wide (40 μm), resistive (1 Ω/□) microstrip line; the loss due to resistance dampens the picosecond pulses launched on the bias line, eliminating the spurious oscillations observed in Section 4.3.2. The MSM photodiode itself consists of interdigitated Nb fingers deposited on the silicon substrate of the Josephson chip. The nominal width and spacing of the fingers are both 1 μm, and the active area of the MSM photodiode is 20 μm × 20 μm. Electro-optic sampling experiments have shown that at cryogenic temperatures such photodetectors generate electrical pulses with widths below 10 ps (FWHM) [101].

Several copies of the Josephson chip were fabricated at HYPRES, Inc., with special processing for the integrated MSM photodiodes [39]. After the functionality of the RSFQ circuits was checked with low frequency electrical testing, the chip was prepared for the experiment with the optical clocking system. The next two sections explain how the optical fiber threaded through the cryogenic sample holder was aligned to the MSM photodiode and how the Josephson chip was protected against flux trapping problems.

6.1.2 Alignment of Optical Fiber to MSM Photodiode

The optical fiber threaded through the cryogenic sample holder is aligned to the MSM photodiode on the Josephson chip with the technique shown in Figure 6-3. The glass capillary and quartz spacer are both glued to the chip. The optical fiber fits snugly inside the glass capillary, which is a precision component manufactured by Nippon Electric Glass for splicing fibers together. The fiber itself is not glued but is pushed downward with gentle pressure so that its cleaved end rests against the quartz spacer; leaving the fiber unglued

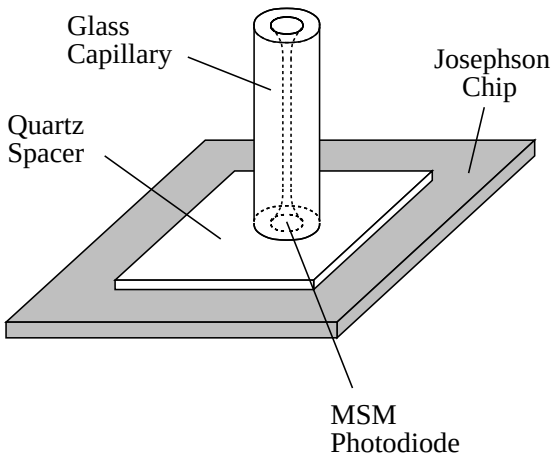


Figure 6-3: Technique for aligning optical fiber to on-chip photodetector. The glass capillary holds the fiber in place over the MSM photodiode.

simplifies the task of changing chips in the sample holder. The quartz spacer, which is 50 μm thick, increases the area of the MSM photodiode illuminated by the cone of light emitted from the 3.1 μm core of the fiber, reducing local saturation effects in the device. The spacer also helps protect the chip surface during alignment of the capillary. Both the spacer and the capillary are glued with ultraviolet-cured optical adhesive (Norland Optical Adhesive 81), which usually survives several thermal cycles.

The alignment of the capillary is performed under a manual probe station. Probe tips are connected to two pads of the chip so that the MSM photodiode is biased at about 1.5 V by an alkaline battery. The photocurrent is monitored with a Keithley 169 digital multimeter (DMM). (Except for a small increase in its leakage current, the MSM photodiode works as well at room-temperature as at cryogenic temperatures.) Prior to gluing, the capillary is held above the chip surface by a self-closing tweezer mounted to a manually-controlled three-axis translation stage (from Newport Corporation). Inserted inside the capillary is a piece of single-mode optical fiber illuminated by 200 μW of 633 nm light from a helium-neon laser. The capillary is then positioned with the translation stage so that the photocurrent monitored with the DMM is maximized. With the aligned capillary in contact with the quartz spacer, a drop of optical adhesive is applied to the base of the capillary. Due to surface tension, the optical adhesive naturally spreads around the entire circumference of the capillary. The cone-shaped opening[2] at the bottom of the capillary tube, visible in Figure 6-3, prevents the optical adhesive from spreading inward to the optical fiber. (Since this fiber has to be removed from the capillary after the alignment procedure, it must not be glued in place.) After a final check of the photocurrent to make sure that application of the optical adhesive did not disturb the alignment of the capillary, the optical adhesive is cured by exposing it to light from an ultraviolet lamp. The optical fiber is then removed from the capillary, which is released from the tweezer.

[2]As indicated in Figure 6-3, the opening at the top of the capillary tube is also cone-shaped in order to facilitate insertion of the optical fiber.

6.1.3 Avoidance of Flux Trapping Problems

The operation of a Josephson circuit can be disrupted by flux trapping problems [124, 125, 126]. Magnetic flux quanta may be trapped in the superconducting ground plane when it is cooled through the critical temperature (T_c) in a nonzero ambient magnetic field. If the magnetic field from one of these flux quanta couples significantly to a nearby Josephson circuit, the operating points of the Josephson junctions may be shifted enough that the circuit malfunctions. Two lines of defense are employed to protect the Josephson circuits from trapped magnetic flux. The first line of defense is implemented on the Josephson chip itself. Holes and elongated slots known as "moats" are etched in the superconducting ground plane. These holes and moats act as energetically favorable pinning sites for the magnetic flux quanta and are located so that any magnetic flux trapped within them is negligibly coupled to the Josephson circuitry. The effectiveness of such holes and moats for avoiding flux trapping problems has been experimentally confirmed by several researchers [124, 125, 126]. In the case of the circuit used for the optically triggered T flip-flop experiment, many small ground plane holes were placed amidst the Josephson junctions; some of the holes near the DC/SFQ converter can be seen in Figure 6-2 as arrays of small boxes, unconnected to other structures in the layout. While such small holes are not as effective protection against flux trapping as larger holes and moats [125], they are more than adequate for testing the small circuit considered here, which contains only 27 Josephson junctions. Larger ground plane holes and moats are used in the design of the modulator test chip described in Chapter 10, which contains over 4000 Josephson junctions.

The protection against flux trapping offered by ground plane holes and moats may be overcome if the ambient magnetic field in which the chip is cooled into the superconducting state is too large. Therefore, the second line of defense against flux trapping is to minimize this ambient magnetic field. In this work, a very low ambient magnetic field has been achieved by cooling down the Josephson chip inside a specially designed liquid helium dewar [127] originally constructed for the IBM Josephson computer project [128]. The major design features of this liquid helium dewar are depicted in Figure 6-4. The Josephson chip placed inside the cryogenic sample holder sits at the bottom of the dewar. The bottom region of the dewar is shielded from the earth's magnetic field by three nested cans made of moly-permalloy. Because the bottom of the dewar is shaped into a narrow "tail", these shields can be relatively small and inexpensive. With proper degaussing of the innermost shield, it is possible to achieve ambient magnetic fields inside the dewar on the order of 1 microgauss (μG).

Shielding the Josephson chip from external magnetic fields is not, however, sufficient to ensure that it traps no magnetic flux during cooldown. If the chip is cooled down too rapidly, thermal gradients may induce currents in the metal components of the sample holder which generate transient magnetic fields. At the chip surface, these transient magnetic fields may be orders of magnitude greater than 1 μG [124]. To avoid flux trapping due to thermally generated magnetic fields, the dewar includes provisions for cooling down the Josephson chip very slowly with minimal thermal gradients. A fiberglass tube inserted inside the dewar separates the sample volume where the Josephson chip resides from the outer reservoir in which most of the liquid helium is stored. The liquid helium can flow between these two chambers through an opening at the bottom of the fiberglass tube. As explained shortly, a slow cooldown of the Josephson chip is accomplished by allowing the liquid helium to flow gradually from the outer reservoir into the sample volume. The flow of liquid helium

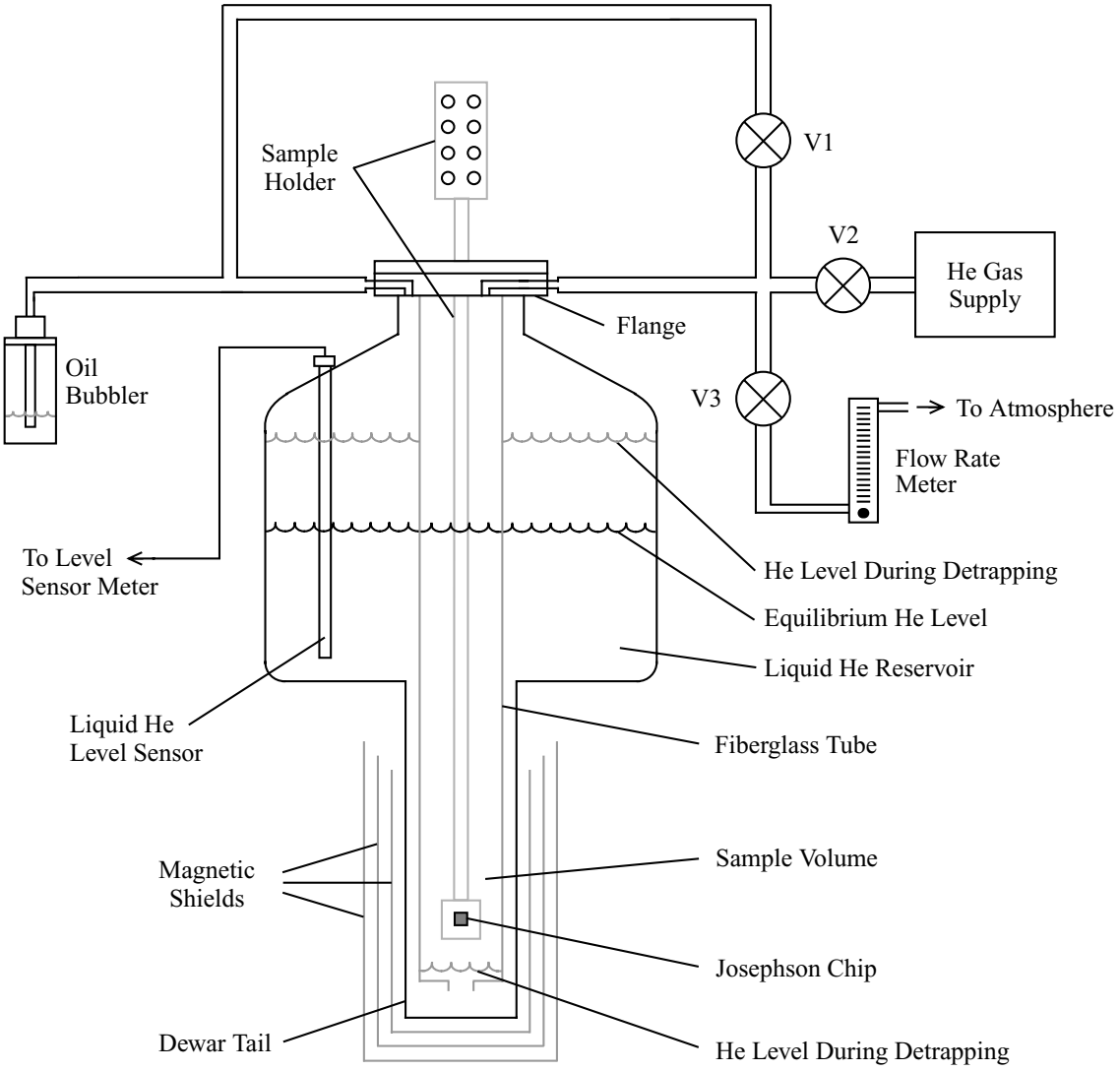


Figure 6-4: Magnetically shielded liquid helium dewar with provisions for slow cooldown of Josephson chip.

between the chambers is controlled by varying the pressure inside the sample volume. This pressure is increased and decreased by opening and closing valves V1, V2, and V3.

Except when the chip is being "detrapped" with the slow cooldown procedure, V1 is open, and V2 and V3 are closed. To prevent air from backstreaming into the dewar and forming ice, both the sample volume and the outer reservoir are vented to the atmosphere through an oil bubbler. Since the pressures in the two chambers are allowed to equalize through V1, the liquid helium levels inside and outside the fiberglass tube are even, as indicated in the figure. When the sample holder is first lowered into the dewar, the chip is cooled down to the superconducting state outside the low-field region of the sample volume, and a large amount of magnetic flux is trapped in the ground plane of the chip. Once the sample holder is fully inserted into the dewar, and the chip is inside the low-field region of the sample volume, this trapped magnetic flux is eliminated with the slow cooldown procedure.

The first step in the slow cooldown procedure is to warm the chip above T_c. Valve V1 is closed, and the sample volume is pressurized with warm helium gas by opening V2. The increased pressure in the sample volume pushes the liquid helium out the bottom of the fiberglass tube into the outer reservoir. Consequently, the liquid helium level inside the fiberglass tube drops, while the level of the reservoir rises. Since the liquid helium level sensor of the dewar measures the level inside the reservoir, the reading on the level sensor meter rises during this step of the procedure. After about 8 minutes, the reading stops rising, as all of the liquid helium has been pushed out of the sample volume. At this point, V2 is closed, and the chip slowly warms up in the vapor above the liquid helium, as illustrated in the figure. This step lasts about 7 minutes, during which the temperature of the chip rises above T_c, and the trapped magnetic flux is extinguished. Next, V3 is opened, and the excess pressure in the sample volume is released to the atmosphere through a flow rate meter. Valve V3 is adjusted to achieve the desired flow rate. As the excess pressure is slowly released, and the liquid helium flows back into the sample volume, the chip gradually cools in the vapor of the rising liquid helium. After about 6 minutes, the liquid helium level is high enough that the temperature of the chip falls below T_c. After a few more minutes, V1 is again opened, V3 is closed, and the liquid helium levels are returned to equilibrium. The Josephson chip is now ready to be tested. The total time required to complete the slow cooldown procedure is about 24 minutes.

6.1.4 Experimental Results

After the chip was slowly cooled into the superconducting state with the procedure described in the previous section, the circuit was connected to the room-temperature electronics. A Keithley 236 source-measure unit operating in its current source mode supplied the bias (3.0 mA) for the Josephson circuitry. The MSM photodiode was biased at a fairly high voltage (5 V) so that its photogenerated carriers would reach saturation velocity, and its response time would be fast. This voltage was provided by a Hewlett-Packard 6115A precision power supply. Two cascaded B & H Electronics DC3002 MIC-A amplifiers were used to increase the output of the SFQ/DC converter by 40 dB. The combined bandwidth of the cascaded amplifiers was measured to be 2.3 GHz. The amplified output was recorded with a Tektronix 11402 digital oscilloscope.

Only the first four stages of the optical pulse splitter were used in this experiment. (For this reason, the pulse splitter configuration in this experiment is described by a code of four letters, not eight.) Figure 6-5 presents the operation of the optically triggered T flip-flop for four different configurations of the pulse splitter. The oscilloscope was triggered on the 80.6 MHz pulse train generated by the laser, which is shown in Figure 6-5(a). The amplified output of the SFQ/DC converter is shown for the four different cases in Figure 6-5(b). To improve the SNR of the measurements, 1024 averages were taken for each waveform. With a pulse splitter configuration of SSSS, all the pulse rate doubling stages are disabled, and the T flip-flop is toggled at the repetition rate of the laser (top trace in Figure 6-5(b)). Other pulse splitter configurations generate more optical pulses, and the T flip-flop is toggled more often. In each case, the circuit produces the expected output pattern. The high stability of the oscilloscope traces indicates that each incident optical pulse is being reliably converted into one SFQ pulse.

Correct operation at higher frequency is shown in Figure 6-6, which demonstrates optical triggering of the T flip-flop at 1.3 GHz in both (a) continuous and (b) burst modes. With

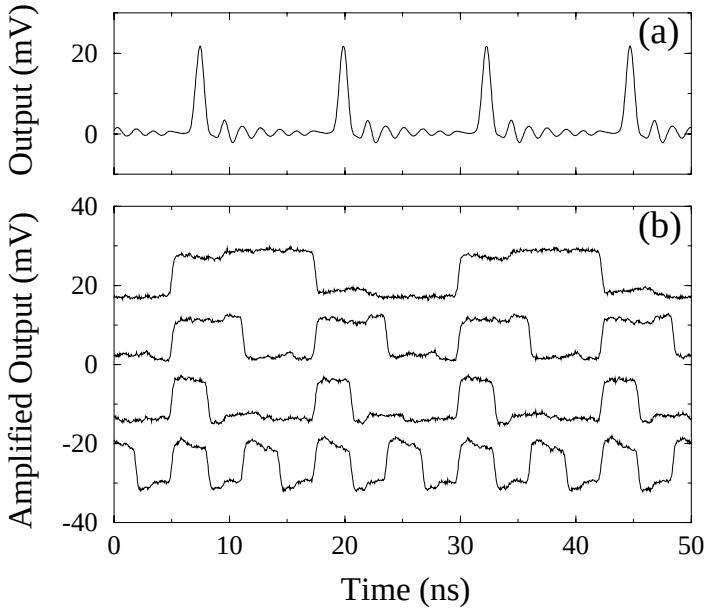


Figure 6-5: Demonstration of T flip-flop being optically triggered with different pulse patterns. (a) 80.6 MHz pulse train generated by laser (and measured with the high speed photodiode shown in Figure 5-1). (b) Circuit output for four different configurations of the optical pulse splitter. From top to bottom, the four traces (which are offset for clarity) correspond to pulse splitter configurations SSSS, XSSS, SXSS, and XXSS.

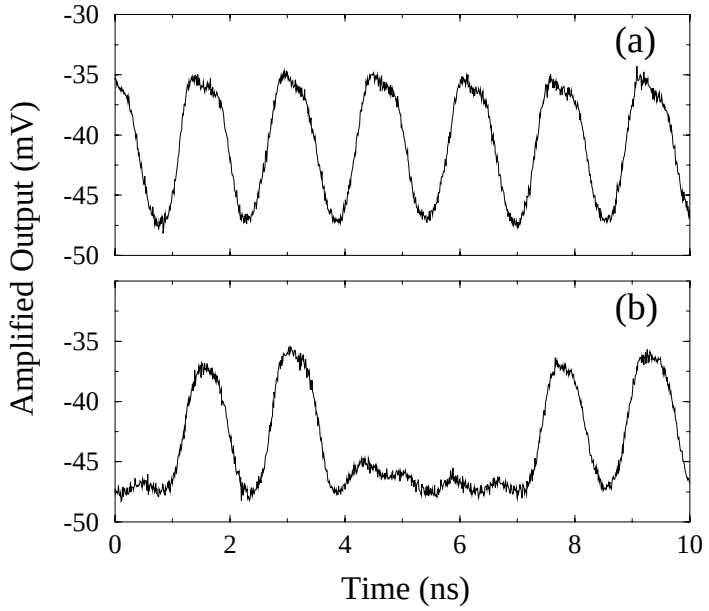


Figure 6-6: Operation of optically triggered T flip-flop at 1.3 GHz. (a) The pulse splitter configuration is XXXX. (b) The pulse splitter configuration is XSXX.

a pulse splitter configuration of XXXX, a continuous 1.3 GHz optical pulse train toggles the T flip-flop to produce an alternating stream of 1's and 0's. With a pulse splitter configuration of XSXX, a burst of four optical pulses (about 776 ps apart) arrives every 6.2 ns, triggering the T flip-flop to produce a repeating 10100000 output code at 1.3 Gbit/s.

Testing at higher frequencies was precluded by the bandwidth limitations of the cryogenic sample holder and the cascaded amplifiers mentioned above. Optical clocking at much higher frequencies was demonstrated in the optically triggered JTL experiment, which is the subject of the next section.

6.2 Optically Triggered JTL Experiment

6.2.1 Description of Experiment

In the optically triggered JTL experiment, depicted in Figure 6-7, each current pulse from the MSM photodiode switches junction J_1, generating an SFQ pulse which then propagates along the JTL formed by junctions J_2 through J_6. To determine if the correct pulse rate is being generated on the JTL, a precise measurement of the Josephson voltage is made with a nanovoltmeter (Hewlett-Packard 34420A). If each optical pulse generates one SFQ pulse on the JTL, the voltage should equal $N\Phi_0 F_{laser}$, where N is the pulse rate multiplication factor achieved by the pulse splitter, and F_{laser} is the pulse repetition rate of the laser, a frequency easily measured with a counter. In general, N equals 2^m, where m is the number of X's in the code describing the pulse splitter configuration.

The main advantage of the SFQ pulse generator shown in Figure 6-7 over the DC/SFQ converter used in the T flip-flop experiment is higher sensitivity, which reduces the optical pulse energy needed to switch the circuit – by a factor of 3, according to JSIM simulations. At the high pulse repetition rates (20.6 GHz) used in this experiment, such a reduction in the optical pulse energy is helpful in keeping down the average optical power incident on the chip. The addition of inductor L_1 and resistor R_1 to the circuit increases the range of input current pulses from the MSM photodiode for which the pulse generator produces a single SFQ pulse. After an SFQ pulse is triggered across junction J_1, a counterclockwise circulating current through the loop formed by L_1, R_1, and J_1 persists long enough to inhibit the generation of a second SFQ pulse from the same input pulse. The L_1/R_1 time constant (12 ps) is chosen so that the circulating current decays away before the next input pulse from the MSM photodiode arrives ($\approx$ 48.5 ps later for 20.6 GHz operation). According to simulation, the SFQ pulse generator of Figure 6-7 has an input margin of $\pm$ 48% when triggered by picosecond pulses from the MSM photodiode – smaller than that of the DC/SFQ converter but more than enough to accommodate the 25-30% variations in optical pulse energies.

The RSFQ circuitry shown in Figure 6-7 was laid out and fabricated on the same chip as the circuitry for the T flip-flop experiment. The layout of the optoelectronic interface is virtually identical to that shown in Figure 6-2, except in this case the MSM photodiode is located 750 μm away from the Josephson circuits. Again the chip was prepared for the experiment by gluing a glass capillary over the MSM photodiode.

In μV-level voltage measurements, thermoelectric voltages are a major source of offset error. In order to eliminate all offset errors in the measurement, a computer-controlled shutter was added to the optical clocking setup so that the voltage from the Josephson

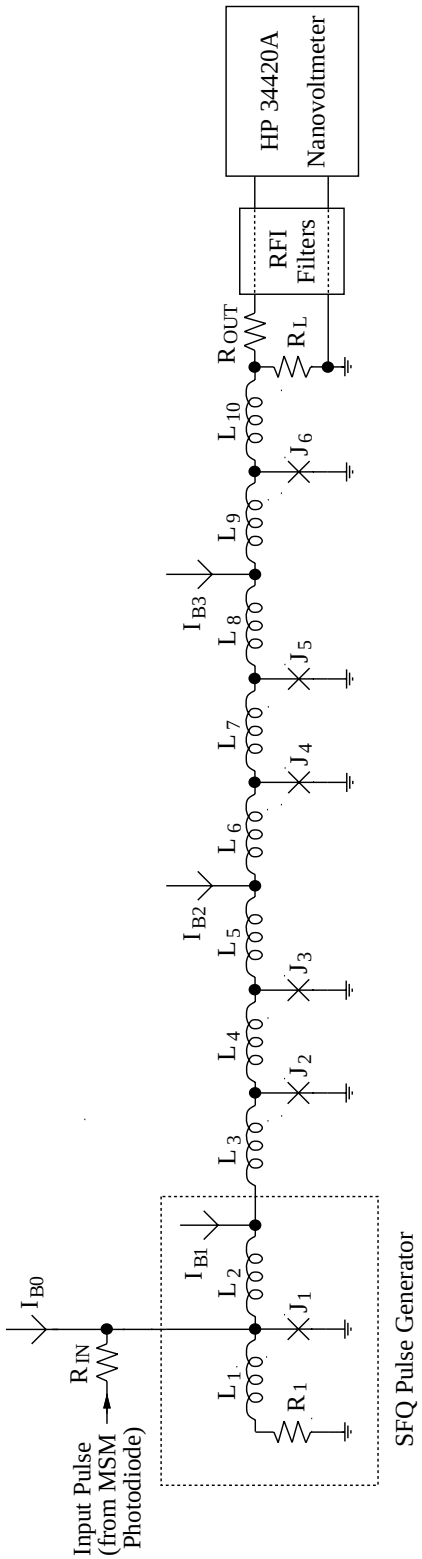


Figure 6-7: Optically triggered JTL experiment. The nominal circuit parameters are: R_{IN}=10 Ω, R_1=0.67 Ω, R_L=2 Ω, R_{OUT}=54 Ω, L_1=8 pH, L_2=1.1 pH, L_3=1.6 pH, L_4=L_7=3.9 pH, L_5=L_6=L_8=L_9=L_{10}=2.0 pH, I_{c1}=171 μA, I_{c2}=I_{c3}=I_{c4}=I_{c5}=I_{c6}=245 μA, I_{B0}=−93 μA, I_{B1}=388 μA, and I_{B2}=I_{B3}=343 μA.

chip could be measured with and without the light applied to the MSM photodiode; the difference is the actual voltage due to generation of SFQ pulses on the JTL. After 30 seconds of signal averaging, readings with a typical noise level of a few nV were obtained.

High frequency noise from the nanovoltmeter interfering with the Josephson circuitry must also be considered. To protect the Josephson circuitry from such noise, passive radio frequency interference (RFI) filters were placed between the chip and the nanovoltmeter. Both differential-mode and common-mode noises are attenuated with the RFI filters, which are shown in Figure 6-8. The differential-mode noise is suppressed with a commercial signal line filter (Lindgren LTC-2640-C10K), which is implemented with low-pass LC ladder networks. The attenuation of this filter is specified to be greater than 100 dB for frequencies between 330 kHz and 10 GHz. The common-mode noise is suppressed with ferrite beads and toroids (from Fair-Rite Products) which were applied to the coaxial cable connected to the nanovoltmeter. A total of ten beads and four toroids were used to raise the common-mode impedance of the cable above 1 kΩ over a frequency range of 1 to 500 MHz.

6.2.2 Experimental Results

The bias voltage (for the MSM photodiode) and currents (for the Josephson circuits) were supplied to the chip with the room-temperature test equipment that had been used earlier in the optically-triggered T flip-flop experiment. In this experiment, all eight stages of the optical pulse splitter were put to use.

The experimental results are summarized in Table 6.1, which presents the Josephson voltage data for nineteen different optical pulse patterns. Pulse patterns 1, 2, 6, 9, 11, 13,

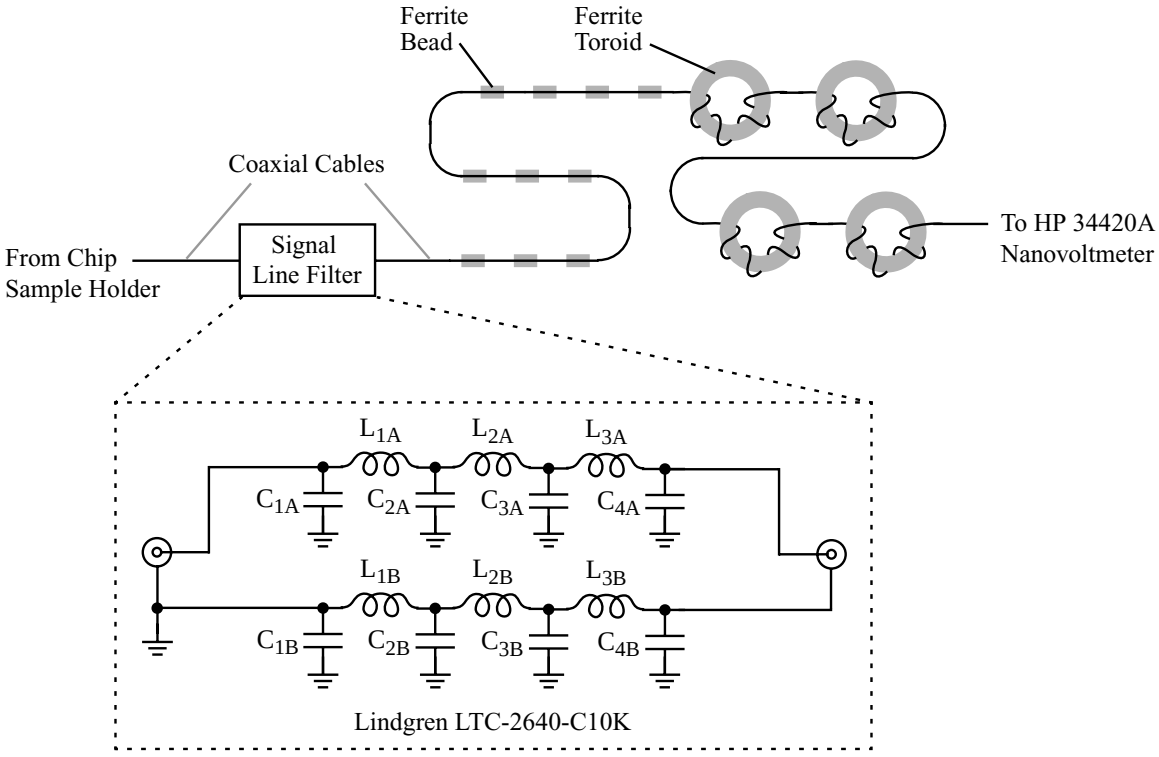


Figure 6-8: RFI filters for suppression of high frequency noise from nanovoltmeter.

Table 6.1: Josephson voltage data for nineteen different optical pulse patterns.

No.	Pulse Splitter Configuration	Voltage (μV)	N= $\frac{\text{Voltage}}{\Phi_0 F_{\text{laser}}}$
1	S S S S S S S S	0.1653	0.992
2	XS S S S S S S	0.3296	1.979
3	S S S S S S S X	0.3339	2.004
4	S S S S S S XS	0.3285	1.972
5	S S S S S XS S	0.3301	1.982
6	XXS S S S S S	0.6654	3.995
7	S S S S S S XX	0.6674	4.007
8	S S S S S XS X	0.6635	3.983
9	XXXS S S S S	1.3334	8.005
10	S S S S S XXX	1.3332	8.003
11	XXXXS S S S	2.6660	16.005
12	S S S S XXXX	2.6645	15.996
13	XXXXXS S S	5.3254	31.970
14	S S S XXXXX	5.3311	32.004
15	XXXXXXS S	10.6553	63.966
16	S S XXXXXX	10.6609	64.000
17	XXXXXXXS	21.3162	127.966
18	S XXXXXXX	21.3239	128.013
19	XXXXXXXX	42.6475	256.024

15, 17, and 19 are continuous pulse trains ranging in frequency from 80.6 MHz to 20.6 GHz. The other pulse patterns represent bursts of different numbers of pulses at various clock rates. In the last column of the table, the measured Josephson voltage is divided by $\Phi_0 F_{\text{laser}}$ to obtain N, the pulse rate multiplication factor of the pulse splitter. F_{laser} was measured with a Hewlett-Packard 5335A counter to be 80.55598 MHz. In every case, N is found to be very close to the expected value of 2^m; the biggest deviation (0.034) corresponds to a voltage error of only 5.7 nV, within the noise level of the measurements. Thus, each optical pulse pattern is generating the correct number of SFQ pulses on the JTL. (At least most of the time – Josephson voltage measurements are incapable of detecting rare errors.) For a continuous 20.6 GHz pulse train (i.e., pattern 19), the average optical power incident on the Josephson chip is about 880 μW. The average energy of the incident optical pulses is therefore about 43 fJ. An important point to make is that no adjustment of optical pulse energy or circuit bias current was made between the measurements listed in Table 6.1. Operation is effectively independent of bit pattern and clock frequency, indicating a very wide bandwidth for the optoelectronic interface.

Part III

Superconducting Bandpass Delta-Sigma Modulator

Chapter 7

Modulator Operating Principles

This chapter presents the basic design and operating principles of the superconducting bandpass $\Delta\Sigma$ modulator. An understanding of circuit operation is first developed by examining a modulator based on a lumped element LC resonator. Intuitive explanations are supported by more rigorous quantitative analysis, and various circuit refinements are discussed. Next the practical advantages and design complications of employing a transmission line resonator are considered. Modulator output spectra and ADC performance are predicted with a linearized model. Finally, the modulator described in this thesis is compared with other superconducting bandpass $\Delta\Sigma$ modulators reported in the literature.

7.1 Modulator Based on LC Resonator

The basic concept of the superconducting bandpass $\Delta\Sigma$ modulator is demonstrated with the circuit shown in Figure 7-1. An analog input current I_{in} is applied to the resonator formed by inductor L and capacitor C. The inductor current i_L is quantized by a standard SFQ timed comparator [31] comprising Josephson junctions J_1 and J_2. A high value of inductor current (above the comparator threshold) biases J_2 close to its critical current. Therefore, when the sampling pulse generator applies an SFQ pulse to the two series junctions, J_2 switches, and an SFQ pulse appears on the output of the modulator. On the other hand, if the inductor current is small (below the comparator threshold), J_2 is not driven close to its critical current, and the sampling pulse switches J_1 instead of J_2. In this case, no SFQ pulse appears on the modulator output. The binary output code of the modulator follows the RSFQ basic convention described in Section 2.2.7. Within a given period of the sampling clock, each SFQ output pulse represents a binary 1, and its absence represents a binary 0. The relative number of 1's and 0's in the modulator output code can be adjusted by adding a dc bias to the input current I_{in}.

The SFQ voltage pulses across J_2 not only represent the binary output code of the modulator but also provide feedback to the LC resonator. Each SFQ pulse generated across J_2 reduces the inductor current i_L by approximately Φ_0/L. (On the time scale of the SFQ pulse, the impedance of capacitor C is almost negligible.) The resonator feedback normally accomplished in a bandpass $\Delta\Sigma$ modulator with a separate DAC (cf. Figure 2-5) is realized here as kickback from the SFQ comparator itself. Since circuits based on two-terminal devices typically have limited isolation between input and output, the use of such

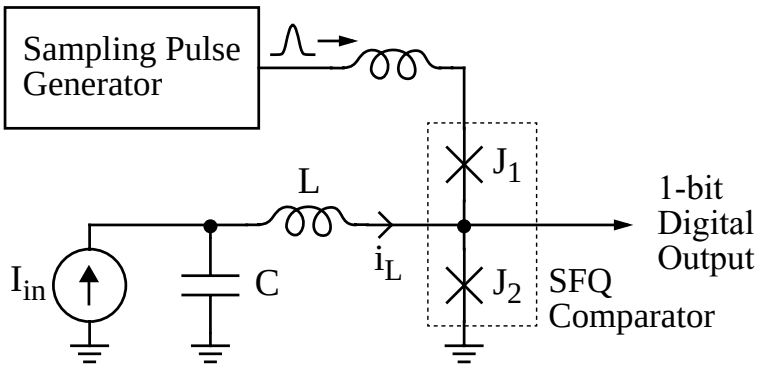


Figure 7-1: Superconducting bandpass $\Delta\Sigma$ modulator based on LC resonator.

kickback is natural in Josephson technology and is featured in several superconducting ADC designs [66, 56, 68, 129, 35, 58]. The intrinsic quantization of the SFQ pulse ensures that the feedback delivered to the resonator is precise and uniform – a critical requirement for achieving high performance in bandpass $\Delta\Sigma$ modulators [23, 130, 131].

The feedback gain achieved by this kickback effect is a function of the frequency-dependent impedance shunting junction J_2. At the resonant frequency of the series LC network, the reactances of capacitor C and inductor L cancel, and J_2 is shunted with a very low impedance (zero impedance if L and C are lossless). This low impedance magnifies the current injected back into the resonator, so that near resonance the feedback gain is very large, and quantization noise is suppressed.

While a feedback model with frequency-dependent loop gain can be used to calculate the noise shaping of the modulator, the suppression of the quantization noise at resonance also has a simple physical interpretation. Since the SFQ voltage pulses across J_2 represent the binary output code, there is a direct correspondence between quantization noise in the output code and the voltage noise across J_2. At the resonant frequency, the series LC network effectively shorts out J_2, and the voltage noise across J_2 is suppressed. Accordingly, the corresponding quantization noise is also minimized. This physical interpretation of the noise shaping process also explains why modulator performance is insensitive to Johnson noise from the damping resistors shunting J_1 and J_2. At the resonant frequency, the thermally generated noise currents from the damping resistors are shunted away from J_2 into the series LC network, whose impedance is much lower than that of a Josephson junction; consequently, such noise currents have little influence on the modulator output[1]. In general, both quantization and thermal noise are suppressed at frequencies at which J_2 is shunted with a very low impedance. This physical interpretation of noise shaping is particularly helpful in understanding more complex superconducting modulators (such as those based on transmission line resonators), for which exact analytical results are difficult to obtain. Such modulators will be discussed later in this chapter, after a more quantitative analysis

[1]The insensitivity of the modulator to Johnson noise from the damping resistors can also be explained with the feedback model (Figure 2-5). Johnson noise from the damping resistors produces threshold fluctuations in the current comparator comprising J_1 and J_2. Because of the large loop gain in front of the comparator, such comparator errors have negligible effect on the input-referred noise level of the modulator. The physical interpretation discussed above, though, provides a more intuitive, less mathematical view of the noise suppression process.

of the circuit shown in Figure 7-1.

7.1.1 Quantitative Analysis

Because the quantizer inside a $\Delta\Sigma$ modulator loop samples its input at discrete times (determined by a sampling clock with period T), a $\Delta\Sigma$ modulator can be treated as a discrete-time system, even if the loop filter is implemented with continuous-time components [131, 132]. Therefore, the first step in analyzing a continuous-time $\Delta\Sigma$ modulator is to transform it into an equivalent discrete-time system, for which difference equations and z-transform relations can be formulated. Such a transformation is now carried out for the circuit of Figure 7-1.

The transformation of a general continuous-time $\Delta\Sigma$ modulator into a discrete-time system is derived with state-space methods in [132]. The transformation given here closely follows the derivation in that paper (though state-space notation is not used). However, a different mathematical model for the feedback DAC must be assumed, as the pulses produced by the SFQ comparator differ in two basic ways from the feedback signals normally used in semiconductor $\Delta\Sigma$ modulators.

First, the pulses produced by the SFQ comparator are unipolar: within each sampling period, either a positive SFQ output pulse is generated across Josephson junction J_2, or no output pulse is generated. In contrast, the feedback pulses in most semiconductor $\Delta\Sigma$ modulators are bipolar (e.g., ± 1 V). This difference does not substantially affect either the operation or analysis of the $\Delta\Sigma$ modulator, as there is a simple relationship between unipolar and bipolar feedback, illustrated in Figure 7-2. In the figure, $v_q(t)$ represents the unipolar output pulses generated across J_2, $v_{q2}(t)$ is a bipolar feedback signal corresponding to the same output code, and $v_{q1}(t)$ is a periodic pulse train. Since $v_q(t) = v_{q1}(t) + v_{q2}(t)$, and the continuous-time circuit elements form a linear time-invariant (LTI) network, superposition can be applied in calculating the response of the LC resonator to the voltage

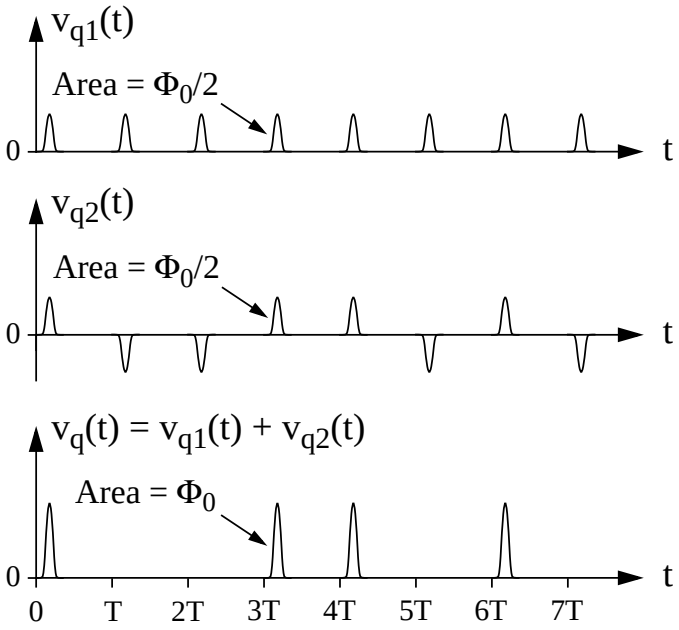


Figure 7-2: Relationship between unipolar and bipolar feedback pulses.

pulses generated across J_2. Consider the response due to periodic component $v_{q1}(t)$. By time-invariance, the resonator response is periodic with period T, so that the same value of inductor current i_L is sampled by the SFQ comparator on each clock cycle. Thus, the effect of component $v_{q1}(t)$ on modulator operation can be reduced to a fixed offset in the comparator. Since such an offset can be compensated by adding a dc bias to the input current I_{in}, the resonator response to component $v_{q1}(t)$ can be ignored. Only the resonator response to the bipolar feedback signal $v_{q2}(t)$ needs to be considered in a mathematical treatment of the modulator.

The second difference is more significant in its effect on modulator operation and cannot be ignored in the analysis. The time duration of the pulses produced by the SFQ comparator is significantly shorter than and independent of the sampling period T. In most semiconductor continuous-time $\Delta\Sigma$ modulators, the width of the feedback pulses is either T in the case of non-return-to-zero (NRZ) waveforms [131] or $T/2$ in the case of return-to-zero (RZ) waveforms [26]. Because of their relative immunity to pattern-dependent distortion (such as that caused by unequal rise and fall times), feedback DACs with RZ waveforms are the preferred option for continuous-time modulators [132]. Since the time duration of each SFQ pulse is only a small fraction of the sampling period T, the pulses produced by the SFQ comparator do not overlap in time and represent a type of RZ feedback; pattern-dependent distortion is minimal. The width of the SFQ pulse is determined not by external clock signals but by parameters of the Josephson junction itself: its critical current, capacitance, and shunt resistance (i.e., the parameters of the RSJ model discussed in Section 2.2.1). For niobium junctions with 1 kA/cm^2 critical current density (typical of present-day low-T_c superconducting technology [123]), the SFQ pulse is about[2] 4 ps wide [29]. Even at sampling rates up to 40 GHz, the SFQ pulse width is considerably shorter than $T/2$. In the analysis presented here, the bipolar pulses in feedback signal $v_{q2}(t)$ are approximated as impulses with zero width and area equal to $\pm\Phi_0/2$. The delay of the comparator is neglected in this model, so the impulses are generated right after[3] the sampling times $t = nT$. If $i_L(nT)$ is positive, a positive impulse is generated; otherwise, a negative impulse is generated.

Figure 7-3 shows the idealized circuit used for analysis of the superconducting modulator. The SFQ comparator is modeled as a voltage source equal to the bipolar impulse signal $v_{q2}(t)$ just described in the last paragraph. Voltage source v_{in}, capacitor C, and inductor L form a Thévenin equivalent circuit for the input network in Figure 7-1 provided that the Fourier transforms of the input sources are related by

$$V_{in}(j\omega) = \frac{1}{j\omega C} I_{in}(j\omega). \tag{7.1}$$

A convenient choice of state variables for analyzing this circuit is the capacitor voltage v_C

[2]The SFQ pulse width can be affected by circuit loading of the Josephson junction. The 4 ps number is accurate for a Josephson junction either unloaded or lightly loaded by other circuitry. If the junction is heavily loaded, the SFQ pulse width is broadened but still in the range of 4-10 ps. In any case, the width of the SFQ pulse is still a small fraction of the sampling period T.

[3]Each negative or positive impulse in $v_{q2}(t)$ instantaneously changes the inductor current i_L by $\pm\Phi_0/2L$. The comparator makes its decision based on the value of i_L prior to this instantaneous change. To avoid ambiguity about the value of i_L being sampled by the comparator, the impulses in the model are generated not at the sampling times $t = nT$, but at $t = nT + \delta t$, where δt is positive but arbitrarily small.

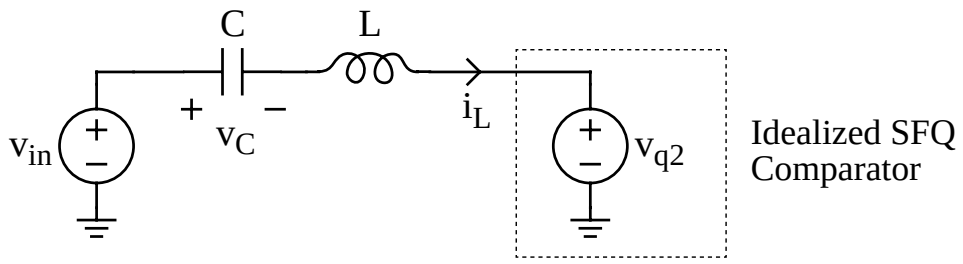


Figure 7-3: Idealized model for superconducting modulator based on LC resonator.

and the inductor flux, normalized to the area ($\Phi_0/2$) of the feedback pulses in $v_{q2}(t)$:

$$u \equiv \frac{2Li_L}{\Phi_0}. \tag{7.2}$$

With this choice of variables, the state equations for the circuit of Figure 7-3 are

$$\frac{du}{dt} = \frac{2}{\Phi_0}(v_{in} - v_C - v_{q2}), \tag{7.3a}$$

$$\frac{dv_C}{dt} = \frac{\omega_0^2 \Phi_0}{2} u, \tag{7.3b}$$

where the resonant frequency $\omega_0 = 1/\sqrt{LC}$. Solving this system of differential equations over the time interval $(n-1)T \le t \le nT$ yields

$$u(nT) = \cos(\omega_0 T)u((n-1)T) - \frac{2}{\omega_0 \Phi_0}\sin(\omega_0 T)v_C((n-1)T) + \int_{(n-1)T}^{nT}(v_{in}(\tau) - v_{q2}(\tau))h_u(nT-\tau)d\tau, \tag{7.4a}$$

$$v_C(nT) = \frac{\omega_0 \Phi_0}{2}\sin(\omega_0 T)u((n-1)T) + \cos(\omega_0 T)v_C((n-1)T) + \int_{(n-1)T}^{nT}(v_{in}(\tau) - v_{q2}(\tau))h_{vc}(nT-\tau)d\tau, \tag{7.4b}$$

where $h_u(t)$ and $h_{vc}(t)$ are the respective responses of states u and v_C to a unit impulse on input v_{in}:

$$h_u(t) = \begin{cases} 0 & \text{if } t < 0, \\ \frac{2}{\Phi_0}\cos\omega_0 t & \text{if } t \ge 0, \end{cases} \tag{7.5a}$$

$$h_{vc}(t) = \begin{cases} 0 & \text{if } t < 0, \\ \omega_0 \sin\omega_0 t & \text{if } t \ge 0. \end{cases} \tag{7.5b}$$

Only one impulse in feedback signal $v_{q2}(t)$ lies in the time interval $(n-1)T \le t \le nT$, so

$$\int_{(n-1)T}^{nT} v_{q2}(\tau)h_u(nT-\tau)d\tau = \frac{\Phi_0}{2}\text{sgn}(u[n-1])h_u(T) = \text{sgn}(u[n-1])\cos\omega_0 T \tag{7.6a}$$

and

$$\int_{(n-1)T}^{nT} v_{q2}(\tau)h_{vc}(nT-\tau)d\tau = \frac{\Phi_0}{2}\text{sgn}(u[n-1])h_{vc}(T) = \frac{\omega_0\Phi_0}{2}\text{sgn}(u[n-1])\sin\omega_0 T, \quad (7.6b)$$

where

$$\text{sgn}(x) = \begin{cases} -1 & \text{if } x < 0, \\ 1 & \text{if } x \geq 0, \end{cases} \quad (7.7)$$

and the discrete-time sequence $u[n] = u(nT)$. Following similar notation, $v_C[n] = v_C(nT)$. After substitution of Equations 7.6, Equations 7.4 become

$$u[n] = \cos(\omega_0 T)(u[n-1] - \text{sgn}(u[n-1])) - \frac{2}{\omega_0\Phi_0}\sin(\omega_0 T)v_C[n-1] + g_u[n], \quad (7.8a)$$

$$v_C[n] = \frac{\omega_0\Phi_0}{2}\sin(\omega_0 T)(u[n-1] - \text{sgn}(u[n-1])) + \cos(\omega_0 T)v_C[n-1] + g_{vc}[n], \quad (7.8b)$$

where

$$g_u[n] = \int_{(n-1)T}^{nT} v_{in}(\tau)h_u(nT-\tau)d\tau, \quad (7.9a)$$

and

$$g_{vc}[n] = \int_{(n-1)T}^{nT} v_{in}(\tau)h_{vc}(nT-\tau)d\tau. \quad (7.9b)$$

Because of the normalization used in defining state variable u, each negative or positive impulse in $v_{q2}(t)$ changes u by ± 1. With quantization levels at ± 1, the modulator output $y[n] = \text{sgn}(u[n])$. If, as discussed in Section 2.1.2, the comparator is modeled as a source of additive white noise $e[n]$, $y[n] = u[n] + e[n]$. Therefore, Equations 7.8 can be rewritten as

$$u[n] = -\cos(\omega_0 T)e[n-1] - \frac{2}{\omega_0\Phi_0}\sin(\omega_0 T)v_C[n-1] + g_u[n], \quad (7.10a)$$

$$v_C[n] = -\frac{\omega_0\Phi_0}{2}\sin(\omega_0 T)e[n-1] + \cos(\omega_0 T)v_C[n-1] + g_{vc}[n]. \quad (7.10b)$$

The signal transfer function (STF) and noise transfer function (NTF) of the modulator are calculated by applying z-transforms to Equations 7.10, with $z = e^{j\omega T}$. The algebraic manipulations are somewhat lengthy and are presented in Appendix A. There it is shown that the z-transform of the output $y[n]$ is related to the z-transforms of the sampled input voltage $v_{in}[n] = v_{in}(nT)$ and the quantization error $e[n]$ by

$$Y(e^{j\omega T}) = \text{STF}(e^{j\omega T})V_{in}(e^{j\omega T}) + \text{NTF}(e^{j\omega T})E(e^{j\omega T}) \quad \text{for } |\omega| \leq \pi/T, \quad (7.11)$$

where

$$\text{STF}(e^{j\omega T}) = \frac{j2\omega}{\Phi_0} \cdot \frac{1 - 2\cos(\omega_0 T)e^{-j\omega T} + e^{-j2\omega T}}{(\omega_0^2 - \omega^2)(1 - \cos(\omega_0 T)e^{-j\omega T})}, \quad (7.12)$$

and

$$\text{NTF}(e^{j\omega T}) = \frac{1 - 2\cos(\omega_0 T)e^{-j\omega T} + e^{-j2\omega T}}{1 - \cos(\omega_0 T)e^{-j\omega T}}. \quad (7.13)$$

Direct evaluation shows that $\text{NTF}(e^{j\omega T}) = 0$ for $\omega = \pm\omega_0$. As desired, there is a null in

the quantization noise spectrum at the resonant frequency of the LC network. The STF given in Equation 7.12 also has zeros at $\omega = \pm\omega_0$, but these zeros are cancelled out by poles corresponding to the $\omega_0^2 - \omega^2$ term in the denominator. Because of these pole-zero cancellations, the STF of the modulator is fairly flat over a broad band of frequencies spanning ω_0. The magnitudes of the STF and NTF given in Equations 7.12 and 7.13 are plotted in Figure 7-4 for resonant frequency ω_0 equal to (a) one-tenth the sampling rate and (b) one-quarter the sampling rate. In each plot, the STF is normalized to its magnitude at $\omega = \omega_0$. Both the band-reject noise shaping of the NTF and the flat response of the STF near frequency ω_0 are evident in the figure. The magnitude of the STF peaks at a frequency more than 30% higher than ω_0; the magnitude of the STF at $\omega = \omega_0$ is lower than this peak value, but only slightly (< 1 dB).

A simple expression for the magnitude of the STF at $\omega = \omega_0$ can be obtained by applying l'Hôpital's rule:

$$\begin{aligned} |\mathrm{STF}(e^{j\omega_0 T})| &= \left| \frac{2\omega_0}{\Phi_0} \cdot \frac{2T\cos(\omega_0 T)e^{-j\omega_0 T} - 2Te^{-j2\omega_0 T}}{2\omega_0(1-\cos(\omega_0 T)e^{-j\omega_0 T})} \right| \\ &= \frac{2T}{\Phi_0} \left| \frac{-e^{-j2\omega_0 T}(1-\cos(\omega_0 T)e^{j\omega_0 T})}{1-\cos(\omega_0 T)e^{-j\omega_0 T}} \right| = \frac{2T}{\Phi_0}. \end{aligned} \tag{7.14}$$

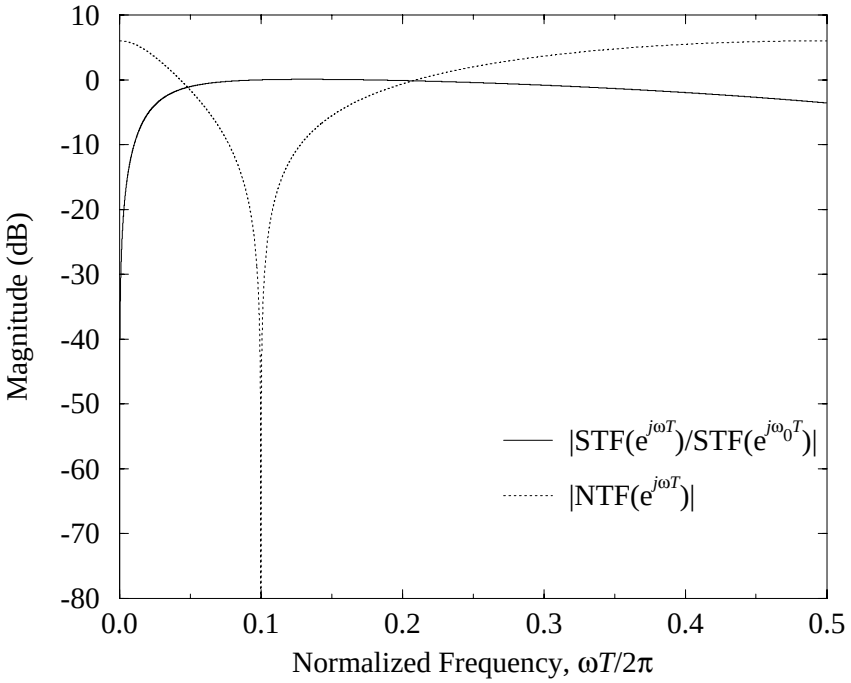
Since modulator output $y[n]$ oscillates between ± 1 quantization levels, a full-scale output has an amplitude of unity. For an input tone at frequency ω_0, the input amplitude needed to produce a full-scale output equals

$$v_{fs} = \frac{1}{\mathrm{STF}(e^{j\omega_0 T})} = \frac{\Phi_0}{2T}. \tag{7.15}$$

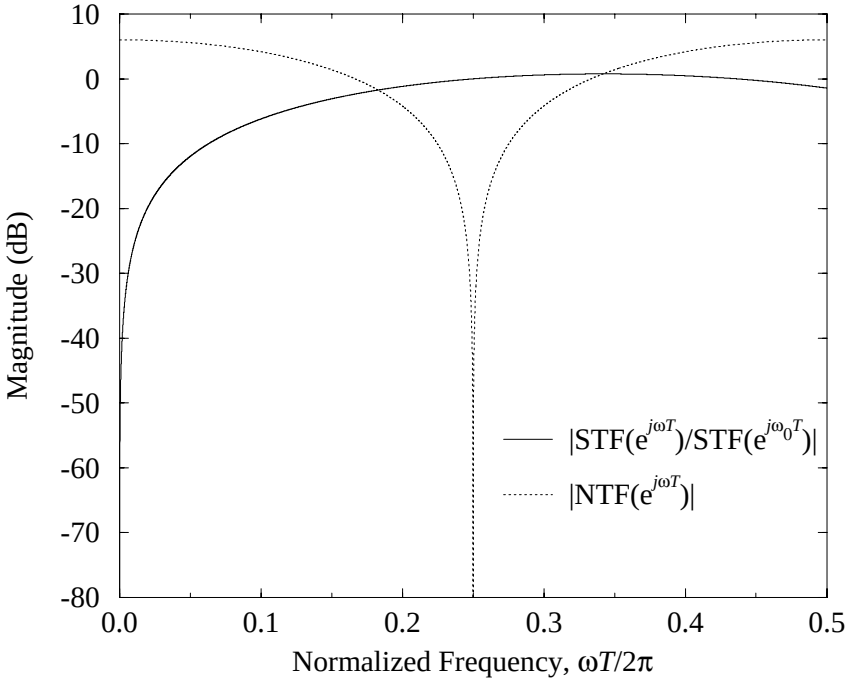
The full-scale input voltage given in Equation 7.15 is closely related to the Josephson voltage. Near resonance, the impedance of the series LC network is much lower than that of a Josephson junction, and the voltage source v_{in} in the Thévenin equivalent input circuit is directly impressed upon junction J_2 of the SFQ comparator. A full-scale output is attained when the average voltage across J_2 is modulated between 0 (corresponding to all 0's in the output code) and Φ_0/T (corresponding to all 1's in the output code). Assuming that the modulator is biased near the midpoint of this range (producing about half 1's and 0's), these limits are reached when the zero-to-peak ac voltage across J_2 equals $\Phi_0/2T$ – precisely the value given in Equation 7.15.

This intuitive view of modulator operation, in which a Thévenin equivalent input voltage (with negligible source impedance near resonance) is directly impressed upon the lower junction of the SFQ comparator, shows that the relationship between the full-scale input voltage and the Josephson voltage is fundamental and holds true for other superconducting modulators. This relationship is especially useful in estimating the input sensitivity of more complex modulators (such as those based on transmission line resonators), for which the exact STF cannot be analytically derived. Once the relationship between the actual input source and the Thévenin equivalent input voltage is determined, the amplitude of a full-scale input follows from Equation 7.15.

The signal transfer function given in Equation 7.12 describes the response of the modulator to Thévenin equivalent input voltage v_{in}. The actual input source in the modulator of Figure 7-1 is current source I_{in}. Since v_{in} and I_{in} are related by Equation 7.1, the signal



(a)



(b)

Figure 7-4: Signal and noise transfer functions of superconducting modulator based on LC resonator with (a) $\omega_0 = \pi/5T$ and (b) $\omega_0 = \pi/2T$.

transfer function describing the response of the modulator to current source I_{in} equals

$$\mathrm{STF}_I(e^{j\omega T}) = \frac{1}{j\omega C}\mathrm{STF}(e^{j\omega T}) = \frac{2}{C\Phi_0} \cdot \frac{1 - 2\cos(\omega_0 T)e^{-j\omega T} + e^{-j2\omega T}}{(\omega_0^2 - \omega^2)(1 - \cos(\omega_0 T)e^{-j\omega T})}. \tag{7.16}$$

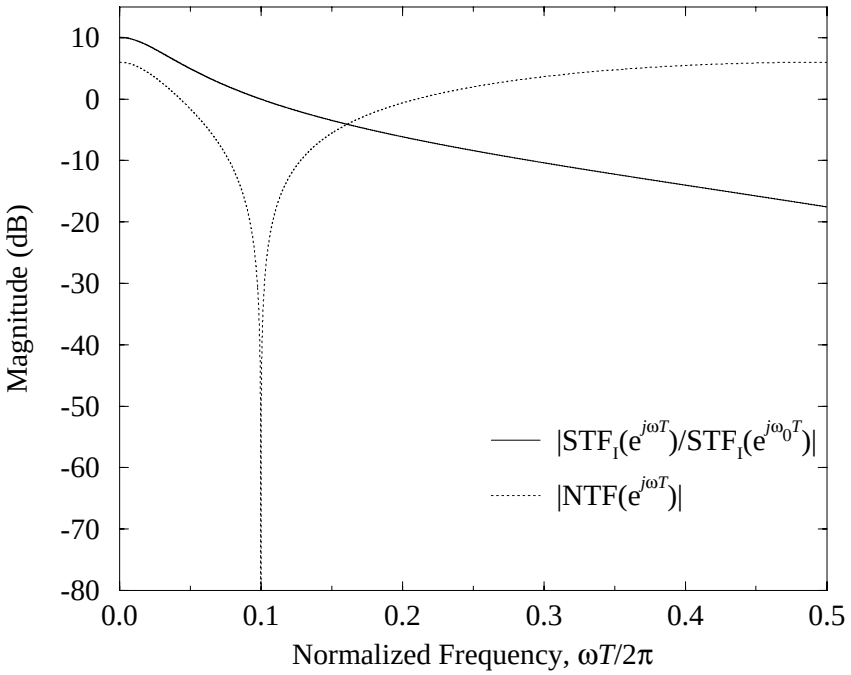
The magnitudes of this signal transfer function and the noise transfer function given in Equation 7.13 are plotted in Figure 7-5; the values of ω_0 match those in Figure 7-4. The signal transfer function is still fairly flat near resonant frequency ω_0, but its magnitude is now largest at low frequencies.

7.1.2 Circuit Refinements

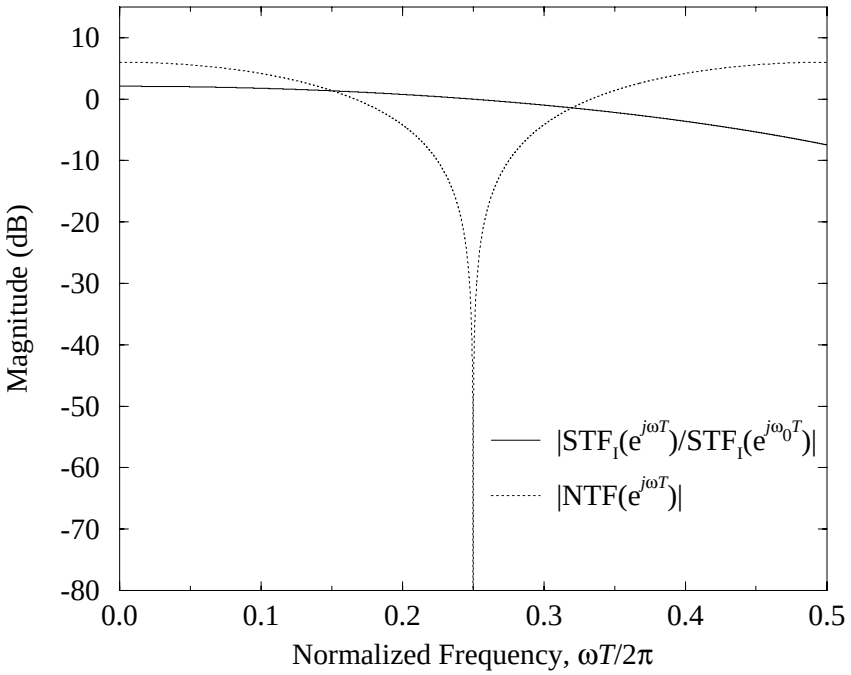
The circuit of Figure 7-1 represents the simplest possible implementation of the superconducting bandpass $\Delta\Sigma$ modulator. Though feasible in such a form, the modulator can be significantly improved with only minor circuit modifications.

The first such modification reduces the sensitivity of modulator operating point to device parameters. In order to accommodate the largest possible input signal and achieve the maximum dynamic range, the SFQ comparator should be biased to produce about half 1's and half 0's in the output code. In principle, the operating point of the comparator can be adjusted by adding a dc bias to the input current I_{in}, but the required bias current depends on a large number of factors: the RSJ parameters of the Josephson junctions, the resonator impedance, circuit loading of the comparator output, even the level of thermal noise [133]. A more robust method of setting the modulator operating point is to bias the lower Josephson junction of the comparator with a voltage source instead of a current source, as shown in Figure 7-6. Since no dc voltage is dropped across superconducting inductor L_b, source V_b fixes the average voltage across junction J_2; by the Josephson voltage-frequency relation, the average rate of SFQ pulses produced by the comparator is stabilized. An output code with approximately equal numbers of 1's and 0's is obtained by setting V_b close to $f_s\Phi_0/2$, where the sampling rate $f_s = 1/T$. Near the resonant frequency ω_0, the impedance of the series LC network is much lower than that of bias inductor L_b, and the bias network has little effect on the STF and NTF of the modulator. The circuit of Figure 7-6 is self-biasing, in that the current through inductor L_b automatically compensates for comparator offset caused by variations in device parameters.

Such insensitivity to device parameters is only achieved if the source impedance of bias voltage V_b is much lower than that of a Josephson junction. Two approaches to creating a very low impedance bias voltage are depicted in Figure 7-7. In the first approach (Figure 7-7(a)), a dc voltage is generated by driving an external current I_b through grounded resistor R_b, whose value is only a few mΩ. The external current needed to develop the desired voltage across such a low-value resistor is fairly high (in the tens of mA), but the power dissipated in resistor R_b is negligible (below 1 μW). In the second approach (Figure 7-7(b)), a bias voltage with zero source resistance and virtually perfect accuracy is obtained by filtering the output of an SFQ pulse generator with a low-pass filter; such a voltage source is a key circuit in a superconducting low-pass ADC based on phase modulation [134]. The RSFQ T flip-flop operates as a divide-by-two prescaler and generates SFQ pulses at a frequency $f_s/2$. After these pulses propagate through a JTL amplifier, their ac components are rejected with the low-pass filter formed by inductor L_0 and resistor R_0. (If more attenuation of ac ripple is needed, a higher-order RL filter may be used.) The output of the



(a)



(b)

Figure 7-5: Signal and noise transfer functions of superconducting modulator based on LC resonator when driven by current source I_{in}. (a) $\omega_0 = \pi/5T$. (b) $\omega_0 = \pi/2T$.

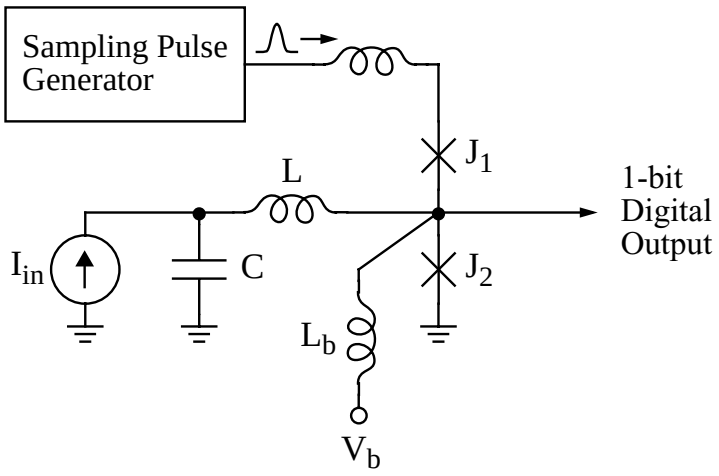
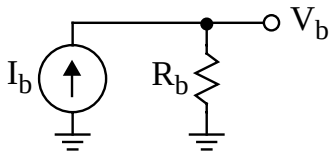
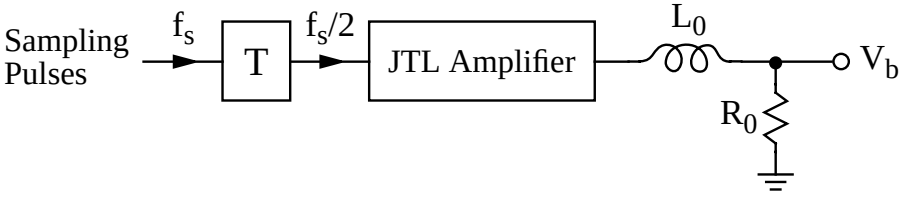


Figure 7-6: Superconducting modulator with improved bias circuitry.



(a)



(b)

Figure 7-7: Methods for generating bias voltage V_b. (a) Low-value resistor driven by external current source. (b) Josephson voltage source with RL low-pass filter.

low-pass filter is a dc voltage precisely equal to $f_s\Phi_0/2$. The source resistance of this bias circuit is zero provided that the last Josephson junction in the JTL amplifier is large enough that its switching is not hindered by load current. Almost paradoxically, the very accuracy of this circuit is its biggest drawback in this application. Low-order $\Delta\Sigma$ modulators such as bandpass modulators with a single resonator are prone to idle tone problems when biased at exactly half of full-scale [53]. Biasing the modulator slightly away from half of full-scale (so that, for instance, the fraction of 1's in the output code is 51.2%) reduces susceptibility to idle tones with negligible degradation of dynamic range [54]. Unfortunately, the superconducting modulator cannot be biased away from half of full-scale with the circuit of Figure 7-7(b), as bias voltage V_b is fixed by the Josephson voltage-frequency relation. In contrast, the bias voltage generated by the circuit of Figure 7-7(a) can be varied with external current I_b. For this reason, the circuit of Figure 7-7(a) is the preferred choice in

this application.

The next modification improves comparator performance near metastability. Like any regenerative comparator, the SFQ comparator may be driven into metastability by inputs close to its threshold. As shown in the next chapter, the speed with which the comparator recovers from this condition is the main limiting factor in the performance of the superconducting modulator. For fastest recovery, the comparator should be biased so that the regenerative time constant during metastability is as short as possible. Since the nonlinear inductance of a Josephson junction is related to its phase ϕ by [28]

$$L_J = \frac{\Phi_0}{2\pi I_c \cos\phi}, \tag{7.17}$$

the smallest negative inductances and, consequently, shortest regenerative time constant are obtained if the phases of comparator junctions J_1 and J_2 are close to π in the metastable condition. In the pendulum analogy reviewed in Section 2.2.1, both pendula should be fully inverted, pointing straight up. Because of the Josephson voltage-phase relation, application of the sampling SFQ pulse increases the phase drop across the two series junctions by 2π. Until the comparator recovers from metastability and completes its decision, the two junction phases are approximately equal, so both phases increase by about π when the sampling pulse is applied. If the junction phases are near zero before the sampling pulse arrives, the junction phases will be close to π after the sampling pulse arrives, and recovery from metastability will be relatively quick. Therefore, the comparator junctions should be biased at low currents prior to arrival of the sampling pulse. The modification presented here is a practical method of achieving such a bias condition.

In an actual implementation, the sampling pulse is delivered to the SFQ comparator with a JTL amplifier, such as the one formed by Josephson junctions J_{C1} and J_{C2} in Figure 7-8. For the moment, assume that $I_0 = 0$. L_c is the coupling inductance between J_{C2} and the upper junction of the comparator, J_1. L_c must be a small inductance; otherwise, the phase drop across J_1 and J_2 is not well controlled, and both junctions of the comparator may switch upon application of the sampling pulse, resulting in a faulty mode of operation [135]. Achieving high gain in the JTL amplifier requires that junctions J_{C1} and J_{C2} be biased close to their critical currents. Since the phase of J_{C2} is relatively large, and L_c is a small inductance, substantial current flows through L_c into series junctions J_1 and J_2, biasing the comparator junctions at current levels which are too high for rapid recovery from metastability. A more optimal bias condition for the comparator can be achieved by adding an extra current source to the circuit. If I_0 is adjusted to equal the current flowing through L_c, the bias currents of J_1 and J_2 will be small, and recovery from metastability will be fast. While source I_0 does draw dc current away from J_{C2}, a change in JTL operating point can be compensated by increasing bias current I_C and modifying the inductances between junctions J_{C1} and J_{C2}. In the experiments presented later in this thesis, I_0 was generated with an external current source and was varied for best modulator performance.

Other modifications to the modulator make the circuit more compatible with finite source resistances. A typical signal source at microwave frequencies is neither a current source nor a voltage source but has a source resistance R_s matched to that of a transmission line (e.g., 50 Ω for most coaxial cables). If such a signal source is directly connected to the resonator, the finite source resistance may spoil the loaded Q of the resonator, increasing the quantization noise at the center frequency of the modulator. Low resonator Q also

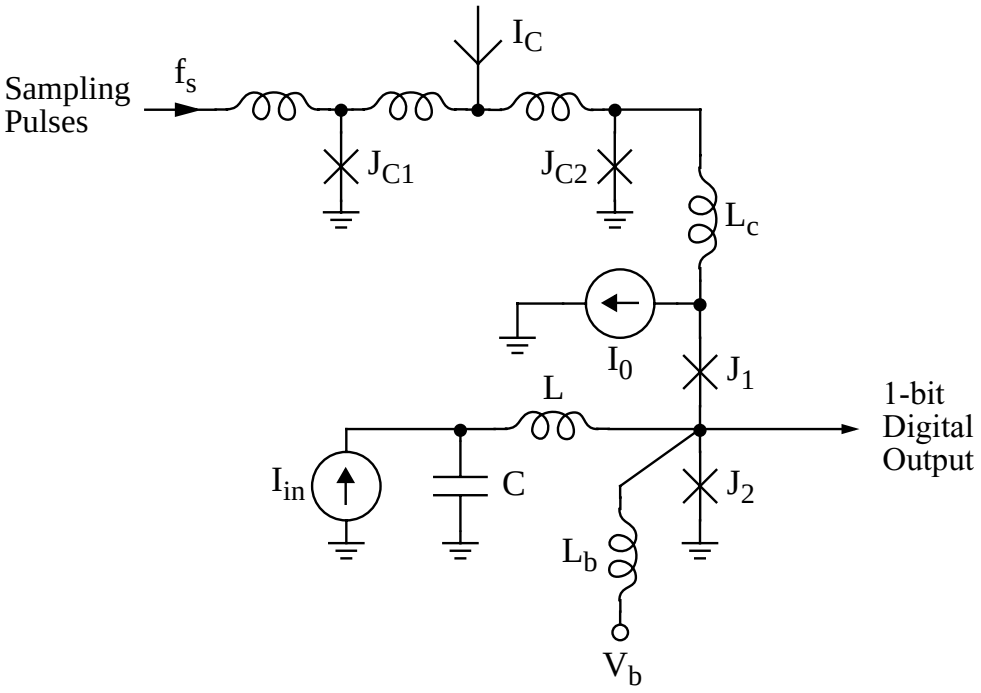


Figure 7-8: Superconducting modulator with comparator biased for faster recovery from metastability.

causes idle tone problems [23]. As an example, if current source I_{in} in Figure 7-1 is replaced by a signal generator with source resistance R_s, the loaded Q is[4]

$$Q_{ld} = \frac{R_s}{\omega_0 L}. \tag{7.18}$$

Resonant frequency ω_0 is dictated by application requirements, while selection of inductance L is constrained by signal level considerations. Each SFQ output pulse generated by the comparator reduces the inductor current by approximately Φ_0/L. If L is too large, modulator performance will be limited by thermal noise, as the current fed back to the resonator will not be much higher than the intrinsic noise level of the comparator (typically, a few μA [136]). If L is too small, the low impedance of the resonator will load the comparator heavily, and switching speed will suffer. An inductance L close to 50 pH represents a good compromise. For a center frequency equal to 2 GHz, $L = 50$ pH, and $R_s = 50\ \Omega$, the loaded Q is 80. A modulator design with such a modest value of loaded Q does not provide optimal noise shaping for narrowband applications and fails to take full advantage of the low loss of superconductivity. Indeed, even some semiconductor bandpass $\Delta\Sigma$ modulators operating at room-temperature have resonators with loaded Q values above 100 [137].

A higher loaded Q can be obtained if the source is coupled to the resonator through a passive network composed of resistors, capacitors, inductors, or transmission lines. In principle, such networks can be quite complex and might include prefilters for better rejection of out-of-band signals, but only the simplest networks are considered here. In Figure 7-9, the

[4]Resonator losses which limit the unloaded Q are not considered here.

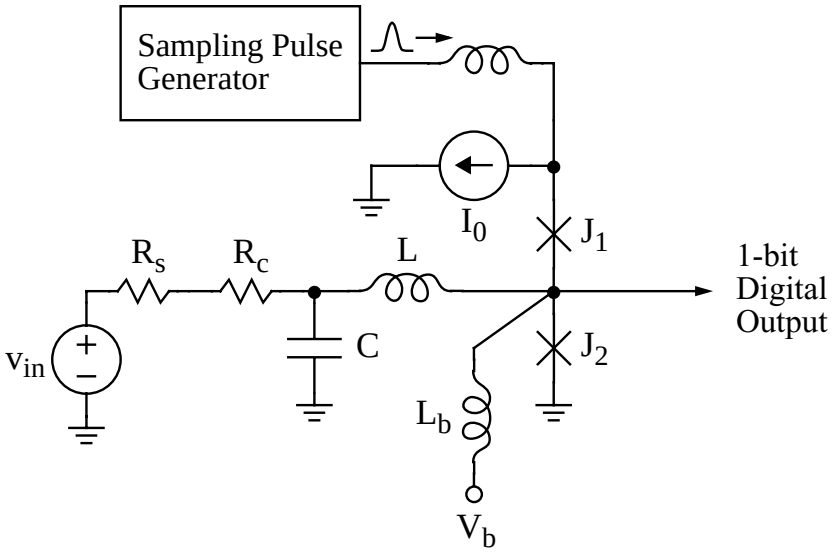


Figure 7-9: Superconducting modulator with signal source coupled to resonator through resistor R_c.

source is coupled to the resonator through resistor R_c. Since the loaded Q of the resonator is now

$$Q_{ld} = \frac{R_s + R_c}{\omega_0 L}, \tag{7.19}$$

a large enhancement of loaded Q can be achieved if $R_c \gg R_s$.

The penalty paid for such Q enhancement is reduced input sensitivity. As explained in the previous section, the superconducting modulator produces a full-scale output when the Thévenin equivalent voltage of the input network has an amplitude equal to $\Phi_0/2T$ (Equation 7.15). In this case, the input network connected to the SFQ comparator comprises source v_{in}, resistors R_s and R_c, capacitor C, and inductors L and L_b. Letting v_{th} be the Thévenin equivalent voltage (at the port connected to the comparator), standard network analysis shows that

$$V_{th}(j\omega) = \frac{j\omega L_b}{R_s + R_c - \omega^2 C(R_s + R_c)(L + L_b) + j\omega(L + L_b)} V_{in}(j\omega). \tag{7.20}$$

Since input frequencies near the modulator center frequency are of primary interest, this equation is evaluated at $\omega = \omega_0$:

$$V_{th}(j\omega_0) = \frac{-j\omega_0 L_b}{\omega_0^2 L_b C(R_s + R_c) - j\omega_0(L + L_b)} V_{in}(j\omega_0). \tag{7.21}$$

The first term in the denominator is much larger than the second term, assuming that $Q_{ld} \gg 1$ and L_b is at least comparable to L. Therefore,

$$V_{th}(j\omega_0) \approx \frac{-j}{\omega_0 C(R_s + R_c)} V_{in}(j\omega_0) = \frac{-j\omega_0 L}{R_s + R_c} V_{in}(j\omega_0) = \frac{-j}{Q_{ld}} V_{in}(j\omega_0). \tag{7.22}$$

Since the amplitude of v_{in} is larger than that of v_{th} by a factor of Q_{ld}, the input amplitude

needed to produce a full-scale output is (approximately)

$$v_{in,fs} \approx \frac{Q_{ld}\Phi_0}{2T}. \tag{7.23}$$

Thus, an increase in loaded Q reduces the input sensitivity proportionately.

Alternatively, the source can be coupled to the resonator with a small capacitor C_c, as shown in Figure 7-10. Because the coupling capacitor is not dissipative like a resistor, capacitive coupling permits a better tradeoff between loaded Q and input sensitivity than that given in Equation 7.23. A general expression for the Q of a resonant circuit is [138]

$$Q = \frac{\omega_0 W_t}{P_d}, \tag{7.24}$$

where W_t is the total stored energy, and P_d is the average power dissipation at resonance. Assuming that the load placed on the resonator by R_s and C_c is small (a necessary condition for even modest values of loaded Q), W_t is approximately equal to the stored energy of the unloaded LC resonator:

$$W_t \approx \frac{1}{2} C V_0^2, \tag{7.25}$$

where V_0 is the amplitude of the oscillating voltage across capacitor C. Resistor R_s is the only dissipative element in the circuit, so

$$P_d = \frac{V_0^2}{2} \Re e \left\{ \frac{1}{R_s + \frac{1}{j\omega_0 C_c}} \right\} = \frac{V_0^2}{2} \cdot \frac{\omega_0^2 R_s C_c^2}{1 + \omega_0^2 R_s^2 C_c^2}. \tag{7.26}$$

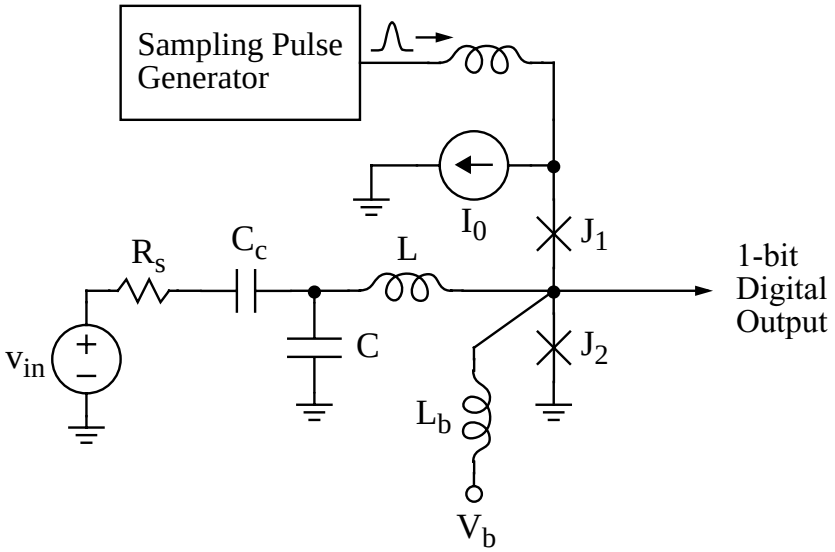


Figure 7-10: Superconducting modulator with signal source coupled to resonator through capacitor C_c.

Therefore, according to Equation 7.24,

$$Q_{ld} \approx \frac{C(1+\omega_0^2 R_s^2 C_c^2)}{\omega_0 R_s C_c^2} = Q_{ld0}\left(1+\frac{1}{\omega_0^2 R_s^2 C_c^2}\right), \tag{7.27}$$

where $Q_{ld0} = \omega_0 R_s C = R_s/\omega_0 L$; comparison with Equation 7.18 shows that Q_{ld0} is the loaded Q obtained by connecting the signal source directly to the resonator. For values of C_c large enough that $\omega_0 R_s C_c \gg 1$, the coupling capacitor is effectively a short at the resonant frequency, and $Q_{ld} \approx Q_{ld0}$. For values of C_c small enough that $\omega_0 R_s C_c \ll 1$, the resonator is coupled to the source much more weakly, and the loaded Q is much higher.

The input sensitivity of the modulator is again estimated by calculating the Thévenin equivalent voltage of the input network (at the port connected to the comparator). Standard network analysis shows that

$$V_{th}(j\omega) = \frac{-\omega^2 L_b C_c}{(1+j\omega R_s C_c)(1-\omega^2 C(L+L_b)) - \omega^2 C_c(L+L_b)} V_{in}(j\omega). \tag{7.28}$$

Evaluation of this equation at $\omega = \omega_0$ yields

$$V_{th}(j\omega_0) = \frac{L_b C_c}{L_b C(1+j\omega_0 R_s C_c) + C_c(L+L_b)} V_{in}(j\omega_0). \tag{7.29}$$

The first term in the denominator is much larger than the second term, assuming that $\sqrt{Q_{ld}Q_{ld0}} \gg 1$ and L_b is at least comparable to L. Therefore,

$$V_{th}(j\omega_0) \approx \frac{C_c}{C(1+j\omega_0 R_s C_c)} V_{in}(j\omega_0). \tag{7.30}$$

From this relationship between v_{th} and v_{in}, it follows that the input amplitude needed to produce a full-scale output is

$$v_{in,fs} \approx \frac{C\sqrt{1+\omega_0^2 R_s^2 C_c^2}}{C_c} \cdot \frac{\Phi_0}{2T}. \tag{7.31}$$

From Equation 7.27 and the definition of Q_{ld0},

$$\sqrt{Q_{ld}Q_{ld0}} \approx \frac{C\sqrt{1+\omega_0^2 R_s^2 C_c^2}}{C_c}, \tag{7.32}$$

so Equation 7.31 can be rewritten as

$$v_{in,fs} \approx \frac{\sqrt{Q_{ld}Q_{ld0}}\Phi_0}{2T}. \tag{7.33}$$

For values of C_c large enough that $\omega_0 R_s C_c \gg 1$, $Q_{ld} \approx Q_{ld0}$, and the input sensitivity matches that achieved by connecting the source directly to the resonator. As Q_{ld} is increased by reducing the coupling capacitance, the input sensitivity decreases, but only with a square root dependence on loaded Q, not proportionately as in the case of resistive coupling (cf. Equation 7.23). For very high values of loaded Q (i.e., $Q_{ld} \gg Q_{ld0}$), the input sensitivity with capacitive coupling is significantly higher than with resistive coupling.

Besides having a fundamental advantage in sensitivity, capacitive coupling is also more practicable than resistive coupling in current superconducting technology. A resistor on the order of 1 kΩ is needed to obtain a high loaded Q with resistive coupling. Such a resistor would have a very large length-to-width ratio, as the sheet resistance of thin film resistors in typical Josephson circuit processes is only about 1 Ω/□ [123]. The parasitic capacitance of a resistor with the required dimensions would be too large for the resistor to be usable at microwave frequencies. In contrast, a coupling capacitor with the required value (typically, in the range 0.1-0.5 pF) is easily realized by overlapping two superconducting wiring layers to form a parallel plate structure. Even for C_c=0.5 pF, the area of such a capacitor is small – less than 80×80 μm^2 for typical process parameters. A capacitor of such dimensions can be considered a lumped element at all frequencies of interest.

7.1.3 Difficulty of Implementation

The circuit shown in Figure 7-10 would be a practical design for a superconducting bandpass ΔΣ modulator if all the circuit elements were realizable. As just discussed, a coupling capacitor C_c in the range of 0.1-0.5 pF is easily fabricated in current superconducting technology. Implementation of inductors with the required values (about 50 pH for L and 100 pH for L_b) is also straightforward, as such inductances are not uncommon in Josephson circuits [68, 35, 58]. The real challenge is implementation of capacitor C, the value of which is set by the resonant frequency $\omega_0 = 1/\sqrt{LC}$. For a modulator center frequency equal to 2 GHz, and L = 50 pH, the required value of C is 127 pF – a large capacitance for a Josephson integrated circuit. As explained in the last section, L is constrained by signal level considerations to be about 50 pH, so C cannot be significantly reduced by increasing L.

Because capacitors in Josephson technology are made from superconducting wiring layers separated by relatively thick insulation, specific capacitance is small, and capacitor areas are large. As an example, the specific capacitance between the M1 and M0 layers in the HYPRES process is nominally 0.277 fF/μm^2 [123]. The area of a 127 pF capacitor made from these layers is 677×677 μm^2. As demonstrated by the optoelectronic sampling experiments described in Chapter 4, the electromagnetic wave velocity along microstrip-like structures in superconducting technology is about 100 μm/ps, so a capacitor of such dimensions cannot be considered a lumped element on the picosecond time scale of the SFQ pulse. Instead, the structure responds as a two-dimensional resonator [139]. The internal resonances of the structure can have a significant effect on performance, even though they are at frequencies much higher than the center frequency of the modulator. As shown later in this chapter, resonant modes at frequencies above half the sampling rate appear in the digital output code of the modulator as "aliased" modes (with frequencies between 0 and $f_s/2$). Resonant modes which are aliased to frequencies near the modulator center frequency interfere with the desired noise shaping, increasing the in-band noise. A key design principle for a bandpass ΔΣ modulator which includes a distributed resonator is that *all higher-order resonant modes with a significant Q be chosen so that they are not aliased into the band of interest.*

As discussed later, this design requirement can be met in the case of a one-dimensional resonator such as a transmission line, whose resonances are relatively few in number and widely spaced in frequency. Meeting this design requirement is more difficult when a two-dimensional resonator is employed. Over a given frequency range, a two-dimensional res-

onator has a larger number of resonances at a more closely spaced set of frequencies, and even a small variation in process parameters can shift one of the aliased modes into the band of interest. In current Josephson technology, any resonator in the 1-3 GHz range is physically large enough that its distributed nature must be considered. Therefore, the real choice in designing a superconducting bandpass $\Delta\Sigma$ modulator is not lumped element or distributed resonator, but the *type* of distributed resonator. Because it presents fewer problems with aliased modes, a transmission line resonator was chosen for this project.

If a capacitor with high specific capacitance were added to a Josephson circuit process, the dimensions of capacitor C could be reduced to the point where the capacitor behaves as a lumped element at all frequencies of interest. The most straightforward process modification would be to add a structure with a thinner dielectric layer between superconducting metal layers; a large increase in specific capacitance could be achieved before leakage due to tunneling becomes a problem [140]. If such capacitor technology were added to a Josephson circuit process, a lumped element resonator would become realizable, and the decision to use a lumped element or distributed resonator for the superconducting modulator should be reevaluated on grounds of performance rather than feasibility.

7.2 Modulator Based on Transmission Line Resonator

As just explained, a transmission line resonator is currently the most practical type for the superconducting bandpass $\Delta\Sigma$ modulator. Proper scaling of signal levels requires that the characteristic impedance Z_0 of the transmission line be comparable to that of a Josephson junction, on the order of 1 Ω. Consequently, the transmission line should be a low-impedance microstrip structure [141] rather than a higher-impedance coplanar structure [142, 143]. Microstrip lines are used extensively in superconducting electronics [31, 128, 144] and have been thoroughly studied and characterized [109, 70, 71, 145, 146]. The optoelectronic sampling experiments of Chapter 4 showed that such lines have low loss at frequencies up to the gap frequency of Nb (0.7 THz). Others have demonstrated that the Q of a superconducting microstrip resonator in the low GHz range can exceed 10^4 if the insulating dielectric has low loss, and the superconducting layers are free from impurities and surface defects [27]. A resonator with such a high value of Q is essentially ideal, in that the noise shaping of the bandpass modulator is then limited by imperfections in circuit components other than the resonator.

A superconducting bandpass $\Delta\Sigma$ modulator based on a transmission line resonator can be derived from a lumped element modulator by replacing the LC network with a transmission line. As an example, the modulator derived from the circuit of Figure 7-10 is illustrated in Figure 7-11. The analog signal source is capacitively coupled to one end of the superconducting microstrip line, and the current flowing out of the other end is quantized by the SFQ comparator. The microstrip line is fully specified as an idealized transmission line by its characteristic impedance Z_0 and its propagation delay T_d [147]. As in the case of the lumped element modulator, capacitive coupling of the input permits a better tradeoff between loaded Q and input sensitivity than does resistive coupling. A high loaded Q ($Q_{ld} > 1000$) is maintained by keeping capacitor C_c small. Since each SFQ pulse generated across J_2 injects current back into the microstrip line, resonator feedback is once again realized as kickback from the SFQ comparator.

The physical interpretation of the noise suppression process is particularly helpful in

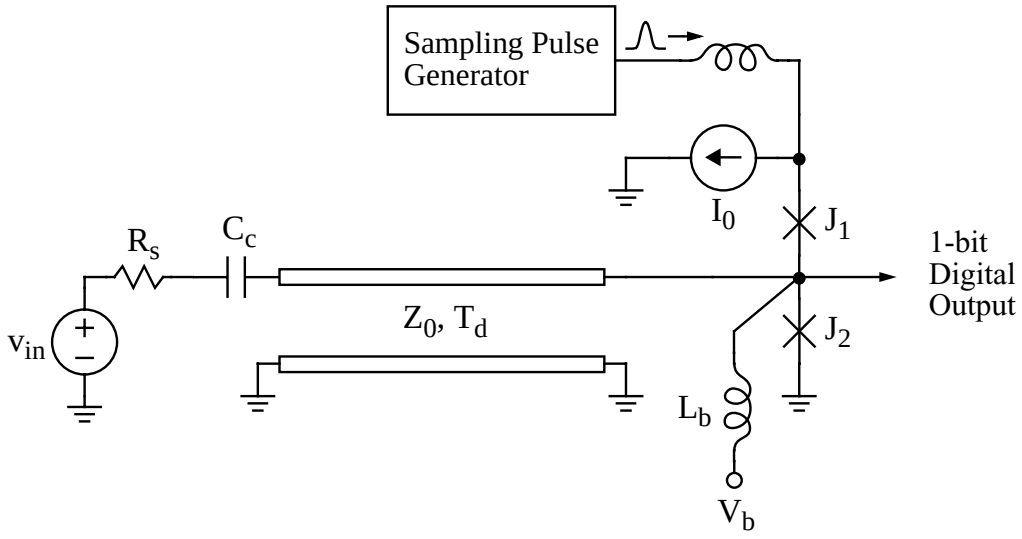


Figure 7-11: Superconducting bandpass $\Delta\Sigma$ modulator based on transmission line.

understanding the noise shaping of superconducting modulators employing transmission line resonators. As argued earlier, both quantization and thermal noise are suppressed at frequencies at which junction J_2 is shunted with a very low impedance. One such frequency ($\omega_0 = \pi/2T_d$) corresponds to the quarter-wave resonance of the microstrip line. Since the impedance of the small capacitor C_c is much higher than Z_0, the left end of the microstrip line in Figure 7-11 is effectively terminated in an open circuit, which at quarter-wave resonance is reflected as a short circuit shunting J_2. A large suppression of in-band noise can be achieved by selecting the transmission line length so that this resonant frequency equals the desired center frequency of the modulator.

While quarter-wave resonance is responsible for suppression of in-band noise near the modulator center frequency, quantization noise is also minimized at other frequencies, corresponding to higher-order modes on the microstrip line. The locations of these other minima follow directly from the impedance of an open-circuited transmission line, given by [147]

$$Z_{oc}(j\omega) \approx -jZ_0 \cot \omega T_d. \tag{7.34}$$

Since the cotangent function equals zero at all odd multiples of $\pi/2$, junction J_2 is shunted with a low impedance (and quantization noise is suppressed) at odd multiples of ω_0. In practice, not all of these higher-order modes play a significant role in quantization noise shaping, as modes at very high frequencies (e.g., 100 GHz) have low values of loaded Q. Loaded Q drops with increasing frequency for two reasons. First, the impedance of capacitor C_c decreases, and the microstrip line becomes more tightly coupled to source resistance R_s, a dissipative element. Second, the inherent losses of the superconductors increase, so the unloaded Q is reduced as well [27]. Nonetheless, several higher-order modes do have significant values of loaded Q, and the quantization noise spectrum exhibits several distinct minima. There is also a minimum at $\omega = 0$ since inductor L_b shunts junction J_2 with a very low impedance near dc. (This minimum at dc is common to all modulators in which the SFQ comparator is biased with a voltage source [66].)

The large number of modes at many different frequencies distinguishes such a modula-

tor from those with a single resonant frequency, such as the lumped element modulators described earlier. High-order bandpass $\Delta\Sigma$ modulators have been implemented in semiconductor technology [23], but in such designs all the poles of the loop filter are located at nearly identical frequencies, not spread across the entire output spectrum of the modulator. The large number of modes at widely spaced frequencies not only complicates the appearance of the output spectrum but also raises important theoretical questions, especially regarding modulator stability. A rigorous theory for the stability of $\Delta\Sigma$ modulators with orders greater than 3 does not exist. High-order modulators are typically designed with empirical methods using rules-of-thumb derived from the experience of past designs. Such rules-of-thumb provide little guidance here, as they are not accurate for modulators with unusual loop filters [52]. A loop filter based on a transmission line, with strong resonances at widely spaced frequencies, definitely qualifies as "unusual". Fortunately, simulations such as those presented in the next chapter show that the circuit of Figure 7-11 is inherently very stable. However, the lack of a theoretical model for stability complicates efforts to improve and optimize the modulator, as proposed changes may compromise modulator stability in unexpected ways, reducing overall performance. Such design complications are hardly surprising. While bandpass $\Delta\Sigma$ modulators with transmission line resonators have been contemplated in the past [148], they have not been implemented until now. One of the achievements of this thesis project has been to demonstrate that such modulators can achieve high performance, even though a comprehensive design methodology is still lacking.

The output spectrum of a modulator with a transmission line resonator is further complicated by "aliased" modes – a phenomenon not observed in previous $\Delta\Sigma$ modulators. Typically, there are some higher-order resonant modes with significant values of loaded Q at frequencies above half the sampling rate. As shown later in the chapter, such modes affect the quantization noise shaping at aliased frequencies (between 0 and $f_s/2$). In most cases, aliased modes do not affect modulator performance but simply add additional minima to the quantization noise spectrum. However, if a higher-order mode is aliased to a frequency near quarter-wave resonance, it can interfere with the desired noise shaping, increasing noise at the center frequency of the modulator. Design techniques for avoiding such problems with aliased modes are discussed later in the chapter.

The large number of resonant modes complicates the design and analysis of the modulator, but such a high-order system may have some operational advantages over the lumped element modulators discussed earlier. Most analyses of $\Delta\Sigma$ modulator operation assume that the quantization error of the comparator is uncorrelated with the input signal, but this approximation is often inaccurate with low-order modulators [53]. In this thesis project, lumped element modulators have not been simulated and characterized as extensively as those with transmission lines. Nonetheless, preliminary investigations suggest that modulators based on a single LC resonator sometimes generate significant tones at frequencies harmonically related to the input frequency, indicating undesirable correlation between the quantization error and the input. Under similar input conditions, the output spectrum of a modulator based on a transmission line is free from tonal problems and more like random noise. While further study is needed before making a definitive conclusion, it appears that the high order of a modulator employing a transmission line helps to decorrelate the quantization error. Presumably, similar benefits could be obtained with modulators based on more complex LC networks, such as lumped element transmission lines [149].

Directly connecting the microstrip line to the SFQ comparator as indicated in Fig-

ure 7-11 has one major drawback. Unlike the LC resonator, the microstrip line shunts J_2 with a low impedance on the time scale over which the Josephson junction switches. Since the SFQ pulse duration is much shorter than propagation delay T_d, the microstrip line acts as a simple resistive shunt equal to Z_0 while junction J_2 is generating an SFQ pulse. As stated earlier, Z_0 is a small value, on the order of 1 Ω. Since the speed of an SFQ circuit is proportional to the I_cR product [31], such heavy shunting of J_2 undesirably increases the switching time of the SFQ comparator.

Such degradation of comparator performance can be avoided by placing a small inductor L_r between the microstrip transmission line and the SFQ comparator, as demonstrated in Figure 7-12. At very high frequencies, inductor L_r has a high enough impedance that it effectively isolates the SFQ comparator from the low impedance microstrip line while junction J_2 is switching and generating an SFQ pulse. Because of this isolation, the fast switching time of the comparator is preserved. At lower frequencies, the main effect of L_r is to alter the resonant frequencies of the circuit. Resonance now occurs at frequencies at which the reactance of the microstrip transmission line is negative and equal in magnitude to the positive reactance of inductor L_r. According to Equation 7.34, the reactance of the transmission line is negative at frequencies ω just below odd multiples of $\pi/2T_d$, so the resonant frequencies are shifted downward. As an example, if $Z_0 = 1\ \Omega$ and $T_d = 100$ ps, the addition of series inductor $L_r = 20$ pH reduces the quarter-wave resonant frequency ω_0 from 2.5 GHz to approximately 2.09 GHz. Such a shift in resonant frequency is easily compensated by changing resonator parameters.

The superconducting bandpass ΔΣ modulator of Figure 7-12 is the circuit implemented and experimentally demonstrated in this thesis project. Its operation and performance are now examined in more detail.

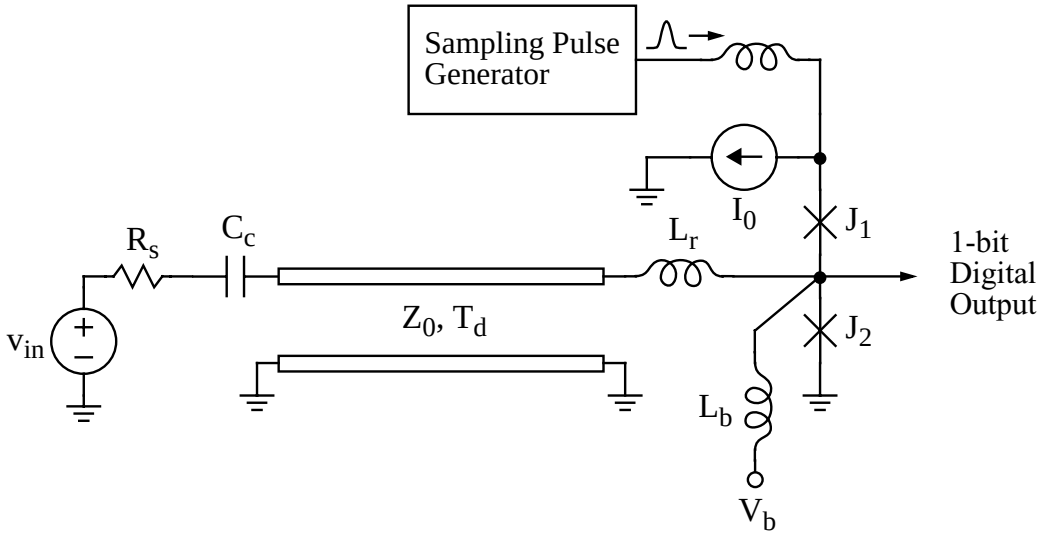


Figure 7-12: Superconducting modulator with inductor L_r between microstrip transmission line and SFQ comparator.

7.2.1 Input Sensitivity and Loaded Q

As in the case of the lumped element modulators, there is a tradeoff between input sensitivity and loaded Q. For large values of coupling capacitor C_c, the resonator is strongly coupled to the input source, the input sensitivity is high, and loaded Q is relatively low. For small values of C_c (such that $\omega_0 R_s C_c \ll 1$), the resonator is more weakly coupled to the source, the input sensitivity is lower, and loaded Q is higher. As now demonstrated, there is a simple quantitative relationship between input sensitivity and loaded Q.

An exact expression for the signal transfer function (STF) of a modulator employing a transmission line resonator cannot be analytically derived. As discussed in previous sections, the input sensitivity of a modulator can be estimated by calculating the Thévenin equivalent voltage of the input network (at the port connected to the SFQ comparator). Calculation of the Thévenin equivalent voltage requires solving the wave equations of the transmission line, subject to appropriate boundary conditions. Details of the analysis are reserved for Appendix B, where it is shown that the Thévenin equivalent voltage at resonant frequency[5] ω_0 approximately equals

$$V_{th}(j\omega_0) \approx \frac{\omega_0 Z_0 C_c}{\sin(\omega_0 T_d)(1 + j\omega_0 R_s C_c)} V_{in}(j\omega_0). \tag{7.35}$$

Since the modulator produces a full-scale output when the Thévenin equivalent voltage has an amplitude equal to $\Phi_0/2T$, it follows that

$$v_{in,fs} \approx \frac{\sin(\omega_0 T_d)\sqrt{1 + \omega_0^2 R_s^2 C_c^2}}{\omega_0 Z_0 C_c} \cdot \frac{\Phi_0}{2T}. \tag{7.36}$$

The loaded Q of the resonator is obtained by applying the general definition of Q given in Equation 7.24. The details of calculating the total stored energy and average power dissipation at resonance are presented in Appendix B. There it is shown that the loaded Q approximately equals

$$Q_{ld} \approx \frac{(\omega_0 T_d + \sin\omega_0 T_d \cos\omega_0 T_d)(1 + \omega_0^2 R_s^2 C_c^2)}{2\omega_0^2 R_s Z_0 C_c^2}. \tag{7.37}$$

For values of C_c small enough that $\omega_0 R_s C_c \ll 1$, the loaded Q is inversely proportional to C_c^2, as in the case of a capacitively coupled lumped element resonator (cf. Equation 7.27). For values of C_c large enough that $\omega_0 R_s C_c \gg 1$, the coupling capacitor is effectively a short, and Q_{ld} approaches Q_{ld0}, the loaded Q obtained by connecting the signal source directly to the resonator:

$$Q_{ld0} \approx \frac{R_s(\omega_0 T_d + \sin\omega_0 T_d \cos\omega_0 T_d)}{2Z_0}. \tag{7.38}$$

From Equations 7.37 and 7.38,

$$\sqrt{Q_{ld} Q_{ld0}} \approx \frac{(\omega_0 T_d + \sin\omega_0 T_d \cos\omega_0 T_d)\sqrt{1 + \omega_0^2 R_s^2 C_c^2}}{2\omega_0 Z_0 C_c}, \tag{7.39}$$

[5]Frequency ω_0 is defined here to be the quarter-wave resonant frequency of the circuit *after* addition of inductor L_r. Therefore, $\omega_0 < \pi/2T_d$.

so Equation 7.36 can be rewritten as

$$v_{in,fs} \approx \mathrm{F}(\omega_0 T_d) \frac{\sqrt{Q_{ld} Q_{ld0}} \Phi_0}{2T}, \tag{7.40}$$

where

$$\mathrm{F}(\omega_0 T_d) = \frac{2 \sin \omega_0 T_d}{\omega_0 T_d + \sin \omega_0 T_d \cos \omega_0 T_d}. \tag{7.41}$$

Prefactor $\mathrm{F}(\omega_0 T_d)$ is independent of loaded Q and has a value between 1 and $4/\pi$ for any choice of circuit parameters. Except for this prefactor close to unity, the relationship between input sensitivity and loaded Q is identical to that of a capacitively coupled lumped element resonator (cf. Equation 7.33). Since increases in loaded Q only reduce the input sensitivity with a square root dependence, sensitivity is fairly high even with very large values of loaded Q. As an example, if $Z_0 = 1\ \Omega$, $T_d = 100$ ps, $L_r = 20$ pH, $R_s = 50\ \Omega$, $C_c = 0.1$ pF, and $f_s = 20$ GHz, the loaded Q at quarter-wave resonance (2.09 GHz) exceeds 9000, and $v_{in,fs}$ equals 15.3 mV.

In practice, transmission line losses which limit the unloaded Q of the microstrip resonator may dominate the coupling losses considered in this section. Even with such losses, though, the loaded Q of the resonator is likely to be high enough not to degrade the noise shaping of the modulator. Such transmission line losses have a negligible effect on the input sensitivity.

7.2.2 NTF

The noise transfer function (NTF) for the lumped element modulator of Figure 7-1 was calculated in Section 7.1.1 by deriving the difference equations of an equivalent discrete-time system and applying z-transforms. Such an approach is not practical for studying the modulator of Figure 7-12. A continuous-time system with a large number of resonant modes would require an equivalent discrete-time system with many state variables. Furthermore, the continuous-time impulse response of the resonator has no closed-form solution, so one cannot write equations analogous to Equations 7.5. Therefore, a different approach to calculating the NTF must be used here.

The method, which is based on calculating the frequency-dependent loop gain of the feedback model, is applicable to any continuous-time $\Delta\Sigma$ modulator. The main disadvantage of the method is that it is not suitable for calculating the STF since prefiltering of the input signal prior to sampling (an important feature of continuous-time $\Delta\Sigma$ modulators [132, 150]) is not accounted for. Circuit simulations presented in the next chapter show that the STF is quite flat over a broad band of frequencies spanning quarter-wave resonance, so the lack of an analytical expression for the STF is not a major concern. In designing the circuit, one only needs to consider the input sensitivity at the resonant frequency, given by Equation 7.36. In contrast, a thorough understanding of the NTF is crucial for proper design of the modulator.

In general, the NTF of a $\Delta\Sigma$ modulator with loop filter $H(z)$ equals

$$\mathrm{NTF}(z) = \frac{1}{1 + KH(z)}. \tag{7.42}$$

K is the effective gain of the comparator, shown by Ardalan and Paulos [51] to depend on

the joint statistics of the comparator input $u[n]$ and output $y[n]$:

$$K = \frac{E\{u[n]y[n]\}}{E\{u^2[n]\}}. \tag{7.43}$$

For the superconducting modulators considered here, $u[n]$ is the comparator input current i_q at sampling times $t = nT$,

$$u[n] = i_q[n] = i_q(nT), \tag{7.44}$$

and $y[n] = \mathrm{sgn}(u[n])$.

The loop filter $H(z)$ and comparator gain K are now estimated for the generalized model of a superconducting $\Delta\Sigma$ modulator presented in Figure 7-13. As in the earlier analysis of a superconducting modulator based on a lumped element LC resonator, the SFQ comparator is modeled as a voltage source equal to $v_{q2}(t)$, the bipolar feedback signal depicted in Figure 7-2. Voltage source v_{th} and series impedance Z_{th} represent the Thévenin equivalent circuit for the complete input network connected to the SFQ comparator. In calculating the frequency-dependent loop gain ($KH(z)$), the input source is suppressed, so $v_{th} = 0$. For the circuit of Figure 7-12, Z_{th} equals the impedance presented to the SFQ comparator by the network comprising R_s, C_c, L_r, L_b, and the transmission line. With the appropriate selection of Z_{th}, other superconducting modulators can be represented with this model, including the lumped element LC modulators described earlier and first-order low-pass modulators [66].

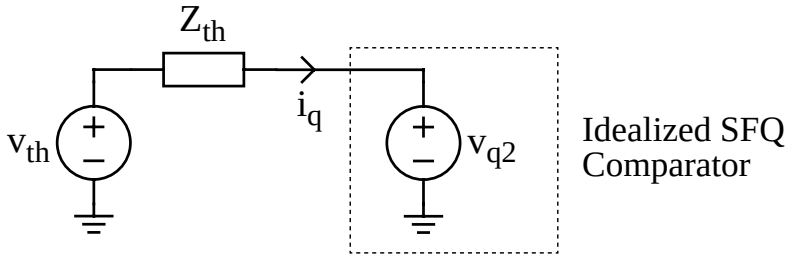


Figure 7-13: Generalized model for superconducting $\Delta\Sigma$ modulator.

$H(z)$ is the z-domain transfer function from the comparator output back to its input (with the signal inversion indicated in the block diagram of Figure 2-3). Letting $z = e^{j\omega T}$,

$$H(z) = H(e^{j\omega T}) = \sum_{n=-\infty}^{\infty} h[n]e^{-j\omega nT}, \tag{7.45}$$

where $-h[n]$ is the sequence of input currents $i_q[n]$ sampled by the comparator in response to a single binary 1 on output $y[n]$. Let $-h_c(t)$ be the continuous-time current $i_q(t)$ generated by a single positive pulse in feedback signal $v_{q2}(t)$. Since $h[n] = h_c(nT)$, $H(e^{j\omega T})$ is related to Fourier transform $H_c(j\omega)$ by basic sampling theory [1]:

$$H(e^{j\omega T}) = \frac{1}{T}\sum_{k=-\infty}^{\infty} H_c\left(j\omega - j\frac{2\pi k}{T}\right). \tag{7.46}$$

If $P(j\omega)$ is the Fourier transform of a single positive pulse in $v_{q2}(t)$, then $H_c(j\omega) =$

$Y_{th}(j\omega)P(j\omega)$, where the admittance $Y_{th}(j\omega) = 1/Z_{th}(j\omega)$. Therefore,

$$H(e^{j\omega T}) = \frac{1}{T}\sum_{k=-\infty}^{\infty} Y_{th}\left(j\omega - j\frac{2\pi k}{T}\right) P\left(j\omega - j\frac{2\pi k}{T}\right). \tag{7.47}$$

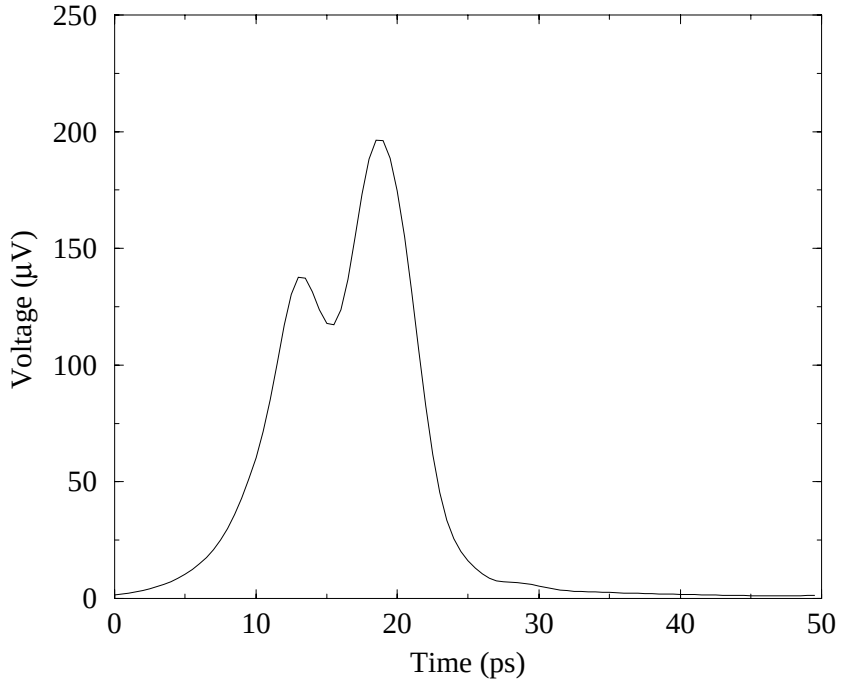
In the analysis of a lumped element LC resonator presented in Section 7.1.1, each positive pulse in $v_{q2}(t)$ was modeled as an impulse with zero width and an area equal to $\Phi_0/2$. In the frequency domain, this corresponds to letting $P(j\omega) = \Phi_0/2$ for all frequencies ω. While such a simple model for SFQ pulse generation could be used here, more accurate estimates of the frequency-dependent loop gain and the NTF are obtained if $P(j\omega)$ characterizes the spectral content of a real SFQ pulse, one having nonzero width. The best approach to obtaining an estimate for $P(j\omega)$ is to simulate the modulator of Figure 7-12 with a circuit simulator such as JSIM [122]. Figure 7-14(a) shows a typical SFQ voltage pulse produced by the comparator during operation of the superconducting modulator. In the JSIM simulation, the device parameters corresponded to niobium junctions with 1 kA/cm^2 critical current density. Because the input overdrive of the comparator is typically[6] smaller than the current levels used in RSFQ digital circuits, the comparator switches relatively slowly, and the SFQ output pulse is about twice as wide as the SFQ pulses generated by RSFQ logic gates. The Fourier transform of the simulated SFQ pulse is plotted in Figure 7-14(b). In the plot, the magnitude is normalized to its value at dc ($\omega = 0$). Since each positive pulse in $v_{q2}(t)$ has an area equal to $\Phi_0/2$,

$$P(j\omega)\,|_{\omega=0} = \Phi_0/2. \tag{7.48}$$

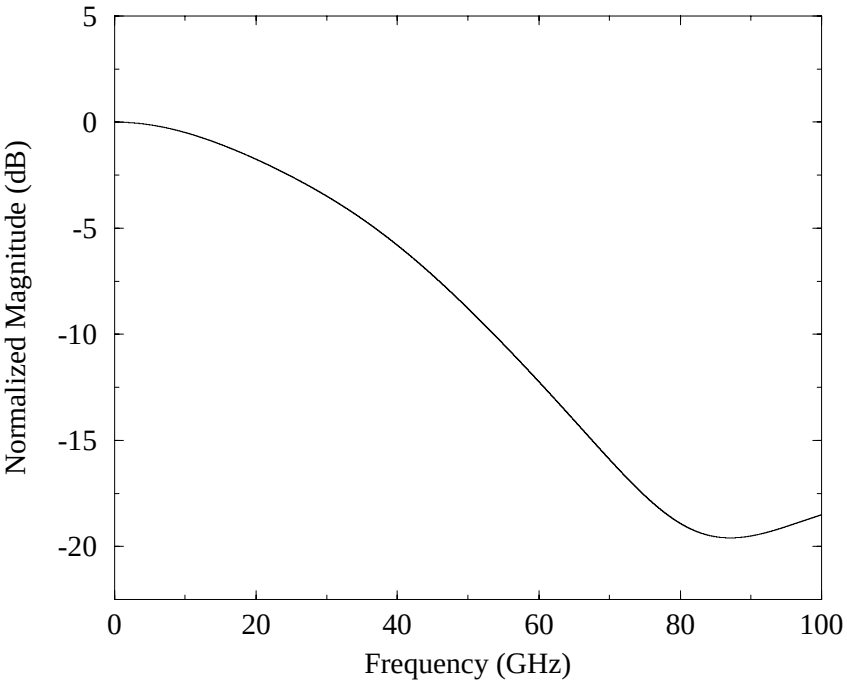
As illustrated in Figure 7-14(b), the magnitude of $P(j\omega)$ is within 3 dB of its low frequency value up to almost 30 GHz. Because each SFQ pulse contains significant spectral energy up to tens of GHz, many higher-order modes of the transmission line are excited during modulator operation. Some of these modes are responsible for the phenomenon of aliased modes, discussed below. In the analysis of Section 7.1.1, the propagation delay of the comparator was neglected. In the analysis presented here, a comparator delay τ can be incorporated into the model by adding a linear phase term $e^{-j\omega\tau}$ to $P(j\omega)$.

Equation 7.47 shows that loop filter $H(e^{j\omega T})$ equals a superposition of repeated copies of $Y_{th}(j\omega)P(j\omega)$, shifted in frequency by integer multiples of the sampling rate. If one assumes that $Y_{th}(j\omega)P(j\omega) \approx 0$ for $\omega \geq \pi/T$, these repeated copies do not overlap, and $H(e^{j\omega T})$ is

[6] In a $\Delta\Sigma$ modulator, the input to the comparator consists of random idling noise superimposed on a filtered version of the modulator input. The input overdrive of the comparator varies from clock cycle to clock cycle. In some clock cycles, the input overdrive is relatively high (almost as large as the switching current in a logic gate), and the width of the SFQ pulse generated by the comparator is shorter than that shown in Figure 7-14(a). In other clock cycles, the comparator input current is just slightly above threshold, and the width of the SFQ output pulse is longer than that shown in Figure 7-14(a). In most clock cycles, the input overdrive has a level between these limiting cases, and the SFQ output pulse is more similar to that shown in the figure.



(a)



(b)

Figure 7-14: (a) Typical SFQ voltage pulse produced by comparator during modulator operation, and (b) its Fourier transform (normalized to dc value).

proportional to $Y_{th}(j\omega)P(j\omega)$ without aliasing[7]:

$$H(e^{j\omega T}) \approx \tfrac{1}{T} Y_{th}(j\omega)P(j\omega) \quad \text{for } |\omega| \leq \pi/T. \tag{7.49}$$

This equation is consistent with the physical interpretation of the noise shaping process mentioned earlier in the chapter. At frequencies at which the lower junction of the SFQ comparator is shunted with a very low impedance, $Y_{th}(j\omega)$ and $H(e^{j\omega T})$ are very large, and the NTF given by Equation 7.42 is very small. While the assumption that $Y_{th}(j\omega)P(j\omega) \approx 0$ for $\omega \geq \pi/T$ is a reasonable approximation for the lumped element LC modulators considered earlier, it is a poor approximation for the circuit of Figure 7-12. Because of higher-order modes on the transmission line, there are a large number of frequencies at which $Y_{th}(j\omega)$ is maximized. Typically, some of these frequencies exceed half the sampling rate, invalidating the assumption behind Equation 7.49. According to Equation 7.47, higher-order modes at frequencies above half the sampling rate affect the quantization noise shaping at aliased frequencies (between 0 and half the sampling rate). As an example, if $Y_{th}(j\omega)$ has a local maximum due to a higher-order resonance at 17 GHz, and the sampling rate is 20 GHz, $H(e^{j\omega T})$ has a local maximum at 20-17=3 GHz, and quantization noise at 3 GHz is suppressed according to Equation 7.42. As explained in the next section, such aliased modes must be considered carefully in designing the modulator.

In principle, the effective comparator gain K is given by Equation 7.43. Such a definition can be applied by acquiring the joint statistics of $u[n]$ and $y[n]$ from long simulations of the modulator, but obtaining an analytical expression for K requires a different approach, based on a number of approximations. The key concept underlying the analysis is that signal levels in a $\Delta\Sigma$ modulator automatically adjust themselves to make the *broadband* loop gain unity [151]. Of course, the loop gain is much greater than unity at frequencies at which the quantization noise is suppressed (e.g., at quarter-wave resonance), but such high loop gain is only found over narrow frequency bands. At most frequencies, the loop gain is close to unity. Therefore, in a broadband sense,

$$K\overline{H} \approx 1, \tag{7.50}$$

where $\overline{H}$ is the magnitude of $H(e^{j\omega T})$ averaged (in some manner) over frequencies between 0 and half the sampling rate. The aliasing due to higher-order resonant modes and discussed in the previous paragraph primarily affects $H(e^{j\omega T})$ over narrow frequency bands and has little effect on the broadband loop gain. Ignoring aliasing, Equation 7.49 applies, so

$$\overline{H} \approx \frac{1}{T}\overline{Y}_{th}\overline{P}, \tag{7.51}$$

where $\overline{Y}_{th}$ and $\overline{P}$ are the magnitudes of $Y_{th}(j\omega)$ and $P(j\omega)$ averaged (in some manner) over frequencies between 0 and half the sampling rate. As illustrated in Figure 7-14(b), the

[7] Aliasing in this context refers to modification of loop filter $H(e^{j\omega T})$ due to interference between successive terms in Equation 7.47, not to distortion of the input signal due to undersampling. The aliasing discussed here is similar to that encountered in designing digital filters from continuous-time prototypes by the method of impulse invariance [1]. A digital filter designed by impulse invariance does not distort the input signal with aliasing if the sampling rate exceeds the Nyquist rate, but its characteristics differ from its continuous-time prototype because of interference between terms such as those in Equation 7.47.

magnitude of $P(j\omega)$ is relatively flat up to frequencies exceeding 20 GHz, so

$$\overline{P} \approx P(j\omega) \mid_{\omega=0} = \Phi_0/2. \tag{7.52}$$

A simple estimate for $\overline{Y}_{th}$ is obtained by making a crude approximation. At most frequencies, $Z_{th}(j\omega)$ is dominated by the impedance of an open-circuited transmission line, given by Equation 7.34. Over narrow bands of frequencies (near resonance), this impedance can be very large or very small, but over most frequencies, the cotangent function in Equation 7.34 has a magnitude on the order of unity, and $Z_{th}(j\omega)$ has a magnitude on the order of Z_0. Therefore, $\overline{Y}_{th}$ can be roughly approximated as

$$\overline{Y}_{th} \approx 1/Z_0. \tag{7.53}$$

Combining Equations 7.50 through 7.53 and solving for the comparator gain K yields

$$K \approx \frac{2Z_0T}{\Phi_0}. \tag{7.54}$$

To check this result, the comparator gain K was also calculated according to Equation 7.43, using data from a long JSIM simulation of the modulator (Figure 7-12). The more rigorous calculation showed that Equation 7.54 tends to overestimate the comparator gain – by a factor of 1.6, for the circuit parameters used in the simulation ($Z_0 = 1\ \Omega$, $T_d = 100$ ps, $L_r = 20$ pH, $L_b = 100$ pH, $R_s = 62.25\ \Omega$, $C_c = 0.11$ pF, $I_{c1} = I_{c2} = 271\ \mu A$, $I_cR_n = 300\ \mu V$, and $f_s = 20$ GHz). Such an error in the estimate for K is quite reasonable, considering the roughness of the approximations made in deriving Equation 7.54.

Despite its inaccuracies, Equation 7.54 is quite helpful in understanding how the comparator gain K scales with circuit parameters. For example, if all of the impedances of the input network are halved, the loop filter transfer function $H(e^{j\omega T})$ is doubled, as the expression given in 7.47 scales proportionally with $Y_{th}(j\omega)$. Such a change has little effect on modulator performance, however. Since impedance scaling of the input network requires a proportional reduction in Z_0, the comparator gain K given by Equation 7.54 is now smaller by a factor of two, and the frequency-dependent loop gain is unchanged. Consequently, quantization noise shaping in the modulator is insensitive to simple scaling of circuit impedances. In an actual design, circuit impedances are scaled so that current levels are best matched to the characteristics of the SFQ comparator, such as its input noise level and its sensitivity to load current.

An approximate expression for the NTF of the modulator is now given. From Equations 7.47 and 7.54, it follows that the loop gain $KH(e^{j\omega T})$ is approximately

$$KH(e^{j\omega T}) \approx \frac{2Z_0}{\Phi_0} \sum_{k=-\infty}^{\infty} Y_{th}\left(j\omega - j\frac{2\pi k}{T}\right) P\left(j\omega - j\frac{2\pi k}{T}\right). \tag{7.55}$$

Let $\widetilde{P}(j\omega)$ be $P(j\omega)$ normalized to its dc value (i.e., the function plotted in Figure 7-14(b)):

$$\widetilde{P}(j\omega) \equiv \frac{P(j\omega)}{P(j0)} = \frac{2P(j\omega)}{\Phi_0}. \tag{7.56}$$

Then Equation 7.55 can be rewritten as

$$KH(e^{j\omega T}) \approx Z_0 \sum_{k=-\infty}^{\infty} Y_{th}\left(j\omega - j\frac{2\pi k}{T}\right) \widetilde{P}\left(j\omega - j\frac{2\pi k}{T}\right), \tag{7.57}$$

and the NTF given in Equation 7.42 becomes

$$\mathrm{NTF}(e^{j\omega T}) \approx \frac{1}{1 + Z_0 \sum_{k=-\infty}^{\infty} Y_{th}\left(j\omega - j\frac{2\pi k}{T}\right) \widetilde{P}\left(j\omega - j\frac{2\pi k}{T}\right)}. \tag{7.58}$$

Each term in Equation 7.57 is a frequency-shifted copy of $Z_0 Y_{th}(j\omega)\widetilde{P}(j\omega)$, whose magnitude is plotted in Figure 7-15 for the modulator of Figure 7-12; circuit parameters are listed in the figure caption. There are 20 resonant peaks between 0 and 100 GHz, corresponding to multiple modes on the transmission line. The height of each peak decreases with frequency for two reasons. As explained earlier, the loaded Q of each resonant mode drops with increasing frequency, reducing the value of $Y_{th}(j\omega)$ at resonance. The second (and less significant) factor is the smaller magnitude of $\widetilde{P}(j\omega)$ at higher frequencies (cf. Figure 7-14(b)). Above 45 GHz, the peaks are smaller than unity (0 dB) and have little effect on the frequency-dependent loop gain or the NTF.

Because $|Z_0 Y_{th}(j\omega)\widetilde{P}(j\omega)|$ is small at very high frequencies, it is only necessary to include a finite number of terms in Equation 7.57 when estimating loop gain $KH(e^{j\omega T})$ for values of ω between 0 and π/T. If the terms that represent aliasing from spectral components of $Z_0 Y_{th}(j\omega)\widetilde{P}(j\omega)$ above 90 GHz are excluded, and the sampling rate is 20 GHz, the estimated loop gain $KH(e^{j\omega T})$ is that shown in Figure 7-16(a). At least 10 resonant peaks are visible in the plot. The frequencies of the two largest peaks (2.09 and 6.41 GHz) are the only physical resonances of the tranmission line below 10 GHz. All the other peaks signify transmission line resonances above 10 GHz which have been shifted into the band between 0 and 10 GHz by the process of aliasing. Because of these aliased modes, the loop gain is large at several frequencies, and several distinct minima are visible in the NTF, shown in Figure 7-16(b).

The plots shown in Figure 7-16 were generated under the assumption of negligible comparator delay. As mentioned earlier, a comparator delay τ can be incorporated into the model by adding a linear phase term $e^{-j\omega\tau}$ to $\widetilde{P}(j\omega)$. The effect of comparator delay on the NTF is illustrated in Figure 7-17. The NTF shown by the solid line is identical to that in Figure 7-16(b); the dotted line shows the NTF with a comparator delay of 3 ps. With the comparator delay added to the model, the minima in the NTF are virtually unchanged, but the maxima are larger and somewhat sharper, exceeding 0 dB at several frequencies and 9 dB near 3.9 GHz. Such peaking in the quantization noise spectrum of the modulator is also observed in the JSIM circuit simulations presented in the next chapter. Out-of-band NTF gains above 5-6 dB often indicate poor stability in high-order $\Delta\Sigma$ modulators [52, 152], but such rules-of-thumb do not apply here. While the modulator of Figure 7-12 has many modes, the poles of the loop filter are located at widely spaced frequencies and do not act with any degree of multiplicity. Consequently, both the shaping of quantization noise near resonance and the stability are more typical of low-order $\Delta\Sigma$ modulators. As presented later, JSIM simulations show that modulator stability is excellent for typical circuit parameters.

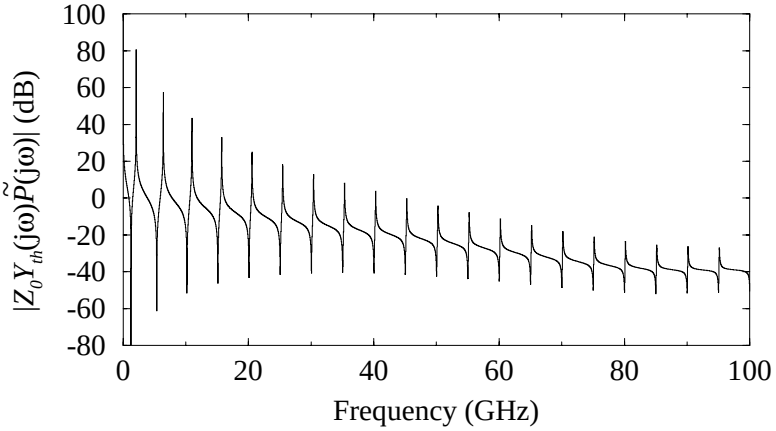
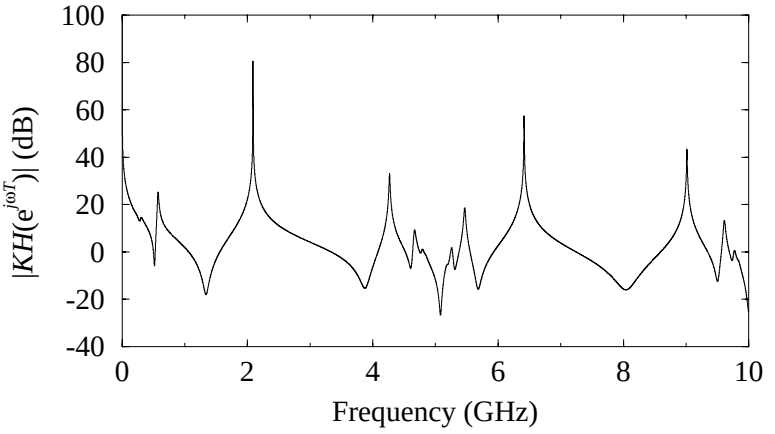
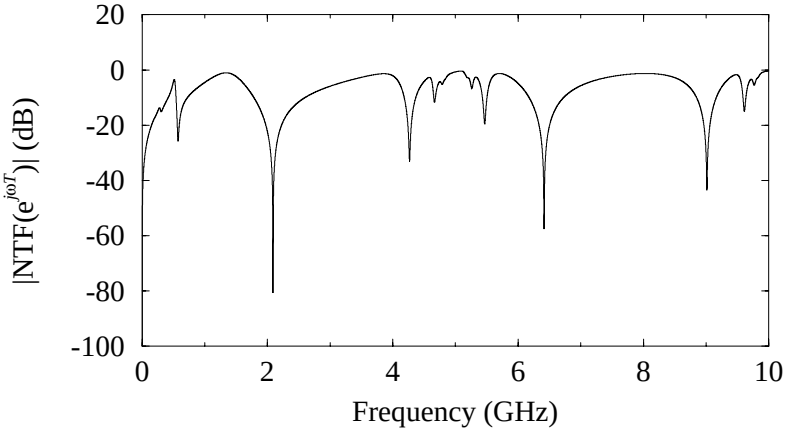


Figure 7-15: Magnitude of $Z_0 Y_{th}(j\omega)\widetilde{P}(j\omega)$ as a function of frequency. The parameters for the circuit of Figure 7-12 are: $Z_0 = 1\ \Omega$, $T_d = 100$ ps, $L_r = 20$ pH, $L_b = 100$ pH, $R_s = 50\ \Omega$, and $C_c = 0.1$ pF.



(a)



(b)

Figure 7-16: (a) Frequency-dependent loop gain $KH(e^{j\omega T})$ and (b) NTF for circuit of Figure 7-12. The circuit parameters equal those in the caption above, and $f_s = 20$ GHz.

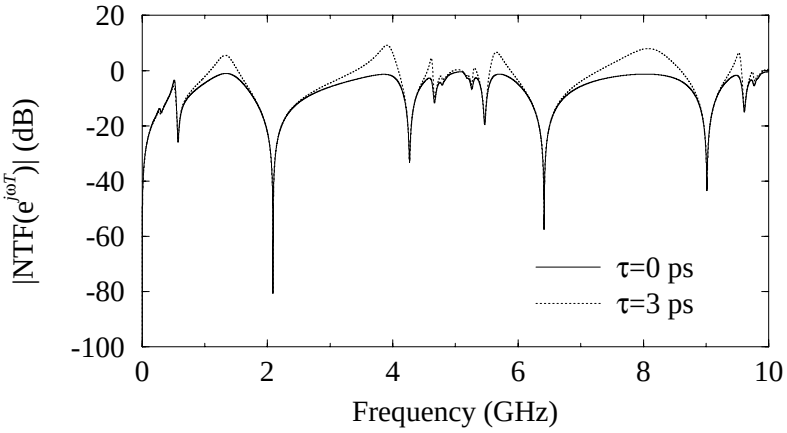


Figure 7-17: Effect of comparator delay on NTF.

7.2.3 Management of Aliased Modes

For the circuit parameters used in generating Figures 7-15 through 7-17, no higher-order mode is aliased to a frequency near quarter-wave resonance (2.09 GHz), and the NTF has a strong minimum at that frequency. For other circuit parameters, a higher-order mode may alias to a frequency close to quarter-wave resonance and interfere with the desired noise shaping. Mathematically, one of the aliasing terms (with $k \neq 0$) in Equation 7.57 may have a magnitude comparable to that of the $k = 0$ term for some frequency ω near quarter-wave resonance. If the terms add out-of-phase, substantial cancellation of the loop gain $KH(e^{j\omega T})$ can occur, and the quantization noise near the center frequency of the modulator increases. Conservative design dictates that the potential for such cancellation not be ignored, as the phase relationship between the terms is highly unpredictable. Since the phase of $Y_{th}(j\omega)$ changes rapidly near resonance, even small variations in circuit parameters can have a dramatic effect on the phase relationship. Moreover, the comparator delay, which adds substantial phase shift to the aliased terms, is not really a constant but varies from clock cycle to clock cycle (depending on the input overdrive level).

In order to avoid such problems, the modulator should be designed so that no higher-order mode with a significant Q aliases to a frequency near quarter-wave resonance, even after expected parameter variations. Limiting the Q of resonances near and above the sampling rate improves the robustness of the circuit. Consider again the loop gain $KH(e^{j\omega T})$ plotted in Figure 7-16(a), which assumes a sampling rate of 20 GHz. The aliased mode closest to quarter-wave resonance is the resonant peak at 0.57 GHz, due to a transmission line resonance at 20.57 GHz. If the frequency of this transmission line resonance is increased by 7%, to about 22.0 GHz, the aliased mode moves from 0.57 GHz to 2.0 GHz and begins to interfere with the noise shaping at the center frequency of the modulator. The significance of such interference depends on the relative size of the aliasing term in Equation 7.57. Assume, for instance, an oversampling ratio of 256, so that the signal bandwidth is 39 MHz. The minimum value of the loop gain $KH(e^{j\omega T})$ over a 39 MHz bandwidth centered at 2.09 GHz is 36 dB. Since the peak of the aliased mode is only 25 dB, a factor of 3.5 (11 dB) smaller, interference from this aliased mode is weak and has little impact on the in-band noise of the modulator. On the other hand, if the loaded Q of the higher-order transmission line

mode were increased (e.g., by reducing the coupling capacitance C_c), the aliased mode would have a larger peak, and interference effects could be significant. In Figure 7-16(a), the aliased modes at 4.27 and 9.01 GHz (due to transmission line resonances at 15.73 and 10.99 GHz, respectively) have larger peaks than the one at 0.57 GHz. Fortunately, these aliased modes are far enough from quarter-wave resonance not to cause interference, even after being shifted in frequency by parameter variations of a typical Josephson circuit process [123]. Finally, the advantage of a very high sampling rate in minimizing problems with aliased modes should be pointed out. If the sampling rate were increased to 40 GHz, there would be virtually no aliased modes near quarter-wave resonance, as the magnitude of $Z_0 Y_{th}(j\omega)\widetilde{P}(j\omega)$ (Figure 7-15) does not have large peak values for frequencies near and above 40 GHz. In summary, interference from aliased modes can be avoided through careful selection of resonant frequencies, limiting the loaded Q values of higher-order modes with the appropriate input coupling network, and employing a very high sampling rate (e.g., 20-40 GHz).

7.2.4 Practical Considerations for Input Coupling Network

Previous sections showed the transmission line resonator of the modulator connected to the microwave input source with a single small capacitor C_c. A small capacitor, however, does not provide good impedance matching with the transmission line (e.g., coaxial cable) used to deliver the analog input to the superconducting chip. In microwave systems, a good impedance match is often necessary to ensure accurate and reliable results [153]. The impedance matching can be greatly improved by adding a termination resistor R_t to the input coupling network, as shown in Figure 7-18. Since C_c is a small capacitor, its impedance at signal frequencies is much greater than $Z_{0,s}$, the characteristic impedance of the input transmission line, and good matching is obtained if $R_t = Z_{0,s}$ (usually, 50 Ω).

The addition of termination resistor R_t reduces the Thévenin equivalent resistance connected to capacitor C_c by a factor of two. As explained in the last section, interference from aliased modes can be minimized by limiting the loaded Q values of higher-order transmission line resonances. A reduction of the Thévenin equivalent resistance connected to C_c is not consistent with this goal. Assuming a small value of C_c, such a reduction increases the loaded Q (Equation 7.37) and exacerbates problems with aliased modes. Therefore,

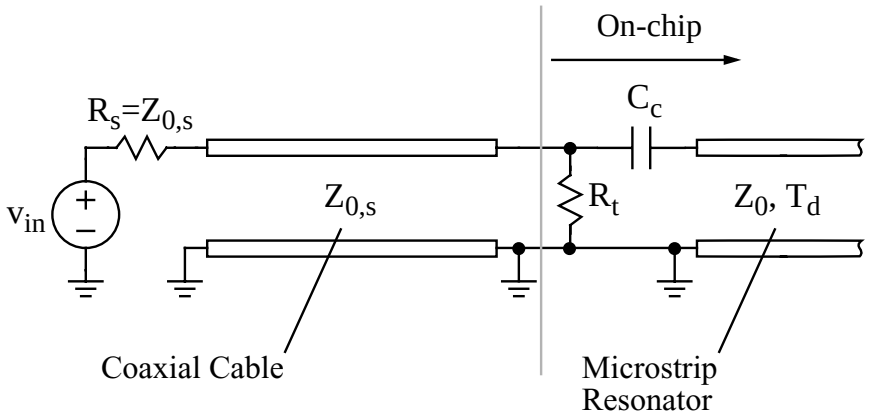


Figure 7-18: Input coupling network with termination resistor R_t.

the increase in loaded Q due to reduction of the Thévenin equivalent resistance should be compensated.

The simplest method of compensation is to increase the coupling capacitance C_c. This lowers the loaded Q but also increases the sensitivity of the modulator (Equation 7.36). An increase in sensitivity is desirable in an actual software radio receiver since it reduces the need for RF amplification in front of the superconducting modulator. For the purposes of a first laboratory demonstration, though, high sensitivity was deemed a drawback, as the SNR of the modulator might be degraded by noise from various room-temperature instruments. Therefore, a different method of compensation was chosen for the experimental modulator implemented in this thesis project.

The input coupling network of the experimental modulator is shown in Figure 7-19. The additional resistors provide more degrees of freedom in designing the network, making it possible to meet three separate requirements. Its input resistance, $R_1 \parallel (R_2 + R_3)$, equals 50 Ω, ensuring a good impedance match with the coaxial cable carrying the input signal. The network reduces the sensitivity of the test chip by 6 dB, as R_2 and R_3 form a 2:1 voltage divider. With the 50 Ω source in the circuit, the Thévenin equivalent resistance connected to capacitor C_c is 62.25 Ω, a resistance high enough to limit the loaded Q values of the resonator. In fact, the loaded Q values are slightly lower than those considered in the previous section.

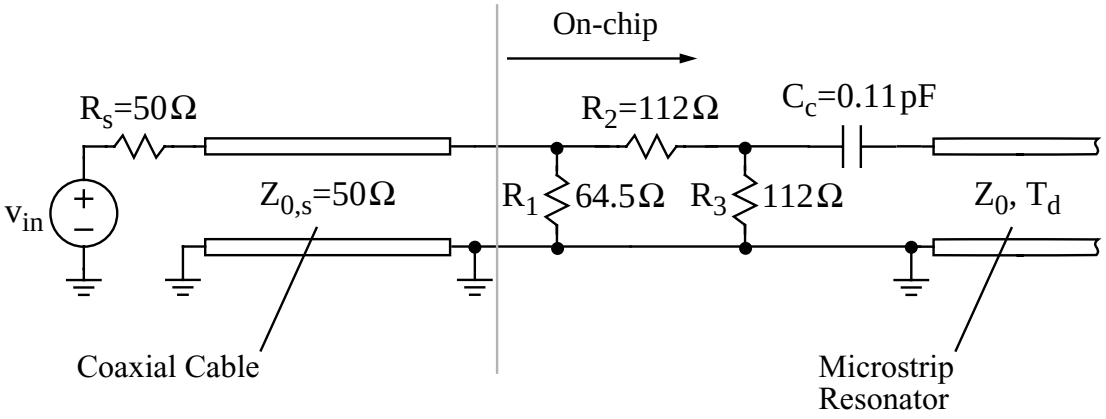


Figure 7-19: Input coupling network used for experimental modulator.

7.2.5 ADC Performance Predicted by Linearized Model

In the linearized model described in Section 2.1.2, the quantizer is modeled as a source of additive independent white noise $e[n]$, whose variance is [55]

$$\sigma_e^2 = E\{e^2[n]\} = \frac{\Delta^2}{12}, \tag{7.59}$$

where Δ is the level spacing of the quantizer. For a single-bit quantizer with ± 1 output levels, $\Delta = 2$. Since the noise power of $e[n]$ is evenly distributed across frequencies ω between $-\pi/T$ and π/T, the integrated noise power of the modulator output in a bandwidth $\Delta\omega$

centered at resonant frequency ω_0 equals

$$\begin{aligned} n^2 &= \frac{\sigma_e^2 T}{2\pi}\left(\int_{-\omega_0-\Delta\omega/2}^{-\omega_0+\Delta\omega/2} |\mathrm{NTF}(e^{j\omega T})|^2 d\omega + \int_{\omega_0-\Delta\omega/2}^{\omega_0+\Delta\omega/2} |\mathrm{NTF}(e^{j\omega T})|^2 d\omega\right) \\ &= \frac{\sigma_e^2 T}{\pi}\int_{\omega_0-\Delta\omega/2}^{\omega_0+\Delta\omega/2} |\mathrm{NTF}(e^{j\omega T})|^2 d\omega. \end{aligned} \tag{7.60}$$

After substitution of the NTF given by Equation 7.58, the total in-band noise power can be determined by numerical integration of this equation.

The result of such a calculation is now presented for the experimental modulator implemented in this thesis project (Figure 7-12). The nominal circuit parameters are: $Z_0 = 1\ \Omega$, $T_d = 100$ ps, $L_r = 20$ pH, $L_b = 100$ pH, $R_s = 62.25\ \Omega$, and $C_c = 0.11$ pF. The last two parameters are chosen so that resistor R_s and capacitor C_c form a Thévenin equivalent circuit for the real input coupling network (Figure 7-19). The critical currents of the Josephson junctions are irrelevant, as the current sensitivity of the SFQ comparator is ignored here. The comparator is modeled as ideal, except for a 3 ps delay which contributes a linear phase term to $\widetilde{P}(j\omega)$. Table 7.1 shows the in-band noise for three different signal bandwidths (centered at quarter-wave resonance) and two different sampling rates. The noise levels are expressed in dB, relative to the power of a full-scale (FS) sinusoidal output (with peak values equal to ± 1). For a given sampling rate, a one-octave decrease in signal bandwidth (doubling the oversampling ratio) reduces the in-band noise by 9 dB, the ideal value for a bandpass $\Delta\Sigma$ modulator employing a single resonator. The high loaded Q (> 6000) at quarter-wave resonance ensures almost ideal shaping of the quantization noise. For a given bandwidth, though, a one-octave increase in sampling rate (also doubling the oversampling ratio) reduces the in-band noise by only 3 dB, not the expected value of 9 dB. According to Equation 7.54, the effective comparator gain K is proportional to the sampling clock period T. The reduction in effective comparator gain with increasing sampling rate (by 6 dB per octave) accounts for the smaller than expected improvement in in-band noise.

This smaller than expected improvement in in-band noise at higher sampling rates is not real, however, but is an artifact of the crude approximations made in estimating the comparator gain K given in Equation 7.54. In particular, the approximation for $\overline{Y}_{th}$ given in Equation 7.53 is not accurate for sampling rates above 20 GHz. Above 8 GHz, the impedance of inductor L_r is larger than Z_0 and cannot be ignored. Since the impedance of the inductor increases with frequency, the frequency-averaged admittance $\overline{Y}_{th}$ is reduced at higher sampling rates. If $\overline{Y}_{th}$ is reduced in direct proportion to the sampling clock period, Equations 7.50 and 7.51 show that the effective comparator gain K remains unchanged with increasing sampling rate. JSIM simulations of an idealized bandpass modulator, described

Table 7.1: In-band noise predicted by linearized model.

	Sampling Rate	
Bandwidth	20 GHz	40 GHz
9.8 MHz	-84.8 dBFS	-87.8 dBFS
19.5 MHz	-75.8 dBFS	-78.8 dBFS
39 MHz	-66.7 dBFS	-69.7 dBFS

in Section 8.3 of the next chapter, demonstrate that an increase in sampling rate from 20 to 40 GHz does not reduce the comparator gain K significantly and, consequently, the in-band noise is reduced by 8-9 dB, close to the ideal value. Because of the difficulty in estimating the comparator gain K, the in-band noise levels shown in Table 7.1 should not be considered reliable indicators of modulator performance but are provided here as reference points for the more accurate circuit simulation results presented later.

The degradation of quantization noise shaping with lower values of loaded Q is illustrated in Table 7.2. An increase in the coupling capacitance C_c from 0.11 pF to 1 pF reduces the loaded Q at quarter-wave resonance from about 6050 to 121. (All other circuit parameters are unchanged.) With such a modest value of loaded Q, the notch in the quantization noise spectrum at the resonant frequency is no longer sharp and deep, but washed out and relatively shallow. The elevation of in-band noise levels is easily observed in comparing Tables 7.1 and 7.2. The degradation of performance is greater for narrower bandwidths, which benefit the most from a deep notch at resonance. For this reason, the in-band noise over a 9.8 MHz bandwidth is only 4.1 dB lower than over a 19.5 MHz bandwidth, instead of the 9 dB difference expected with ideal noise shaping. Since the loaded Q of the superconducting resonator used in the experimental modulator is much larger than 121 (even after accounting for physical losses in the transmission line), such degradation of quantization noise shaping is negligible.

7.3 Other Superconducting Bandpass $\Delta\Sigma$ Modulators

Historically, the first proposal for a superconducting bandpass $\Delta\Sigma$ modulator is the patent by Przybysz and Miller [67]. The circuit described in their patent is illustrated in Figure 7-20. The analog input is applied to an *RLC* circuit which is resonant at the center frequency of the input signal. The current flowing through the inductor is quantized by Josephson junction J_1, which serves as a simple comparator. If the sum of i_L and the peak current from the sampling pulse generator exceeds its critical current, junction J_1 switches, and an SFQ pulse appears on the output of the modulator. Otherwise, the junction does not switch, and no SFQ pulse is generated. In accord with the RSFQ basic convention, each SFQ output pulse represents a binary 1, and its absence represents a binary 0. A straightforward modification of the circuit would be to replace this single-junction comparator with the two-junction comparator described earlier in this chapter. Though not discussed in their patent, such a modification would make the circuit more compatible with standard RSFQ clock drivers such as JTL amplifiers.

The major difference between this modulator and the one investigated in this thesis

Table 7.2: In-band noise with reduced loaded Q of resonator ($Q_{ld} = 121$).

	Sampling Rate	
Bandwidth	20 GHz	40 GHz
9.8 MHz	-74.7 dBFS	-77.8 dBFS
19.5 MHz	-70.6 dBFS	-73.6 dBFS
39 MHz	-64.8 dBFS	-67.8 dBFS

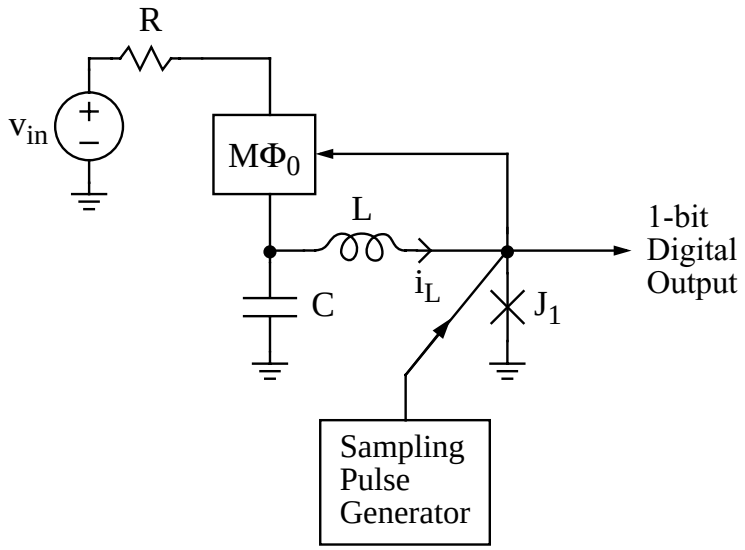


Figure 7-20: Superconducting bandpass ΔΣ modulator employing multiple flux quanta feedback.

project is the manner in which feedback to the resonator is implemented. In the circuit of Figure 7-20, kickback from the SFQ comparator does reduce the inductor current i_L, but additional feedback to the resonator is provided with an outer loop connected to a multiple flux quanta generator, which produces M feedback SFQ pulses for each SFQ pulse appearing across junction J_1. This type of multiple flux quanta feedback has also been proposed for realizing second-order low-pass ΔΣ modulators [56, 58, 57]. Even though the loaded Q of the resonator is small (only 3.2 for the example values given in the patent), a large suppression of in-band noise is achieved because of the large loop gain provided by the multiple flux quanta feedback. The patent presents analysis showing that in-band SNR improves with larger values of M, up to the point where modulator stability is compromised. For the example given in the patent, the ideal value of M is about 50. Even higher values of M would be needed if the loaded Q were increased. Consider, for instance, increasing resistance R. Such a change increases the loaded Q proportionately, but the larger series resistance reduces the current generated by the multiple flux quanta feedback. To maintain the same gain in the outer loop, M also needs to be increased proportionately. In the example given in the patent, the center frequency is only 150 MHz, and the signal bandwidth is 60 MHz. For center frequencies which are much greater than the signal bandwidth, higher values of loaded Q would be required, and M would need to be quite large.

Unfortunately, implementation of the multiple flux quanta feedback generator is difficult. Because Josephson devices have relatively low gain, complex circuits using many junctions are needed to implement a feedback generator with a significant value of M [57, 154]. Due to inevitable gain-bandwidth limitations, the circuit delay of a feedback generator with a large value of M is significantly longer than the switching time of a simple SFQ comparator. Consequently, the maximum sampling rate of the modulator shown in Figure 7-20 is much lower than the sampling rates demonstrated in this project. Experimentally, only feedback generators with small values of M (≤ 4) have been demonstrated to date [35, 58]. One such small feedback generator was used to demonstrate a second-order low-pass ΔΣ modulator,

but the sampling rate was only 180 MHz [35], so feedback delays were inconsequential.

A more practicable superconducting bandpass $\Delta\Sigma$ modulator has been proposed by Fujimaki and his research group at Nagoya University [10]. Though discovery was independent, their circuit is identical to the lumped element modulator of Figure 7-1. The operation of their modulator was confirmed by circuit simulations similar to those presented in the next chapter. Their design does not incorporate any of the circuit refinements described in Section 7.1.2, and the effect of finite source resistance on the loaded Q of the resonator is not discussed in their paper. The first experimental demonstration of a superconducting bandpass $\Delta\Sigma$ modulator was reported less than two years ago by Hashimoto and his research group at ISTEC [155]. The schematic of their experimental modulator is identical to the lumped element circuit described and simulated by Fujimaki and his co-workers. The measured performance was far below the theoretical limit of the Josephson circuitry. The difficulties of high speed interfacing with room-temperature test equipment limited the sampling rate to only 2.86 GHz, and the measured in-band noise was higher than expected, possibly due to crosstalk from external clock and ac bias lines [156]. The modulator center frequency was 0.71 GHz. An LC circuit with such a low resonant frequency requires a large value (540 pF) of capacitance for a Josephson integrated circuit, and their layout shows a triangle-shaped capacitor which is over 1 mm long. A capacitor with such physical dimensions cannot be considered a lumped element on the picosecond time scale of the SFQ pulse. In principle, higher-order resonances of the structure may appear in the digital output code of the modulator as aliased modes, but their data show only one minimum in the quantization noise spectrum, at the modulator center frequency. One possible explanation for the lack of aliased modes might be that the higher-order resonances excited by each SFQ pulse have low enough values of loaded Q that they dissipate before the next sampling period. Such resonances might be more visible in the output spectrum at higher sampling rates.

7.4 Summary

This chapter has explained the operating principles of superconducting bandpass $\Delta\Sigma$ modulators. Important design considerations not discussed in the open literature have been studied. The design of the input coupling network is critical in maintaining high loaded Q with practical source resistances, and capacitive coupling of the input permits a fundamentally better tradeoff between loaded Q and input sensitivity. Circuit refinements to improve bias stability and comparator performance near metastability have also been described. In current Josephson technology, a transmission line resonator is the most practical type for the superconducting bandpass $\Delta\Sigma$ modulator. The output spectrum of a bandpass modulator based on a transmission line is complicated by the large number of resonant modes, including aliased modes due to resonances at frequencies above half the sampling rate. Interference from aliased modes should be avoided through careful selection of resonant frequencies, limiting the loaded Q values of higher-order modes, and employing a very high sampling rate. The performance of the modulator as an ADC for narrowband RF signals has been estimated with a linearized model, in which the comparator is modeled as a source of additive white noise. In the next chapter, such estimates are compared with the results of detailed JSIM circuit simulations.

Chapter 8

Simulated Modulator Performance

This chapter presents the results of JSIM circuit simulations of a superconducting bandpass $\Delta\Sigma$ modulator based on a transmission line resonator. The simulated output spectra show close agreement with the NTF calculated in the last chapter and exhibit the effects of aliased modes. The in-band noise, however, is significantly higher than that predicted by the linearized model. Delay modulation effects in the SFQ comparator are shown to be responsible for this excess noise near the resonant frequency. Finally, the simulated SNR and intermodulation distortion of the modulator are presented and discussed.

8.1 Simulated Circuit

Figure 8-1 is a detailed schematic of the circuit simulated with JSIM; circuit parameters are listed in the figure caption. The heart of the circuit is the bandpass $\Delta\Sigma$ modulator introduced in the last chapter. In order to make the simulation as realistic as possible, the inductance values, including parasitics L_{p1} through L_{p4}, were calculated from the physical layout of the modulator fabricated and tested in this thesis project. (The inductance calculation program Lmeter [157] and other software tools used in designing the modulator test chip are reviewed in Chapter 10.) Voltage source v_{in}, resistor R_s, and capacitor C_c represent the Thévenin equivalent circuit for the input coupling network (Figure 7-19) of the experimental modulator. A four-stage JTL driven by voltage source V_c operates as a sampling pulse generator, which triggers junction J_3. According to the Josephson voltage-frequency relation, the sampling rate equals V_c/Φ_0. The four junctions in the JTL and junction J_3 have a large critical current (1.0 mA) so that a robust and low impedance clock driver is obtained. In the simulations, bias voltage V_b is slightly higher than $V_c/2$, so that the SFQ comparator produces slightly more 1's than 0's in the output code (e.g., 51.2% versus 48.8%). This avoids the idle tone problems sometimes observed when the modulator is biased at exactly half of full-scale. As explained in the last chapter, current source I_0 biases the SFQ comparator for best performance near metastability. The large value of bias current I_b (1.04 mA) compensates for the current drawn away from J_3 by source I_0. A one-stage shift register provides a realistic load for the SFQ comparator. The data and clock outputs of the circuit are terminated with appropriate loads in the form of one-stage JTLs. Termination of the one-stage JTLs is not critical since JTLs are among the most robust circuits in RSFQ logic [158].

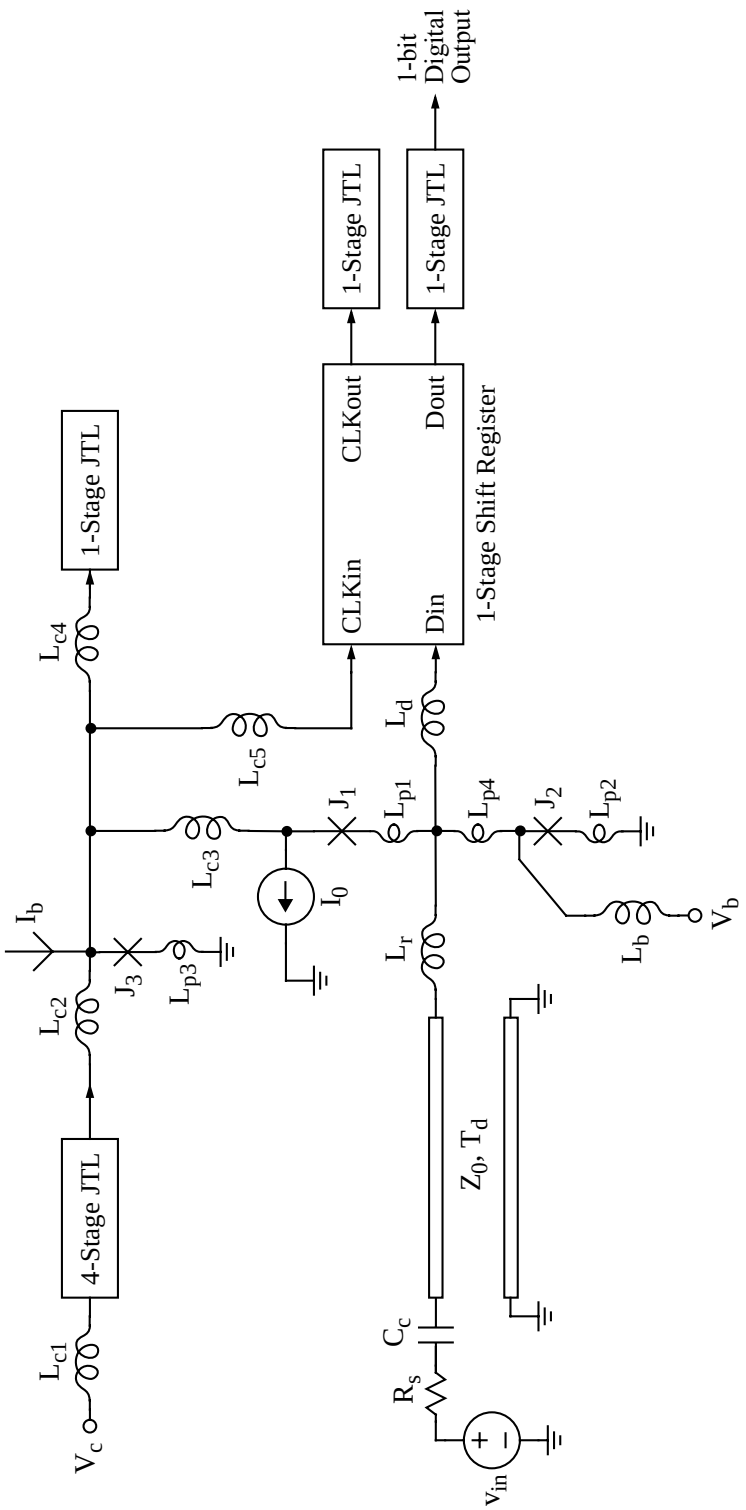


Figure 8-1: Superconducting bandpass $\Delta\Sigma$ modulator loaded by one stage of shift register. The circuit parameters are: R_s=62.25 Ω, C_c=0.11 pF, Z_0=1 Ω, T_d=100 ps, L_r=20 pH, L_b=100 pH, L_{c1}=2.4 pH, L_{c2}=0.99 pH, L_{c3}=0.74 pH, L_{c4}=1.89 pH, L_{c5}=1.91 pH, L_d=4.81 pH, L_{p1}=0.41 pH, L_{p2}=0.06 pH, L_{p3}=0.06 pH, L_{p4}=0.30 pH, I_{c1}=I_{c2}=271 μA, I_{c3}=1.0 mA, I_0=380 μA, and I_b=1.04 mA.

The one-stage shift register circuit is detailed in Figure 8-2. The design is based on the buffered RSFQ shift register cell first shown by Mukhanov [159] and is optimized for concurrent flow clocking, in which the data and clock pulses travel in the same direction. For proper operation, the clock pulse should trigger the decision-making pair J_4–J_5 before the data pulse is stored as a circulating current through storage inductor L_q. The delay added by the buffering JTL comprising junctions J_1 through J_3 ensures that this race condition is satisfied. The buffering JTL also reduces hysteresis in the SFQ comparator of the modulator. Because circuits based on two-terminal devices offer relatively limited isolation, the loading of one Josephson circuit by another often has significant effects. In this case, the presence or absence of a circulating current through L_q affects the operating point of the SFQ comparator and, therefore, its threshold. Since the bit stored (as a circulating current) in the shift register represents the previous decision of the comparator, the threshold of the comparator is hysteretic, depending on its previous decisions. The magnitude of the hysteresis is reduced by adding more junctions to the buffering JTL. The use of a three-junction buffering JTL reduces the hysteresis of the comparator threshold to about 6 μA, comparable to the input noise level of the comparator [136].

The version of JSIM used for the simulations includes the stochastic extension reported by Satchell [160] for modeling thermal noise. Included in the circuit model are the Johnson noise sources from the room-temperature (300 K) source resistance (50 Ω), the resistors in the input coupling network (at 4.2 K), and the shunt resistors of the Josephson junctions (also at 4.2 K). The effects of random clock jitter can be studied by varying the intensity of the noise sources inside the four-stage JTL which generates the sampling pulses. On the experimental test chip, the current pulses from the on-chip MSM photodiode are converted into SFQ clock pulses by the SFQ pulse generator used in the optically triggered JTL

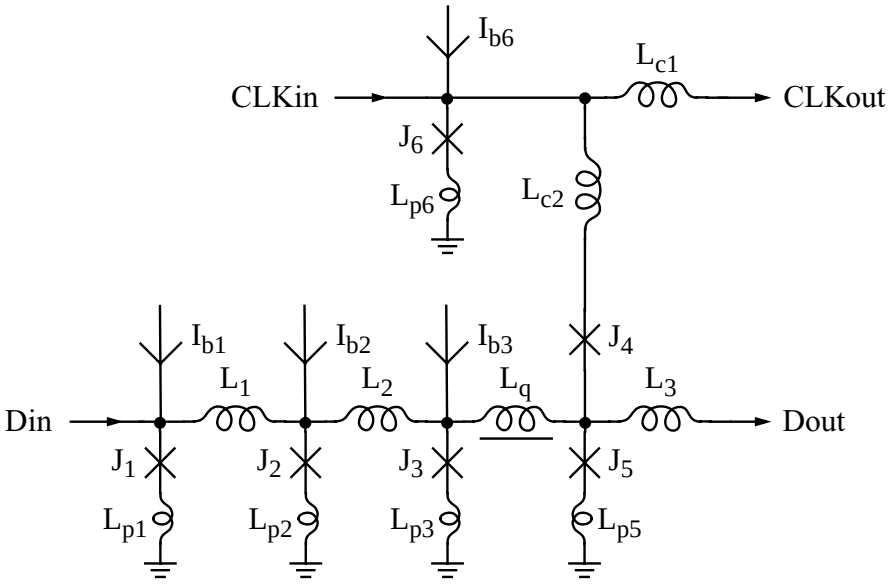


Figure 8-2: Buffered RSFQ shift register cell. The circuit parameters are: L_1=4.0 pH, L_2=2.74 pH, L_3=4.84 pH, L_q=6.0 pH, L_{c1}=1.86 pH, L_{c2}=2.06 pH, L_{p1}=L_{p2}=0.15 pH, L_{p3}=0.13 pH, L_{p5}=0.19 pH, L_{p6}=0.14 pH, I_{c1}=I_{c2}=I_{c3}=245 μA, I_{c4}=221 μA, I_{c5}=271 μA, I_{c6}=500 μA, I_{b1}=196 μA, I_{b2}=205 μA, I_{b3}=119 μA, and I_{b6}=414 μA.

experiment (Figure 6-7). In order to maintain high input sensitivity and minimize the required optical power incident on the photodiode, a junction with relatively small critical current (171 μA) is used in the SFQ pulse generator. The output of this SFQ pulse generator is fed into a thirteen-stage JTL amplifier. The current gain of this amplifier allows it to drive the SFQ comparator of the modulator with a low impedance. The accumulation of jitter through the JTL amplifier was studied with a JSIM simulation in which each junction was shunted with a noise current corresponding to the Johnson noise of its shunt resistor. For the parameters used on the experimental test chip[1], the simulation showed that the jitter accumulated through the JTL amplifier equals about 0.32 ps rms. In simulating the superconducting modulator with the circuit of Figure 8-1, the noise sources inside the four-stage JTL were increased in intensity until the jitter of the SFQ pulses clocking the SFQ comparator equaled 0.32 ps rms, to match the experimental conditions as closely as possible.

The junction parameters are typical of a niobium process with 1 kA/cm^2 critical current density [123]. For each junction in the circuit, the shunt resistor is chosen for critical damping ($\beta_c = 1$), and the product of the critical current and shunt resistance equals 300 μV. The transmission line resonator is represented with the ideal transmission line model available in JSIM, so losses in the superconducting microstrip line are ignored in the simulations.

8.2 Output Spectra

Figure 8-3 plots the simulated output spectra of the modulator at a 20 GHz sampling rate with (a) no input and (b) a large input (1.0 dB below full-scale (FS)) at 2.13 GHz. The output code length in each simulation is 131072. Periodogram averaging [1] is used to reduce the variance of the spectral estimates. Specifically, each output code is divided into multiple 16384-bit segments, each of which is windowed by a Blackman window and transformed into a spectral estimate with a 16384-point FFT. Averaging of these spectral estimates yields the spectra shown in the figure. Under both input conditions, proper noise shaping is observed. The minimum in the quantization noise near 2.05 GHz corresponds to quarter-wave resonance of the transmission line. The simulated in-band idle channel noise at a 20 GHz sampling rate is listed in the second column of Table 8.1 for three different signal bandwidths. The in-band noise in the presence of a large input (calculated from the spectrum of Figure 8-3(b)) is less than 1 dB higher than the values listed in the table. As predicted by the linearized model studied in the last chapter, other minima are visible in the quantization noise spectrum. The minimum at dc is due to bias inductor L_b, and the minima at higher frequencies correspond to higher-order transmission line modes. All of these higher-order modes except the one at 6.32 GHz are aliased modes, corresponding to physical resonances above 10 GHz.

Figure 8-4 plots the simulated output spectra of the modulator at a 40 GHz sampling rate with (a) no input and (b) a large input (-1.0 dBFS) at 2.13 GHz. The output code lengths are again 131072, and periodogram averaging identical to that described in the

[1]In retrospect, lower jitter could probably be achieved by using a JTL amplifier with fewer stages. Such a redesign is not a priority, however, as the simulations presented in this chapter indicate that random clock jitter is not the dominant source of in-band noise for the superconducting modulator.

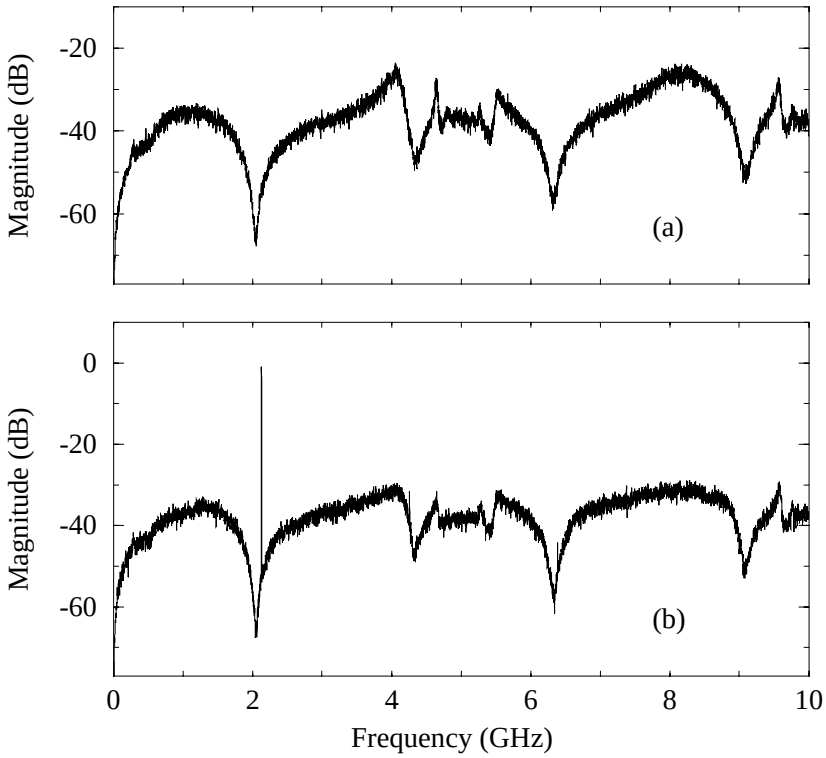


Figure 8-3: Simulated output spectra of superconducting bandpass modulator sampling at 20 GHz with (a) no input and (b) a large input (-1.0 dBFS) at 2.13 GHz.

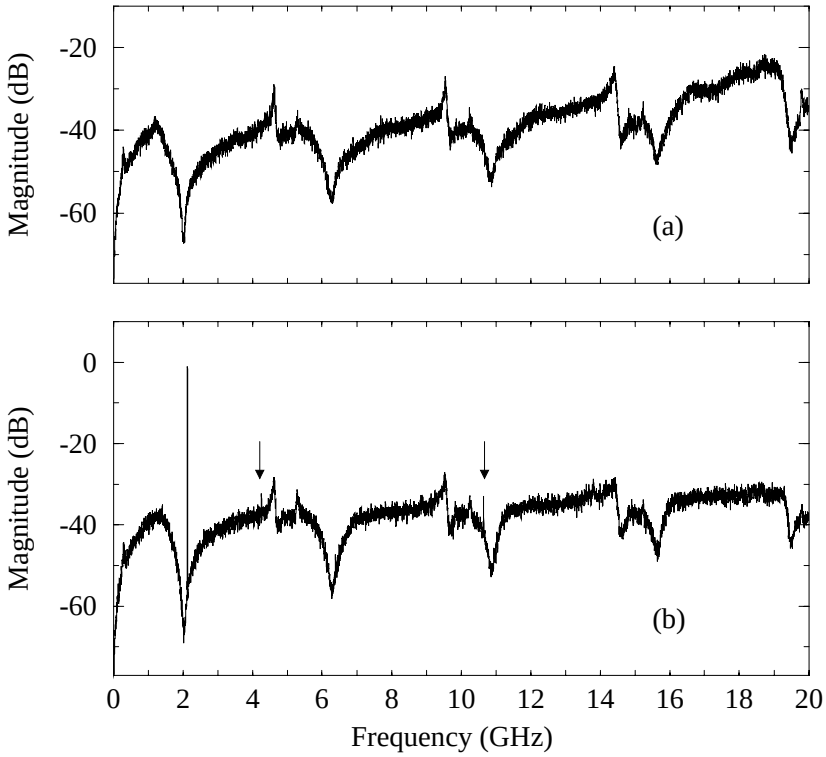


Figure 8-4: Simulated output spectra of superconducting bandpass modulator sampling at 40 GHz with (a) no input and (b) a large input (-1.0 dBFS) at 2.13 GHz.

Table 8.1: Simulated in-band noise with no input.

	Sampling Rate	
Bandwidth	20 GHz	40 GHz
9.8 MHz	-59.7 dBFS	-62.6 dBFS
19.5 MHz	-56.5 dBFS	-59.2 dBFS
39 MHz	-52.5 dBFS	-56.2 dBFS

previous paragraph is used to reduce the variance of the spectral estimates. The increase in sampling rate reduces the number of aliased modes which affect the quantization noise shaping. Most of the minima in the quantization noise spectrum now occur at frequencies equal to the physical resonances of the transmission line – roughly, at odd multiples of quarter-wave resonance. The simulated in-band idle channel noise at a 40 GHz sampling rate is listed in the third column of Table 8.1 for three different signal bandwidths. Because of the higher oversampling ratio, the in-band noise is lower at a 40 GHz sampling rate than at a 20 GHz sampling rate, though only by about 3 dB. The reason for this relatively small improvement is explained later in the next section.

The modulator does not operate reliably at sampling rates much higher than 40 GHz. If the clock period is too small, the SFQ comparator does not have enough time to recover from metastable conditions with a high probability. Occasionally, the comparator generates SFQ output pulses which are late enough that they violate the setup time of the one-stage shift register, and bit errors in the output code are produced. Even at a sampling rate of 40 GHz, the output code contains some bit errors due to metastability, but the error rate (less than 1 in 10^5 clock cycles) is low enough not to affect ADC performance.

Some harmonic distortion, such as the tones identified by arrows in Figure 8-4(b), is generated when the modulator is driven by large inputs. The spectral distribution of the harmonic distortion is similar to the shaping of the quantization noise, with the largest harmonic components found at frequencies with small loop gain. Such frequency-shaped distortion is exhibited even by ideal $\Delta\Sigma$ modulators [161] and does not indicate a problem in circuit operation. Since the harmonic components are at frequencies much higher than the signal band, they are easily removed by digital filtering of the modulator output and have little effect on ADC performance. The in-band intermodulation distortion of the bandpass modulator is much more important and is examined at the end of the chapter.

Figure 8-5 compares the simulated idle channel spectrum of Figure 8-3(a) with the quantization noise spectrum predicted by the linearized model, whose NTF was calculated in the last chapter. The overall contour of the simulated spectrum, including the locations and shapes of its maxima and minima, is remarkably similar to the prediction of the linearized model. In the linearized model, the comparator is assumed to have a delay of 3 ps. As pointed out in the last chapter, incorporating such a delay into the linearized model makes the peaks in the NTF larger and sharper. As illustrated in Figure 8-5, peaks of similar magnitude and sharpness are also observed in the JSIM simulation data. (Note, for example, the maxima near 4.1 and 8.2 GHz).

Closer examination of the figure, however, reveals a few discrepancies between the simulated spectrum and the prediction of the linearized model. At most frequencies, the simulated quantization noise is a few dB higher than predicted by the linearized model. As

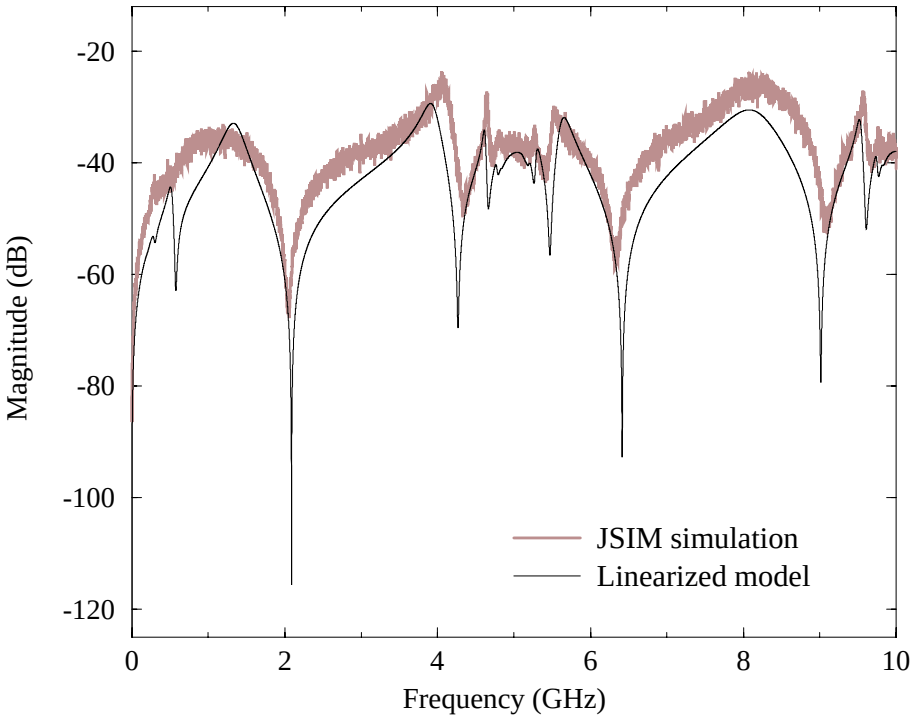


Figure 8-5: Comparison of simulated idle channel spectrum with prediction of linearized model. The sampling rate is 20 GHz.

noted in the last chapter, Equation 7.54 tends to overestimate the comparator gain K – by a factor of 1.6, for the circuit parameters used in this simulation. Since the actual loop gain of the modulator is smaller than expected, somewhat higher noise is observed at most frequencies.

The locations of the minima in the simulated noise spectrum are also slightly shifted from the locations predicted by the linearized model. For instance, the minimum corresponding to quarter-wave resonance is located at 2.09 GHz in the linearized model but at 2.05 GHz in the simulated spectrum. In principle, parasitic inductances in the simulated circuit (such as L_{p2} and L_{p4} in Figure 8-1) reduce the resonant frequencies of the transmission line, but their values are too small to account for the observed shifts in the minima. The shifts in the minima are primarily due to the nonlinear inductance of junction J_2 in the SFQ comparator of the modulator. Equation 7.17 of the last chapter expresses the nonlinear inductance of a Josephson junction in terms of its critical current I_c and its phase ϕ. Even its minimum value (at $\phi = 0$) is larger than the parasitic inductances just mentioned. Moreover, its value increases considerably during the generation of an SFQ pulse, when ϕ increases by 2π. The inductance is even momentarily infinite at $\phi = \pi/2$ and $\phi = 3\pi/2$. While the short duration of the SFQ pulse diminishes the significance of the large inductance values during switching, the effective inductance (in a time-averaged sense) is still high enough to reduce the resonant frequencies of the transmission line, thereby accounting for the observed shifts in the quantization noise minima. Additional evidence for this explanation is provided by the simulation data at a sampling rate of 40 GHz. At this higher sampling rate, the time duration of each SFQ pulse is a larger fraction of the clock period, and the effective

inductance of junction J_2 in the SFQ comparator is influenced more by the large inductance values during switching. Consequently, the quantization noise minimum corresponding to quarter-wave resonance is shifted even further from the prediction of the linearized model and is found at 2.02 GHz. In general, the nonlinear inductance of junction J_2 reduces the frequencies of the transmission line resonances. Due to the nature of aliasing, some of these downward-shifted resonances are aliased to frequencies which are *higher* than the values predicted by the linearized model. (In Figure 8-5, note the aliased modes near 4.3 and 9.0 GHz). Since simulations show that the shift in the quarter-wave resonant frequency is virtually independent of the input conditions of the modulator, the center frequency of the modulator can be compensated (for a given sampling rate) by minor adjustment of resonator parameters. Simulations presented at the end of the chapter also indicate that the nonlinear inductances of the Josephson junctions do not cause problems with intermodulation distortion.

The most serious discrepancy between the simulated spectrum and the prediction of the linearized model is the lack of depth in the simulated quantization noise minima, indicating excess noise at the resonant frequencies. Because of the excess noise at quarter-wave resonance, narrowing the bandwidth by a factor of two reduces the in-band noise by only 3-4 dB, as illustrated in Table 8.1. In comparison, the linearized model predicts a 9 dB reduction in in-band noise for a one-octave decrease in signal bandwidth (cf. Table 7.1). For the signal bandwidths and sampling rates considered in Tables 7.1 and 8.1, the simulated in-band noise is significantly higher than predicted by the linearized model – by 14–25 dB, with the degradation being larger at narrower bandwidths. In principle, thermal noise and clock jitter increase the in-band noise of the modulator, but turning off the thermal noise sources in the simulation (including those inside the four-stage JTL that are used to model random clock jitter) reduces the in-band noise by only 1.7 dB. As the next section explains, the excess noise at quarter-wave resonance is not due to thermal noise or clock jitter but to delay modulation in the SFQ comparator [2].

8.3 Effect of Delay Modulation in SFQ Comparator

As in the case of semiconductor voltage comparators [162, 163], the response time of the SFQ comparator is a function of input overdrive level. Figure 8-6 shows the SFQ pulse generated by the comparator for two different levels of overdrive. If the input current is 100 μA above threshold, the comparator is far from metastability, and its lower junction (J_2 in Figure 8-1) switches without hesitation. In this case, the delay of the output SFQ pulse is short. If the input current is only 10 μA above threshold, the comparator is driven temporarily into a metastable state, in which the phases of the two junctions in the comparator are close to π, corresponding to inverted pendula in the pendulum analogy

[2] While the thermal noise and clock jitter in the circuit model increase in-band noise by 1.7 dB, the *direct effect* of thermal noise and clock jitter on modulator performance is smaller than this number suggests. Because delay modulation in the SFQ comparator is responsible for most of the in-band noise, even a small change in the amount of delay modulation affects the in-band noise level. Adding thermal noise and clock jitter to the circuit model changes the amount of delay modulation by altering the statistics of the comparator input current. If, as explained in the next section, the magnitude of the delay modulation is reduced to a negligible level by reducing the circuit time constants, the in-band noise due to thermal noise and clock jitter is lower than one would predict from the 1.7 dB number mentioned above. For all practical purposes, the performance of the current modulator design is not limited by thermal noise or random clock jitter.

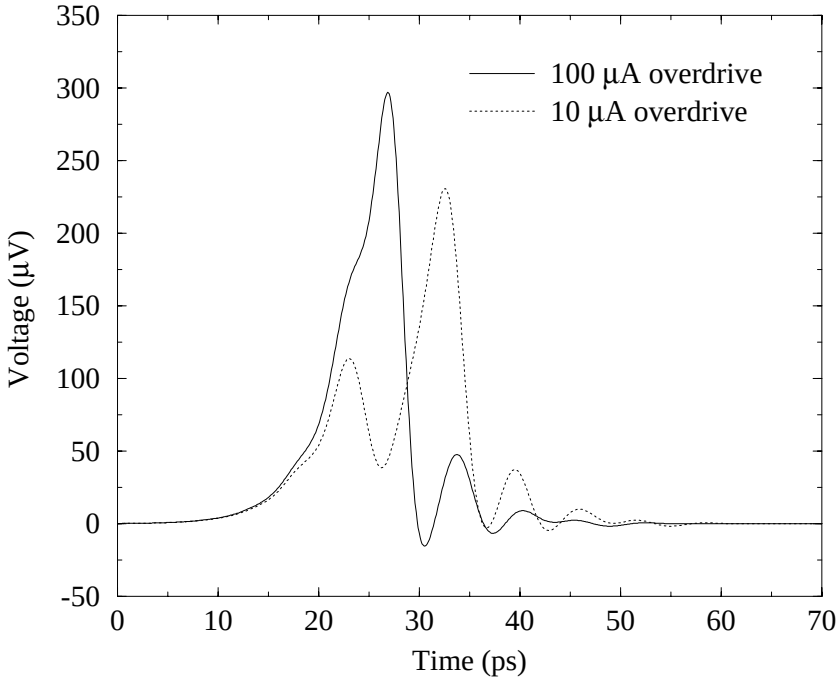


Figure 8-6: SFQ pulse generated by comparator for two different input overdrive levels.

of Section 2.2.1. Since the voltage across the lower junction is proportional to the time derivative of its phase, the output voltage is small while the junctions are hung up in this unstable state. (In Figure 8-6, note the dip in voltage at $t = 26$ ps.) Eventually, the comparator recovers from this unstable state and completes its decision, but the output pulse is delayed by the time spent during metastability. The natural quantization of the SFQ pulse ensures that the areas of both voltage pulses in Figure 8-6 are exactly equal to Φ_0. This preservation of pulse area, even under metastable conditions, is a unique advantage of SFQ technology and minimizes some of the time domain nonidealities that limit the performance of semiconductor bandpass $\Delta\Sigma$ modulators [26]. Nonetheless, the modulation of comparator delay with input overdrive evident in Figure 8-6 places significant limitations on the performance of the superconducting modulator. Since the input overdrive of the comparator varies from clock cycle to clock cycle during modulator operation, signal-dependent jitter is added to the SFQ pulses generated by the comparator and "fed back" to the resonator. Such signal-dependent jitter is known to degrade the SNR of continuous-time $\Delta\Sigma$ modulators [163].

The signal-dependent jitter can be reduced in magnitude by careful design of the comparator circuit and proper scaling of resonator impedances. As explained in the last chapter, current source I_0 in Figure 8-1 is used to bias the comparator for fastest recovery from metastability. Reducing the resonator impedances increases the currents quantized by the comparator and decreases the probability of a comparator input which is so close to threshold that it induces metastability. A very low impedance resonator, however, will load the comparator heavily and degrade switching speed. Several JSIM simulations of the modulator with different resonator impedances were run in order to find a good compromise. The lowest simulated in-band noise was obtained with the component values listed

in the caption of Figure 8-1. Even with this optimized circuit, the signal-dependent jitter due to delay modulation in the SFQ comparator is significant – about 1.9 ps rms according to JSIM simulations. Such jitter is almost six times greater than the clock jitter due to thermal noise and is the dominant source of excess noise at quarter-wave resonance.

To check this explanation for the excess noise, the time constants of the SFQ comparator in the simulation were greatly reduced by setting the junction capacitances to zero and by increasing the shunt resistances so that the I_cR_n products equaled 4.7 mV (impossibly high for niobium junctions [29], but useful here for modeling an idealized modulator). The change in time constants does not eliminate delay modulation in the comparator but reduces its magnitude to a negligible level. The thermal noise sources in the simulation (including those used to model random clock jitter) were turned off so that the increase in in-band noise due to delay modulation could be studied in isolation. Figure 8-7 plots the idle channel spectrum of the modulator when simulated under these conditions. Periodogram averaging identical to that described earlier is used to reduce the variance of the spectral estimate. Because delay modulation in the SFQ comparator is now negligible, the in-band noise is no longer degraded by signal-dependent jitter, and the minimum in the quantization noise spectrum at quarter-wave resonance is much deeper (by 24 dB). Due to the shorter time constants, the time duration of each SFQ pulse is now a smaller fraction of the clock period, and the effective inductance of junction J_2 in the comparator is influenced less by the large inductance values during switching. For this reason, the location of the quantization noise minimum corresponding to quarter-wave resonance (2.074 GHz) is closer to the prediction of the linearized model (2.09 GHz).

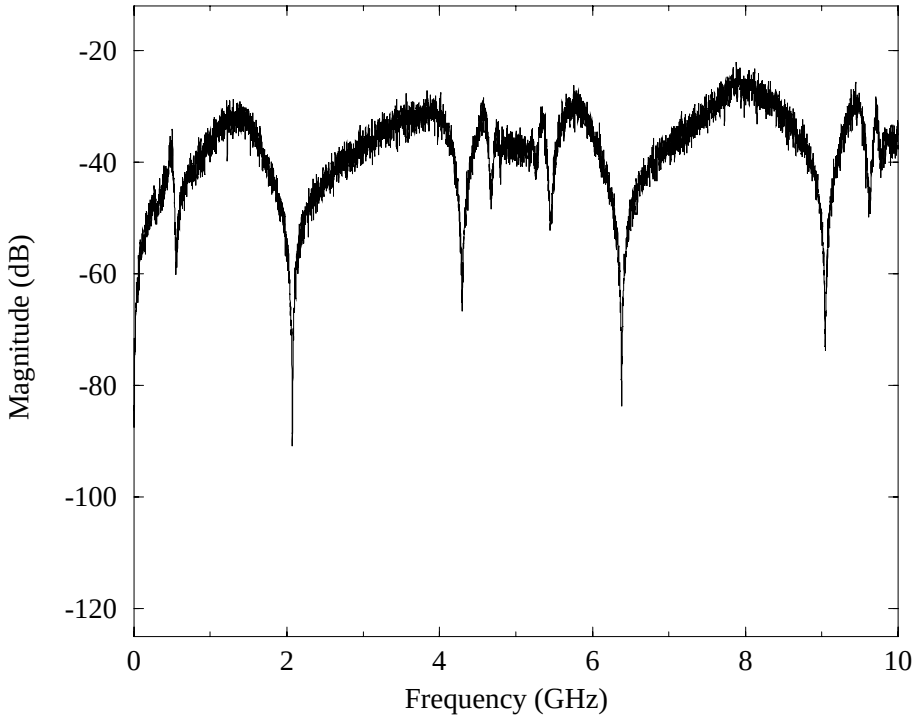


Figure 8-7: Simulated idle channel spectrum with negligible delay modulation in SFQ comparator. The sampling rate of the modulator is 20 GHz.

Table 8.2: Simulated in-band idle channel noise with negligible delay modulation in SFQ comparator.

	Sampling Rate	
Bandwidth	20 GHz	40 GHz
9.8 MHz	-77.4 dBFS	-84.9 dBFS
19.5 MHz	-67.6 dBFS	-76.9 dBFS
39 MHz	-59.6 dBFS	-67.8 dBFS

Table 8.2 presents the simulated in-band idle channel noise of the modulator with negligible delay modulation in the SFQ comparator, for three different signal bandwidths and two different sampling rates. Because the minimum in the noise spectrum near quarter-wave resonance is now much deeper, a one-octave reduction in signal bandwidth reduces the in-band noise by about 8-9 dB, close to the 9 dB value predicted by the linearized model. The in-band noise levels are still 2-8 dB higher than predicted (cf. Table 7.1), but these differences are primarily due to overestimating the comparator gain K in the linearized model. In fact, the in-band noise levels listed in Table 8.2 are more representative of the performance of an ideal bandpass $\Delta\Sigma$ modulator than are the values predicted by the linearized model, whose quantitative accuracy for single-bit $\Delta\Sigma$ modulators is limited [20]. Doubling the sampling rate from 20 to 40 GHz reduces the in-band noise by 8-9 dB, close to the 9 dB/octave rate expected for a bandpass modulator employing a single resonator [23].

Comparison of Tables 8.1 and 8.2 shows that the degradation of performance due to delay modulation in the SFQ comparator is substantial. For the bandwidths and sampling rates considered in the tables, the signal-dependent jitter of a comparator with realistic junction parameters (typical of a niobium process with 1 kA/cm^2 critical current density) increases the in-band noise by 7-22 dB, with the degradation being larger at higher oversampling ratios. While future scaling of Josephson technology to submicron dimensions [31, 164, 48, 165] would decrease circuit time constants and reduce the magnitude of the delay modulation, the importance of the problem will not be diminished by improvements in process technology. Since more advanced technology would allow increased sampling rates and oversampling ratios, the basic problem of delay modulation in the comparator would remain, just on a higher performance plane.

A more fundamental solution would be to improve the design of the comparator circuit itself. In the design of continuous-time $\Delta\Sigma$ modulators in semiconductor technology, signal-dependent jitter is greatly reduced by placing a latch between the comparator and the feedback DAC [166, 163, 26]. Such an approach is more difficult to apply to superconducting circuits based on two-terminal Josephson junctions. Because of the lack of isolation between input and output, the kickback from most SFQ comparators immediately changes the current being quantized, and it is harder to separate the operations of quantization and feedback. Appendix C describes an SFQ comparator based on an "inductive divider", in which *part* of the feedback delivered to the resonator is retimed by an internal latch. As explained in the appendix, this comparator does reduce signal-dependent jitter and improves the quality of noise-shaping near quarter-wave resonance. However, the feedback delay added by the latching circuit reduces the stability of the modulator and decreases the maximum sampling rate. Because the simulated in-band noise increases markedly with

large inputs, the peak SNR is actually slightly lower than for the circuit examined in this chapter. Similar drawbacks to increasing the loop delay with a latch have been observed in the design of semiconductor modulators [163]. The comparator described in Appendix C is a more complex design and has smaller operating margins than the two-junction SFQ comparator considered in this chapter. Because the peak SNR was not improved, this more complex comparator was not chosen for the experimental modulator implemented in this thesis project.

Shortly after the modulator test chip was submitted for fabrication, Semenov presented an intriguing paper [167] describing a "nondestructive" SFQ comparator which uses magnetic coupling rather than direct coupling to eliminate kickback from the comparator, so that *all* of the feedback can be retimed by a latch. In principle, such a comparator would allow the signal-dependent jitter to be reduced to a level which is utterly negligible, but again the latching circuit increases the loop delay. The impact of this delay upon the maximum sampling rate and peak SNR would have to be studied before deciding to use this type of comparator in the bandpass modulator. Such a study has not been conducted in this project, and the design of the optimum comparator circuit for the bandpass modulator remains an important topic of future research.

The bandpass modulator shown in Figure 8-1 is the circuit employed on the test chip fabricated for this thesis project. While the two-junction SFQ comparator does generate SFQ output pulses with significant signal-dependent jitter, its simplicity and large operating margins made it the best candidate for a first laboratory demonstration of the superconducting bandpass $\Delta\Sigma$ modulator. The chapter now returns to a discussion of the simulated performance of this circuit (with realistic junction parameters).

8.4 STF and Input Sensitivity

The simulated STF of the superconducting modulator at a 20 GHz sampling rate is shown in Figure 8-8. In the plot, the STF is normalized to its magnitude at 2.05 GHz, approximately the frequency at which the quantization noise is minimized. The STF is remarkably flat over a broad band of frequencies spanning quarter-wave resonance. Its magnitude varies by less than 1.6 dB between 1.5 and 2.5 GHz and by less than 0.3 dB over signal bands of interest (less than 100 MHz wide). Such small variations are negligible in a real system, as parasitics in the packaging of the chip would likely contribute to greater deviations in frequency response. At an input frequency of 2.05 GHz and a sampling rate of 20 GHz, the input amplitude needed to produce a full-scale (FS) output is 13.8 mV for the simulated circuit. Since the input coupling network (Figure 7-19) of the experimental modulator includes a 6 dB attenuator, this corresponds to a 27.6 mV input amplitude for the real circuit. The simulated input sensitivity is within 0.2 dB of that predicted by Equation 7.36.

8.5 SNR and Stability

Figure 8-9 plots the simulated SNR of the modulator as a function of input signal amplitude, for two different signal bandwidths and two different sampling rates. The input frequency in each case is 2.13 GHz, just above the modulator center frequency. Peak SNR is achieved at an input signal amplitude near -1 dBFS. At a sampling rate of 20 GHz, peak SNR is 55.2 dB

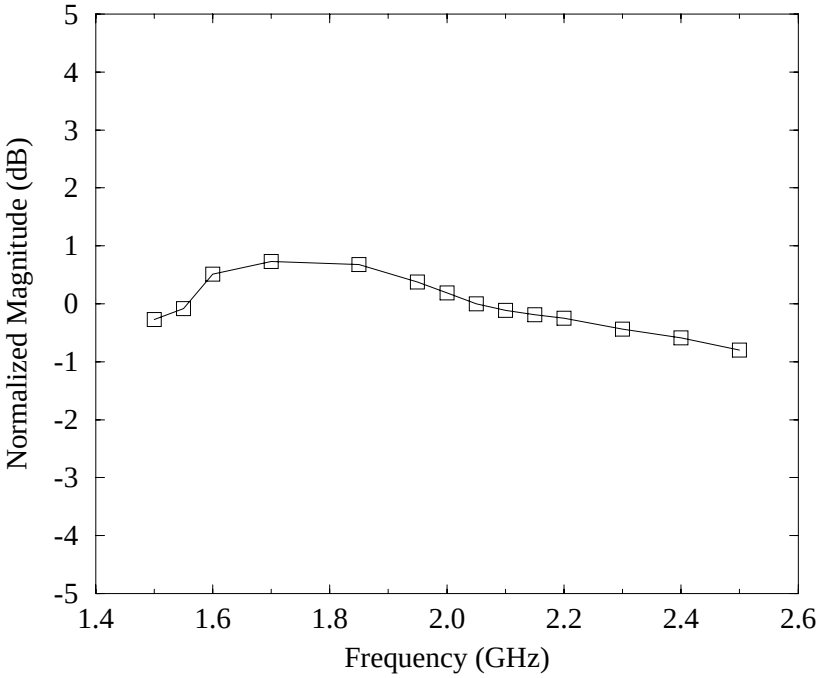
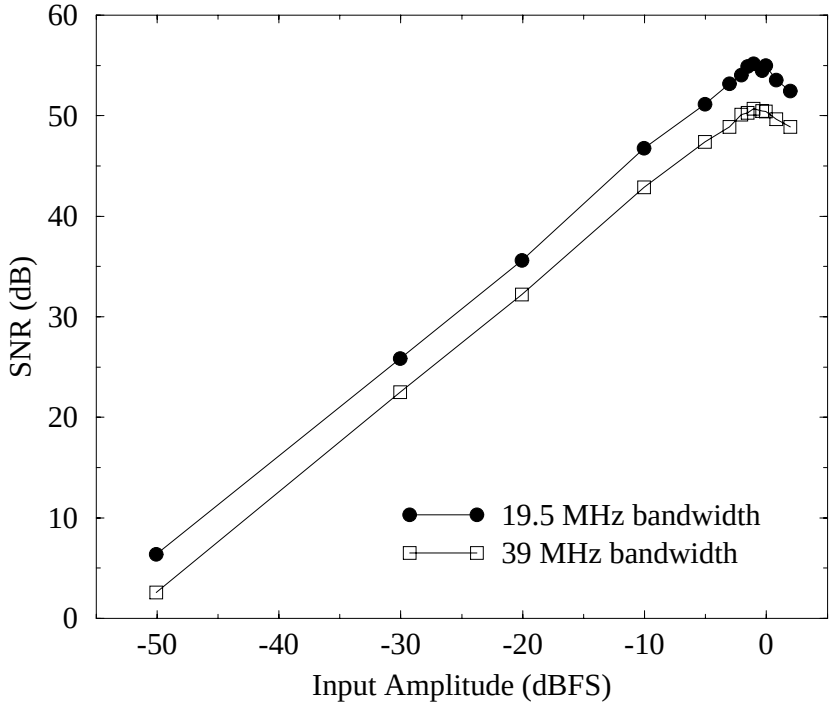


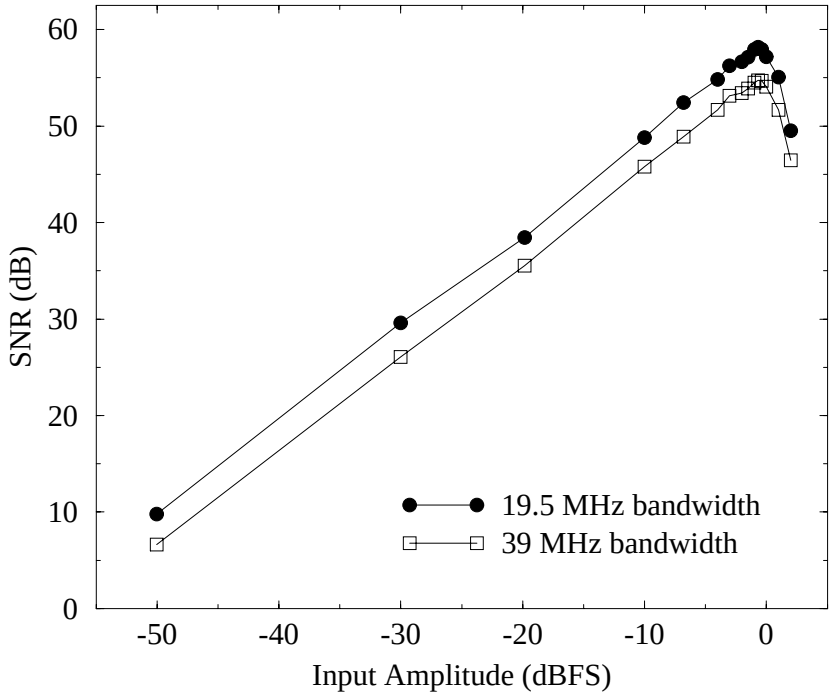
Figure 8-8: Simulated STF of superconducting bandpass $\Delta\Sigma$ modulator, normalized to magnitude at 2.05 GHz. The sampling rate is 20 GHz.

and 50.7 dB over bandwidths of 19.5 MHz and 39 MHz, respectively. At a sampling rate of 40 GHz, peak SNR is 58.2 dB and 54.8 dB over bandwidths of 19.5 MHz and 39 MHz, respectively. Because of the excess noise due to delay modulation in the comparator, a one-octave change in sampling rate or bandwidth changes the peak SNR by only 3-4.5 dB. In all cases, the increase in in-band noise with input signal level is less than 1 dB for inputs as large as -1 dBFS. Signal compression is negligible (< 0.1 dB) for input amplitudes up to 0 dBFS, beyond which compression due to clipping occurs.

The small increase in in-band noise with input signal level and the gradual overload characteristics shown in Figure 8-9 indicate excellent modulator stability [52]. The stability of the modulator was also checked by overloading the modulator for several thousand clock cycles and then examining its return to normal operating conditions. The modulator can be overloaded positively (beyond an output code of all 1's) by raising voltage source V_b in Figure 8-1 from its normal value (e.g., $0.512V_c$) to a high value such as $1.47V_c$. The modulator can be overloaded negatively (beyond an output code of all 0's) by lowering V_b to a negative value such as $-0.45V_c$. In both cases, the modulator recovers from overload and resumes proper operation once V_b is returned to its normal value. In other simulations, the modulator was overloaded for several thousand clock cycles by a 2.13 GHz input with a very large amplitude, such as 8.6 dBFS. According to these simulations, the modulator recovers from overload and resumes proper operation once the input amplitude is reduced below 0 dBFS. The graceful recovery from extreme overload demonstrates that the superconducting modulator is unconditionally stable. In contrast, high-order $\Delta\Sigma$ modulators (such as bandpass modulators employing multiple resonators) are conditionally stable systems, which can be driven by large inputs into oscillations that persist even after the inputs



(a)



(b)

Figure 8-9: Simulated SNR as a function of input signal amplitude for sampling rates of (a) 20 GHz and (b) 40 GHz. The input frequency in each case is 2.13 GHz.

that caused them are removed [168].

8.6 Intermodulation Distortion

Figure 8-10 shows the result of a two-tone intermodulation (IM) distortion test of the superconducting bandpass $\Delta\Sigma$ modulator. The sampling rate is 20 GHz, and both input amplitudes are -6.8 dBFS. The input frequencies (2.09 and 2.13 GHz) have been selected so that the lower third-order IM distortion product falls at the modulator center frequency (2.05 GHz). High frequency resolution is needed in order to detect low-level distortion products above the noise floor. To increase the frequency resolution of the simulated spectrum, the simulation time was increased so that a 524288-point FFT could be applied to the output code. Even with such high resolution, no distortion product at 2.05 GHz can be seen above the noise floor (-81 dBFS). On the other hand, the upper third-order IM distortion product at 2.17 GHz is clearly visible and is -54.8 dBFS. Also visible is the lower fifth-order IM distortion product at 2.01 GHz, with an amplitude of -66.8 dBFS. Because these distortion products lie outside the band of interest, they can be removed with digital filtering and do not affect ADC performance. The relative amplitudes of the distortion products demonstrate that IM distortion is spectrally shaped in the same way as the quantization noise: minimum at quarter-wave resonance and higher at frequencies away from resonance. Such frequency-shaped distortion does not indicate a problem in circuit operation, as even ideal $\Delta\Sigma$ modulators exhibit increased distortion at frequencies where the loop gain is small [161].

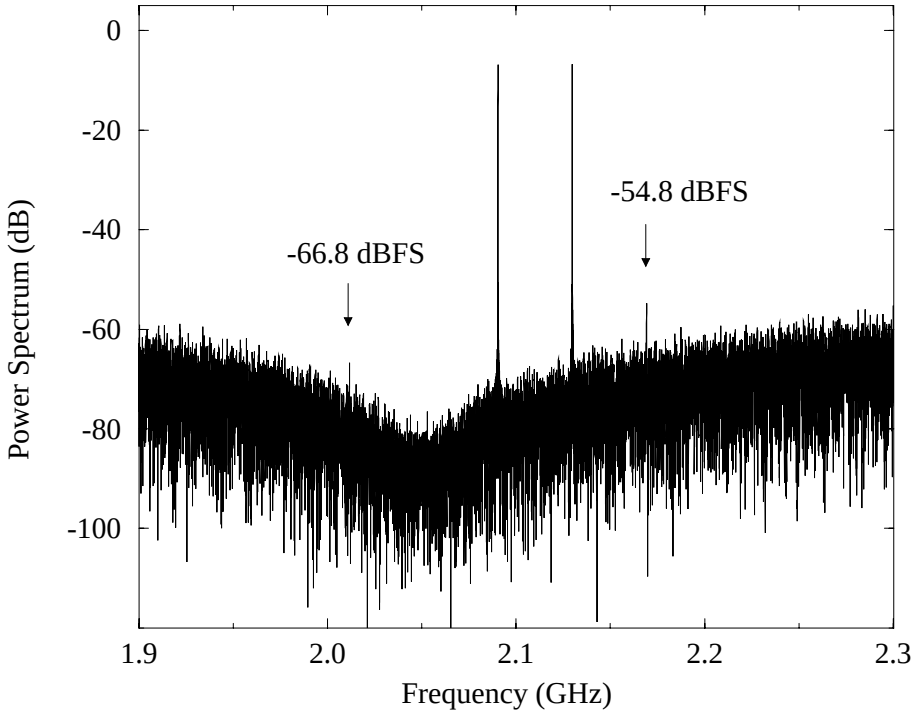


Figure 8-10: Two-tone intermodulation distortion test of superconducting modulator at a sampling rate of 20 GHz.

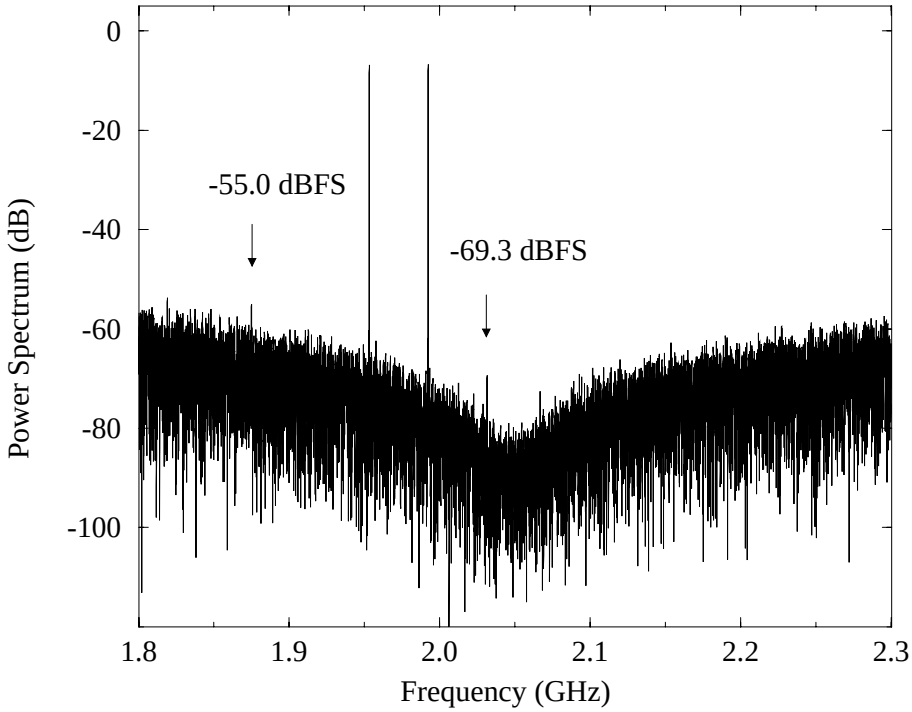


Figure 8-11: Worst-case intermodulation distortion test for a 39 MHz bandwidth and a 20 GHz sampling rate.

Because the IM distortion is frequency-shaped in this way, the largest in-band IM distortion is found at the edges of the signal band. Figure 8-11 shows the result of a worst-case IM distortion test for a 39 MHz bandwidth centered at quarter-wave resonance. Again the sampling rate is 20 GHz, and both input amplitudes are -6.8 dBFS. In this case, the input frequencies (1.953 and 1.992 GHz) have been selected so that the upper third-order and fifth-order IM distortion products fall at 2.031 and 2.07 GHz (the edges of the signal band). The distortion product at 2.031 GHz is clearly visible and is -69.3 dBFS. The distortion product at 2.07 GHz is buried beneath the noise floor (-83 dBFS). A larger (-55.0 dBFS) distortion product at 1.875 GHz is also visible but unimportant since it is out-of-band. Hence, in-band IM distortion is better than -69 dBFS (roughly, 11-bit linearity) over a 39 MHz bandwidth. For narrower bandwidths, in-band distortion is even lower.

Chapter 9

Segmented Correlation

9.1 Motivation

Circuit simulations such as those described in the last chapter show that the superconducting bandpass $\Delta\Sigma$ modulator can achieve sampling rates exceeding 40 GHz. As explained in Section 1.3, testing a superconducting circuit at such high frequencies presents formidable experimental challenges. In this thesis project, a variety of techniques have been developed to overcome such challenges. Other chapters describe the methods (such as optical clocking) used to trigger the superconducting modulator at frequencies in the tens of GHz. This chapter addresses the challenge of handling the modulator output, whose data rate greatly exceeds the capacity of the interface to room-temperature test equipment. The key idea introduced in the chapter is a new ADC testing method based on "segmented correlation", which allows accurate measurement of ADC performance with only limited readout requirements on the interface.

On-chip processing of the output data can be used to reduce the bandwidth requirements for readout, typically at the expense of circuit complexity. For use in an actual system, the preferred approach is to incorporate a complex on-chip decimator, which rejects out-of-band signals and noise with a digital filter so that the sampling rate can be reduced to the Nyquist rate without distortion from aliasing [169]. For a first demonstration of the bandpass modulator studied in this thesis project, however, an on-chip decimator was not an attractive option for several reasons. The design of a digital circuit as complex as a decimator is an enormous challenge with the software tools used in RSFQ circuit design, which are relatively primitive compared with those available in semiconductor circuit design. While an on-chip decimator for baseband ADCs has been demonstrated in RSFQ logic [34], success was only obtained after a number of design iterations [170]. Typically, complex decimator circuits operate at lower frequencies than do superconducting $\Delta\Sigma$ modulators. The fastest decimator reported to date [171] was designed for a baseband ADC and operated at 19.6 GHz, less than half the maximum sampling rate of the modulator demonstrated in this project. In general, the bandpass $\Delta\Sigma$ modulator requires a decimator which is more complex than the low-pass decimators demonstrated to date in RSFQ logic, though the difference in complexity can be small if the modulator center frequency is a simple fraction (e.g., 1/4 or 1/8)

of the sampling rate [169]. Unfortunately, the relationship between the center frequency and sampling rate could not be set precisely in the present experiment. The pulse rate of the optical clock source described in Chapter 5 is fixed and precise, but the modulator center frequency depends on the parameters of the microstrip line resonator, some of which are not accurately known. A particularly important source of uncertainty is the effective dielectric constant of the microstrip line. Since inductances are more important than capacitances in Josephson technology, dielectric constants are not accurately characterized in most Josephson integrated circuit processes [123, 172]. A bandpass decimator with a center frequency which could be changed to an arbitrary fraction of the sampling rate would likely be too complex for implementation in current Josephson technology. Another disadvantage of using a decimator is that the output spectrum of the modulator can only be observed inside the band of interest, precluding examination of spectral features outside the band of interest (such as idle tones or quantization noise minima due to aliased modes) which may provide valuable insight into modulator operation.

Another approach to interfacing is to capture the modulator output data with an on-chip acquisition memory, which can be later uploaded to room-temperature electronics at low speed. Such an acquisition memory is usually built with shift registers [44]. Unfortunately, integration limits of current Josephson technology do not allow large on-chip memories. The longest superconducting shift register reported to date [41] is only 1024 bits long and employs counterflow clocking, in which the data and clock pulses travel in opposite directions. Shift registers with concurrent flow clocking, in which the data and clock pulses travel in the same direction, are more suitable for acquiring the modulator output data, as the output data and sampling clock pulses are created in the same physical area of the chip. Shift register cells which support concurrent flow clocking (such as that shown in Figure 8-2) use at least twice as many junctions per stored bit than do the two-junction cells used in the 1024-bit register cited above, so the acquisition memory for the modulator is limited to *at most* 512 bits. The test chip fabricated for this thesis project includes a 256-bit acquisition memory, which is a more practical choice for maintaining acceptable circuit yield.

Meaningful characterization of an oversampling ADC generally requires that the number of samples captured with the acquisition memory be substantially larger than the oversampling ratio (OSR). A 256-bit acquisition memory does not meet this requirement for the superconducting modulator studied here. If, for instance, the sampling rate is 20 GHz, and the signal bandwidth is 39 MHz, the OSR is 256, and a 256-bit sequence corresponds to only one point of output data at the Nyquist rate. For higher sampling rates or lower bandwidths, the OSR is even larger, and a 256-bit sequence corresponds to less than one point of output data at the Nyquist rate. If output spectra are calculated by taking 256-point FFTs of the captured sequences, the frequency resolution is broader than the signal bandwidth and too coarse for accurate measurement of in-band noise.

This chapter explains how segmented correlation can be used to estimate the output spectrum of an ADC with fine frequency resolution, even when the data record lengths are limited by small acquisition memories. The basic concept of segmented correlation is presented in the next section. The remainder of the chapter examines the accuracy of the spectral estimation and discusses some practical details of using the technique, which is applicable to a wide range of ADCs.

9.2 Basic Concept

The concept of segmented correlation is based upon the following observation. Mathematically, the power spectrum is the Fourier transform of the autocorrelation function $R[n]$ of the output data [1]. Therefore, estimating the power spectrum with fine frequency resolution is equivalent to estimating $R[n]$ up to a large value of n. (Estimating $R[n]$ for negative values of n need not be addressed directly since $R[n]$ is an even function.) If a single L-point segment of the output data stream is captured with a shift register memory bank, $R[n]$ can be estimated only for values of n up to $(L-1)$. On the other hand, if two segments of the output data stream are captured with a pair of shift register memory banks, as illustrated in Figure 9-1, $R[n]$ can be estimated for values of n much larger than the lengths of the individual shift registers. In the figure, L is the length of each captured segment and is typically less than the OSR; M is the number of ADC output samples skipped between acquiring the A and B segments and is set by an on-chip programmable counter from 0 to N. Since counting times grow exponentially with the number of counter stages, N may be much larger than the OSR. Cross-correlation between the A and B segments generates estimates of $R[n]$ for values of n between $(M+1)$ and $(M+2L-1)$ – a relatively narrow range as L is not large. By reprogramming the value of M (from 0 to N), different sections of $R[n]$ can be estimated through successive measurements, after which an estimate for the entire function $R[n]$ (from $n=0$ up to $n=N+2L-1\approx N$) can be assembled. Fourier transformation of the assembled estimate then yields a power spectrum with frequency resolution comparable to an N-point FFT. An advantage of the technique over using an on-chip decimator is that the entire output spectrum (from dc to half the clock rate) can be observed.

A precise mathematical description of the cross-correlation suggested in Figure 9-1 clarifies the key concepts. Let $y[i]$ be the sequence of ADC output samples, with the index i defined so that $y[0]$ corresponds to the first sample captured in shift register memory bank A. Then cross-correlation of the A and B segments yields an estimate of the autocorrelation function given by

$$\hat{R}_M[n] = \begin{cases} \frac{1}{L}\sum_{i=M+L-n}^{L-1} y[i]y[i+n], & \\ \qquad\qquad M+1 \le n \le M+L, & \\ \frac{1}{L}\sum_{i=0}^{M+2L-1-n} y[i]y[i+n], & \\ \qquad\qquad M+L < n \le M+2L-1, & \\ 0 \qquad\qquad \text{otherwise.} & \end{cases} \tag{9.1}$$

Since $R[n] = E\{y[i]y[i+n]\}$ (by definition), the expected value of the estimate is

$$E\{\hat{R}_M[n]\} = w_M[n]R[n], \tag{9.2}$$

where

$$w_M[n] = \begin{cases} \frac{L-|n-M-L|}{L}, & M+1 \le n \le M+2L-1, \\ 0 \qquad\qquad & \text{otherwise.} \end{cases} \tag{9.3}$$

Except for $n=M+L$, $w_M[n]<1$, and therefore $\hat{R}_M[n]$ is a biased estimate of $R[n]$. (This bias arises because fewer terms in the cross-correlation contribute to $\hat{R}_M[n]$ for n farther from $M+L$.)

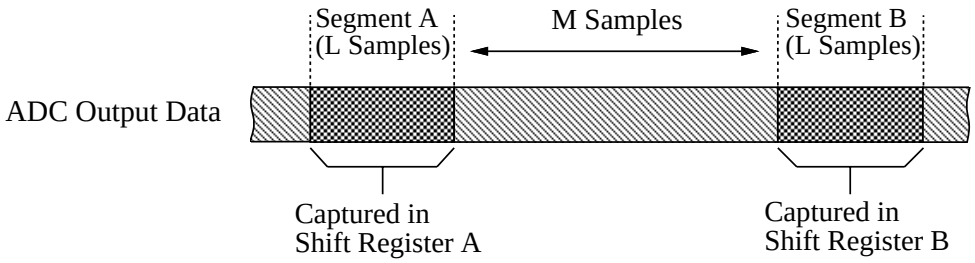


Figure 9-1: Segmented correlation technique. Cross-correlation of the data segments captured in the A and B shift register memory banks generates estimates of $R[n]$ for values of n much larger than the shift register lengths if $M \gg L$.

Since the value of M is programmable, an ensemble of estimates $\hat{R}_M[n]$ can be produced through successive measurements. While each estimate $\hat{R}_M[n]$ has a bias given by Equations 9.2 and 9.3, an unbiased estimate of $R[n]$ can be obtained by adding the various estimates together in such a way that their biases cancel out. As an example, consider adding together four estimates, denoted by $\hat{R}_{auto}[n]$, $\hat{R}_0[n]$, $\hat{R}_L[n]$, and $\hat{R}_{2L}[n]$. $\hat{R}_{auto}[n]$ is obtained by correlating segment A with itself (autocorrelation), while the other estimates are cross-correlations given by Equation 9.1 for $M = 0, L, 2L$. For non-negative n, the expected value of $\hat{R}_{auto}[n]$ is given by [1]

$$E\{\hat{R}_{auto}[n]\} = w_{auto}[n]R[n], \tag{9.4}$$

where

$$w_{auto}[n] = \begin{cases} \frac{L-n}{L}, & 0 \le n \le L-1, \\ 0 & \text{otherwise.} \end{cases} \tag{9.5}$$

Letting $\hat{R}[n]$ be the sum of the four estimates,

$$E\{\hat{R}[n]\} = (w_{auto}[n] + w_0[n] + w_L[n] + w_{2L}[n])R[n]. \tag{9.6}$$

As shown graphically in Figure 9-2, $\hat{R}[n]$ is an unbiased estimate of $R[n]$ for $0 \le n \le 3L$. By adding estimates corresponding to $M = 3L, 4L, \ldots$, unbiased estimates of $R[n]$ can be acquired over a larger range of n, ultimately up to $n = N + L \approx N$. As shown in the next section, Fourier transformation of this unbiased estimate yields an unbiased estimate of the power spectrum. The frequency resolution of the spectral estimate is fine enough for evaluating oversampling converters if $N \gg$ OSR.

More generally, each segmented correlation estimate $\hat{R}_M[n]$ can be multiplied by a weighting function (or window) $G_M[n]$ before the various segmented correlation estimates are added together. Letting $\widetilde{R}_M[n]$ be

$$\widetilde{R}_M[n] = G_M[n]\hat{R}_M[n], \tag{9.7}$$

the expected value of the weighted segmented correlation estimate is

$$E\{\widetilde{R}_M[n]\} = \widetilde{w}_M[n]R[n], \tag{9.8}$$

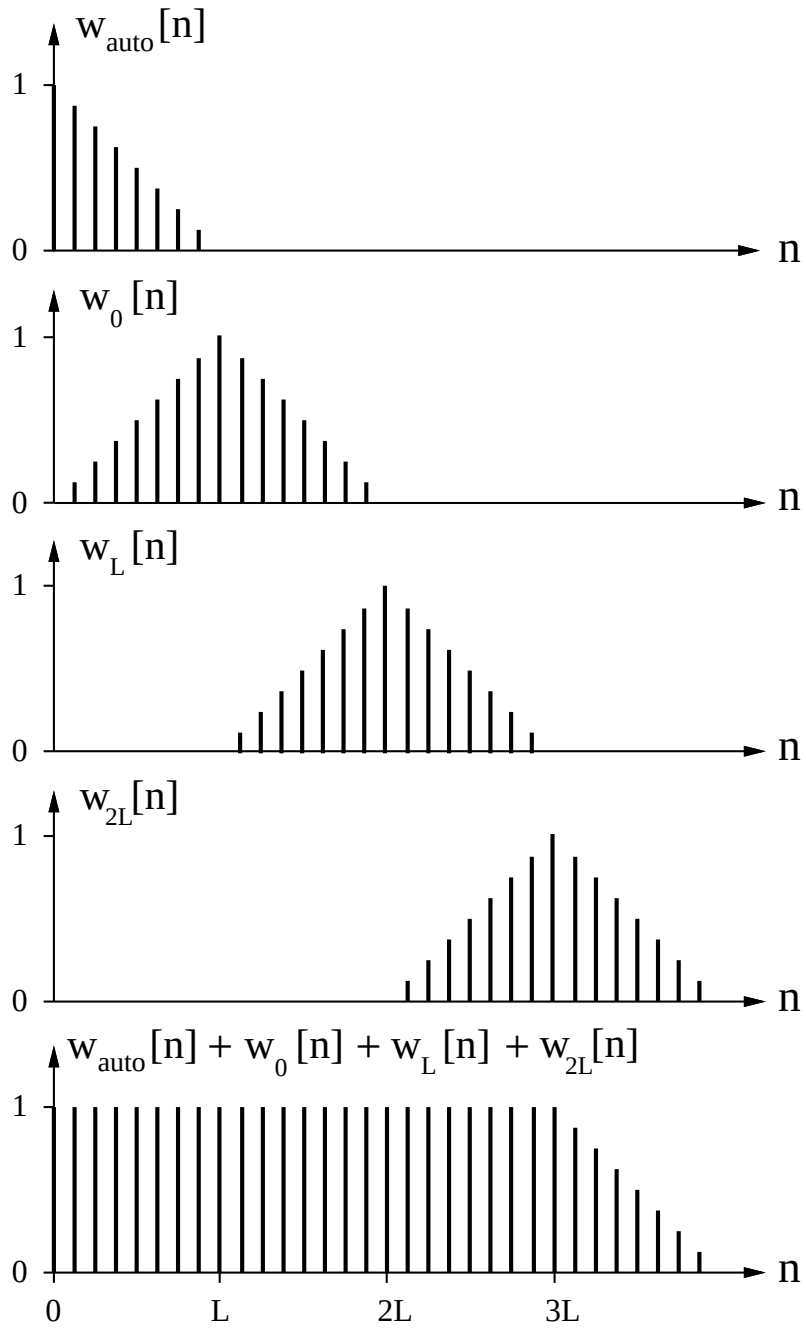


Figure 9-2: Obtaining an unbiased estimate of $R[n]$. Even though each segmented correlation estimate is biased according to Equations 9.2–9.5, a proper combination of estimates cancels out their biases over a wide range of n (bottom graph).

where

$$\widetilde{w}_M[n] = G_M[n]w_M[n]. \tag{9.9}$$

Similarly, $\widetilde{R}_{auto}[n]$ is defined to be the weighted estimate

$$\widetilde{R}_{auto}[n] = G_{auto}[n]\hat{R}_{auto}[n], \tag{9.10}$$

with expected value

$$E\{\widetilde{R}_{auto}[n]\} = \widetilde{w}_{auto}[n]R[n], \tag{9.11}$$

where

$$\widetilde{w}_{auto}[n] = G_{auto}[n]w_{auto}[n]. \tag{9.12}$$

To achieve an unbiased estimate of $R[n]$, the weighting functions $G_{auto}[n]$ and $G_M[n]$ should be chosen so that the biases given by Equations 9.8, 9.9, 9.11, and 9.12 cancel out when the weighted segmented correlation estimates are added together. As an example, consider the weighting functions given by

$$G_{auto}[n] = \begin{cases} \frac{L}{L-n}\cos^2\left(\frac{\pi n}{2L}\right), & 0 \le n \le L-1, \\ 0 & \text{otherwise,} \end{cases} \tag{9.13}$$

and

$$G_M[n] = \begin{cases} \frac{L}{L-|n-M-L|}\cos^2\left[\frac{\pi(n-M-L)}{2L}\right], & M+1 \le n \le M+2L-1, \\ 0 & \text{otherwise.} \end{cases} \tag{9.14}$$

It then follows from Equations 9.3, 9.5, 9.9, and 9.12 that

$$\widetilde{w}_{auto}[n] = \begin{cases} \cos^2\left(\frac{\pi n}{2L}\right), & 0 \le n \le L-1, \\ 0 & \text{otherwise,} \end{cases} \tag{9.15}$$

and

$$\widetilde{w}_M[n] = \begin{cases} \cos^2\left[\frac{\pi(n-M-L)}{2L}\right], & M+1 \le n \le M+2L-1, \\ 0 & \text{otherwise.} \end{cases} \tag{9.16}$$

Now consider adding together estimates $\widetilde{R}_{auto}[n]$, $\widetilde{R}_0[n]$, $\widetilde{R}_L[n]$, $\widetilde{R}_{2L}[n]$, etc. As shown graphically in Figure 9-3, this combination of estimates cancels out the sinusoidally weighted biases given by Equations 9.15 and 9.16 over a wide range of n.

The advantage of using weighting functions with tapered ends (such as the sinusoidal ones just considered) is that the segmented correlation estimates $\widetilde{R}_M[n]$ are weighted relatively little at values of n far from $M+L$, where few terms in the cross-correlation contribute to the estimate, and the estimate is noisy (with a large variance). For a given amount of measurement data, the noise in the assembled estimate is reduced. The sinusoidal weighting functions given by Equations 9.13 and 9.14 are used in Chapter 12 to analyze the performance of the experimental modulator with the segmented correlation technique. Undoubtedly, other weighting functions could be chosen, with the constraint that the biases of the weighted segmented correlation estimates cancel out when added together, as illustrated in Figure 9-3. Finding the optimum weighting function for the segmented correlation estimates may be a valuable topic for future research.

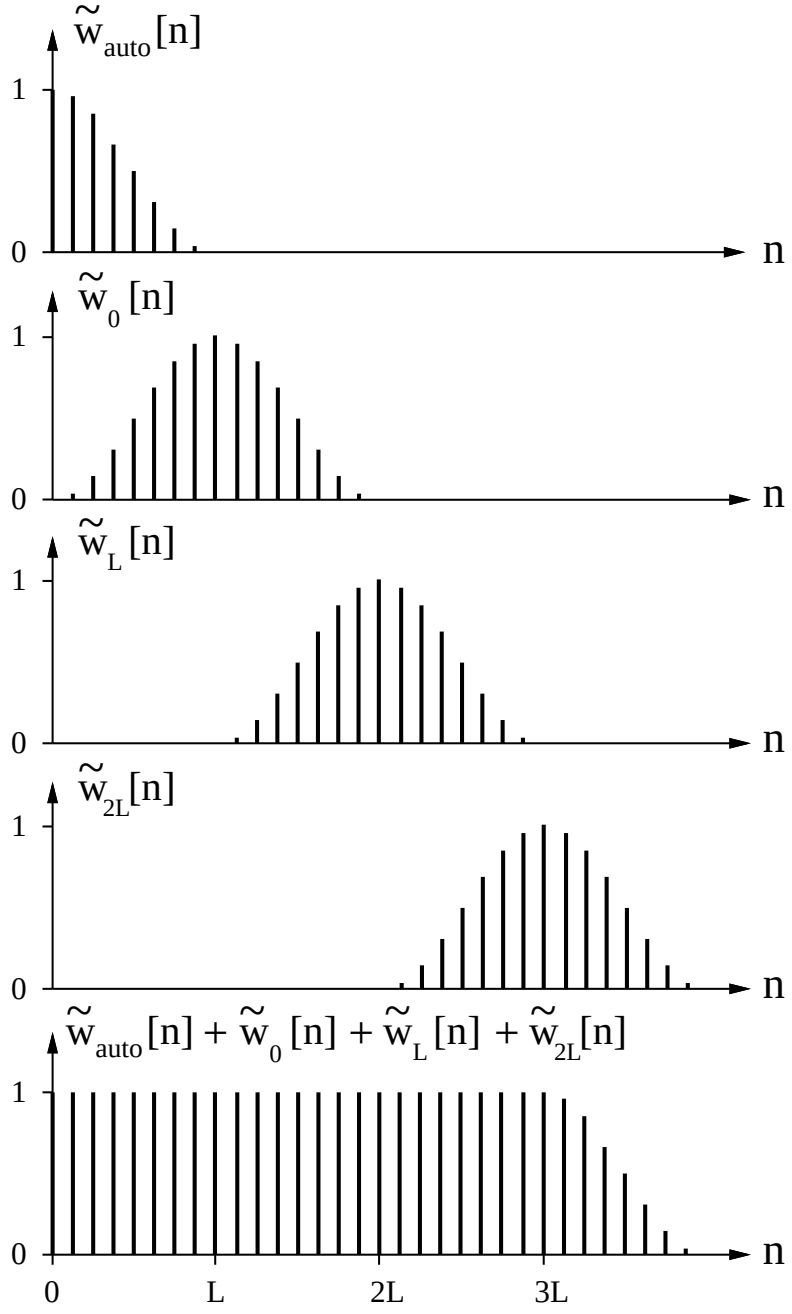


Figure 9-3: Alternative choice for cancellation of bias. Combining segmented correlation estimates with sinusoidally weighted biases yields an unbiased estimate of $R[n]$ over a wide range of n (bottom graph).

9.3 Accuracy of Spectral Estimation

Consider the spectral estimate

$$\hat{S}(e^{j\Omega}) = \sum_{n=-N}^{N} c_w[n]\hat{R}[n]e^{-j\Omega n}, \tag{9.17}$$

where $c_w[n]$ is a symmetric $(2N+1)$-point window, $\hat{R}[n]$ is the sum of segmented correlation estimates just discussed (with or without weighting functions), and $\Omega = \omega T$. Since $\hat{R}[n]$ and $c_w[n]$ are even functions, $\hat{S}(e^{j\Omega})$ will be real and even. The accuracy of this spectral estimate is evaluated by calculating its expected value and variance. Since the expectation operator is linear,

$$E\{\hat{S}(e^{j\Omega})\} = \sum_{n=-N}^{N} c_w[n]E\{\hat{R}[n]\}e^{-j\Omega n}. \tag{9.18}$$

With a proper combination of segmented correlation estimates, $E\{\hat{R}[n]\} = R[n]$ over the range of the summation, so

$$E\{\hat{S}(e^{j\Omega})\} = \sum_{n=-N}^{N} c_w[n]R[n]e^{-j\Omega n} \tag{9.19}$$

Thus, the expected value of $\hat{S}(e^{j\Omega})$ equals the Fourier transform of the actual autocorrelation function (windowed by $c_w[n]$). Provided that $c_w[n]$ is chosen suitably, the spectral estimate is unbiased[1].

Calculation of the variance of $\hat{S}(e^{j\Omega})$ is more difficult and is reserved for Appendix D. There it is shown that

$$\mathrm{var}[\hat{S}(e^{j\Omega})] \approx \frac{2N}{KL}(S_L(e^{j\Omega}))^2, \tag{9.20}$$

where K is the number of segmented cross-correlations averaged to form each estimate $\hat{R}_M[n]$ (using data from K successive measurements), and $S_L(e^{j\Omega})$ is a "smeared" version of the true power spectrum $S(e^{j\Omega})$, with frequency resolution approximately that of an L-point FFT. The distinction between $S(e^{j\Omega})$ and $S_L(e^{j\Omega})$ is particularly important if the ADC being tested is a $\Delta\Sigma$ modulator which employs quantization noise shaping. For instance, consider a bandpass $\Delta\Sigma$ modulator with a center frequency of Ω_c. As illustrated in Figure 9-4, the true output noise spectrum $S(e^{j\Omega})$ exhibits a deep null for frequencies near Ω_c, but the depth of the null is diminished for the smeared spectrum $S_L(e^{j\Omega})$. Over this frequency range, the relatively large value of $S_L(e^{j\Omega})$ increases the variance of the spectral estimate $\hat{S}(e^{j\Omega})$, necessitating a larger value of K (and longer measurement time). For this reason, L should not be much smaller than the OSR.

For the spectral estimate $\hat{S}(e^{j\Omega})$ to be useful, its variance should be no greater than $(S(e^{j\Omega}))^2$, the spectrum to be estimated. Setting the variance given by Equation 9.20 equal to $(S(e^{j\Omega}))^2$, the number of averages K needed to obtain an accurate spectral estimate is

[1]More precisely, the spectral estimate is *asymptotically* unbiased. Any spectral estimate with finite frequency resolution (including a standard FFT) is biased in the sense that its expected value equals a smoothed version of the true power spectrum. A spectral estimate is asymptotically unbiased if its bias approaches zero as the frequency resolution is increased [1].

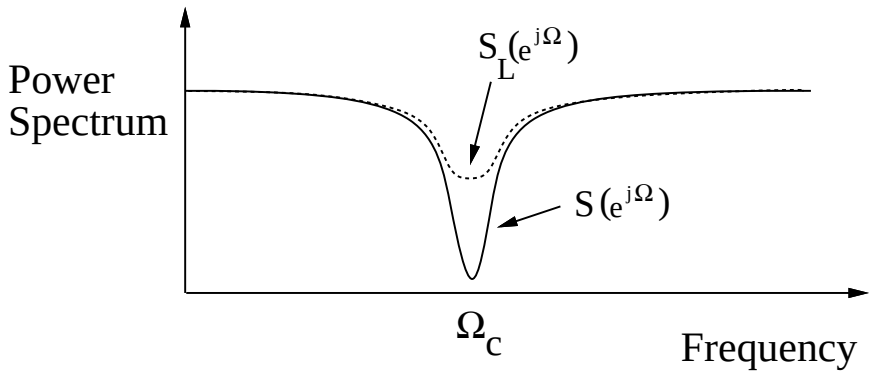


Figure 9-4: Comparison of $S(e^{j\Omega})$ and $S_L(e^{j\Omega})$ for a bandpass $\Delta\Sigma$ modulator with center frequency Ω_c.

found to be

$$K = \frac{2N}{L} \max \left(\frac{S_L(e^{j\Omega})}{S(e^{j\Omega})} \right)^2 . \tag{9.21}$$

Note that Ω in Equation 9.21 is evaluated at the frequency for which the ratio $S_L(e^{j\Omega})/S(e^{j\Omega})$ is maximized – for instance, at $\Omega = \Omega_c$ in Figure 9-4. The total number N_S of segmented cross-correlations to be calculated equals K times the number of $\hat{R}_M[n]$ (or $\widetilde{R}_M[n]$ if weighting is used) summed together to form $\hat{R}[n]$, which is approximately N/L if one of the schemes suggested in Figures 9-2 and 9-3 is used; therefore $N_S = KN/L$. The total measurement time T_M is obtained by multiplying N_S by the time it takes to calculate a single segmented cross-correlation.

For typical values of L and N, the time necessary to calculate a single segmented cross-correlation is limited by the need to wait up to N clock cycles between loading shift register memory banks A and B, *not* the time needed to read out the memory banks to room-temperature electronics. As an example, consider a $\Delta\Sigma$ modulator generating 1-bit outputs at a clock rate of 20 GHz. If $M = N = 8192$ and $L = 128$, it takes approximately 0.4 μs to load the A and B shift register memory banks with a total of 256 bits. In order to unload the bits as fast as they are loaded, the readout rate off the chip must equal 256 bits/(0.4 μs)=640 Mbit/s. Such a data rate is almost four times lower than the readout rate of the decimator reported in [34] and can be accommodated by most interfaces.

Consequently, the total measurement time T_M is

$$T_M = N_S \frac{N}{f_s} = \frac{KN^2}{f_s L} = \frac{2N^3}{f_s L^2} \max \left(\frac{S_L(e^{j\Omega})}{S(e^{j\Omega})} \right)^2 . \tag{9.22}$$

To illustrate the dependence of T_M on N and L, the measurement times for the superconducting modulator studied in this thesis project are presented in Table 9.1. The sampling rate f_s is assumed to be 20 GHz. The ratio $S_L(e^{j\Omega})/S(e^{j\Omega})$ at the modulator center frequency Ω_c is computed for $L = 128$ and $L = 64$ from the circuit simulation data discussed in the last chapter and is listed in the fourth column of the table. Case 1 shows that a power spectrum with the frequency resolution of an 8192-point FFT can be obtained after only 11 seconds of acquiring data. Since T_M is proportional to N^3, increasing N dramat-

Table 9.1: Measurement times for the superconducting bandpass $\Delta\Sigma$ modulator at a sampling rate of 20 GHz.

Case	N	L	$\frac{S_L(e^{j\Omega_c})}{S(e^{j\Omega_c})}$	T_M (seconds)
1	8192	128	57.5	11
2	16384	128	57.5	89
3	32768	128	57.5	710
4	8192	64	120.2	194
5	32768	64	120.2	12411

ically lengthens measurement times (cases 2 and 3). Even for $N = 32768$, however, the measurement time is not excessive (less than 12 minutes). The dependence of T_M on L is even stronger. Reducing L from 128 to 64 multiplies measurement times by more than 17 (cases 4 and 5). (The larger value of $S_L(e^{j\Omega_c})/S(e^{j\Omega_c})$ is a major factor here.) For large values of N and small values of L, measurement times become very long (over 3.4 hours for case 5).

For most of the cases listed in Table 9.1, the amount of data acquired during the measurement is substantially more than 1 Gbyte, and calculating the cross-correlations on a general-purpose computer would be very time-consuming. Fortunately, though, correlation is a common operation in signal processing, and special-purpose correlation hardware is available. For example, a correlator board designed for radio astronomy is described in [173]. This correlator board uses 32 custom CMOS correlator chips to achieve a computation rate in excess of 10^{12} operations per second. Such hardware would be able to calculate the cross-correlations in "real-time" – as fast as the data can be read out of shift register memory banks A and B.

The measurement times listed in Table 9.1 were calculated under the assumption that the shift register memory banks are unloaded as fast as they can be loaded (with $M = N$). Even though such a readout rate can be accommodated by most interfaces, a lower readout rate is sometimes advantageous. The modulator test chip described in the next chapter employs a readout rate one-fourth of that assumed in the table above. This lower readout rate allows simpler timing circuitry to synchronize loading and unloading of the shift register memory banks. The reduced bandwidth requirements for readout also allow the outputs of the chip to be amplified by room-temperature electronics with less noise. The penalty paid for these advantages is a measurement time four times longer than that given by Equation 9.22. Even with this penalty, the measurement time of the modulator test chip (with $N = 8060$ and $L = 128$) is less than 1 minute at a sampling rate of 20 GHz (cf. case 1 in Table 9.1).

9.4 Summary

This chapter has described an ADC testing method based on segmented correlation which yields high resolution estimates of the output spectrum, even when data record lengths are limited by small on-chip memories. Cross-correlation of two short segments of the output data stream provides an estimate of the autocorrelation function $R[n]$, over a narrow range

of n. Other sections of $R[n]$ are estimated by reprogramming a counter so that a different number of ADC output samples are skipped between acquiring the two segments. These segmented correlation estimates are then combined to generate an unbiased estimate of $R[n]$ over a range of n much larger than the segment lengths. Fourier transformation of this unbiased estimate yields an unbiased estimate of the output spectrum, with frequency resolution fine enough for studying oversampling converters. Since the entire spectrum (from dc to half the clock rate) is estimated, a wide range of ADCs, including low-pass and bandpass $\Delta\Sigma$ modulators, can be studied with the method. In order to reduce the variance of the spectral estimate, the cross-correlations are averaged, and typical measurement times range from several seconds to several minutes. The next chapter presents the design of a test chip for evaluating the superconducting bandpass $\Delta\Sigma$ modulator by segmented correlation.

Chapter 10

Modulator Test Chip

This chapter presents the design of a test chip for experimental evaluation of the superconducting bandpass $\Delta\Sigma$ modulator. The design allows multi-GHz testing of the bandpass modulator with only modest bandwidth requirements on the electrical interface to room-temperature electronics. An optoelectronic interface with integrated MSM photodiode allows optical clocking of the modulator at a sampling rate of 20.6 GHz. An on-chip Josephson clock source permits sampling at even higher frequencies (up to 45 GHz). The chip includes a 256-bit acquisition memory to capture the high speed output of the modulator and contains the timing circuitry required for segmented correlation measurements.

The first section of the chapter presents the test chip architecture and explains the functions of the main digital circuit blocks. Key implementation details of these circuit blocks are described in later sections. The test chip is designed for the standard HYPRES niobium process with 1 kA/cm^2 critical current density [123].

10.1 Architecture

The architecture of the modulator test chip is illustrated in Figure 10-1. The MSM photodiode which converts the picosecond optical pulses into fast electrical pulses is identical to the one used in the experiments on optically clocked Josephson circuits discussed in Chapter 6. The layout of the optoelectronic interface is similar to that shown in Figure 6-2 and incorporates the transmission line termination techniques whose effectiveness was demonstrated in the optoelectronic sampling experiments of Chapter 4. The current pulses from the MSM photodiode are converted into SFQ clock pulses by the SFQ pulse generator used in the optically triggered JTL experiment (Figure 6-7). A clock amplifier in the form of a thirteen-stage JTL amplifier provides the current gain needed to drive the SFQ comparator of the modulator with a low impedance. Alternatively, the bandpass modulator can be triggered by an on-chip oscillator. If the dc bias current through the junction of the SFQ pulse generator (J_1 in Figure 6-7) is increased about its critical current, the junction spontaneously generates SFQ pulses which are picked up by the JTL amplifier and transferred to the bandpass modulator. While the frequency stability and jitter of this on-chip oscillator are inferior to those of the optical source, its frequency can be varied between 20 and 45 GHz by simple adjustment of dc bias currents. Such tunability is useful for studying modulator operation at different sampling rates. With both optical clocking and on-chip

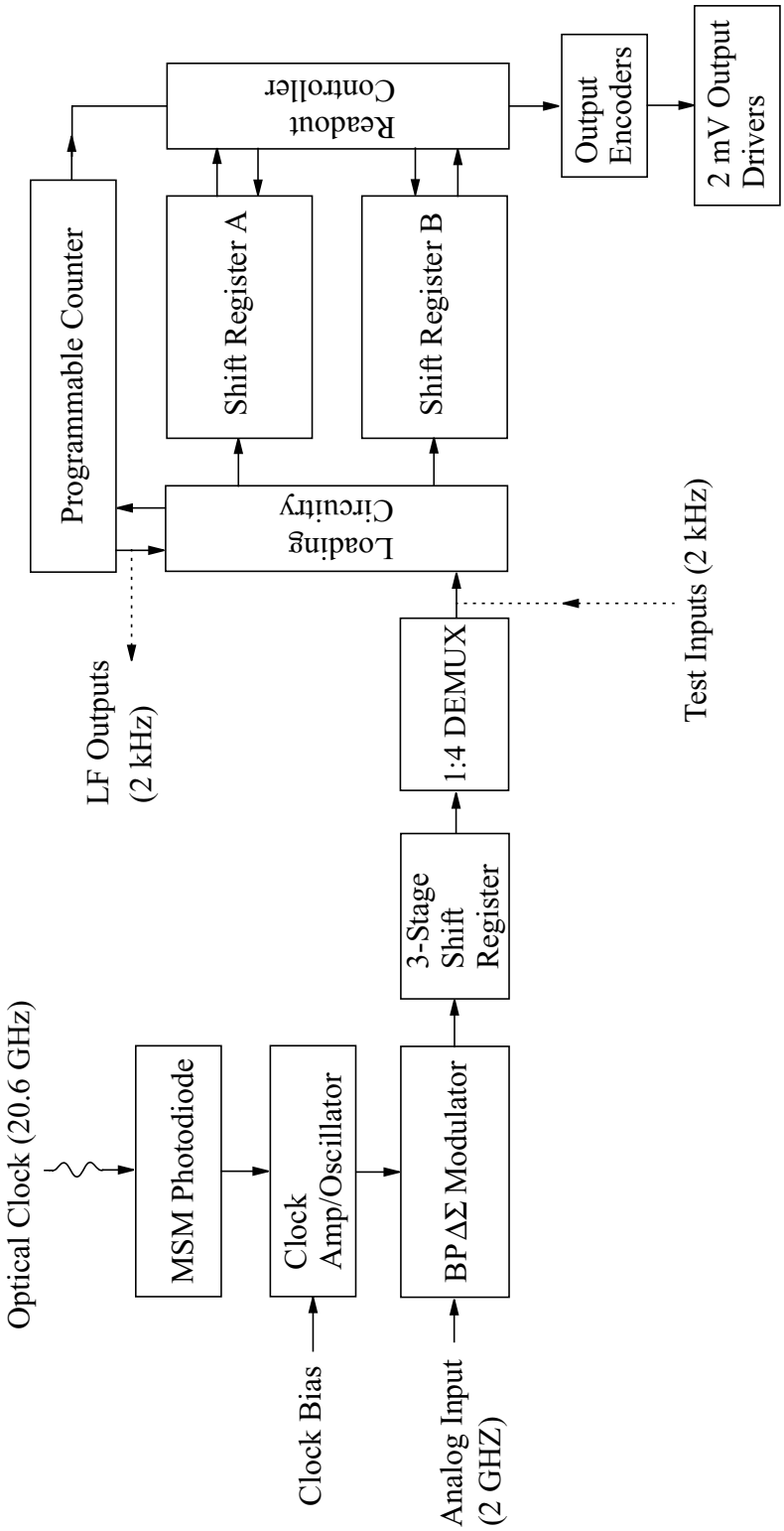


Figure 10-1: Test chip block diagram.

clock generation, the high speed clock is not delivered over an electrical cable to the test chip, so crosstalk between clock and signal lines is virtually eliminated.

The analog input (near 2 GHz) is delivered to the test chip electrically over the coaxial cable of the sample holder. As explained in Section 7.2.4, the input coupling network of the experimental modulator includes a 6 dB resistive attenuator in order to reduce the sensitivity of the modulator to noise from room-temperature instruments. The single-bit output of the modulator is fed through a three-stage shift register before being converted to 4-bit words at one-fourth the sampling rate by a 1:4 demultiplexer (DEMUX). Each of the three shift register stages is identical to the cell shown in Figure 8-2. The function of the three-stage shift register is similar to the "conditioner" described in [68]. Because of metastability in the SFQ comparator, some of the SFQ data pulses produced by the modulator may be delayed relative to the sampling clock. Retiming these pulses three times with a short shift register ensures (with a very high probability) that they are properly synchronized with the clock pulses before entering the DEMUX. The use of a 1:4 DEMUX is a major factor behind the success of this project in demonstrating sampling rates as high as 45 GHz, as it allows the largest digital circuits (the shift register memory banks and the programmable counter) of the test chip to operate at a reduced clock rate ($f_s/4$), where timing margins are larger.

The 4-bit wide output of the DEMUX is loaded into shift register memory banks A and B, under the control of a programmable counter. Each 128-bit memory bank is organized as four rows of 32-bit shift registers. The number of bits skipped for segmented correlation measurements is set by programming the counter with 11 external control currents. After loading is completed, a readout controller unloads the captured data and transfers them to the serial outputs of the chip, in exactly the same bit order as originally generated by the bandpass modulator. The programmable counter generates timing signals for the readout controller so that proper synchronization between loading and unloading is maintained. As explained later in the chapter, the output signals from the chip are encoded for good dc balance so that they can be detected with ac-coupled amplifiers, which are cheaper and less sensitive to power-line interference [174] than dc-coupled amplifiers. The voltages generated by typical RSFQ logic circuits are too small to be detected at high bit rates with room-temperature electronics. The test chip therefore includes output drivers which boost the output swing to 2 mV, which is large enough to be amplified with negligible noise by wideband (GHz) room-temperature amplifiers.

Because the yield of a circuit as complex as the modulator test chip is low in current Josephson technology, several chips must usually be screened for functionality before finding one suitable for a high frequency test of the bandpass modulator. Diagnostic inputs and outputs, shown as dotted lines in Figure 10-1, are used to test the functionality and operating margins of the large digital circuits on the chip at low frequency (e.g., 2 kHz). The test inputs drive standard DC/SFQ converters [31], whose SFQ output pulses are inserted onto the data and clock lines through confluence buffers (reviewed in Section 2.2.6). Only digital circuits downstream of this insertion point can be tested for functionality at low frequency. Digital circuits such as the 1:4 DEMUX and the three-stage shift register preceding it are not exercised during low frequency testing and are ignored in screening chips for functionality. Fortunately, these circuits are only a small fraction of the total circuitry on the chip, so if the rest of the chip works correctly, there is a good chance that these circuits are also functional. Ultimately, the functionality of these circuits is verified

by examining the measured performance of the bandpass modulator during high frequency testing. Since a problem in one of these digital circuits would corrupt the modulator output data, good ADC performance indicates that the circuits are working correctly. The low frequency (LF) diagnostic outputs of the chip are used to monitor the signals (generated by the programmable counter) that control loading of shift register memory banks A and B. These outputs are generated with standard SFQ/DC converters [31], so their output swing is only 100-200 μV. Such output levels are too small to be useful during high speed testing but are large enough to be detected reliably at low speed by audio-frequency (kHz) room-temperature electronics. Both these outputs and the "high voltage" (2 mV) outputs are used during low frequency testing of the chips for functionality.

The precise synchronization between loading and unloading of the shift register memory banks is illustrated in the timing diagrams of Figure 10-2. M, the number of data bits skipped between loading of shift register memory banks A and B, equals 0 in Figure 10-2(a) and 8060 in Figure 10-2(b). The first two signals in each timing diagram represent the outputs generated by the high voltage output drivers of the chip. The data segments captured with the integrated acquisition memory are read out serially over the DATA output at a bit rate of $f_s/128$. The time required to unload all 256 bits stored in shift register memory banks A and B equals 32768 periods of the sampling clock. The other high voltage output is the START bit, which is a framing signal marking the first of 128 bits being unloaded from shift register memory bank A. Such a framing signal is required for proper interpretation of the DATA output since there is no break in the data stream between unloading memory banks A and B. The LOADA and LOADB pulses are generated by the programmable counter and trigger loading of shift register memory banks A and B, respectively. These are the signals monitored by the low frequency diagnostic outputs mentioned in the previous paragraph. If $M = 0$ (Figure 10-2(a)), the LOADA pulses are immediately followed by the LOADB pulses, so 256 consecutive bits from the bandpass modulator are captured in shift register memory banks A and B. If $M = 8060$ (Figure 10-2(b)), extra delay is added to the LOADB pulses so that 8060 data bits are skipped between loading shift register memory banks A and B. As demonstrated later in the chapter, the design of the programmable counter allows M to be varied from 0 to 8060, in increments of 4. For all such values of M, shift register memory bank A is loaded while shift register memory bank B is being unloaded, and vice versa. This "ping-pong" arrangement allows the DATA signal to be read out without interruption.

10.2 Circuit Implementation

10.2.1 Design Strategy

The modulator test chip implemented in this thesis project employs 4065 Josephson junctions and is one of the most complex RSFQ circuits ever demonstrated. (For sake of comparison, the largest fully functional RSFQ circuit reported to date is a baseband ADC with on-chip decimator employing about 6000 Josephson junctions [171].) A conservative design strategy contributed to successful operation of this complex chip after only one design cycle. With only one exception [1], the logic design of each digital circuit block was chosen to use

[1]The logic of the programmable counter requires a single-pole double-throw SFQ switch controlled by a single external dc current. The design of such a switch, which has not been reported by other researchers,

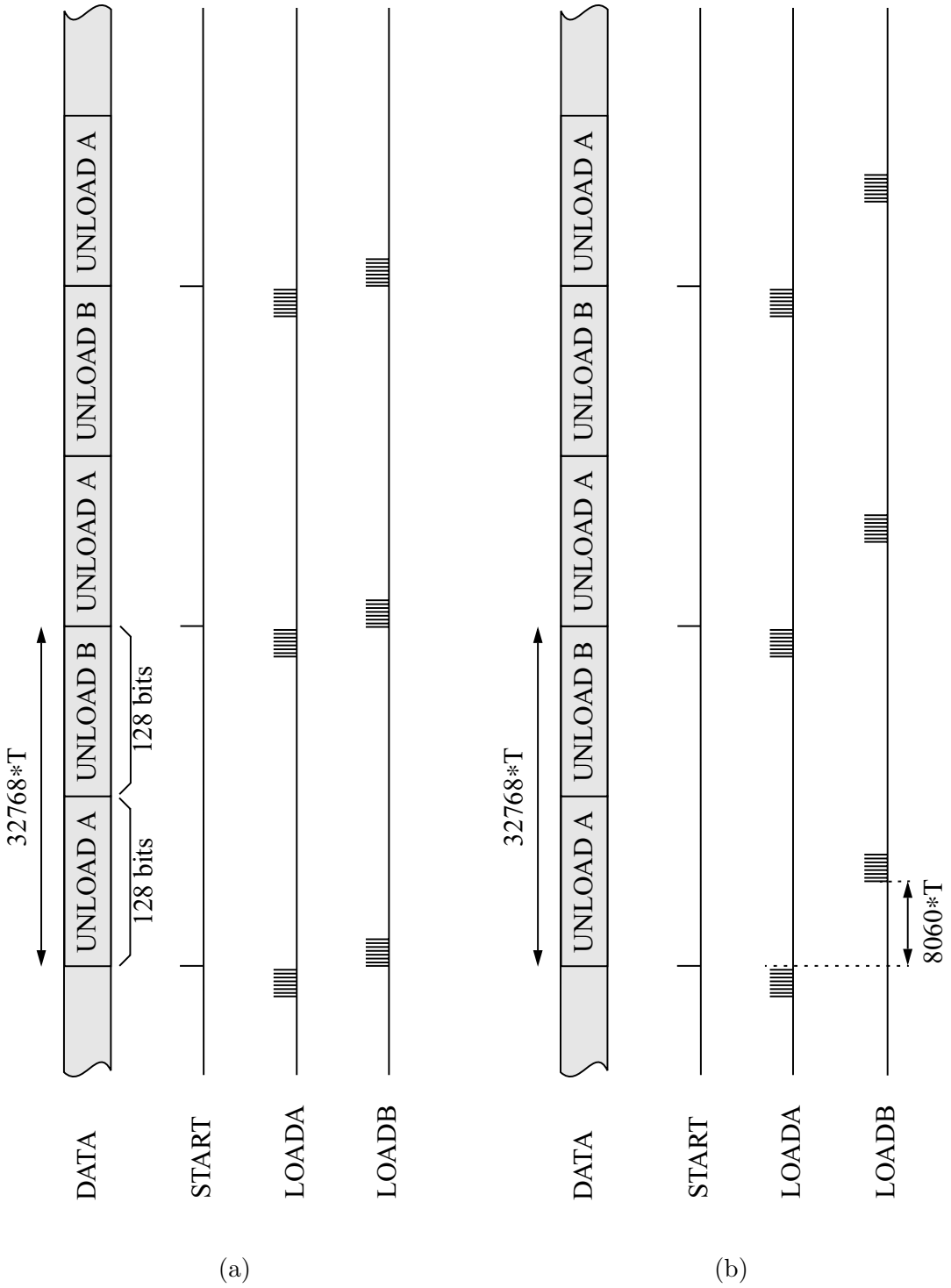


Figure 10-2: Timing diagrams for loading and unloading shift register banks A and B. (a) $M = 0$. (b) $M = 8060$.

only RSFQ cells which had been shown (in either published literature or unpublished technical reports) to have large experimental operating margins. The test chip design does not include any register cells with nondestructive readout (NDRO). While versatile in terms of functionality, NDRO cells are more complex and have smaller operating margins [31, 121] than destructive readout (DRO) circuits such as the D latch reviewed in Section 2.2.8. For all of the RSFQ cells used in the test chip design, the smallest (simulated) margin for a junction critical current is at least 30%. For most cells, the smallest critical current margin is in the range of 35-40%.

The design effort was reduced significantly by incorporating RSFQ circuit layouts that were generously donated by Semenov at the State University of New York (SUNY) Stony Brook, and by several researchers at HYPRES, Inc. The use of these layouts also increased the probability of success since they had all been previously fabricated and experimentally verified. Some of these designs, such as the high voltage (2 mV) output drivers and the shift register cells used in memory banks A and B, were used with little or no modification. Most circuits, though, were moderately altered for their specific roles in the test chip. Circuit cells donated by multiple designers are often incompatible in terms of power supply voltages, impedance levels, and layout dimensions. In many cases, circuit cells donated by one designer had to be redesigned in the "style" of another. Circuits were also redesigned for specific load conditions. (As mentioned in previous chapters, the relative lack of isolation in Josephson circuits makes them particularly sensitive to loading.)

Even when donated circuit cells were used without modification, their parameters were extracted from the layouts so that their operation within larger circuit structures could be simulated. Such simulations are particularly important for studying race conditions and other timing issues that affect operation of the large digital circuit blocks. The only large digital circuit whose timing was not extensively studied in this manner is the readout controller. Since the output data rate of the chip is $f_s/128$, the operating frequency of the readout controller is only about 350 MHz at the maximum sampling rate (45 GHz) of the test chip, and Josephson circuit delays in the readout controller are negligible. Racing within the readout controller is avoided through the use of two-phase clocking [175, 73]. The readout controller is also the only circuit block designed with a standard cell approach [176], in which RSFQ gates from a library (in this case, the one developed at SUNY Stony Brook [121]) are treated as building blocks, connected together with two or more stages of JTL between inputs and outputs. Full custom design and layout were used for all other circuit blocks on the test chip because of their need to operate at multi-GHz frequencies.

The test chip employs as many separate power supplies as can be afforded with the wiring of the cryogenic sample holder: 22, not counting the bias voltage for the MSM photodiode or several offset currents used to adjust the operating points of individual analog and digital circuits. The different supply voltages used in circuit cells donated by different designers partly explain why so many independent sources are used, but there are more important reasons behind this choice. Since concurrent flow clocking is used in most of the digital circuits that operate at multi-GHz frequencies, many race conditions need to be satisfied for proper operation of the test chip. Conservative design practice ensures that most race conditions are reliably satisfied. The criterion adopted for this design is that the circuit delay encountered by the second pulse in a race should be at least twice the circuit

is detailed in Section 10.2.4.

delay encountered by the first pulse. In a few cases, however, such a conservative criterion is inconsistent with achieving the desired operating frequency. In these cases, independent power supplies are used to tune the delays of the JTLs along which the racing pulses propagate. Such use of tunable JTL delays for optimizing race conditions has been previously demonstrated [47]. More generally, adjustments of dc bias currents may be required to compensate for variations in process parameters (particularly, critical currents [176]) across the chip. A large number of independent supplies increases the chance that all of the circuits on the chip can be biased within their operating margins. Finally, separate supplies are used to power the bandpass modulator, the JTL amplifier for the sampling clock, and the three-stage shift register connected to the bandpass modulator so that noise from the large digital circuits of the test chip does not interfere with the more sensitive analog circuitry.

10.2.2 Design Tools

Suitable software tools are an absolute necessity for designing a superconducting integrated circuit as complex as the modulator test chip. Compared with their semiconductor counterparts, RSFQ logic circuits have relatively small parameter margins (e.g., 30-40% for junction critical currents). In order to achieve high performance and acceptable yield, circuits must be carefully optimized to have the highest possible simulated margins [158, 177]. The layout of each circuit cell must also be carefully executed so that parameters closely match those used in simulation. Even a 10% discrepancy in parameters may compromise the performance or robustness of a design. This section reviews the software tools that were used to design the test chip with the accuracy required for RSFQ logic.

In Chapter 8, the performance of the superconducting bandpass $\Delta\Sigma$ modulator was studied with JSIM circuit simulations. In principle, JSIM simulations can also be used to evaluate RSFQ logic circuits, but the circuit simulator PSCAN [178], developed at SUNY Stony Brook, has several features which make it more convenient for designing RSFQ logic circuits efficiently and reliably. The research group at SUNY Stony Brook has integrated PSCAN into a Cadence-based design environment, so that schematic entry with Cadence can be used to generate a PSCAN netlist automatically. In contrast, the manual generation of netlists for JSIM is cumbersome and error-prone with even medium-scale circuits. Perhaps the most valuable feature of PSCAN is a single flux quantum hardware description language (SFQHDL) that allows the circuit designer to specify the correct behavior of a circuit being simulated in terms of SFQ switching events. During a transient circuit simulation, a tool called the SFQHDL analyzer examines the waveform data (especially, junction phases) for consistency with the SFQHDL description in deciding if the circuit is operating correctly. Such automated waveform analysis is faster and more reliable than manual inspection and allows rapid calculation of circuit operating margins. In addition, PSCAN includes optimization algorithms which automatically vary specified parameters of the circuit in order to improve margins deemed to be unsatisfactorily low. Such automation of the circuit optimization process reduces the time required to design a basic RSFQ cell from several days to several hours [178].

After optimization of the schematic, a circuit layout is manually created with the layout editor in Cadence. The Josephson junctions themselves are usually selected from a library of junction layouts, which have been carefully designed according to known process characteristics (such as the relationship between drawn junction area and critical current [123]). This hierarchical approach decreases layout time and reduces opportunities for human error. The

Cadence customization performed by the group at SUNY Stony Brook supports automatic generation of bias resistors with a specific value, including the effects of contact resistance. The most crucial and time-consuming part of laying out RSFQ circuits is arranging the circuit elements and designing the interconnect so that the inductances match the parameters used in simulation. After a preliminary layout is created, all the inductances (including parasitics) are extracted from the layout with Lmeter [157], a two-dimensional inductance estimator for multilayer superconducting integrated circuits. The accuracy of the inductances calculated with Lmeter, about 5% [179], is sufficient for the design of RSFQ circuits, which have inductance margins of 40-50% [178]. Files with the correct format for Lmeter are generated automatically from the circuit layout by code included in the Cadence customization mentioned above. The inductances calculated with Lmeter are compared with those of the simulated circuit, and the layout is modified so that the extracted inductances are closer to the design values. Such modification often involves not only changes to the interconnect dimensions but also repositioning of the Josephson junctions within the layout. If the inductances of the simulated circuit were set to unrealistic values, a physical layout with the required inductances cannot be realized, and the circuit must be redesigned with more realistic parameter values. Fortunately, with enough circuit design experience, such dead ends can usually be avoided. Even after the layout has been modified so that the extracted inductances are close to the design values, the extracted parasitic inductances may differ significantly from those originally assumed for the simulated circuit. Therefore, the circuit is resimulated with the parasitic inductances extracted from the layout, and the operating margins recomputed. If the margins are notably degraded, the circuit is reoptimized with the more realistic values of parasitic inductance, and the layout is modified accordingly. Typically, only a minor modification (such as slight resizing of a storage inductor in a flip-flop) is required at this stage of the design. Finally, the Cadence tool Diva is used to check the entire layout for violations of the HYPRES design rules [123].

These software tools are the minimum requirement for the design of RSFQ circuits as complex as the modulator test chip. Other tools, routinely used in the design of complex semiconductor circuits, would expedite the design of superconducting integrated circuits but were not available at the time the modulator test chip was designed. The lack of automated layout versus schematic (LVS) verification was particularly inconvenient. While inductance calculation with Lmeter did confirm the integrity of the wiring within a gate, the connections between gates were only checked for logical correctness and physical alignment manually[2]. The sizing of all Josephson junctions and bias resistors was also checked manually. Because Josephson circuits have relatively small operating margins, even moderate errors (e.g., 10%) in the sizing of components can severely degrade circuit operation and yield. The connections of bias resistors to the numerous power supply lines of the test chip were also checked manually. Because manual checking is prone to human error, the test chip was checked and rechecked multiple times at each stage of its design. The heavy use of manual verification delayed the layout process by several months.

The lack of high-level tools for timing verification also complicated the design of the test chip. While circuit simulations with PSCAN were used to calculate the delays of RSFQ logic cells, simulation times grow rapidly with increasing circuit complexity. A few of the larger

[2]Since the extraction of inductances from layouts much larger than a single RSFQ gate is not computationally practical with Lmeter, Lmeter is not useful for checking the assembly of RSFQ gates into more complex circuit structures.

digital circuit blocks (most notably, the 1:4 DEMUX described in Section 10.2.3) were simulated in their entirety with PSCAN in order to study circuit timing in great detail, but the computation times of such simulations precluded their use for most of the larger circuit blocks. PSCAN simulation for timing verification of the whole test chip was utterly impractical. In the design of semiconductor digital circuits, timing verification of complex circuitry is accomplished with high-level logic simulators based on hardware description languages such as VHDL or Verilog HDL [179]. Without such high-level tools, timing verification of the modulator test chip could only be conducted manually, by adding up the delays of individual RSFQ cells within each large digital circuit block. Conservative design criteria (such as the one for race conditions mentioned in Section 10.2.1) were adopted so that minor errors in timing analysis did not jeopardize circuit functionality.

Finally, it is worth noting that the RSFQ design software developed at SUNY Stony Brook has been subsequently upgraded to include both LVS and high-level timing verification based on VHDL [180]. Similar tools are also now provided with the RSFQ design software developed at the University of Rochester [179]. The availability of such tools should improve the efficiency with which complex RSFQ circuits are designed in the future.

10.2.3 1:4 DEMUX

The block diagram of the 1:4 DEMUX is shown in Figure 10-3. The design uses a binary tree architecture [181], in which the data bits are first demultiplexed from one signal line to two signal lines, and then from two signal lines to four signal lines. The required routing of the SFQ data pulses is performed in three 1:2 DEMUX switching cores. Only the first 1:2 DEMUX switching core operates at f_s, the sampling rate of the bandpass modulator; the other two cores operate at $f_s/2$, so that their timing requirements are greatly relaxed. This is a fundamental advantage of a binary tree architecture over the shift-and-dump architecture described in [182], in which all stages are clocked at the incoming data rate. The two T flip-flops divide the sampling rate down by a factor of four. The data bits entering each 1:2 DEMUX switching core are alternately routed to its two outputs by driving the dual clock inputs with the complementary outputs of the appropriate T flip-flop. The D latches at the output of each 1:2 DEMUX switching core are used for time alignment of the demultiplexed data with the frequency-divided clocks.

Concurrent flow clocking is used throughout the DEMUX, so there are numerous races between the data pulses and clock pulses propagating along the JTLs represented as lines with arrows in the figure. The D latch shown in front of the first 1:2 DEMUX switching core actually represents the last storage cell of the three-stage shift register preceding the DEMUX. As discussed in Section 8.1, the shift register is designed so that this cell is destructively read out by the clock pulse before the data pulse from the previous shift register stage arrives. For all other cells in the DEMUX, the JTL delays are adjusted so that the clock pulses arrive *after* the data pulses. For instance, the delays along the JTLs labeled B and C are long enough that an SFQ data pulse propagating along the JTL labeled A arrives at and is stored inside the first 1:2 DEMUX switching core in advance of the SFQ clock pulse. When an SFQ pulse does arrive at one of its dual clock inputs, the 1:2 DEMUX switching core releases the stored data bit to the corresponding output. Note that the same clock pulse which releases a data bit from the last storage cell of the three-stage shift register later releases that data bit from the 1:2 DEMUX switching core. With this type of concurrent flow clocking (sometimes called *clock-follow-data* clocking [73]), the data

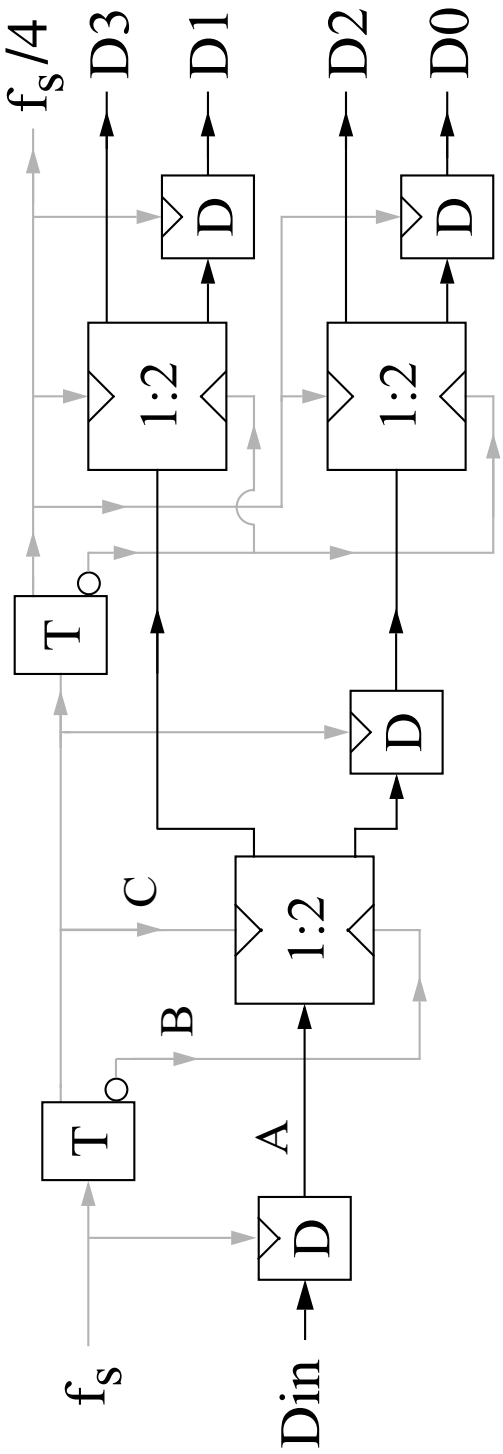


Figure 10-3: Block diagram of 1:4 DEMUX.

bits are pushed along from one cell to the next by the advancing wavefront of a single clock pulse. Since the data bits are only stored momentarily inside each cell in the data path, this type of concurrent flow clocking is not useful for memory circuits such as the shift registers used in the 256-bit acquisition memory of the test chip. For circuits such as the 1:4 DEMUX, though, such clocking is a powerful technique for controlling the skew between the propagating data and clock pulses.

The 1:4 DEMUX is the most complex digital circuit on the test chip clocked at f_s. Achieving the desired operating speed requires careful matching of delays along the JTLs which carry the SFQ data and clock pulses. Especially important are the delays of the JTLs labeled A, B, and C, which control the skew between the data and clock pulses arriving at the first 1:2 DEMUX switching core. For proper operation of the circuit, the data pulse must precede the clock pulse (at either of the dual inputs) by at least the setup time of the 1:2 DEMUX switching core. On the other hand, if the data pulse arrives too much earlier than the clock pulse, the maximum operating frequency will be degraded by excessive skew. In this design, independent power supplies are used to tune the delays of the JTLs labeled A, B, and C so that the skew between the data and clock pulses can be experimentally optimized for highest performance, even in the face of process parameter variations.

Figure 10-4 is a schematic of the 1:2 DEMUX switching core. This RSFQ cell, donated to this project by Kaplan at HYPRES, Inc., is derived from the B flip-flop originally described by Polonsky [183]. When an SFQ pulse arrives at the D input, it induces a 2π leap of phase (SFQ pulse generation) in junction J_1, and a binary 1 is stored as a circulating current through inductor L_q. By symmetry, this circulating current splits equally between junctions J_{2A} and J_{2B}, driving these junctions as well as J_{3A} and J_{3B} close to their critical currents. When an SFQ pulse later arrives at the CLK1 input, it is transferred over the JTL formed by J_{7A} and J_{8A} to decision-making pair J_{3A}–J_{4A}. Since its current is already close to its critical current, junction J_{3A} switches, and the SFQ pulse generated across this junction is picked up and transferred to the Q1 output over the JTL formed by J_{5A} and J_{6A}. The SFQ pulse generated across J_{3A} also induces switching of J_{2B}. Since J_{3B} does not switch, no SFQ pulse appears on the Q2 output. The switching of junctions J_{3A} and J_{2B} annihilates the circulating current, so readout of a binary 1 to the Q1 output is destructive and resets the circuit. Destructive readout of a binary 1 to the Q2 output is accomplished in a completely symmetric manner by applying an SFQ pulse to the CLK2 input. In this case, the junctions that switch are J_{7B}, J_{8B}, J_{3B}, J_{2A}, J_{5B}, and J_{6B}. On the other hand, if no SFQ pulse arrives at the D input because the data bit is a 0, no circulating current through L_q is set up before an SFQ clock pulse is applied to either the CLK1 or CLK2 inputs. In this case, when the SFQ clock pulse applied to the CLK1 (CLK2) input reaches decision-making pair J_{3A}–J_{4A} (J_{3B}–J_{4B}), upper junction J_{4A} (J_{4B}) switches instead of lower junction J_{3A} (J_{3B}). The state of the circuit remains unchanged, and the absence of an SFQ pulse on the Q1 (Q2) output represents a binary 0.

The entire 1:4 DEMUX shown in Figure 10-3 was simulated with PSCAN in order to evaluate race conditions and optimize circuit timing. With nominal circuit parameters, the maximum operating frequency is 38 GHz in simulation. Even higher operating frequencies could be obtained by changing the delays of the JTLs labeled A, B, and C, but such tweaking was not carried out in simulation since its utility would be limited by parameter variations in the fabricated circuit. Instead, these JTL delays were adjusted at the time of the experiment with the independent power supplies mentioned above.

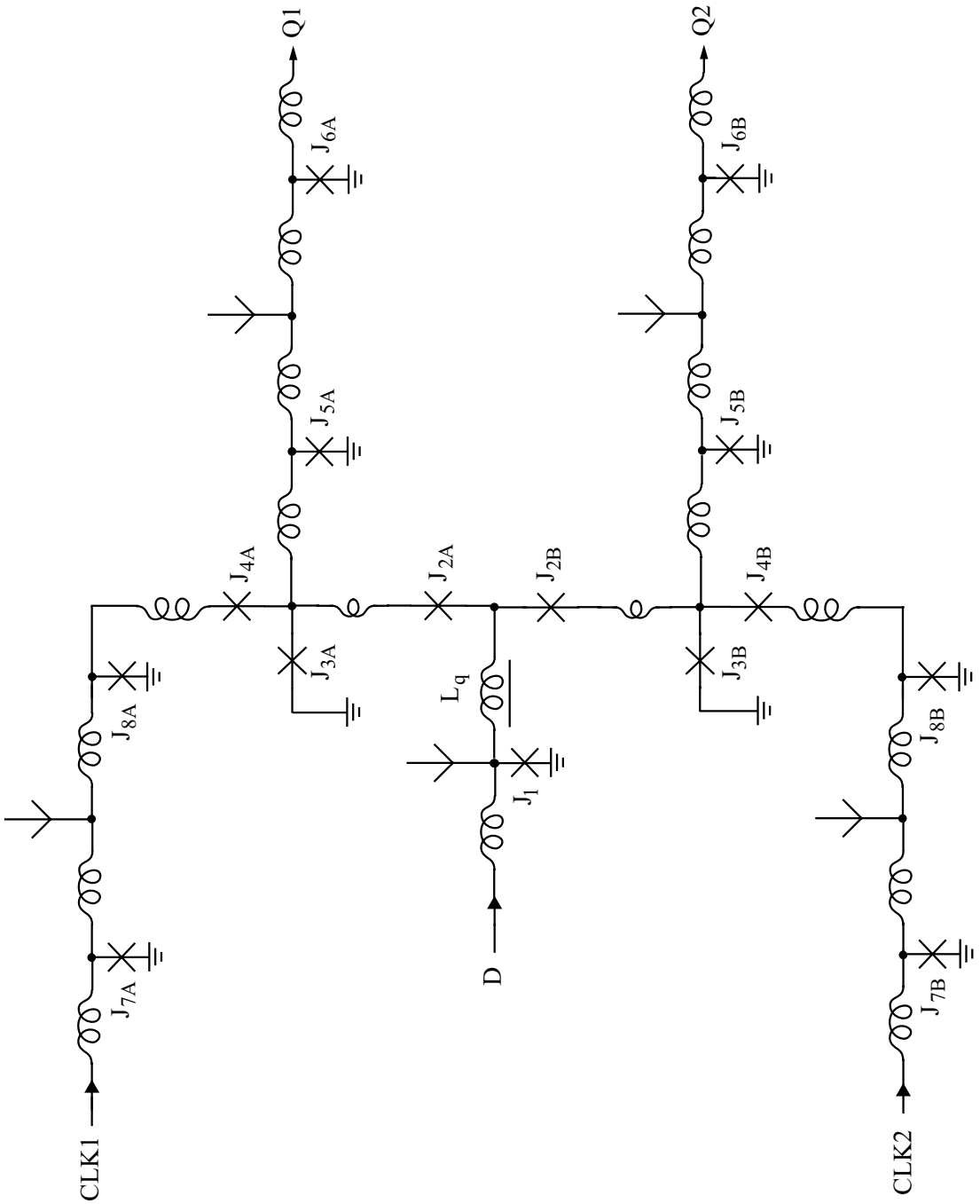


Figure 10-4: Schematic of 1:2 DEMUX switching core.

10.2.4 Programmable Counter

The programmable counter generates the timing signals which control loading and unloading of the 256-bit acquisition memory in accord with the timing diagrams of Figure 10-2. The key part of this circuit block is the programmable delay generator shown in Figure 10-5. The A and B outputs initiate loading of shift register memory banks A and B, respectively. The T flip-flops form a simple ripple counter, the output of which is fed back along two rows of D latches. With 13 T flip-flops in the ripple counter, one A pulse and one B pulse are generated every 8192 CLK cycles, equal to 32768 periods of the modulator sampling clock. The connections between the T flip-flops and D latches D_{0A}–D_{10A} are identical to those in the low-skew frequency divider described by Lin and Semenov [184], but a programmable delay between the A and B outputs is added with little extra circuitry by switching the clocking of D latches D_{0B}–D_{10B}. Switches S_0–S_{10} are controlled by 11 external currents. If all of the switches are in the 0 position, the pipelining latency along the lower row of D latches matches that along the upper row, and the A and B pulses are generated on the same cycle of CLK. Moving some of the switches to the 1 position increases the pipelining latency along the lower row, and the B pulse is delayed relative to the A pulse. For instance, moving S_0 from the 0 to 1 position increases the pipelining latency by one CLK cycle. Moving S_1 from the 0 to 1 position increases the pipelining latency by two CLK cycles since T flip-flop T_1, which clocks D latch D_{1B}, is toggling at half the rate of T_0. More generally, moving S_k from the 0 to 1 position increases the pipelining latency by 2^k CLK cycles, so the relative delay (in CLK periods) between the A and B pulses equals the 11-bit code given by S_0–S_{10} (from 0 to 2047). Since the programmable delay generator is clocked at $f_s/4$, M, the number of data bits skipped between loading shift register memory banks A and B for segmented correlation measurements, can be varied from 0 to 8060, in increments of 4. Because each stage of the delay generator is pipelined, the maximum operating frequency is independent of the number of stages and equals 21 GHz in simulation.

It should be noted that a race condition is introduced when one of the switches is moved from the 0 to 1 position. Consider, for instance, switch S_0. If S_0 is in the 1 position, the same output of T_0 which clocks D_{0B} also triggers T_1, which in turn clocks D_{1B}. For proper operation of the programmable delay generator, D_{0B} must be clocked before an SFQ pulse released from D_{1B} arrives at its data input. In this design, the stages of the delay generator are connected together with JTLs whose delays are large enough that this race condition is reliably satisfied.

In addition to the main A and B outputs, the programmable delay generator produces two other outputs, UNLOAD and HVSET. These signals are used as a two-phase clock (at $f_s/128$) in the readout controller.

The RSFQ circuit which realizes the single-pole double-throw switching action required by S_0–S_{10} is the only component in the programmable delay generator which has not been previously described by other researchers. The most straightforward implementation of such a circuit is to connect two independently controlled single-pole single-throw SFQ switches to a confluence buffer, as indicated in Figure 10-6. Junctions J_{1A}, J_{4A}, J_{1B}, and J_{4B} are used as short input and output JTLs for the two switch pairs J_{2A}–J_{3A} and J_{2B}–J_{3B}, which are controlled by external currents I_{sw1} and I_{sw2}, respectively. Such SFQ switch pairs controlled by external dc currents have been previously used in RSFQ logic circuits [41]. When an SFQ pulse is applied to switch pair J_{2A}–J_{3A}, it induces a 2π leap of phase across J_{3A} if I_{sw1} is at a high level and across J_{2A} if I_{sw1} is at a low level. In the former case, the SFQ pulse

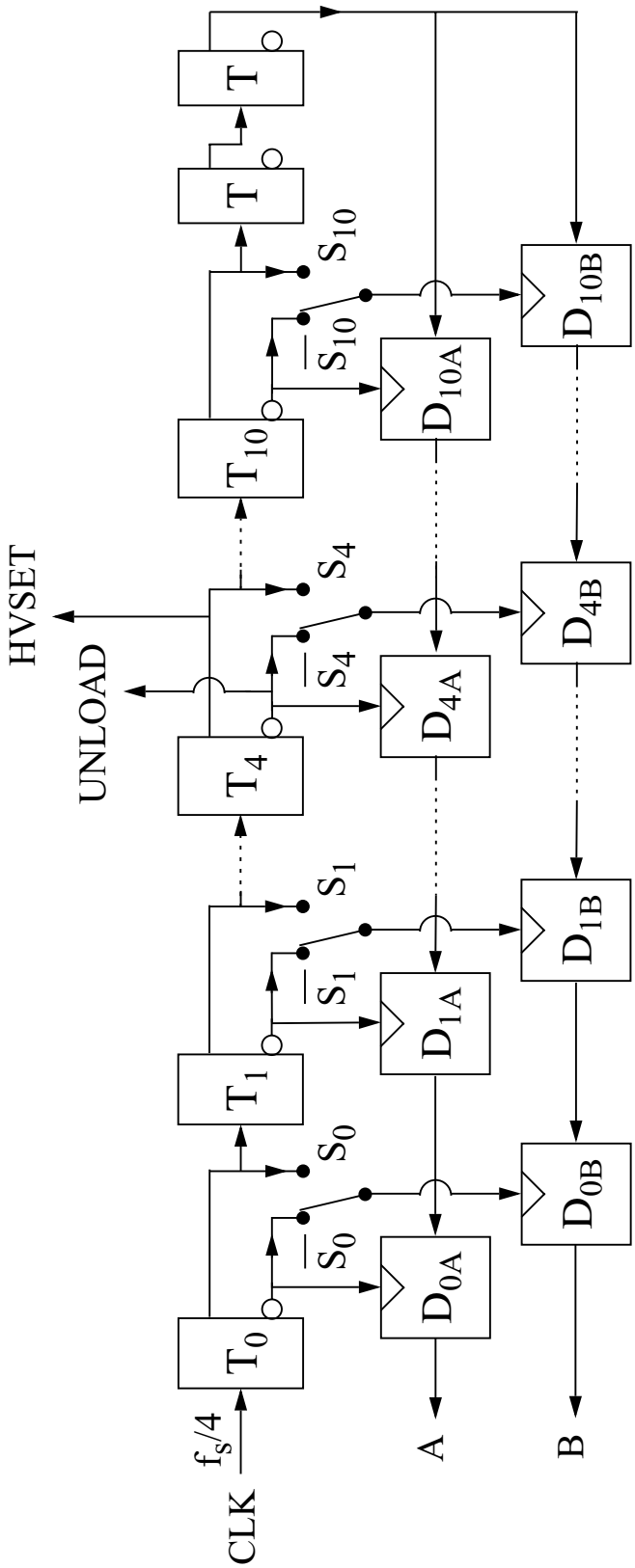


Figure 10-5: Block diagram of programmable delay generator.

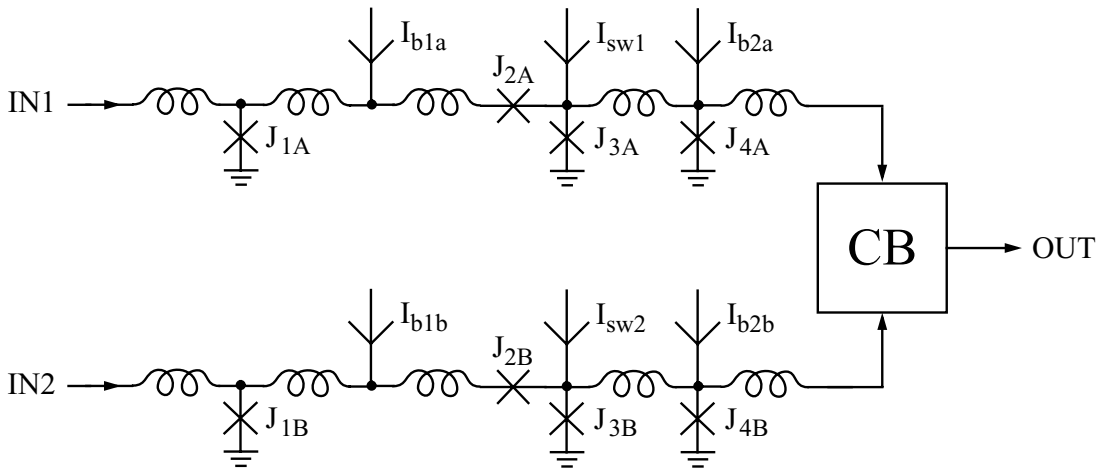


Figure 10-6: Implementation of single-pole double-throw SFQ switch as two independently controlled single-throw switches connected together with confluence buffer (CB).

is transferred to the output through the confluence buffer, and the switch between IN1 and OUT appears "closed". In the latter case, no SFQ pulse is passed to the confluence buffer, and the switch between IN1 and OUT appears "open". Switch pair J_{2B}–J_{3B} operates in exactly the same manner. Single-pole double-throw switching action is accomplished by setting I_{sw1} high when I_{sw2} is low, and vice versa. Because such signal inversion cannot be achieved on-chip with Josephson circuitry, this single-pole double-throw switch requires two external control currents, and a total of 22 external currents would be needed to control the 11 switches in the programmable delay generator. Such a large number of external currents is difficult to provide with the limited number of pads contacted by the cryogenic sample holder.

An improved single-pole double-throw switch which requires only one external control current is obtained by replacing the lower junctions in the two switch pairs with double-junction (DJ) SQUIDs whose critical currents are modulated in a complementary fashion by a common control current. In the schematic shown in Figure 10-7, J_{3A}, J_{4A}, L_{F1A}, and L_{P3A} form one DJ SQUID loop, and J_{3B}, J_{4B}, L_{F1B}, and L_{P3B} form the other. Magnetic flux is applied to the SQUIDs with external current I_{sw}, which is split by a resistive current divider formed by R_A and R_B and directly injected into inductors L_{F1A} and L_{F1B}. The applied flux modulates the critical currents of the DJ SQUIDs. Consider first the gating of an IN2 input pulse by the right half of the circuit. When the critical current of the right DJ SQUID is small, an SFQ pulse entering the circuit through J_{1B} induces switching of J_{3B} and J_{4B}, and an SFQ pulse is passed to the output through the confluence buffer. When the critical current of the right DJ SQUID is large, the SFQ input pulse induces switching of J_{2B} instead of the junctions in the SQUID, and no SFQ pulse is passed to the confluence buffer. The IN1 input is gated in a similar manner by the left DJ SQUID, but current I_{off} is used to offset the flux in this SQUID by approximately $\Phi_0/2$ so that its critical current modulation as a function of I_{sw} is opposite to that of the right DJ SQUID. For the right DJ SQUID, the critical current is large when I_{sw} is at a low level and small when I_{sw} is at a high level. For the left DJ SQUID, the critical current is small when I_{sw} is at a low level

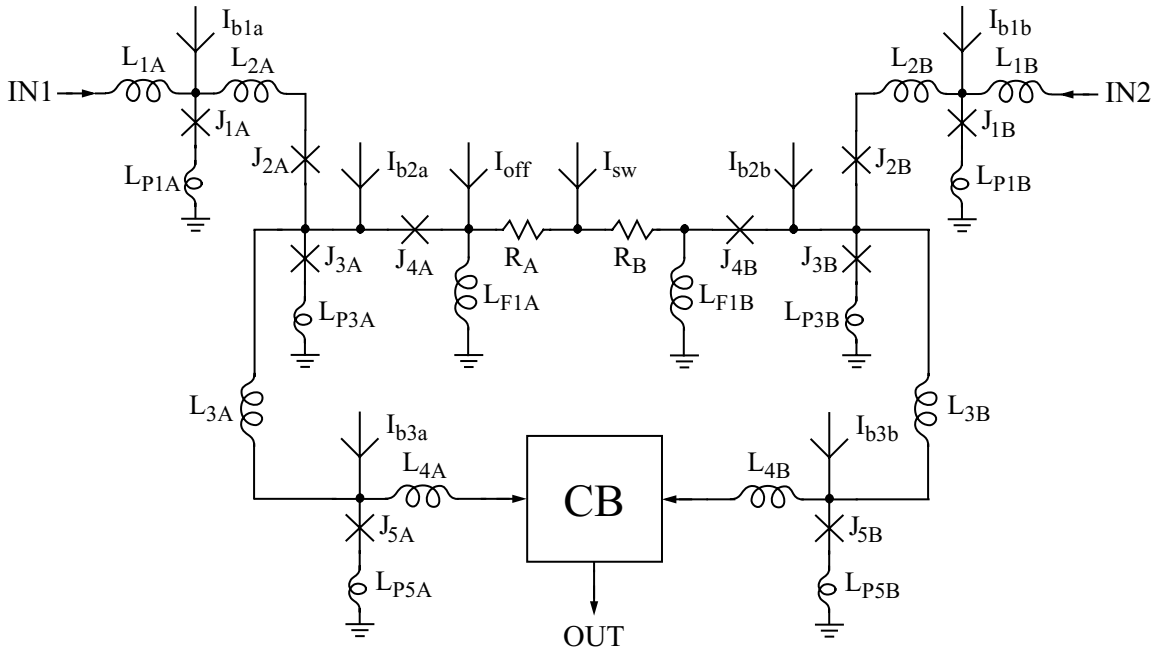


Figure 10-7: Single-pole double-throw SFQ switch controlled by single external current. The circuit parameters are: R_A=6.43 Ω, R_B=6.01 Ω, L_{F1A}=L_{F1B}=1.91 pH, L_{1A}=3.3 pH, L_{1B}=L_{2A}=L_{2B}=2.4 pH, L_{3A}=L_{3B}=4.38 pH, L_{4A}=L_{4B}=3.6 pH, L_{P1A}=L_{P1B}=0.30 pH, L_{P3A}=L_{P3B}=0.18 pH, L_{P5A}=L_{P5B}=0.11 pH, I_{c1A}=I_{c1B}=I_{c5A}=I_{c5B}=248 μA, I_{c2A}=I_{c2B}=I_{c3A}=I_{c3B}=235 μA, I_{c4A}=I_{c4B}=221 μA, I_{b1a}=138 μA, I_{b1b}=144 μA, I_{b2a}=I_{b2b}=162 μA, I_{b3a}=I_{b3b}=178 μA, I_{off}=546 μA, and I_{sw}=−301 μA (low value), 790 μA (high value).

and large when I_{sw} is at a high level. Consequently, IN1 input pulses are passed to the output when I_{sw} is low, and IN2 input pulses are passed to the output when I_{sw} is high.

The single-pole double-throw SFQ switch shown in Figure 10-7 was designed and optimized with the PSCAN simulator; the parameter values of the final design are listed in the figure caption. The inductance values were extracted with Lmeter from the Cadence layout of the cell. Table 10.1 lists the simulated operating margins of the switch with these parameter values. In addition to the margins of individual circuit parameters, such as I_{c2A} and L_{F1A}, the table also lists the margins of three global parameters (with nominal values of unity): *XI*, which multiplies all bias currents; *XJ*, which multiplies all junction critical currents; and *XL*, which multiplies all inductances. The margins of the global parameters indicate the sensitivity of the circuit to correlated variations among several circuit elements [183], such as those due to process parameter variations [177]. For proper circuit operation, it is important that the correct magnetic fluxes be applied to the two DJ SQUIDs. For fixed values of I_{off} and I_{sw}, the applied fluxes are proportional to L_{F1A} and L_{F1B}, and the relatively small margins of these inductances limit the lower and upper margins of global parameter *XL*. Variations in these inductances, though, are easily compensated by altering the values of I_{off} and I_{sw} so that the fluxes applied to the DJ SQUIDs have the correct values. Since I_{sw} is an external control current, its value is easily adjusted with room-temperature electronics. Flexible adjustment of I_{off} is only possible if this current is generated from its own independent power supply. Assuming that inductance variations

Table 10.1: Operating margins[a] of single-pole double-throw SFQ switch.

Circuit Parameter	Lower Margin (%)	Upper Margin (%)
XI	-41	37
XJ	-28	41
XL	-21	25
I_{c1A}, I_{c1B}	< -70	> 70
I_{c2A}	-38	38
I_{c2B}	-40	40
I_{c3A}	-50	50
I_{c3B}	-50	53
I_{c4A}	-49	52
I_{c4B}	-48	50
I_{c5A}	-65	54
I_{c5B}	-44	55
L_{F1A}	-21	27
L_{F1B}	-44	25
I_{off}	-41	30
I_{b2a}, I_{b2b}	< -70	> 70

[a]The margins are only accurately calculated up to ±70%.

are fairly uniform across the chip, one independent supply is sufficient to adjust current I_{off} globally for each single-pole double-throw SFQ switch used in the programmable delay generator. Adding this independent supply to the 11 I_{sw} control currents, the total number of external connections needed[3] to adjust and control the programmable delay generator is 12, or 10 fewer than if the switch design of Figure 10-6 were used. The other margins listed in Table 10.1 are larger than those of most RSFQ cells [31, 121]. The smallest margin of a junction critical current is that of J_{2A} and equals ±38%.

As mentioned earlier in the chapter, each half of the 256-bit acquisition memory on the test chip is organized as four rows of 32-bit shift registers. Loading of each row is accomplished by clocking the 32-bit shift register with 32 consecutive SFQ pulses at a frequency of $f_s/4$. The timer circuit shown in Figure 10-8 converts each A output pulse from the programmable delay generator into a burst of 32 LOADA pulses, which clock the four rows of shift register memory bank A. An identical copy of this circuit converts each B output pulse from the programmable delay generator into a burst of 32 LOADB pulses, which clock the four rows of shift register memory bank B. (These LOADA and LOADB pulses were depicted earlier in the timing diagrams of Figure 10-2. In the diagrams, the number of pulses and their spacing are not accurate for the sake of legibility.) The heart of the timer circuit is the "clock controller" discussed by Likharev and Semenov [31]. T flip-

[3]The test chip implemented in this project actually uses 13 external connections for adjustment and control of the programmable delay generator. In order to compensate for possible nonuniformity of inductance values across the chip, two independent power supplies are used to adjust the I_{off} currents: one for switches S_0–S_3 and one for switches S_4–S_{10}. The experimental results, though, show that this precaution was unnecessary, and one independent supply would have been sufficient for adjusting all the I_{off} currents.

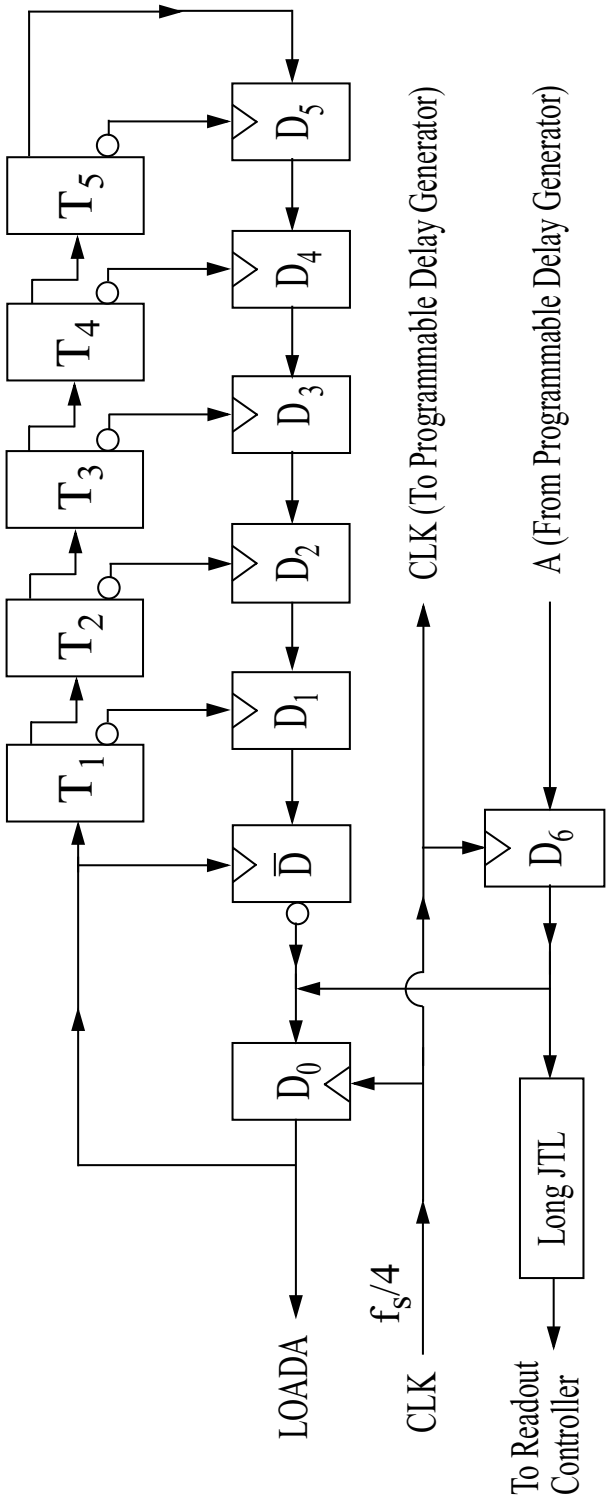


Figure 10-8: Timer for generating 32 LOADA pulses.

flops T_1–T_5 and D latches D_1–D_5 form a low-skew frequency divider similar to the circuitry in the programmable delay generator. A feedback loop is created by connecting the output of the frequency divider back to its input through a timed inverter and D latch D_0. The burst of LOADA pulses begins when an A output pulse from the programmable delay generator is injected into this loop (with a confluence buffer) and loaded into D_0. Upon each successive CLK pulse, D_0 is destructively read out, a LOADA pulse is generated which clocks both the frequency divider and the inverter, and the output of the inverter reloads D_0. This cycle is repeated until the frequency divider produces an SFQ output pulse which loads the timed inverter with a binary 1. Upon the next CLK pulse, a LOADA pulse is generated, but D_0 is not reloaded since the inverter generates no SFQ output pulse (binary 0). No more LOADA pulses are generated until D_0 is loaded by the next A output pulse from the programmable delay generator. The length of each burst of LOADA pulses is determined by the number of stages in the frequency divider; with five stages, each burst is 32 pulses long.

D latch D_6 provides a stage of pipelining between this timer circuit and the programmable delay generator. Since the circuitry which produces the LOADB pulses also contains such a latch, the latency added by such pipelining does not change the relative delay between the LOADA and LOADB pulses. The output of D_6 is also transferred over a long (> 2 mm) JTL to the readout controller on the other side of the chip. This timing signal is used to synchronize readout of the acquisition memory with the LOADA and LOADB pulses.

10.2.5 Shift Register Acquisition Memory

Figure 10-9 shows shift register memory bank A, together with its loading and unloading circuitry. The other half of the 256-bit acquisition memory, shift register memory bank B, is identical to this one. The four rows of 32-bit shift registers are built from an RSFQ cell donated to this project by Rylov at HYPRES, Inc. This RSFQ cell is optimized for concurrent flow clocking and is similar to the buffered shift register cell shown earlier in Figure 8-2. The use of one less junction in the buffering JTL, though, reduces the number of junctions contained in each shift register stage from six to five. The layout area of this cell, 40 μm $\times$ 120 μm, is relatively compact for this type of circuit.

While the shift register cells are optimized for concurrent flow clocking, they also function reliably with counterflow clocking, though their maximum operating frequency is lower in this mode. Because the junctions which carry the SFQ clock pulses along the shift register form a uniform (non-amplifying) JTL, clock pulses can propagate in either direction through the shift register. A unique feature of this shift register memory bank design is the use of *bidirectional* clocking. Concurrent flow clocking is used during loading of the shift registers, and counterflow clocking is used during unloading of the shift registers. (Note that the clock lines between the shift register cells have arrows at both ends. In the counterflow mode, the direction of clock propagation is opposite to that implied by the CLKin and CLKout labels of the cells.) Data bits are shifted into each 32-bit shift register by inserting 32 LOADA pulses (from the programmable counter) into its clock line through a unidirectional buffer (reviewed in Section 2.2.5). When these LOADA pulses reach the right end of the shift register, they are blocked from entering the unloading circuitry by a second unidirectional buffer, pointed in the opposite direction. During unloading, data bits are shifted out of each 32-bit shift register by inserting 32 UNLOADA pulses (from the

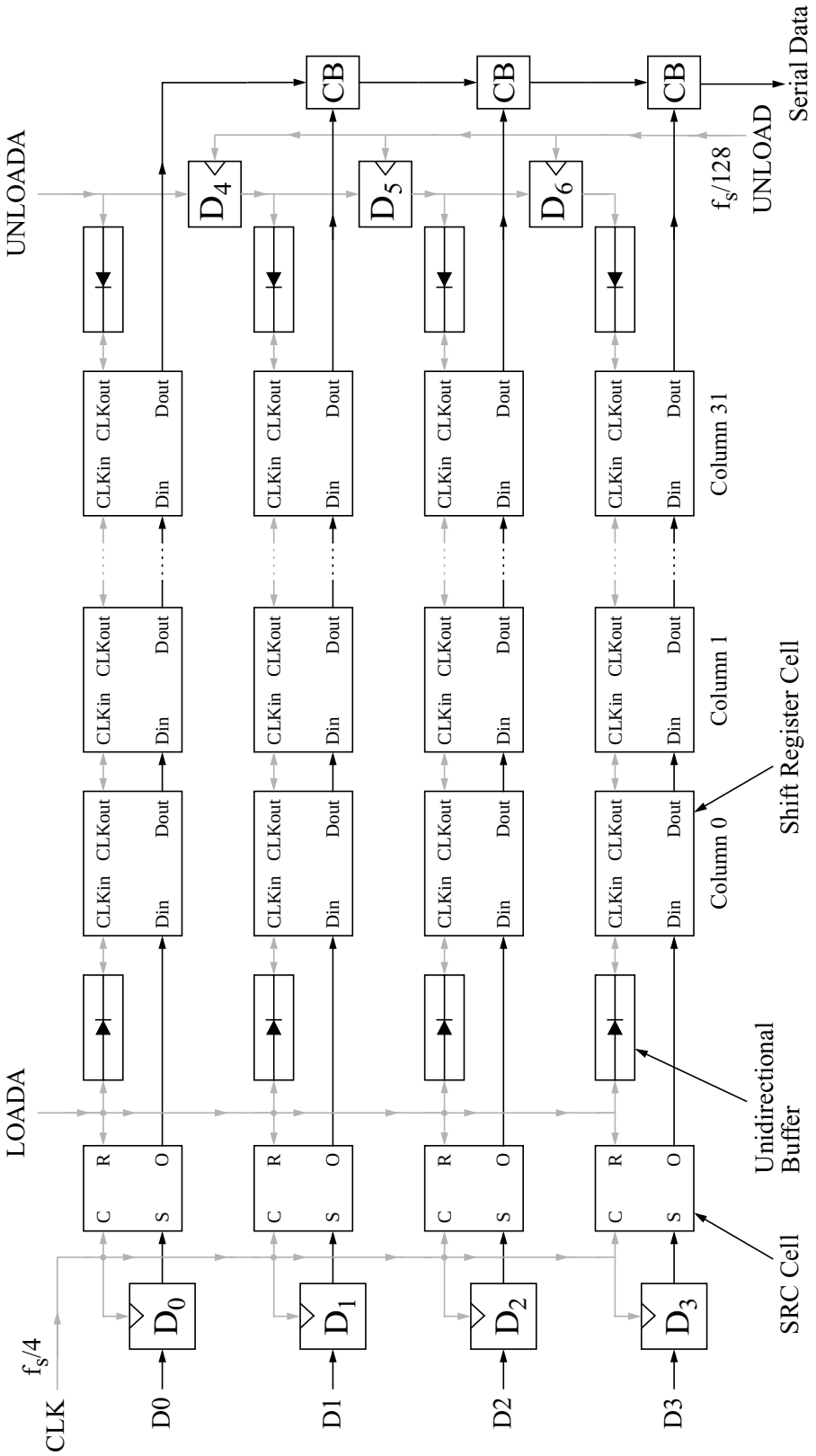


Figure 10-9: Shift register memory bank A with loading and unloading circuitry.

readout controller) into its clock line through the second unidirectional buffer. When these UNLOADA pulses reach the left end of the shift register, they are blocked from entering the loading circuitry by the first unidirectional buffer. The lower maximum operating frequency of the shift register in this counterflow mode is irrelevant at the modest frequencies used for readout. By permitting the loading circuitry and the readout controller to be placed at opposite ends of the shift registers, this bidirectional clocking scheme simplifies the layout of the test chip. This is particularly beneficial at the loading end, where a tight and efficient layout is essential for achieving multi-GHz operating frequencies.

The loading and unloading circuits are now discussed in more detail. Signals CLK and D0-D3 are the frequency-divided ($f_s/4$) clock and 4-bit wide data produced by the 1:4 DEMUX. Logic gates known as Set-Read-Clear (SRC) cells are used to select the data bits to be stored in the shift registers. The SRC cell [185] is a destructive readout latch which can be cleared (reset) without the generation of an SFQ output pulse. An SFQ data pulse arriving at the S input loads the SRC cell with a binary 1. Application of a LOADA pulse to the R input destructively reads out the SRC cell to its O output so that the data bit is transferred to the first cell of the 32-bit shift register. If no LOADA pulse arrives during that particular CLK cycle, the data bit remains in the SRC cell until the beginning of the next CLK cycle, when the SRC cell is cleared by an SFQ pulse arriving at its C input. Thus, the data bit is discarded in the absence of a LOADA pulse.

Several race conditions need to be satisfied for proper operation of the loading circuitry. Most of the races are confined inside local regions of circuitry. Since the SRC cells must be in the "0" state when the data pulses arrive at their S inputs, the CLK pulse must clear the SRC cells before it reads out D latches D_0–D_3. Similarly, the LOADA pulse must clock the 32-bit shift registers before it reads out the data from the SRC cells. The use of short JTL delay lines ensures that these local race conditions are satisfied with a large timing margin. A more challenging problem is controlling the skew between signals D0–D3, CLK, and LOADA, which are generated in different areas of the chip (up to 1 mm away) and delivered to the shift register memory bank over long JTLs (with up to 23 junctions per signal line). While the delays of these long JTLs are carefully matched in the design, such matching may be degraded by parameter variations in the fabricated circuit, and unwanted signal skew may compromise the operation of the loading circuitry. To compensate for such parameter variations, three independent power supplies are used to tune the delays of these long JTLs: one for the JTLs which carry the D0–D3 data pulses, one for the JTL which carries the CLK pulses, and one for the JTL which carries the LOADA pulses[4].

Data bits are read out serially from the shift register memory banks at a rate of $f_s/128$, the frequency of the UNLOAD signal generated by the programmable delay generator (Figure 10-5). The first data bit is shifted out of the first shift register row (row 0) when the readout controller generates an UNLOADA pulse. This data bit propagates through JTLs and confluence buffers to the serial data output, which is connected to the high voltage output driver discussed in the next section. Upon the next UNLOAD cycle, the UNLOADA pulse is clocked through D latch D_4, and a data bit is shifted out of shift register row 1 and transferred to the serial data output. Similarly, two more data bits are unloaded from

[4]These three same supplies provide power to the long JTLs which deliver signals D0–D3, CLK, and LOADB to shift register memory bank B. Therefore, the signal skew cannot be optimized independently for the two halves of the acquisition memory. The experimental results show that an acceptable compromise is easily reached.

rows 2 and 3 over the next two UNLOAD cycles. Upon the next UNLOAD cycle, the readout controller generates another UNLOADA pulse, and four more bits are successively unloaded from rows 0–3. Eventually, after 32 UNLOADA pulses, all of the bits captured in shift register memory bank A are unloaded to the serial data output, in exactly the same bit order as originally generated by the bandpass modulator. The timer circuit in the readout controller which generates the burst of 32 UNLOADA pulses is a simplified version[5] of the circuit shown in Figure 10-8.

Figure 10-10 is a schematic of the SRC cell, donated to this project by Rylov at HYPRES, Inc. This circuit is derived from the RSFQ B flip-flop [183] and is similar in operation to the 1:2 DEMUX switching core[6]. When an SFQ pulse arrives at the S input, it induces a 2π leap of phase in junction J_1, and a binary 1 is stored as a circulating current through L_q. The majority of this circulating current flows into J_3 and J_4; a smaller portion flows into J_2. When an SFQ pulse later arrives at the R input, it is transferred over the JTL comprising J_{11} through J_{13} to decision-making pair J_4–J_5. Since its current is already close to its critical current, junction J_4 switches, and the SFQ pulse generated across this junction is picked up and transferred to the O output over the JTL formed by J_6 and J_7. The SFQ pulse generated across J_4 also induces switching of J_2. The switching of J_4 and J_2 annihilates the circulating current, so readout of the data bit to the O output is destructive and resets the circuit. Clearing of a binary 1 stored in the circuit is accomplished by applying an SFQ pulse to the C input. This pulse is transferred over the JTL comprising J_8 through J_{10} to decision-making pair J_2–J_3. Due to the circulating current through L_q, J_3 switches, and the SFQ pulse generated across this junction annihilates the circulating current. Since J_4 does not switch, the circuit is reset without an SFQ pulse appearing on the O output. On the other hand, if no SFQ pulse arrives at the S input because the data bit is a 0, no circulating current through L_q is set up before an SFQ pulse is applied to the R input. In this case, when the SFQ pulse applied to the R input reaches decision-making pair J_4–J_5, J_5 switches instead of J_4. The state of the circuit remains unchanged, and the absence of an SFQ pulse on the O output represents a binary 0. Similarly, the state of the circuit remains unchanged if an SFQ pulse is applied to the C input when the circuit is already in the "0" state. In this case, the only junctions which switch are J_8, J_9, J_{10}, and J_2.

10.2.6 Output Interface Circuits

The high voltage (HV) output drivers of the test chip boost the RSFQ signal levels up to voltages (> 2 mV) which are large enough to be detected reliably by wideband (GHz) room-temperature amplifiers. The simplest Josephson output drivers which generate voltage levels in excess of 2 mV are latching circuits based on switching one or more unshunted, underdamped junctions to the voltage state [174]. The major drawback of using circuits based on unshunted junctions is their need for ac power. Because the transition to the

[5]The low skew of the frequency divider shown in Figure 10-8 is not needed at the relatively low operating frequency of the readout controller. The circuit is therefore simplified by replacing the low-skew frequency divider with a simple ripple counter comprising five T flip-flops (with no D latches).

[6]In fact, an SRC cell can be implemented as a 1:2 DEMUX switching core with one of its outputs logically unconnected (though suitably terminated). Clearing the cell could then be accomplished by reading out a binary 1 to the unused output. However, a circuit specifically designed for the SRC function is more economical in terms of junction count and layout area.

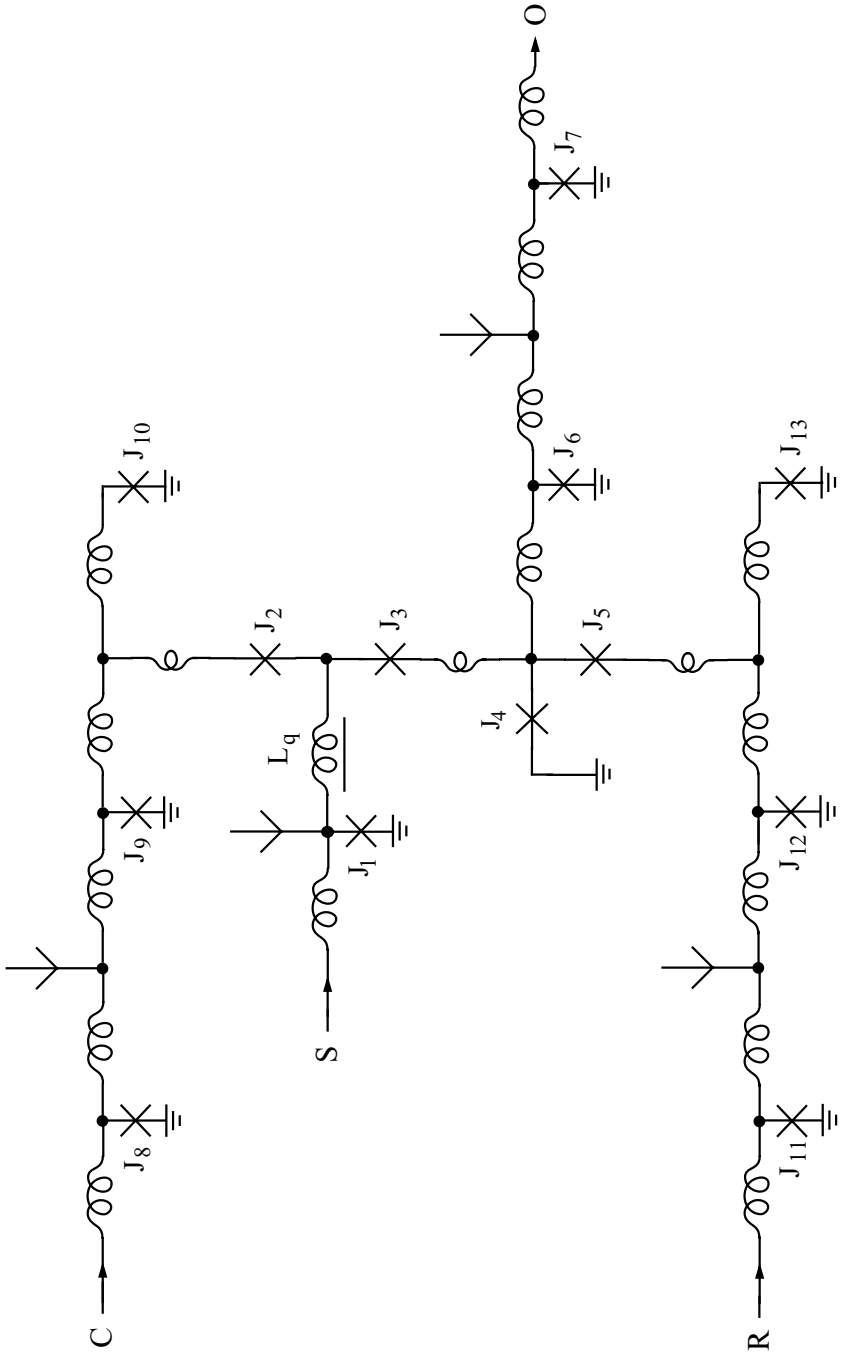


Figure 10-10: Set-Read-Clear (SRC) cell.

voltage state is hysteretic, an unshunted junction can only be reset to the superconducting state by reducing its bias current below I_{min} (recall Figure 2-9(a)) during each readout cycle. Due to crosstalk and ground bounce, supplying the output drivers with ac power which is modulated on and off at the readout rate (in the hundreds of MHz) can disturb the operation of other circuits on the test chip [186]. In their report on the first experimental demonstration of a superconducting bandpass $\Delta\Sigma$ modulator, Hashimoto and his research group at ISTEC attributed the higher than expected in-band noise to interference from ac power [156].

To avoid the problems associated with ac power, the test chip employs exclusively dc-powered circuitry, and all of the Josephson junctions are externally shunted to be nonhysteretic. The two high voltage outputs of the chip are generated with a pair of dc-powered output drivers, one of which is illustrated in Figure 10-11. This circuit, reported in [186], was donated to this project by Rylov at HYPRES, Inc. The SFQ pulse inputs are first converted to "low voltage" dc levels (100-200 μV) with a reset-set (RS) type of SFQ/DC converter. The low voltage output of the SFQ/DC converter is then distributed with a large array of amplifying JTLs and splitters to 12 SQUID control amplifiers. The low voltage input of each SQUID control amplifier is converted into a current with a single resistor; this control current is magnetically coupled to two symmetric DJ SQUIDs. While the voltage modulation across each DJ SQUID is only about 100 μV, an output swing in excess of 2 mV is obtained by connecting all 24 DJ SQUIDs in series. All of the SQUIDs in the series string are biased with a single dc current source. An output driver with multi-GHz bandwidth is attained by careful matching of the delays along the multiple JTL paths. This circuit has demonstrated low bit error rates ($< 10^{-11}$) up to data rates of 4 Gbit/s [186]. Such performance is much higher than required for the modulator test chip, for which the readout rate is only about 350 Mbit/s at the maximum sampling rate ($f_s = 45$ GHz).

The high voltage output drivers just described are compatible with either ac-coupled or dc-coupled readout electronics. In this work, the two high voltage outputs of the test chip (signified as DATA and START in Figure 10-2) are detected with ac-coupled room-temperature amplifiers, which are cheaper and less sensitive to power-line interference [174] than dc-coupled amplifiers with similar bandwidths (> 1 GHz). In general, transmission of digital signals over ac-coupled channels is most easily accomplished if the signals are encoded for good dc balance [187]. Assuming that the superconducting bandpass $\Delta\Sigma$ modulator is biased so that it produces approximately equal numbers of 1's and 0's, the DATA output naturally has good dc balance and needs no special encoding. Since it is ac-coupled, the analog input has no effect on the dc balance of the DATA output. On the other hand, the START bit is only asserted when the first DATA bit (out of 256 bits) is being read out from the acquisition memory. Because of its low duty cycle, the START bit output must be encoded for good dc balance.

Figure 10-12 shows the output encoder for the START bit and its timing diagram. Signals HVSET and UNLOAD, produced by the programmable delay generator (Figure 10-5), provide the two-phase clock for the readout controller. In the absence of an A_DLY pulse, the inverter is in the "0" state, so the two-phase clock signals alternately set and reset the high voltage output driver, thereby generating a square wave output with a 50% duty cycle and a frequency equal to the readout rate ($f_s/128$). The START bit is logically asserted upon the arrival of an A_DLY pulse, which is derived by passing the A output of the programmable delay generator through a couple of D latches; the pipelining latency of the

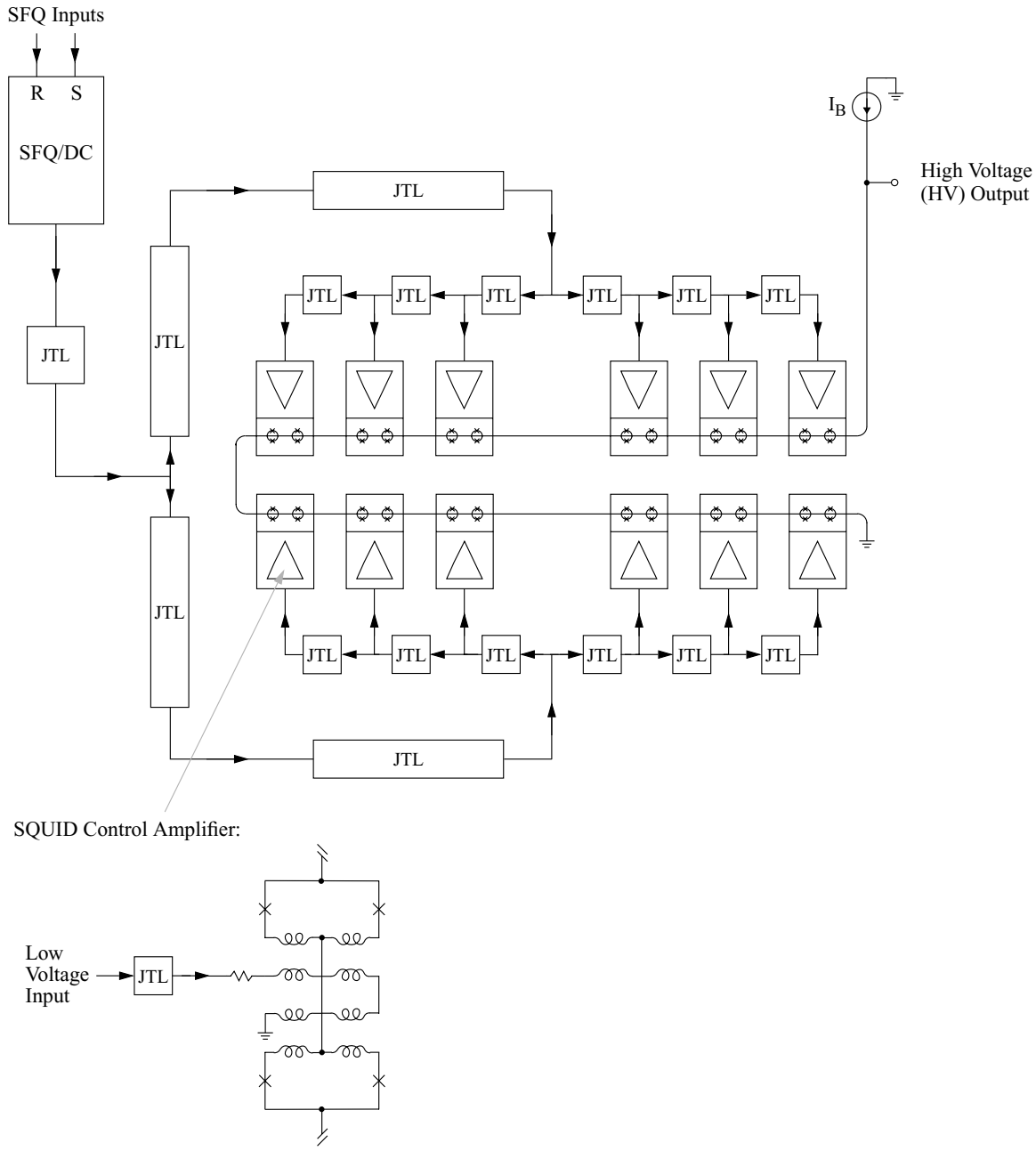


Figure 10-11: High voltage (HV) output driver with 2 mV output swing.

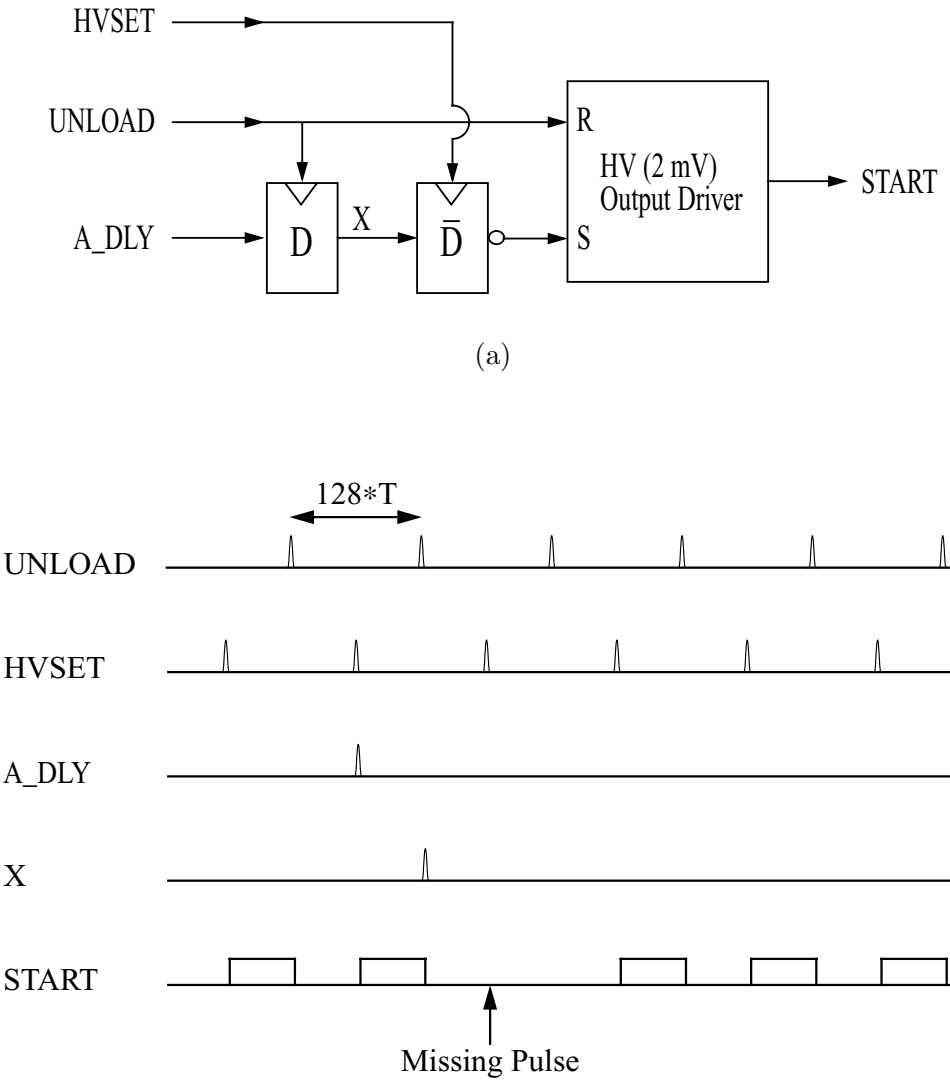


Figure 10-12: Output encoder for START bit. (a) Block diagram (including high voltage output driver). (b) Timing diagram.

D latches is chosen so that the START bit is asserted on the high voltage output at the correct time. Loading the inverter with a binary 1 inhibits setting of the high voltage output driver, and the missing pulse denotes assertion of the START bit. Because of its infrequent occurrence, the missing pulse has a negligible effect on the dc balance of the output signal. The encoded START bit output and the unencoded DATA output can be amplified with high waveform fidelity by ac-coupled amplifiers, provided that the low frequency cutoff of the amplifiers is much lower than the readout rate. In the experiments discussed in Chapter 12, the readout rate in all cases exceeds 160 Mbit/s, and the low frequency cutoff of the ac-coupled amplifiers is below 100 kHz.

10.2.7 Layout and Fabrication

The test chip is laid out for the standard HYPRES niobium process [123] with 1 kA/cm^2 critical current density for the Josephson junctions. The minimum feature sizes of the Josephson circuits obey all design rules, such as 2 μm widths for metal lines and 3 μm$\times$3 μm areas for the Josephson junctions. The design rules are only violated in the layout of the MSM photodiode, whose interdigitated fingers have the same 1 μm width and spacing as the MSM photodiodes used earlier for optical clocking of simple Josephson circuits (Chapter 6).

The importance of full custom layout for maximizing the performance of RSFQ circuits can hardly be overstated. Because RSFQ circuits are not tolerant of excessive inductances between stages, logic gates in different physical locations cannot be connected together with long wires ($>$ 50–100 μm). Such gates can be connected together with JTLs, but the propagation delay of a JTL (at least 4 ps per stage) can degrade the maximum operating frequency. In order to achieve the highest performance, the usage of JTLs between stages must be minimized by arranging the RSFQ cells so that their inputs and outputs are in close proximity. Finding such an arrangement is simple for regular circuit structures such as shift registers but much more labor-intensive for random logic. In the latter case, several custom variations of each RSFQ elementary cell may be needed to meet the different requirements on layout dimensions and input/output locations in various physical environments.

A good example of full custom layout is that of the 1:4 DEMUX, shown in Figure 10-13. In the figure, the layout has been mirrored so that the direction of signal flow matches that in the block diagram of Figure 10-3. The number of Josephson junctions in the layout equals 145. The circuitry labeled C_DIA is not part of the 1:4 DEMUX proper but contains a DC/SFQ converter and a confluence buffer for inserting SFQ pulses onto the clock output line during low frequency diagnostic testing; similar circuits (not shown in the figure) are used for inserting SFQ pulses onto data output lines D0–D3. Not counting the circuitry labeled C_DIA, the area of the 1:4 DEMUX is approximately 400 μm $\times$ 800 μm. As mentioned earlier, the 1:4 DEMUX is the most complex circuit on the test chip clocked at f_s, and its layout is heavily optimized for highest performance. Common layouts are used for the two T flip-flops and for the three 1:2 DEMUX switching cores, but the layouts of the other cells are all customized for each specific situation. Note, for instance, the different layout configurations used for the three D latches. The layout of the D latch at the output of the first 1:2 DEMUX switching core is elongated, and the data input and output are located at opposite ends. The relatively large separation between input and output reduces the number of JTL stages needed for transferring the SFQ data pulses across the DEMUX, thereby reducing propagation delay. In contrast, the other two D latches are designed to fit into a compact area, with shapes dictated by the needs of neighboring circuitry. In

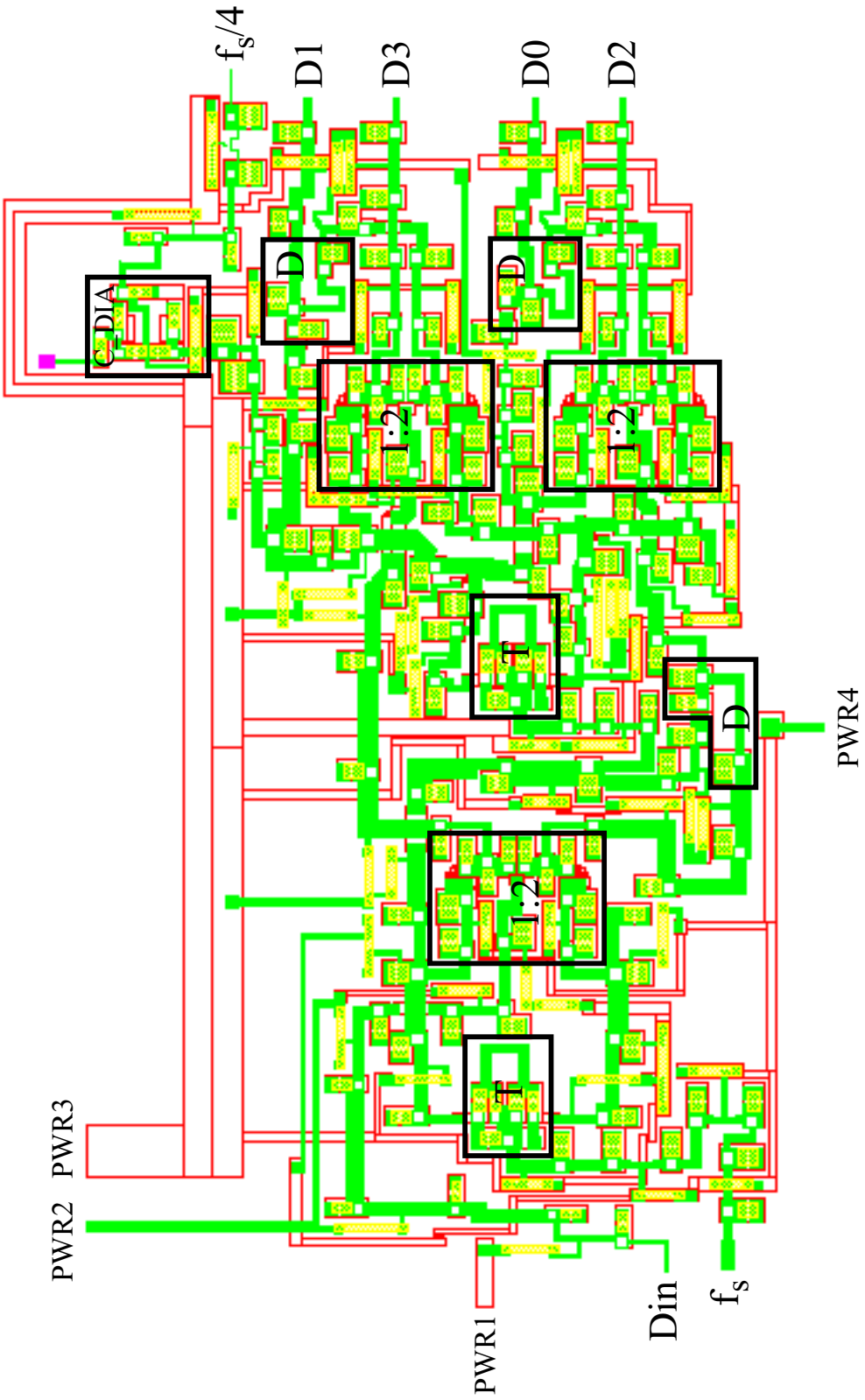


Figure 10-13: Layout of 1:4 DEMUX.

the figure, the Josephson circuits not enclosed inside the labeled boxes are the JTLs and splitters that transfer and distribute the SFQ pulses between the RSFQ cells. These circuits have been carefully laid out (in most cases, one junction at a time) so that the propagation delays of the JTLs between cells are close to the values optimized in circuit simulations. A particularly challenging task was the layout of the JTLs and splitters in the middle of the three 1:2 DEMUX switching cores and surrounding the second T flip-flop. This circuitry had to be packed very close together in order not to add delay with extra JTL stages. Most of the power for the 1:4 DEMUX is provided over the supply line labeled PWR3. Auxiliary supply lines PWR1, PWR2, and PWR4 are used for tuning the delays of the JTLs along which the data and clock pulses propagate.

Custom layout techniques were also applied to other circuits on the test chip which operate at multi-GHz frequencies, such as the programmable counter and the loading circuitry of the shift register memory banks. In most cases, though, the layouts of these other circuits did not have to be optimized to the same degree as the 1:4 DEMUX layout since their operating frequency is lower ($f_s/4$).

A potential source of problems for a complex superconducting circuit is magnetic coupling between large power supply currents and the Josephson circuitry [188, 189]. Such coupling, which is not modeled by existing software tools, may shift the operating points of the junctions and degrade circuit margins. Both the currents in the power supply lines and the return currents flowing through the superconducting ground plane may couple to the Josephson circuits. The focus in this section is on the design of the power supply lines for minimum magnetic disturbance of the Josephson circuitry. Section 11.2.1 explains how magnetic coupling from ground plane return currents is reduced by proper grounding of the test chip to the external setup.

In general, coupling from mutual inductance is largely avoided by routing the power supply lines so that they cross signal lines orthogonally. Such wire routing reduces mutual coupling significantly, but not necessarily perfectly. The currents flowing through the supply lines may be slightly distorted from perfect orthogonality at signal crossovers by the presence of nearby corners or processing nonuniformities. Because the mutual coupling due to imperfect orthogonality has not been comprehensively studied for typical Josephson integrated circuit processes, a conservative design approach was adopted for the layout of the power supply grid. Power supply lines only cross signal wires which are elements of JTL stages, whose large operating margins make them relatively tolerant of disturbances. Power supply lines are never routed across storage inductors, whose circulating current values are critical to the operation of RSFQ logic. Furthermore, the stress placed on each JTL stage by magnetic coupling is minimized by the use of filamentary power distribution, the concept of which is illustrated in Figure 10-14. In this hypothetical example, power is supplied to eight RSFQ circuits from a common supply. If a single power supply line were used to cross the long JTL which surrounds the eight RSFQ circuits, the value of the supply current at the signal crossover would equal the current drawn by all eight circuits. If the eight circuits are fairly complex, this value of current might be large enough to disturb the JTL magnetically at the point of crossover. A better approach is to cross the JTL at several points along its length with a number of filaments connected to the main supply line. In the example shown in the figure, the value of current in each filament crossing the JTL equals the total current drawn by two RSFQ circuits. Therefore, the stress placed on a single JTL stage by magnetic coupling is reduced by a factor of four. If necessary, the stress on each JTL stage

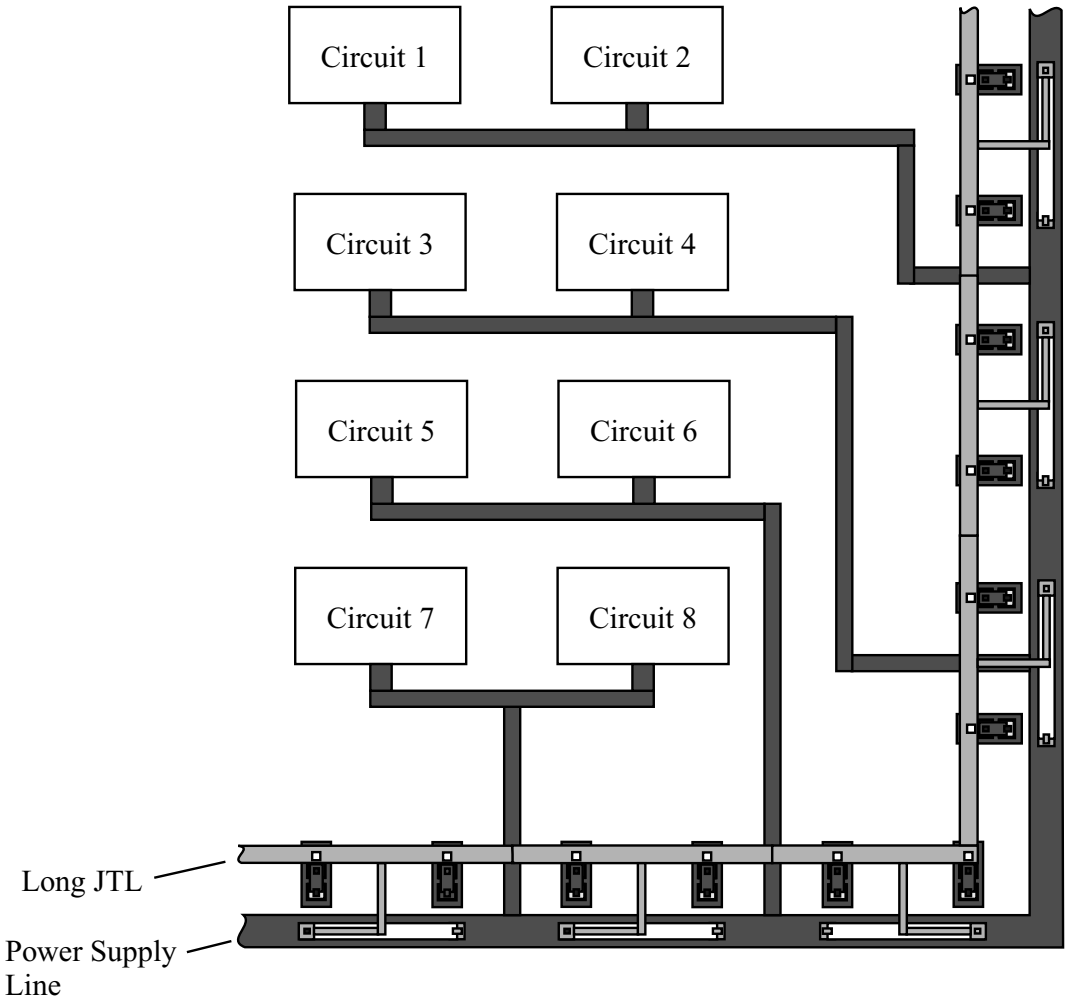


Figure 10-14: Example of filamentary power distribution.

could be reduced further by increasing the number of filaments that cross the JTL. The number of filaments employed in the power supply grid of the modulator test chip is large enough that the maximum supply current crossing a single JTL stage is less than 8 mA, even though the supply currents at the pads of the chip are as high as 95 mA. Experience has shown that crossovers carrying less than 10 mA of supply current do not degrade JTL margins noticeably [190]. Several examples of filamentary power distribution can be seen in the 1:4 DEMUX layout shown in Figure 10-13.

Another consideration in routing signal and supply lines is not specific to Josephson technology but is important for any mixed-signal circuit: isolation of sensitive analog circuits from noise generated by large digital circuits. While interference from the digital circuits is mitigated by the small signal levels of RSFQ logic, the high sensitivity of the superconducting bandpass $\Delta\Sigma$ modulator justifies the use of good isolation techniques. The supply lines that deliver power to the bandpass modulator and the JTL amplifier for the sampling clock are routed so that they do not cross the power supply lines of the large digital circuit blocks. No wires of any kind cross the signal path (including the microstrip

resonator) which connects the analog input to the SFQ comparator of the bandpass modulator. The pad for the analog input and the pads for the two high voltage (2 mV) digital outputs are located on different sides of the test chip.

As discussed in Chapter 6, ground plane holes and moats are often used to protect Josephson circuits from trapped magnetic flux. In accordance with the recommendations of Robertazzi [126], large and numerous holes and moats are etched in the ground plane of the modulator test chip. It is important, though, not to remove ground plane underneath signal and power lines so that return currents are not disturbed.

Sixteen copies of the modulator test chip were fabricated at HYPRES, Inc., with special processing for the integrated MSM photodiodes [39]. Figure 10-15 shows a micrograph of the fabricated test chip. The chip employs 4065 Josephson junctions, and its size (6.3 mm $\times$ 6.3 mm) and pad layout are chosen to fit the cryogenic sample holder. The test chip uses all but two of the 64 pads visible in the micrograph. The majority of the pads are used for connecting 22 independent current sources (and their associated grounds) to the supply lines and ground plane of the test chip. The total current drawn from all the sources is 820 mA. Not counting the optical power incident on the MSM photodiode, on-chip power dissipation is about 1.9 mW. When the test chip is triggered by the 20.6 GHz optical clock, the average optical power incident on the MSM photodiode is about 1.1 mW. To protect them from heat generated by the incident light, all Josephson circuits are located at least 600 μm away from the MSM photodiode. The transmission line resonator of the bandpass $\Delta\Sigma$ modulator is implemented as a microstrip structure between the M2 layer and the M0 ground plane. With a width of 70 μm, the transmission line impedance Z_0 is 1 Ω and matches the value used in the circuit simulations of Chapter 8. With a length of 1 cm, the propagation delay T_d of the transmission line is nominally 97 ps, which is 3% smaller than the value of T_d used in the circuit simulations. This adjustment is made so that when the experimental modulator is triggered by the 20.6 GHz optical clock, the ratio of center frequency to sampling rate matches that of the simulated circuit at a 20 GHz sampling rate. As evident in the test chip micrograph, the microstrip line is laid out with nine right-angle bends in order to fit into the available space. Each of these bends is compensated for minimal reflection by cutting the outside corner with a 50% chamfer, in accordance with standard microwave engineering formulas [191]. To achieve highest operating speed, the large digital circuits are arranged so that all high speed (i.e., multi-GHz) communications between blocks are local. For this reason, there is a close correspondence between the physical layout and the functional block diagram of Figure 10-1.

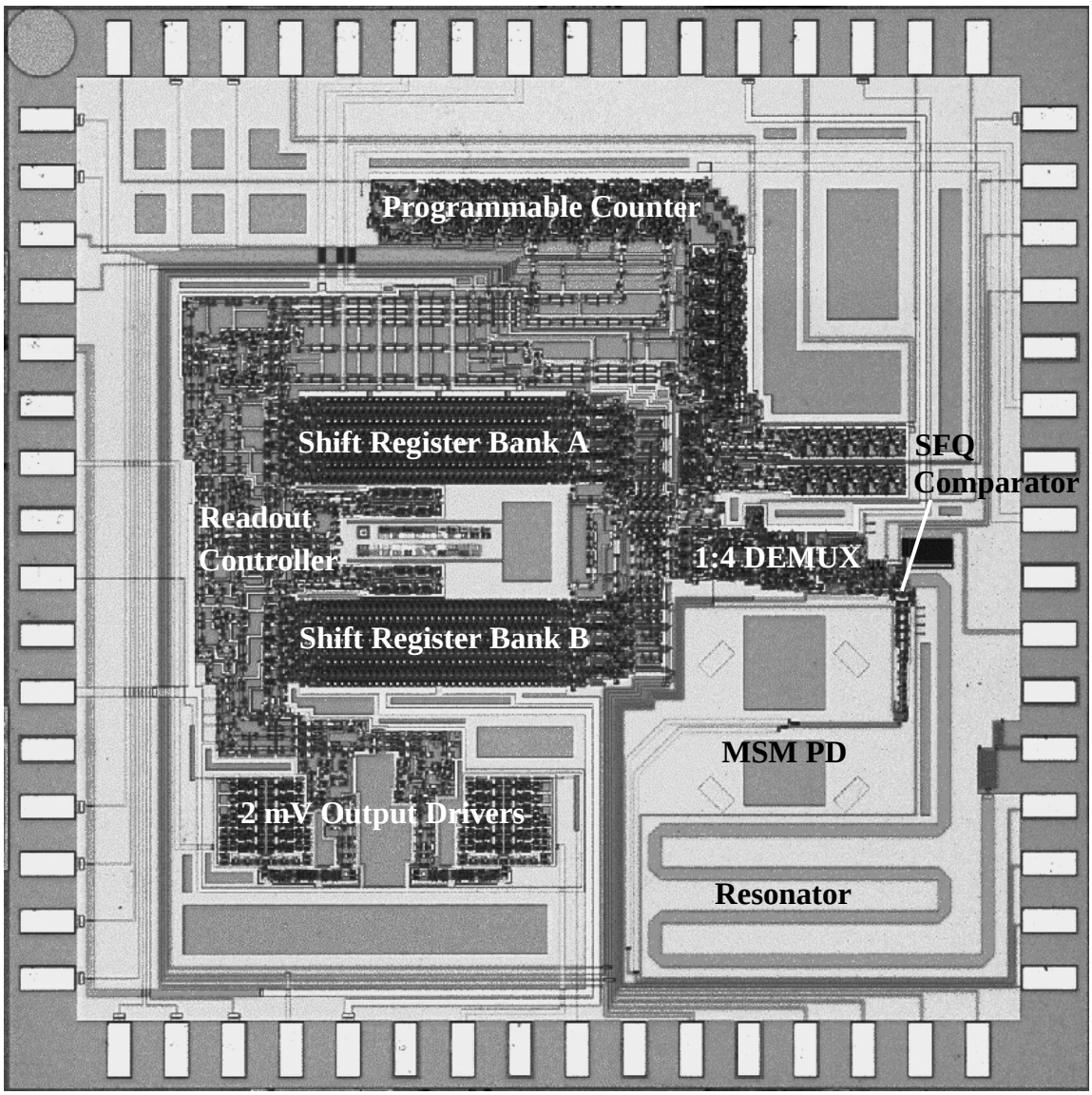


Figure 10-15: Micrograph of modulator test chip.

Chapter 11

Test System for Superconducting Circuits

A wide variety of laboratory equipment is used for experimental evaluation of the modulator test chip described in the last chapter. The optical clocking setup used for external triggering of the modulator at 20.6 GHz was already detailed in Chapter 5, and its usage with simple Josephson circuits was demonstrated in Chapter 6. This chapter focuses on the room-temperature electronics employed for testing complex RSFQ circuits such as the modulator test chip. Because Josephson circuits operate with small voltage levels and are sensitive to noise, custom hardware is usually required to interface these circuits with standard test instrumentation [192, 193]. The low frequency (<10 kHz) and high frequency (160–350 MHz) interface circuits are discussed in different sections of the chapter. The final section of the chapter explains the diagnostic capabilities provided by the test system software.

An important feature of the custom hardware constructed for this project is the use of optically isolated grounds for controlling the flow of return currents in the ground plane of the superconducting chip. The flow of ground plane return currents can be controlled to reduce their magnetic coupling to the Josephson circuits. This topic, which has only recently been discussed by other researchers [189, 194], is examined later in the chapter, after a description of the overall test system.

11.1 Overall Test System

Figure 11-1 depicts the major components of the test system used for experimental evaluation of the modulator test chip. The test system is logically divided into a low frequency part and a high frequency part. The low frequency part provides dc bias currents and low frequency control signals (such as the 11 currents used to configure the programmable counter) to the Josephson circuitry. In addition, this part of the setup affords comprehensive diagnostic testing of the large digital circuits on the test chip, so that each die can be screened for functionality before proceeding with high speed testing. The high frequency part of the setup supplies the 20.6 GHz optical clock and the analog input (near 2 GHz) to the bandpass modulator and measures the DATA and START outputs of the test chip during high speed testing.

Most of the functions used during low frequency diagnostic testing are implemented in software, by programming an IBM Intellistation Personal Computer (PC) with a 500 MHz

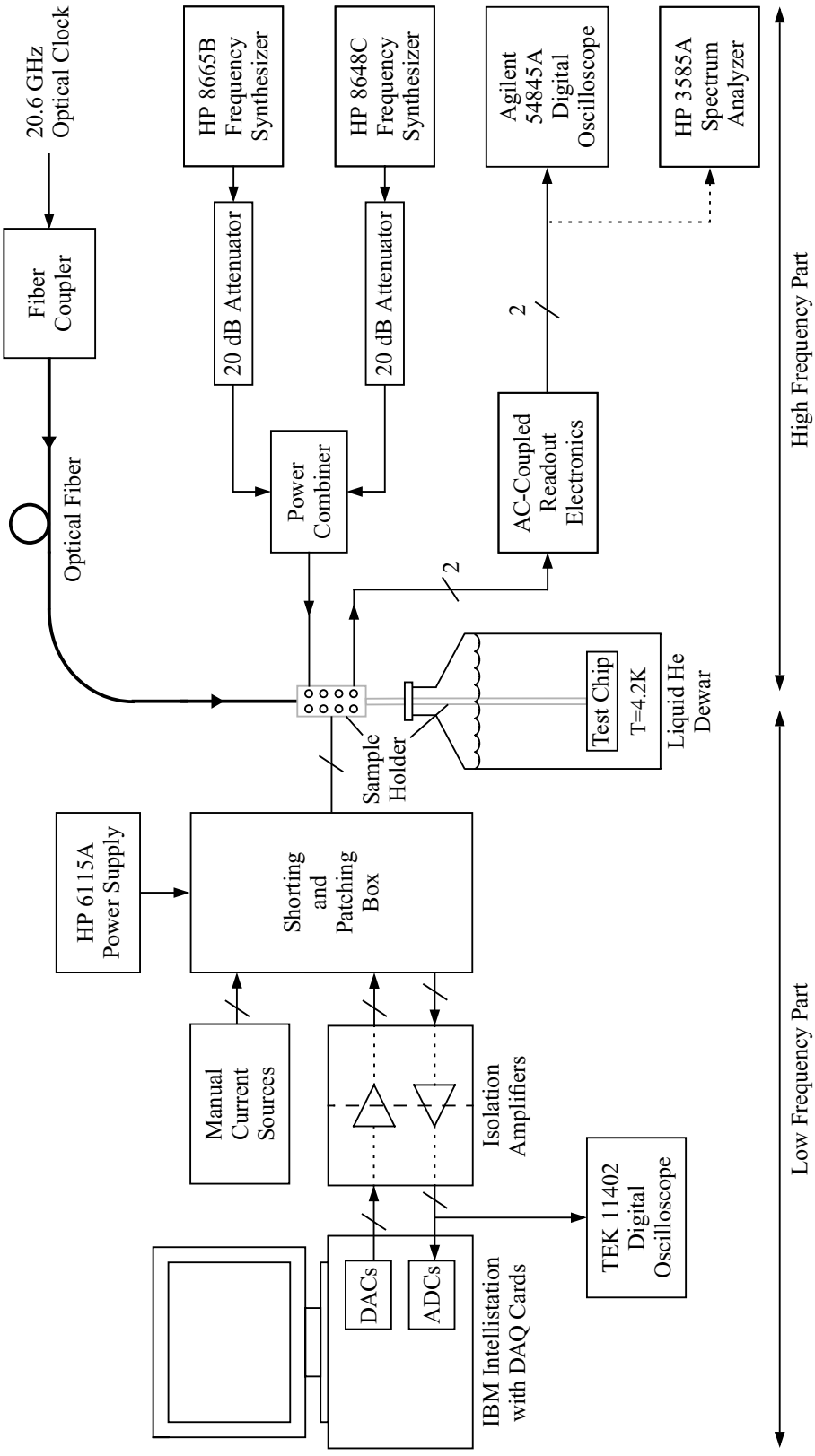


Figure 11-1: Test setup for the superconducting bandpass $\Delta\Sigma$ modulator.

Pentium III microprocessor. The computer is interfaced with the laboratory setup through two data acquisition (DAQ) cards installed in its PCI slots; these two cards (National Instruments PCI-MIO-16E-4 and PCI-6704) are equipped with a total of 34 analog outputs and 8 differential analog inputs. An important consideration in automated testing of a superconducting chip is protecting the sensitive Josephson circuits from noise generated by the computer [192]. In this work, the Josephson circuitry is protected from such noise by placing optically-coupled isolation amplifiers between the analog inputs and outputs of the DAQ cards and the rest of the experimental setup. Further protection against radio frequency interference (RFI) is provided by adding ferrite beads to the electrical cables connected to the cryogenic sample holder. The optically-coupled isolation amplifiers are linear in operation, so the currents delivered to the test chip are proportional to the analog outputs of the DAQ cards, and the analog inputs of the DAQ cards are proportional to the output voltages generated by the Josephson circuits. The proportional control allows the dc bias currents and control current levels to be adjusted in software by writing different values to the analog outputs of the DAQ cards. All 34 analog outputs of the DAQ cards are employed in the experiment. A couple of these outputs are used to synthesize low frequency (typically, 2 kHz) pulse patterns which trigger the diagnostic inputs of the test chip during functionality testing of the large digital circuits; the rest of the analog outputs are used to set dc bias and control currents for the Josephson circuits. Functionality of each test chip is determined by measuring its four outputs (DATA, START, and the two diagnostic outputs which monitor LOADA and LOADB) with the analog inputs of the DAQ cards and comparing them (in software) with the expected output patterns. If an error is detected by the test software, the problem can be manually inspected by recording the output waveforms of the Josephson circuits with a Tektronix 11402 digital oscilloscope.

In addition to the 34 current sources controlled by the PC, the experimental setup includes 7 current sources which are manually adjusted with 10-turn potentiometers; the potentiometers have calibrated dials so that their settings can be recorded. These battery-powered sources have noise levels better than 90 dB below their maximum output currents and are primarily used to provide power to the most sensitive circuits on the test chip, such as the bandpass modulator and the JTL amplifier for the sampling clock. A Hewlett-Packard 6115A precision power supply provides the bias (typically, 5 V) for the MSM photodiode when the chip is being optically clocked. All of the low frequency connections to the test chip are made through a shorting and patching box. Inside this box is a circuit board with jumper wires connecting the low frequency electronics of the test system to the pins of the Josephson chip. This circuit board is removable; by replacing it with a circuit board having a different set of jumper wires, the system can be reconfigured for testing other Josephson chip designs (with different pinouts). Such reconfigurability has been used, for example, in testing the 1:4 DEMUX diagnostic circuit that is presented and discussed in Section 12.1. Mechanical toggle switches on the front panel of the shorting and patching box are used to short all of the wiring to earth ground when connecting the electrical cables to the cryogenic sample holder; such grounding reduces the chance of damaging the Josephson chip with electrostatic discharge (ESD). Other toggle switches on the front panel are used to disconnect the pins of the Josephson chip from the room-temperature electronics; this feature is used during the slow cooldown procedure described in Section 6.1.3 to ensure that no currents (including those due to thermoelectric effects) flow to the chip which might induce flux trapping. These functions of the toggle switches are identical to the functions

of the relays in the test system developed at SUNY Stony Brook [193].

The modulator test chip is placed in the cryogenic sample holder, which is inserted into the magnetically shielded liquid helium dewar described earlier in Section 6.1.3. The picosecond optical pulses from the optical clocking setup are delivered to the superconducting chip via single-mode fiber. Alignment between the single-mode fiber and the MSM photodiode is maintained by gluing a glass capillary and quartz spacer to the test chip, as explained previously in Section 6.1.2.

Low-loss coaxial cables with 50 Ω characteristic impedance and SMA connectors are used to connect high frequency test instruments to the cryogenic sample holder. Hewlett-Packard 8665B and 8648C frequency synthesizers[1] are used to generate the analog input for the superconducting bandpass $\Delta\Sigma$ modulator. For single-tone tests of the modulator, only one synthesizer is used; for two-tone IM distortion tests, the signals from the two synthesizers are coupled together with a broadband, resistive power combiner (Picosecond Pulse Labs 5330A). The insertion of 20 dB attenuators between the synthesizers and the power combiner suppresses interactions between the synthesizers which can generate IM distortion. Since the insertion loss of the power combiner is 6 dB, the output of each synthesizer is attenuated by 26 dB before it reaches the coaxial cable connected to the input pin of the modulator test chip. In order to ensure accurate measurement of the input sensitivity of the bandpass modulator, the losses of the input cable and connectors (including the section of cable inside the sample holder itself) were calibrated out with a Hewlett-Packard 8753A network analyzer.

The ac-coupled readout electronics, which are presented in Section 11.3, amplify the DATA and START outputs of the test chip up to signal levels (≈ 100 mV) which are easily measured with standard high frequency test equipment. For this laboratory demonstration, no custom hardware was built to capture and process the digital data being read out from the modulator test chip. Instead, the amplified outputs of the test chip are recorded in a single-shot manner with an Agilent 54845A digital oscilloscope. The high sampling rate of this oscilloscope (8 GHz on two channels simultaneously) is more than adequate for faithful capture of the output data, whose maximum readout rate is only about 350 Mbit/s. An advanced triggering function of the oscilloscope is used to synchronize waveform acquisition with the missing pulses on the START output (recall Figure 10-12(b)). While the high speed memory of the oscilloscope captures each single-shot waveform record in real-time, transfer of the data from that memory to the internal hard drive of the oscilloscope is much slower and severely limits the number of waveform records that can be stored in a given measurement time. Consequently, measurement times for segmented correlation are orders of magnitude longer than those listed earlier in Table 9.1, which assumed that the data bits being read out from the test chip would be processed in real-time by custom hardware, so that all of the 256-bit sequences captured with the on-chip acquisition memory would contribute to the segmented correlation estimates. Because the sampling oscilloscope only captures a very small fraction of the 256-bit sequences read out from the on-chip acquisition memory, segmented correlation measurements for estimating the autocorrelation function $R[n]$ up to large values of n are not practical with the present experimental setup, even though the test chip design allows M, the number of data bits skipped between loading of the

[1]Two different models of synthesizers were used in the experiment not because of differences in their performance, but simply because they were the ones available for this project.

shift register memory banks, to be programmed to a value as large as 8060. Nonetheless, enough data can be acquired with the sampling oscilloscope for more modest segmented correlation measurements, in which $R[n]$ is estimated only up to $n = 511$.

After the experimental measurements are completed, the waveform records stored on the hard drive of the Agilent 54845A oscilloscope are uploaded to an IBM RS/6000 workstation and then converted to binary output codes by software programs written in C and MATLAB. Additional MATLAB programs are used to apply windows and FFTs to these output codes, as well as calculate the segmented correlation estimates. The flexibility afforded by recording the output waveforms with a sampling oscilloscope and analyzing the data in software is particularly beneficial for a first laboratory demonstration, as the data processing routines can be easily modified to accommodate experimental conditions (e.g., sampling rate) which differ from those originally anticipated. On the other hand, the long measurement latency (at least several minutes) introduced by post-processing of the output data on a remote computer is a major disadvantage when debugging the modulator test chip. During debugging, the DATA output of the test chip is connected to a Hewlett-Packard 3585A spectrum analyzer, which provides a real-time display of the output spectrum of the bandpass modulator. Since the spectrum analyzer operates in the analog domain, the spectrum measured in this manner is sensitive to the shapes of the pulses on the DATA output and is easily degraded by various types of waveform distortion, such as that due to unequal rise and fall times. Such a measurement is therefore not suitable for quantitative analysis of modulator performance, but the ability to provide qualitative information about modulator operation in real-time is invaluable when adjusting circuit parameters for proper functionality. Since the readout rate of the modulator test chip equals $f_s/128$, the spectrum measured with this analog technique is a frequency-scaled version of the modulator output spectrum. Therefore, suppression of the quantization noise at quarter-wave resonance (near 2.1 GHz) appears as a reduction of noise at 2.1 GHz/128=16.4 MHz, well within the 40 MHz range of the 3585A spectrum analyzer.

An analog spectrum analyzer can also be used to monitor the START output of the test chip. Ignoring the missing pulses that denote assertion of the START bit, the START output is a square wave with a frequency of $f_s/128$. Since an on-chip frequency divider generates this square wave from the sampling clock, the frequency stability of the sampling clock can be monitored by measuring the spectral linewidth of the square wave on the START output. Such monitoring is especially useful when the bandpass modulator is triggered by the on-chip Josephson oscillator, whose frequency stability is a sensitive function of dc bias currents. In the experiments discussed in the next chapter, the frequency of the square wave on the START output ranges from approximately 160 MHz to 350 MHz and is too high for the 3585A spectrum analyzer. Therefore, a higher frequency spectrum analyzer (Hewlett-Packard 8568B) is used to measure the linewidth of this signal.

11.2 Low Frequency Electronics

11.2.1 Management of Ground Plane Currents

The grounding of the test system is an important consideration in the design of the room-temperature electronics which supply dc bias currents and low frequency control currents to the Josephson circuits. Because the return currents flowing through the superconducting

ground plane can couple magnetically to the Josephson circuits on the test chip, it is desirable that the physical distribution of such currents be managed for minimum disturbance of the active circuitry [189, 194]. As now demonstrated, the physical distribution of the ground plane return currents is heavily influenced by the grounding of the external test electronics.

In general, the return current in the superconducting ground plane follows the path of least inductance, under the constraint that the currents at the ground pads are those dictated by the grounding of the external setup. Figure 11-2 presents an illustrative example in which two current sources are used to provide power to two different circuits on a Josephson chip. In the figure, the gray arrows indicate the flow of return current for source 1 when (a) the sources have isolated grounds and (b) the sources share a common ground. In the first case, all of the return current flows back to the ground pad connected to source 1. Because this current follows the path of least inductance, its physical distribution in the ground plane is localized underneath the supply lines which deliver power to circuit 1. Since the magnetic fields generated by the supply and return currents are largely confined inside the microstrip structures formed by the supply lines above the ground plane, the magnetic disturbance of nearby Josephson circuits is minimal. The stray magnetic fields are larger near the pads, where the separation between the supply current and return current is inevitably larger (but is minimized by the use of adjacent pads). To avoid coupling to these fields, the Josephson circuitry should not be located too close to the pads.

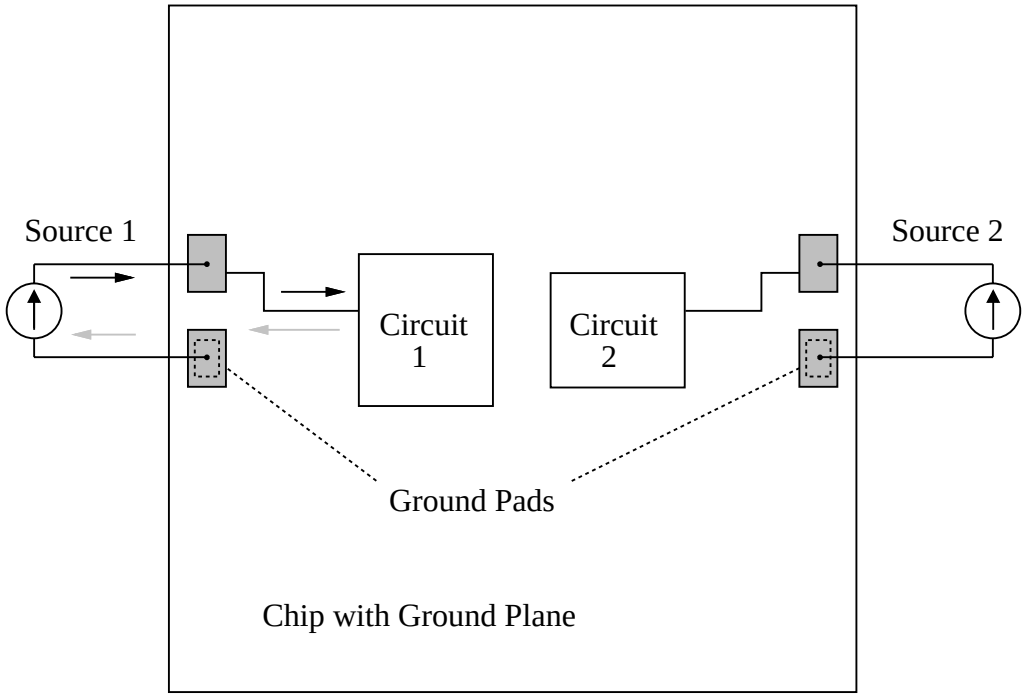
In the second case, the return current for source 1 flows back to both pads connected to the common ground. The proportion of the return current flowing into each ground pad of the Josephson chip depends on the relative values of parasitic resistances R_{p1} and R_{p2}. In most experimental setups, the parasitic resistances of the ground return lines are comparable, so about half the return current for source 1 flows into each ground pad. Part of the current returning to the right pad flows through or near circuit 2, magnetically disturbing it. Such undesirable coupling, which has been recently demonstrated experimentally [189], is difficult to avoid when a superconducting integrated circuit is powered by multiple sources sharing a common ground, as is the case with the Josephson test systems described in [192, 193].

In this project, the sources which supply bias currents and control currents to the modulator test chip have isolated grounds so that the return currents flow through the superconducting ground plane in the manner suggested in Figure 11-2(a). While each isolated source can be implemented as a battery with a series resistor for setting the value of current, such a source is not amenable to computer automation. Computer-controlled current sources with isolated grounds are realized with optically-coupled isolation amplifiers, as explained next.

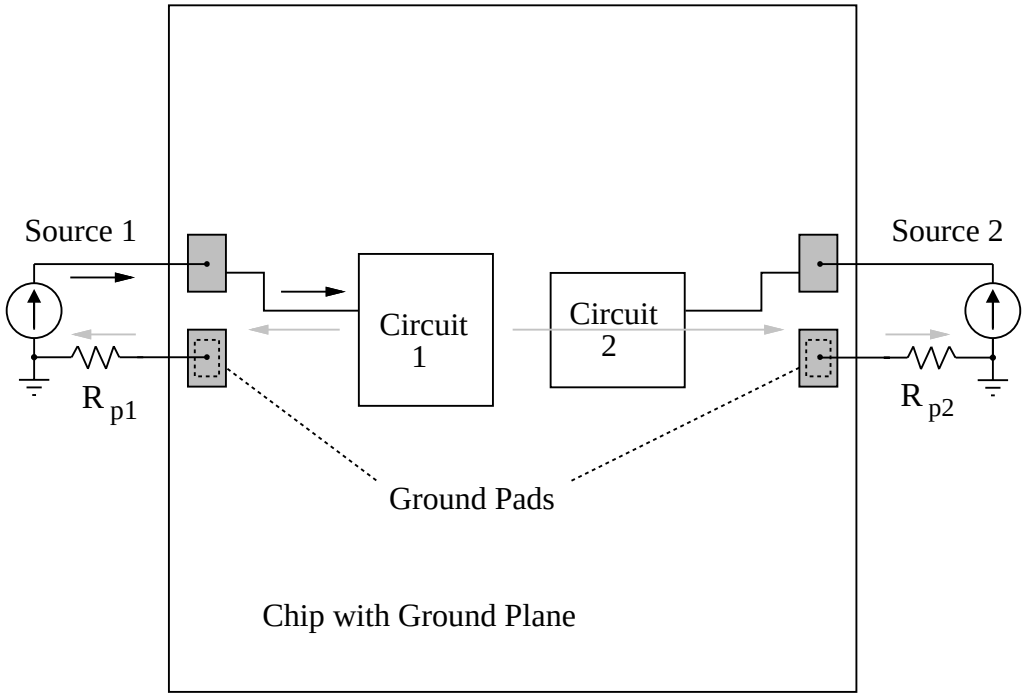
11.2.2 Optically-Isolated Current Sources

As mentioned earlier, the 34 analog outputs of the DAQ cards installed inside the computer are connected to optically-coupled isolation amplifiers. The optical isolation not only protects the Josephson circuitry from electrical noise generated by the computer but also allows each output channel to have a separate ground, as indicated in Figure 11-3. The circuits on the output side of the isolation barrier are powered from separate battery supplies in order to maintain electrical isolation between channels.

Ideally, each of the 34 output channels would have a separate ground, which would be



(a)



(b)

Figure 11-2: Ground plane current flow with (a) isolated sources and (b) sources sharing a common ground.

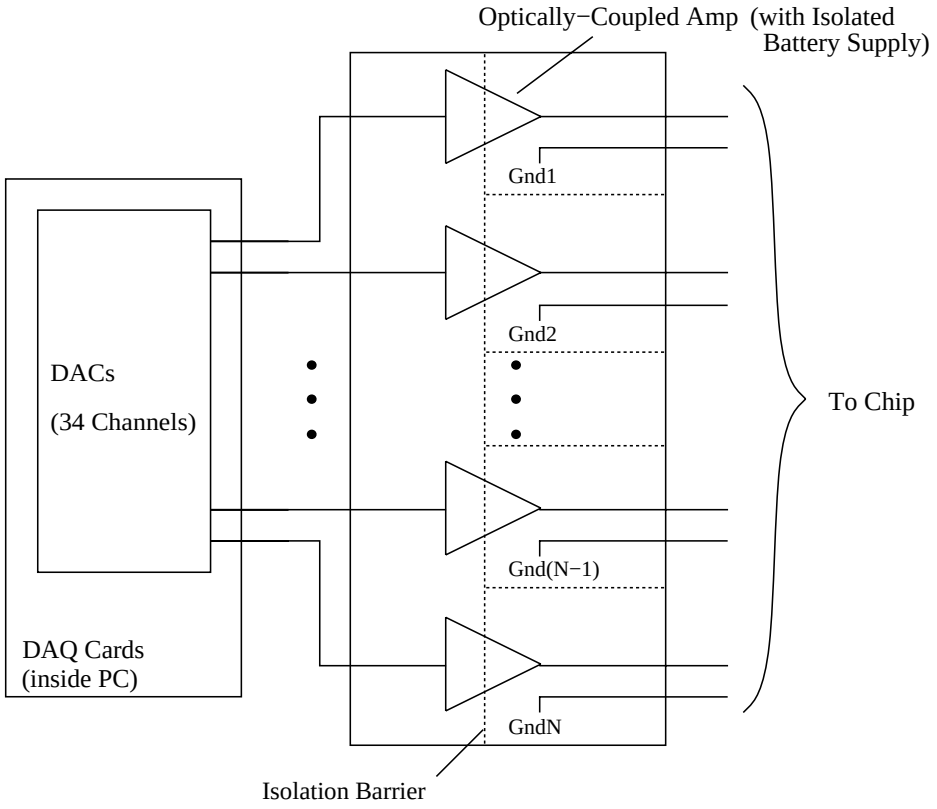


Figure 11-3: Computer-controlled current sources with optical isolation of individual channels.

connected with its own pad to the superconducting ground plane of the test chip. However, the limited number of pads contacted by the cryogenic sample holder renders such an approach impractical. In fact, the modulator test chip uses only 12 ground pads for sinking the return currents of all low frequency sources. These 12 ground pads are spatially distributed along the four sides of the test chip, and each one handles the return currents of the sources connected to pads in its vicinity, ranging in number from 1 to 6. Since there are only 12 external connections available for the return currents, there is no benefit in using a separate ground for each of the 34 computer-controlled current sources in the experimental setup. Instead, the 34 sources are divided into 16 groups, each of which has a separate ground. Sources within each group share the same ground and can therefore be powered from the same battery supply, reducing the number of separate battery supplies used in these current sources from 34 to 16. The 16 separate grounds of the computer-controlled current sources are connected to 12 ground pads of the test chip with jumper wires on the circuit board inside the shorting and patching box.

The optically-coupled isolation amplifier, whose schematic is shown in Figure 11-4, is a standard application circuit for the Infineon IL300 linear optocoupler [195]. The IL300 consists of an infrared light-emitting diode (LED) illuminating a matched pair of galvanically isolated photodiodes. One photodiode, with photocurrent I_{P1}, is connected to the input circuit and provides a feedback signal to the op-amp whose output voltage controls the drive current of the LED. This servo loop regulates the optical output of the LED so that I_{P1}

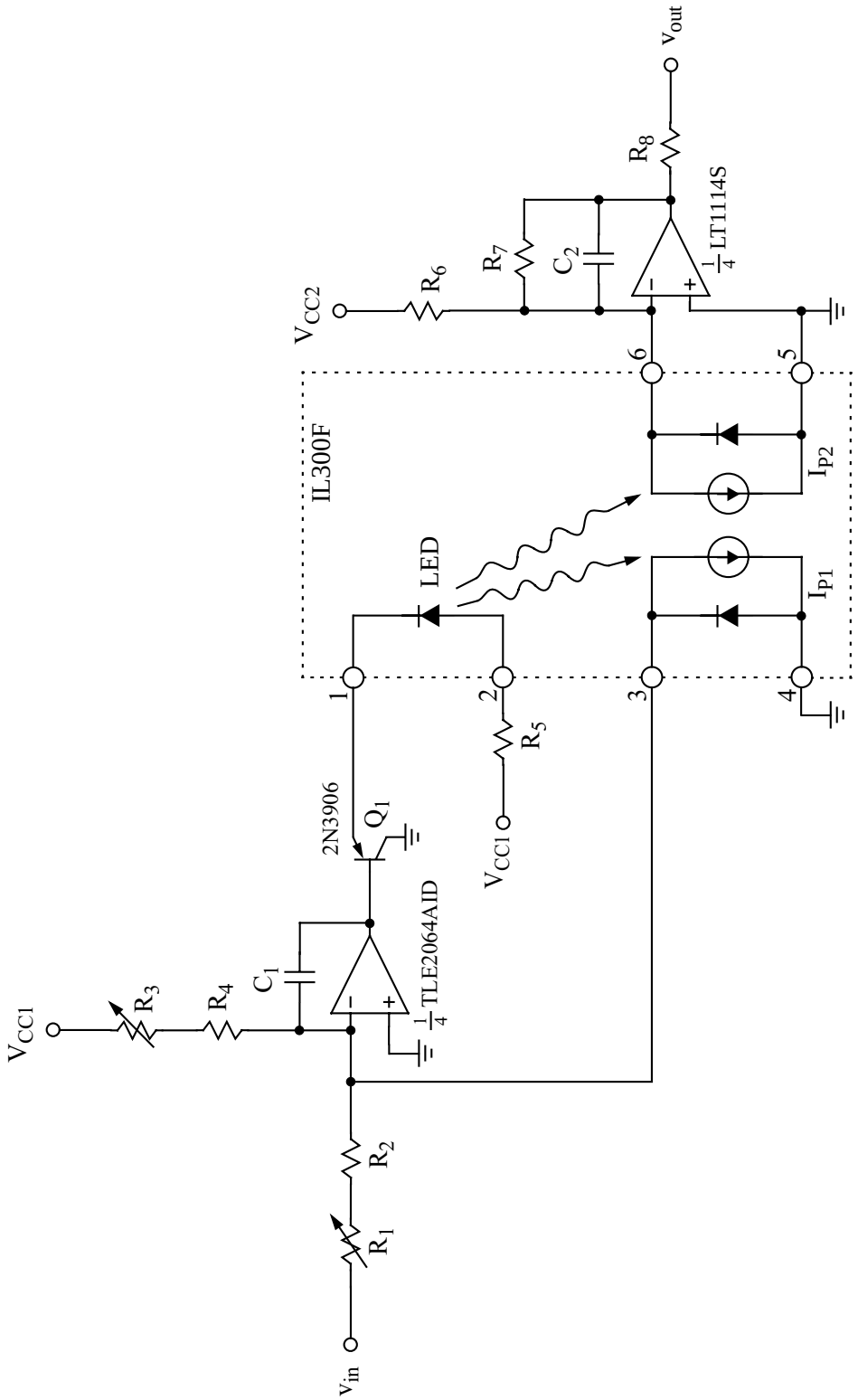


Figure 11-4: Optically-coupled isolation amplifier. The circuit parameters are: R_1= 100 kΩ (10T), R_2=365 kΩ, R_3=100 kΩ (10T), R_4=332 kΩ, R_5=649 Ω, R_6=432 kΩ, R_7=412 kΩ, R_8=2 kΩ, C_1=27 pF, C_2=15 pF, V_{CC1}=12 V, and V_{CC2}=13.8 V.

is a linear function of the input voltage v_{in} and independent of the LED's characteristics, which vary with temperature and time (due to aging). Since the photodiodes are matched, photocurrent I_{P2} accurately tracks I_{P1}. The op-amp on the output side of the isolation barrier converts photocurrent I_{P2} to an output voltage which is linearly related to v_{in}.

The photocurrents I_{P1} and I_{P2} are inherently unipolar signals. Bipolar operation of the isolation amplifier is achieved by prebiasing the input circuit so that the LED and photodiodes operate from a quiescent operating point with positive values of I_{P1} and I_{P2}. The bias is introduced by adding a dc current equal to $V_{CC1}/(R_3 + R_4)$ into the summing junction of the input op-amp. This bias is compensated in the output signal by adding a dc current equal to V_{CC2}/R_6 into the summing junction of the output op-amp. In order to obtain low offset drift and high accuracy ($\approx 0.1\%$), voltages V_{CC1} and V_{CC2} are generated with precision regulators (Linear Technology models LT1085-12 and LT1020, respectively). Regulation of V_{CC2} is particularly important since the output circuit is powered from 9 V lithium batteries (connected in series), whose voltages slowly drop as they discharge. The gain and offset of the isolation amplifier are adjusted with potentiometers R_1 and R_3 so that $v_{out} = v_{in}$ up to voltages of ± 10 V (with the output unloaded). Precision (0.1%) resistor R_8 is used to set the output current delivered into a short circuit load, which is a good approximation for a low impedance Josephson circuit. With R_8=2 kΩ, the full-scale output of the computer-controlled current source is ± 5 mA. Other circuit parameters are listed in the figure caption.

The optically-coupled isolation amplifiers placed between the outputs of the Josephson chip and the analog inputs of the DAQ cards are implemented with almost identical circuitry. The only changes made to the design are modifications for higher gain. An instrumentation amplifier (Analog Devices AMP01FX) set for a gain of 1000 is added as a low-noise preamplifier stage in front of the servo loop for the LED. The gain is further increased by reducing the values of resistors R_1 and R_2 by a factor of two. With these modifications, the total gain is 2000 – sufficient for amplifying the low voltages (100–200 μV) on the diagnostic outputs of the modulator test chip up to signal levels (> 200 mV) which can be accurately measured with the DAQ cards.

11.2.3 Booster Amplifier

The output currents (up to ± 5 mA) directly provided by the optically-coupled isolation amplifiers are sufficient to drive the diagnostic inputs of the modulator test chip, to control the switches in the programmable counter, and to power the smaller Josephson circuits (with less than 40 junctions). Larger current sources for powering more complex Josephson circuits are realized by connecting the outputs of the isolation amplifiers to booster amplifiers, such as the one shown in Figure 11-5. This voltage-controlled current source is similar to a design described in [196] but simplified for unipolar operation. The booster amplifier operates from a single positive supply (V_{CC}), generated by connecting six AA alkaline batteries in series. Each booster amplifier in the test setup has its own separate battery supply so that electrical isolation between channels is preserved. The input buffer op-amp (Analog Devices AD820BN) and the precision difference amplifier (Burr-Brown INA132P) are well suited for such single-supply applications [197, 198]. Since the optically-coupled isolation amplifier has an output resistance of 2 kΩ, its unloaded full-scale output voltage of ± 10 V is reduced to ± 1 V by the loading of input resistor R_{in}=223 Ω. The booster amplifiers are not ordinarily used with negative input voltages, which are clamped to ≈ 0 V by

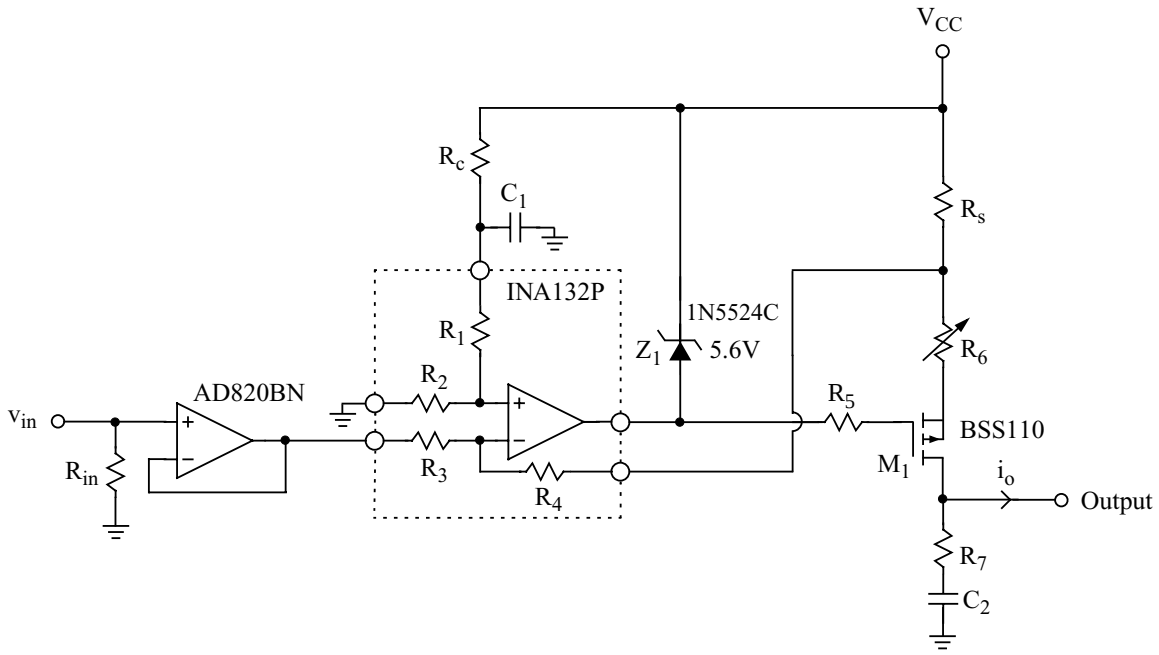


Figure 11-5: Booster amplifier for sourcing currents up to 50 mA. The circuit parameters are: R_{in}= 223 Ω, R_1=R_2=R_3=R_4=40 kΩ, R_5=100 Ω, R_6=100 Ω (15T), R_7=1 kΩ, R_s=R_c=20 Ω, C_1=0.047 μF, C_2=6800 pF, and V_{CC}=6–9 V.

clipping of the AD820BN op-amp and result in minimal output current. The 0–1 V output of the AD820BN is compared with the voltage drop across current-sensing resistor R_s by the INA132P difference amplifier, whose output drives the gate of M_1, a p-channel power MOSFET (Fairchild BSS110). Through negative feedback, the current flowing through M_1 is adjusted until the error between these two voltages is nulled. Since the drain and source currents of a MOSFET are identical, the output current i_o is proportional to the voltage drop across R_s and, therefore, to v_{in}.

The output of the booster amplifier is connected to the superconducting circuit through long wires with substantial inductance, whose impedance rises with frequency. An output filter formed by R_7 and C_2 limits the high frequency impedance at the drain of M_1 so that parasitic oscillations are avoided. The transient response is well damped for load inductances up to 80 μH. Zener diode Z_1 clamps the output voltage of the INA132P (by tripping its current limit) so that M_1 cannot be driven to produce an output current much larger than full-scale, even on a transient basis. Potentiometer R_6 is adjusted so that i_o is about 13% higher than that corresponding to a full-scale input when the Zener diode clamp is activated. The Zener diode clamp is included in the design as a precautionary measure; it is not activated if proper experimental procedures are followed (so that, for instance, the output of the booster amplifier is never open-circuited).

The on-chip resistors (R_1 through R_4) of the INA132P are laser-trimmed [198] for accurate gain and high common-mode rejection (> 76 dB). The high common-mode rejection helps ensure that the output current of the booster amplifier is nearly independent of the supply voltage V_{CC}. The use of compensation resistor R_c also improves the power supply rejection of the booster amplifier. Assuming that the op-amps are ideal and that

R_1=R_2=R_3=R_4, the dc output current of the booster amplifier is related to v_{in} and V_{CC} by

$$i_o = \left(\frac{1}{R_s} + \frac{1}{R_1}\right) v_{in} + \left(\frac{\frac{R_c}{R_s} - 1}{2R_1 + R_c}\right) V_{CC}. \tag{11.1}$$

Note that i_o is only independent of V_{CC} if R_c=R_s. Because the value of R_1 is much larger than that of R_s (or R_c), the component of i_o due to V_{CC} is negligible if R_c is matched within 1% of R_s. With such matching, Equation 11.1 can be approximated as

$$i_o \approx \left(\frac{1}{R_s} + \frac{1}{R_1}\right) v_{in} \approx \frac{v_{in}}{R_s}. \tag{11.2}$$

The excellent power supply rejection of the booster amplifier allows it to operate from an unregulated battery supply; as the batteries discharge, and V_{CC} drops from 9 V to 6 V, the output current changes by less than 0.1% of full-scale.

For the circuit parameters listed in the caption of Figure 11-5, the full-scale output current (with v_{in} = 1 V) equals 50 mA. The full-scale output current is easily set to other values by changing resistances R_s, R_c, and R_6. In total, 17 booster amplifiers are used to power the modulator test chip, with full-scale output currents ranging from 14 to 125 mA. For booster amplifiers with full-scale output currents in excess of 60 mA, output transistor M_1 is implemented as two BSS110 MOSFETs wired in parallel in order to observe rated device limits on power dissipation; hand-selection of the two MOSFETs for best matching ensures nearly equal sharing of the output current.

11.3 AC-Coupled Readout Electronics

Figure 11-6 presents the ac-coupled readout electronics used for detecting the DATA output of the modulator test chip at high speed (f_s/128 = 160–350 Mbit/s). All of the broadband coaxial components were purchased from Picosecond Pulse Labs (PSPL) [199]. A bias tee is used to inject dc current (I_B in Figure 10-11) which biases the series array of DJ SQUIDs in the high voltage (HV) output driver of the test chip. (The risetime filter, whose function is discussed in the next paragraph, acts as a simple wire for dc currents.) The use of the same wire for biasing and reading out the DJ SQUIDs reduces the number of pads required for operating the HV output driver. The bias current generates small dc voltage drops along the coaxial cable connected to the HV output driver, but the ac-coupled amplifiers are insensitive to such voltages. A simple resistive network is used to derive the bias current ($\approx$ 300 μA) from a 5 V bandgap voltage reference (Analog Devices REF195), which is powered from a 9 V lithium battery. The bias current is manually adjusted with 10-turn potentiometer R_1 so that the output swing of the HV output driver is maximized.

Two cascaded amplifiers increase the 2 mV output of the HV output driver up to signal levels ($\approx$ 100 mV) which are easily measured with standard high frequency test equipment. The combined bandwidth of the cascaded amplifiers is about 1.5 GHz. The 5810B amplifier has a noise figure of 5 dB, and its high input return loss ($>$ 30 dB up to 1.5 GHz) helps ensure that little signal energy is reflected back to the modulator test chip – an important consideration, as the impedance of the series array of DJ SQUIDs in the HV output driver is too low and nonlinear to provide effective source termination of a 50 Ω coaxial cable. The input return loss of the 5810B amplifier rapidly declines at frequencies above 1.5 GHz;

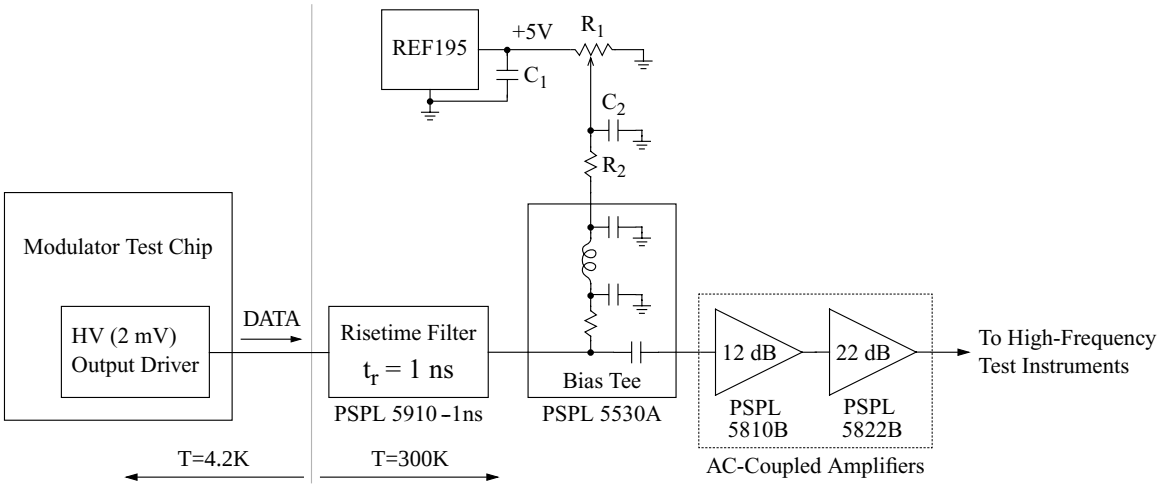


Figure 11-6: DATA output of test chip connected to ac-coupled readout electronics.

reflections in this frequency range are reduced by inserting a risetime filter between the HV output driver and the bias tee. The risetime filter is a low-pass filter whose time domain response is optimized for processing digital pulse streams. The PSPL design filters by absorption [199], so that frequency components of the input signal above the cutoff frequency ($f_c = 0.35/t_r = 350$ MHz) are internally absorbed in resistive elements and not reflected back toward the source. Since the filtered signal arriving at its input contains negligible energy above 1.5 GHz, the input return loss of the 5810B amplifier at such high frequencies is irrelevant to the operation of the readout channel.

The ac-coupled readout electronics used for detecting the START output of the modulator test chip are identical to those just discussed, except that the risetime filter is replaced by one (PSPL 5915-500ps) with half the value of t_r (and twice the cutoff frequency). Since the pulses on the START output have half the width of those on the DATA output, they require twice the bandwidth for distortion-free transmission.

11.4 Test System Software

The test system software running on the PC was written using the National Instruments LabWindows/CVI package, an integrated ANSI C development environment designed for automated measurement applications [200]. The use of the ANSI C programming language provides virtually unlimited flexibility and compatibility with a wide range of program libraries. Within the test program, low frequency test patterns for evaluating circuit functionality are stored in arrays, whose size is limited only by the 256 MByte memory of the PC. The length and complexity of the test patterns which can be generated are more than adequate for testing any RSFQ circuit which can be fabricated in current Josephson technology. The ANSI C code is compiled for fast execution; typically, the time spent processing and interpreting the results of a low frequency diagnostic test is negligible compared to the time originally spent acquiring the data with the DAQ cards. The LabWindows/CVI package features built-in libraries for operating National Instruments DAQ cards, controlling GPIB instruments, and designing a graphical user interface through which the user

enters commands and test parameters and observes the results of low frequency testing. The graphical user interface allows the user to vary operating parameters such as dc bias currents in an interactive manner.

As explained earlier in Section 11.1, the functionality of an RSFQ circuit is evaluated by writing the test patterns to a couple of the analog outputs of the DAQ cards and measuring the response of the circuit with the analog inputs of the DAQ cards. The measured response is then compared in software with the output patterns expected from the circuit under test. A pop-up window notifies the user whether the circuit has passed or failed the functionality test. If the circuit is not functional, the user can modify the operating parameters and try the test again. Once functionality has been achieved, the user can run software routines for automated margin measurement, in which an operating parameter such as a computer-controlled bias current is systematically varied until the circuit no longer passes the functionality test. In addition to the margins of individual bias currents, the global bias current margins can be measured by increasing and decreasing all of the computer-controlled bias currents at the same time. No software routines for optimizing the operating parameters for highest margins were written. Instead, the operating parameters were adjusted manually by the user until the measured margins were maximized.

Chapter 12

Modulator Test Chip Results

This chapter presents the experimental results from the modulator test chip. Low frequency (2 kHz) diagnostic testing was used to verify the design and screen the 16 copies of the modulator test chip for functionality. One copy was found to pass all low frequency tests and was then used in a high frequency demonstration of the bandpass modulator. High speed clocking of the modulator was accomplished both optically (at 20.6 GHz) and with the on-chip Josephson source (up to 45 GHz). The results of segmented correlation measurements are discussed at the end of the chapter.

As explained in Section 10.1, some digital circuits of the modulator test chip such as the 1:4 DEMUX and the three-stage shift register preceding it cannot be tested for functionality at low frequency, as they lie upstream of the point at which the diagnostic test inputs insert SFQ pulses onto the data and clock lines through confluence buffers. In order to verify the design of these digital circuits, a separate diagnostic circuit incorporating them was laid out and fabricated. This diagnostic circuit and its test results are examined in the first section of the chapter, after which the main results on the modulator test chip are presented.

12.1 1:4 DEMUX Diagnostic Circuit

Figure 12-1 shows the block diagram of the diagnostic circuit used for evaluating the digital circuits at the output of the bandpass modulator, the most significant of which is the 1:4 DEMUX described in Section 10.2.3. The SFQ comparator is identical to the comparator of the bandpass modulator, but in this case its input is not an analog signal but a digital signal DATA_IN, which is supplied to the diagnostic circuit as a binary-valued external current. The amplitude of DATA_IN greatly exceeds the input noise level of the SFQ comparator so that data bits can be loaded into the three-stage shift register with a negligible error rate. External current CLK_IN drives a standard DC/SFQ converter [31], generating SFQ pulses which clock the digital circuits at low frequency (e.g., f_{in}=1 kHz). Ignoring the dependence of SFQ comparator delay on input overdrive level (which is higher in this digital mode of operation than typical for the bandpass modulator), the timing between the data and clock pulses arriving at the three-stage shift register matches that on the modulator test chip. All of the circuitry after the SFQ comparator up to (but not including) the toggling (T–type) SFQ/DC converters [31] is copied from the layout of the modulator test chip. The SFQ/DC converters are added so that the frequency-divided clock and data outputs of the

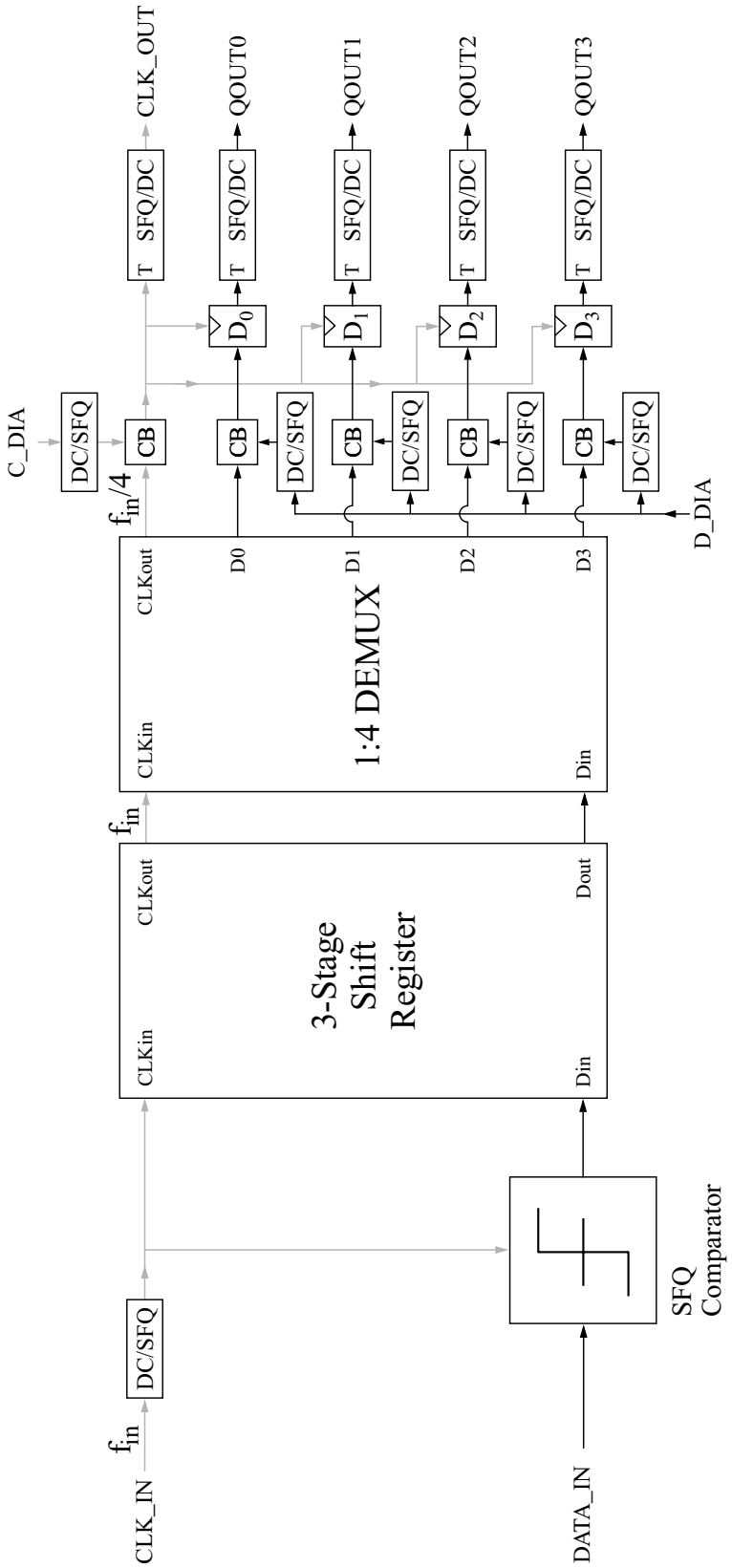


Figure 12-1: Block diagram of diagnostic circuit for 1:4 DEMUX.

1:4 DEMUX can be monitored with room-temperature instruments such as oscilloscopes. External inputs C_DIA and D_DIA can be used to insert SFQ pulses onto the clock and data output lines through the confluence buffers at the output of the 1:4 DEMUX; these inputs, which are the ones used for low frequency testing of the modulator test chip, have only limited utility in this relatively small diagnostic circuit.

Figure 12-2 illustrates operation of this diagnostic circuit at a clock rate of 1 kHz. The input data pattern, listed in the figure caption, provides a comprehensive test of the 1:4 DEMUX. Each SFQ clock or data pulse produced by the 1:4 DEMUX is registered as a transition in the output of an SFQ/DC converter. Examination of the waveforms shown in the figure confirms correct operation of the 1:4 DEMUX. The pipelining latency added by the three-stage shift register increases the delay between the input DATA_IN and the data outputs QOUT0–QOUT3. On the other hand, the D latches labeled D_0–D_3 in Figure 12-1 do not add any pipelining latency, as the circuit delays are such that the SFQ clock pulses from the 1:4 DEMUX arrive at these latches *after* they have been loaded with the SFQ data pulses. As discussed earlier, this type of concurrent flow clocking is used extensively inside the 1:4 DEMUX itself.

The measured bias and input current margins of the 1:4 DEMUX diagnostic circuit are listed in Table 12.1. In measuring the margins for global bias current (XI), all of the computer-controlled bias currents are increased and decreased together, with the exception of I/O_PWR, which supplies power to input and output circuits such as the DC/SFQ and SFQ/DC converters and to various JTLs connecting them to the rest of the diagnostic cir-

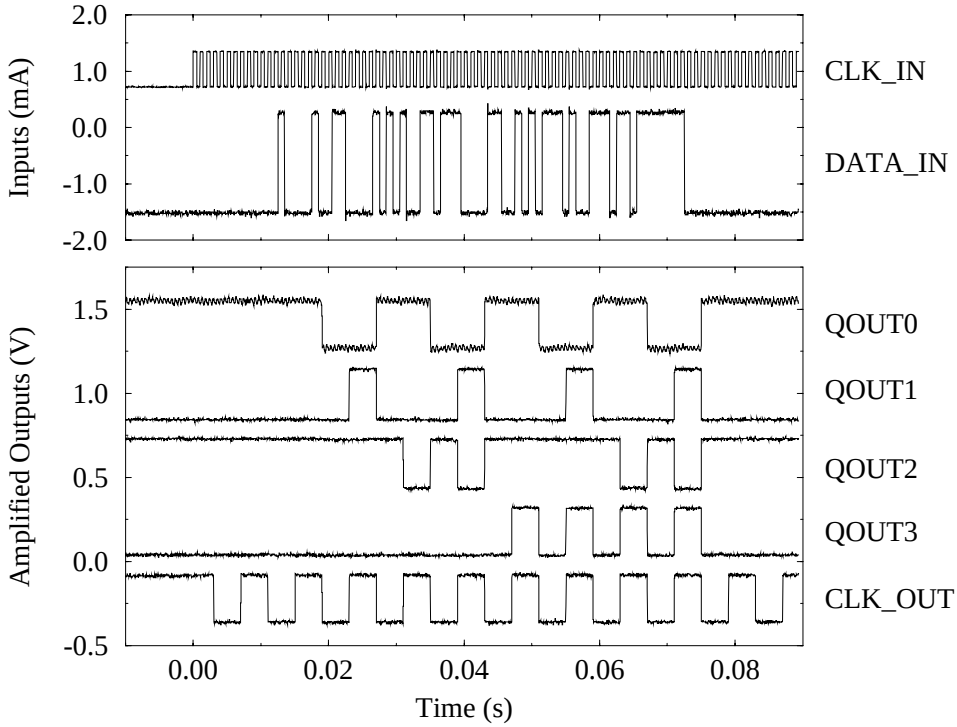


Figure 12-2: Operation of 1:4 DEMUX at 1 kHz. The input data pattern is 1000 0100 1100 0010 1010 0110 1110 0001 1001 0101 1101 0011 1011 0111 1111. For clarity, the waveforms are offset.

Table 12.1: Measured bias and input current margins[a] of 1:4 DEMUX diagnostic circuit.

Bias or Input Current Name	Value (mA)	Lower Margin (%)	Upper Margin (%)
XI	N/A	−27.2	25.9
D_SHIFT	3.00	−50.3	36.6
C_SHIFT	8.00	−27.2	28.4
DEMUX_PWR	45.00	−27.2	27.2
D_ADJ	3.40	−48.4	32.2
C_ADJ	4.60	< -60.0	36.6
I/O_PWR	9.90	−20.9	23.4
CLK_IN (low value)	-0.10	< -60.0	> 60.0
CLK_IN (high value)	0.53	−44.1	45.3
DATA_IN (low value)	-0.69	< -60.0	> 60.0
DATA_IN (high value)	1.11	< -60.0	> 60.0

[a]The margins were only measured up to ±60%.

cuit. Compared with most RSFQ cells, SFQ/DC converters have relatively small operating margins [31]. To prevent the global bias current margins from being limited by these peripheral circuits, I/O_PWR is not varied in concert with the other bias currents but held at its nominal value (9.9 mA). The global bias current margins are primarily limited by the margins of DEMUX_PWR, the main supply current for the 1:4 DEMUX. For sake of comparison, the simulated global bias current margins are only a few percent larger: -30%, +29%. Independent supply currents D_ADJ and C_ADJ are used to adjust the delays of JTLs within the 1:4 DEMUX so that the skew between the data and clock pulses is optimized for highest performance. Independent supply currents D_SHIFT and C_SHIFT perform a similar function within the three-stage shift register.

12.2 Low Frequency Testing of Modulator Test Chip

The 16 copies of the modulator test chip were first screened for functionality at low speed (2 kHz). As an example of such testing, Figure 12-3 shows correct operation of the programmable counter with three different relative delays between the LOADA and LOADB pulses. (Note the longer time scale in the third case.) The CLK signal which clocks the programmable counter is generated with one of the diagnostic inputs of the chip. Since the low frequency diagnostic outputs are generated with T-type SFQ/DC converters, each SFQ pulse in the LOADA and LOADB bursts is registered as a transition in one of the output waveforms. With a relative delay less than 32 CLK cycles, the LOADA and LOADB bursts overlap in time. Such short relative delays are not used in testing the bandpass modulator since there is no benefit in loading shift register memory banks A and B with redundant data. Furthermore, such short relative delays create a timing conflict between loading and unloading of shift register memory bank B. As illustrated earlier in the timing diagrams of Figure 10-2, the shift register memory banks are loaded and unloaded in a "ping-pong" arrangement, in which memory bank A is loaded while memory bank B is unloaded, and vice

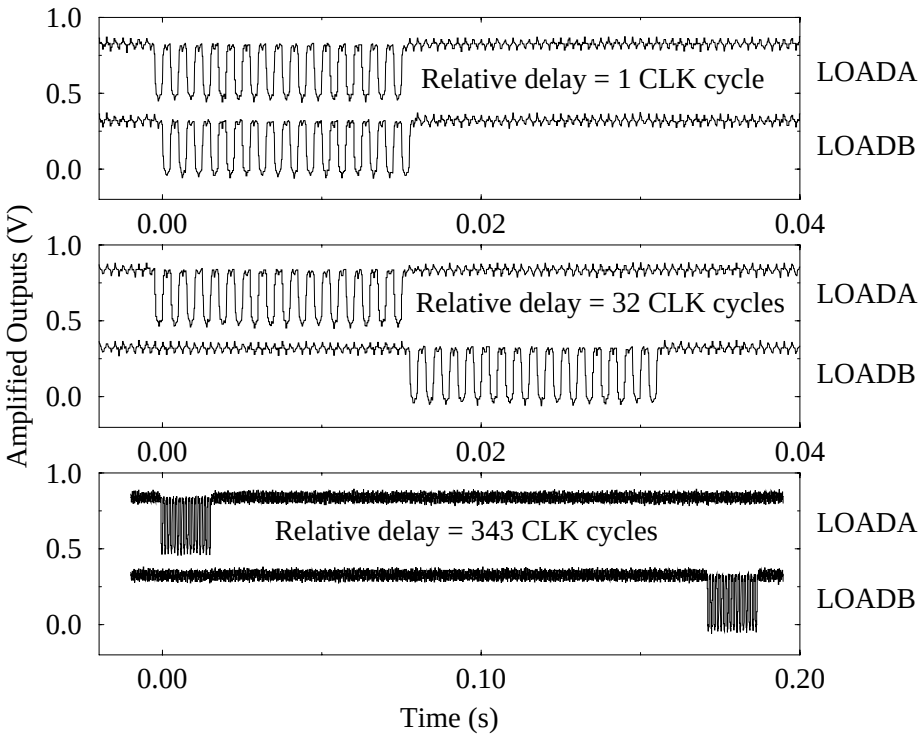


Figure 12-3: Operation of the programmable counter with three different relative delays between the LOADA and LOADB pulses. The frequency of CLK is 2 kHz. For clarity, the waveforms are offset.

versa. This arrangement fails if the LOADA and LOADB bursts overlap in time, as memory bank B will begin loading before it has finished unloading. Thus, while the programmable counter itself operates correctly for relative delays as small as 0 CLK cycles, the smallest relative delay used in testing the bandpass modulator is 32 CLK cycles, for which the first LOADB pulse immediately follows the last LOADA pulse, and the two 128-bit memory banks acquire 256 consecutive bits of the modulator output. Relative delays greater than 32 CLK cycles are used for segmented correlation measurements.

Other digital circuits of the modulator test chip were evaluated with a comprehensive set of test patterns. One copy of the modulator test chip passed all low frequency testing. Table 12.2 presents the measured margins for global bias current (XI) and for individual bias currents of 13 major subsystems, including parts of the programmable counter, the loading circuitry, shift register memory banks A and B, and the readout controller. Since the 1:4 DEMUX and the three-stage shift register preceding it are not exercised during low frequency testing, their margins are not listed in the table. To achieve higher operating speed, several of the bias currents are adjusted away from the midpoints of their operating ranges. Bias currents CLK_JTL, DATA_JTL, and LOAD_JTL are the three independent supplies mentioned in Section 10.2.5 for optimizing signal skew within the loading circuitry. The global bias current margins are limited by the margins of READOUT_2, which supplies power to most of the readout controller. The small margins for this bias current are apparently due to a fabrication defect. (Other copies of the modulator test chip had much larger margins for this bias current but suffered from other fatal defects.) Even with these

Table 12.2: Measured bias current margins of modulator test chip.

Bias Current Name	Value (mA)	Lower Margin (%)	Upper Margin (%)
XI	N/A	−3.6	4.1
PROGCNTR_1	36.0	−29.4	19.4
PROGCNTR_2	75.0	−20.6	14.4
TIMERS	25.9	−25.6	25.6
CLK_JTL	15.6	−23.1	26.9
DATA_JTL	16.1	−26.9	38.1
LOAD_JTL	25.2	−49.4	16.9
SRC_CELLS	32.0	−41.9	25.6
SHFTREGA_1	62.0	−18.1	13.1
SHFTREGA_2	60.3	−24.4	13.1
SHFTREGB_1	60.0	−28.1	18.1
SHFTREGB_2	60.0	−15.6	14.4
READOUT_1	57.0	−24.4	24.4
READOUT_2	95.1	−3.6	4.1

small margins, the readout controller was found to operate reliably.

Following the slow cooldown procedure described in Section 6.1.3 largely eliminated flux trapping problems, and the operating margins of the modulator test chip were consistent from cooldown to cooldown. However, some problems with magnetic contamination were encountered. On two separate occasions over the course of several months of testing, the digital circuitry on the modulator test chip ceased working properly, and the same exact errors were detected repeatedly after several cooldowns. In the first case, correct operation was restored by careful cleaning of the chip, suggesting that a magnetized particle of dust or dirt may have fallen on its surface. In the second case, cleaning the chip did not solve the problem, but correct operation was restored by demagnetizing the chip itself with a Radio Shack degausser. In both cases, the operating margins were restored to those listed in Table 12.2. Developing a better understanding of magnetic contamination effects and their impact on the yield of complex Josephson circuits may be a valuable topic for future research.

12.3 Basic Functionality of Bandpass $\Delta\Sigma$ Modulator

The basic functionality of the superconducting bandpass $\Delta\Sigma$ modulator was first established by triggering the modulator test chip with the optical clock source. Figure 12-4 shows the two outputs DATA and START generated by the high voltage output drivers of the chip at a sampling rate of 20.6 GHz. The readout controller unloads the DATA bits from the on-chip acquisition memory at a rate of 161 Mbit/s ($=f_s/128$). The relatively low bandwidth requirements for readout allow amplification of the output signals with a high SNR, and the bit error rate is negligible. The shape of the waveform on the START bit output is close to ideal (cf. Figure 10-12(b)). In this measurement, the oscilloscope is triggered off the *previous* missing pulse on the START bit output, about 1.59 μs earlier than the one

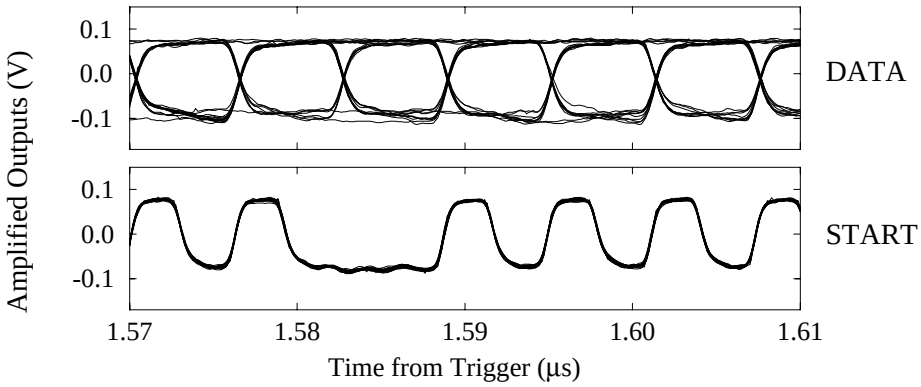
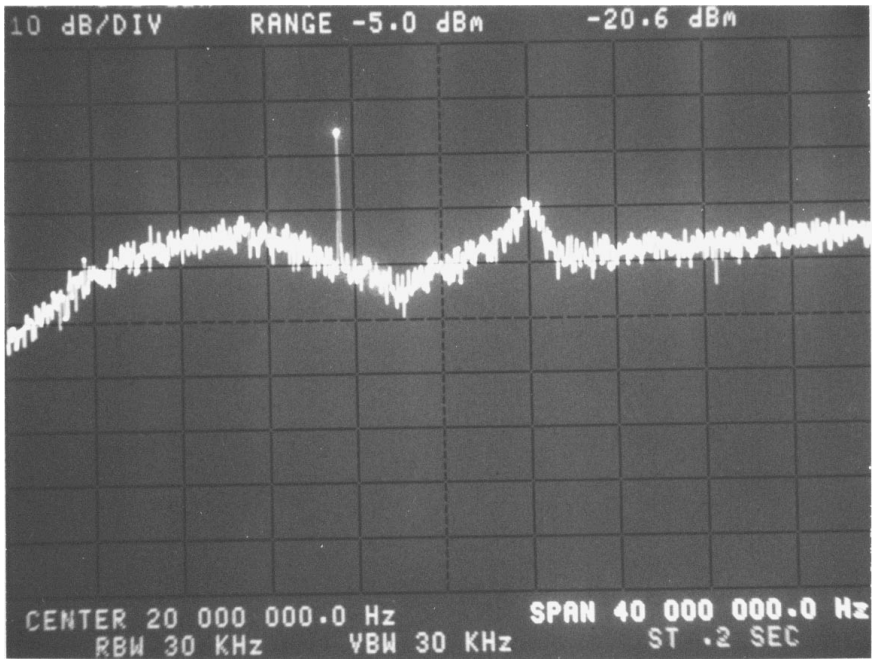


Figure 12-4: Output waveforms generated by test chip when clocked by optical source (f_s=20.6 GHz).

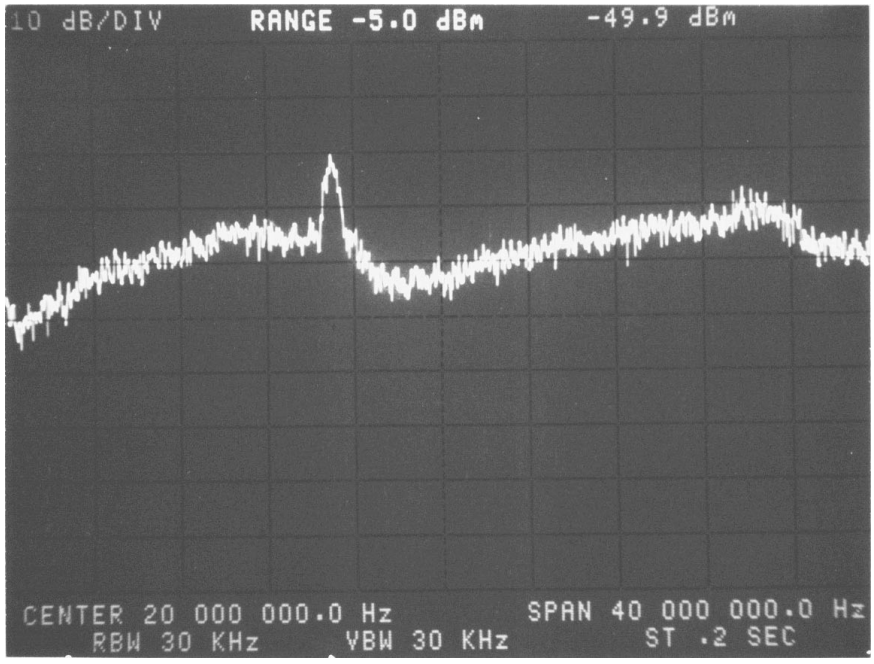
visible in the figure. The excellent frequency stability of the optical clock source is evident in the lack of jitter on the measured waveforms so long after the triggering event. Similar measurements with the relatively unstable on-chip clock source show much higher levels of jitter.

As explained in the last chapter, a real-time display of the modulator output spectrum is obtained by connecting the DATA output of the test chip to an analog spectrum analyzer. Examples of such measurements are illustrated in Figure 12-5. For the measurement shown in Figure 12-5(a), the modulator is optically clocked at 20.6 GHz and driven by an analog input near 1.9454 GHz. The on-chip programmable counter is configured so that the shift register memory banks capture 256 consecutive bits of the modulator output. While the 256-bit sequences are read out as an unbroken stream on the DATA output, the component of the DATA output due to the analog input is not, in general, a continuous sinusoid but contains phase jumps between each 256-bit sequence. However, such phase jumps can be avoided if the ratio of input frequency to sampling rate is carefully adjusted so that the number (32512) of modulator output bits skipped between acquiring 256-bit sequences corresponds to an integral number of periods of the input. With such an adjustment, the component of the DATA output due to the analog input approximates a continuous sinusoid, which appears as a narrow line on the display of the spectrum analyzer (Figure 12-5(a)). Since the bit rate of the DATA output equals $f_s/128$, the frequency of this line equals 1.9454 GHz/128=15.2 MHz. The frequency resolution of the measured noise spectrum is still low, as the quantization noise components are virtually uncorrelated between different 256-bit sequences. The minimum in the measured noise at 18 MHz indicates that the quantization noise of the modulator is suppressed near 2.3 GHz, which is consistent with the spectral analysis of the binary output data presented later in the chapter.

For the measurement shown in Figure 12-5(b), the modulator is clocked by the on-chip Josephson oscillator at 22 GHz and driven by an analog input at 1.91 GHz. The relatively poor frequency stability of the on-chip oscillator precludes precise adjustment of the ratio of input frequency to sampling rate. Consequently, the component of the DATA output due to the analog input contains random phase jumps between each 256-bit sequence in the data stream. Because of the lack of phase coherence between 256-bit sequences, the input signal is displayed on the spectrum analyzer with only limited frequency resolution,



(a)



(b)

Figure 12-5: Measurements of DATA output with analog spectrum analyzer. (a) The modulator is optically clocked at 20.6 GHz and driven by -28.8 dBm input at 1.9454 GHz. (b) The modulator is clocked by the on-chip Josephson oscillator at 22 GHz and driven by -29.1 dBm input at 1.91 GHz.

corresponding to that of a single 256-bit sequence. The two spectra shown in Figure 12-5 exhibit a local maximum in the measured noise at a frequency above the minimum at 18 MHz. The dependence of the location of this maximum on the sampling rate indicates that it is due to an aliased mode.

While these measurements with the spectrum analyzer demonstrate the noise shaping of the modulator qualitatively, the accuracy of this analog technique is limited by its sensitivity to noise and waveform distortion on the DATA output. Quantitatively accurate estimates of modulator performance are obtained by analyzing the binary output codes in software. Some of the processing applied to the experimental data was motivated by clocking problems encountered when the modulator was triggered by the optical source. These problems are therefore described next, after which the measured performance of the modulator is discussed.

12.4 Modulator Performance with Optical Clock Source

12.4.1 Clocking Problems

Two distinct clocking problems were encountered when the modulator was triggered with the optical clock source. First, the conversion of current pulses from the MSM photodiode into SFQ clock pulses was not completely reliable. Occasional missing clock pulses were indicated by output waveforms delayed from their usual positions in time, as exemplified by the dotted traces in Figure 12-6. The primary cause of the problem was the unexpectedly low sensitivity of the MSM photodiode. Even with the average power of the 20.6 GHz optical pulse train turned up to about 1.1 mW (the maximum that could be delivered to the chip by the optical clocking setup), the dc photocurrent was about 30% lower than in the optically triggered JTL experiment discussed in Chapter 6. The problem was further exacerbated by the critical current density of the fabricated chip, which was 23.4% higher than nominal. The relatively large critical currents of the Josephson junctions hindered their switching by weak photocurrent pulses. Fortunately, these clocking errors were rare enough not to affect most of the waveform records acquired by the digital oscilloscope. The few waveform records that exhibited these errors were easily screened out by examining the timing of the output waveforms and subsequently ignored in calculating the output spectra of the modulator. Even for waveform records without missing clock pulses, though, the jitter of the sampling clock was likely degraded by sluggish switching of the junction triggered by the photocurrent.

Under normal operating conditions, the second clocking problem was more serious and affected all of the waveform records. As noted earlier, the 1:4 DEMUX on the modulator test chip could not be tested for functionality at low frequency. High frequency testing with the optical clock source revealed a problem in the operation of this circuit. If the bias current for the 1:4 DEMUX were set to a value below its normal operating range, the clocking was stable (except for the rare errors considered in the previous paragraph), and the missing pulse on the START bit output was asserted at the expected time (top trace in Figure 12-7). However, if the bias current for the 1:4 DEMUX were set to a value within its normal operating range, the SFQ data pulses propagating through the 1:4 DEMUX sometimes triggered SFQ pulses on one of the clock JTLs. The extra clock pulses made the on-chip counters run faster, and the missing pulse on the START bit output was asserted

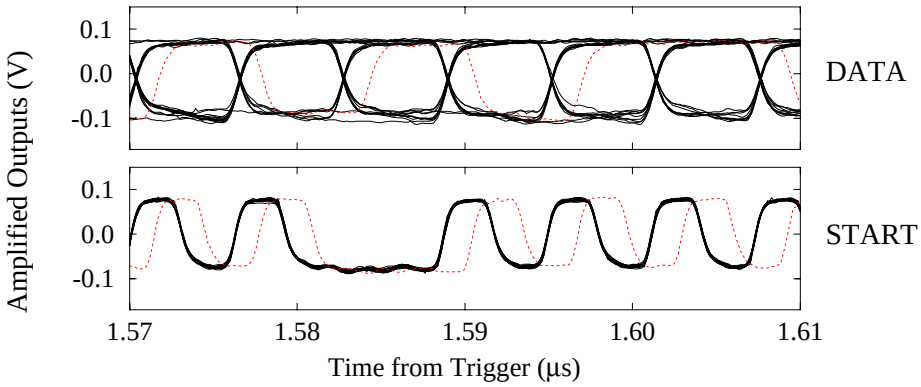


Figure 12-6: Output waveforms indicating occasional missing clock pulses with test chip triggered by optical source.

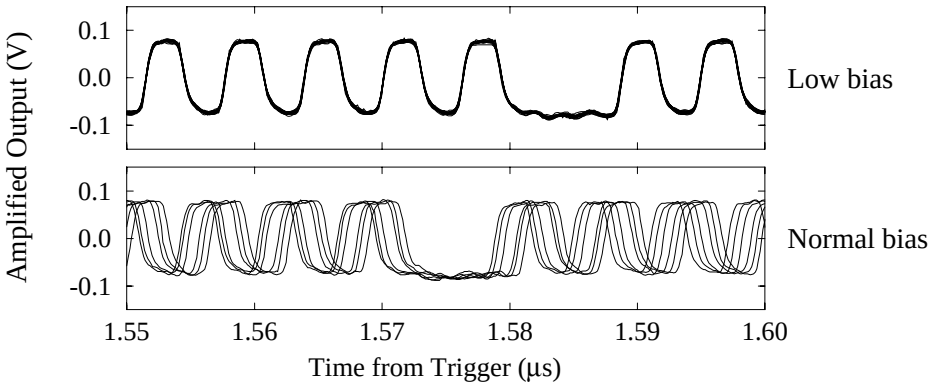


Figure 12-7: START bit output at low (34.0 mA) and normal (48.0 mA) values of bias current for the 1:4 DEMUX. At a normal value of bias current, extra clock pulses are erroneously generated within the DEMUX, and the START bit is asserted earlier than expected. The test chip is being clocked by the optical source.

earlier than expected (bottom trace in Figure 12-7). Random variations in the number of extra clock pulses account for the jittered appearance of the START bit output. Since the extra clock pulses are triggered by the SFQ data pulses, this clocking problem disappears if the SFQ comparator of the bandpass modulator is biased to generate all 0's.

When first discovered, this problem was attributed to a fabrication defect within the 1:4 DEMUX. Surprisingly, though, this problem disappeared during subsequent testing of the bandpass modulator with the on-chip Josephson clock source. As discussed later, magnetic contamination is the most likely explanation for this problem, which complicated all of the measurements performed with the optical clock source.

It should be mentioned that the oscilloscope data presented in Figures 12-4 and 12-6 were obtained with a low value of bias current for the 1:4 DEMUX so that the timing of the output waveforms was not affected by the generation of extra clock pulses. A low value of bias current was also used for the spectrum analyzer measurement shown in Figure 12-5(a) in order to achieve the clocking stability necessary for displaying a narrow spectral line. An underbiased mode of operation cannot be used for accurate measurement of modulator

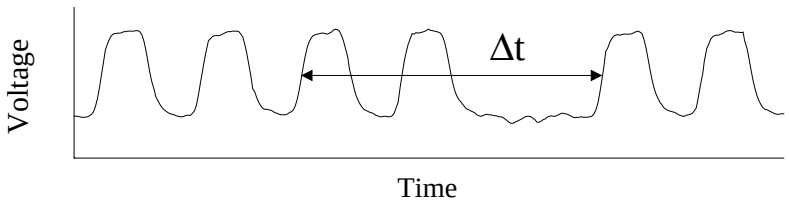
performance, though, as the 1:4 DEMUX does not process the data bits correctly at low bias currents. (Such errors at low bias reduced the depth of the noise minimum displayed in Figure 12-5(a)). The data obtained with a normal value of bias current for the 1:4 DEMUX can be used for accurate measurement of modulator performance, but only if the binary output codes corrupted by the extra clock pulses are screened out before calculating the output spectra of the modulator. The method and results of such screening are described next.

12.4.2 Measured Results After Screening Out Corrupted Data

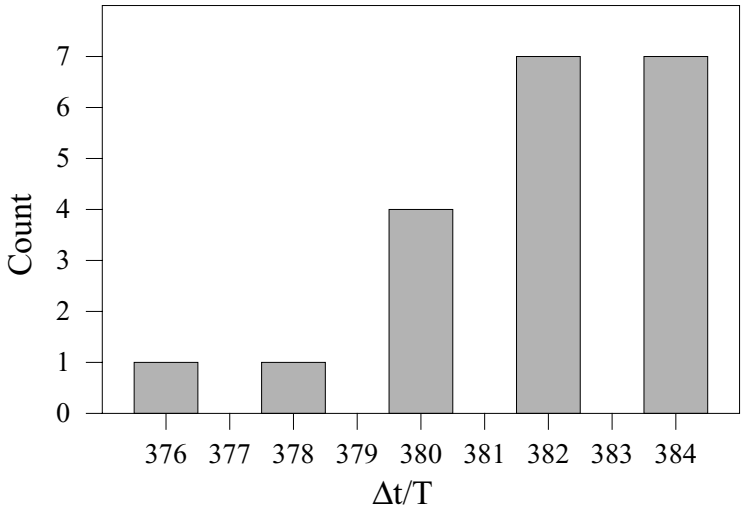
While the extra clock pulses alter the times at which the DATA output bits appear within the waveform records acquired by the digital oscilloscope, the DATA output is still an accurate representation of the data captured in the on-chip acquisition memory, as unloading of the memory banks at a readout rate of $f_s/128$ is not logically disturbed by a few extra clock pulses generated within the high speed section of the chip. On the other hand, the high speed loading of the memory banks can be disturbed by even a single extra clock pulse, so the data captured in the acquisition memory may not be an accurate representation of the modulator output. To avoid problems with data corruption and obtain accurate measurement of modulator performance, it is necessary to screen out those waveform records which indicate that one or more extra clock pulses were generated during loading.

The screening of each waveform record is based on careful examination of the START bit output. Because loading and unloading of the acquisition memory are precisely synchronized, there is a well-defined timing relationship between loading of the acquisition memory and assertion of the missing pulse on the START bit output. Assuming that the programmable counter is configured so that shift register memory banks A and B capture 256 consecutive bits of the modulator output, loading of both memory banks occurs within a time interval Δt defined between two rising edges of the START bit waveform and shown in Figure 12-8(a). Ideally, Δt equals $384T$, where $T = 1/f_s$. However, Δt will be smaller than $384T$ if one or more extra clock pulses were generated during loading since such pulses advance the states of the on-chip counters. Thus, waveform records for which the measured value of $\Delta t/T$ (after rounding to the nearest integer) is less than 384 should be screened out. Figure 12-8(b) shows an example histogram of $\Delta t/T$ for 20 waveform records acquired by the digital oscilloscope. The histogram shows that 13 out of the 20 waveform records should be screened out. It is worth noting that $\Delta t/T$ always differs from 384 by a multiple of two. This indicates that the problem in the 1:4 DEMUX was located after the first stage of the binary tree shown in Figure 10-3.

Figure 12-9 shows the modulator output spectra that are calculated before and after screening out the corrupted waveform records. Each of the binary output codes is windowed by a Kaiser window [1] with $\beta = 4.5$ prior to computing the 256-point FFTs averaged in making the plots. The limited frequency resolution of the 256-point FFTs is reflected in the width ($\approx$ 200 MHz) of the input tone at 1.95 GHz. The input frequency has been chosen so that this wide tone does not obscure the quantization noise near the modulator center frequency (2.3 GHz). Screening out the corrupted data dramatically increases the sharpness and depth of the noise minima at dc, 2.3 GHz, 7.0 GHz, and 8.5 GHz. Over a 20 MHz bandwidth centered at 2.3 GHz, the measured in-band noise is improved by screening from -34.4 dBFS to -48.0 dBFS. After screening, the measured in-band noise is limited by the low frequency resolution of the 256-point FFTs, which smears the noise spectrum near



(a)



(b)

Figure 12-8: (a) Time interval Δt defined from START bit waveform. (b) Example histogram of $\Delta t/T$ for 20 waveform records.

2.3 GHz. For sake of comparison, the in-band noise over a 20 MHz bandwidth calculated by averaging 256-point FFTs of circuit simulation data is -49.7 dB, only 1.7 dB lower. Because the frequency resolution of the measurement is limited, doubling the bandwidth from 20 to 40 MHz increases the measured in-band noise by only 3.4 dB, to -44.6 dBFS. The quantization noise minimum at 8.5 GHz and maximum at 8.1 GHz are the result of aliased modes and do not appear in output spectra measured at higher sampling rates, shown later in the chapter.

Evaluation of the modulator test chip with the optical clock source ended prematurely when a voltage spike created by an error in experimental procedure severely damaged the MSM photodiode. More comprehensive testing of the bandpass modulator was conducted with the on-chip Josephson clock source, whose frequency stability and jitter were better than anticipated. For this reason, most discussion of the experimental results on the bandpass modulator is reserved for the next section. Nonetheless, the close correspondence between simulated and measured in-band noise levels makes these results with the optical clock source a valuable point of reference.

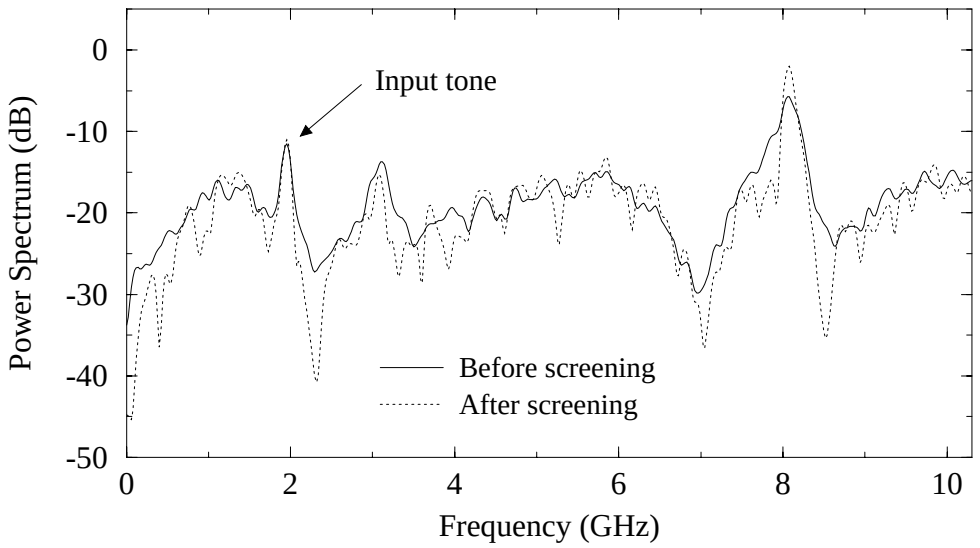


Figure 12-9: Comparison of measured output spectra before and after screening out corrupted waveform records. The modulator is optically clocked at 20.6 GHz and driven by -29.1 dBm input at 1.95 GHz.

12.5 Modulator Performance with Josephson Clock Source

12.5.1 Disappearance of Problem with 1:4 DEMUX

Initial testing of the modulator test chip with the Josephson clock source exhibited the same problem with the 1:4 DEMUX which had corrupted some of the data measured with the optical clock source. Therefore, the problem was not due to heat generated by the light incident upon the MSM photodiode. The problem with the 1:4 DEMUX disappeared, though, when the glass capillary used for fiber alignment (Section 6.1.2) fell off the chip due to weakening of the glue after several thermal cycles. While the 1:4 DEMUX was not covered by the glass capillary itself, it was covered by some of the glue, which fell off with the capillary. The sudden disappearance of the problem after the glue fell off suggests two possible explanations. The layer of glue on the chip surface may have hindered cooling of the circuit by the liquid helium. However, the 1:4 DEMUX was not the only circuit covered by the layer of glue, so it is not clear why it would have been the only one troubled by self-heating. A more likely explanation for this localized problem is that a magnetized particle of dust or dirt may have been trapped in the glue covering the 1:4 DEMUX. As mentioned earlier, similar problems with magnetic contamination in other areas of the chip were encountered during low frequency testing.

Since the problem with the 1:4 DEMUX disappeared, the screening described in the last section was not applied to the data measured with the Josephson clock source. The only screening applied to the experimental data presented below was motivated by the relatively poor frequency stability of the Josephson oscillator. To reduce the effects of clock frequency drift on the measured performance of the modulator, waveform records with clock rates that differed by more than $\pm 0.06\%$ from the ensemble average were screened out by examining the time intervals between the missing pulses on the START bit output. At f_s=40.2 GHz (the sampling rate used for the segmented correlation measurements), about 30% of the

waveform records were rejected by such screening.

12.5.2 Output Spectra and SNR

The best modulator performance with the Josephson clock source is attained at sampling rates near 40 GHz. The output spectra of the modulator at a 42.6 GHz sampling rate are shown in Figure 12-10. Each of the binary output codes is windowed by a Kaiser window with $\beta = 6.5$ prior to computing the 256-point FFTs averaged in making the plots. The width ($\approx$ 500 MHz) of the input tone at 1.7 GHz again reflects the low frequency resolution of the 256-point FFTs. Except for the low resolution, the spectra are similar to the simulated ones shown in Figure 8-4. For the spectra shown in Figure 12-10, the quantization noise minimum corresponding to quarter-wave resonance is located at about 2.25 GHz, slightly lower than the value of 2.3 GHz measured with the optical clock source. The simulations of Chapter 8 showed a similar downward shift in modulator center frequency with increase in sampling rate. Higher resolution estimates of the output spectrum based on segmented correlation data presented later in the chapter indicate that the actual center frequency of the modulator at sampling rates near 40 GHz is closer to 2.23 GHz, about 7% higher than that predicted by circuit simulation. Most likely, the effective dielectric constant of the microstrip transmission line resonator is smaller than expected. (As pointed out in Chapter 9, dielectric constants are not accurately characterized in most Josephson integrated circuit processes.) The amplitude of a FS input is -17.4 dBm (30 mV rms into 50 Ω). After accounting for the 6 dB attenuator on the modulator test chip, input sensitivity is about 2 dB higher than that predicted by Equation 7.36.

Figure 12-11 plots the measured SNR as a function of input level for a signal bandwidth of 20.8 MHz. Peak SNR is over 49 dB. The low frequency resolution of the measurements (based on 256-point FFTs) limits the SNR by smearing the noise spectra near the modulator center frequency.

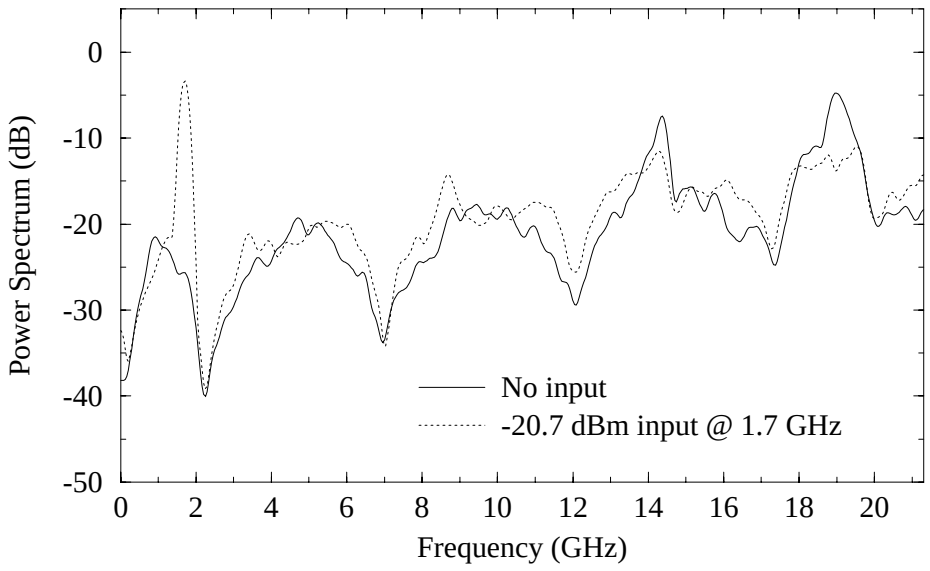


Figure 12-10: Measured output spectra of modulator at f_s=42.6 GHz.

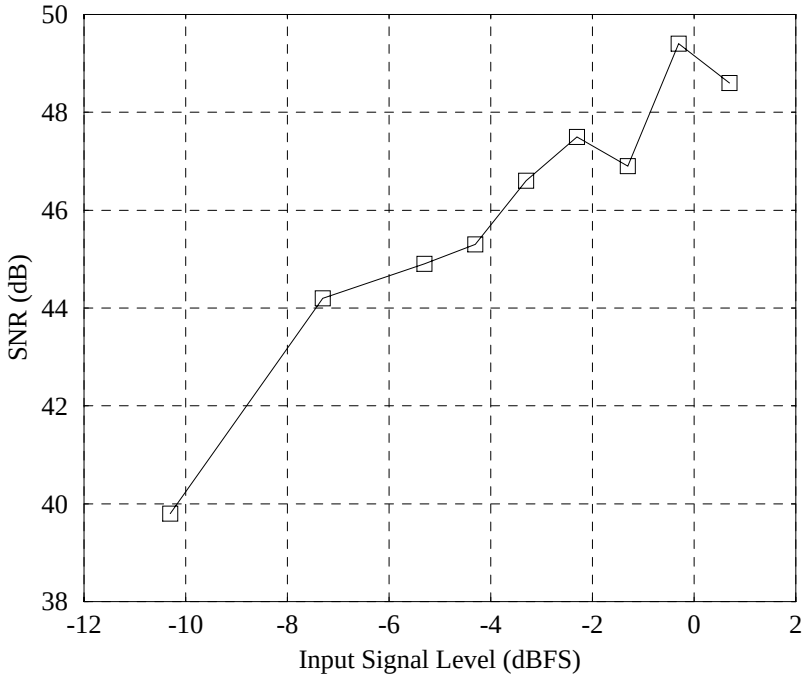


Figure 12-11: Measured SNR as a function of input level for a signal bandwidth of 20.8 MHz. The input frequency is 1.7 GHz, and f_s=42.6 GHz.

12.5.3 Dependence of In-Band Noise on Sampling Rate

The tunability of the Josephson oscillator allows the bandpass modulator to be operated at different sampling rates. Figure 12-12 plots the measured in-band noise over a 20 MHz bandwidth as a function of the sampling rate. While all the in-band noise levels are compromised by the low frequency resolution of the measurements, the general dependence on sampling rate is clear. As noted above, the in-band noise achieved with the 20.6 GHz optical clock is only 1.7 dB higher than the in-band noise predicted by simulation. Oscilloscope measurements of the output waveforms show that the on-chip Josephson oscillator has poor frequency stability and relatively high jitter near 20 GHz. Consequently, the in-band noise with the on-chip source is almost 6 dB higher than with the optical clock. The frequency stability and jitter of the on-chip source improve at higher frequencies, however. For sampling rates between 33 and 42.6 GHz, the increase in oversampling ratio more than compensates for the higher jitter of the on-chip source. The minimum in-band noise is found at a sampling rate of 40.2 GHz, where the Josephson oscillator has the narrowest linewidth according to analog spectrum analyzer measurements. As demonstrated in Section 12.5.5, even lower in-band noise levels at a 40.2 GHz sampling rate are measured by increasing the frequency resolution with the segmented correlation technique. Above 45 GHz, the digital circuitry of the modulator test chip malfunctions, and no meaningful data can be acquired.

12.5.4 Intermodulation Distortion Test

Figure 12-13 shows the result of a two-tone IM distortion test of the bandpass modulator. The input frequencies, 1.30 and 1.775 GHz, are chosen so that the upper third-order IM distortion product falls at 2.25 GHz, close to the quantization noise minimum at 2.23 GHz.

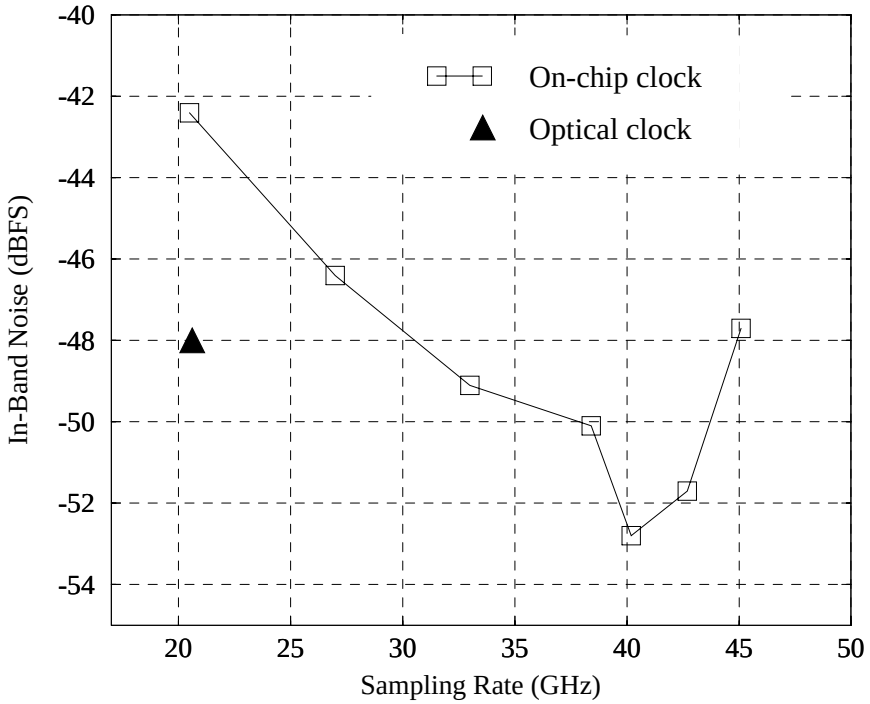


Figure 12-12: Measured in-band noise over 20 MHz bandwidth as a function of sampling rate.

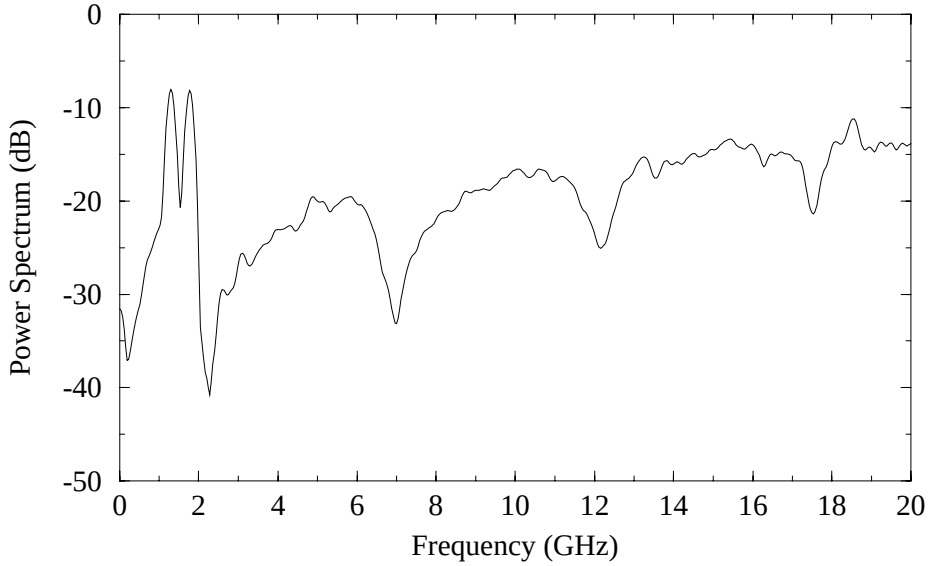


Figure 12-13: Two-tone IM distortion test with 1.30 and 1.775 GHz inputs (f_s=40.3 GHz).

Both input amplitudes are -8 dBFS. No distortion product near 2.25 GHz can be observed above the noise floor, which is only 40 dB below FS because of the low frequency resolution of the measurement (based on 256-point FFTs). This limited test only shows that there is no gross distortion problem with the modulator. To demonstrate the low levels of IM distortion predicted by simulation, measurements with much higher frequency resolution would be required.

12.5.5 Segmented Correlation Measurements with No Input

Since the lowest in-band noise of the modulator was obtained with the Josephson clock source operating at 40.2 GHz, more accurate measurements of the output spectrum were made at this sampling rate with the segmented correlation technique. This section presents the segmented correlation data measured under idle channel conditions (i.e., no input). The next section describes the extra complications incurred in interpreting the segmented correlation data measured with an input tone.

As explained in the last chapter, the amount of modulator output data that can be acquired in a given measurement time is severely limited by the slow transfer of waveform records to the hard drive of the digital oscilloscope. About 4000 of the 256-bit sequences read out from shift register memory banks A and B can be acquired in half an hour. Such an amount of data is only sufficient[1] for the most modest segmented correlation measurements, in which the autocorrelation function $R[n]$ is estimated up to $n = 511$, and the frequency resolution of the estimated spectrum is about twice that of a 256-point FFT. Even if the test setup were upgraded so that much more of the data produced by the modulator test chip could be utilized, though, estimation of $R[n]$ for values of n much larger than 511 would likely be hindered by frequency variations of the on-chip clock source (up to $\pm 0.06\%$ after the screening described in Section 12.5.1).

An estimate of $R[n]$ (from $n = 0$ up to $n = 511$) is obtained by adding together four (averaged) segmented correlation estimates. In accordance with the notation of Chapter 9, these four estimates are denoted by $\hat{R}_{auto}[n]$, $\hat{R}_0[n]$, $\hat{R}_L[n]$, and $\hat{R}_{2L}[n]$, with $L = 128$. $\hat{R}_{auto}[n]$ and $\hat{R}_0[n]$ are calculated from the binary output codes with M (the number of modulator output bits skipped between loading shift register memory banks A and B) equal to 0. $\hat{R}_L[n]$ and $\hat{R}_{2L}[n]$ are calculated from the binary output codes with $M = L = 128$ and $M = 2L = 256$, respectively. Before adding them together, the four segmented correlation estimates are multiplied by the weighting functions given by Equations 9.13 and 9.14. As first shown in Figure 9-3, the estimate of $R[n]$ assembled from these four weighted estimates is unbiased for values of n between 0 and 384 and progressively biased for values of n between 385 and 511.

Unlike periodograms (i.e., standard FFTs), power spectra based on estimation of $R[n]$ are not guaranteed to be nonnegative at all frequencies [1]. An important factor in achieving a physically reasonable estimate of the power spectrum is the choice of window (function $c_w[n]$ in Equation 9.17) applied to the estimate of $R[n]$. Choosing a window with a nonnegative Fourier transform ensures that the *expected value* of the spectral estimate is nonnegative

[1]Even for estimating $R[n]$ up to $n = 511$, the number of segmented cross-correlations which can be averaged with this small amount of data does not meet the requirement given by Equation 9.21. Because this equation was derived from a worst-case analysis of the variance in the spectral estimate, it tends to overestimate the number of averages needed to obtain a useful result. The experimental results in this section demonstrate that a somewhat smaller number of averages can be used in practice.

at all frequencies. (The spectral estimate itself may still be negative if its variance is excessive.) Since $c_w[n]$ is an even function, its Fourier transform is real and even but not necessarily nonnegative. For the idle channel data examined in this section, $c_w[n]$ is chosen to be the convolution

$$c_w[n] = w_K[n] * w_K[-n], \tag{12.1}$$

where $w_K[n]$ is a 512-point Kaiser window with $\beta = 4.5$. By the properties of Fourier transforms,

$$\mathcal{F}\{c_w[n]\} = |\mathcal{F}\{w_K[n]\}|^2 \geq 0. \tag{12.2}$$

Figure 12-14 shows the idle channel spectrum of the modulator measured by segmented correlation. The estimated spectrum, which is normalized to a FS input, is strictly positive and physically reasonable. The improved resolution gained by segmented correlation is illustrated in Figure 12-15, which compares the spectrum obtained by estimating $R[n]$ up to $n = 511$ with averaging 256-point FFTs of experimental data. A Kaiser window with $\beta = 4.5$ is applied to the binary output codes prior to calculating the 256-point FFTs. Also plotted in the figure are spectra obtained by including fewer segmented correlation estimates (e.g., only $\hat{R}_{auto}[n]$ and $\hat{R}_0[n]$) in the assembled estimate for $R[n]$, so that $R[n]$ is estimated only up to $n = 127$ or $n = 255$. These lower resolution spectra, along with the average of the 256-point FFTs, are normalized so that the spectral density of broadband noise matches that obtained by estimating $R[n]$ up to $n = 511$. The spectrum obtained by estimating $R[n]$ up to $n = 255$ is almost identical to the average of the 256-point FFTs. Estimation of $R[n]$ up to $n = 511$ effectively doubles the frequency resolution and reduces the measured in-band noise over a 19.6 MHz bandwidth by over 3 dB, to -57 dBFS. The measured in-band noise over a 39.3 MHz bandwidth is -53 dBFS. These are the lowest noise levels achieved during testing of the bandpass modulator.

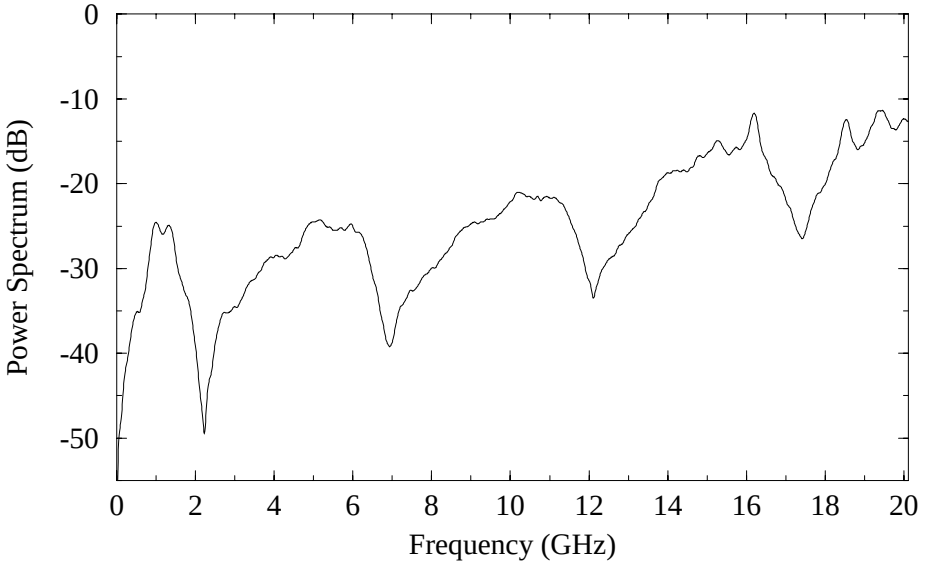


Figure 12-14: Idle channel spectrum obtained by segmented correlation, with $R[n]$ estimated up to $n = 511$ (f_s=40.2 GHz).

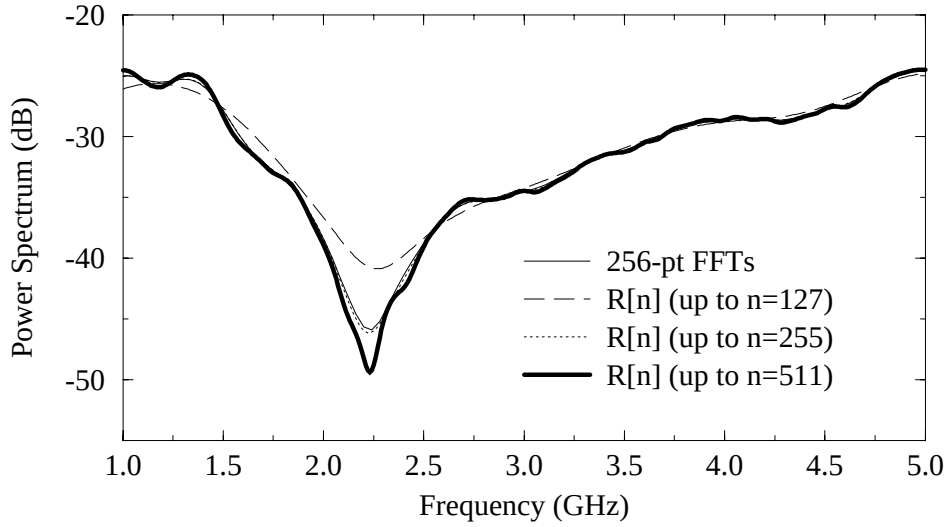


Figure 12-15: Comparison of idle channel spectra obtained by segmented correlation with 256-point FFTs of experimental data (f_s=40.2 GHz).

To compare with theory, the experimental spectrum obtained by estimating $R[n]$ up to $n = 511$ is plotted against the result of averaging 512-point FFTs of circuit simulation data in Figure 12-16. A Kaiser window with $\beta = 4.5$ is applied to the simulated output codes prior to calculating the 512-point FFTs. The resonant frequency of the simulated circuit is chosen to match the experimental data; no other fitting parameters are used. The measured and simulated in-band noise levels match almost perfectly. Since the limited frequency resolution of the 512-point FFTs degrades the simulated in-band noise by 2.5 dB, the true in-band noise of the experimental modulator over a 19.6 MHz bandwidth is probably about -59 dBFS.

12.5.6 Segmented Correlation Measurements with Input Tone

Figure 12-17 shows the measured output spectra obtained by segmented correlation and by standard 256-point FFTs when the modulator is driven by a sinusoidal input. The -27.8 dBm input at 1.70 GHz produces a -9.6 dBFS tone in the modulator output. The segmented correlation data are processed in the manner described in the last section, but a different window is applied to the estimate of $R[n]$. The window function $c_w[n]$ is still given by Equation 12.1, but in this case $w_K[n]$ is a 512-point Kaiser window with $\beta = 6.5$. The use of a window with better sidelobe suppression decreases spectral leakage from the input tone, at the expense of slightly reduced frequency resolution. For similar reasons, a Kaiser window with $\beta = 6.5$ is applied to the binary output codes prior to calculating the 256-point FFTs. The normalization of the plotted spectra is identical to that used in Figure 12-15. The resolution enhancement by segmented correlation is most clearly shown by the shape of the input tone, which becomes taller and narrower as $R[n]$ is estimated up to larger values of n. Note that the frequency resolution of the spectrum obtained by estimating $R[n]$ up to $n = 255$ matches that of the 256-point FFTs.

Unfortunately, the spectra obtained by estimating $R[n]$ up to $n = 255$ and $n = 511$ are not accurate near the quantization noise minimum at quarter-wave resonance (2.23 GHz).

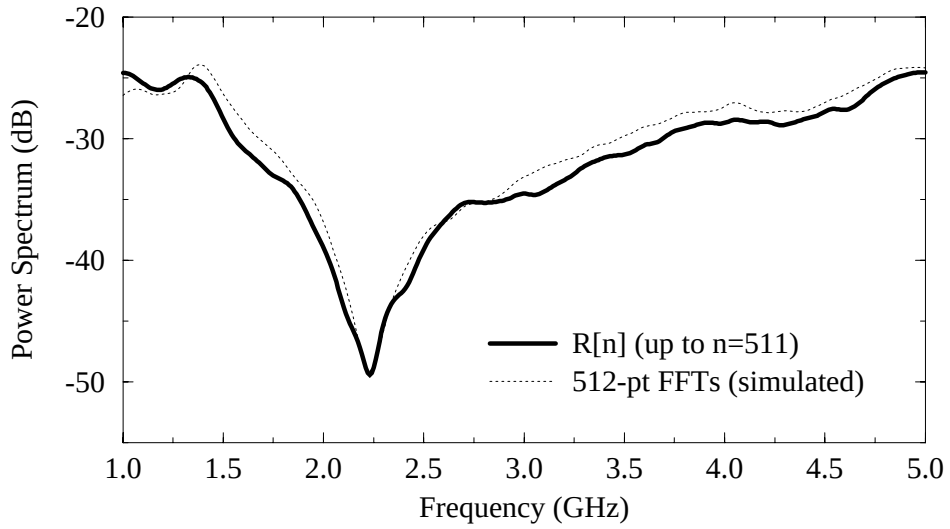


Figure 12-16: Comparison of experimental spectrum obtained by segmented correlation with 512-point FFTs of simulated data (f_s=40.2 GHz).

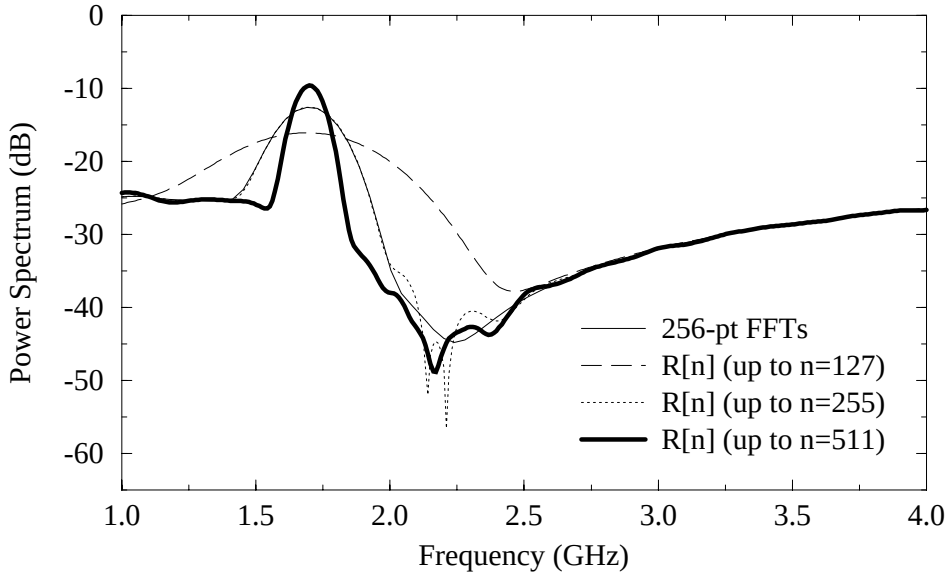


Figure 12-17: Measured output spectra obtained by segmented correlation and 256-point FFTs, with -27.8 dBm input at 1.70 GHz (f_s=40.2 GHz).

According to Equation 9.20, the variance of a segmented correlation spectral estimate is proportional to the square of $S_L(e^{j\Omega})$, which is a smeared version of the true power spectrum, with frequency resolution approximately that of an L-point (in this case, 128-point) FFT. A question not explicitly addressed in Chapter 9 is whether or not the signal power due to the input contributes to $S_L(e^{j\Omega})$ and increases the variance of the spectral estimate near the input frequency. The answer to this question depends on the randomness of the input signal phase in each 256-bit sequence captured by the on-chip acquisition memory. If the sinusoidal input were phase-locked to the loading and unloading cycles of the modulator test chip, the input signal phase in each 256-bit sequence would be fixed. In this case, the component of the binary output codes due to the input signal would be deterministic and would not increase the variance of the spectral estimate. Such phase-locking cannot be accomplished in this experiment, as the Josephson oscillator which clocks the modulator test chip is asynchronous with the frequency synthesizers used to generate the input signal. Consequently, the component of the binary output codes due to the input signal is random (in phase) and does increase the variance of the spectral estimate. Since $S_L(e^{j\Omega})$ only has the frequency resolution of a 128-point FFT, the variance of the spectral estimate is increased over a broad band of frequencies centered at the input frequency (and closely approximated as the band of frequencies spanned by the input tone shown with the long dashed line in Figure 12-17). The estimation error due to the increased variance significantly compromises the accuracy of the spectrum near quarter-wave resonance, where the true quantization noise is small. The "power spectrum" obtained by estimating $R[n]$ up to $n = 255$ is even negative for frequencies between the two cusps at 2.14 and 2.21 GHz. (Figure 12-17 shows only the magnitudes, not the signs of the estimated spectra.) The spectrum obtained by estimating $R[n]$ up to $n = 511$ is positive at all frequencies but exhibits anomalous wiggles near quarter-wave resonance, and the location of the noise minimum is not consistent with that seen in the 256-point FFTs. Because of these inaccuracies, the in-band noise of the modulator cannot be calculated from the segmented correlation spectral estimates shown in Figure 12-17.

In principle, these inaccuracies can be avoided by calculating *residual noise spectra*, for which the sinusoidal input signal component is subtracted from each of the binary output codes prior to computing the segmented correlations. However, the high quantization noise power in the single-bit code of the modulator hinders accurate fitting of a sinusoid to a finite segment of output data, especially one which is only 256 bits long [201, 202]. Satisfactory fitting of sinusoids to the 256-bit codes is achieved with the sinusoidal signal analysis technique developed by Hong [202, 203] at Motorola. This is a least squares method in which a sinusoid is fitted to a data segment *in the frequency domain*, after both sinusoid and data segment have been windowed and Fourier transformed. Superior numerical robustness can be obtained by restricting the frequency range over which the fitting procedure is applied (ignoring, for instance, frequencies where the shaped quantization noise is very large). The window applied to the sinusoid and data segment can be chosen to mitigate problems due to spectral leakage. For the modulator output data studied here, a Kaiser window with $\beta = 2$ gives near-optimum results.

The sinusoids were fitted to the binary output codes with Hong's own software routines. In a collaborative arrangement, the binary output codes were electronically delivered to Hong, who processed them and returned a file listing the amplitude, phase, and normalized

frequency[2] of the best-fitted sinusoid for each 256-bit output code. For cases in which modulator output bits were skipped between loading shift register memory banks A and B, the best-fitted sinusoid has a deterministic phase jump between the 128th and 129th bits of the output code. A minor modification was made to Hong's software to take into account such phase jumps [204].

Figure 12-18 shows the residual noise spectra that are calculated after the best-fitted sinusoids have been subtracted from the data segments. The dips in the noise spectra near 1.7 GHz are artifacts of Hong's algorithm, which cannot perfectly distinguish between signal and noise energy at the input frequency. Nonetheless, the cancellation of the input signal component is accurate enough that the errors in the spectral estimates near the quantization noise minimum at quarter-wave resonance are substantially reduced. Near this minimum, the spectral estimates are physically reasonable and qualitatively similar to those shown in Figure 12-15. For the spectrum obtained by estimating $R[n]$ up to $n = 511$, the noise minimum is now located at the expected frequency (2.23 GHz). For the spectra obtained by estimating $R[n]$ up to $n = 255$ and $n = 511$, the in-band noise levels over a 19.6 MHz bandwidth are higher than in the case of no input (Figure 12-15) by 1.7 and 2.3 dB, respectively. This increase in noise is probably not real, as it is not observed in the average of the 256-point FFTs. Most likely, some small errors in the segmented correlation spectral estimates remain due to imperfect fitting of the sinusoids to the binary output codes. As suggested earlier, the best way to eliminate such errors would be to phase-lock the input to the loading and unloading cycles of the modulator test chip.

[2]In fitting a sinusoid to a discrete-time data sequence, it is important to know the normalized frequency, the ratio of input frequency to sampling rate. While the input frequency (1.70 GHz) is precisely set by the frequency synthesizer, the normalized frequency slightly drifts because of the relatively poor stability of the Josephson clock source. Therefore, Hong's technique is used to estimate not only the amplitude and phase but also the normalized frequency of the best-fitted sinusoid.

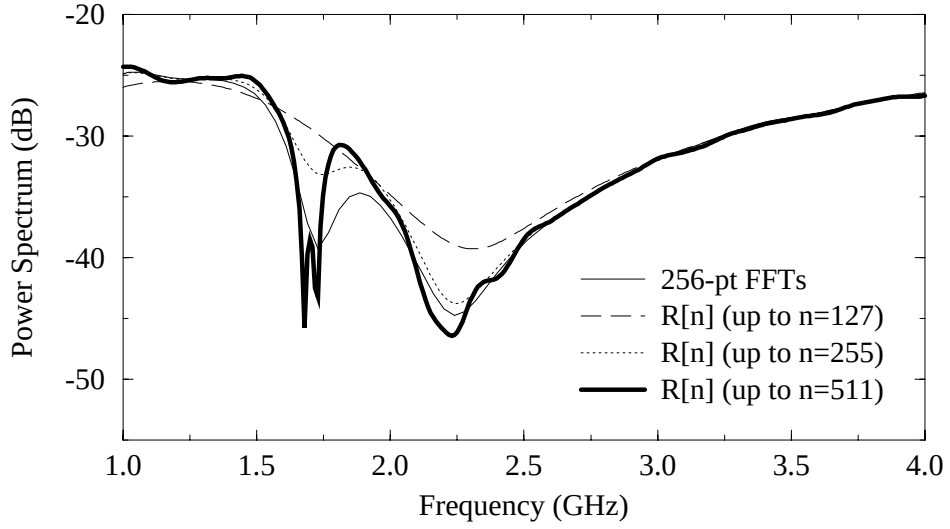


Figure 12-18: Residual noise spectra obtained by segmented correlation and 256-point FFTs, with the best-fitted sinusoids subtracted from the data segments.

Part IV

Epilogue

Chapter 13

Conclusions

13.1 Thesis Summary

The potential of superconducting technology for direct analog-to-digital conversion of multi-GHz RF signals was investigated by designing and experimentally demonstrating a superconducting bandpass $\Delta\Sigma$ modulator. Several advantages of superconducting electronics contribute to the high performance of the modulator. A resonator with a very high value of Q is formed from a superconducting microstrip transmission line. A very fast comparator is realized with Josephson junctions, whose fast switching speed allows sampling rates in excess of 40 GHz. The intrinsic quantization of the SFQ voltage pulses generated by the comparator ensures that the feedback pulses delivered to the resonator have a precise and uniform area, even at the highest sampling rates. Capacitive coupling of the input signal permits a favorable tradeoff between the loaded Q of the resonator and the input sensitivity of the modulator. Even with loaded Q values above 5000, the circuit is more than an order of magnitude more sensitive than typical semiconductor bandpass $\Delta\Sigma$ modulators.

A linearized model of the modulator was used to explain the main features of its output spectra, including the appearance of aliased modes. The predictions of the linearized model were compared to the results from detailed circuit simulations of the modulator. The most serious discrepancy between the simulation results and the predictions of the linearized model is excess noise in the simulated spectra at the center frequency of the modulator. Signal-dependent jitter due to delay modulation in the comparator of the modulator was shown to be the cause of this excess noise, which limits the SNR achieved by the circuit. The delay modulation in the comparator was not found to degrade the linearity of the modulator. According to simulations, the in-band IM distortion over a 39 MHz signal bandwidth is better than -69 dBFS, corresponding to roughly 11 bits of linearity. In-band IM distortion is even lower over narrower bandwidths.

While the superconducting bandpass $\Delta\Sigma$ modulator is a simple circuit, demonstration of a Josephson circuit operating at clock rates in the tens of GHz is often hindered by experimental problems. To overcome such problems, new strategies and techniques were developed for the high speed testing of multi-GHz circuits. The optical clocking system implemented in this project permits high speed triggering of superconducting circuits, unencumbered by the bandwidth limitations of an electrical interface to room-temperature electronics. The system is capable of triggering superconducting circuits with a variety of

pulse patterns, at clock frequencies from 80.6 MHz up to 20.6 GHz. Alternatively, even higher frequency triggering of a superconducting circuit can be accomplished by using a Josephson oscillator as an internal clock source. Capturing the data generated by the superconducting bandpass $\Delta\Sigma$ modulator with an on-chip acquisition memory greatly relaxes the bandwidth requirements for readout, but the small size of the on-chip memory severely limits the frequency resolution of spectral estimates based on standard FFTs, hindering accurate measurement of ADC performance. Higher resolution estimates of the output spectrum are obtained with the segmented correlation technique introduced in this dissertation. While demonstrated here with the superconducting bandpass $\Delta\Sigma$ modulator, this powerful technique is applicable to testing a wide range of ADCs in different technologies.

These testing methods have been applied in demonstrating a superconducting bandpass $\Delta\Sigma$ modulator fabricated in a niobium integrated circuit process with 1 kA/cm^2 critical current density for the Josephson junctions. The noise shaping of the experimental modulator closely matches that predicted by circuit simulation. The measured center frequency (2.23 GHz at sampling rates near 40 GHz), sampling rate (up to 45 GHz), dynamic range (greater than 57 dB over a 19.6 MHz bandwidth), and input sensitivity (-17.4 dBm FS) are the highest reported to date in any technology. The SNR (49 dB over a 20.8 MHz bandwidth) is limited by the frequency resolution of the measurement but still exceeds the SNRs of semiconductor modulators with comparable center frequencies. Such record-setting performance clearly confirms that superconducting technology is an attractive candidate for realizing direct analog-to-digital conversion of RF signals in the GHz range.

13.2 Future Work

While the performance of the superconducting bandpass $\Delta\Sigma$ modulator demonstrated in this project is the best shown to date and represents a significant advance in the state of the art, even higher performance is required for the RF ADC in a typical software radio receiver. As an example, consider digitizing an entire cellular band with a width of 25 MHz. From the simulation results presented in Chapter 8, one would estimate[1] that the superconducting modulator achieves an SNR of about 57 dB and an SFDR of about 75 dB over a 25 MHz bandwidth when operating at a 40 GHz sampling rate. An SNR of 57 dB over a 25 MHz bandwidth is 12 dB lower than that calculated in Section 1.2 for the example of an ideal 8-bit ADC oversampling the signal at 4 GHz (OSR=80). Since the SNR of an ideal 8-bit ADC oversampling at 4 GHz is only marginally adequate for the software radio application, the SNR of the superconducting modulator should be improved by at least 15 dB. To meet the dynamic range requirements of most software radio systems, the SFDR of the superconducting modulator should be improved by at least 20 dB, to about 95 dB.

An important finding in this thesis is that the SNR of the modulator is limited by delay modulation effects in the comparator. As discussed in Section 8.3, the signal-dependent jitter due to delay modulation can be reduced by placing a latch between the comparator and the circuitry which delivers feedback to the resonator, but the delay added by the latch

[1]The estimated SFDR of the modulator for a 25 MHz bandwidth and a 40 GHz sampling rate is an extrapolation from the results of Figure 8-11, which shows the worst-case in-band IM distortion for a 39 MHz bandwidth and a 20 GHz sampling rate. Since simulations show that the IM distortion is spectrally shaped in the same way as the quantization noise, the magnitude of the largest in-band distortion product is inversely proportional to the oversampling ratio.

reduces the stability of the modulator and decreases the maximum sampling rate, limiting the improvement in SNR. Designing comparator and feedback circuits which provide the optimum tradeoff between signal-dependent jitter and excess loop delay in order to obtain the highest SNR is an important topic of future research. However, preliminary investigations conducted during this project indicate that the increase in SNR that can be achieved with improved comparator and feedback circuits is likely to be modest and significantly less than 15 dB. Such circuit changes would also not improve the SFDR of the modulator.

Another approach to increasing the SNR of the modulator is to fabricate it in a more advanced Josephson integrated circuit process. For instance, if the modulator were fabricated in the latest TRW niobium process [205], the critical current density of the Josephson junctions would be increased from 1 kA/cm^2 to 8 kA/cm^2. Since the circuit time constants are inversely proportional to the square root of the critical current density [165], the magnitude of the delay modulation would be reduced by $\sqrt{8}$, increasing the SNR by about 9 dB. In addition, the shorter time constants would allow the circuit to operate at a higher sampling rate, adding a few more dB to the SNR. If the switch to a more advanced Josephson process is combined with a more optimized design of the modulator, a 15 dB improvement in SNR may indeed be achievable. The increase in oversampling ratio would also improve the SFDR since the loop gain of the modulator over the band of interest would be higher, but obtaining the desired 20 dB improvement would require sampling rates (e.g., 400 GHz) which might not be attainable even if niobium technology were scaled to deep submicron dimensions [165].

A more promising approach to obtaining the desired improvements in SNR and SFDR is to combine a couple of superconducting bandpass $\Delta\Sigma$ modulators in a two-stage ADC architecture, as shown below in Figure 13-1. The first bandpass modulator produces a 1-bit output code which is an initial estimate of the analog input signal. This initial estimate is then converted back into an analog representation with a 1-bit DAC and a continuous-time bandpass filter which rejects the out-of-band quantization noise generated by the

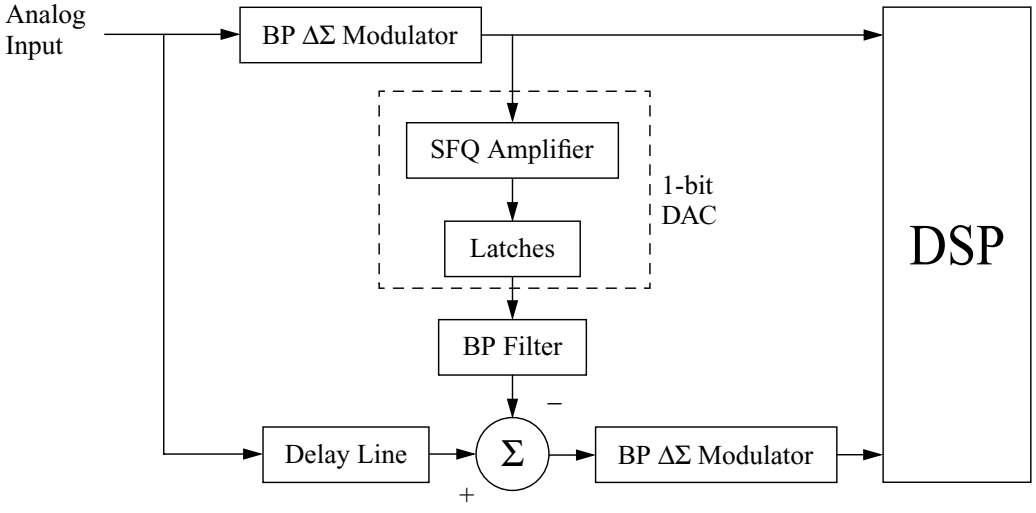


Figure 13-1: Two-stage architecture for superconducting bandpass ADC.

first bandpass modulator. This filtered signal is then subtracted[2] from a delayed version of the analog input to form a residual error signal, which is measured with the second bandpass modulator. The measured error is then cancelled from the initial estimate of the analog input with a digital signal processor (DSP). It should be pointed out this proposed architecture differs from the cascaded modulator (so-called "MASH") architectures that are typically implemented in semiconductor technology [206], in which the signal fed to the second modulator is the difference between the input and output of the quantizer in the first modulator. Here the signal fed to the second modulator is the difference between the (filtered) output of the first modulator and the analog input itself (after a suitable delay). In fact, the proposed architecture is more similar to the two-step subranging architecture employed in many conventional Nyquist-rate ADCs [207].

The performance of the proposed architecture depends critically on the accuracy of the 1-bit DAC used to convert the digital output of the first modulator back into analog form. As pointed out many times in this thesis, the SFQ voltage pulses generated by Josephson circuits have a very precise area. The necessary power gain can be added to the 1-bit DAC by passing the SFQ pulses through amplifying JTLs and splitters. Virtually all random and signal-dependent jitter can be eliminated by retiming these SFQ pulses with latches placed at the output of the 1-bit DAC. This solves the delay modulation problem which limits the SNR of the circuit demonstrated in this work. Since these latches are outside the feedback loops of the bandpass modulators, their delays do not reduce the maximum sampling rate of the circuit and are easily compensated by increasing the length of the delay line between the analog input and the second modulator stage.

Ideally, the bits of resolution achieved with this two-stage architecture should be double that achieved with a single bandpass modulator. In practice, the performance improvement will be limited by the difficulty of matching the gain and delay of the two paths between the analog input and the second bandpass modulator. However, even with only 10% matching between the paths, both the SNR and SFDR would be improved by 20 dB, enough to meet the software radio requirements. Of course, if better matching were achieved, or if the Josephson circuitry were implemented in a more advanced process with a critical current density higher than 1 kA/cm^2, even higher performance could be obtained.

Developing a practical scheme for tuning the center frequency of the modulator is another significant area of research. A small tuning range would be helpful to correct for manufacturing tolerances, while a larger tuning range would provide valuable flexibility in signal reception. The resonant frequencies of high-T_c superconducting microstrip transmission lines have been electrically tuned by changing the dielectric constant of a ferroelectric film such as $SrTiO_3$ with an applied bias voltage [208], but a ferroelectric film may not be materials compatible with a low-T_c Josephson integrated circuits process. In principle, the resonant frequency could be varied over a wide range by switching in and out transmission line sections of different lengths with RF-MEMS devices [209], but RF-MEMS devices have yet to be integrated with Josephson technology.

One approach to tuning which would not require any changes to a Josephson integrated circuits process is suggested by the analysis of aliased modes presented in Chapter 7. The location of the minimum in the quantization noise spectrum due to an aliased mode depends

[2]If magnetic coupling is used to combine the signals, the necessary signal inversion is easily accomplished by using opposite directions for the windings.

on the sampling rate. Consequently, if the suppression of the quantization noise at the modulator center frequency were due to an aliased mode, small changes in the sampling rate could be used to effect a large tuning range. For instance, if the transmission line had a physical resonance at 18 GHz, and the sampling rate were 20 GHz, the minimum in the quantization noise due to the aliased mode would be located at 2 GHz. If the sampling rate were raised by 5% to 21 GHz, the minimum in the quantization noise due to the aliased mode would move up to 3 GHz, an increase of 50%. Of course, the practicality of this tuning scheme depends upon the ADC performance achieved by a bandpass modulator operating in this "aliased regime", which has yet to be studied.

Integration of an RSFQ decimator on the same chip as the superconducting bandpass $\Delta\Sigma$ modulator is highly desirable for use in an actual system. The design of such a decimator was not studied in this project and remains an important topic for future research. A useful starting point for such a design would be the low-pass decimators described in [72, 188], but the decimator for the bandpass modulator would be a more complex circuit, especially if tuning of the center frequency is required.

Because the amount of data that could be acquired with the test setup was relatively modest, the segmented correlation technique introduced in this dissertation was only experimentally demonstrated with the superconducting bandpass $\Delta\Sigma$ modulator in a limited capacity, effectively doubling the frequency resolution of a standard 256-point FFT. The ultimate capabilities and limitations of this ADC testing method will only be discovered when it is applied to obtain much greater enhancements in frequency resolution. It was postulated in Section 12.5.6 that phase-locking the analog input to the data segments being captured would improve the accuracy of the spectral estimates obtained by segmented correlation. Confirming this claim experimentally would be a valuable exercise.

As discussed in Chapter 12, problems with magnetic contamination which caused faulty circuit operation were encountered a few times during testing of the Josephson chips. Magnetic contamination may also explain why the dependence of circuit yield on junction count seemed to be weaker than that predicted by a simple point defect model. (Another researcher in the field has observed similar yield statistics [210]). Since the field from a magnetized particle of dust or dirt may extend over a fairly large area of the chip, even small Josephson circuits may be vulnerable to such contamination. In general, developing a better understanding of magnetic contamination and learning how to avoid it would help make superconducting technology more practical.

The optical clocking system implemented in this thesis project is well-suited to testing Josephson circuits but is large, delicate, and maintenance demanding. In a real system, optical clocking will only be practical if a more compact and reliable optical source can be used. While sources such as mode-locked erbium-doped fiber lasers [82] generate optical pulses at multi-GHz repetition rates and are reasonably compact, their operating wavelengths are too long to produce a fast response from the silicon MSM photodiodes employed in this work. Therefore, unless a compact source is developed which generates multi-GHz pulses of short wavelength light, the silicon MSM photodiode will have to be replaced with a type more suitable for longer wavelengths, possibly by fabricating the Josephson circuitry on a different substrate material (e.g., InGaAs).

Appendix A

STF and NTF of Modulator Based on LC Resonator

The signal and noise transfer functions of the superconducting bandpass $\Delta\Sigma$ modulator based on an LC resonator (Figure 7-1) are calculated by applying z-transforms to the difference equations describing the equivalent discrete-time system (Equations 7.10). Letting $z = e^{j\omega T}$, the z-transform of a sequence $x[n]$ is

$$X(z) = X(e^{j\omega T}) = \sum_{n=-\infty}^{\infty} x[n]e^{-j\omega nT}. \tag{A.1}$$

Applying z-transforms to both sides of Equations 7.10 gives

$$U(e^{j\omega T}) = -\cos(\omega_0 T)e^{-j\omega T}E(e^{j\omega T}) - \frac{2}{\omega_0\Phi_0}\sin(\omega_0 T)e^{-j\omega T}V_C(e^{j\omega T}) + G_u(e^{j\omega T}), \tag{A.2a}$$

$$V_C(e^{j\omega T}) = -\frac{\omega_0\Phi_0}{2}\sin(\omega_0 T)e^{-j\omega T}E(e^{j\omega T}) + \cos(\omega_0 T)e^{-j\omega T}V_C(e^{j\omega T}) + G_{vc}(e^{j\omega T}). \tag{A.2b}$$

$G_u(e^{j\omega T})$ and $G_{vc}(e^{j\omega T})$ are the z-transforms of $g_u[n]$ and $g_{vc}[n]$, whose definitions (Equations 7.9) can be rewritten as

$$g_u[n] = \int_{-\infty}^{\infty} v_{in}(\tau)\widetilde{h}_u(nT-\tau)d\tau, \tag{A.3a}$$

$$g_{vc}[n] = \int_{-\infty}^{\infty} v_{in}(\tau)\widetilde{h}_{vc}(nT-\tau)d\tau, \tag{A.3b}$$

where $\widetilde{h}_u(t)$ and $\widetilde{h}_{vc}(t)$ equal $h_u(t)$ and $h_{vc}(t)$ (defined in Equations 7.5) over the time interval $0 \le t \le T$ and zero elsewhere:

$$\widetilde{h}_u(t) = \begin{cases} h_u(t) = \frac{2}{\Phi_0}\cos\omega_0 t & \text{if } 0 \le t \le T, \\ 0 & \text{otherwise,} \end{cases} \tag{A.4a}$$

$$\widetilde{h}_{vc}(t) = \begin{cases} h_{vc}(t) = \omega_0 \sin\omega_0 t & \text{if } 0 \le t \le T, \\ 0 & \text{otherwise.} \end{cases} \tag{A.4b}$$

According to Equation A.3a, discrete-time sequence $g_u[n]$ can be considered samples of a continuous-time signal $g_{cu}(t)$ given by the convolution

$$g_{cu}(t) = \widetilde{h}_u(t) * v_{in}(t). \tag{A.5}$$

By the convolution theorem of Fourier transforms,

$$G_{cu}(j\omega) = \widetilde{H}_u(j\omega)V_{in}(j\omega). \tag{A.6}$$

Assuming that $V_{in}(j\omega) = 0$ for $|\omega| \geq \pi/T$, so that no aliasing occurs, the Nyquist sampling theorem provides a simple relation between $G_u(e^{j\omega T})$ and $G_{cu}(j\omega)$:

$$G_u(e^{j\omega T}) = \tfrac{1}{T}G_{cu}(j\omega) = \tfrac{1}{T}\widetilde{H}_u(j\omega)V_{in}(j\omega) \quad \text{for } |\omega| \leq \pi/T. \tag{A.7}$$

(Since $G_u(e^{j\omega T})$ is a periodic function of ω with period $2\pi/T$, only frequencies for which $|\omega| \leq \pi/T$ need be considered here. To simplify the visual presentation, the condition $|\omega| \leq \pi/T$ is not explicitly stated in the equations to follow but is assumed throughout the analysis.) If the sequence $v_{in}[n]$ is defined to be the sampled input voltage,

$$v_{in}[n] = v_{in}(nT), \tag{A.8}$$

the z-transform of $v_{in}[n]$ equals

$$V_{in}(e^{j\omega T}) = \frac{1}{T}V_{in}(j\omega). \tag{A.9}$$

Thus Equation A.7 can be expressed as

$$G_u(e^{j\omega T}) = \widetilde{H}_u(j\omega)V_{in}(e^{j\omega T}). \tag{A.10}$$

Similarly, it follows from Equation A.3b that

$$G_{vc}(e^{j\omega T}) = \widetilde{H}_{vc}(j\omega)V_{in}(e^{j\omega T}). \tag{A.11}$$

By the definition of the Fourier transform,

$$\widetilde{H}_u(j\omega) = \int_{-\infty}^{\infty} \widetilde{h}_u(t)e^{-j\omega t}dt = \frac{2}{\Phi_0}\int_0^T \cos(\omega_0 t)e^{-j\omega t}dt, \tag{A.12a}$$

$$\widetilde{H}_{vc}(j\omega) = \int_{-\infty}^{\infty} \widetilde{h}_{vc}(t)e^{-j\omega t}dt = \omega_0\int_0^T \sin(\omega_0 t)e^{-j\omega t}dt. \tag{A.12b}$$

After evaluating the integrals with standard methods, $\widetilde{H}_u(j\omega)$ and $\widetilde{H}_{vc}(j\omega)$ are found to be

$$\widetilde{H}_u(j\omega) = \frac{2}{\Phi_0}\cdot\frac{j\omega + \omega_0\sin(\omega_0 T)e^{-j\omega T} - j\omega\cos(\omega_0 T)e^{-j\omega T}}{\omega_0^2 - \omega^2}, \tag{A.13a}$$

$$\widetilde{H}_{vc}(j\omega) = \omega_0\frac{\omega_0 - j\omega\sin(\omega_0 T)e^{-j\omega T} - \omega_0\cos(\omega_0 T)e^{-j\omega T}}{\omega_0^2 - \omega^2}. \tag{A.13b}$$

Therefore, Equations A.10 and A.11 become

$$G_u(e^{j\omega T}) = \frac{2}{\Phi_0} \cdot \frac{j\omega + \omega_0 \sin(\omega_0 T)e^{-j\omega T} - j\omega \cos(\omega_0 T)e^{-j\omega T}}{\omega_0^2 - \omega^2} V_{in}(e^{j\omega T}), \tag{A.14a}$$

$$G_{vc}(e^{j\omega T}) = \omega_0 \frac{\omega_0 - j\omega \sin(\omega_0 T)e^{-j\omega T} - \omega_0 \cos(\omega_0 T)e^{-j\omega T}}{\omega_0^2 - \omega^2} V_{in}(e^{j\omega T}). \tag{A.14b}$$

Substituting these results into Equations A.2 and eliminating variable $V_C(e^{j\omega T})$ from the system of equations, one obtains

$$\begin{aligned} U(e^{j\omega T}) = \frac{j2\omega}{\Phi_0} \cdot \frac{1 - 2\cos(\omega_0 T)e^{-j\omega T} + e^{-j2\omega T}}{(\omega_0^2 - \omega^2)(1 - \cos(\omega_0 T)e^{-j\omega T})} V_{in}(e^{j\omega T}) \\ + \frac{-\cos(\omega_0 T)e^{-j\omega T} + e^{-j2\omega T}}{1 - \cos(\omega_0 T)e^{-j\omega T}} E(e^{j\omega T}). \end{aligned} \tag{A.15}$$

Since the modulator output $y[n]$ is the sum of the comparator input $u[n]$ and the quantization error $e[n]$,

$$\begin{aligned} Y(e^{j\omega T}) &= U(e^{j\omega T}) + E(e^{j\omega T}) \\ &= \mathrm{STF}(e^{j\omega T})V_{in}(e^{j\omega T}) + \mathrm{NTF}(e^{j\omega T})E(e^{j\omega T}) \quad \text{for } |\omega| \le \pi/T, \end{aligned} \tag{A.16}$$

where the signal transfer function is

$$\mathrm{STF}(e^{j\omega T}) = \frac{j2\omega}{\Phi_0} \cdot \frac{1 - 2\cos(\omega_0 T)e^{-j\omega T} + e^{-j2\omega T}}{(\omega_0^2 - \omega^2)(1 - \cos(\omega_0 T)e^{-j\omega T})}, \tag{A.17}$$

and the noise transfer function is

$$\mathrm{NTF}(e^{j\omega T}) = \frac{1 - 2\cos(\omega_0 T)e^{-j\omega T} + e^{-j2\omega T}}{1 - \cos(\omega_0 T)e^{-j\omega T}}. \tag{A.18}$$

The condition $|\omega| \le \pi/T$, assumed throughout the analysis, is restated in Equation A.16 for emphasis.

Appendix B

Transmission Line Resonator Properties

The bandpass $\Delta\Sigma$ modulator demonstrated in this thesis project employs a superconducting transmission line resonator. This appendix reviews key properties of such a resonator, including the total stored energy, average power dissipation, and loaded Q. The Thévenin equivalent voltage of the resonator when capacitively coupled to a signal source near resonant frequency ω_0 is also calculated. These results were used in Section 7.2.1 in deriving a quantitative relationship between the loaded Q of the resonator and the input sensitivity of the modulator.

The properties considered here characterize the resonator when it is operated as an open-loop element, without any feedback pulses from the SFQ comparator. A circuit model suitable for analyzing these properties can be derived from the modulator schematic (Figure 7-12) by replacing the SFQ comparator with a short circuit to ground, as shown in Figure B-1. The propagation delay T_d and length l of the transmission line are related by [147]

$$T_d = l\sqrt{LC}, \tag{B.1}$$

where L and C are the inductance and capacitance per unit length, respectively. This circuit model is now applied in the sections to follow.

B.1 Total Stored Energy

Assuming that the load placed on the resonator by circuit elements R_s and C_c is small (a necessary condition for even modest values of loaded Q), the total stored energy W_t is approximately that of an unloaded transmission line resonator (with $C_c = 0$). The first step in calculating W_t for the unloaded resonator is to find the current and voltage waveforms along the transmission line. In general, the waveforms along the transmission line can be considered a superposition of forward and backward traveling waves [147], so the complex amplitudes for voltage and current can be expressed as a function of position x,

$$V(x) = Ae^{-jkx} + Be^{jkx}, \tag{B.2a}$$

$$I(x) = \frac{Ae^{-jkx}}{Z_0} - \frac{Be^{jkx}}{Z_0}, \tag{B.2b}$$

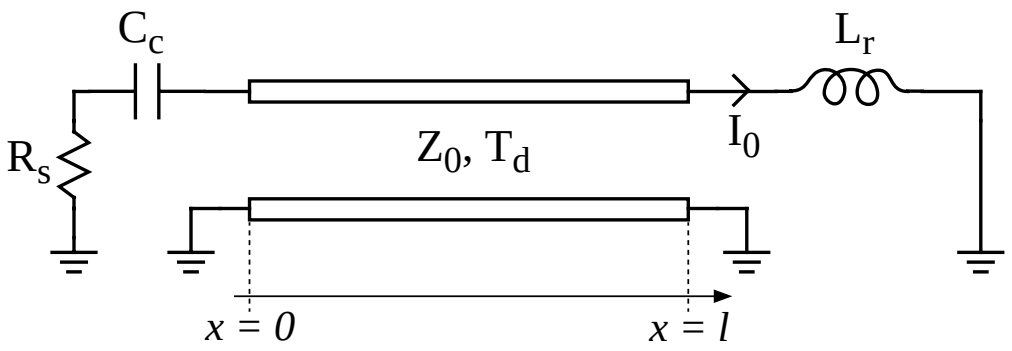


Figure B-1: Circuit model for determining properties of transmission line resonator.

where the wave vector k at resonant frequency ω_0 equals

$$k = \omega_0 \sqrt{LC}. \tag{B.3}$$

Coefficients A and B are determined by applying boundary conditions at each end of the transmission line:

$$I(0) = 0, \tag{B.4a}$$
$$I(l) = I_0, \tag{B.4b}$$

where I_0 is the amplitude of the oscillating current through L_r (assumed to be real). After applying these boundary conditions and obtaining A and B, Equations B.2 become

$$V(x) = \frac{jI_0 Z_0 \cos kx}{\sin kl}, \tag{B.5a}$$
$$I(x) = \frac{I_0 \sin kx}{\sin kl}. \tag{B.5b}$$

From Equations B.1 and B.3, it follows that $kl = \omega_0 T_d$, so

$$V(l) = jI_0 Z_0 \cot kl = jI_0 Z_0 \cot \omega_0 T_d. \tag{B.6}$$

The final boundary condition to be applied is that the voltage given by this expression must equal the voltage drop across inductor L_r, equal to $j\omega_0 L_r I_0$. After equating expressions and cancelling terms, the resonance condition which determines ω_0 is obtained:

$$\omega_0 L_r = Z_0 \cot \omega_0 T_d. \tag{B.7}$$

There are three significant contributions to the total stored energy of the resonator: the electric field inside the transmission line, the magnetic field inside the transmission line, and the energy stored in inductor L_r. Ignoring dissipation, the total stored energy remains constant at resonance, so

$$W_t = \langle W_e \rangle + \langle W_m \rangle + \frac{1}{4} L_r I_0^2, \tag{B.8}$$

where $\langle W_e \rangle$ is the time-averaged electric energy stored in the transmission line, and $\langle W_m \rangle$ is the time-averaged magnetic energy stored in the transmission line. $\langle W_e \rangle$ is calculated

by integrating the time-averaged electric energy per unit length over the length of the transmission line:

$$\langle W_e \rangle = \frac{1}{4}\int_0^l C|V(x)|^2 dx. \tag{B.9}$$

After substituting Equation B.5a and applying standard integration methods,

$$\langle W_e \rangle = \frac{CI_0^2 Z_0^2}{4\sin^2 kl}\int_0^l \cos^2(kx)dx = \frac{CI_0^2 Z_0^2}{8\sin^2 kl}(l + \sin(2kl)/2k). \tag{B.10}$$

Since $Z_0 = \sqrt{L/C}$, $T_d = l\sqrt{LC}$, and $kl = \omega_0 T_d$, Equation B.10 can be rewritten as

$$\langle W_e \rangle = \frac{I_0^2 Z_0}{8\sin^2 \omega_0 T_d}(T_d + \sin(2\omega_0 T_d)/2\omega_0). \tag{B.11}$$

Similarly,

$$\langle W_m \rangle = \frac{1}{4}\int_0^l L|I(x)|^2 dx = \frac{I_0^2 Z_0}{8\sin^2 \omega_0 T_d}(T_d - \sin(2\omega_0 T_d)/2\omega_0). \tag{B.12}$$

Substituting these expressions for $\langle W_e \rangle$ and $\langle W_m \rangle$ into Equation B.8 yields the final expression for the total stored energy W_t:

$$W_t = \frac{I_0^2}{4}\left(L_r + \frac{Z_0 T_d}{\sin^2 \omega_0 T_d}\right). \tag{B.13}$$

B.2 Average Power Dissipation and Loaded Q

Resistor R_s is the only dissipative element in the circuit of Figure B-1, so the average power dissipation at resonance equals

$$P_d = \frac{|V(0)|^2}{2}\Re e\left\{\frac{1}{R_s + \frac{1}{j\omega_0 C_c}}\right\} = \frac{|V(0)|^2}{2}\cdot\frac{\omega_0^2 R_s C_c^2}{1 + \omega_0^2 R_s^2 C_c^2}. \tag{B.14}$$

Under the assumption that the resonator is only lightly loaded by R_s and C_c, the current and voltage waveforms along the transmission line are close to those of the unloaded case, given by Equations B.5. Therefore,

$$|V(0)| \approx \frac{I_0 Z_0}{\sin kl} = \frac{I_0 Z_0}{\sin \omega_0 T_d}, \tag{B.15}$$

and P_d is approximately

$$P_d \approx \frac{I_0^2 Z_0^2}{2\sin^2 \omega_0 T_d}\cdot\frac{\omega_0^2 R_s C_c^2}{1 + \omega_0^2 R_s^2 C_c^2}. \tag{B.16}$$

An approximate expression for the loaded Q of the resonator is found by substituting Equations B.13 and B.16 into the general definition of Q (Equation 7.24):

$$Q_{ld} = \frac{\omega_0 W_t}{P_d} \approx \frac{(Z_0 T_d + L_r \sin^2 \omega_0 T_d)(1 + \omega_0^2 R_s^2 C_c^2)}{2\omega_0 R_s Z_0^2 C_c^2}. \tag{B.17}$$

Multiplying numerator and denominator by ω_0 and applying the resonance condition of

Equation B.7 give a more convenient expression for loaded Q:

$$Q_{ld} \approx \frac{(\omega_0 T_d + \sin\omega_0 T_d \cos\omega_0 T_d)(1+\omega_0^2 R_s^2 C_c^2)}{2\omega_0^2 R_s Z_0 C_c^2}. \tag{B.18}$$

B.3 Thévenin Equivalent Voltage

The Thévenin equivalent voltage of the input network (at the port connected to the SFQ comparator) is now estimated. The complete input network for the modulator of Figure 7-12 is shown in Figure B-2. In calculating the Thévenin equivalent voltage v_{th} in response to input v_{in}, all other independent sources are set to zero, so inductor L_b is connected to an incremental ground.

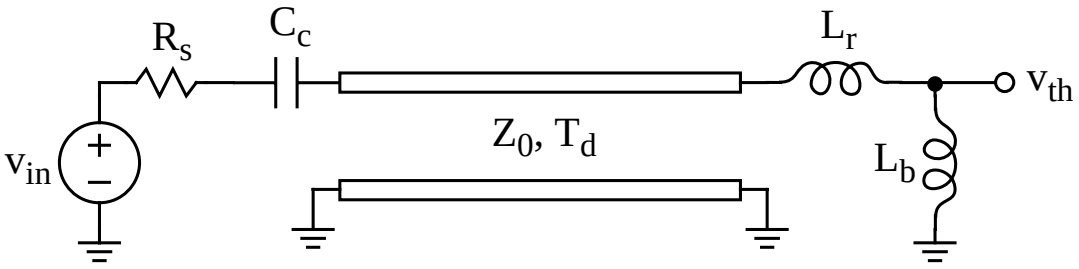


Figure B-2: Complete input network for modulator based on transmission line.

In general, the loading of the input network by inductor L_b does influence the Thévenin equivalent voltage v_{th}. Near the resonant frequency, however, the reactances of the transmission line and inductor L_r cancel, and the impedance of the network connected to L_b is much smaller than that of L_b itself. Consequently, inductor L_b can be ignored in estimating the Thévenin equivalent voltage near resonant frequency ω_0, as suggested in Figure B-3. With this simplification, the boundary conditions at the ends of the transmission line are identical [1] to those considered in Section B.1. Therefore, it follows from Equation B.5a that

$$V_{th}(j\omega_0) = \frac{-jI_1 Z_0}{\sin kl} = \frac{-jI_1 Z_0}{\sin\omega_0 T_d}. \tag{B.19}$$

The minus sign in the numerator results from defining the direction of current I_1 to be into the port of the transmission line, in contrast with the outward direction of current I_0 in Figure B-1.

Since the input impedance of the open-circuited transmission line near resonant frequency ω_0 is much smaller than the impedance of the series network formed by R_s and C_c, current I_1 is approximately

$$I_1 \approx \frac{1}{R_s + \frac{1}{j\omega_0 C_c}} V_{in}(j\omega_0). \tag{B.20}$$

Substituting this equation into Equation B.19 yields the desired relation between Thévenin

[1] Note, though, that the roles of the two ends are reversed here. The right end of the transmission line is now open-circuited.

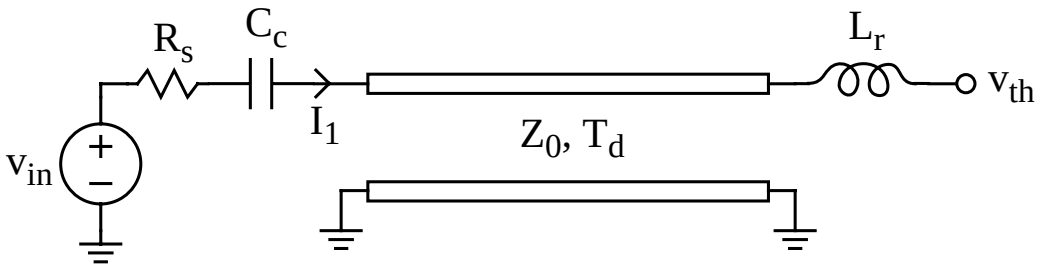


Figure B-3: Simplified input network for estimating Thévenin equivalent voltage v_{th} near resonant frequency ω_0.

equivalent voltage v_{th} and input source v_{in} near resonant frequency ω_0:

$$V_{th}(j\omega_0) \approx \frac{\omega_0 Z_0 C_c}{\sin(\omega_0 T_d)(1 + j\omega_0 R_s C_c)} V_{in}(j\omega_0). \tag{B.21}$$

Appendix C

SFQ Comparator Based on Inductive Divider

The simulations presented in Chapter 8 showed that signal-dependent jitter due to delay modulation in the SFQ comparator is the main limiting factor in the performance of the superconducting bandpass $\Delta\Sigma$ modulator implemented and experimentally demonstrated in this thesis project. This appendix describes a more complex SFQ comparator based on an "inductive divider", in which part of the kickback pulse appearing at the comparator input is retimed by an internal latch. The retiming of part of the kickback pulse decreases signal-dependent jitter, but the extra feedback delay added by the internal latch is a disadvantage for the stability of $\Delta\Sigma$ modulators. The following sections describe the operation of this alternative comparator and present the simulated performance of a bandpass $\Delta\Sigma$ modulator employing it.

C.1 Circuit Description

Figure C-1 is a schematic of the SFQ comparator based on an inductive divider. The input current i_q is split into two components i_A and i_B by the inductive current divider formed by inductors L_{IA} and L_{IB}. Ignoring the small nonlinear inductances of junctions J_2 and J_4, the input current splits according to the ratios

$$i_A = \frac{L_{IB}}{L_{IA} + L_{IB}}\, i_q, \tag{C.1a}$$

$$i_B = \frac{L_{IA}}{L_{IA} + L_{IB}}\, i_q. \tag{C.1b}$$

Current i_A is quantized by decision-making pair J_1–J_2, which operates in the same manner as the SFQ comparator discussed in Chapters 7 and 8. In the case of a binary 1 decision, the SFQ pulse generated across J_2 sets up a circulating current through the SQUID loop formed by J_2, L_{IA}, L_{IB}, and J_4. Inductances L_{IA} and L_{IB} are chosen so that this circulating current drives J_4 close to (but not above) its critical current. After an appropriate delay set by a JTL, the sampling pulse switches J_4. The SFQ pulse generated across J_4 represents a binary 1 output of the comparator and also annihilates the circulating current, resetting the circuit for the next clock cycle. In essence, the SQUID loop operates as a destructive

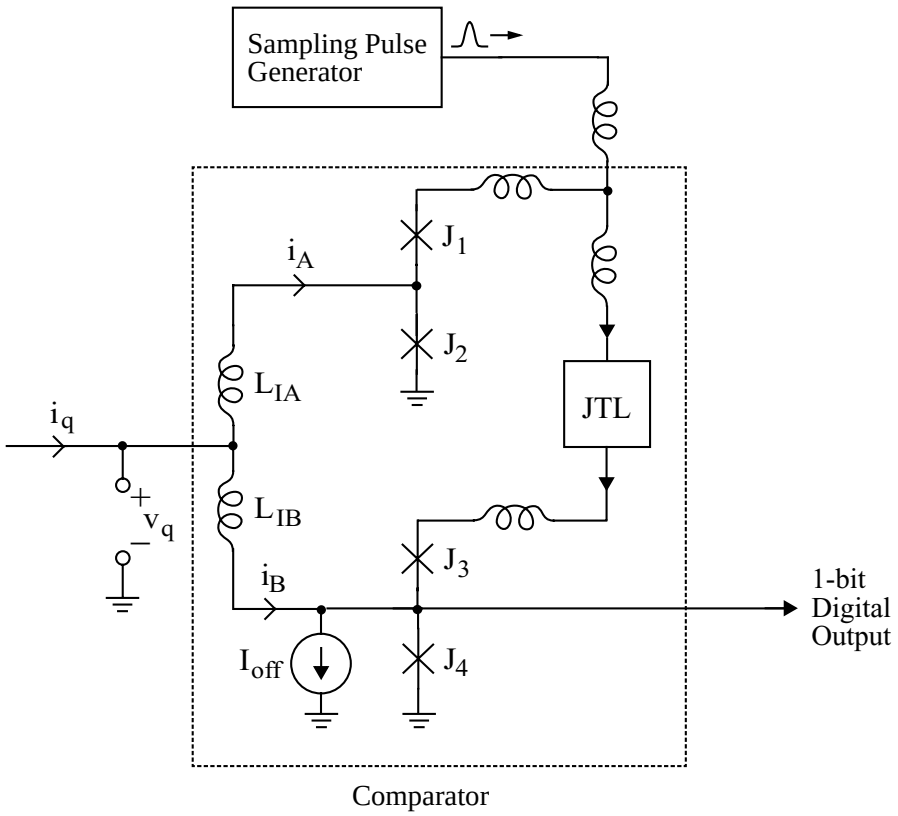


Figure C-1: SFQ comparator based on inductive divider.

readout latch, storing the decision of the upper pair J_1–J_2 as a circulating current until it is read out by the lower pair J_3–J_4. In the case of a binary 0 decision, the sampling pulse switches J_1 instead of J_2, so no circulating current is induced through the SQUID loop. With no circulating current, J_4 is not biased close to its critical current when the delayed sampling pulse arrives. Therefore, the sampling pulse switches J_3 instead of J_4. The absence of an SFQ output pulse represents a binary 0.

Despite being similar circuits, decision-making pairs J_1–J_2 and J_3–J_4 perform completely different functions within the comparator. Upper pair J_1–J_2 makes its decision based on the analog input current i_q, but lower pair J_3–J_4 operates as a digital logic circuit, making its decision based on the presence or absence of the circulating current through the SQUID loop. For proper operation, the circuit must be designed so that J_4 *only* switches in response to the circulating current, not to the component of the input current flowing through L_{IB} (given by Equation C.1b). Current source I_{off} adds an input offset[1] to the threshold of lower pair J_3–J_4 so that its decisions are not affected by the analog input (over the expected range of input current.)

The advantage of the circuit can be appreciated by considering the kickback at the input. Assume that input current i_q is supplied by a high impedance current source. When

[1]Alternatively, the threshold can be adjusted by modifying the critical currents of the junctions so that $I_{c4} > I_{c3}$. For the purpose of presentation, the inclusion of current source I_{off} in Figure C-1 makes this adjustment explicit.

the comparator makes a decision of binary 1, two distinct voltage pulses appear at the comparator input, as shown in Figure C-2. The first pulse is due to the switching of J_2, and the second pulse is due to the switching of J_4. The time delay Δt between the pulses is determined by the propagation delay of the JTL which delivers the sampling pulse to the lower pair J_3–J_4. As indicated on the figure, the areas of the two pulses depend on the relative sizes of inductors L_{IA} and L_{IB}. The pulses are equal in area if $L_{IA} = L_{IB}$. For any choice of L_{IA} and L_{IB}, the sum of the pulse areas equals Φ_0. In an integrated sense, the total kickback is identical to that of the simple two-junction SFQ comparator discussed earlier, but part of the kickback is delayed by retiming with the internal latch.

During operation of the $\Delta\Sigma$ modulator, some comparator inputs are close enough to threshold that they drive decision-making pair J_1–J_2 temporarily into a metastable state, and the switching of these junctions is slower than in other clock cycles. As discussed at length in Section 8.3, the variation in delay from clock cycle to clock cycle adds signal-dependent jitter to the pulses "fed back" to the resonator. In this case, signal-dependent jitter is added to the first voltage pulse shown in Figure C-2. On the other hand, the second voltage pulse is relatively jitter-free since it is retimed by the internal latch. Decision-making pair J_3–J_4 does not suffer from the problem of metastability since it makes its decision based on a binary quantity (the presence or absence of a circulating current through the SQUID loop). If $L_{IA} = L_{IB}$, so that the two pulses in Figure C-2 have equal area, half of the kickback would be jitter-free, and the excess in-band noise due to delay modulation in the comparator would be reduced by roughly a factor of two. Even larger reductions can be achieved by making $L_{IA} > L_{IB}$ so that the second pulse is larger in area than the first. Increasing the ratio of L_{IA} to L_{IB}, however, reduces current i_A (given by Equation C.1a). Because of the finite sensitivity of decision-making pair J_1–J_2, one cannot be too aggressive in setting the ratio of L_{IA} to L_{IB}. In practice, a compromise between minimizing signal-dependent jitter and maintaining adequate signal levels must be found.

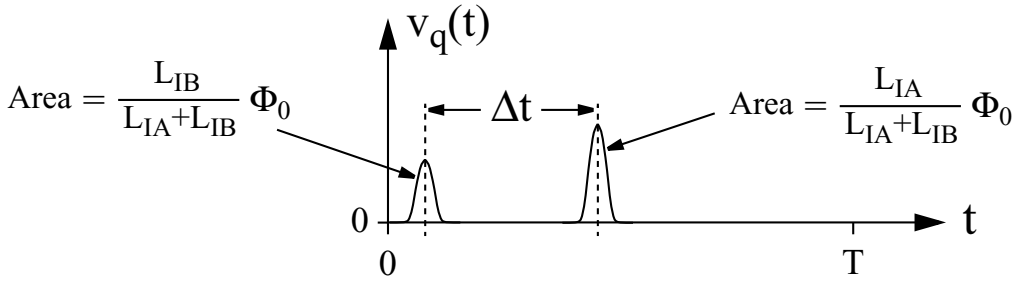


Figure C-2: Kickback voltage pulses appearing at comparator input when comparator makes a decision of binary 1.

C.2 Performance as Component of Bandpass $\Delta\Sigma$ Modulator

The SFQ comparator based on an inductive divider has both advantages and disadvantages as a component of a $\Delta\Sigma$ modulator. While retiming by the internal latch reduces excess in-band noise due to delay modulation, the feedback delay introduced by the latch decreases the maximum sampling rate and adversely affects modulator stability. To evaluate the tradeoffs involved, a bandpass $\Delta\Sigma$ modulator employing this comparator was simulated with JSIM.

The simulated circuit was derived from the one shown in Figure 8-1 by replacing the simple two-junction SFQ comparator with the comparator of Figure C-1. In this case, however, the comparator output was not loaded by an RSFQ circuit (such as the one-stage shift register depicted in Figure 8-1). Moderate loading of decision-making pair J_3–J_4 is unlikely to affect modulator performance significantly. Since this pair of junctions operates as a digital logic circuit, its switching is much less sensitive to load current than is the switching of the simple two-junction comparator, which needs to resolve analog inputs close to threshold. In contrast with the simulations presented in Chapter 8, these JSIM simulations did not include thermal noise and random clock jitter in the model. Therefore, the simulated in-band noise of the modulator may be slightly optimistic (most likely, by 1-2 dB).

In order to ensure adequate circuit margins and reliable operation, a relatively conservative choice of parameters was used in designing the comparator: $L_{IA} = L_{IB} = 3$ pH, $I_{c1} = I_{c2} = I_{c3} = I_{c4} = 271$ μA, and $I_{off} = 160$ μA. Since the ratio of L_{IA} to L_{IB} is unity, the two pulses illustrated in Figure C-2 have equal area. The small but nonzero input inductance ($L_{IA} \parallel L_{IB} = 1.5$ pH) of the comparator reduces the resonant frequencies of the modulator circuit. In the simulated circuit, this effect was compensated by reducing inductance L_r in Figure 8-1 from 20 to 18.5 pH. The JTL shown in Figure C-1 must have a large enough delay that metastable conditions of decision-making pair J_1–J_2 are resolved with high probability before the sampling pulse is delivered to decision-making pair J_3–J_4. Otherwise, decision-making pair J_3–J_4 makes frequent logical errors due to violations of its setup time, and modulator performance (such as SNR) suffers. The number of JTL stages in the simulated circuit was increased until the frequency of such errors became very low (e.g., less than 1 in 10^4 clock cycles). With a five-stage JTL, a very low error rate is obtained, and the time delay Δt between the two parts of the kickback pulse is about 26 ps. This 26 ps delay introduced by the internal latch reduces the maximum sampling rate of the modulator. The simulations presented in Chapter 8 showed that a modulator employing the simple two-junction SFQ comparator can operate reliably with high performance at a sampling rate of 40 GHz, corresponding to a sampling clock period of 25 ps. With the additional 26 ps delay, the maximum sampling rate is reduced to about 20 GHz ($T = 50$ ps).

The simulated in-band idle channel noise of the bandpass modulator at a 20 GHz sampling rate is listed in the first row of Table C.1. The reduction of signal-dependent jitter due to delay modulation increases the depth of the minimum in the noise spectrum near quarter-wave resonance. Because of the improved quality of noise-shaping, a one-octave decrease in signal bandwidth now reduces the in-band noise by over 7 dB, substantially better than the 3-4 dB achieved with the simple two-junction comparator (cf. Table 8.1) and closer to the ideal value of 9 dB. Comparing performance at the same 20 GHz sampling rate, the in-band noise over a 19.5 MHz bandwidth is almost 6 dB lower than with the simple two-junction comparator – close to the factor of two reduction expected with $L_{IA} = L_{IB}$. Comparing performance at *different* sampling rates, the in-band noise over a 19.5 MHz bandwidth is about 3 dB lower than with the simple two-junction comparator operating at 40 GHz (twice the sampling rate of this circuit).

Unfortunately, the in-band noise is degraded by the presence of large input signals. The second and third rows of Table C.1 show the simulated in-band noise of the modulator with a 2.12 GHz input signal at two different amplitudes. As the input approaches full-scale, the in-band noise increases by over 5 dB. (For sake of comparison, the in-band noise of the modulator employing the simple two-junction SFQ comparator increases by less than 1 dB

Table C.1: Simulated in-band noise of bandpass modulator employing comparator based on inductive divider. The input frequency is 2.12 GHz, and the sampling rate is 20 GHz.

	Bandwidth	
Input Amplitude	19.5 MHz	39 MHz
0 (no input)	-62.3 dBFS	-55.2 dBFS
-6.9 dBFS	-60.3 dBFS	-53.2 dBFS
-0.8 dBFS	-57.1 dBFS	-49.5 dBFS

for inputs within 1 dB of full-scale.) The increase in in-band noise is also accompanied by larger input currents to the comparator. Large comparator inputs often indicate the approach of instability in $\Delta\Sigma$ modulators [211]. In this case, the feedback delay added by the latch weakens modulator stability. The large comparator inputs reduce the effective gain of the comparator, so that the in-band noise of the modulator increases [51]. Since the quantization noise at all frequencies near quarter-wave resonance is magnified by the same scale factor, the shape of the noise spectrum near this resonance is unchanged. For this reason, a decrease in signal bandwidth from 39 to 19.5 MHz still reduces the in-band noise by over 7 dB. The increase in in-band noise with large inputs limits the peak SNR. Over a 19.5 MHz bandwidth, the peak SNR (56.3 dB) is only 1 dB better than with the simple two-junction comparator operating at 20 GHz and about 2 dB *worse* than with the simple two-junction comparator operating at 40 GHz. Hence, the feedback delay added by the latch degrades the peak SNR as much as the reduction in signal-dependent jitter improves it. Similar tradeoffs have been observed in the design of semiconductor modulators [163]. The increase in in-band noise with large inputs is a serious disadvantage in radio applications, in which very weak signals often need to be detected in the presence of strong interference [4]. Since the peak SNR was not improved, the more complex comparator described in this appendix was not chosen for the modulator implemented in this thesis project.

Appendix D

Variance of Segmented Correlation Spectral Estimate

Let $\hat{R}[n]$ be the sum of (unweighted) segmented correlation estimates

$$\hat{R}[n] = \hat{R}_{auto}[n] + \sum_{k=0}^{\frac{N}{L}} \hat{R}_{kL}[n]. \tag{D.1}$$

As discussed in Section 9.2, the variance of the estimated autocorrelation function can usually be reduced by weighting each of the terms in Equation D.1 with a tapered function such as that given by Equation 9.14. This appendix presents a worst-case calculation for the variance of the segmented correlation estimate, so such weighting is not considered here. Similarly, the window function $c_w[n]$ in Equation 9.17 is assumed to be rectangular. Therefore, by the linearity of Fourier transforms,

$$\hat{S}(e^{j\Omega}) = \mathcal{F}\{c_w[n]\hat{R}[n]\} = \mathcal{F}\{\hat{R}[n]\} = \mathcal{F}\{\hat{R}_{auto}[n]\} + \sum_{k=0}^{\frac{N}{L}} \mathcal{F}\{\hat{R}_{kL}[n]\}. \tag{D.2}$$

Since the segmented correlation estimates are obtained through successive measurements, the terms in Equation D.2 are uncorrelated, and the variance of the spectral estimate is

$$\mathrm{var}[\hat{S}(e^{j\Omega})] = \mathrm{var}[\mathcal{F}\{\hat{R}_{auto}[n]\}] + \sum_{k=0}^{\frac{N}{L}} \mathrm{var}[\mathcal{F}\{\hat{R}_{kL}[n]\}]. \tag{D.3}$$

The variance of spectral estimate $\mathcal{F}\{\hat{R}_{auto}[n]\}$ has been shown [212] to be

$$\mathrm{var}[\mathcal{F}\{\hat{R}_{auto}[n]\}] = (S_L(e^{j\Omega}))^2, \tag{D.4}$$

where $S_L(e^{j\Omega})$ is a "smeared" version of the true power spectrum $S(e^{j\Omega})$, with frequency resolution approximately that of an L-point FFT.

The next step in the calculation is to estimate $\mathrm{var}[\mathcal{F}\{\hat{R}_{kL}[n]\}]$. Let $y_A[n]$ be the data segment captured by shift register memory bank A (zero for all n outside the range $0 \leq n \leq L-1$), and $y_B[n]$ be the data segment captured by shift register memory bank B

(zero for all n outside the range $M+L \leq n \leq M+2L-1$), and let $Y_A(e^{j\Omega})$ and $Y_B(e^{j\Omega})$ be their Fourier transforms, respectively. Then, applying standard Fourier transform theorems (and taking into account the even symmetry of $\hat{R}_{kL}[n]$), one can easily show that

$$\begin{aligned} \mathcal{F}\{\hat{R}_{kL}[n]\} &= \tfrac{1}{L}(Y_A^*(e^{j\Omega})Y_B(e^{j\Omega}) + Y_A(e^{j\Omega})Y_B^*(e^{j\Omega})) \\ &= \tfrac{2}{L}\Re e\{Y_A^*(e^{j\Omega})Y_B(e^{j\Omega})\}. \end{aligned} \tag{D.5}$$

For any random variable x, $\mathrm{var}[x] = E\{x^2\} - (E\{x\})^2$, so

$$\begin{aligned} &\mathrm{var}[\mathcal{F}\{\hat{R}_{kL}[n]\}] = \tfrac{2}{L^2}(\Re e\{E\{(Y_A^*(e^{j\Omega})Y_B(e^{j\Omega}))^2\}\} \\ &+E\{|Y_A(e^{j\Omega})|^2|Y_B(e^{j\Omega})|^2)\} - 2(\Re e\{E\{Y_A^*(e^{j\Omega})Y_B(e^{j\Omega})\}\})^2). \end{aligned} \tag{D.6}$$

If N is reasonably large, $y_A[n]$ and $y_B[n]$ are only weakly correlated for most values of $M(=kL)$, and the terms including $E\{(Y_A^*(e^{j\Omega})Y_B(e^{j\Omega}))^2\}$ and $E\{Y_A^*(e^{j\Omega})Y_B(e^{j\Omega})\}$ can be neglected. Thus, Equation D.6 can be simplified,

$$\begin{aligned} \mathrm{var}[\mathcal{F}\{\hat{R}_{kL}[n]\}] &\approx \tfrac{2}{L^2}E\{|Y_A(e^{j\Omega})|^2|Y_B(e^{j\Omega})|^2)\} \\ &\approx 2E\{\tfrac{|Y_A(e^{j\Omega})|^2}{L}\}E\{\tfrac{|Y_B(e^{j\Omega})|^2}{L}\}, \end{aligned} \tag{D.7}$$

where the last approximation assumes weak correlation between $Y_A(e^{j\Omega})$ and $Y_B(e^{j\Omega})$. However, $|Y_A(e^{j\Omega})|^2/L$ and $|Y_B(e^{j\Omega})|^2/L$ are both examples of an L-point periodogram, whose expected value is a smeared version of the true power spectrum, with frequency resolution that of an L-point rectangular window [1]. Thus, $E\{|Y_A(e^{j\Omega})|^2/L\} = E\{|Y_B(e^{j\Omega})|^2/L\} \approx S_L(e^{j\Omega})$, and Equation D.7 can be further approximated,

$$\mathrm{var}[\mathcal{F}\{\hat{R}_{kL}[n]\}] \approx 2(S_L(e^{j\Omega}))^2. \tag{D.8}$$

Substituting Equations D.4 and D.8 into Equation D.3 then gives

$$\mathrm{var}[\hat{S}(e^{j\Omega})] \approx \left(\frac{2N}{L} + 3\right)(S_L(e^{j\Omega}))^2. \tag{D.9}$$

Equation D.9 was derived under the assumption that only one segmented cross-correlation was calculated for each estimate $\hat{R}_{kL}[n]$ in Equation D.1. In practice, to reduce the variance, many segmented cross-correlations (using data from successive measurements) need to be averaged to estimate each $\hat{R}_{kL}[n]$. If K is the number of averages taken for each $\hat{R}_{kL}[n]$, then the variance of the spectral estimate is reduced by $1/K$:

$$\begin{aligned} \mathrm{var}[\hat{S}(e^{j\Omega})] &\approx \tfrac{1}{K}\left(\tfrac{2N}{L} + 3\right)(S_L(e^{j\Omega}))^2 \\ &\approx \tfrac{2N}{KL}(S_L(e^{j\Omega}))^2 \end{aligned} \tag{D.10}$$

since $N \gg L$.

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