THE DETERMINATION OF SEMICONDUCTOR BAND GAP STRUCTURE AND SURFACE STATES USING TUNNELING SPECTROSCOPY

by

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Submitted to the Department of Electrical Engineering
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ABSTRACT

The mechanisms of metal-insulator-semiconductor (MIS) tunneling were explored in order to develop a spectroscopic technique. The theory of MIS tunneling was developed through an extension and modification of the theory of metal-insulator-metal (MIM) tunneling.

Special preparation procedures were formulated so that the thin insulator aluminum-silicon dioxide-silicon devices could be fabricated. A low temperature, nitric acid treatment was developed for the growth of a 100A silicon dioxide layer with dielectric breakdown strength exceeding 5×10^6 V/cm. Test apparatus was designed to permit automatic low current, phase and frequency sensitive measurements. All measurements were made on the (111) face of non-degenerate silicon at room temperature. Experiment and theory were in good agreement.

A novel effect was discovered in p-type devices, whereby the conduction mechanism was tunneling in the enhancement mode, and Schottky emission in the depletion mode. The device current was found to be relatively temperature insensitive in the enhancement mode, but exhibited a positive temperature dependence in the depletion mode.

Phase measurements of the tunnel current led to a new interpretation of the AC tunnel mechanism. The tunnel transit time was very small, so the surface state recombination-generation time became the factor limiting tunnel charge transfer. At frequencies, however, charge transfer was incomplete and the tunnel current decreased with frequency.

Tunneling spectroscopy was demonstrated to be very valuable in obtaining significant data on silicon surfaces, such as the type of material (n- or p- type), surface potential, surface charge (10^{10} - $10^{12}/cm^2$), and surface state distribution ($10^{11}/cm^2$). These data were shown to be in agreement with the literature. A continuous rather than discrete surface state distribution was observed.

Thesis Supervisor: Harry C. Gatos

Title: Professor of Electrical Engineering

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I. INTRODUCTION

A. Semiconductor Surfaces

In the last twenty years, semiconductor surfaces have been studied in great detail. From the date of development of the first point contact transistor, it was apparent that reliable, reproducible, and stable devices could not be fabricated without an understanding of the semiconductor surface.

Shockley and Pearson[1] performed a classical experiment which gave the first understanding of the electrical properties of semiconductor surfaces, i.e. surface states. From a relatively simple field effect capacitor, data were found which gave insight into the density and dynamics of surface states. The early work concentrated on germanium in light of the development of the junction transistor[2]; however, the advent of the planar technology[3] altered the slant of surface research towards silicon. As a result in the last ten years hundreds of articles have appeared on silicon semiconductor surfaces. Many of the articles are listed in bibliographies prepared by Schlaegel[4,5].

In the study of semiconductor surfaces, researchers distinguish between real and clean surfaces. The real surface is prepared by conventional techniques, i.e. mechanical polish and chemical etch, to remove damaged layers and provide a relatively flat surface. This surface is covered by molecules absorbed from the ambient (innate oxide, for example). Clearly, real surfaces are easily prepared, and are those usually encountered in practical application. Clean surfaces are

free of adsorbed matter to better than a few per cent of a monolayer, and may be prepared under high vacuum by cleavage or by high temperature treatment. There is interest in the clean surface because it most closely represents the actual semiconductor surface. However, in practical application, processing of the semiconductor immediately contaminates the surface, meaning only limited measurements on a clean surface can be made.

Extensive work on surface states has been done along both experimental and theoretical lines. Tamm[6] and Shockley[7] theoretically developed the idea of localized states existing in the forbidden gap due to dangling bonds. Much experimental work has been done varying physical parameters to fit experiment to theory, and this work led to considerable understanding of the semiconductor surface. At this time however, experiment and theory do not wholly agree.

Experimentally, surface states are grouped into "slow" and "fast" states. Fast states are those located at the semiconductor-oxide interface, have very short generation-recombination times (less than 10^{-6} seconds), and have densities on the order of 10^{11} to 10^{12} cm^{-2}. The physical characteristics of these fast states such as energy position, density, and capture cross section are fairly well known. The slow states are associated with the oxide of the surface layer and are perhaps the result of absorbed gas atoms and mobile ions within the oxide. Little is known about the slow states except that a typical density is on the order of 10^{13} cm^{-2}.

Probably the most useful theoretical discussions and experimental techniques are described in volumes by Many, Goldstein and Grover[8], Frankl[9], Gatos[10], and Kingston[11].

B. Techniques for Examining Semiconductor Surfaces

The large number of investigators looking at semiconductor surfaces is indicative of the many ways in which these surfaces are being examined. The study of semiconductor surfaces includes two areas:

1) crystalline and chemical properties of the surface, and

2) electronic surface states (or surface states).

First we will define what is meant by a surface state and then we will discuss how these two items interrelate.

A surface state is 1) a location where holes or electrons become trapped, 2) a location where a hole and electron may recombine, or 3) simply a charge center. As the name would imply, these states lie near the semiconductor-oxide interface, either in the insulator or semiconductor. These states may arise from impurities, dislocations, crystalline defects, absorbed gases, moisture, dangling bonds, and anything else disturbing crystalline perfection.

Two of the most important techniques used for the measurement of electronic surface states are the field effect and capacitance voltage methods. The details of these methods are discussed in Appendix A.

The technique of tunneling spectroscopy is the topic of research for this thesis. The theory of tunneling, and experimental techniques will be developed in the next two chapters.

II. THEORETICAL CONSIDERATIONS

A. Tunneling Theory

Tunneling is the quantum mechanical phenomenon which allows electrons or holes to penetrate an energy barrier. This is a familiar problem, and the solution to Schrödinger's equation in the barrier is:

$$\psi = K \exp[-(2m^*/\hbar^2)^{1/2}(W - E)^{1/2}x] \tag{1}$$

where $X_2 \geq x \geq X_1$, and $X_2 - X_1$ = barrier width,

m^* = effective mass in insulator,

W = constant barrier height,

E = energy of particle (W > E),

and the transmission coefficient, which represents the probability of an electron tunneling through the barrier is:

$$T = \exp[-2(2m^*/\hbar^2)^{1/2}(W - E)^{1/2}(X_2 - X_1)] \tag{2}$$

In the case where W is a function of x, the Wentzel-Kramers-Brillouin approximation yields:

$$\psi = K(2m^*/h^2)^{1/2}[W(x) - E]^{1/2}\exp\{-(2m^*/\hbar^2)^{1/2}\int_{X_1}^{X_2}[W(x) - E]^{1/2}dx\} \tag{3}$$

and the transmission coefficient becomes:

$$T(E) = \exp\{-2(2m^*/\hbar^2)^{1/2}\int_{X_1}^{X_2}[W(x) - E]^{1/2}dx\} \tag{4}$$

To find the density of current tunneling from one side of the barrier, the number of electrons impinging on the barrier per unit time

is multiplied by the transmission coefficient.

$$dJ_{X_1} = ev_x n\, T(E_x)\, f(E)\, dK \tag{5}$$

where v_x = velocity impinging on barrier and

v_x for parabolic bands = $(1/\hbar)(\partial E/\partial k_x)$

n = number of electrons per unit

volume of k space = $2/(2\pi)^3$

f(E) = fermi function giving electron occupancy

And so the current density tunneling from one side of the barrier is:

$$J_{X_1} = \frac{e\hbar}{4\pi^3 m^*} \int f(E)T(E_x)k_x dk_x dk_y dk_z \tag{6}$$

In order to simplify this integral, we note that our real interest is in the k_x direction, not in k_y and k_z. If we write $K = k_x + K_\perp$ with $K_\perp \equiv k_y + k_z$, then $dk_y\, dk_z = 2\pi K_\perp dK_\perp$.

Now since for parabolic bands,

$$k_x\, dk_x = m^*/\hbar^2\, dE_x \quad \text{and} \quad K_\perp dK_\perp = m^*/\hbar^2\, dE_\perp$$

we can rewrite equation (6) as

$$J_{X_1} = \frac{em^*}{2\pi^2\hbar^3} \int f(E)\, T(E_x)\, dE_x dE_\perp \tag{7}$$

Using the Jacobian*, $dE_x dE_\perp = dE\, dE_x$, and equation (7) becomes

$$J_{X_1} = \frac{em^*}{2\pi^2\hbar^3} \int f(E)\, T(E_x)\, dE\, dE_x \tag{8}$$

* See Appendix B.

For the case of two electron or hole sources (metals) separated by a thin insulator, there is tunneling from both sides of the barrier. The net current density is the sum of two terms:

$$J_x = \frac{em^*}{2\pi^2 n^3} \int_0^\infty dE[f(E) - f(E + eV)] \int_0^{E_T} T(E_x)dE_x \qquad (9)$$

The term eV corresponds to the increase of energy due to the external bias voltage V.

Equation (9) serves as the starting point for the derivation of the tunneling current in a thin metal-insulator-metal (MIM) structure[12-22]. The details of the tunneling current differ through the various integrations of the transmission coefficient, $T(E_x)$. The approximations of both Stratton[12] and Simmons[13] have been found to describe tunneling through insulating films for limited voltage ranges. More recent approximations[21,22] have wider ranges of validity. For the purpose of obtaining an analytical expression describing MIM tunneling, Stratton's approach will be developed. It is hoped that the expression derived will give some understanding to the more complicated problem of tunneling in the metal-insulator-semiconductor (MIS) structure. It must be pointed out that in the theoretical formulation of MIM and MIS tunneling unoccupied states must be available for electrons to tunnel into. This means equation (9) must be modified to

$$J_x = \frac{2\pi em^*}{n^3} \int_0^\infty dE\rho_1(E)\rho_2(E + eV)[f(E) - f(E + eV)] \int_0^{E} T(E_x)dE_x \qquad (9a)$$

where $\rho_i(E)$ correspond to the density of states at the energy of the semiconductor and metal respectively.

Stratton measures energy from the top of the valence band and defines $\phi(x,V)$ to be the barrier energy profile measured from the Fermi level, E_f (Figure 1). Thus the total energy barrier, $W(x)$ is $\phi(x,V) + E_f$. Now integration by parts of equation (9) yields:

$$J_x = \frac{4\pi e m^*}{h^3} kT \int_0^\infty T(E_x) \ln\left[\frac{1 + \exp(E_f - E_x)/kT}{1 + \exp(E_f - E_x - eV)/kT}\right] dE_x \qquad (10)$$

This is a familiar result also found through other derivations as by Duke[23,24], Hartman[18], and Barker and Gruodis[22]. Stratton assumes that only electrons near the Fermi level dominate the tunneling current, and he thus expands the transmission coefficient in powers of E_x' where $E_x' = E_f - E_x$. The details are presented in Stratton's [12] and equation (10) becomes

$$J_x = J_o \frac{\pi a_1 kT}{\sin(\pi a_1 kT)} \exp(a_2 V - a_3 V^2)[1 - \exp(-a_1 V)] \qquad (11)$$

where

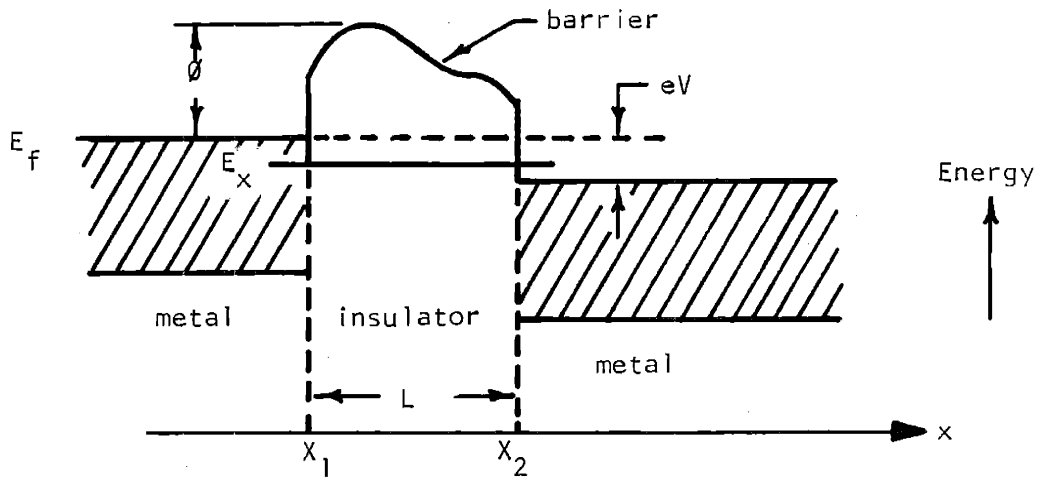
$$J_o = \frac{4\pi e m^*}{a_1^2 h^3} \exp(-a_o)$$

If the barrier is symmetric about $x = 1/2$*, then $a_2 = a_1/2$, and equation (11) becomes

$$J_x = J_o \frac{2\pi a_1 kT}{\sin(\pi a_1 kT)} \exp(-a_3 V^2) \sinh(a_1 V/2) \qquad (12)$$

This theoretical equation has been shown to agree with experimental data obtained from MIM structures[12,25]. Figure 2 shows the very good fit of data obtained on an Al-Al_2O_3-Al sandwich with a 48 Å thick insulator.

* As is generally the case for an MIM structure.



Tunneling Barrier in the MIM Structure

Figure 1

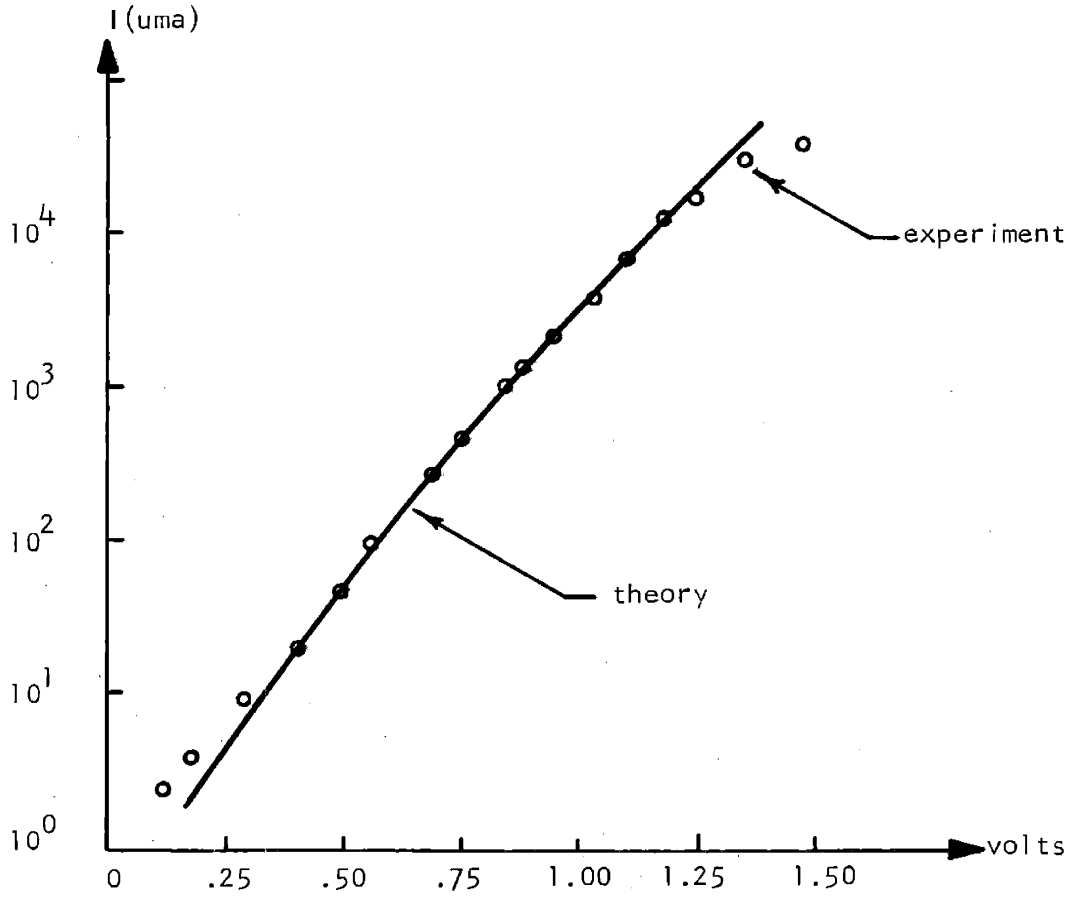


Figure 2

Room Temperature Tunneling Characteristics for the Al-Al_2O_3-Al Structure

B. Tunneling Spectroscopy

Having discussed the theory of MIM tunneling, we wish to make the transition to MIS tunneling. We develop MIS theory by discussing the physical differences between MIM and MIS tunneling, and modifying the MIM equations to fit the MIS system.

The energy band picture of an MIS structure is shown in Figure 3, with an n-type silicon semiconductor. A chemically etched silicon surface usually has more donor states than the bulk[26]. Therefore, the surface is more n-type than the bulk (Figure 3). It is assumed that the energy gap of the insulator is large compared to that of silicon.

The MIS structure differs from the MIM structure in that:

1) The semiconductor has a band gap whereas the metal does not.

2) The metal is an "infinite" source and sink for electrons, while the semiconductor has only a finite number of states.

3) The electrical differences between the metal and semiconductor mean that the tunneling barrier will be nonsymmetric as compared with the Al-Al_2O_3-Al structure. It is these differences which must be discussed in order to modify equation (12) to predict MIS tunneling effects.

Electrons in the metal or the semiconductor cannot tunnel through the insulator unless they lie opposite to unoccupied states in the other electrode. Therefore, no current can flow in the MIS structure of Figure 4 until the metal is biased $+V_2$ or $-V_1$ volts (assuming all the voltage drop is across the insulator, and that the surface states present within the semiconductor's forbidden gap are negligible for now). When $+V_2$ volts are applied to the metal, electrons in the

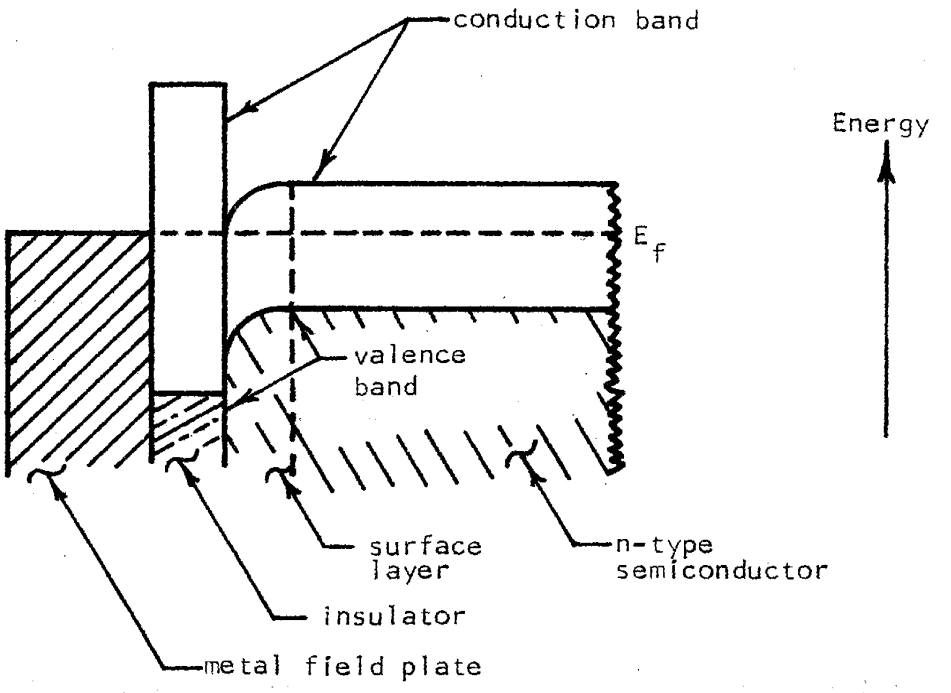


Figure 3

Energy Band Diagram for the MIS Structure

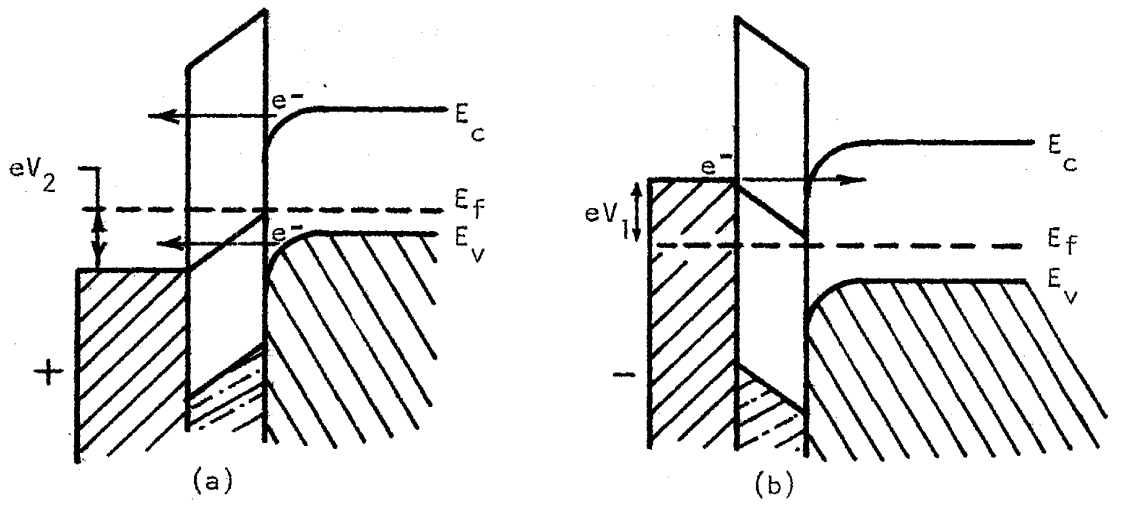


Figure 4

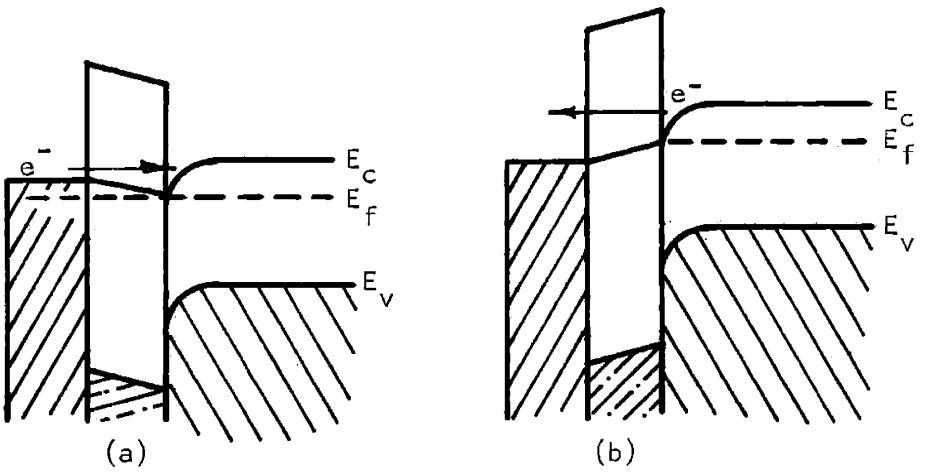
Electron Tunneling in a P-type Semiconductor MIS Structure
With Positive (a) and Negative (b) Bias on the Metal Plate

valence band of the semiconductor tunnel into unoccupied states of the metal. At $-V_1$ volts, electrons at the Fermi level of the metal tunnel into the conduction band of the semiconductor. For positive bias on the metal, electrons from the conduction band can also tunnel into the metal. Since the semiconductor is p-type, the concentration of conduction band electrons is low (so this effect is small).

When the semiconductor is n-type (Figure 5), tunneling is dominated by metal to semiconductor conduction band transitions. In this case there is only a small gap in tunneling V-I characteristics. The n-type semiconductor would be expected to behave more like a metal than would p-type due to conduction band conductivity.

This tunneling gap, $V_o = V_2 - V_1$, must be overcome for tunneling to occur. If we were to replace the applied voltage V, by $V - V_o$, in Stratton's calculation, equation (12) would be corrected to account for this gap. Note that in the p-type semiconductor V_o is greater than that in the n-type, and in the metal, of course $V_o = 0$.

As discussed in Harrison's paper[27], the matrix element for tunneling vanished unless the transverse wave number, k_t, is the same for initial and final states. The Fermi surface of the metal is much larger than the Fermi surface of the semiconductor[28], so the "shadow" cast by the semiconductor Fermi surface is always covered by the large shadow of the metal[29]. Thus, the electrons tunneling from the semiconductor into the metal can easily find an available state, but electrons tunneling from the metal are limited to states within the small area of the shadow cast by the semiconductor.



Electron Tunneling in an N-type Semiconductor MIS Structure with Negative (a) and Positve (b) Bias on the Metal Plate

Figure 5

This restricting of the region of allowed momentum has the effect of reducing the transmission coefficient, $T(E_x)$. Since we have approximated $T(E_x)$ by a series expansion for the MIM structure, the same approximation should hold for MIS structures with the magnitude of the coefficients reduced.

As seen through equations (4) and (9), the tunneling current between two insulated electrodes depends on the shape and magnitude of the energy barrier of the insulator. If the work function of the two electrodes is unequal, the barrier is asymmetric, causing the MIM tunneling current to differ for forward and reverse bias. Simmons[30] investigated this barrier asymmetry for different metals, and found that no changes in the tunneling current were evident until the applied voltage exceeded the lower of the two barrier heights. In the structures which Simmons examined, observed changes were on the order of only several per cent for biases up to ±3 volts. Thus, even for dissimilar electrode metals, equation (12) is applicable.

The above argument holds true for MIS tunneling with the n-type semiconductor, since the tunneling transitions are with the conduction band for both directions of current (Figure 5). For the p-type semiconductor, however, tunneling transitions occur to the valence band for positive bias (on the metal) and to the conduction band for negative bias (Figure 4). Thus, the tunneling barrier is different for different bias polarity, and a current asymmetry should occur.

This qualitative discussion suggests that the theory explaining MIM tunneling is readily adaptable to MIS tunneling. The energy gap

shifts the tunneling characteristics to higher voltages, and the transition probabilities reduce the magnitude of current. Therefore, when surface effects are not considered, Stratton's results can be modified to

$$J_x = J_o \frac{2\pi a_1' kt}{\sin(\pi a_1' kt)} \exp[- a_3'(V - V_o)^2] \sinh[a_1'(V - V_o)/2] \qquad (13)$$

where a_1' and a_3' are smaller than a_1 and a_3 respectively.

The constants a_1' and a_3' are functions of the physical parameters of the insulator (dielectric constant, thickness, and effective mass)[13,15]. Of interest is the fact that a_1' varies inversely with insulator thickness and a_3' varies with the inverse square of insulator thickness.

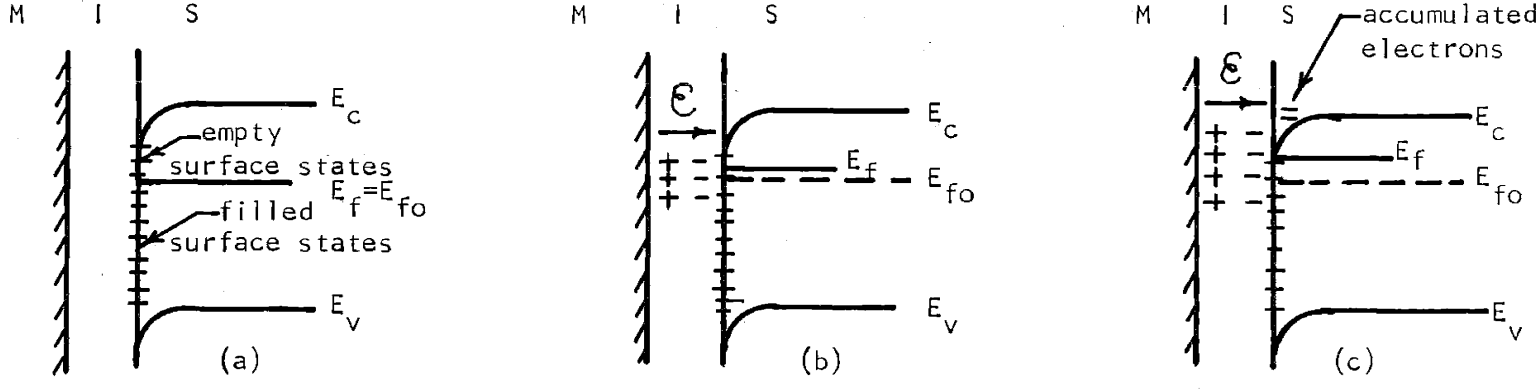
The assumption that a transition can be made from MIM to MIS tunneling via equations (12) and (13) is of course dependent on the fact that we indeed know what the tunneling barrier is. One usually considers the large band gap insulator to be intrinsic, and accordingly the net tunneling barrier could be a function of both the conduction and valence bands of the insulator. This model represents two band tunneling, and the above derivation which was carried out for single band tunneling would not be applicable. In fact we could not even define an effective mass (E vs K relation) in the two band model.

In the case at hand, i.e. a very thin insulator, surface charge on the semiconductor induces charge and thus band bending in the insulator. Since the bulk carrier concentration in the insulator is very low (energy gap for $SiO_2 \simeq 6$ eV), the actual band bending

must be quite large to accomodate the induced charge. If we had a semi-infinite insulator, deep in the bulk the insulator would be intrinsic. But at the surface, near the chage source, the Fermi level would be closer to the conduction band (for SiO_2 on Si on the order of 2eV[31]). In the thin insulator, however, we see only this "extrinsic" insulator, and the tunnel barrier corresponds to the conduction band in the insulator indicating that the one band model is applicable. Furthermore, since on a band model we look only at a small segment of this bent band, the segment can be accurately approximated by a straight line. This model permits us to use the single band theory with a trapezoidal barrier.

Surface Considerations in MIS Tunneling. In this research we plan to study surface states at the semiconductor-insulator interface using the tunneling technique. Tunneling spectroscopy has been reported for silicon[32-34] and InSb[35], and is briefly outlined here.

For simplicity, consider the case where the applied voltage exists entirely on the insulator. Using the energy band diagram of Figure 6(a), it is seen that the Fermi level of the metal can be swept through the band gap of the semiconductor by varying the bias on the metal. Analogous to the effect discussed earlier, i.e. tunneling in the p-type semiconductor when the Fermi level of the metal "saw" the conduction band or valence band edge, the tunneling current will increase when the Fermi level of the metal corresponds to a surface state level. In this manner, it is hoped to characterize the density and energy level of surface states in the band gap.



Effect of Positive Bias on Metal Plate of N-type MIS Structure: (a) No Bias (b) Low Bias (c) High Bias, No Penetration of Electric Field into Semiconductor

Figure 6

The simplifying assumption of the voltage drop existing entirely across the insulator, i.e. no band bending due to applied bias, must be investigated to find regions of applicability, and to make suitable modifications when necessary. The tunneling current depends on the electric field in the insulator[13,15,25], and a knowledge of how the field in the MIS insulator varies with applied voltage will permit understanding of the tunnel current.

The electric field lines resulting from the applied voltage pass through the insulator and terminate on charges in the metal and semiconductor. The charge on the metal appears at the surface and does not penetrate into the metal. The charge on the semiconductor is a more complex situation. Charge can build up in surface states and in a depletion or accumulation layer at the surface. The location of these charges determines the field in the insulator, and thus, the V-I relation of the MIS structure. Specific consideration for the charging of surface states in silicon is considered.

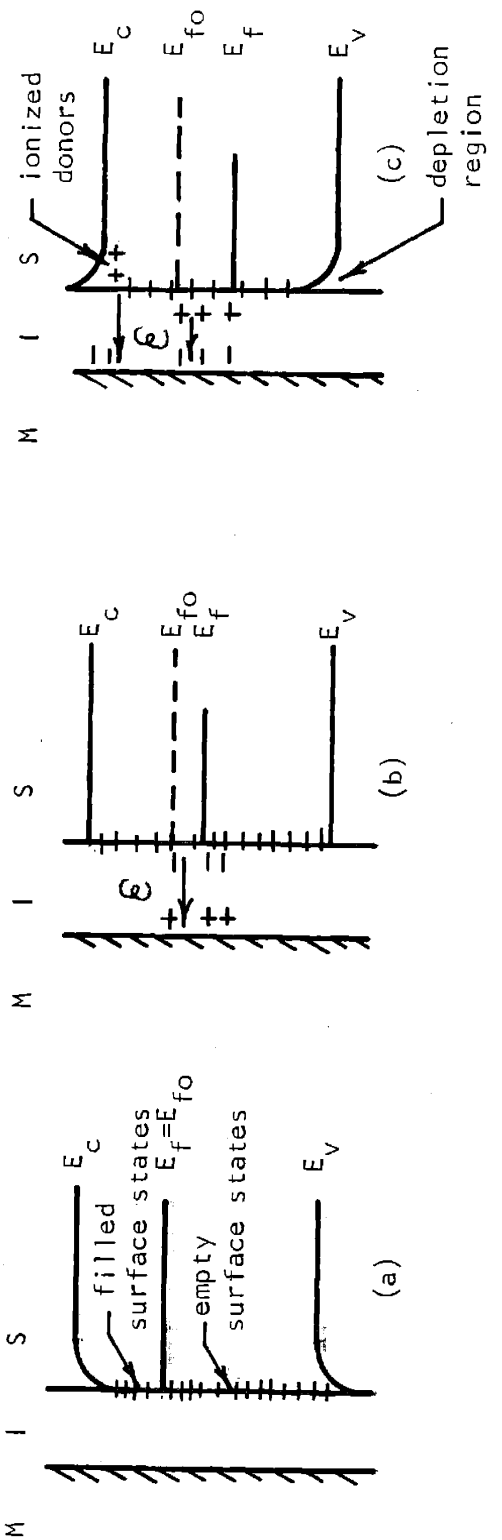
Silicon usually has an excess of donor type surface states. These states are partially filled, according to Fermi statistics, and create an internal electric field. This internal field affects the tunneling characteristics only when the potential barrier is altered by the field.

Many et al.[8] illustrate (Figure 6) the termination of field lines on silicon with surface states. For zero bias, in n-type silicon, the surface states above the Fermi level are empty. If a positive voltage is placed on the metal, electrons are swept to

the semiconductor surface. These excess electrons fill up surface states until equilibrium is reached. With large enough bias, all the surface states become filled so that additional voltage produces an electron accumulation region at the surface. In this situation, the charge in the semiconductor is at the surface and the field in the insulator is proportional to the applied voltage ($E = V/L$). The semiconductor surface appears metallic, and the field does not penetrate the semiconductor.

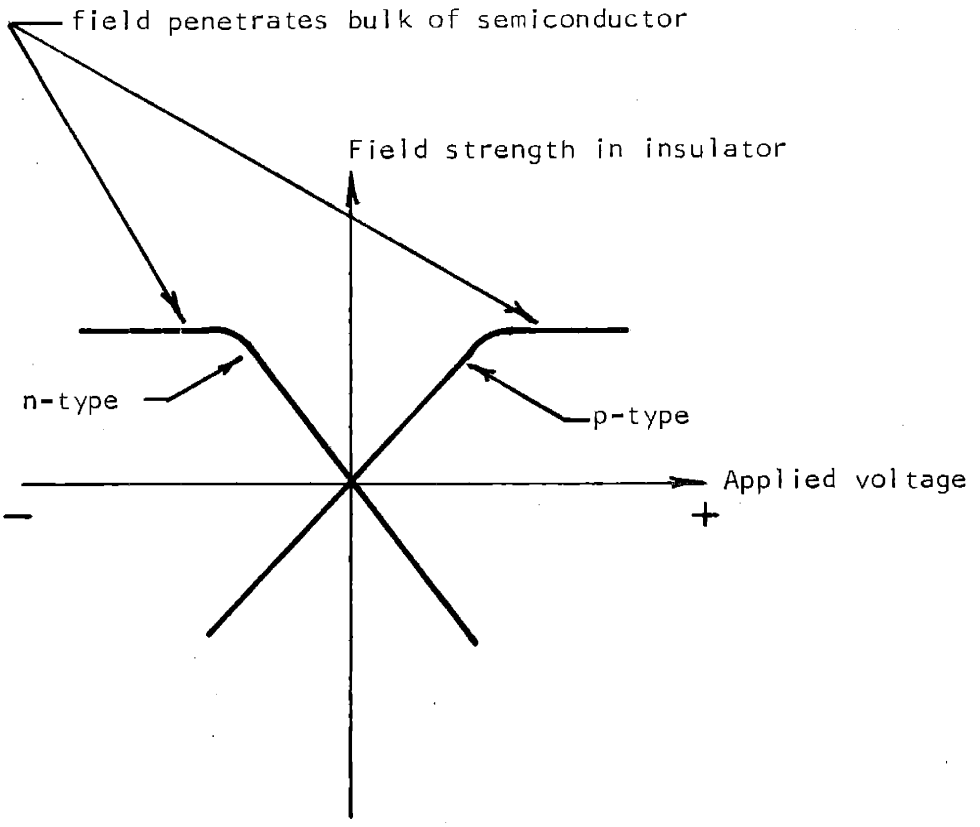
If a negative voltage is applied to the metal, electrons are swept away from the surface and the surface states start to empty. As seen in Figure 7, when the surface states are completely emptied the surface region is made up of immobile positive charges (ionized donors). Field lines terminate on these charges, and the field penetrates the bulk. The same argument holds for the p-type semiconductor, except for a reversal of polarity. This analysis predicts the insulator field to vary with applied voltage as shown in Figure 8. In the regions where the field is proportional to the applied voltage, the MIS tunneling current should increase exponentially as predicted by equation (13). When a depletion layer forms, the insulator field no longer increases proportionally to the applied voltage, and the tunneling current levels off. The predicted V-I characteristics[36] are shown in Figure 9.

The aforementioned has been a description of the technique of tunneling spectroscopy. Although we have specifically alluded to the aluminum-silicon dioxide-silicon system, it should be apparent that the same arguments hold true for the more general metal-



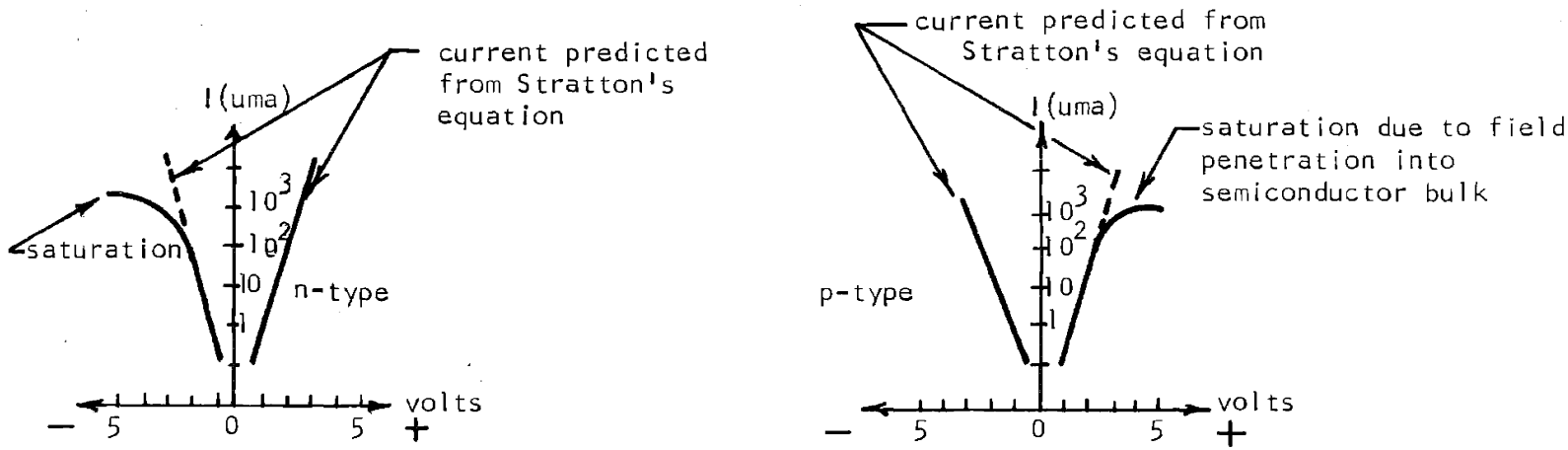
Effect of Negative Bias on Field Plate of N-type MIS Structure: (a) No Bias (b) Low Bias
(c) High Bias Penetration of Field into Semiconductor

Figure 7



Electric Field Strength in Insulator of MIS Structure as a Function of Applied Voltage

Figure 8



I-V Tunneling Characteristics Predicted From MIS Structures With Surface States

Figure 9

insulator-semiconductor structures.

This technique, as described, permits investigation of the conduction and valence band edges, but not of surface states within the bandgap. The following approach is needed to study surface states.

If, when the Fermi level of the metal is slowly "swept" through the gap of the semiconductor, it should see a level of surface states, a tunnel current would flow[34,37] until the states filled or emptied (according to Fermi statistics), then thermal equilibrium would result. Thus, this current would only be transient, and depending on the generation-recombination rate of the surface state, probably be of too short a duration to detect. To overcome this problem, a low level AC signal is superimposed on the DC sweep. In this way, when a surface state level is reached, the AC signal will cause the state to fill and empty in response to the incremental field, and thus a steady state signal is measured. The solution of this problem gives us the added feature of being able to vary frequency to measure surface state dynamics, and also being able to use DC-AC filtering technique to permit measurement of surface states near band edges where the DC signal would dominate. Both the experimental techniques and data obtained will be detailed in the next chapter.

C. Other Conduction Mechanisms in MIS Structure

Having discussed tunneling spectroscopy, the question now arises on the conditions for tunneling to occur and the possibility of other components of current. What we are really asking is how do we know that the current being measured is indeed a tunnel current?

In order to properly answer this question, we must discuss other conduction mechanisms.

Electronic conduction in MIS structures may be classified in six general categories. The pertinent equations are presented in Appendix C, and a brief description of their differences is discussed here.

1. Ionic conduction is due to drift of ionic impurities and defects under the influence of an electric field (for example, silver in ceramic used in capacitors). Absorbed moisture may enhance ionic conduction as shown:

$$-\underset{\underset{O}{|}}{\overset{O}{|}}\text{-O-Si-O-Na} \xrightarrow{HOH} \underset{\underset{O}{|}}{\overset{O}{|}}\text{O-Si-O-H} + Na^{+} + OH^{-}$$

The Na^{+} is small enough to move through the amorphous oxide, but the larger OH^{-} cannot. The physical conduction process may be described as ions jumping from site to site. Evidence of this has been seen in TiO_2 and $BaTiO_3$. These dielectrics become more stable to Na^{+} drift by doping with silver. The silver ions fill in vacancies in the dielectric and the Na^{+} is rendered immobile. The movement of ions on the surface of semiconductors can introduce leakage and device degradation. Until surface passivation was developed, surface leakage was amongst the most severe failure mechanisms in transistors.

Ionic and electronic currents are easily distinguished. The activation energy for ionic conductivity is large (3-4eV) and the ions have a long transit time (low mobility, less than 1 cm^2/V-sec).

Usually DC ionic conductivity decreases with time since ions can not readily be injected or extracted from the insulator. After an initial current flow, positive and negative charges will build up and polarize the insulator. When the applied field is removed, internal fields cause some of the ions to flow back to their equilibrium position with their characteristically long time constants, and hysteresis results.

2. Tunneling and internal field emission are conduction processes via barrier penetration. The four subgrouping are: a) Zener - electrons tunneling from valence band of semiconductor to conduction band of metal; b) Field ionization - electrons from impurity levels of semiconductor to conduction band of metal; c) Field emission - from Fermi level (cathode) to vacuum; d) Field emission - from within valence band to anode. Tunnel currents are characterized by their relative temperature insensitivity and an exponential dependence on insulator width.

3. Impurity conduction - electrons hop from one donor site to another (same for holes and acceptors), but not into conduction band. (This would be ohmic conduction). For very low concentrations of impurity, both donor and acceptor sites are necessary, as acceptors remove electrons from some donors. For intermediate and high concentrations of impurity, acceptors are not necessary. In intermediate concentrations, a hopping process occurs wherein phonon interaction is essential. For very high concentrations, interaction is great, and a relatively high impurity band conductivity results.

Impurity conduction in clean insulators such as SiO_2, SiO, and Si_3N_4 is at a minimum due to very few impurities and the high activation energy between nonoverlapping wave functions. Even at fields of 5×10^6 V/cm, impurity conduction in insulators is estimated at less than 10^{-16} mho/cm[38].

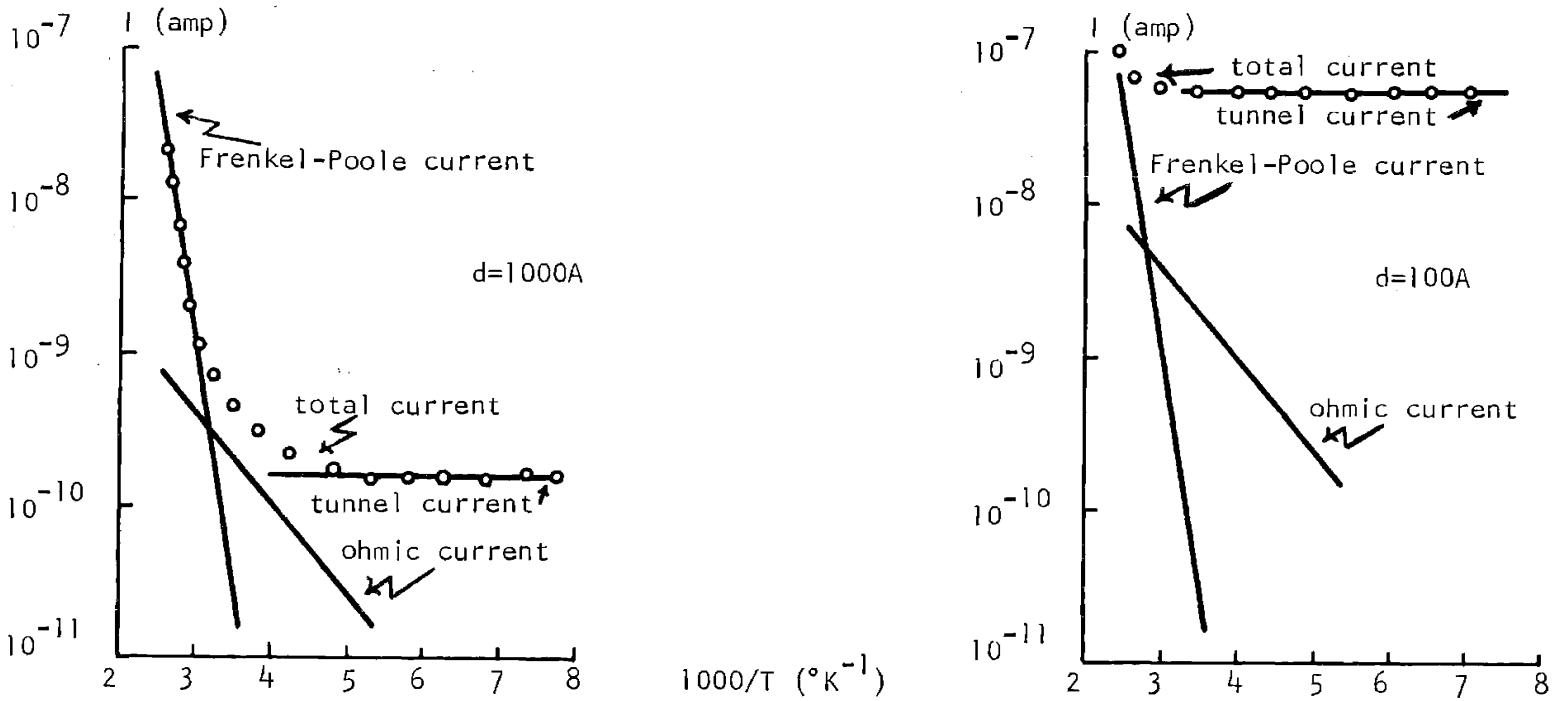
4. Ohmic conduction occurs when electrons are excited into the conduction band and drift under the influence of the applied field.

The ohmic component, which contributes mainly at higher temperatures due to its relatively large activation energy, is easily identified by a linear current voltage plot. This component reaches 10^{-5} amp/cm^2 at 5×10^6 V/cm only at temperatures exceeding 425°K[39]. Thus this component is usually negligible.

Changes in insulator thickness cause linear changes in the ohmic component but cause exponential changes in the tunneling component. The details of these mechanisms are seen in Figure 10.

5. Space charge limited flow is due to build up of a negative space charge at the cathode; further electron flow is limited by repulsive forces. At equilibrium current is proportional to voltage to the second power. Space charge limited flow becomes important only at current densities exceeding 15-20 amp/cm^2[40].

Although tunneling has been reported through films up to 1000A[39], films must be thinner than 200A to observe current densities greater than 10^{-5} amp/cm^2. Space charge limited currents are not observed in MIS structures with insulator thickness less than 2000A[41], most likely due to very low current densities, i.e. no interactions.



Current-Temperature Characteristics of an Au-Si_3N_4-Si Structure at Applied Field of 5×10^6 V/cm. The Tunnel Component Predominates at Low Temperature: the High Temperature Range can be Extended by using a Thinner Insulator. (Reference 39)

Figure 10

6. Schottky emission and Poole-Frenkel effect - both of these processes occur through electron excitation over a barrier. a) Schottky emission occurs when effective barrier height is reduced by intense applied field across the thin insulator. The electrons from the metal or semiconductor are excited to the conduction band of the insulator. b) Poole-Frenkel effect occurs when electrons trapped in insulator are excited to conduction band of insulator.

The Poole-Frenkel component is of the same order of magnitude as the tunneling current at normal intermediate temperatures. At the high temperature range, Poole-Frenkel currents dominate (Figure 10), while at low temperatures the Poole-Frenkel component disappears, so the tunnel current dominates. However, the two components are readily separated because a) the tunnel component is essentially temperature independent, while Pool-Frenkel processes are strongly temperature dependent, and b) tunnel current $\propto V^2 \exp(-a/V)$, while Poole-Frenkel current $\propto V\exp(V^{1/2})$.

The intent of the above discussion is to give some experimental understanding on the conduction mechanisms in MIS structures. It is not a rigorous argument, but one which suggests the possible mechanisms. If experiments are done near absolute zero temperature, one can be reasonably sure that the only possible currents would be either tunnel or space charge limited currents. If one uses a superconductor as the electrode, and if one observes the superconducting gap, then the transport mechanisms must be tunneling. Aside from these extremes, however, we must rely on experimental evidence and experience to analyze the actual conduction mechanism.

III. EXPERIMENTAL PROCEDURE

A. Sample Preparation

The tunneling devices used in these experiments were all of the aluminum-silicon dioxide-silicon structures. This decision was made because of the tremendous interest in, and data available, on silicon, the ease in working with SiO_2 and Al using the planar technology, and the extreme practical value of this almost universal MOS capacitor.

The criteria used in trying to fabricate a tunneling device were:

1) to grow a thin tunneling barrier, less than 200A thick;

2) since the bandgap of Si is 1.1 eV, the thin oxide must be able to withstand fields on the order of 5×10^6 V/cm;

3) capacitance must be minimized so that this 90° out of phase signal does not swamp out the inphase tunnel component (small device area).

Oxidation. At usual oxidation temperatures, 1050-1200°C, the oxide grows so quickly that by the time the wafer is placed inside the tube and taken out, oxides on the order of 300-700A have grown. An attempt was made at growing low temperature oxides (300-800°C) but these oxides had lower breakdown strengths than required (5×10^5 V/cm). This was attributed to a very porous oxide, resulting from low temperature growths. It is known that silicon has an innate oxide 20-60A thick, when exposed to the atmosphere at room temperatures. This oxide was also unsatisfactory (analogous to the low temperature oxide). Other techniques such as anodic plating or

evaporation of SiO_2 proved unsuccessful due to high pinhole density and/or high impurity density causing low breakdown strength.

A technique we discovered was that of passivating the wafer with hot concentrated nitric acid, a good oxidizing agent. The probable reaction is:

$$2HNO_3 \longrightarrow H_2O + 2NO_2$$

and

$$Si + 2NO_2 \longrightarrow SiO_2 + 2NO\uparrow$$

with the net reaction,

$$Si + 2HNO_3 \longrightarrow SiO_2 + H_2O + 2NO\uparrow$$

Because this is a relatively low temperature reaction, the oxide probably grows by diffusion of oxygen through pores in the oxide. And, as observed, the rate of growth of oxide is slow (100A in 3 min.). Yet upon testing the oxide, breakdown fields of 5×10^6 V/cm were measured, which results from hydration tightening the oxide and closing pores,

$$SiO_2 + XH_2O \longrightarrow SiO_2 \cdot (H_2O)_X$$

Electrical Contact. Since the excess handling and elevated temperatures required for wafer dicing and bonding were considered a principle source of device failure, we decided to make electrical contact via a joystick probe.

We encountered difficulty when contact was made to the aluminum. The thin oxide under the aluminum is extremely fragile, and was penetrated by the probe, thus destroying the device. This problem was overcome by fabricating an "expanded" contact. A thick oxide (5000A)

was thermally grown on the substrate, and a thin oxide grown in holes etched through the thick oxide. Evaporated aluminum coats both oxides, and probe contact is made to the stronger thick oxide. Furthermore, because of the thick oxide, extra contributions to device capacitance are minimal.

Having now overcome the basic problem in device fabrication, we go into detail on the processing steps and final device structure.

Processing of Silicon Wafers for Tunnel Test Device

1. Material used:

   a. N-type silicon, resistivity 10, 1.0, 0.5Ω-cm (donor density 5×10^{14}, 6×10^{15}, and $2 \times 10^{16}/cm^3$ respectively) ±20%; dislocation density less than $10^3/cm^2$ as determined by etch pit count; orientation (111) ±0.5°; phosphorous doped. The pulled crystals were grown by Texas Instruments' Lopex (low oxygen) process, with diameter 7/8 - 1 1/8". The crystal had a flat cut on it perpendicular to the [110] direction, and is then sliced into wafers ranging from 7.5 to 9.0 mils thick. All wafers are mechanically polished and chemically etched by the manufacturer.

   b. P-type silicon, resistivity 10, 1.0, 0.5Ω-cm (acceptor density 10^{15}, 2×10^{16}, and $4 \times 10^{16}/cm^3$ respectively) ±20%; dislocation density less than $10^3/cm^2$ as determined by etch pit count; orientation (111) ±0.5°; boron doped. The pulled crystals were grown by Texas Instruments' Lopex process, with diameter 7/8 - 1 1/8". The crystal had a flat cut on it

perpendicular to the [110] direction, and is then sliced into wafers ranging from 7.5 to 9.0 mils thick. All wafers were mechanically polished and chemically etched by the manufacturer.

2. Wafer cleaning:

Note that in the following processes all acids and solvents used are of "Transistar" purity and deionized (DI) water with resistivity exceeding 10^{18} Ω-cm.

a. Immerse wafer in concentrated sulfuric acid (H_2SO_4) at 185°C for 15 minutes, then allow to cool in the acid.

b. Rinse in DI water for 5 minutes.

c. Heat wafers in concentrated nitric acid (HNO_3) at 120°C for 15 minutes.

d. Rinse in DI water for 5 minutes, then dry wafers by spinning.

e. Immerse in concentrated HF at room temperature for 1 minute.

f. Rinse in DI water for 15 minutes, then spin dry.

3. First oxidation:

a. Set oxidation furnace to 1200°C, and purge tube with a steam of dry nitrogen.

b. Place wafers on quartz carrier and insert into tube.

c. Set flow of dry oxygen at 1000 cm^3/min for 15 minutes.

d. Switch to a wet oxygen (steam at 95°C) flow of 500 cm^3/min for 20 minutes.

e. Switch back to dry oxygen flow of 1000 cm^3/min for 15 minutes.

The wafers are now removed from the oxidation tube, and the wafers appear to be green-blue-green, signifying an oxide thickness of 5000A.

4. Oxide photo resist:

   a. Load photo resist (Shipley positive resist #AZ-111 or AZ-1350) into syringe, and apply to wafer through 1 micron Millipore filter.

   b. Spin wafer for 30 seconds to 3000 rpm to get thin (1 micron) uniform coating of photo resist on wafer.

   c. Prebake wafers at 85°C for 10 minutes in an uncovered dish.

   d. Expose wafer to mask #1 (Figure 11) under ultraviolet light for 5 seconds. Resist will stay soft where exposed to light.

   e. Develop wafer for 30 seconds (use 1 part Shipley AZ-303 developer to 4 parts DI water and spray on wafer.

   f. Rinse in DI water for 5 minutes, spin dry, bake for 30 minutes at 85°C and let cool.

5. Oxide etch:

   a. Let wafers cool, then etch oxide in solution of 10 parts NH_3F1 (40% solution) to 1 part concentrated HF. This is a buffered HF solution and the observed etch rate is 800A/min.

   b. Rinse in DI water for 15 minutes, then clean off remaining photo resist in H_2SO_4 at 185°C for 15 minutes.

   c. Allow wafers to cool, rinse in DI water for 5 minutes, then spin dry.

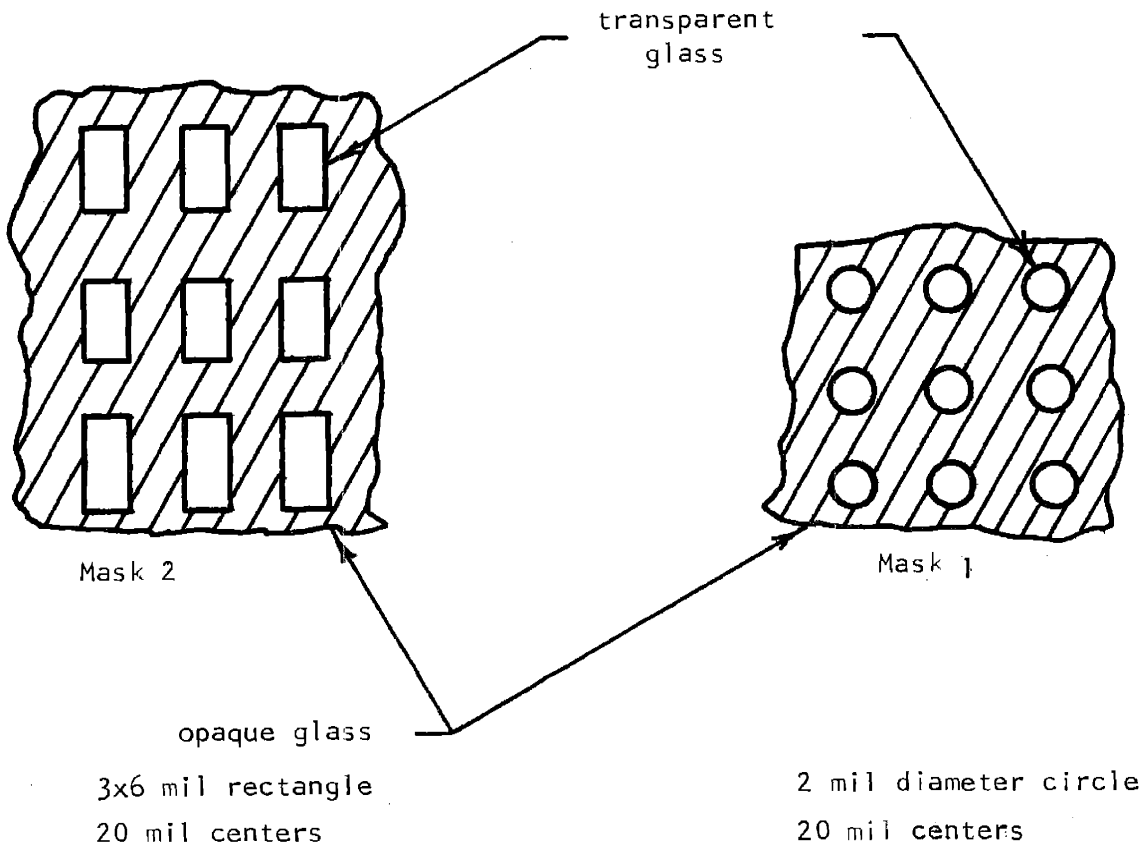


Photo-Lithographic Masks for Device Patterns

Figure 11 Figure 12

At this stage the wafer has the image of mask #1, i.e. 2 mil holes etched through the 5000A oxide down to bare silicon.

6. Second oxidation:

   a. Immerse wafer into concentrated HNO_3 at 120°C for 5 minutes.

   b. Rinse in DI water for 5 minutes, and spin.

At this step a thin oxide (later estimated to be approximately 100A thick) is grown on the silicon in the 2 mil holes.

7. Metallization:

   a. Load wafers into vacuum evaporator

   b. Load pure (99.999%) aluminum into evaporator and deposit using electron beam bombardment. Deposition rate is 10,000A/min at 5×10^{-6} torr, and final aluminum thickness is 5000A.

   c. Dry wafers for 15 minutes at 85°C.

Aluminum metal now covers the entire wafer.

8. Metallization photo resist:

   a. Mix Kodak negative photo resist 1:1 with thinner (Kodak KTFR resist and thinner).

   b. With syringe apply resist through 1 micron filter.

   c. Spin wafer at 6000 rpm for 14 seconds, approximately 8000A layer of photoresist.

   d. Air dry for 15 minutes (do not spin or blow).

   e. Prebake for 3 minutes at 85°C in an uncovered dish.

f. Expose water to mask #2 (Figure 12) under ultraviolet light for 6 seconds. Resist hardens where exposed to light.

g. Develop with Kodak KTFR developer for 1 minute

h. Rinse in DI water for 15 minutes and spin dry.

Following this step the test patterns are fabricated and appear in Figure 13.

10. Removal of photo resist: We cannot use H_2SO_4 to remove the remaining photo resist because the sulfuric acid will also etch the aluminum. Therefore painstaking steps must be followed to clean the relatively insoluble photo resist.

a. Immerse wafers in J-100 (a proprietary organic solvent) at 110°C for 10 minutes.

b. Wash in hot xylene (or trichlorethylene-TCE) for 5 minutes.

c. Rinse in cold xylene (or TCE) for 5 minutes.

d. Rinse in acetone for 5 minutes.

e. Rinse in methanol for 5 minutes.

f. Rinse in DI water and spin dry.

Processing is now completed, and a cross section of the devices shown in Figure 13, appears in Figure 14.

B. Measurement Techniques

In designing test apparatus for an experiment, one must carefully consider the nature of the desired data. In this experiment the requirements are:

1. DC I-V characteristics, voltage range ±1v, current range to 10^{-10} amps.

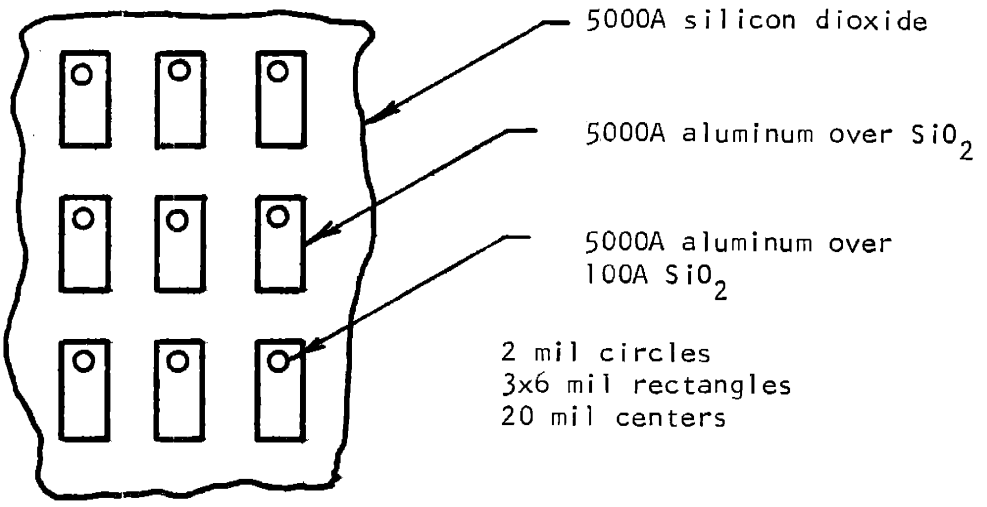


Figure 13

Top View of Processed Wafers

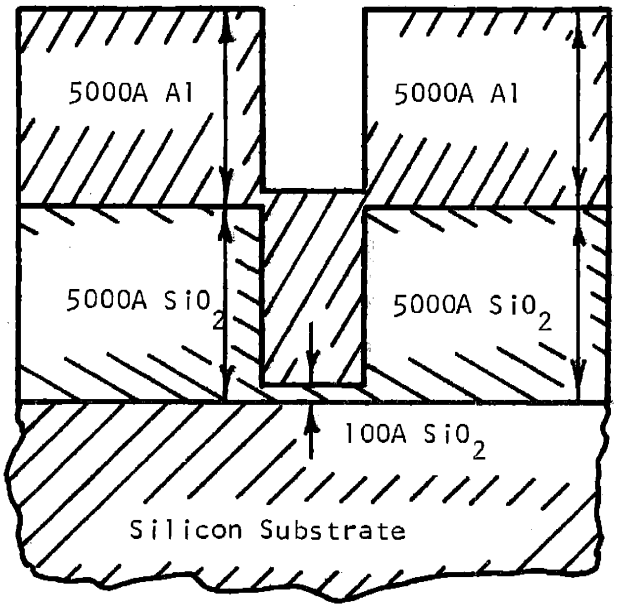


Figure 14

Cross Section View of Processed Wafers

(Not to Scale)

2. DC conductance-voltage measurements.

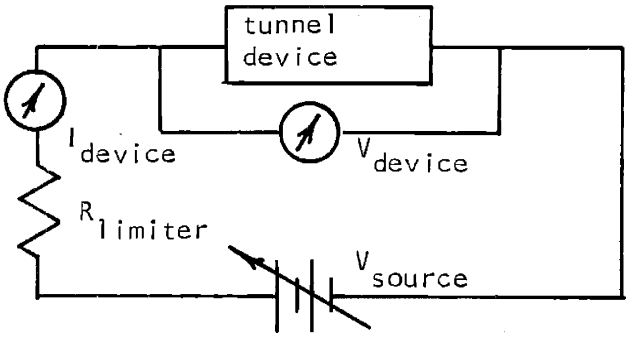
3. AC incremental G-V measurements dealing with currents down to 10^{-13} amps.

4. C-V measurements.

In cases 1-3, current levels are sufficiently small, such that noise problems are an important consideration. It must be remembered that the tunnel samples are basically high value MOS capacitors so that there is the further complication of very high impedance at low frequencies and large, 90° out of phase displacement currents superimposed on the AC tunnel component.

For D. C. measurements, the simplest apparatus is shown in Figure 15. This circuit is not usable here because in most cases the sample impedance is higher than the voltmeter impedance, and the current measured is that through the voltmeter. The next step would be to try a simple Wheatstone bridge; however, the problem of a high sample impedance occurs here too. The way to overcome this problem is to design a bridge with the impedances of the measuring apparatus incorporated. Figure 16 shows a bridge which, when nulled without the tunnel sample, includes all circuit loading. R_I and R_V represent the impedance of the current measuring and voltage measuring devices respectively (oscilloscope and X-Y recorder). If we write the network equations for this bridge we readily find that

$$V_{R_I} = \frac{R_2 R_3 R_I}{R_1 R_2 + R_1 R_I + R_2 R_I - R_2 R_3} I_{sample} \qquad (14a)$$



Simple Measurement Circuit for DC I-V Characteristics

Figure 15

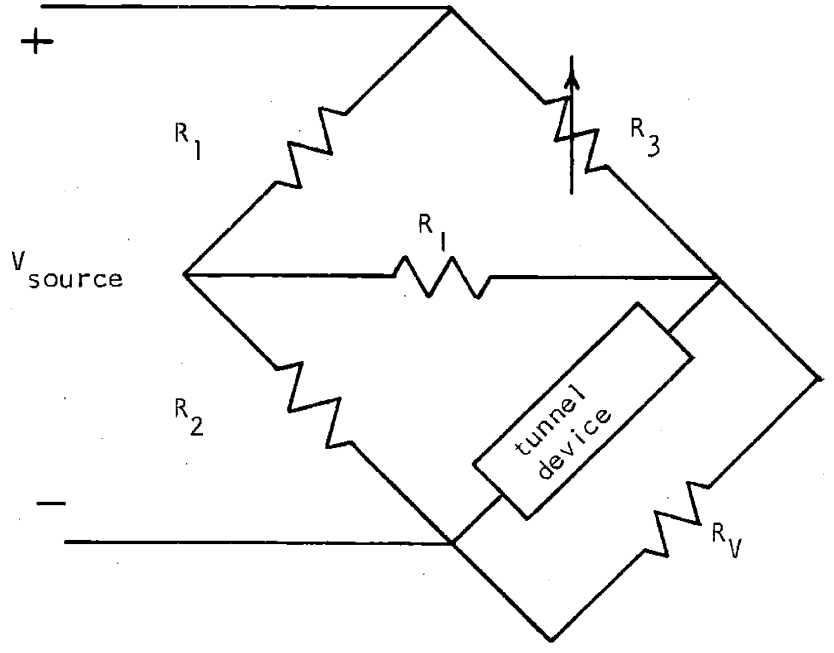


Figure 16

Bridge Circuit Used for AC and DC Measurements on the Tunnel Test Devices

and of course

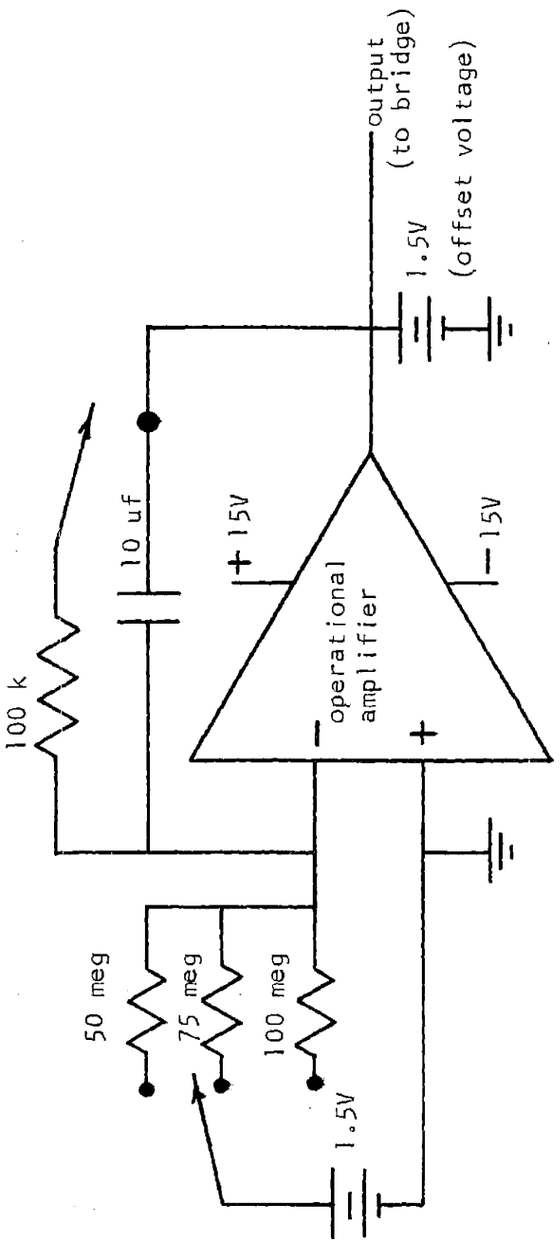
$$V_{R_V} = V_{sample} \tag{14b}$$

Typical values used are R_1 = 1 kΩ, R_2 = 30 kΩ, R_3 = 200 kΩ ten turn pot (for nulling the bridge) and $R_I \simeq R_V \simeq$ 1 megΩ. The actual transfer ratio for the bridge is I_s/V_{R_I} = 36.36 μA/V.

This bridge was connected to an oscilloscope and X-Y recorder, and the I-V characteristics of diodes and resistors were obtained very satisfactorily. In order to automate the measurement process, we designed a circuit to provide a constant DC sweep through the range -1.5 to +1.5 volts. This circuit, shown in Figure 17, is basically a DC integrator with a DC offset voltage. This circuit has the feature of being able to select three different sweep rates, a hold position, and a rapid discharge. Sweep rates range from 10 min/v to 60 min/v.

The next question involves AC measurements, and whether the DC equipment can be suitably modified. The important points in AC measurements are first, because of large capacitance, we need phase detection techniques, and second, because of 60 cycle and other noise problems, we need frequency selection and filtering. It happens that the PAR Lock-In Amplifier, Model HR-8 is ideally and uniquely suited for these measurements, in having both phase and frequency detection capabilities, as well as high gain.

Our DC bridge will be of value for AC measurement if, and only if, we can accurately separate the in-phase tunneling component and



Integrator Circuit Used to Provide Slow DC Sweep to Tunnel Test Devices

Figure 17

the 90° out-of-phase displacement current component. If the tunneling device is modeled as a parallel RC network, the AC analysis carried out in Appendix D shows tanθ of $V_{R_V}/V_{in} \simeq 10^{-4}$, i.e. zero for all practical purposes. This means that the measured output voltage is in phase with the applied signal and pure real. Now we have both a phase and a frequency reference to compare the device current with.

The lock-in amplifier is tuned to the desired frequency, and then, with no sample connected, the amplifier output is nulled using the phase control. It is important to note that even with no test device in the circuit, the external lead and fixture capacitance is significant (on the order of 100 picofarads). So that by using phase-nulling of the amplifier, we are in effect removing the 90° out-of-phase component. We verified this operation of the amplifier by attaching capacitors (with values ranging from 1 pf to 10 uf) to the bridge and observing no departures from null. However, when a parallel RC is attached, the amplifier output is proportional only to the conductance, even at extremes of R = 2 megΩ, C = 10 uf, and f = 25 kHz. Therefore we can use this Wheatstone resistance bridge for DC and AC measurements in conjunction with the PAR HR-8 Lock-In Amplifier.

The sensitivity of the bridge and lock-in amplifier, and the high signal to noise ratio, permit measurement of DC current down to 10^{-11} amp and AC current to 10^{-13} amp. This range is more than sufficient to handle the tunnel devices we have fabricated.

The final step is that of mounting and contacting the sample. As discussed in the previous section, it was judged too inconvenient to dice the wafer into chips and then bond these chips to headers.

Instead, we etch the back of the wafer to bare silicon using HF. Then a cylindrical brass block is etched with HCl, and the wafer placed on this block. The HCl serves the dual function of cleaning the brass and acting as an electrolyte for good ohmic contact. Contact to the tunnel devices on the front side of the wafer is made with a stainless steel probe tip. Measurements on virgin silicon wafers, both n- and p-type, showed this technique to provide good ohmic contacts (resistance $\simeq$ 10 ohms).

IV. RESULTS AND DISCUSSION

A. Results

Experimental results were obtained on twelve different test wafers. These results include DC current-voltage (I-V) curves, DC conductance, AC conductance at 10, 100, 1000, and 10,000 Hz, the difference between AC and DC conductance (to calculate surface state distribution), and capacitance-voltage measurements. The samples are identified in Table I.

Table I

Sample number	Type	Insulator thickness	Dopant (type, $/cm^3$)
P-63	p	40A*	boron 1×10^{15}
P-73	p	20A*	boron 4×10^{16}
N-73	n	58A	phosphorous 5×10^{14}
N-83	n	62A	phosphorous 6×10^{15}
N-124	n	52A	phosphorous 6×10^{15}
N-134	n	30A	phosphorous 5×10^{14}
N-144	n	30A	phosphorous 2×10^{16}
P-154	p	56A	boron 2×10^{16}
P-164	p	51A*	boron 4×10^{16}
P-174	p	31A	boron 1×10^{15}
P-184	p	67A	boron 2×10^{16}
P-194	p	24A*	boron 1×10^{15}

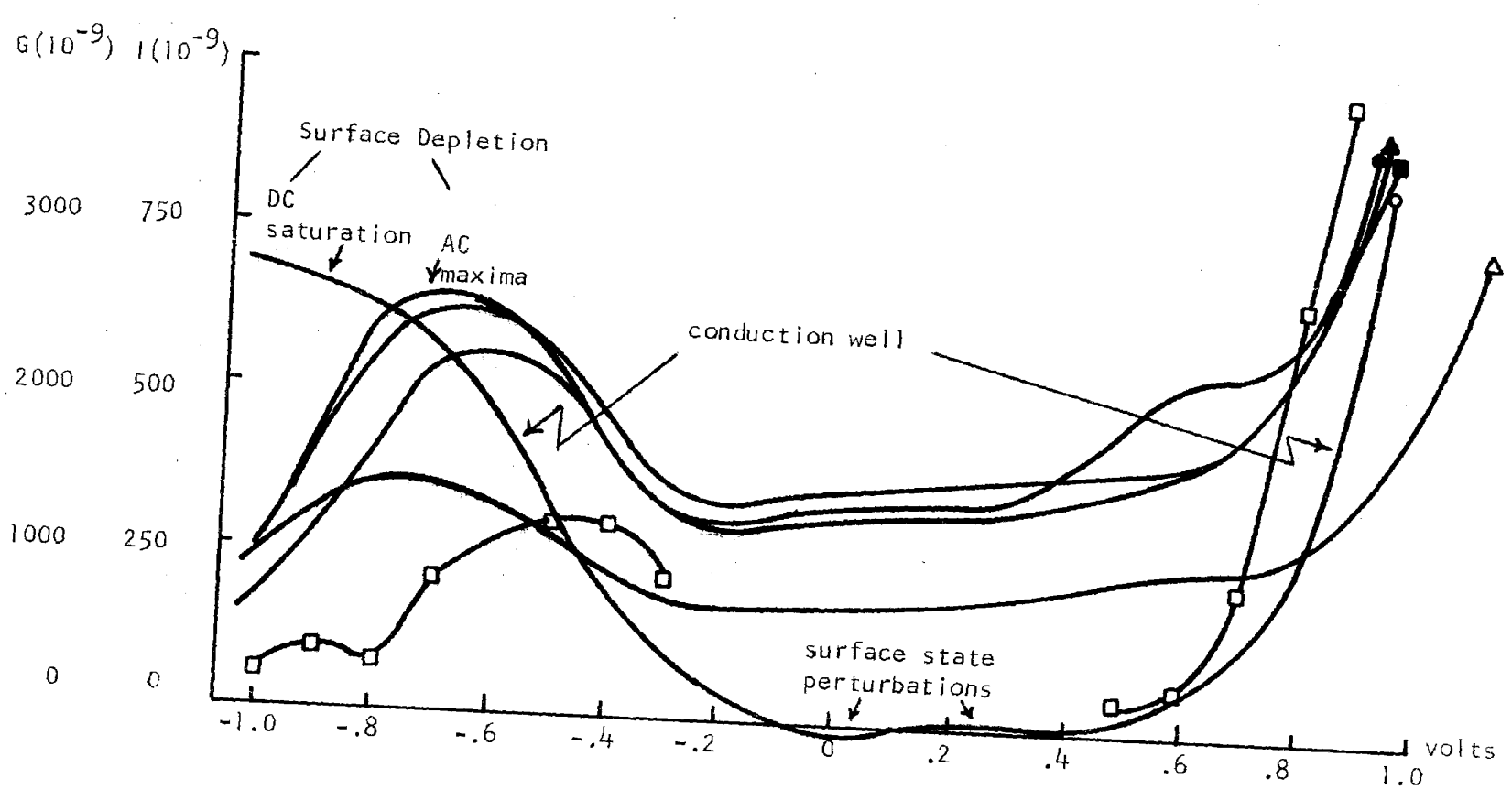
* Denotes rough estimate.

DC Measurements. In order to determine the correlation between the tunneling theory of Chapter II and actual device performance, we performed a series of measurements. The first of these measurements was the DC current-voltage characteristic.

Typical DC tunnel currents were in the 10^{-7} amp range; therefore, no special precautions other than short leads and direct grounding were needed for electrical measurements. A problem resulted, however, in making probe contact. If probe pressure were too light, contact resistance was high and the measurements were not reproducible; if pressure were too great, aluminum was scraped from the silicon dioxide and no contact was made. A successful technique was lowering the probe to the silicon surface adjacent to the contact pad, and the sliding the probe over to the aluminum, thus making contact. Measurements made using this procedure had low contact resistance and were reproducible.

Each test wafer had several hundred devices, and while many devices were non-functional (such as those at the wafer's edge where photo-resist build-up occurred), most exhibited uniform characteristics across the wafer. These characteristics were examined by measuring the current at a fixed voltage for a ten by ten array on each wafer. The measured currents were within ±3% of each other for the arrays.

The DC I-V characteristic of Figure 18 clearly shows the existence of a conduction well in the n-type sample. This well results from the forbidden region of the semiconductor, i.e. the tunnel gap which distinguishes MIS from MIM tunneling.



I-V Characteristics and Conductance

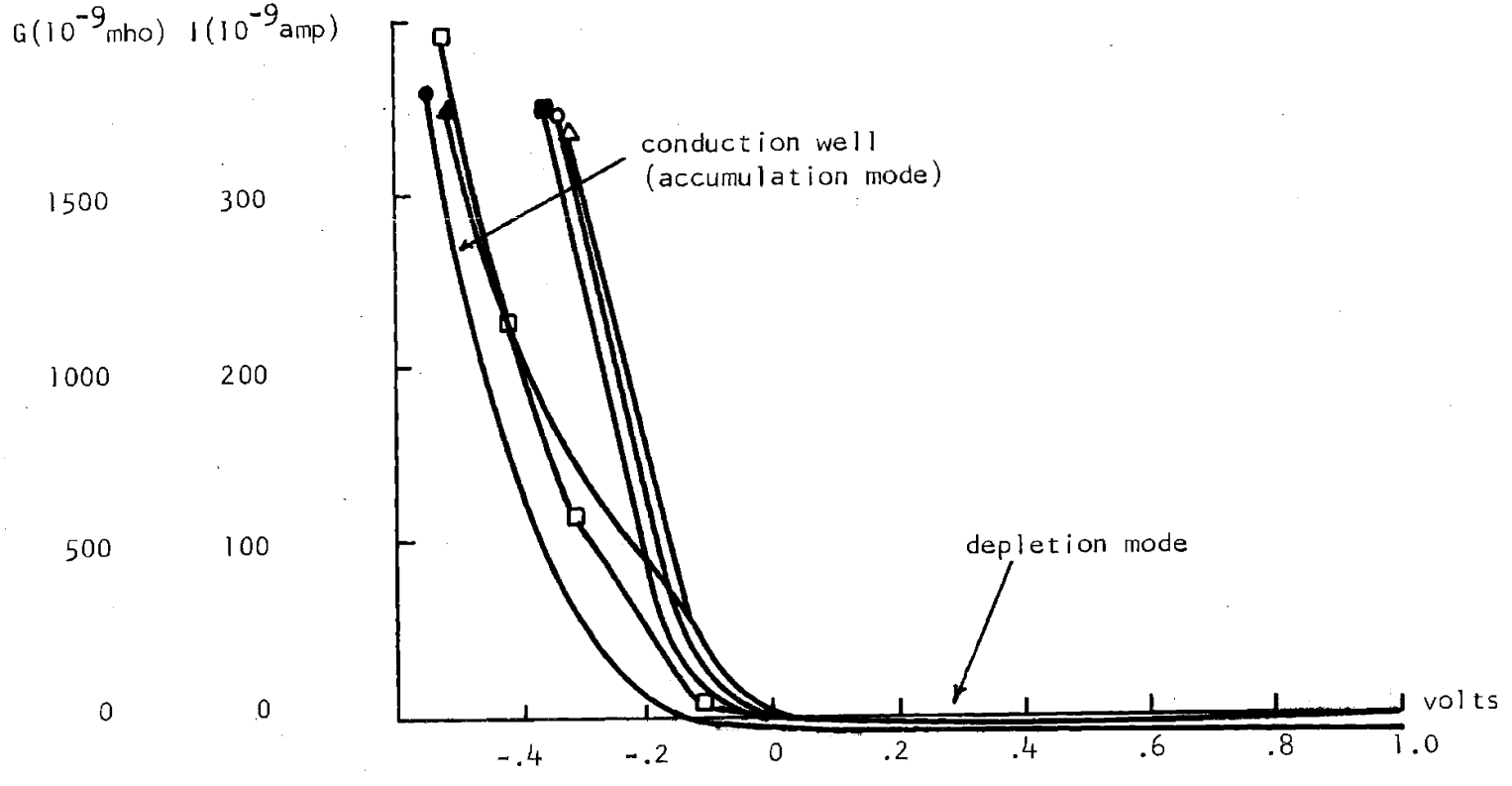
Wafer N-73

○ DC current-voltage
□ DC conductance
▲ 10 Hz conductance
● 100 Hz conductance
■ 1 kHz conductance
△ 10 kHz conductance

Figure 18

There are small perturbations observed in this well which are attributed to the transient response of surface states. These perturbations will be discussed in the interpretation of results. Note that in this figure the width of the conduction will is approximately 1.1 eV, the band gap of silicon. Furthermore, the voltage to the positive side of the conduction well corresponds to the valence band-Fermi level separation ($\simeq$ 0.7 eV); and the voltage to the negative side of the well corresponds to the Fermi level - conduction band separation ($\simeq$ 0.4 eV). While in this example the tunnel characteristics provide a basis for useful spectroscopic analysis of the semiconductor, there are instances where this technique does not apply, that is, when the semiconductor surface becomes depleted before the band edges are reached, as we see in the p-type sample of Figure 19. Of course, the surface of the n-type sample also becomes depleted, however, as seen in the example of Figure 18, depletion occurs after the band edge is reached.

In the enhancement mode for the n-type sample, that is, positive bias on the metal, the tunnel current rises exponentially with increasing voltage. With negative bias, the current starts to rise again (as in MIM tunneling) but the semiconductor surface is depleted, the current level becomes saturated (-.8 V), and the conduction decreases from a maxima (at -.7 V). The p-type sample (Figure 19) shows drastically different I-V characteristics. Since the bands at the surface of the silicon are bent down, the surface appears more n-type or less p-type. The n-type sample is actually enhanced at zero bias, and depletion does not result until fairly large



I-V Characteristics and Conductance Wafer P-164

● DC current-voltage
□ DC conductance
■ 10 Hz conductance
○ 100 Hz conductance
△ 1 kHz conductance
▲ 10 kHz conductance

Figure 19

negative voltages are reached (-.8 V); but the p-type sample is depleted at zero bias, thus the positive voltage side of the conduction well is not seen. In the accumulation mode, electrons become available for tunneling, and the current and conductance increases.

During processing of the tunnel devices it is possible for the aluminum to alloy with the semiconductor and form an ohmic contact, or to just contact the semiconductor and form a rectifying barrier. By direct observation we see that conduction is nonohmic; furthermore, in an injection mode the current would be strongly dependent on temperature[43] and illumination[44], as both change carrier concentration in the semiconductor. The tunnel samples were heated on a hot plate to 85°C and virtually no changes* were seen as compared with room temperature I-V characteristics. The samples were measured under no illumination, under the illumination of a microscope lamp, and that of a 250 watt spot light; no photo-effects were observed.

This line of experimentation gave confidence in the tunneling characteristics, especially in the case of p-type samples which, due to band bending, were depleted with no applied bias, thus showing a characteristic similar to a reverse biased diode.

The DC conductance was calculated by graphically differentiating the DC characteristics of Figures 18 and 19. This mechanical process was relatively inaccurate (estimated up to 20% error), but no other technique was readily available for measuring the DC conductance. The DC conductance is shown in Figures 18 and 19, and will be discussed in the interpretation of data.

* Exception, see page

AC Measurements. Ac measurements were made in an attempt to study the dynamics of tunneling currents and surface states. Typical AC currents were in the 10^{-10} amp range. Thus, special precautions were needed for electrical measurements. Care was taken with respect to lead length and layout, using only shielded cable, shielding of apparatus and connections with metal boxes, and the use of a two level ground system where distinction was maintained between "earth" and chassis ground. Even with these precautions, many times noise levels were too high to make AC measurements, because the laboratory was near high noise RF generators, and in the path of meteorological radar. We frequently resorted to late evening - early morning experimentation to complete AC measurements.

For the AC results, ΔI is measured in response to a fixed ΔV (0.5 mV) superimposed on the DC bias. Therefore the ΔI curve is directly proportional to AC conductance, and the ordinates on the AC curves of Figures 18 and 19 are in mhos, while those in Figures 20 and 21 are in log mhos.

The important features of the AC conductance curves (Figures 18 and 19) are the AC conductance well; that fact that 10, 100 and 1000 Hz curves are almost identical while the 10 kHz curve is considerably different; and that the AC conductance in the forbidden gap region is orders of magnitude greater than DC conductance in that same region. Each of these features is significant and will be discussed in the interpretation of results.

The insulator thickness data of Table I were obtained by plotting capacitance-voltage curves (CV), finding the capacitance associated

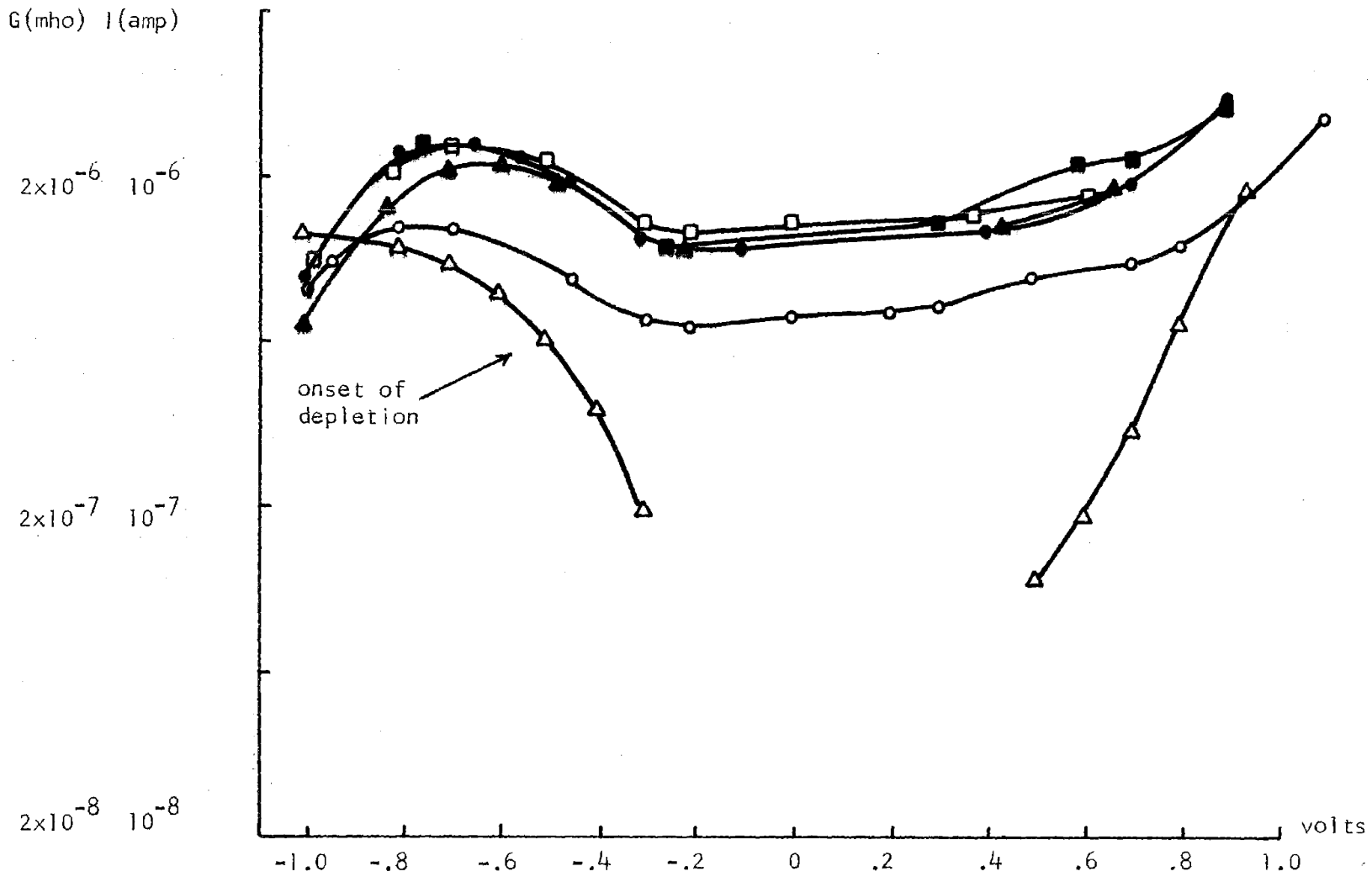
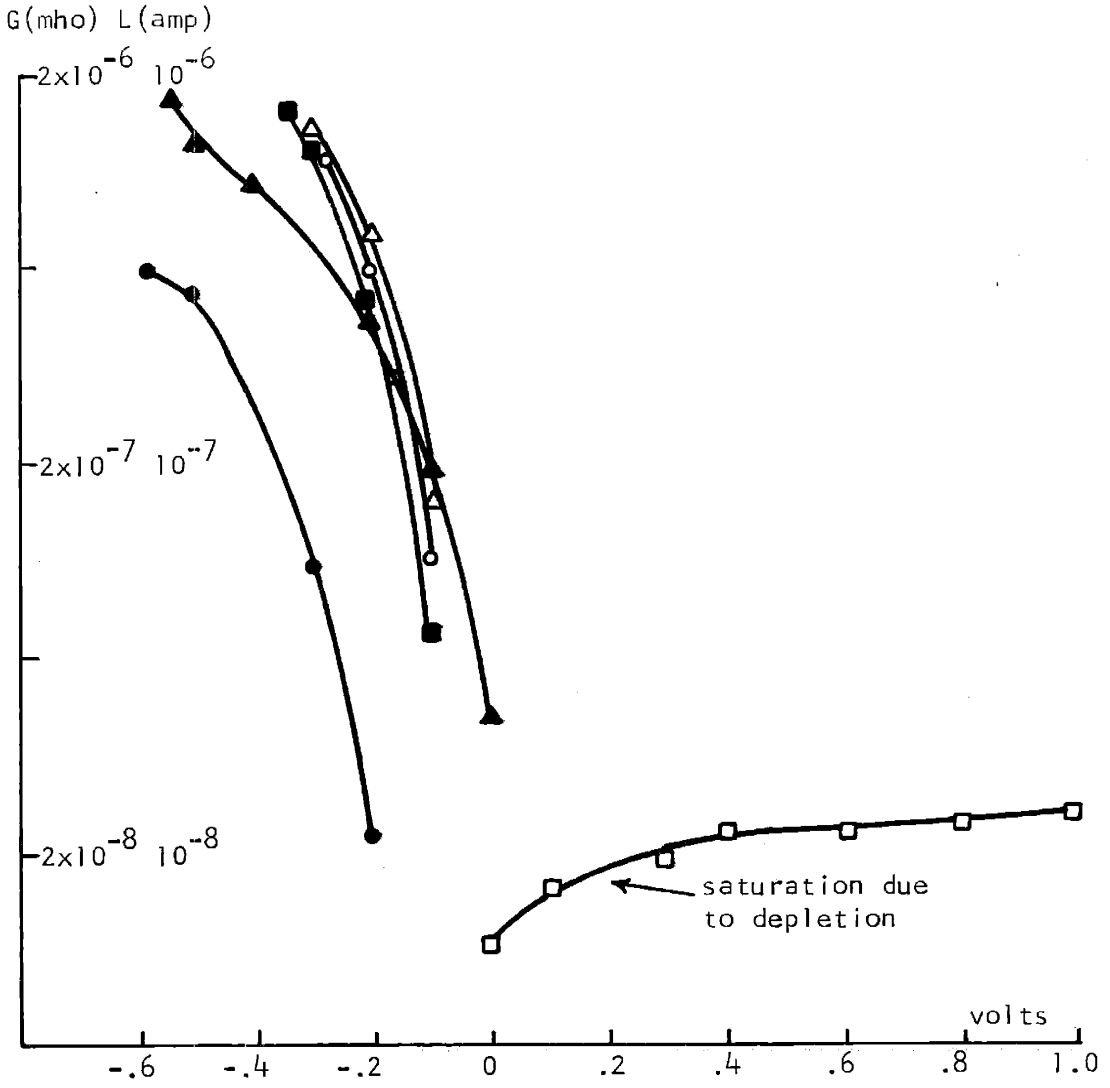


Figure 20

Log I-V Characteristics and Log Conductance Wafer N-73

△ DC current-voltage
● 10 Hz conductance
□ 100 Hz conductance
■ 1 kHz conductance
○ 10 kHz conductance



Log I-V Characteristics and Log Conductance Wafer P-164

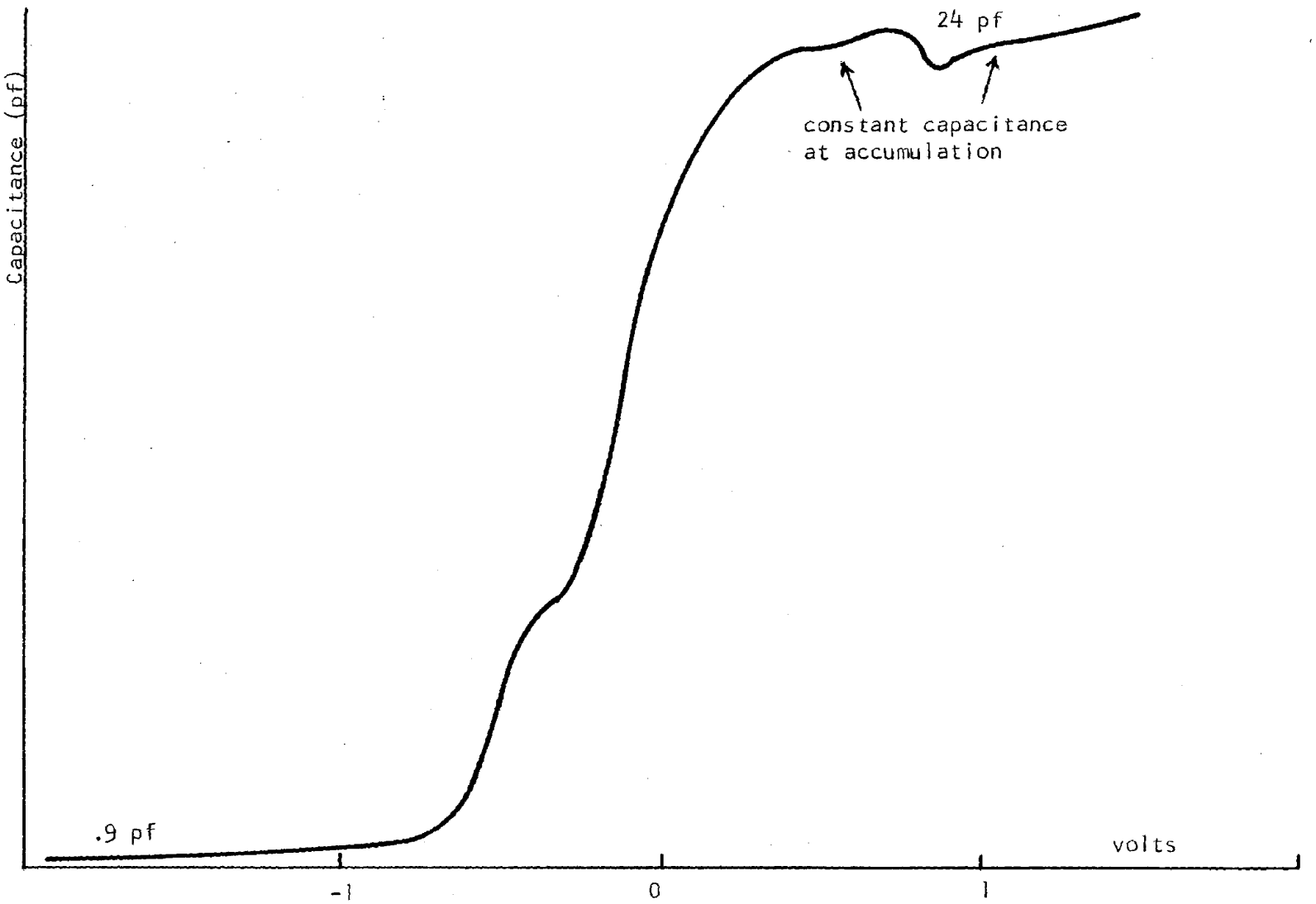
□ ● DC current-voltage
■ 10 Hz conductance
○ 100 Hz conductance
△ 1 kHz conductance
▲ 10 kHz conductance

Figure 21

with the tunnel insulator, and substituting this value into Equation E(2) of Appendix E. The CV measurements were taken on a Boonton Capacitance Meter at a frequency of 10 kHz. The same probe contacting setup used for DC measurements were employed, and these measurements proved especially simple to perform.

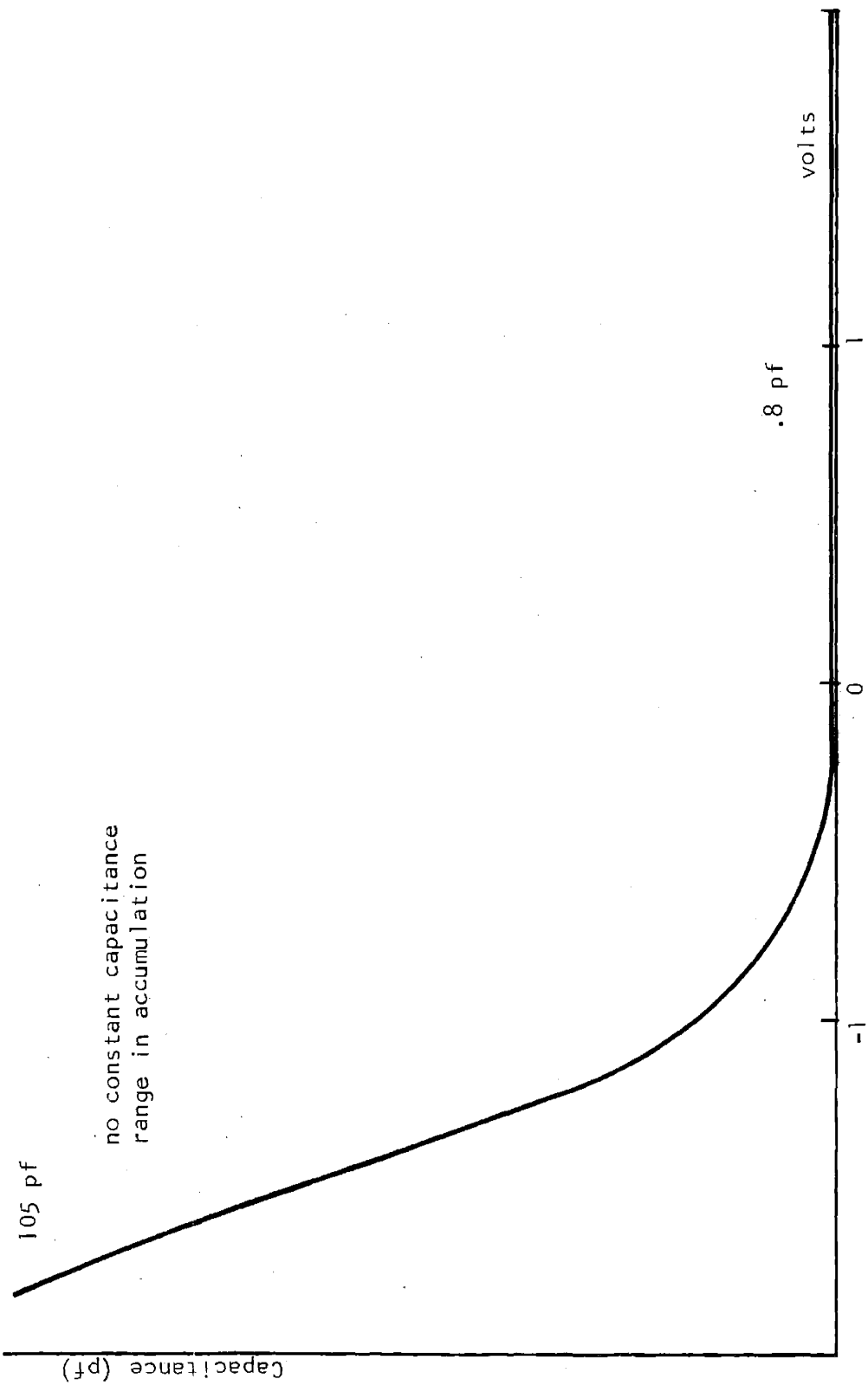
This thickness calculation depended on the assumption that a capacitance could be defined for the tunnel device. A tunnel capacitance was defined if the CV curves showed a constant value of capacitance when the semiconductor was brought into accumulation (positive bias on the metal for n-type semiconductors, and vice versa). This constant accumulation capacitance is analogous to the case of thick insulator MOS capacitors and Figure 22 shows such an example. In many other devices no constant accumulation capacitance range was observed (Figure 23), indicating departures from the ideal behavior of the MOS capacitor. For these devices, insulator thickness was roughly estimated using the capacitance at a predetermined bias voltage. This was, of course, only a guess, and a different procedure was derived (Equation 19).

A discussion of MOS behavior and interpretation of CV data are presented in Appendix A. Departures from the ideal behavior occur when tunnel currents become appreciable as compared to the displacement current. In this non-ideal case, arguments relating to space charge effects do not hold valid. The implications of this nonequilibrium effect will be presented in the interpretation of results.



Capacitance-Voltage Measurements Wafer N-134

Figure 22



Capacitance-Voltage Measurements

Figure 23

In this section we have presented the experimental data using typical curves to illustrate measurement detail. For completeness we have included data on all the other test wafers in Appendix F. Figures F1-F10 show the I-V characteristics and conduction data. Figures F11-F20 show the log of this data, and Figures F21-F30 show the CV curves.

B. Interpretation of Experimental Results

DC Measurements. The DC I-V characteristics shown in Figures 20 and 21 yield much valuable data on the semiconductor used in the MIS structure. These are:

1) type of material (n- or p-type)
2) onset of semiconductor depletion
3) flat band voltage
4) surface potential and surface state concentration.

P-type material will deplete with a positive bias on the metal, and n-type for negative bias. From observation of Figures 20 and 21 we can readily see where departures from exponential I-V characteristics occur, and saturation results indicating depletion. If this saturation occurs for positive bias on the metal, the semiconductor is p-type and vice versa. The onset of depletion is an important fact because it indicates when the electric field starts to penetrate into the semiconductor (i.e. the voltage drop is no longer across just the insulator) and when the bands are flat. The applied voltage at the onset of depletion is the flat band voltage V_{fb}, which is also

the surface potential ψ_s. We can immediately determine the surface electron concentration from

$$n_s = [n_b \exp(-q\psi_s/kT)]^{2/3} \quad (15)$$

where n_s = surface concentration (cm^{-2}), and n_b = bulk concentration (cm^{-3}).

We can use another technique for estimating surface charge which also provides an approach to thickness measurement. Under the assumption that the voltage drop is entirely across the insulator, the boundary condition to Maxwell's Equations gives us the surface charge at the insulator-semiconductor interface as

$$Q_{surface} = \varepsilon E \quad (16)$$

At the onset of depletion, the field strength in the insulator is a maximum (no field penetration into the semiconductor), and is

$$E_{max} = V_{sat}/d \quad (17)$$

Thus we can write the surface state concentration as

$$n_s = Q_{surf}/e = \varepsilon V_{sat}/ed \quad (18)$$

and solving for d we obtain

$$d = \varepsilon V_{sat}/en_s \quad (19)$$

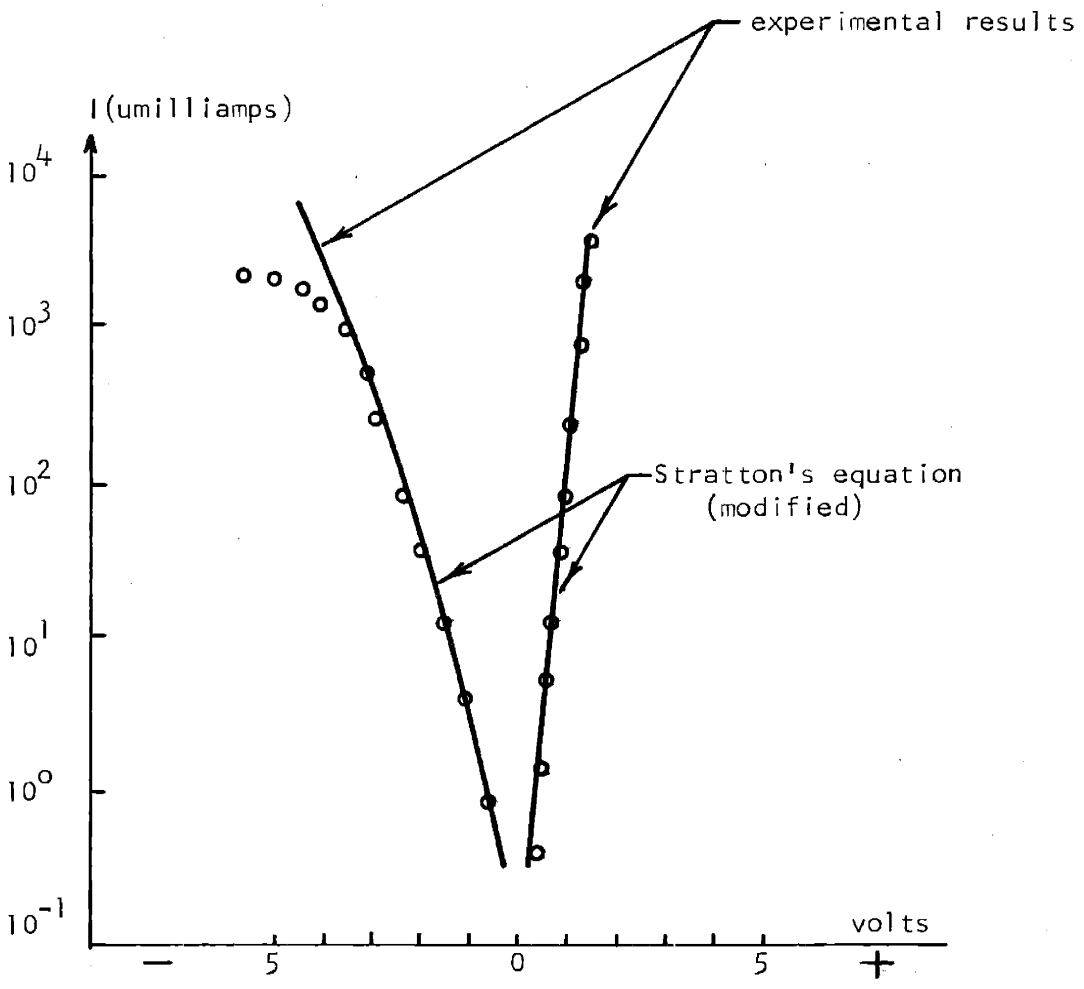
where we solve for n_s from equation (15). In Table II data are presented on the surface potential, surface charge, and insulator thickness.

Table II

Device number	ϕ_s(eV)	n_s(cm^{-2})	d(A)
P-63	.002	1.1×10^{10}	45
P-73	.008	9.5×10^{10}	19
N-73	-.176	6.9×10^{11}	55
N-83	-.080	2.8×10^{11}	61
N-124	-.090	3.6×10^{11}	54
N-134	-.202	1.4×10^{12}	32
N-144	-.070	4.8×10^{11}	32
P-154	.012	5.4×10^{10}	49
P-164	.018	7.2×10^{10}	54
P-174	.002(-)	1.1×10^{10}	40
P-184	.016	4.8×10^{10}	72
P-194	.001(+)	9.6×10^{9}	27

The DC tunneling characteristics of MIS devices are in good agreement with the theory. The modified Stratton equation (13) shows excellent agreement with the MIS tunnel curves of Figure 24. The deviations from modified MIM tunneling occur only when depletion occurs, i.e. when the field penetrates into the bulk of the semiconductor.

Dahlke and Sze[37] have made the observation that if doping is relatively low or the oxide film is extremely thin, then most of the applied voltage will drop across the semiconductor. In this case the Fermi level of the metal is pinned to the semiconductor surface,



Experimental I-V Characteristics of the MIS Structure

Figure 24

meaning that the applied voltage bends the bands of the semiconductor, so that the metal-semiconductor barrier height is the same for all applied voltages. In this case of course, we have the Schottky barrier diode. What these authors have neglected, however, is the intermediate case, where for one range of voltages the field is entirely across the insulator (tunnel emission), and for another range the field penetrates the semiconductor, which could possibly cause the Schottky type emission.

We examined this intermediate case and found that for n-type samples, the measured currents are indeed tunnel currents, as checked by temperature dependence. This would be expected in light of the fact that depletion does not take place immediately. For the p-type samples, however, which are depleted with zero bias, we notice a temperature anomaly. For negative bias and for very small positive bias (V = 75 mV) the measured currents are temperature insensitive, indicating tunnel conduction, but for larger positive bias the current exhibits a positive temperature dependence. Furthermore, this depletion current is relatively independent of bias, thus appearing analogous to the reverse current in a diode. Since we have already ruled out injection because there is no photo-electric effect (see page 60), the conduction mechanism in the positive biased p-type samples must be Schottky emission. As suggested by Dahlke and Sze, increasing the doping concentration or insulator thickness will eliminate the Schottky barriers.

An important feature of the DC conductance curves (Figures 18

and 19) is the appearance of a conductance well (very low conductance within the bandgap region, but the well width is not necessarily the width of the bandgap). Other investigators[28,45,46] have reported a conduction well, but their results have been found to contain inaccuracies[23], For example, Waxman[45,47] discusses the width of the conduction well in terms of depletion layer thickness in the semiconductor. These calculations are based on the fact that quasi-equilibrium conditions exist, i.e. tunnel currents are small and a true capacitance may be defined. As it turns out neither of these assumptions generally hold true, because tunnel currents can be fairly large (on the order of the displacement current) and as we show in Figure 23, the capacitance-voltage plots are not the same as those for thick insulator MOS capacitors. The large conductance well predicted by Waxman is not consistent with other data[28,37], nor with ours, nor even with some of his own experimental curves, because one of his basic assumptions, i.e. a well defined MOS behavior as indicated by CV data, does not hold. C. B. Duke[23] points out that Shewchun et al.[46] are in error on their calculations because they neglect image-force potential and trapped charge in the insulator. They make several other simplifying assumptions, and conclude a conductance well wider than actually observed.

The observation of the conductance well is significant because it clearly shows the distinguishing characteristics of MIM and MIS tunneling.

We have made careful analysis of this conductance well with

respect to CV data and equilibrium assumptions, and have found that the position of the side of the well is determined by the band edge of the semiconductor except when:

1) the CV curves show a constant capacitance range for accumulation bias less than the Fermi level-band edge voltage, or

2) the semiconductor surface becomes depleted at a voltage less than the Fermi level-band edge voltage.

In these exceptions, the position of the side of the conduction well is determined by space charge layer considerations as Waxman and Shewchun predicted. In our more general findings, however, the conduction well side appears at the voltage corresponding to the Fermi level-band edge separation, thus providing us with a spectroscopic technique.

AC Measurements. As postulated earlier, interaction with a surface state is made when the applied DC bias sweeps the Fermi level of the metal to the energy of the surface state. Then the small signal AC perturbation (superimposed on the DC sweep) causes the state to charge and discharge, producing a steady state signal. Clearly this steady state current will increase with increasing density of states.

The DC conductance results primarily from tunneling interaction with the conduction and valence bands. The interaction with surface states at DC is greatly reduced due to charging of the surface states and the resulting thermal equilibrium. This idea is verified by experiment (DC conductance in Figures 18 and 19).

AC conductance, on the other hand, results from interactions with both the band and intergap surface states. As described earlier (page 34), the AC perturbation superimposed on the DC sweep provides a steady state tunnel current resulting from electronic surface structure within the gap. Thus the AC measurement reflects the contribution of surface states to tunnel conduction.

The two most important parameters to consider with respect to AC conductance are the recombination-generation times of the surface states, and the effects on the tunneling barrier height as a function of applied bias.

The tunnel barrier for our MIS devices is the conduction band edge of the silicon dioxide. This results from oxide band bending due to interface charge, making the insulator appear extrinsic (n-type) rather than intrinsic as would be expected. Using the rather good assumption (see page 27) of a trapezoidal tunneling barrier, the effective change in barrier height is $V_{applied}/2$. Using equation (2) we can estimate the effect of the barrier height change on tunneling probability.

$$\frac{T(V)}{T(0)} = \exp\{-2(\frac{2m^*}{\hbar^2})^{1/2}[(W + V/2)^{1/2} - W^{1/2}](x_2 - x_1)\} \qquad (20)$$

Now if V/2W is less than one (V_{max} = 1 and W ≃ 2), a series approximation yields

$$\frac{T(V)}{T(0)} = \exp[-2(\frac{2m^*}{\hbar^2})^{1/2} \frac{V}{4W^{1/2}} (x_2 - x_1)] \qquad (21)$$

and substitution of typical values,

$$\frac{T(V)}{T(0)} = \exp[-.057(x_2 - x_1)V] \triangleq p^{-1}(V) \qquad (22)$$

where $x_2 - x_1$ is measured in A, and V in volts.

This expression shows that the contribution of electrons to the tunnel conductance is enhanced with negative bias on the metal. Therefore the first step in converting tunnel conductance into density of states is to scale the conductance curves by the reciprocal of equation (22), i.e. P(V).

We now consider the effects of the recombination-generation time of the surface states. Because the displacement current is usually large compared with the tunnel current, phase detection methods are necessary to separate these two components. In fact, we must always look only at the in-phase signal, because even a small component of the 90° out of phase displacement current can mask the tunnel current. Therefore we have to be certain that the tunnel current is indeed in-phase.

It has been reported[48] that the tunnel transiton time is very fast (on the order of 10^{-10} seconds). For this reason it is the time delay due to recombination-generation, rather than tunneling, which would cause the tunnel current to lag behind the signal voltage, thus causing a phase shift. The fast surface states, Q_{ss}, have recombination times of 10^{-5} to 10^{-6} seconds[8,9], and if the time constant of the applied AC signal is large compared with these recombination times, the phase shift will be very small and will not affect the tunnel current measurement. At higher signal frequencies,

meaning smaller time constants, the phase shift will become appreciable, and only a component (the pure real component) of the tunnel current will be measured. In effect, at low frequencies, electrons are free to contribute to tunneling, but at higher frequencies electrons in traps can not escape quickly enough to follow the signal frequency, and thus the number of electrons available for tunneling is greatly reduced.

This effect is experimentally verified in Figures 18 and 19. We find that at the lower frequencies, 10, 100 and 1000 Hz, the tunnel conductance curves are essentially the same. At higher frequencies (10 kHz) however, the conductance has decreased considerably, and it drops very rapidly with increasing frequency.

Another way of expressing this same result is that at lower frequencies the full amount of charge available for tunneling is transferred and does contribute to the tunnel current. Of course this charge, the fast surface state density at a given energy level, is transferred according to the tunnel probability of equation (4), but the magnitude of this charge can be determined from the tunnel current.

$$Q_{ss} = \int J_{tunnel} dt \tag{23}$$

Since we measure the RMS value of the tunnel current with the lock-in amplifier, and the tunnel current is sinusoidal,

$$J_{tunnel}(t) = \sqrt{2}\, J_{RMS} \sin(2\pi t/T) \tag{24}$$

and the charge transferred during tunneling is

$$Q_{ss} = \int_{0}^{T/2} \sqrt{2}\, J_{RMS} \sin(2\pi t/T) \tag{25}$$

Evaluation of this integral yields

$$Q_{ss} = \frac{T\sqrt{2}\ J_{RMS}}{\pi} \tag{26}$$

Now if we factor in the tunnel area, electronic charge and AC perturbation voltage, the surface state density, #/cm^2/eV, is

$$N_{ss} = \frac{T\sqrt{2}\ J_{RMS}}{\pi eA\Delta V} \tag{27}$$

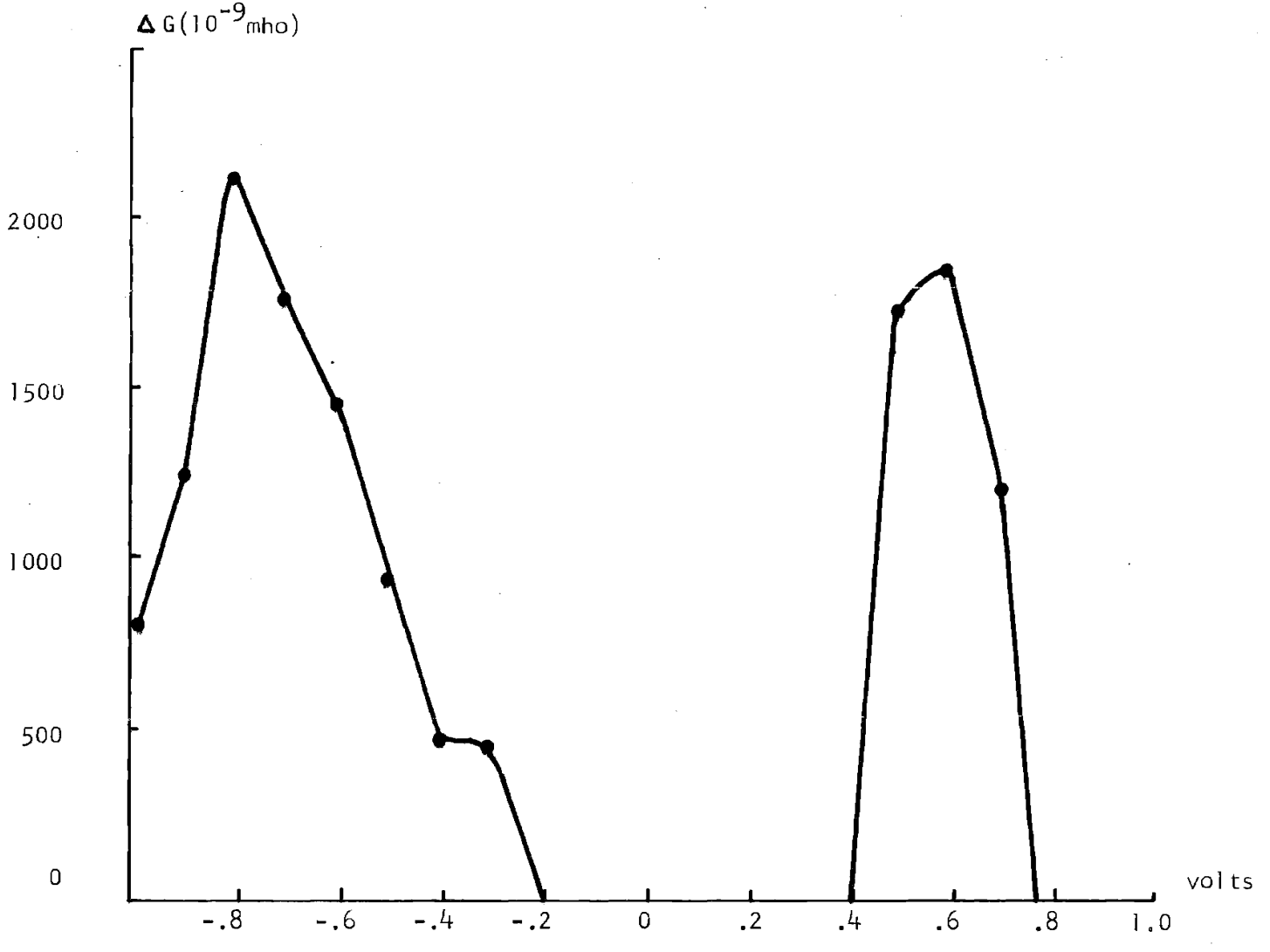
As discussed earlier, the AC measurements yield information on both intergap and band edge states, while the DC measurements primarily represent the band edge contributions. If we subtract DC from AC conductance, we have a ΔG due to intergap surface states and

$$\Delta G = \frac{\Delta I_{AC} - \Delta I_{DC}}{\Delta V} = \frac{J_{RMS}}{\Delta V} \tag{28}$$

the change in conductance data are plotted in Figures 25, 26 and F31-F39. Substitution of equation (28) into equation (27) yields

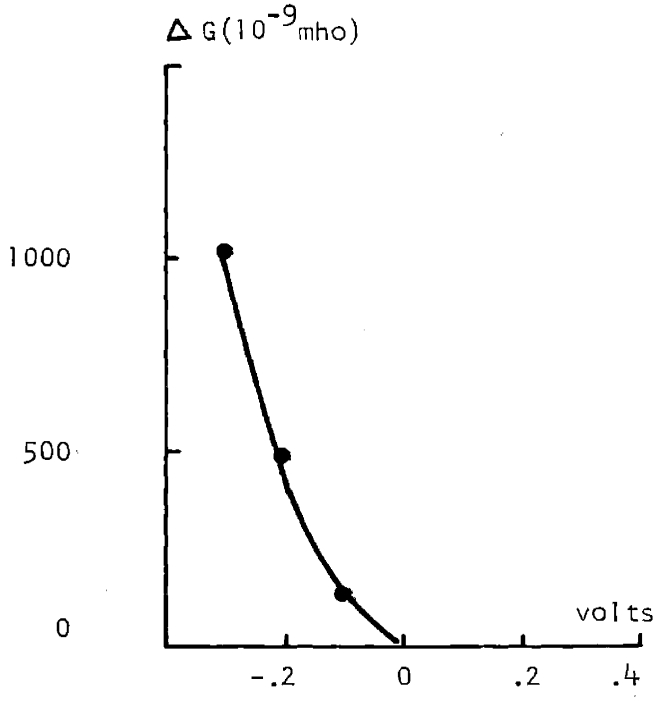
$$N_{ss} = \frac{T\sqrt{2}\ \Delta G}{\pi eA} \tag{29}$$

This result contains a time constant T, meaning N_{ss} seems frequency dependent. We must remember, however, the mechanism of this tunnel charge transfer. At some positive value of the sinusoid, a threshhold voltage is reached where electrons tunnel from the semiconductor surface states to the metal in a time determined by the recombination-generation time τ_{rg} of the fast states ($\simeq 10^{-6}$ seconds). As the sinusoid goes over the peak and descends to this same threshhold voltage, the same surface states fill in another



Surface State Conductance Wafer N-73

Figure 25



Surface State Conductance Wafer P-164

Figure 26

recombination-generation time constant. For the negative going part of the sinusoid we see a similar effect. At a negative threshhold, electrons tunnel from the metal to semiconductor surface states (at a different level, of course, from the positive part of the cycle) in a recombination-generation time constant. And, after the negative peak, electrons tunnel back to the metal in a recombination-generation time constant.

Thus during one cycle of the AC perturbation, a minimum of four fast state time constants must occur for maximum tunnel charge transfer. At high frequencies ($T < 4\ \tau_{rg}$), the charge does not have a chance to transfer and tunnel current will greatly decrease.

At lower frequencies ($T > 4\ \tau_{rg}$) full charge transfer will occur, but the integral of Jdt is not a true measure of tunnel charge because of the "spaces" between the four fast state time constant pulses. Therefore an accurate measure Q_{ss} from equation (23) is made when T equals four recombination-generation time constants (i.e. $T = 4 \times 10^{-6}$ second if we assume a typical value of $\tau_{rg} = 10^{-6}$ second).

Using this value for T, equation (29) becomes

$$N_{ss} = 5.54 \times 10^{17}\ \Delta G$$

and by bringing back the tunnel probability factor equation (22), the conversion from change in conductance ΔG to actual number of surface states/cm^2/eV becomes

$$N'_{ss} = P(V)N_{ss} = 5.54 \times 10^{17} \exp[.057(x_2 - x_1)V]\Delta G$$

Typical results of this calculation are plotted in Figures 27 and 28, and the data on the other test wafers are presented in Appendix F,

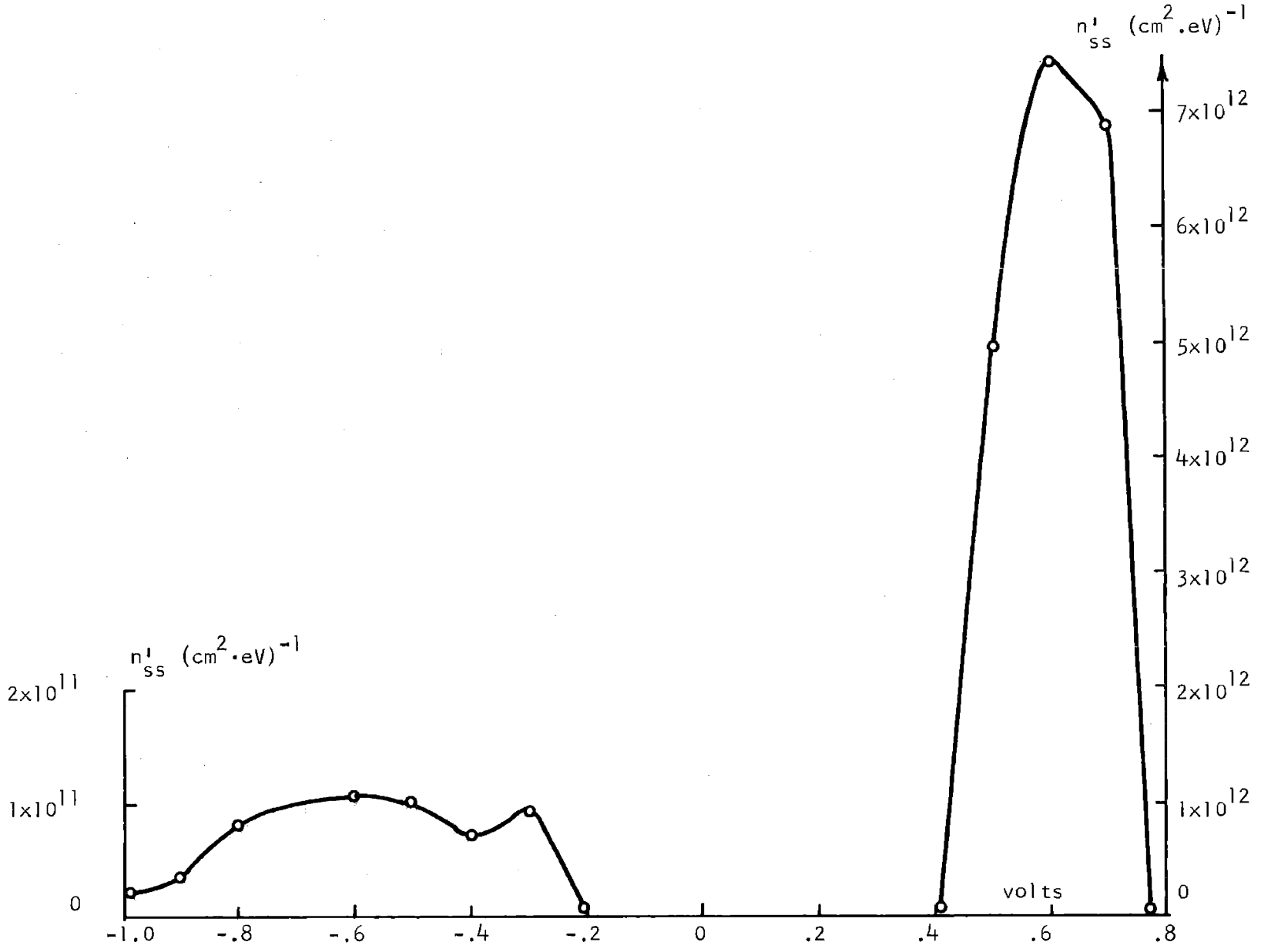


Figure 27

Surface State Distribution as Determined from Tunnel Conductance
Wafer N-73

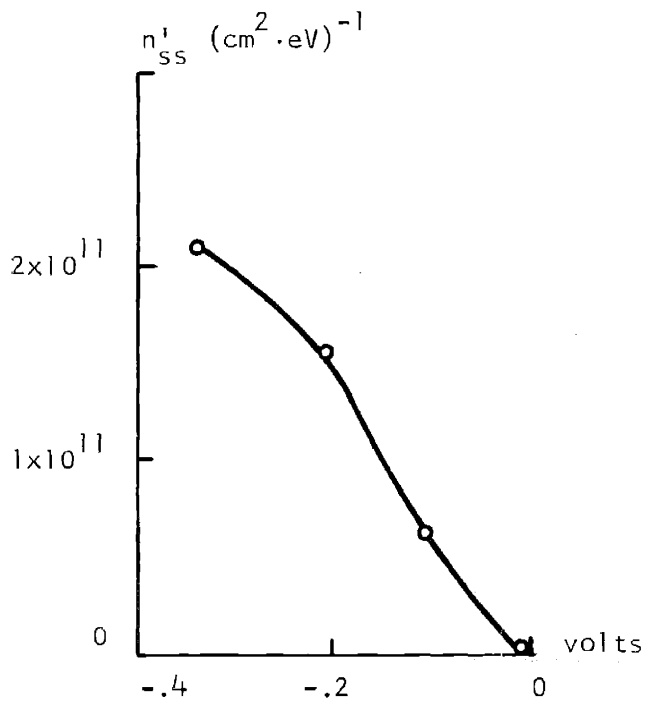


Figure 28

Surface State Distribution as Determined from Tunnel Conductance
Wafer P-164

Figures F40-F48.

We must point out at this time that there is a subtle difference between high frequency techniques causing a phase shift and high frequency techniques causing a reduction in charge transfer. At frequencies when the phase shift comes into importance ($\simeq 10^4$ Hz), charge transfer is still complete; however, the lock-in amplifier measures only the in-phase component which decreases proportionally to the cosine of the phase angle. At higher frequencies ($\simeq 10^6$ Hz) in addition to this phase shift, the recombination-generation times of the states do not permit all the tunnel electrons to follow the applied signal.

A further comment on the AC conductance curves is necessary. Analogous to the DC conductance well is an AC conductance well. We have found, contrary to that reported by Waxman[45], that the AC conductance curve forms a well, but for biases which take the semiconductor into depletion, the side of the well drops to a minima rather than rising continuously. This effect is apparent in Figure 18 and, of course, results from the depletion of surface electrons which contribute to tunneling.

V. SUMMARY

In this research, the theory of MIM tunneling is developed and adapted to MIS tunneling. One essential point is the approximation of the tunnel transimission coefficient. The various approximation techniques include the Stratton method involving an expansion of the transmission expression, which we have used here; the WKB approximation; the Holm-Chow-Simmons method, where the actual barrier is replaced by an equivalent rectangular barrier; and of course, exact numerical integration worked out on computers. Duke discussed these techniques and showed that for limited voltage ranges ($|V| < 1.8$ volts), these methods all hold within a few per cent of each other. Other modifications discussed include the tunneling gap, the transition probability, and the field distribution in the insulator.

Other investigators have reported a tunnel conduction well, but have made errors in their interpretations. We have, for the first time, reported that the sides of the conduction well correspond to the semiconductor band edges whenever the tunnel current is appreciable compared with the displacement current.

We report an unusual device, which for one range of voltage, the conduction mechanism is internal field emission (tunneling), and for another range, the conduction mechanism is Schottky emission. When these devices are operated in depletion the electric field penetrates the semiconductor, and the Fermi level of the metal is pinned to the semiconductor surface. The barrier height remains

constant, analogous to the situation of a reverse biased Schottky diode. In the enhancement mode, the electric field drops entirely across the insulator, i.e. the case of internal field emission. The current in the enhancement mode is relatively temperature insensitive, while in the depletion mode a positive temperature dependence is measured. This temperature dependence characterizes a "hybrid" tunnel-Schottky device. The hybrid effect is seen only in p-type samples because these devices are depleted with zero bias, indicating strong depletion and field penetration into the semiconductor for positive bias. The n-type samples are not depleted until negative voltage approaching the band edge is reached, thus the conduction mode is always tunneling.

We present a new interpretation of the AC tunnel mechanisms. Rather than modeling a tunnel time constant as others have done, we have made careful phase measurements of the AC tunnel conductance and arrived at the following conclusions. If sufficient time is allowed for a state to completely fill or empty (i.e. a recombination-generation time constant τ_{rg} plus a tunnel transition time τ_t), the measured tu-nel current will be independent of frequency. At higher frequencies, states can only partially fill or empty, thus tunnel currents will decrease with increasing frequency above some fixed value of frequency. Since $\tau_t << \tau_{rg}$, this critical frequency is determined only from τ_{rg}. Experimental data agree with our observation that AC tunnel currents are constant over a wide frequency range, but decrease at high frequencies.

The value of tunneling spectroscopy as a tool for studying semiconductor surfaces is determined by the diversity of data obtained using this technique, and, noting that tunnel phenomena probe only the outer surface of the semiconductor under investigation (because tunnel probability tells us that 99% of the tunnel electrons come from within 5A of the surface).

Data obtained on silicon using tunnel spectroscopy include the type of material (n- or p-type), the surface potential, the surface charge (these data are presented in Table II), and the surface state distribution as shown in Figures 27 and 28. The surface charge ranges from $10^{10}/cm^2$ to $10^{12}/cm^2$ and fast surface state densities fall into the $10^{11}/cm^2$ range. These measurements are in good agreement with measruements using other techniques reported in the literature. We observed peaks in the surface state distribution near the band edges, while concentrations were relatively small deep in the band gap. It is interesting to compare the surface state distributions of Figure 27 and 28, with data obtained using other experimental techniques (field effect, capacitance-voltage, surface recombination, contact potential, etc.). Many[8] summarizes these data, and for convenience, they are reproduced in Table III. These measurements show discrete levels distributed throughout the band gap and give indication that a continous distribution is apropo.

Table III

Summary of Fast State Measurements on (111) Silicon Surfaces*

Position (eV)	Density (cm^{-2})
.425	2.5×10^{12}
.400	-
.375	8.0×10^{11}
.275	10^{12}
.250	-
.138	2.0×10^{11}
.125	10^{12}
.100	10^{12}
.075	10^{12}
.013	2.0×10^{11}
.000	5.0×10^{12}
-.050	10^{12}
-.075	3.0×10^{11}
-.175	10^{12}
-.200	3.0×10^{12}
-.300	3.0×10^{12}
-.400	3.0×10^{12}
-.425	1.5×10^{12}

* From Many[8].

Suggestions for Future Work

In order to more fully develop the technique of tunneling spectroscopy, there are certain work areas not covered in this research which should be carried out. All of our measurements were done on the (111) surface of silicon, yet the (110) and (100) planes are also of importance. It has been found that the fast surface state density decreases as we go from the (111) to (110) to (100) planes, and it would be of great value to make tunneling measurements on these faces and determine correlation with the capacitance-voltage measurements.

We have observed hysteresis in our tunneling measurements, similar to that occuring in capacitance-voltage experiments. We feel this hysteresis results from the drift of mobile ions (slow states). Waxman has also reported hysteresis, but no one to date has tried to extract slow state data from this phenomenon. Analogous to techniques used in capacitance-voltage experiments, it should prove relatively simple to make slow state measurements.

An important set of measurements necessary to deepen our understanding of tunneling is low temperature data. It is at low temperatures (below 77°K) where all other conduction mechanisms become negligible with respect to the tunnel current. Furthermore, by observing the behavior of the measured current over a wide temperature range, we can be better able to label currents as tunnel, ohmic, or Schottky (Poole-Frenkel).

Finally, a very important potential application of the tunneling

spectroscopy technique would be its use on different semiconductor materials. There are many fabrication problems to overcome in using different semiconductors such as oxide growth, photo-processing or other masking technique, metallization, and electrical contact. However, with the increasing interest in new materials, particularly gallium phosphide, gallium arsenide, and indium antimonide, it would be worthwhile to approach these problems in order to get new surface measurements.

Appendix A

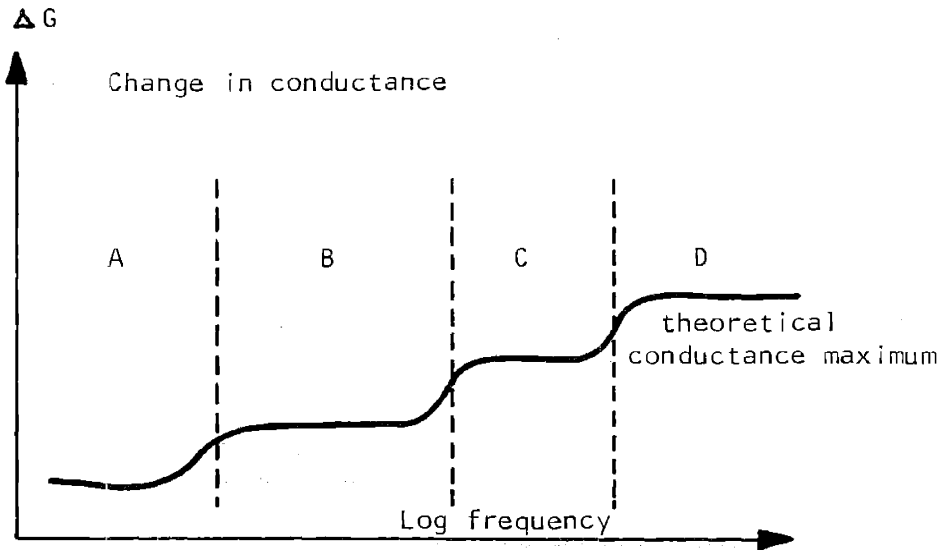
The Field Effect and Capacitance Voltage Techniques for the Investigation of Semiconductor Surface States

I. The Field Effect

The field effect device is merely a metal-insulator-semiconductor (MIS) sandwich, with contacts on the metal and semiconductor. When a voltage is applied to the metal plate, a charge is induced at the semiconductor-insulator interface, thus changing its semiconductor properties. An estimate of the change in surface charge, i.e. change in surface conductance, can be made from the electric field strength. The observed change, however, is only a fraction of the expected change, on the order of 10%. This is due to surface states trapping the induced charge.

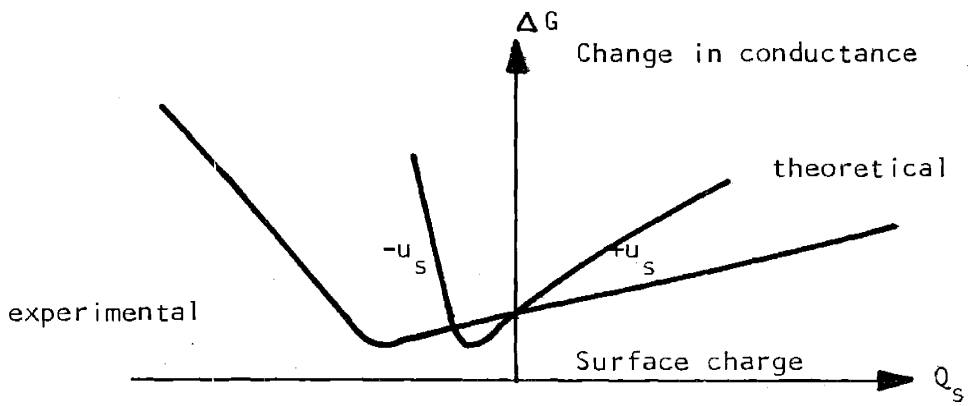
Sinusoidal Field Effect. If a sinusoidal voltage of varying frequency is applied to the metal plate, the change in conductance will range from its theoretical maximum at high frequency to a minimum at low frequency. At high frequencies, the electrons are moving too fast to fall into traps, so all mobile carriers contribute to the conductivity (region D of Figure A1). As the frequency decreases, the traps or surface states with fast recombination times (fast traps) start to fill, and the observed conductivity is lower (regions B and C of Figure A1). Finally, at lower frequencies, the slow traps start to fill, and the conductivity will reach a minimum (region A of Figure A1).

The very fast surface states (recombination time less than



Time Dependence of Surface States Shown Through the Frequency Response of the Sinusoidal Field Effect

Figure A1



Sinusoidal Field Effect to Determine Surface Potential u_s, and Trapped Charge Q_{ss}

Figure A2

microseconds) are labeled as Q_s, and very little is known about them, except that the density is on the order of $10^{10}/cm^2$, and that they are located at the semiconductor-insulator interface. The fast surface states, Q_{ss}, (recombination time ranging from milliseconds to microseconds) are attributed to silicon at the interface (non-stochiometric SiO_2). It has been found[49] that density of Q_{ss} increases with oxides grown on (100) to (110) to (111) planes. This is due to the fact that the (100) planes best accomodate the SiO_2 structure[50]. The slow states (recombination time ranging from tenths of seconds to seconds) are denoted by Q_D, mobile ions in the oxide, and by Q_{surf}, very slow states caused by absorbed gases on the outer oxide surface and moisture.

The surface charge, Q, induced by an applied voltage V is $Q = CV$. The surface charge consists of induced charge in the space charge region, ΔQ_{sc}, and charge trapped in surface states, ΔQ_{ss}. The space charge can be written as $\Delta Q_{sc} = q(\Delta p_s - \Delta n_s)$ and the change in surface conductance as $\Delta G_s = q(\mu_p \Delta p_s + \mu_n \Delta n_s)$. Note that $\Delta G_s / \Delta Q_s$ has the dimensions of mobility, and this ratio is defined as the field effect mobility.

$$\mu_{fe} = \frac{q(\mu_p \Delta p_s + \mu_n \Delta n_s)}{q(\Delta p_s - \Delta n_s) + \Delta Q_{ss}}$$

In the limiting case where the material is either n- or p-type, it is easily seen that μ_{fe} is less than the bulk mobility, μ_n or μ_p, depending on ΔQ_{ss}.

$$\mu_{fe} = \begin{cases} \mu_p(1 + \Delta Q_{ss}/q\Delta p_s)^{-1} & \text{p-type, } \Delta Q_{ss} > 0 \\ -\mu_n(1 - \Delta Q_{ss}/q\Delta n_s)^{-1} & \text{n-type, } \Delta Q_{ss} < 0 \end{cases}$$

Now the various field effect parameters can be determined by plotting ΔG_s vs induced surface charge Q, for the experimental and theoretical cases (Figure A2), where the theoretical plot ignores trapped surface charge. The intercept of the experimental and theoretical curve at Q = 0, yields the surface potential (μ_s). The horizontal difference between the two curves yields ΔQ_{ss} as a function of the surface potential (Figure A3)[51].

The energy of the surface state, E_T, is determined from the inflection point of $d\Delta Q_{ss}/d\mu_s$. And the density of surface states, N_t, is determined from the slope of Figure A2 at $\mu_s = E_T$, i.e.

$N_t = -4dQ_s/d\mu_s$

Pulsed Field Effect. If a voltage pulse is applied to the metal plate, the time constants of the surface state can be measured directly, as indicated in Figure A4. The kinetics[52] of the system are:

$$\frac{dn_t}{dt} = -g(N_c - n_c)n_t + rn_c(N_t - n_t) \qquad (A1)$$

where n_t = no. of electrons in surface states

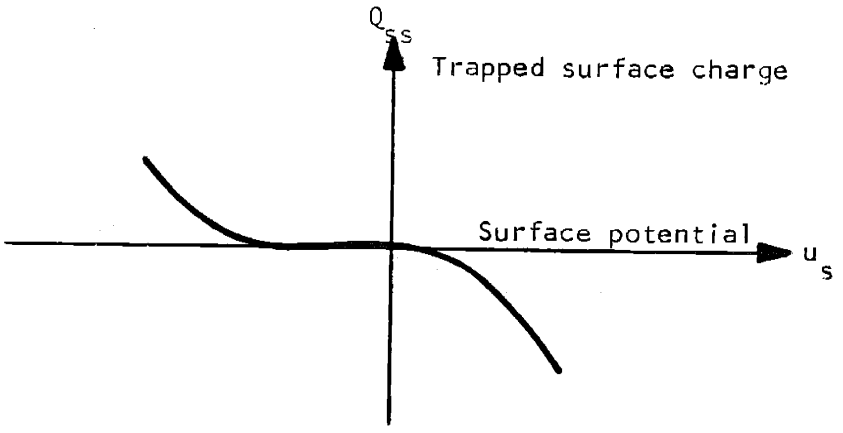
N_t = no. of traps

n_c = free electrons at surface

N_c = C.B. state

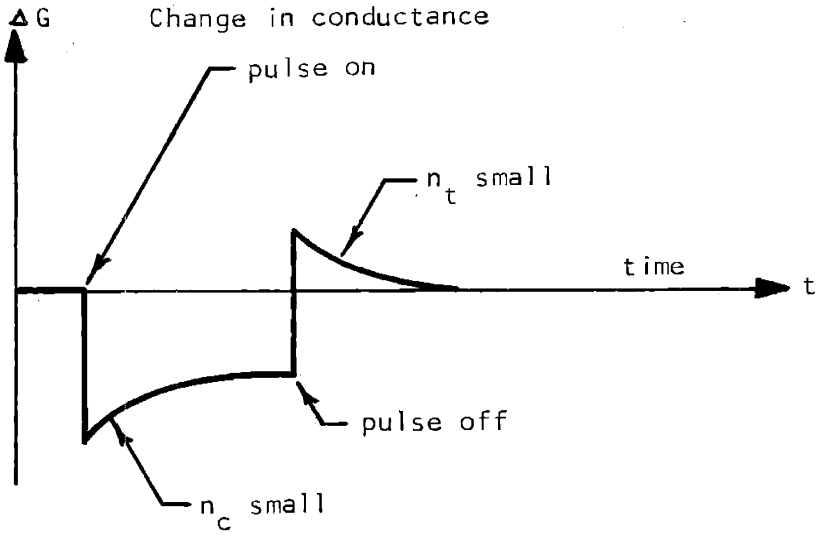
r = recombination rate

g = generation rate



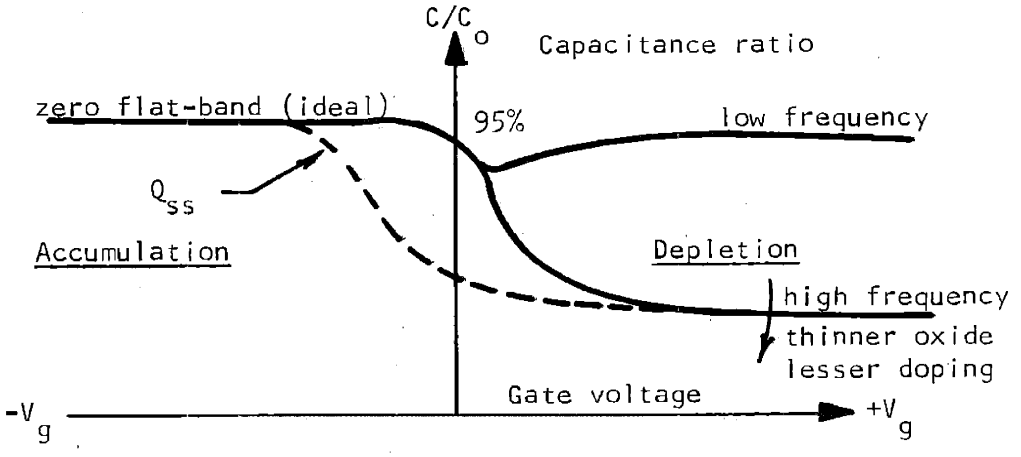
Trapped Surface Charge as a Function of Surface Potential

Figure A3



Pulse Field Effect to Determine Density of States

Figure A4



Capacitance-Voltage Characteristics

Figure A5

At equilibrium $dn_t/dt = 0$, and $g/r = \frac{n_c(N_t - n_t)}{(N_c - n_c)n_t}$. (A2)

Now

$$n_c = \frac{N_c}{\exp(E_c - E_f)/kT + 1} \tag{A3}$$

and

$$n_t = \frac{N_t}{\gamma\exp(E_t - E_f)/kT + 1} \tag{A4}$$

where γ = statistical factor. So,

$$g/r = \gamma\exp(E_t - E_c)/kT \tag{A5}$$

If we apply a pulse such that n_c goes to n_c' where $n_c >> n_c'$

then $$dn_t/dt \simeq -gN_c n_t \tag{A6}$$

and $$n_t = A\exp(-t/\tau) \quad \text{where} \quad \tau = 1/gN_c \tag{A7}$$

Now combining (A7) and (A2) we get

$$1/\tau = r\gamma N_c \exp(E_t - E_c)/kT \tag{A8}$$

If we define a capture cross section as $\sigma(T)$, then

$$r = \sigma(T)\, v_T \tag{A9}$$

where

$$v_T = (3kT/m^*)^{3/2}(1/\sqrt{6\pi}) \tag{A10}$$

Finally,

$$(\tau N_c v_T)^{-1} = \gamma\sigma(T)\exp(E_t - E_c)/kT \tag{A11}$$

where $\gamma\sigma(T)$ is the effective capture cross section and

$$N_c = 2(2\pi m^* kT/h^2)^{3/2} \tag{A12}$$

Since we directly measure τ, we plot $\ell n(\tau N_c v_T)$ vs $1/T$. The slope

of the line yields $E_c - E_t$ and the intercept is $1/\gamma\sigma(T)$.

Now the density of surface states N_t can be determined from the kinetic equation by making n_t suddenly small (voltage pulse goes to zero) as in Figure A4.

When the pulse goes off and $n_t >> n_t'$,

$$dn_c/dt \simeq -rn_cN_t = -\sigma(T)v_Tn_cN_t \qquad (A13)$$

or

$$n_c = B \exp[-t\sigma(T)v_TN_t], \qquad (A14)$$

we graphically measure $\tau = (\sigma v_T N_t)^{-1}$ and since we know $\sigma(T)$ and v_T, we can determine N_t. Typical parameters are: capture cross section for fast traps, 10^{-13} cm^2; for slow states, 10^{-17} cm^2; trap densities on the order of 10^{11} to 10^{12} cm^{-2} (8).

II. Capacitance-Voltage Characteristics

This technique provides a way to calculate:

1) the effective charge, Q_{ss}, at the surface of the semiconductor (directly);

2) the charge in the bulk of the insulator (Na^+) (indirectly);

3) the impurity level of the semiconductor (directly);

4) the insulator thickness (directly);

5) the surface state dynamics.

The features of the capacitance-voltage curve are seen in Figure A5(53).

In the MIS capacitance structure, if we assume no charge density in the oxide or semiconductor-oxide interface, than at accumulation conditions C = C oxide = $\varepsilon_o A/x_o$. At inversion, the capacitance is

Reduced to the series capacitance of the oxide and space charge layer:

$$1/C = x_o/\varepsilon_o A + x_d/\varepsilon_s A \qquad (A15)$$

where x_d = maximum depletion layer thickness = $(4\varepsilon_s\phi_{Fermi}/qN)^{1/2}$. And the depletion approximation[53] between accumulation and inversion is given by

$$C/C_{oxide} = [1 + 2\varepsilon_{ox}^2 V_g/(qN\varepsilon_s x_{ox}^2)]^{-1/2} \qquad (A16)$$

The frequency effects are explained in terms of surface state dynamics and the mechanisms of the space charge layer. According to Grove[54], we consider the effect when a positive voltage applied to an MIS structure is increased by a small amount. As the voltage is increased, more negative charge is induced in the silicon. For the p-type material, holes will be pulled out from the edge of the depletion region and its width will increase slightly. If electron-hole pairs can be generated quickly enough within the space charge layer, the generated holes will replace holes pulled out from the edge, and the generated electrons will be attracted to the surface to form an inversion layer. Therefore, at high frequencies, generation in the SCl is not fast enough to follow the signal change. Thus we measure a series oxide and depletion capacitance. At low frequencies, however, this inversion layer does form, and the measured capacitance is that of the oxide layer alone.

Shifts from the ideal conditions, i.e. zero flat band voltage (zero voltage - zero surface potential) are brought on by charges in the insulator, charges at the semiconductor surface, and the metal-

semiconductor work function, ϕ_{ms}. These effects cause the C-V curve to be shifted to the right or left by the flat band voltage, V_{fb}[8].

$$V_{fb} = \phi_{ms} - Q_{ss}/C_o - 1/C_o \int_0^{x_o} x/x_o \, \rho(x)dx \qquad (A17)$$

Appendix B

The Jacobian Matrix

In the derivation of the tunnel current, we had need to change the variables $dE_x dE_\perp$ to $dE dE_x$ [Equation (8)]. The Jacobian Matrix[55] gives the following relation.

$$dudz = dxdy \left| \begin{matrix} \frac{\partial x}{\partial u} & \frac{\partial y}{\partial z} \\ \frac{\partial x}{\partial u} & \frac{\partial x}{\partial z} \\ \frac{\partial y}{\partial u} & \frac{\partial y}{\partial z} \end{matrix} \right|^2 \tag{B1}$$

Let $u = E_\perp$, $z = E_x$, $x = u + z = E_\perp + E_x = E$ and $y = z = E_x$, then the value of the determinant is 1, and

$$dE_\perp dE_x = dE dE_x \tag{B2}$$

as desired.

Appendix C

Conduction Mechanisms in MIS Structures

1. Ionic conduction. Pertinent equations[56]:

Low field conditions, i.e. $E\ell << kT$,

$$J = nv \frac{Ee^2\ell^2}{kT} = J_o \frac{E\ell}{kT} \exp(-\phi/kT) \tag{C1}$$

High field conditions,

$$J = ne\ell v \exp(E\ell/2kT) = J_o \exp(-\phi/kT + E\ell/kT) \tag{C2}$$

where J = current density, E = electric field strength,

n = ionic carrier density, ℓ = distance between defect or impurity sites,

v = average ion velocity = $(kT)^3/mH^3\nu^2$ [exp(-ϕ/kT)]

where ν = vibrational frequency $\perp$ to jump and ϕ = barrier height.

2. Tunneling and internal field emmission. Pertinent equations:

As discussed in Chapter II, Section A, the transmission probability is

$$T(E) = \exp\{-2(2m/h^2)^{1/2} \int_a^b [V(x) - E]^{1/2} dx\} \tag{C3}$$

and the total current $J_x = j_{a\to b} - j_{b\to a}$ is

$$J_x = \frac{em}{2\pi^2 h^3} \int_0^\infty dE[f(E) - f(E + eV)] \int_0^E T(E_x) dE_x \tag{C4}$$

Now if we consider space chargeeffects[57] in conduction band of insulator, we model the effective bias V'(x) as

$$V'(x) = V(x) - (ne/2\varepsilon)(s - x_1)^2 \tag{C5}$$

where $x_1 = \phi_s/eV$, ϕ = metal-insulator work function, and s = insulator thickness.

The image force correction[57] on the insulator potential is

$$V'(x) = V(x) - \frac{e^2}{4\pi\varepsilon s[1 - (2x/s)^2]} \tag{C6}$$

where x is the distance from the center of the insulator to the charge.

If traps exist in the insulator the component of current due to the traps is[38]

$$J_T = AE^2 \exp(-B/EU^{3/2}) \tag{C7}$$

where A and B are constants and U = trap potential.

In general, the tunneling current may be written as

$$J = AE^n \exp(-B/E) \tag{C8}$$

where A and B are constants depending on the tunneling mode, and n lies between 1 and 3.

3. Schottky emission and Poole-Frenkel effect.

Schottky emission. Pertinent equations:

$$J = A^*(1 - r)T^2 \exp(-\phi/kT) \exp[E^{1/2}e^{3/2}/(2kT\varepsilon^{1/2})] \tag{C9}$$

where $A^* = 120$ amps/cm^2/deg = Dushman-Richardson constant, r = average reflection coefficient, and ϕ = work function of the metal.

There are many sources of error in this formulation in that:

a) the assumption that electrons do not interact is true for low currents only (use of Fermi statistics with no interaction terms);

b) the effective work function increases with space charge build-up near emitter, and decreases with increasing field strength;

c) ϕ, r, and A^* are temperature dependent due to thermal expansion;

d) r depends on the barrier shape

e) absorbed gases influence ϕ;

f) the emitting area is not equal to the actual surface area.

Poole-Frenkel effect. Pertinent equations[56].

$$\sigma = A \exp(-\phi/2kT) \exp[E^{1/2}e^{3/2}/(kT\varepsilon^{1/2})] \qquad (C10)$$

where A = constant and ϕ = trap potential in insulator.

4. Impurity conduction. Impurity conduction is masked if many electrons are in the conduction band, because of the low mobility of electrons at impurity levels (at normal temperatures). For this reason impurity conduction is seen in insulators rather than semiconductors or conductors.

Low concentration (less than $6 \times 10^{15}/cm^3$ in n-type Ge and 2×10^{17} in n-type Si). Under this condition there is small overlap between wave functions, i.e. localized electrons and field, and non-degenerate states. Random "hopping" occurs with no field, with current flow for applied fields. Phonons are absorbed or emitted to conserve energy in the hopping process. The mechanism for hopping or charge transfer is 1) tunneling through a potential barrier from occupied donor to an unoccupied one, and 2) electrons jumping over potential barrier to unoccupied state. The typical activation energy of the potential barrier in silicon is 5×10^{-3} eV.

a) Tunneling theory[58]

i) Probability of electron moving is a function of distance

between sites and it needs phonon assistance.

ii) Electron circuit analogy of three dimensional parallel chains.

iii) Resistivity given by

$$\ell n\rho(T) = f(N) + \varepsilon_1/kT \qquad (C11)$$

where f(N) = function of majority carrier concentration and ε_1 = activation energy, which is $\varepsilon_1 = (e^2/\varepsilon)(4\pi N_D/3)^{1/3}(1 - 1.35\chi^{1/3})$ and $\chi = N_A/N_D$.

b) Hopping theory[59]

More useful at high end of temperature range and at low applied voltages of impurity conduction. The expression for resistivity is

$$\ell n\ \rho(T) = f'(N) + \varepsilon_2/kT \qquad (C12)$$

where ε_2 = activation energy = $\varepsilon_a - 3e^2/\varepsilon a$, and ε_a = energy of impurity centers, and a = distance between centers.

An interesting sidelight is that impurities form a sub-lattice in the host lattice. A relationship[59], $1/a = GN^{1/3}$, where N = impurity concentration and G = .89 for fcc and hcp lattice, .92 for bcc lattice, 1.00 for sc, and 1.15 for the diamond lattice. Thus ε_2 is proportional to $N^{1/3}$, and the slope gives G which determines the impurity sub-lattice.

High concentration. Mott theory[60] states that the transition from a non-metallic to metallic state must occur for any array of atoms as the distance between them is decreased. The transition (from low

to high conductance) is sharp for ordered arrays of atoms, and less sharp for random arrays. At this transition, the activation energy for hopping goes to zero, thus the high conductance. The effective distance between atoms is decreased by increasing impurity concentration, and above a critical transition concentration, the material will appear metallic and the conductivity will be essentially independent of temperature.

ψ is defined as the measure of impurity concentration, and $\psi = (3/4\pi N)^{1/3}/a_o$ where a_o is the Bohr radius of the impurity. The material will be metallic for ψ less than 3, and non-metallic for ψ greater than 3. In the metallic region, $\sigma = 7 \times 10^3 AN^{1/3}$ mhos, where A is the number of interatomic distances in one mean free path, and N is the number of carriers per cubic angstrom.

5. Ohmic conduction. This is the familiar type of conduction in metals and semiconductors, which has a negligible component in insulators. Because of the large forbidden gap in an insulator, very few conduction electrons exist at normal temperatures.

$$J = AE \exp(-E_g/kT) \tag{C13}$$

where E_g is the energy gap of the insulator.

6. Space charge limited current. Pertinent equations:

For the case of one carrier and no traps,

$$J = \sigma E - De\, \partial n/\partial x \tag{C14}$$

Now
$$\partial E/\partial x = \rho/\varepsilon = ne/\varepsilon \tag{C15}$$

and
$$D/\mu = kT/q \tag{C16}$$

so,

$$J = \varepsilon\mu(E\ \partial E/\partial x - \frac{kT}{e}\ \partial^2 E/\partial x^2) \tag{C17}$$

If we neglect the diffusion term,

$$J = \frac{-kT}{e}\ \varepsilon\mu\ \partial^2 E/\partial x^2 \tag{C18}$$

and by integration we get

$$J = 9/8\ \frac{\varepsilon\mu v^2}{[(s + x_o)^{3/2} - x_o^{3/2}]^2} \tag{C19}$$

Now s = actual insulator thickness, while x_o is the place where ∇v is zero. If $x_o << s$,

$$J = 9/8\ \varepsilon\mu v^2/s^3 \quad \text{(Mott and Gurney Law)} \tag{C20}$$

if $x_o \simeq s$ analytical solutions are not available.

Appendix D

Network Equations for Bridge Circuit Used in Tunnel Measurements

Because of phase measurement problems, i.e. the large 90° out of phase displacement current, we must be sure that the test apparatus causes no additional phase effects. We can calculate the bridge response by modeling the tunnel device as a parallel RC network (R_d and C_d). and find the transfer function H(jw), of Figure 16.

$$H(jw) = V_{out}/V_{source} \tag{D1}$$

where V_{out} = voltage across the device.

$$H(jw) = \frac{R_d||R_v||C_d}{R_3+R_d||R_v||C_d} = \frac{1}{R_3/R_v+R_3/R_d+R_3C_djw+1} \tag{D2}$$

Now R_v = 1 megΩ and $R_3 \simeq 1/33$ megΩ at bridge null, so

$$H(jw) = \frac{33}{10^6(1/R_d+C_djw)+34} \tag{D3}$$

and

$$\text{Tan } \theta = \frac{-C_dw10^6}{34 + 10^6/R_d} \tag{D4}$$

Now if at worst case $C_d \simeq 10^{-11}$ f, $w \simeq 6 \times 10^3$/sec, and $R_d >> 10^6$, then tan $\theta_{max} \simeq -1.5 \times 10^{-3}$, and since for small angles tan $\theta \simeq \theta$,

$$\theta \simeq 1.5 \times 10^{-3} \text{ degrees} \tag{D5}$$

Thus the phase shift introduced by the bridge is well below the detectable limits of the lock-in amplifier (10^{-1} degrees).

Appendix E

Calculation of Tunnel Insulator Thickness From Capacitance Measurements

The tunnel device geometry is shown in Figure 13, and the total capacitance of the structure results from parallel contributions of the thick oxide contact area and the thin oxide tunnel area.

$$C_{total} = \varepsilon(A_1/d_1 + A_2/d_2) \tag{E1}$$

where A_1 = contact area = 9.59×10^{11} A^2

A_2 = tunnel area = 2.03×10^{11} A^2

d_1 = thick oxide depth = 5×10^3 A

ε = dielectric constant of SiO_2 = 8.85×10^{-10} pf/A.

Solving for d_2, the tunnel oxide thickness, we find

$$d_2 = \frac{A_2\varepsilon}{C_{total} - A_1\varepsilon/d_1} = \frac{6.99 \times 10^2}{C - .66} \tag{E2}$$

for C in pf and d_2 in A.

For C = 10 pf, $d_2 \simeq 75$ A.

Appendix F

Experimental Data on Tunnel Test Devices

Data on all test devices not specifically alluded to in the text are included here for completeness.

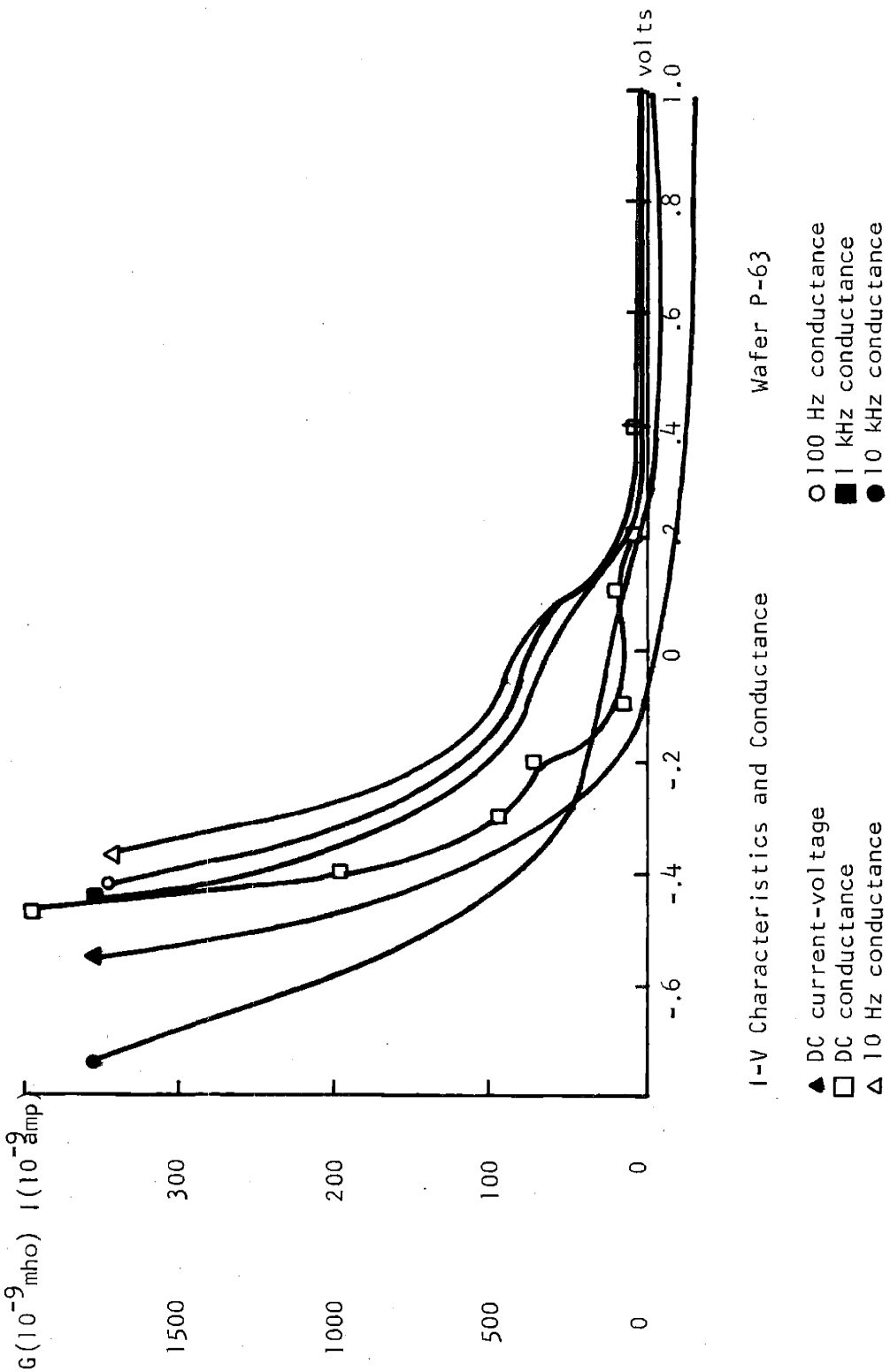
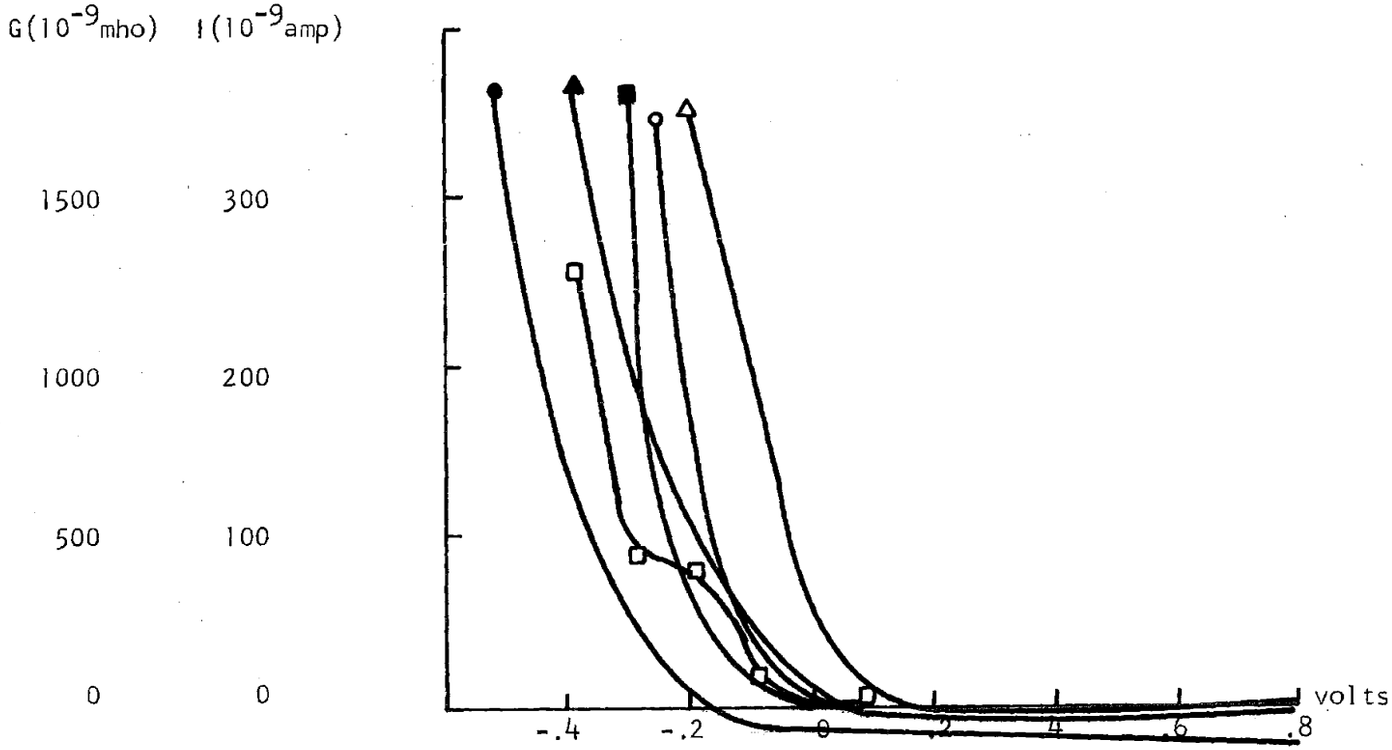

G(10^{-9}mho) I(10^{-9}amp)
1500
1000
500
0
300
200
100
0
-.6
-.4
-.2
0
.2
.4
.6
.8
1.0
volts
I-V Characteristics and Conductance
Wafer P-63
◆ DC current-voltage
□ DC conductance
△ 10 Hz conductance
○ 100 Hz conductance
■ 1 kHz conductance
● 10 kHz conductance

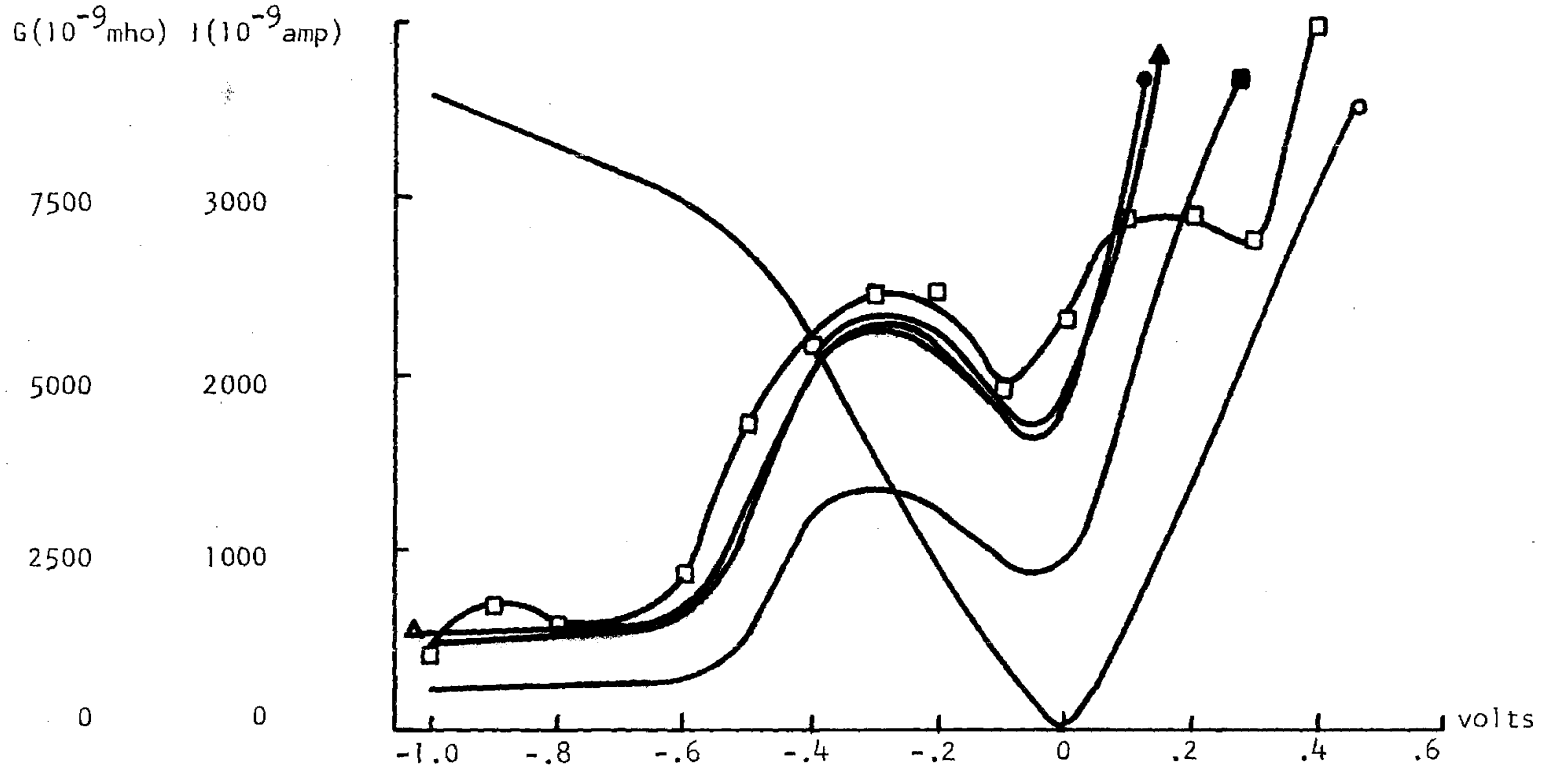
Figure F1



I-V Characteristics and Conductance Wafer P-73

● DC current-voltage
□ DC conductance
■ 10 Hz conductance
○ 100 Hz conductance
△ 1 kHz conductance
▲ 10 kHz conductance

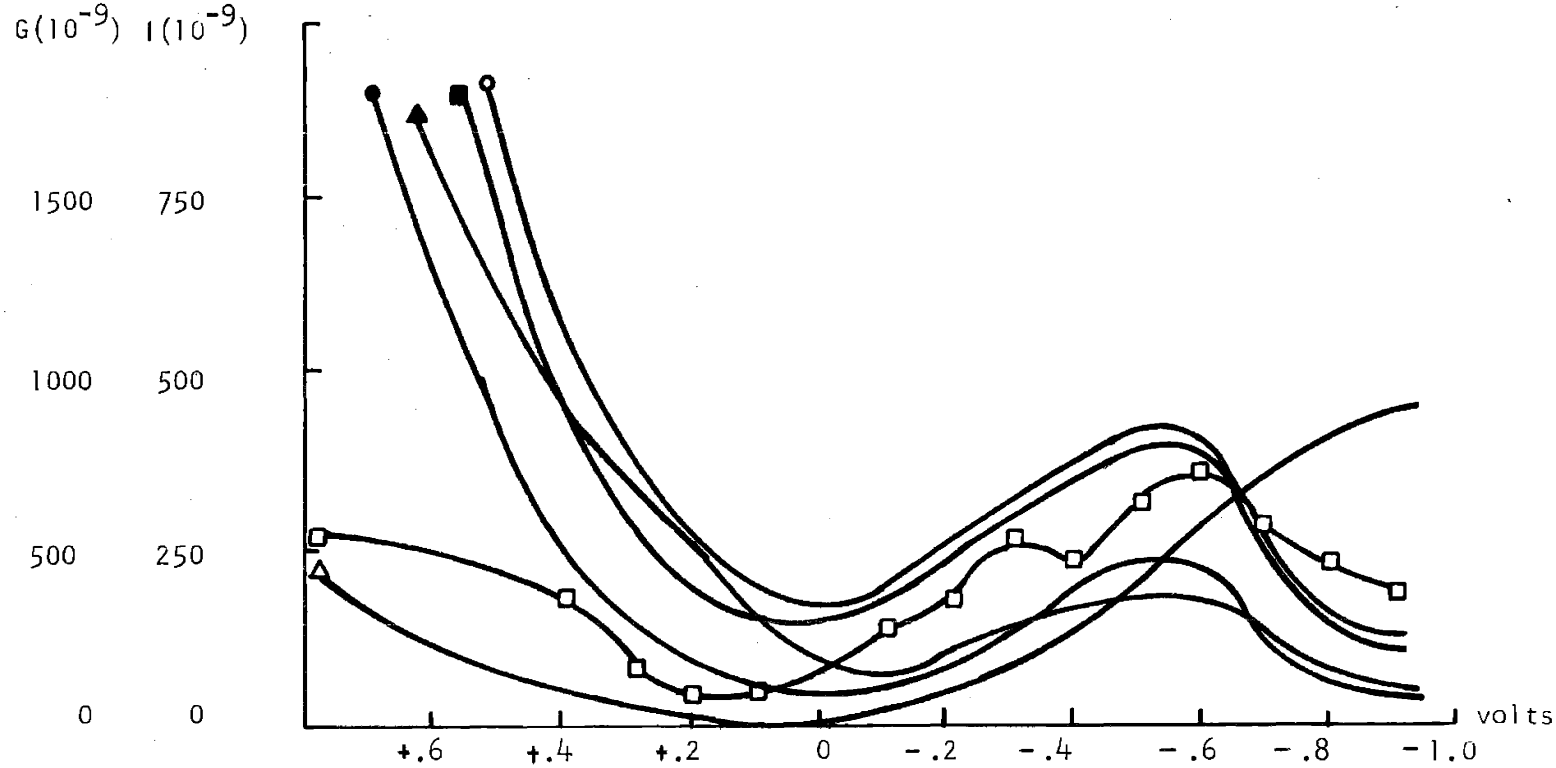
Figure F2



I-V Characteristics and Conductance — Wafer N-83

○ DC current-voltage
□ DC conductance
● 10 Hz conductance
△ 100 Hz conductance
▲ 1 kHz conductance
■ 10 kHz conductance

Figure F3

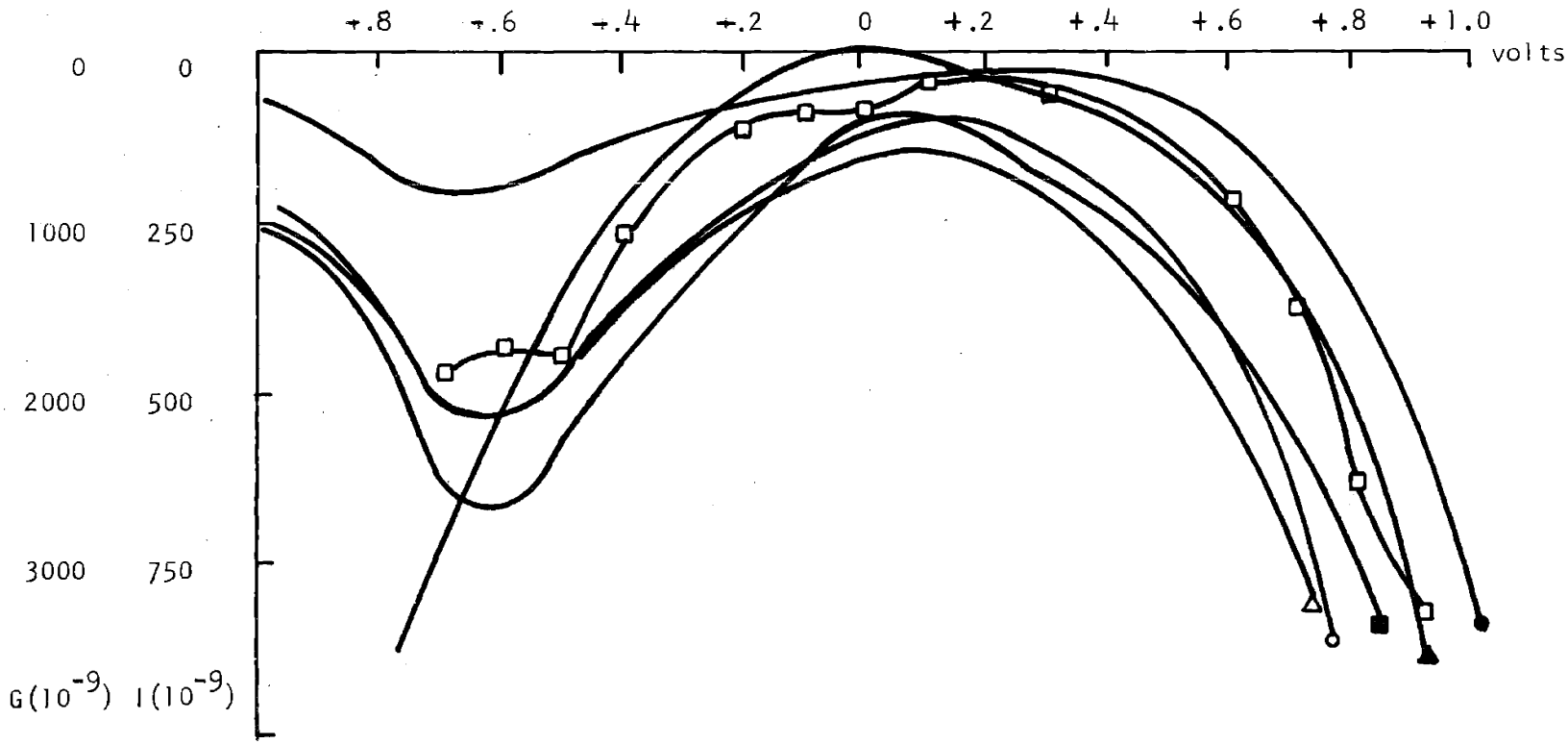


I-V Characteristics and Conductance

Wafer N-124

△ DC current-voltage
□ DC conductance
▲ 10 Hz conductance
○ 100 Hz conductance
■ 1 kHz conductance
● 10 kHz conductance

Figure F4

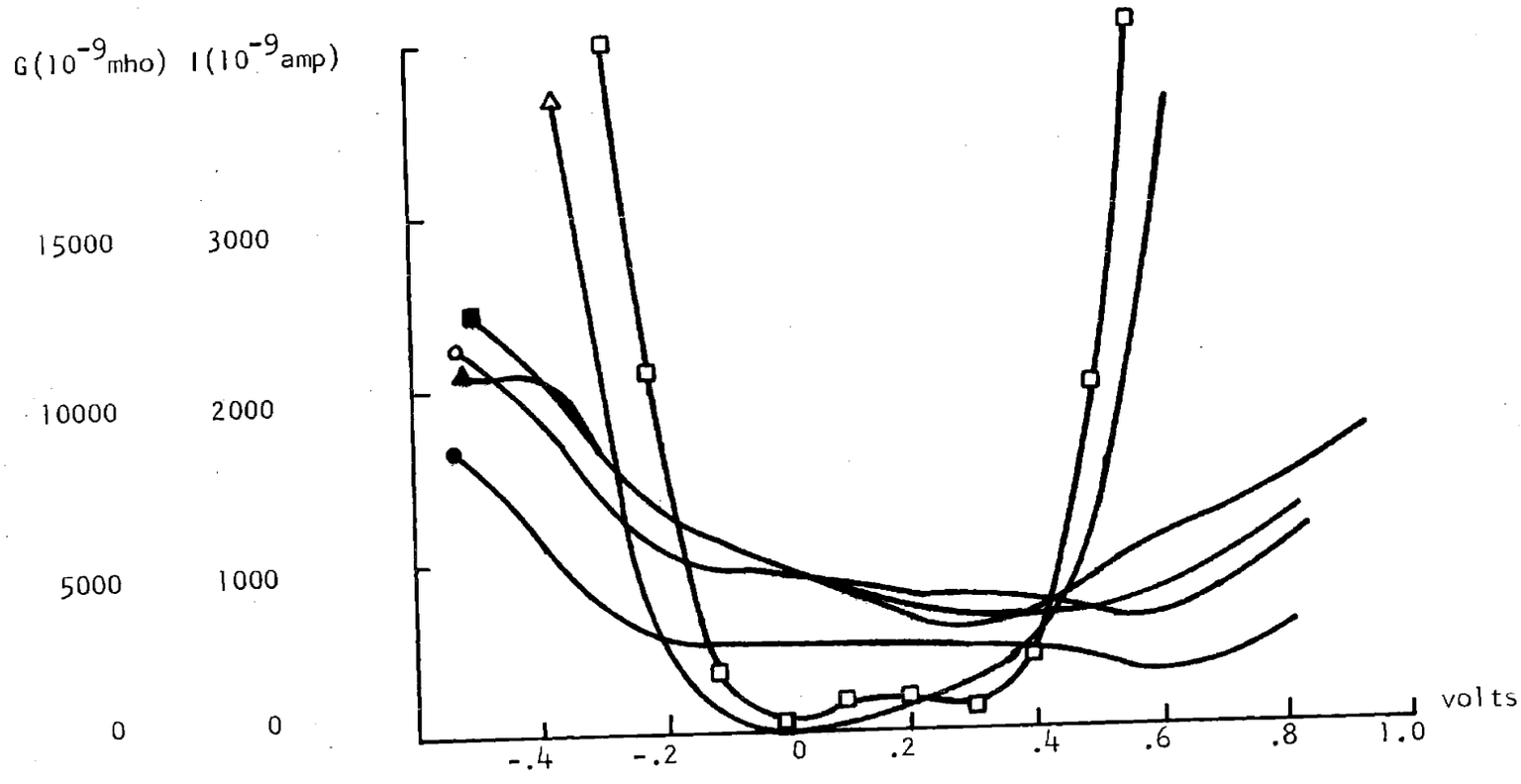


I-V Characteristics and Conductance

Wafer N-134

▲ DC current-voltage
□ DC conductance
■ 10 Hz conductance
△ 100 Hz conductance
○ 1 kHz conductance
● 10 kHz conductance

Figure F5



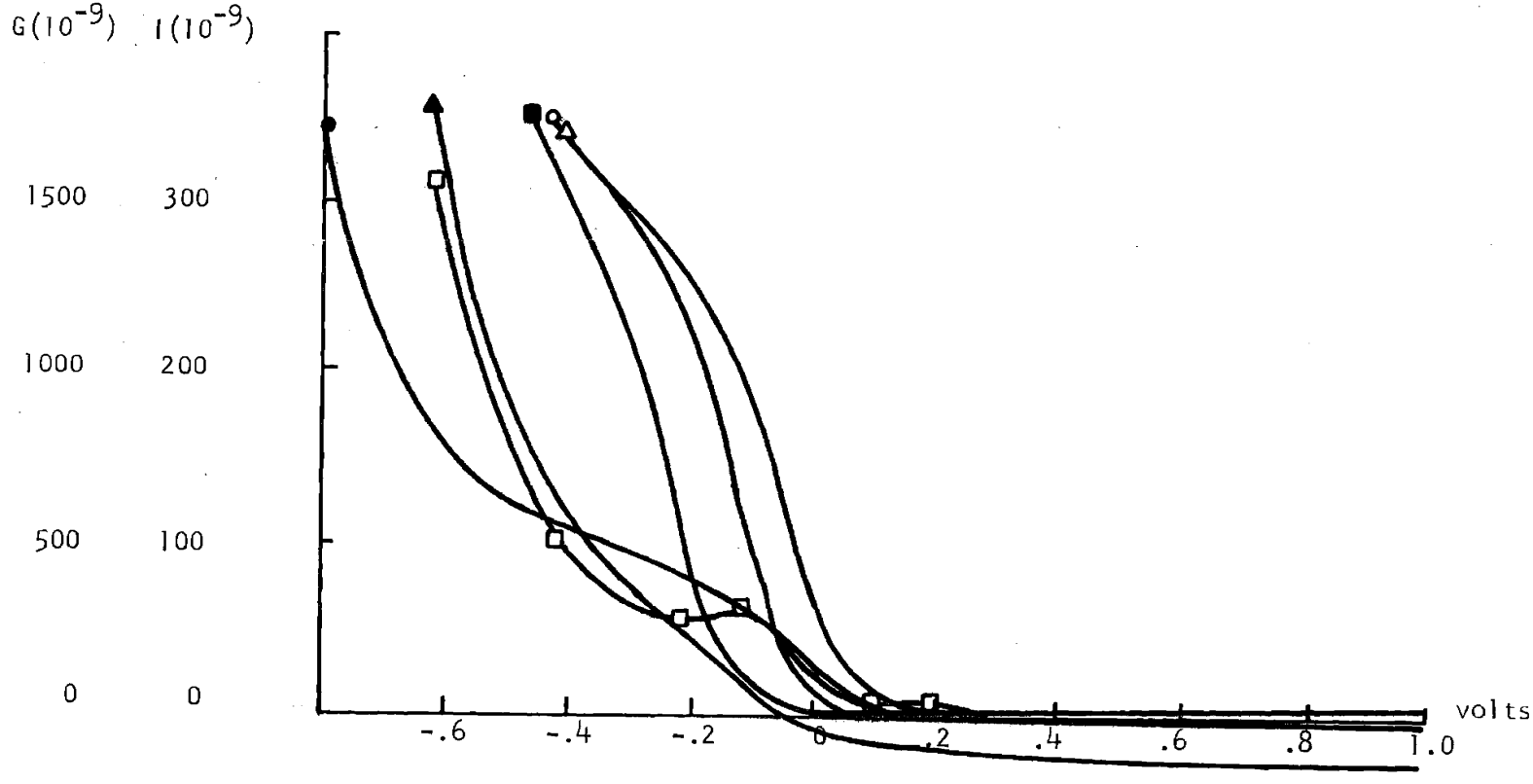
I-V Characteristics and Conductance

Wafer N-144

△ DC current-voltage
□ DC conductance
▲ 10 Hz conductance

■ 100 Hz conductance
○ 1 kHz conductance
● 10 kHz conductance

Figure F6

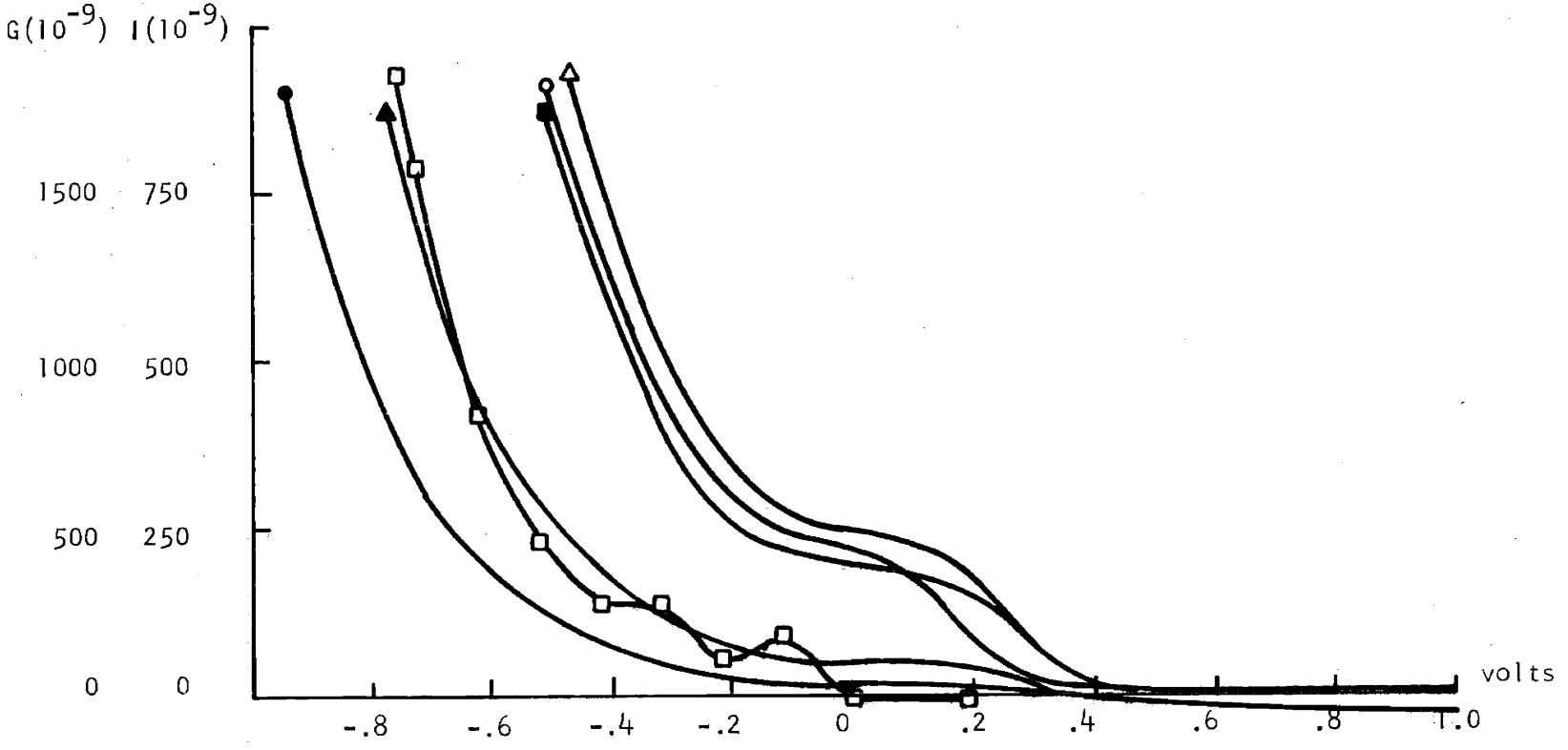


I-V Characteristics and Conductance

Wafer P-154

▲ DC current-voltage
□ DC conductance
■ 10 Hz conductance
△ 100 Hz conductance
○ 1 kHz conductance
● 10 kHz conductance

Figure F7

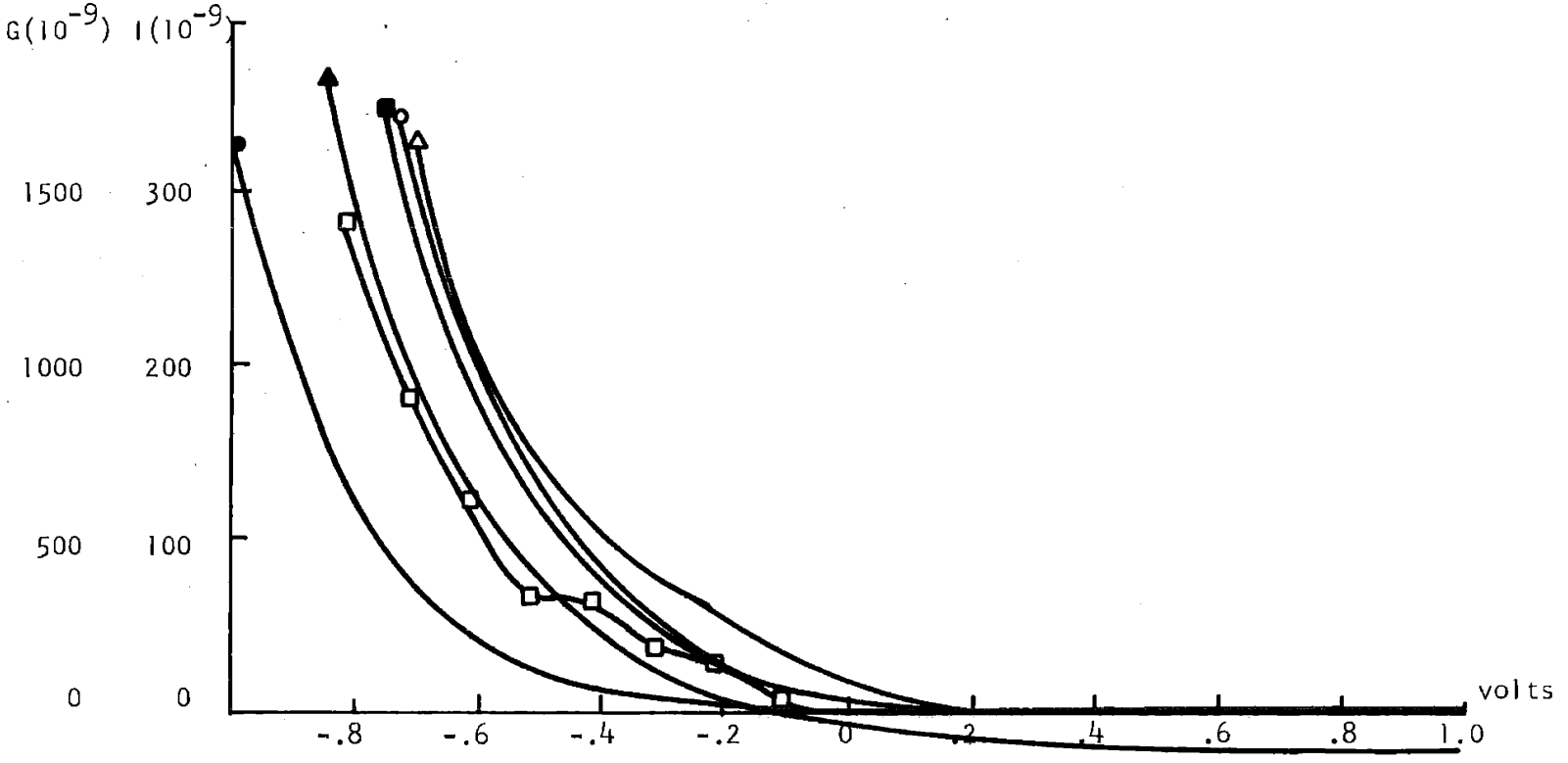


I-V Characteristics and Conductance

Wafer P-174

● DC current-voltage
□ DC conductance
○ 10 Hz conductance
△ 100 Hz conductance
■ 1 kHz conductance
▲ 10 kHz conductance

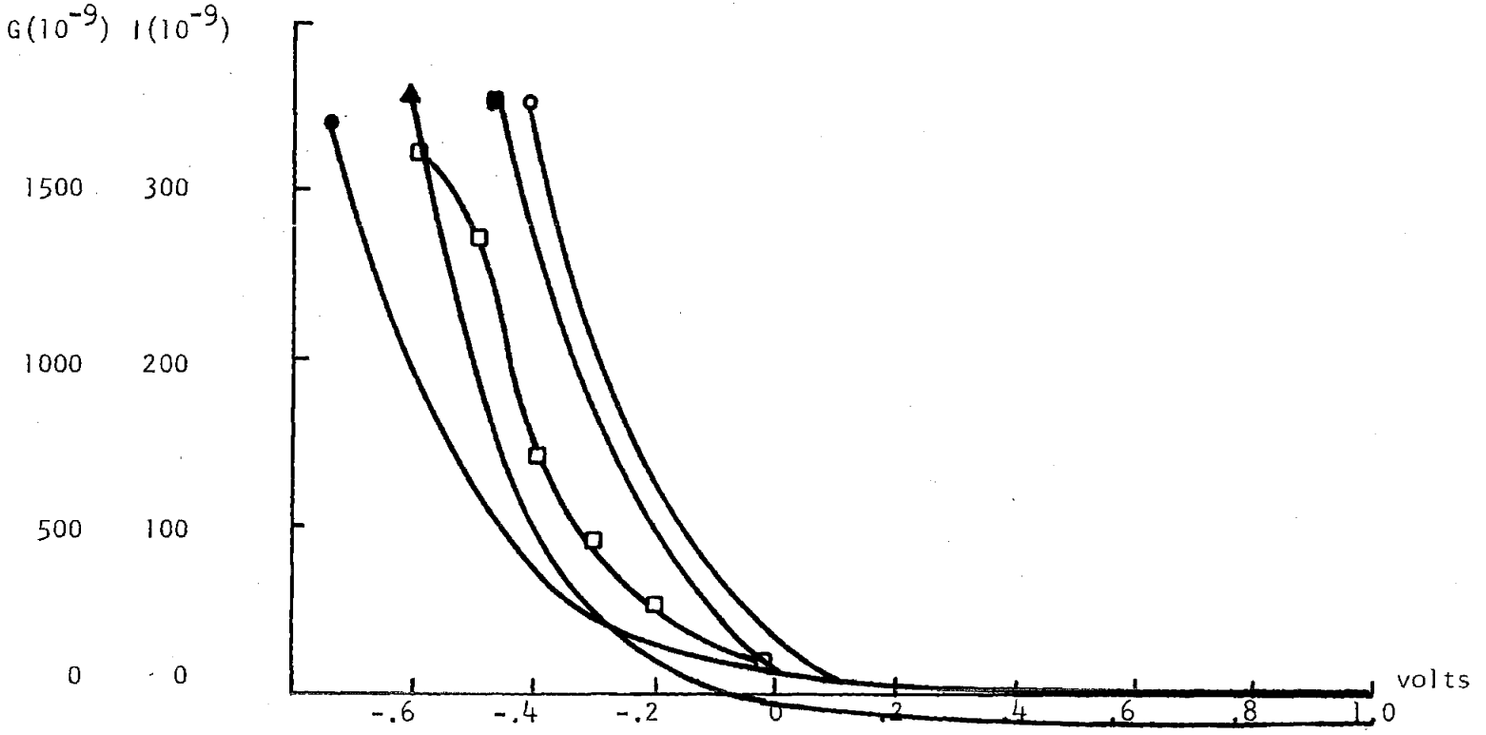
Figure F8



I-V Characteristics and Conductance Wafer P-184

▲ DC current-voltage
□ DC conductance
○ 10 Hz conductance
△ 100 Hz conductance
■ 1 kHz conductance
● 10 kHz conductance

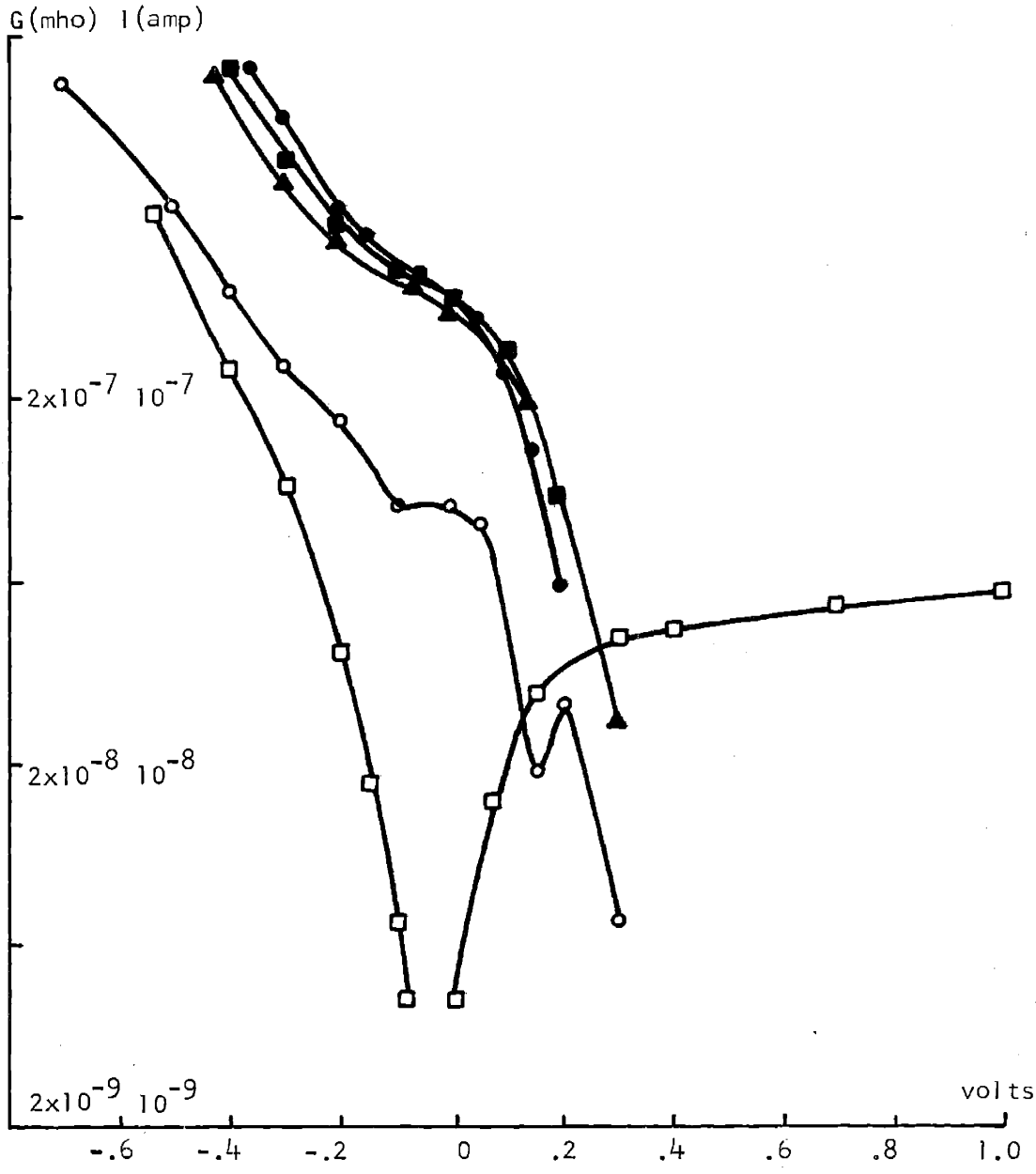
Figure F9



I-V Characteristics and Conductance Wafer P-194

▲ DC current-voltage
□ DC conductance
■ 10 Hz conductance
○ 100 Hz conductance
○ 1 kHz conductance
● 10 kHz conductance

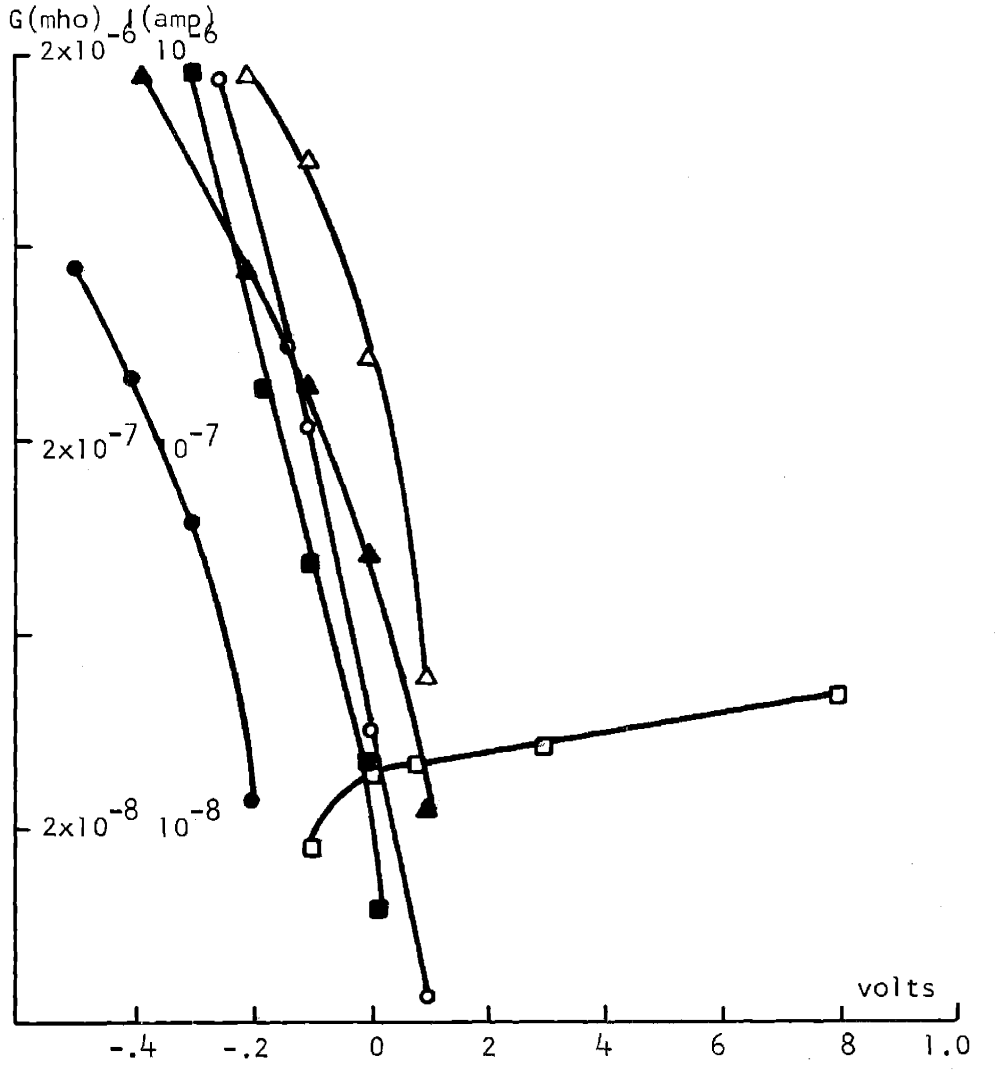
Figure F10



Log I-V Characteristics and Log Conductance Wafer P-63

□ DC current-voltage
● 10 Hz conductance
■ 100 Hz conductance
▲ 1 kHz conductance
○ 10 kHz conductance

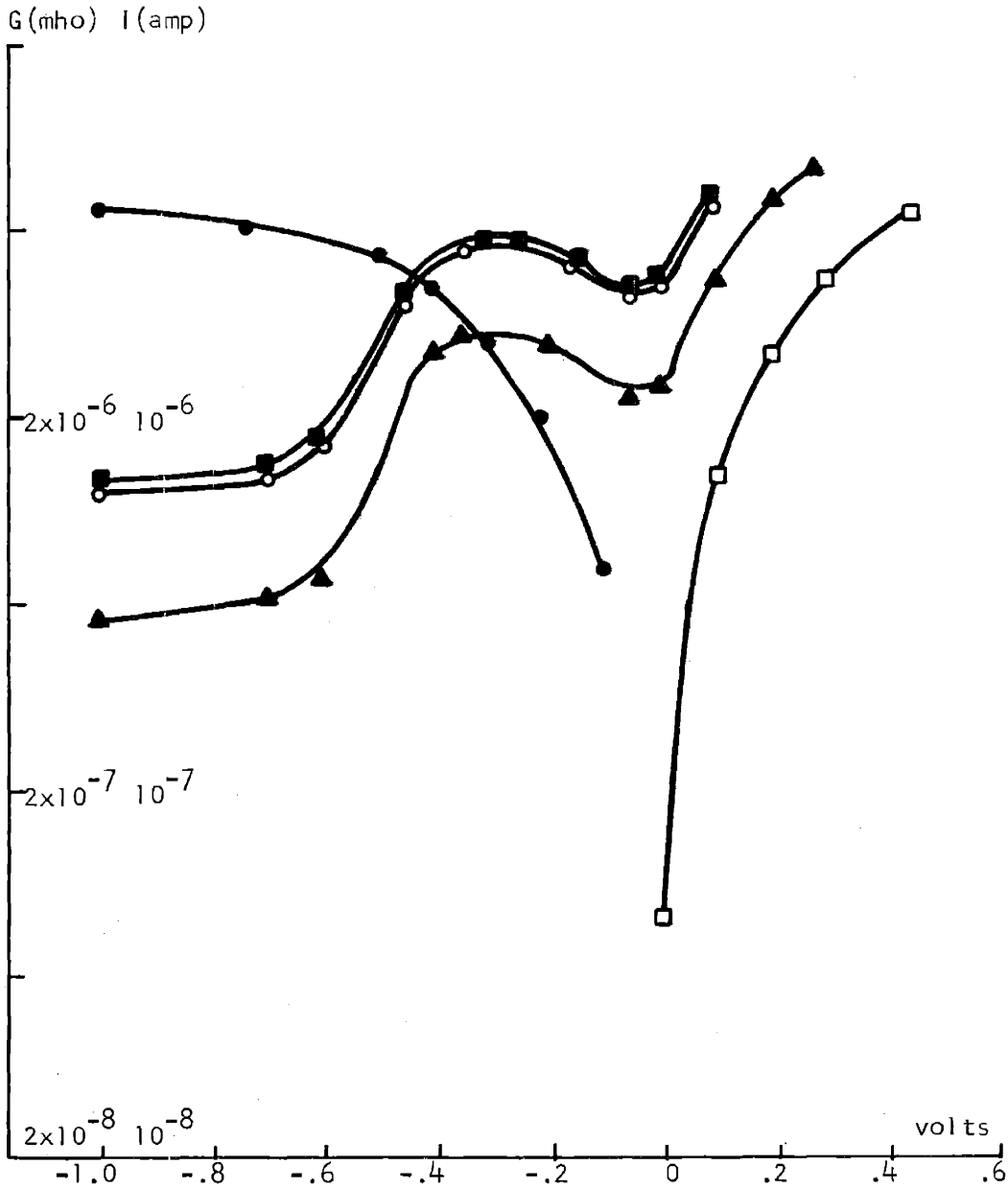
Figure F11



Log I-V Characteristics and Log Conductance Wafer P-73

● □ DC current-voltage
■ 10 Hz conductance
○ 100 Hz conductance
△ 1 kHz conductance
▲ 10 kHz conductance

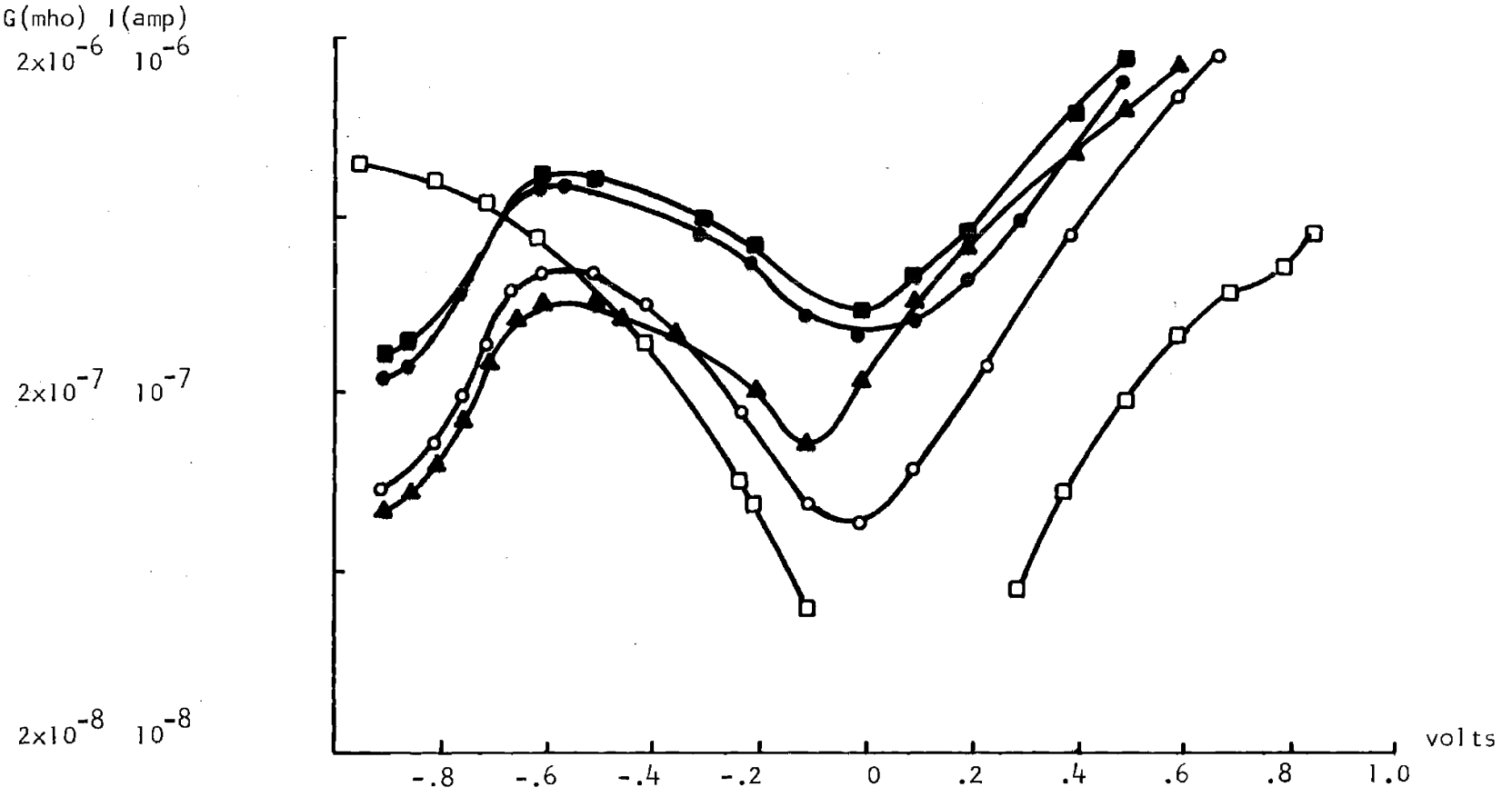
Figure F12



Log I-V Characteristics and Log Conductance Wafer N-83

● □ DC current-voltage
■ 10 Hz conductance
■ 100 kHz conductance
○ 1 kHz conductance
△ 10 kHz conductance

Figure F13



Log I-V Characteristics and Log Conductance Wafer N-124

□ DC current-voltage
▲ 10 Hz conductance
■ 100 Hz conductance
● 1 kHz conductance
○ 10 kHz conductance

Figure F14

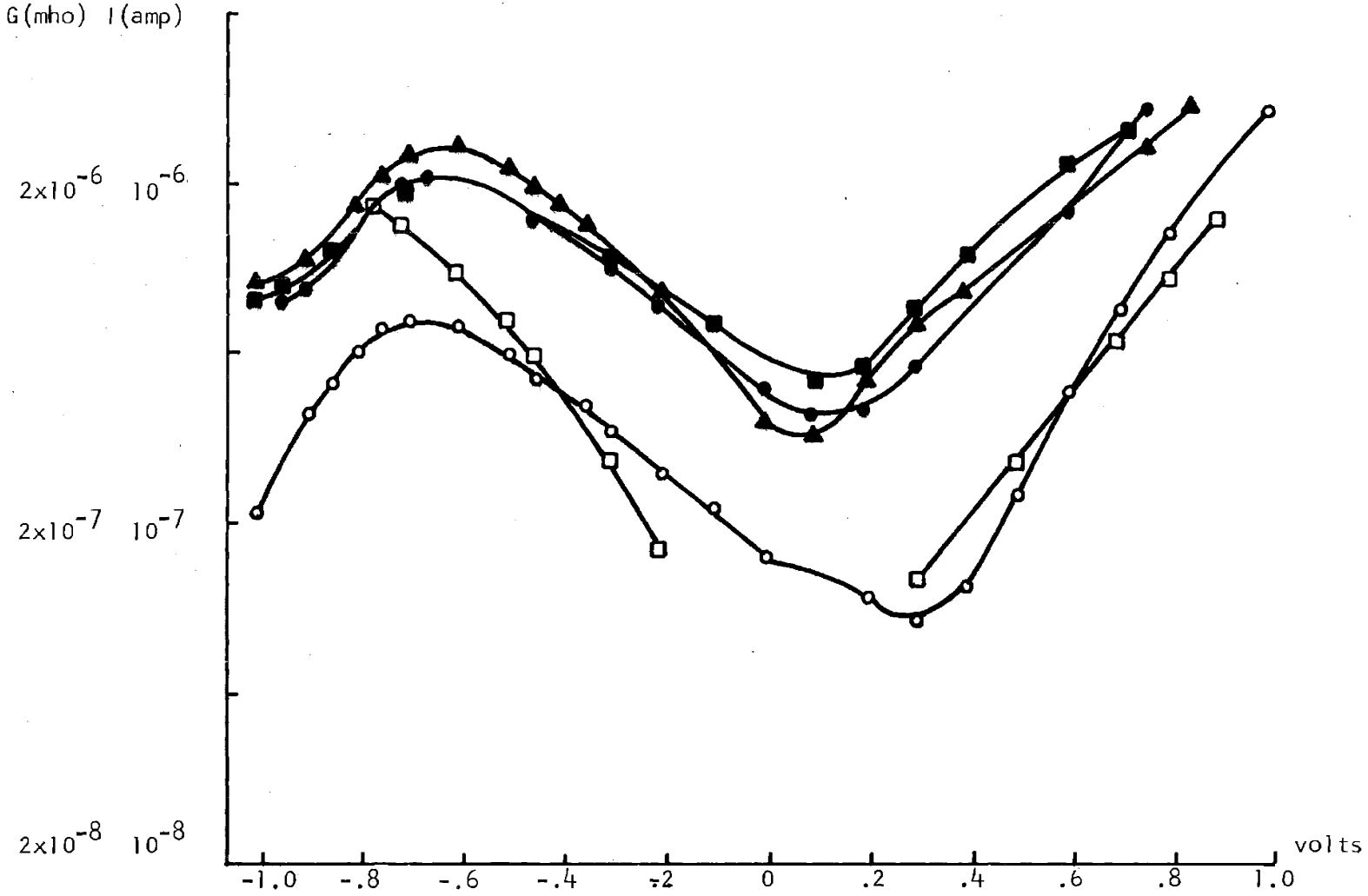
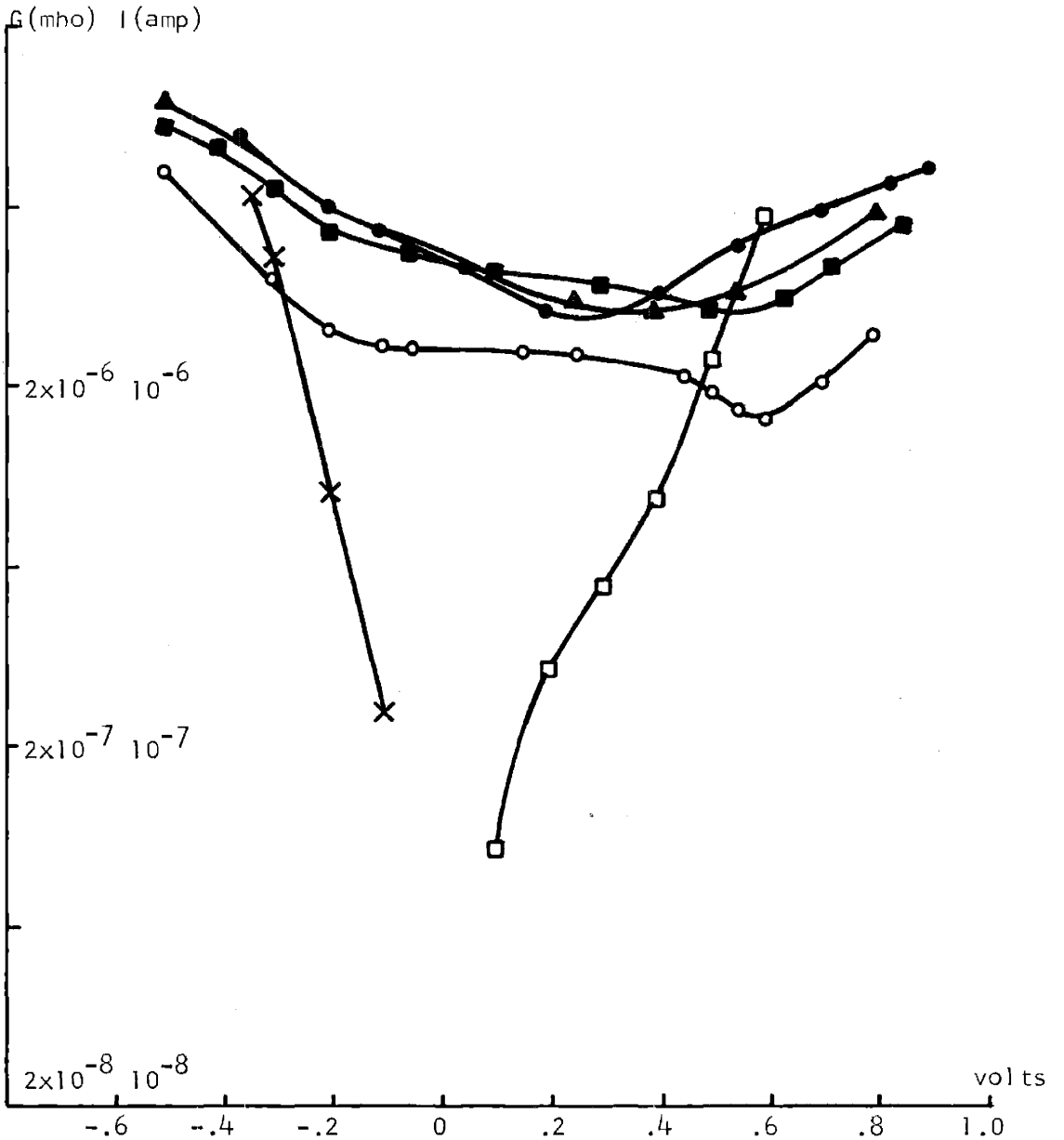


Figure F15

Log I-V Characteristics and Log Conductance Wafer N-134

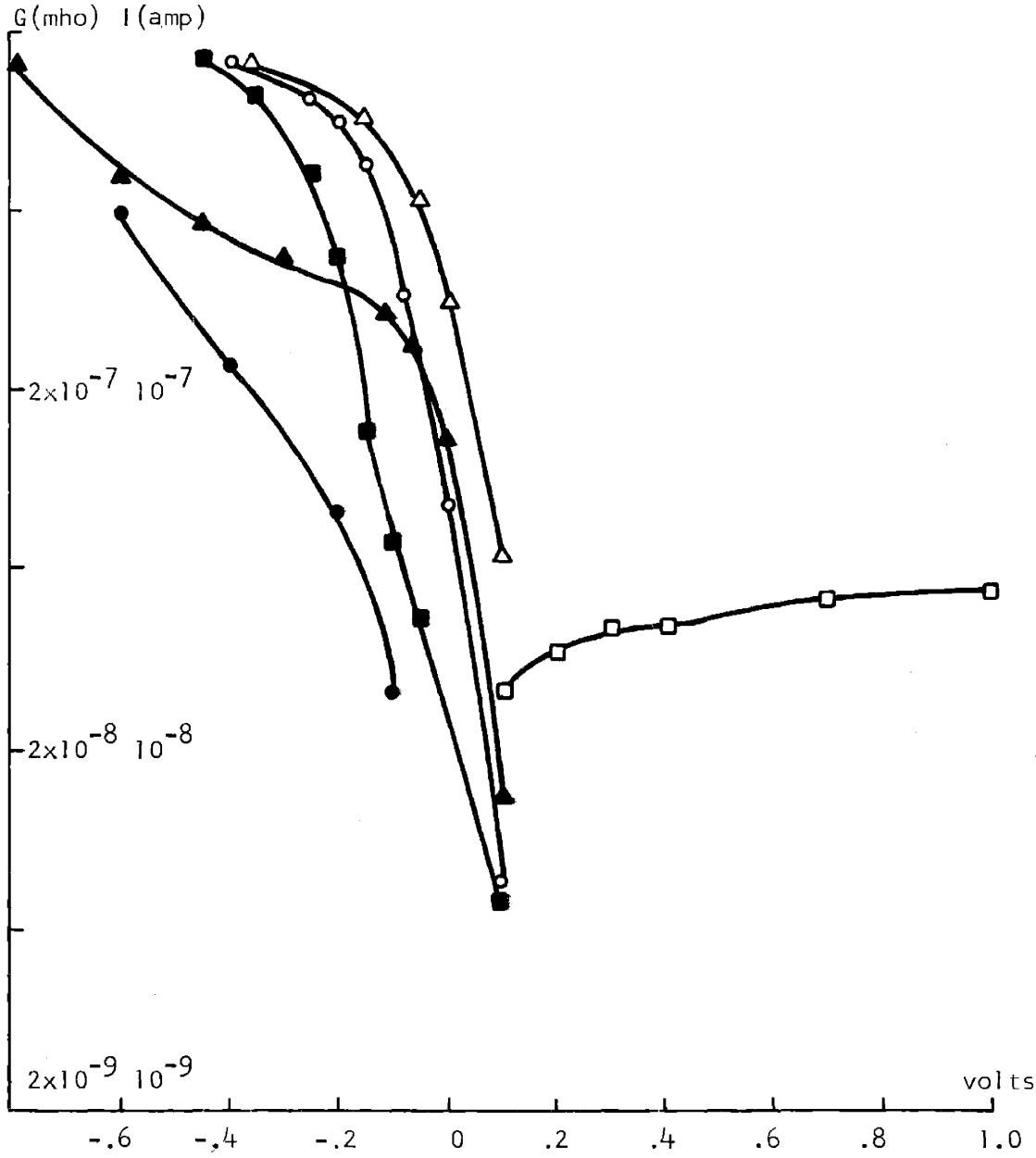
□ DC current-voltage
▲ 10 Hz conductance
■ 100 Hz conductance
● 1 kHz conductance
○ 10 kHz conductance



Log I-V Characteristics and Log Conductance Wafer N-144

□ ✕DC current-voltage
● 10 Hz conductance
▲ 100 Hz conductance
■ 1 kHz conductance
○ 10 kHz conductance

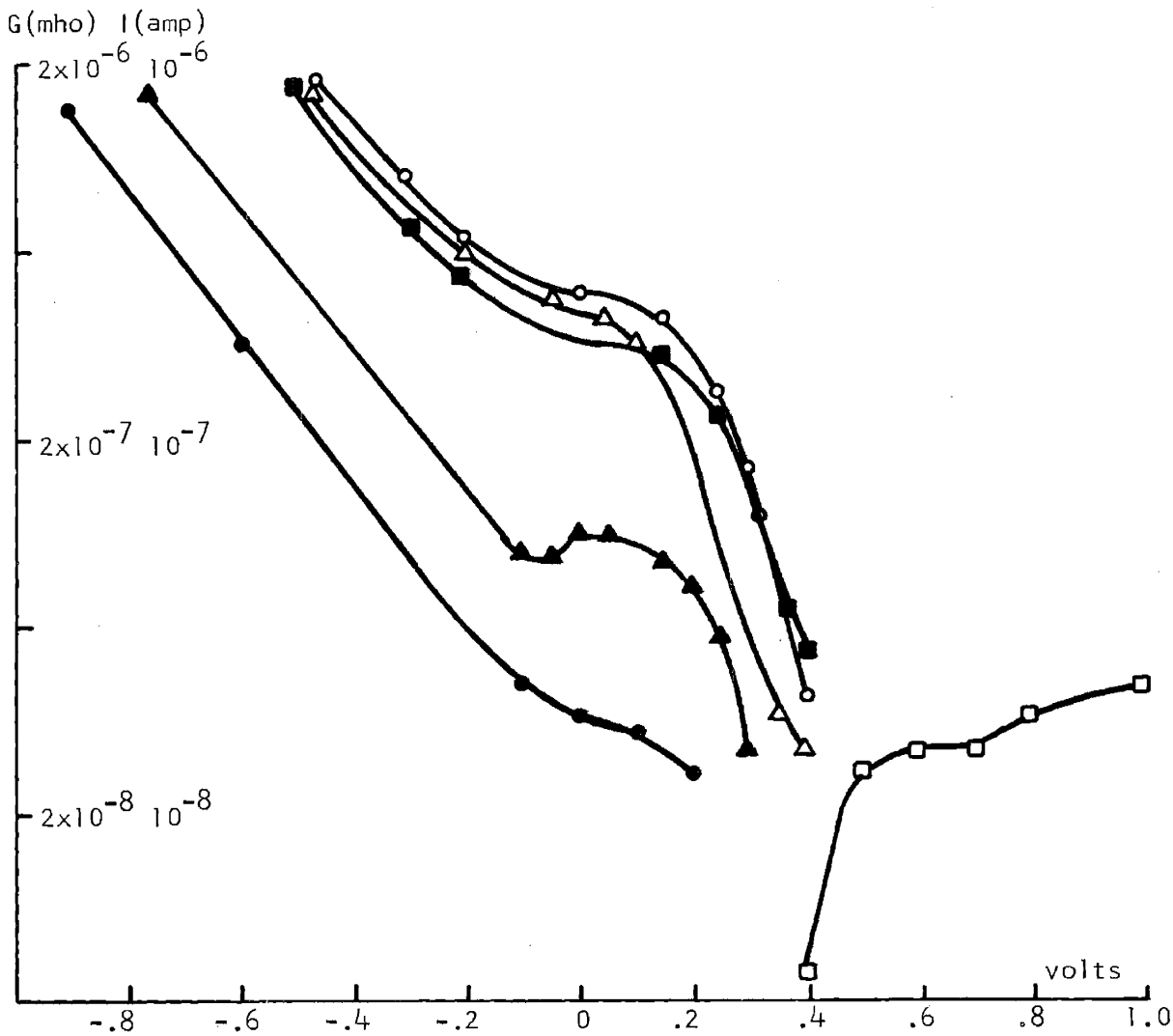
Figure F16



Log I-V Characteristics and Log Conductance Wafer P-154

□ ● DC current-voltage
■ 10 Hz conductance
○ 100 Hz conductance
△ 1 kHz conductance
▲ 10 kHz conductance

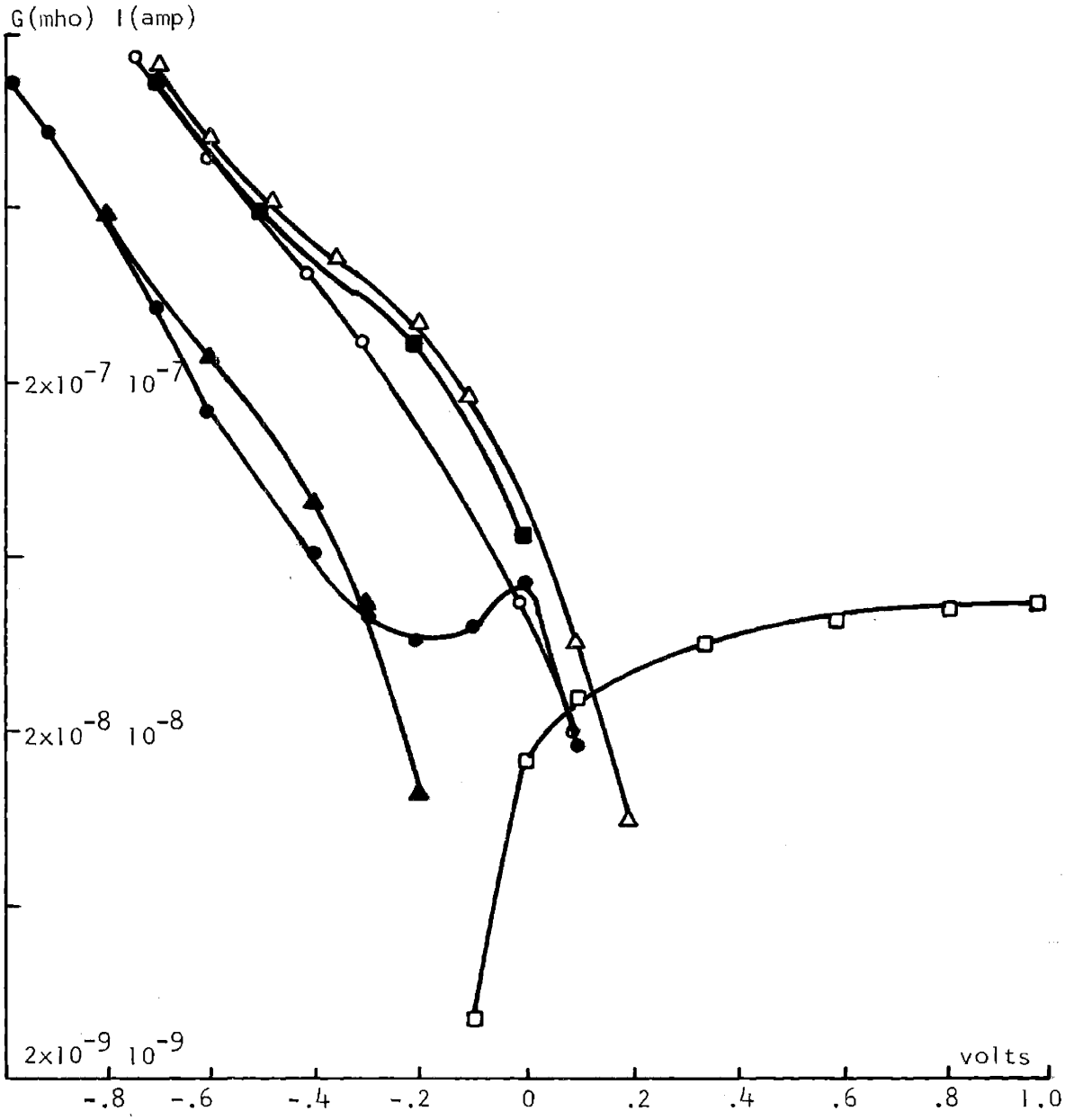
Figure F17



Log I-V Characteristics and Log Conductance Wafer P-174

□ ● DC current-voltage
△ 10 Hz conductance
○ 100 Hz conductance
■ 1 kHz conductance
▲ 10 kHz conductance

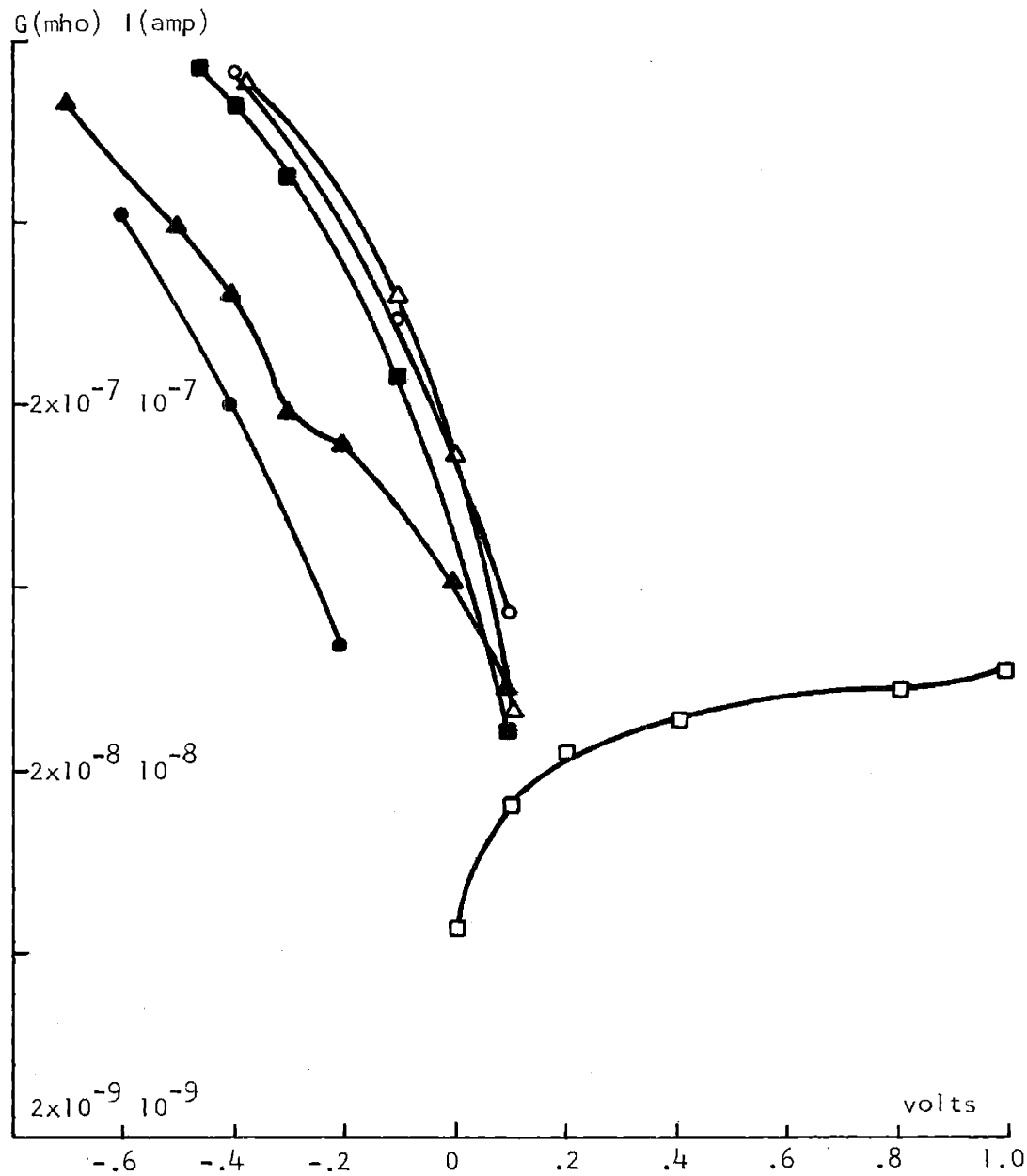
Figure F18



Log I-V Characteristics and Log Conductance Wafer P-184

□ ▲ DC current-voltage
○ 10 Hz conductance
△ 100 Hz conductance
■ 1 kHz conductance
● 10 kHz conductance

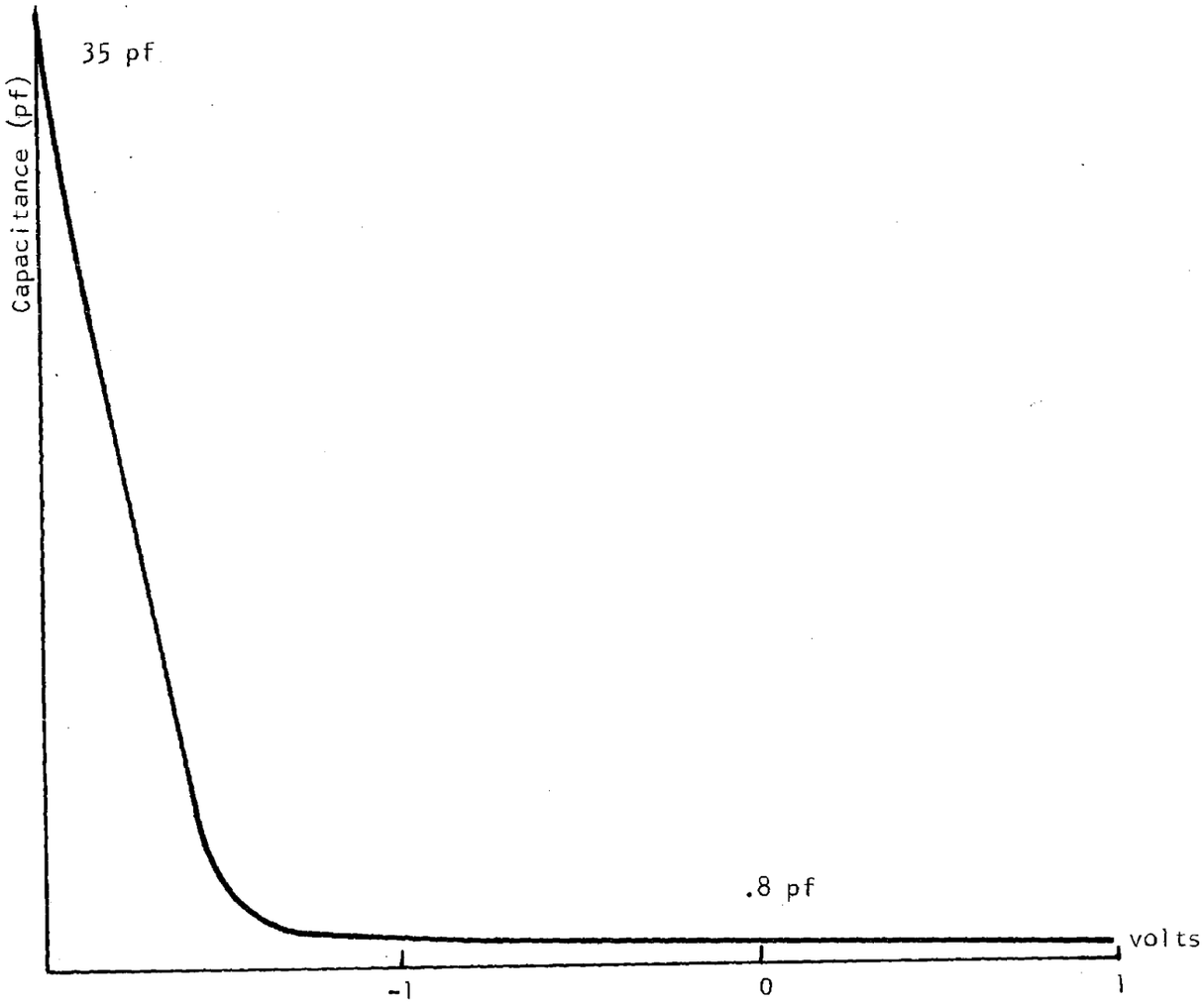
Figure F19



Log I-V Characteristics and Log Conductance Wafer P-194

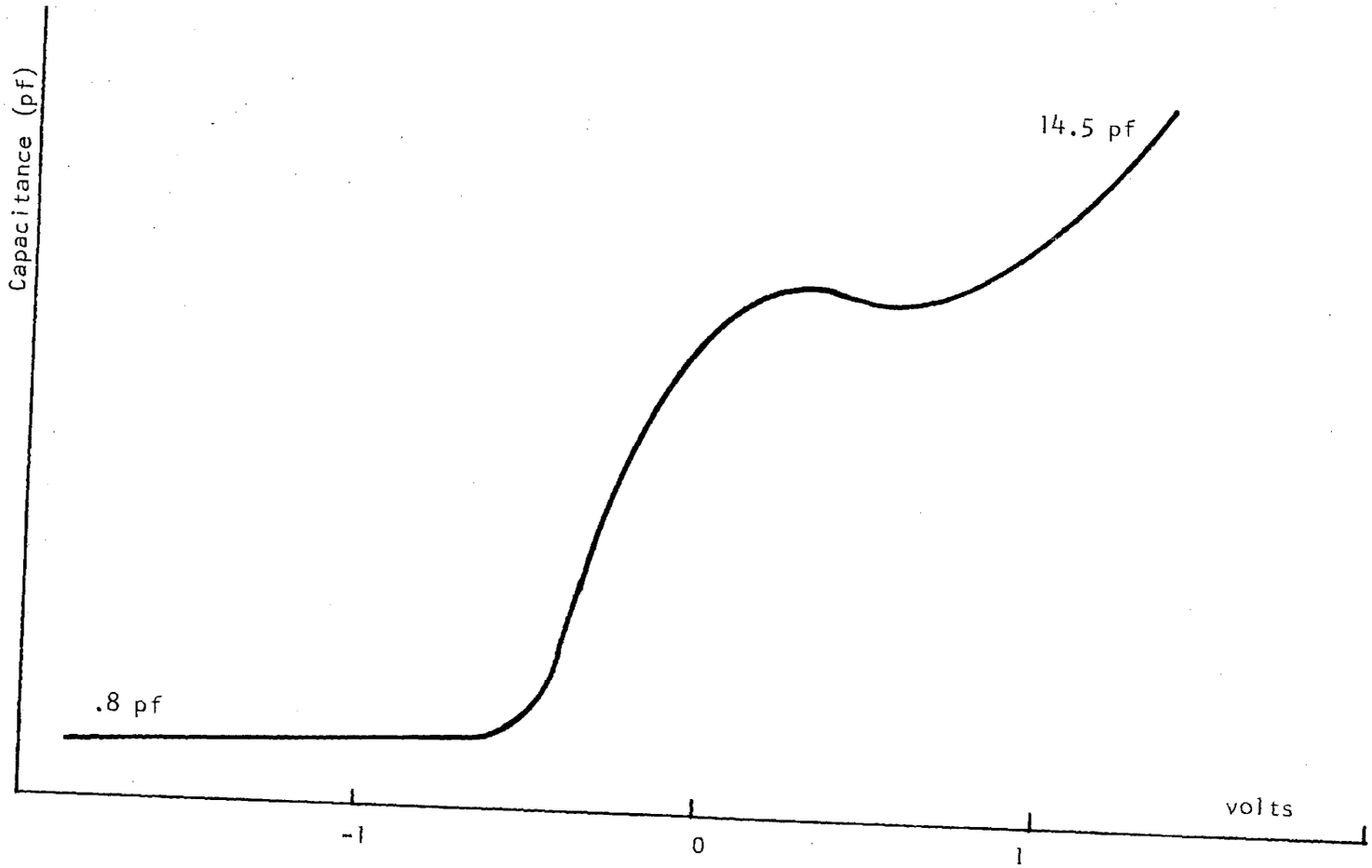
□● DC current-voltage
■ 10 Hz conductance
○ 100 Hz conductance
△ 1 kHz conductance
▲ 10 kHz conductance

Figure F20



Capacitance-Voltage Measurements Wafer P-73

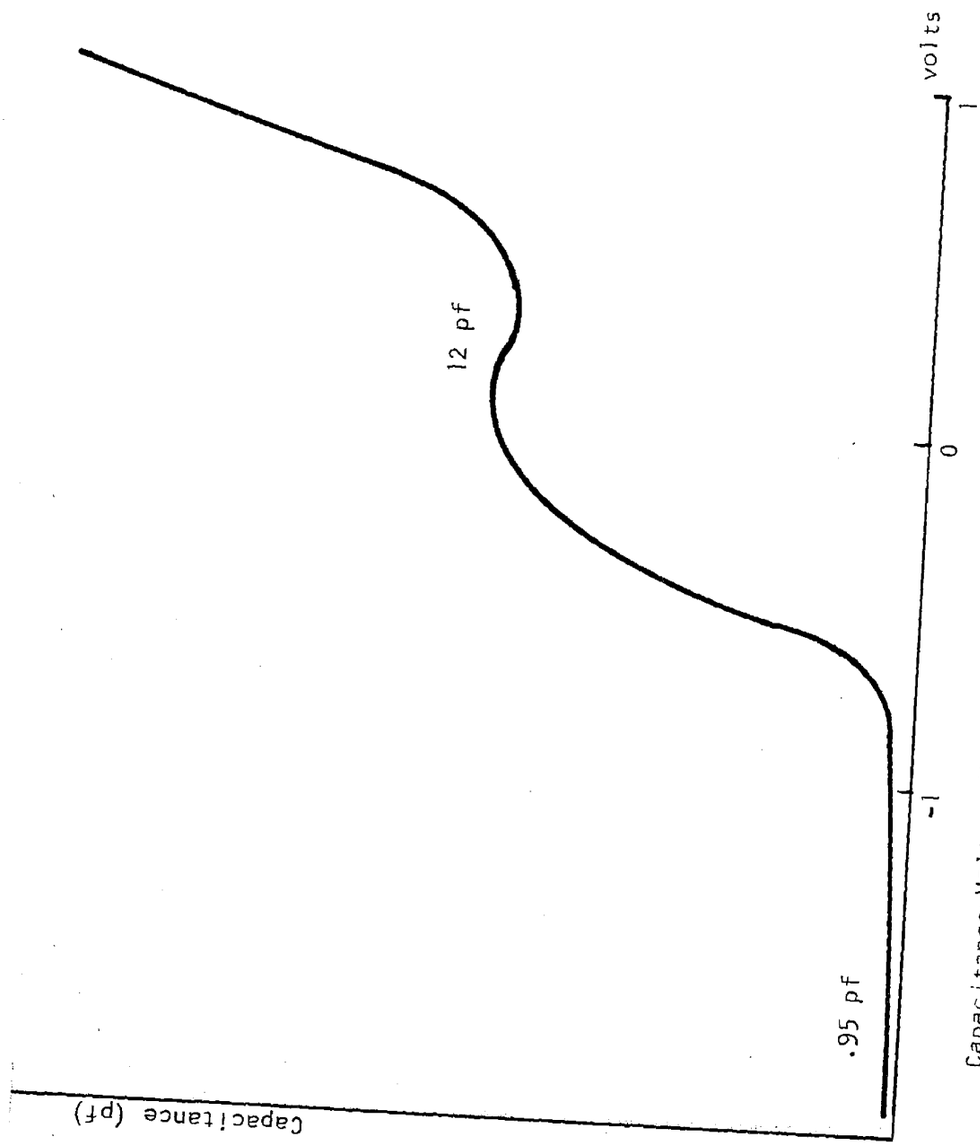
Figure F21



Capacitance-Voltage Measurements

Wafer N-73

Figure F22

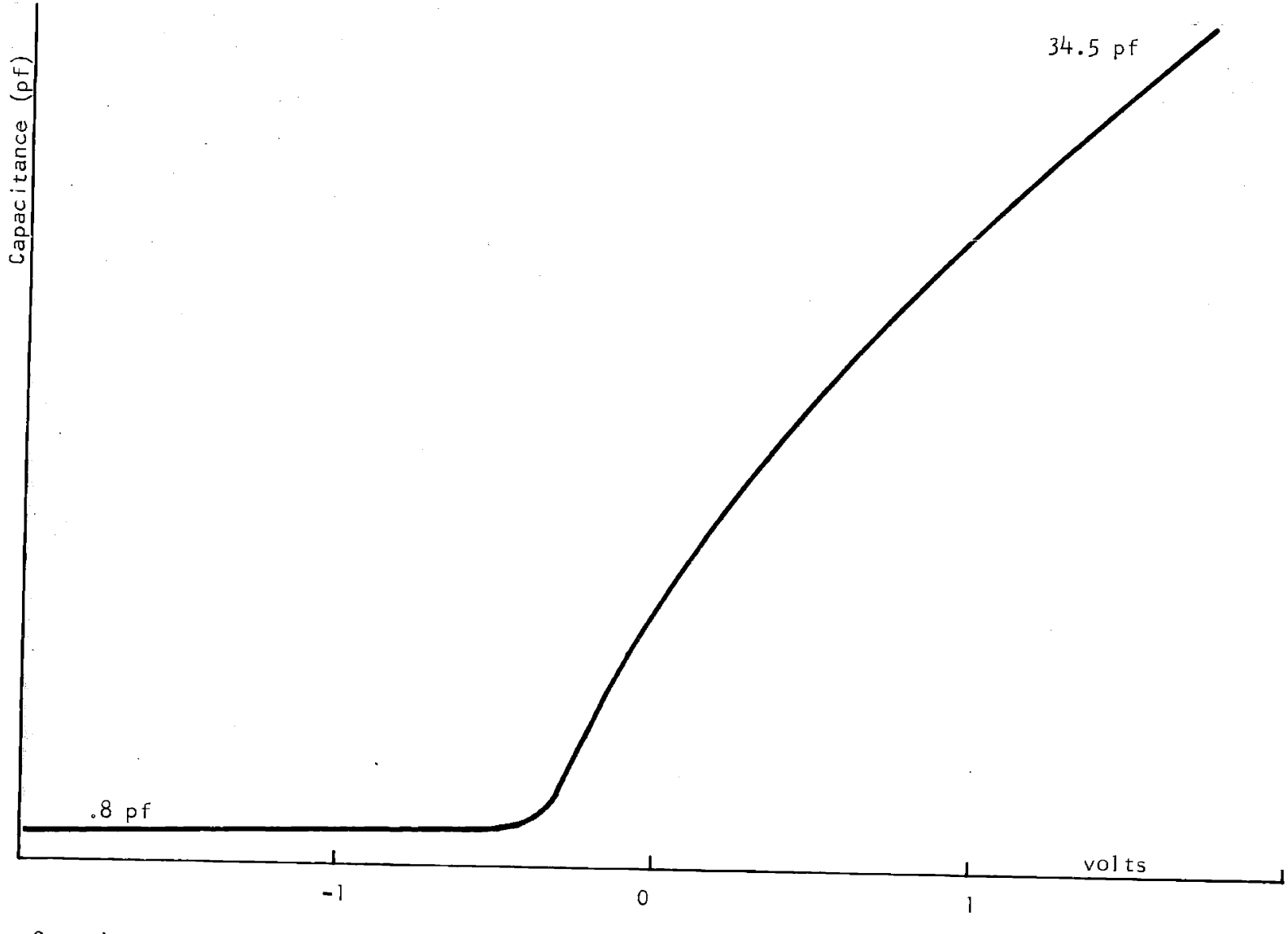


Capacitance-Voltage Measurements

Figure F23

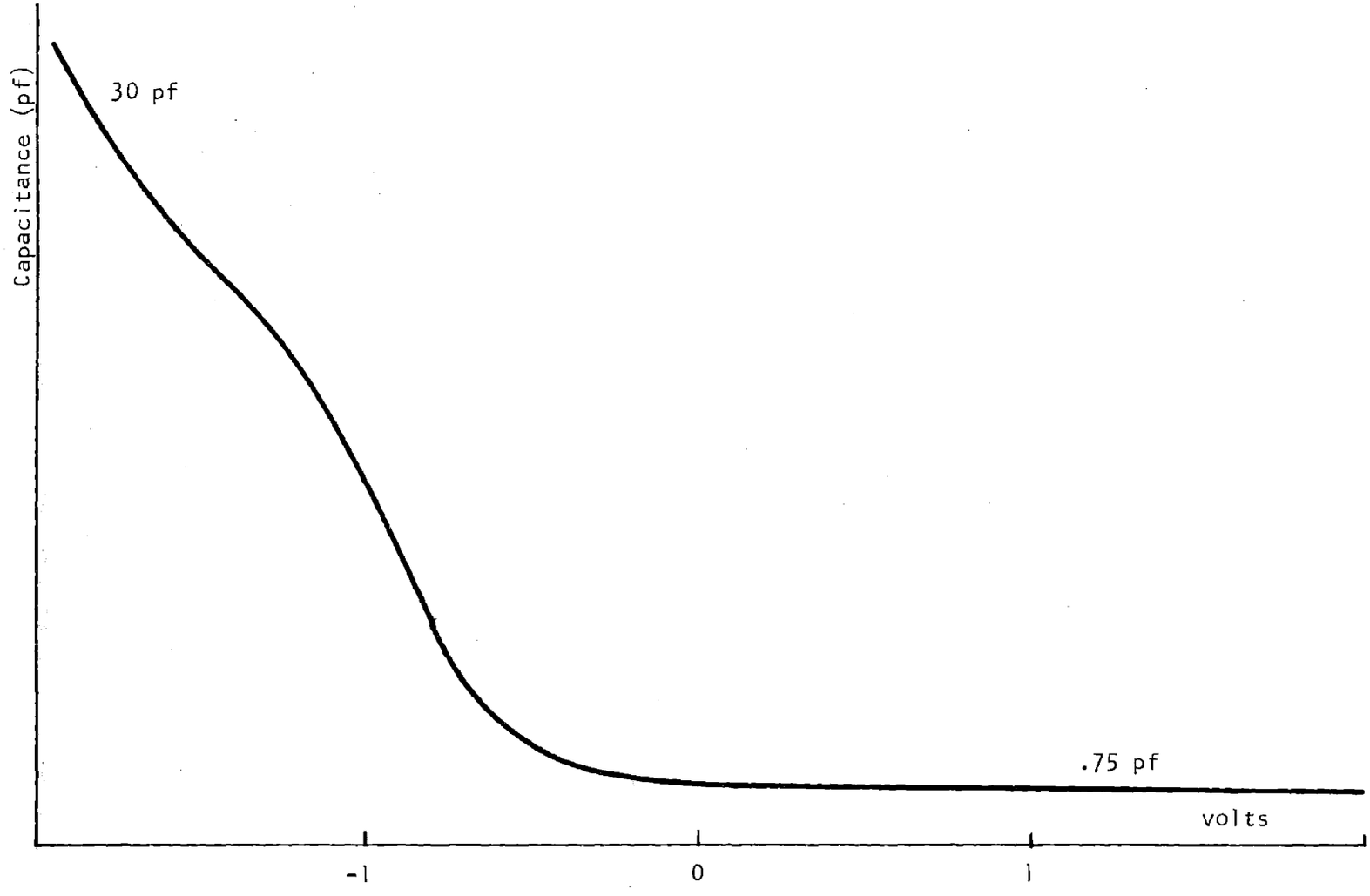
Capacitance-Voltage Measurements Wafer N-124

Figure F24



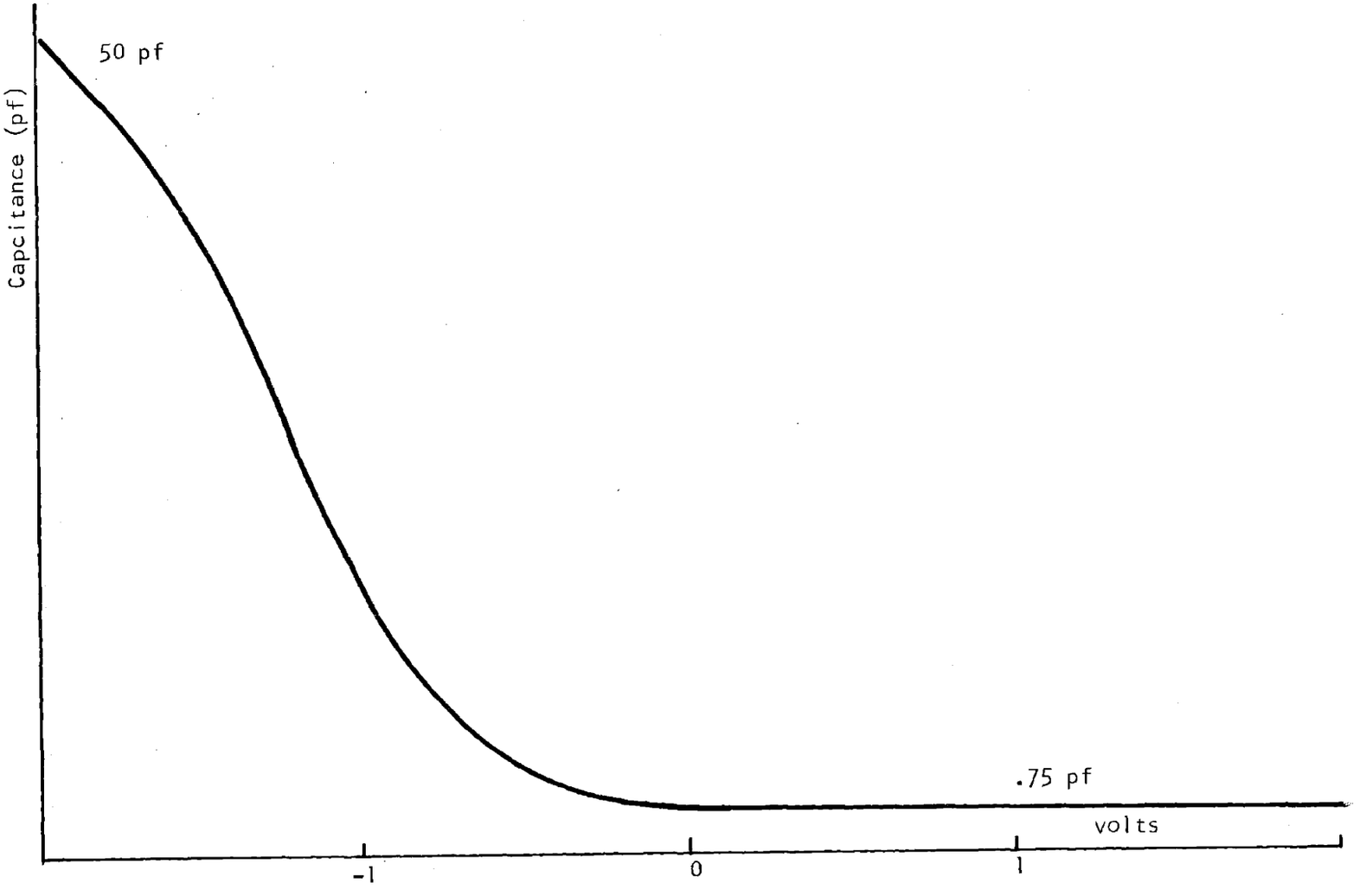
Capacitance-Voltage Measurements Wafer N-144

Figure F25



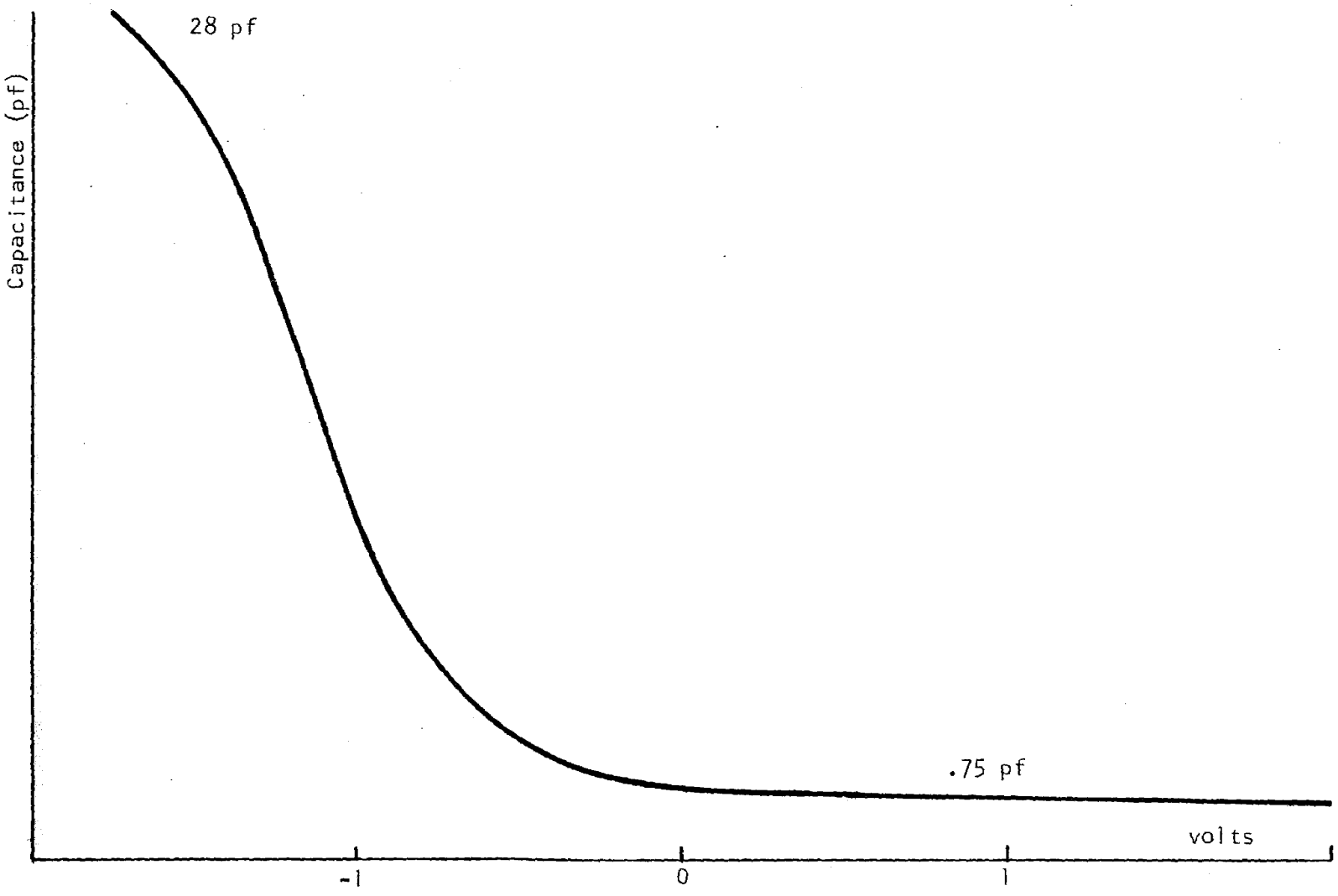
Capacitance-Voltage Measurements Wafer P-154

Figure F26



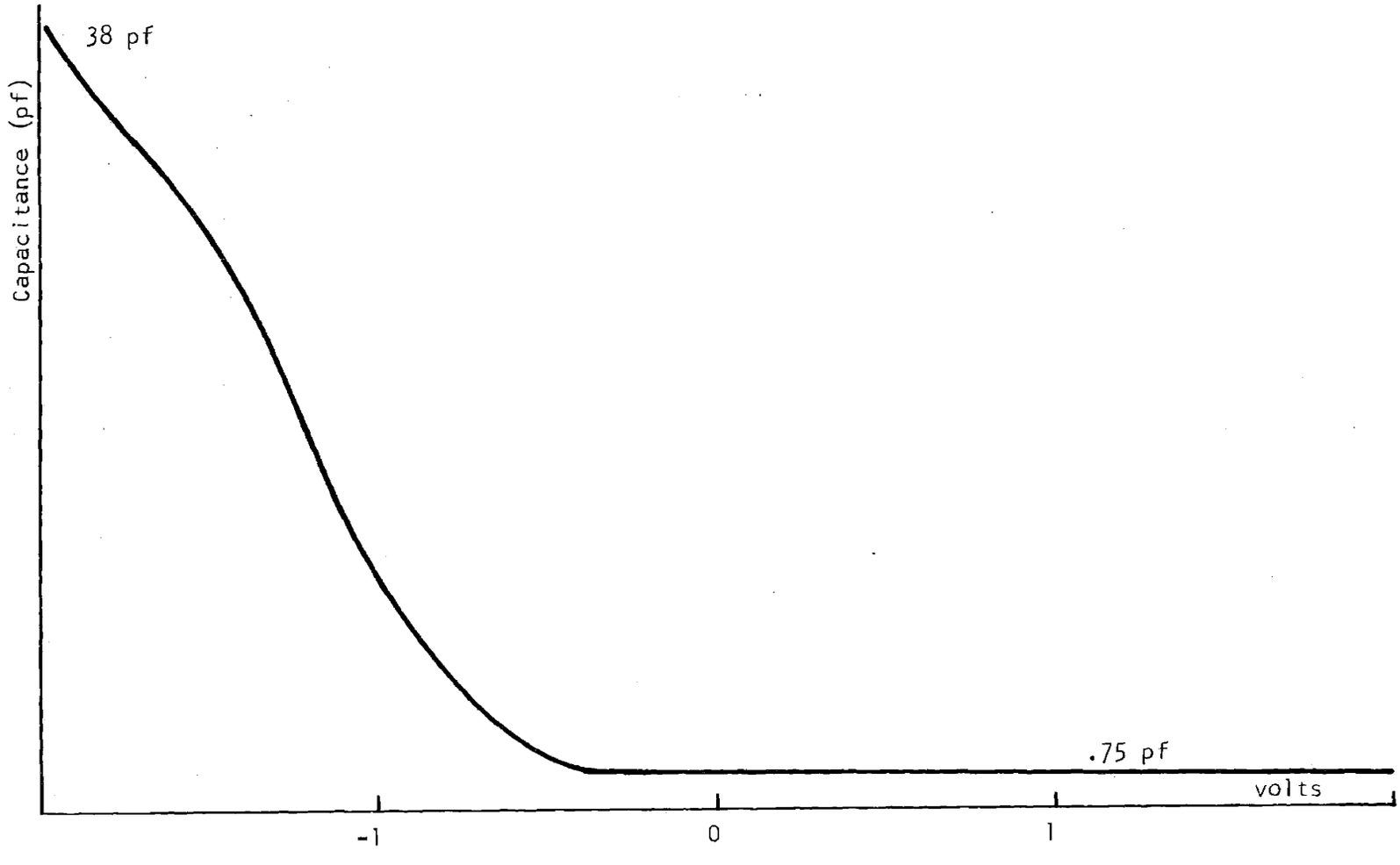
Capacitance-Voltage Measurements Wafer P-164

Figure F27



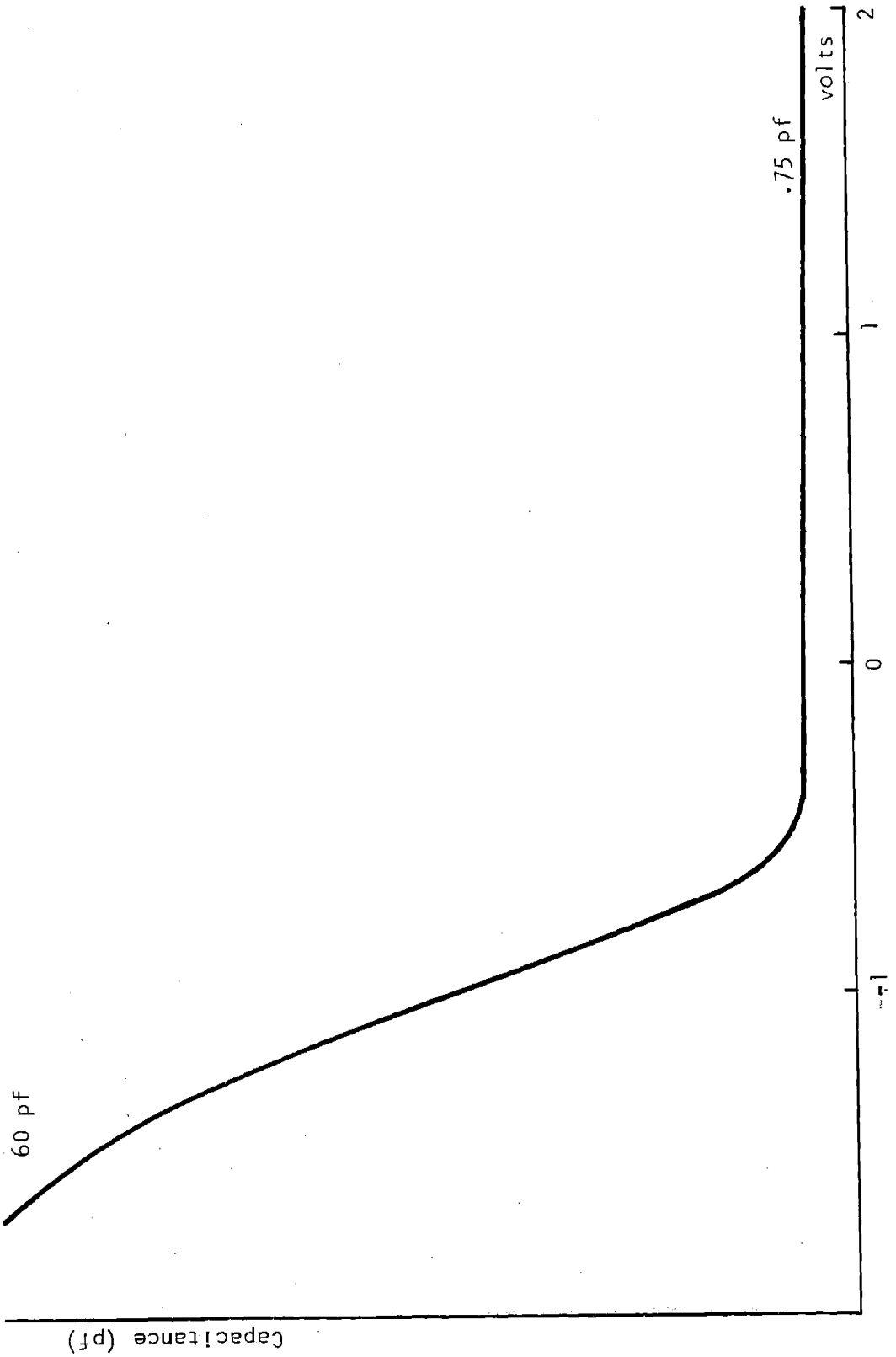
Capacitance-Voltage Measurements Wafer P-174

Figure F28



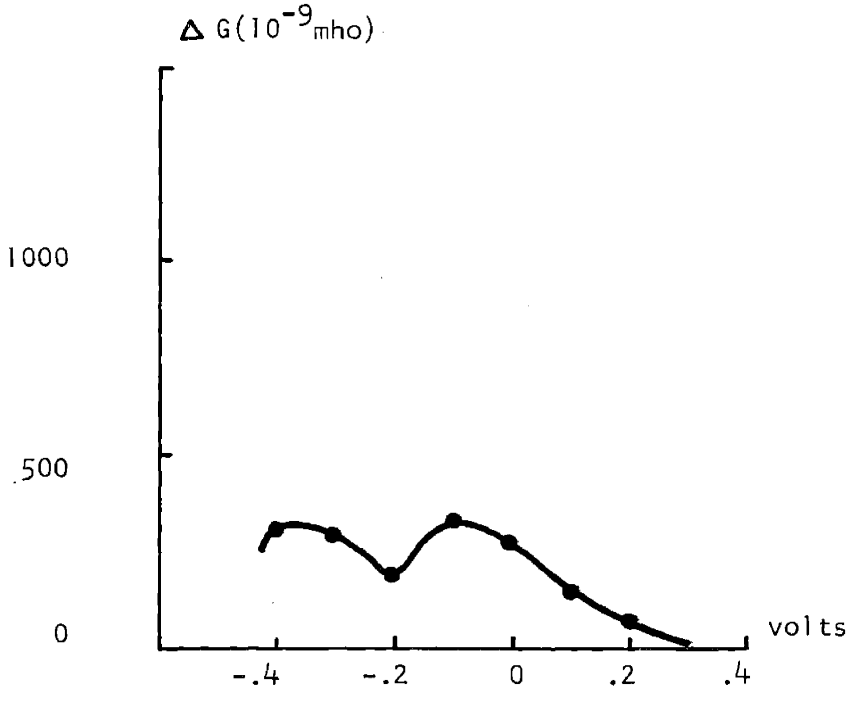
Capacitance-Voltage Measurements Wafer P-184

Figure F29



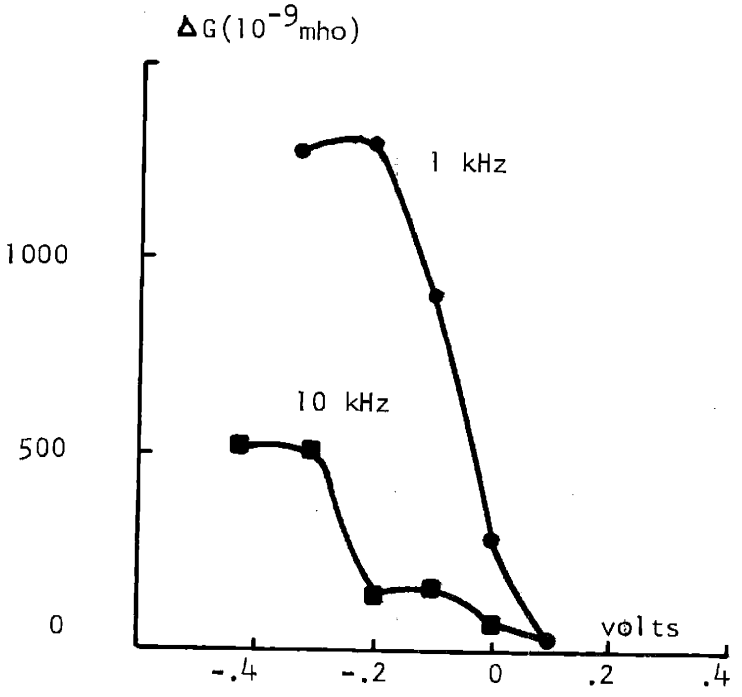
Capacitance-Voltage Measurements Wafer P-194

Figure F30



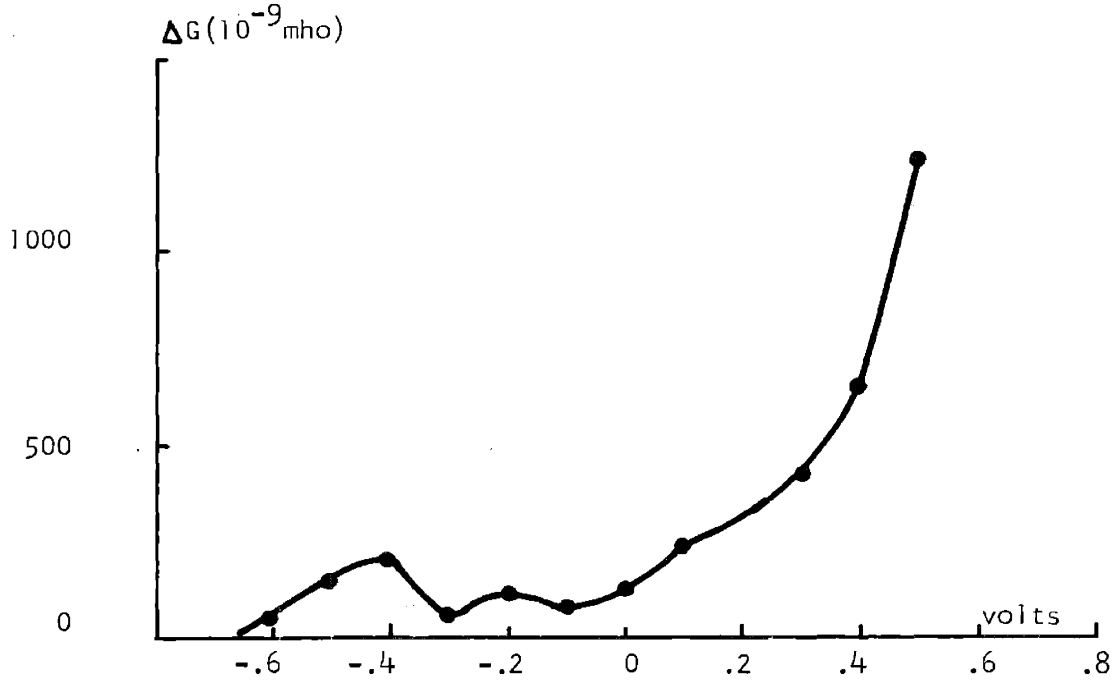
Surface State Conductance Wafer P-63

Figure F31



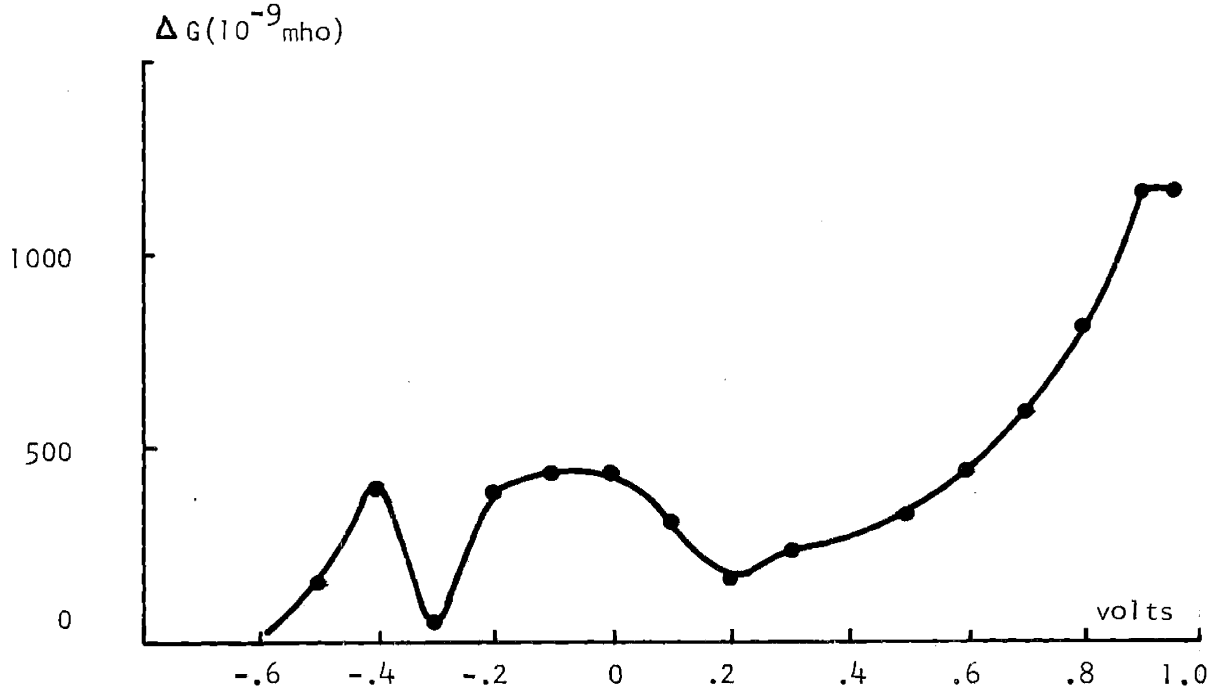
Surface State Conductance Wafer P-73

Figure F32



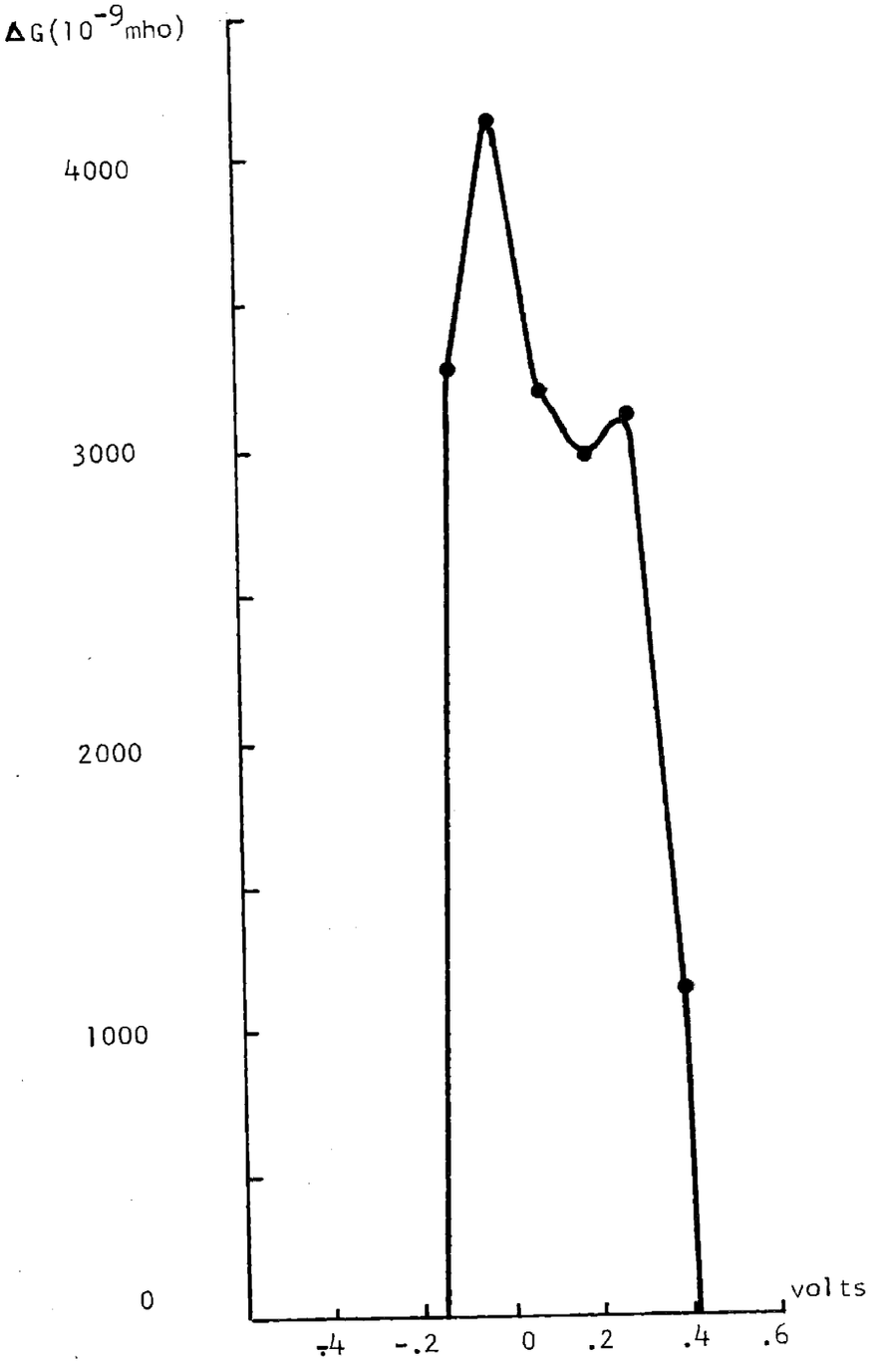
Surface State Conductance Wafer N-124

Figure F33



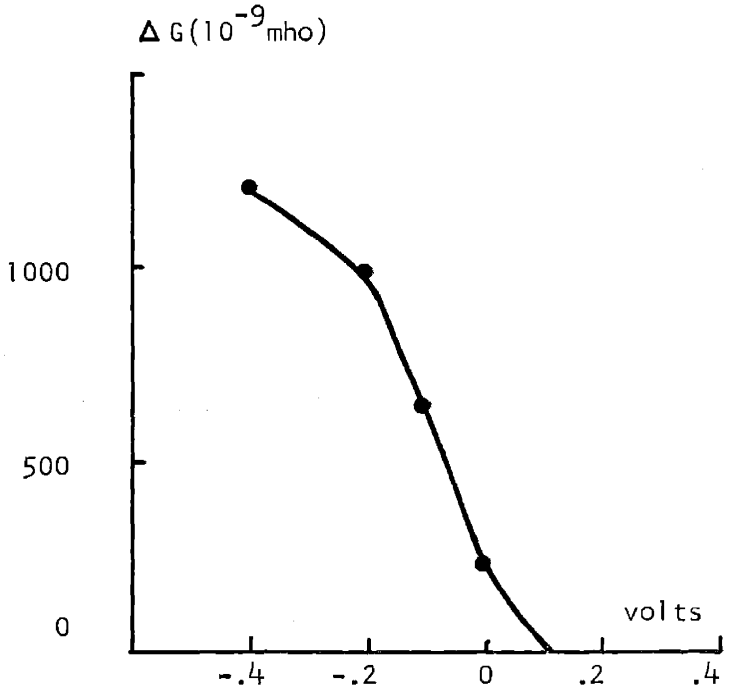
Surface State Conductance Wafer N-134

Figure 34



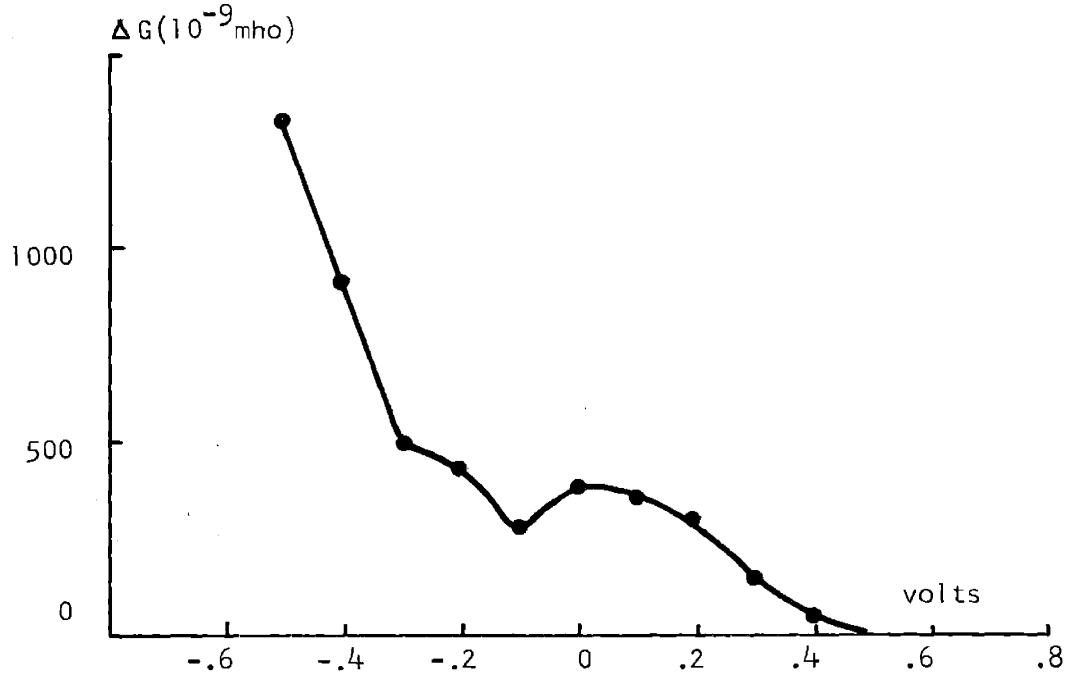
Surface State Conductance Wafer N-144

Figure F35



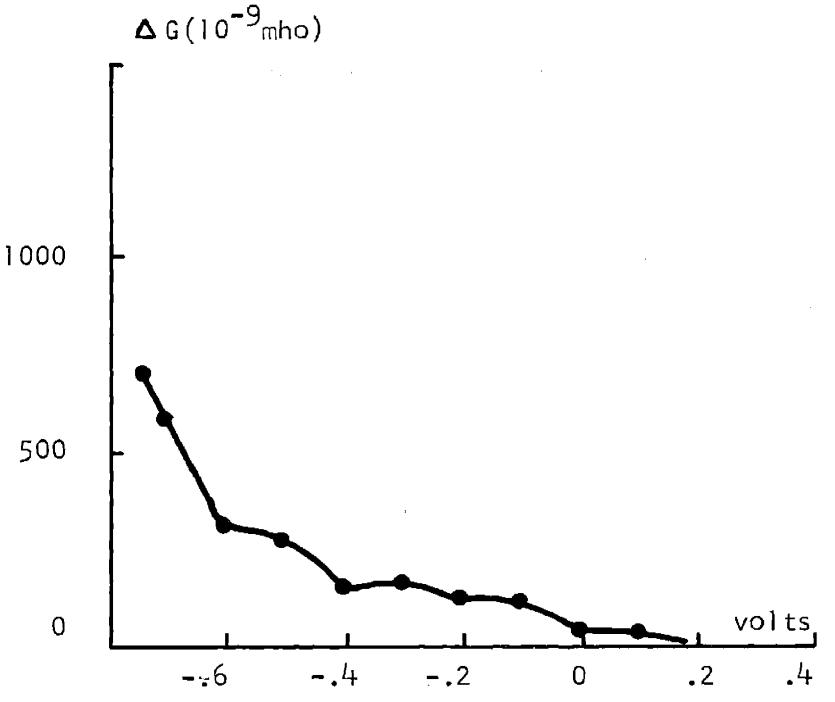
Surface State Conductance Wafer P-154

Figure F36



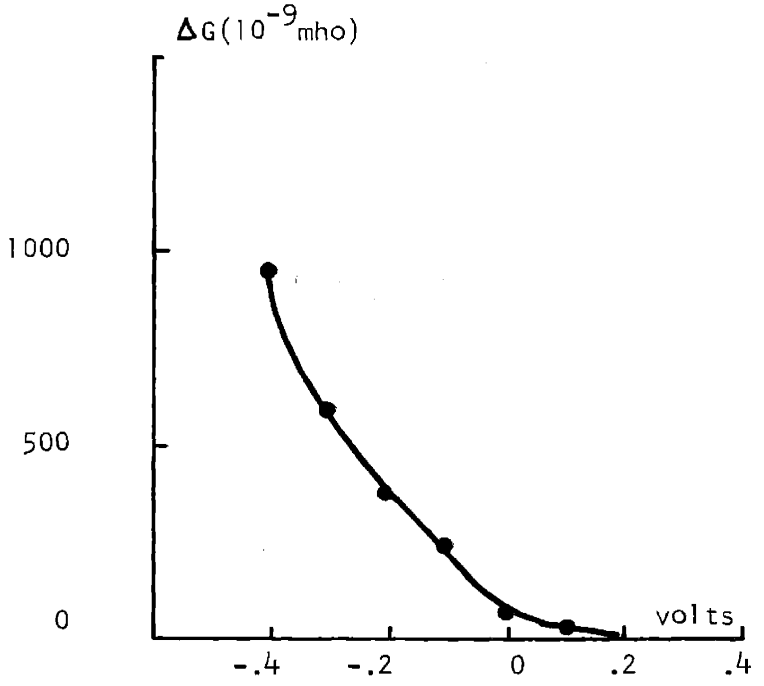
Surface State Conductance Wafer P-174

Figure F37



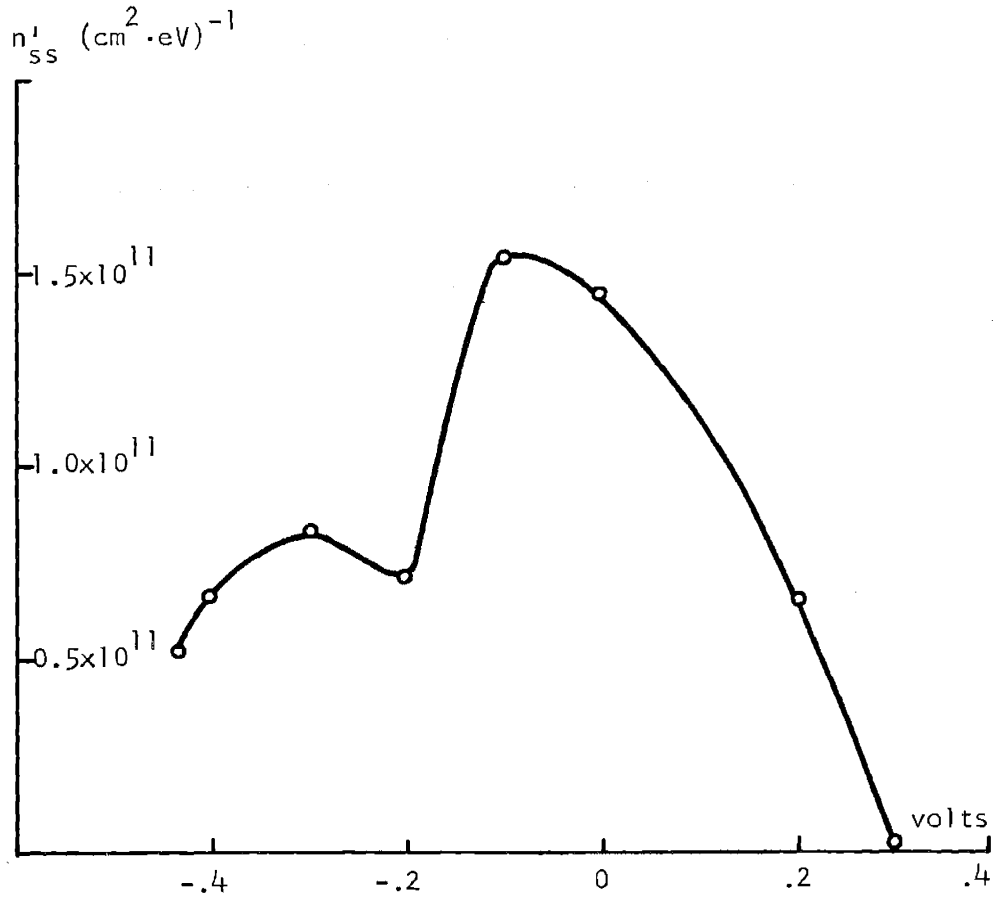
Surface State Conductance Wafer P-184

Figure F38



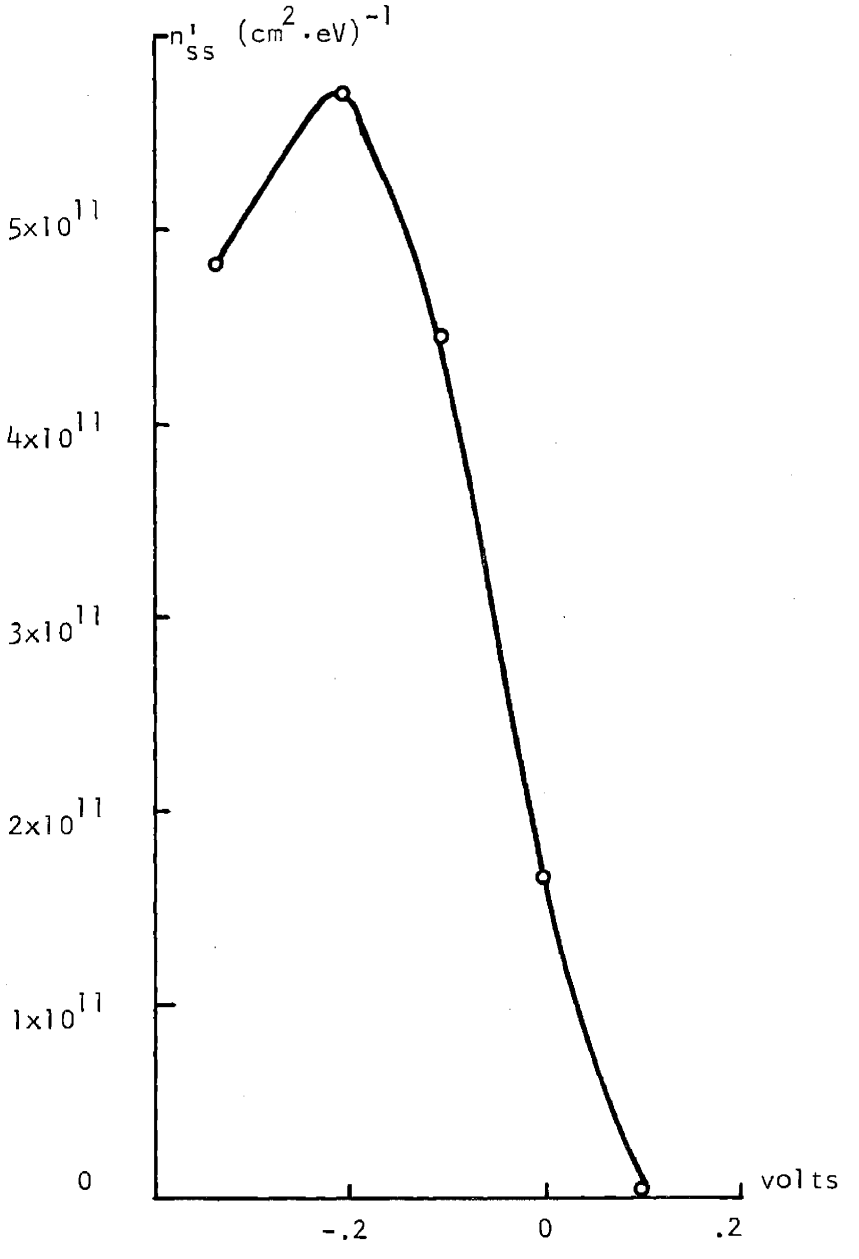
Surface State Conductance Wafer P-194

Figure F39



Surface State Distribution as Determined from Tunnel Conductance
Wafer P-63

Figure F40



Surface State Distribution as Determined from Tunnel Conductance
Wafer P-73

Figure F41

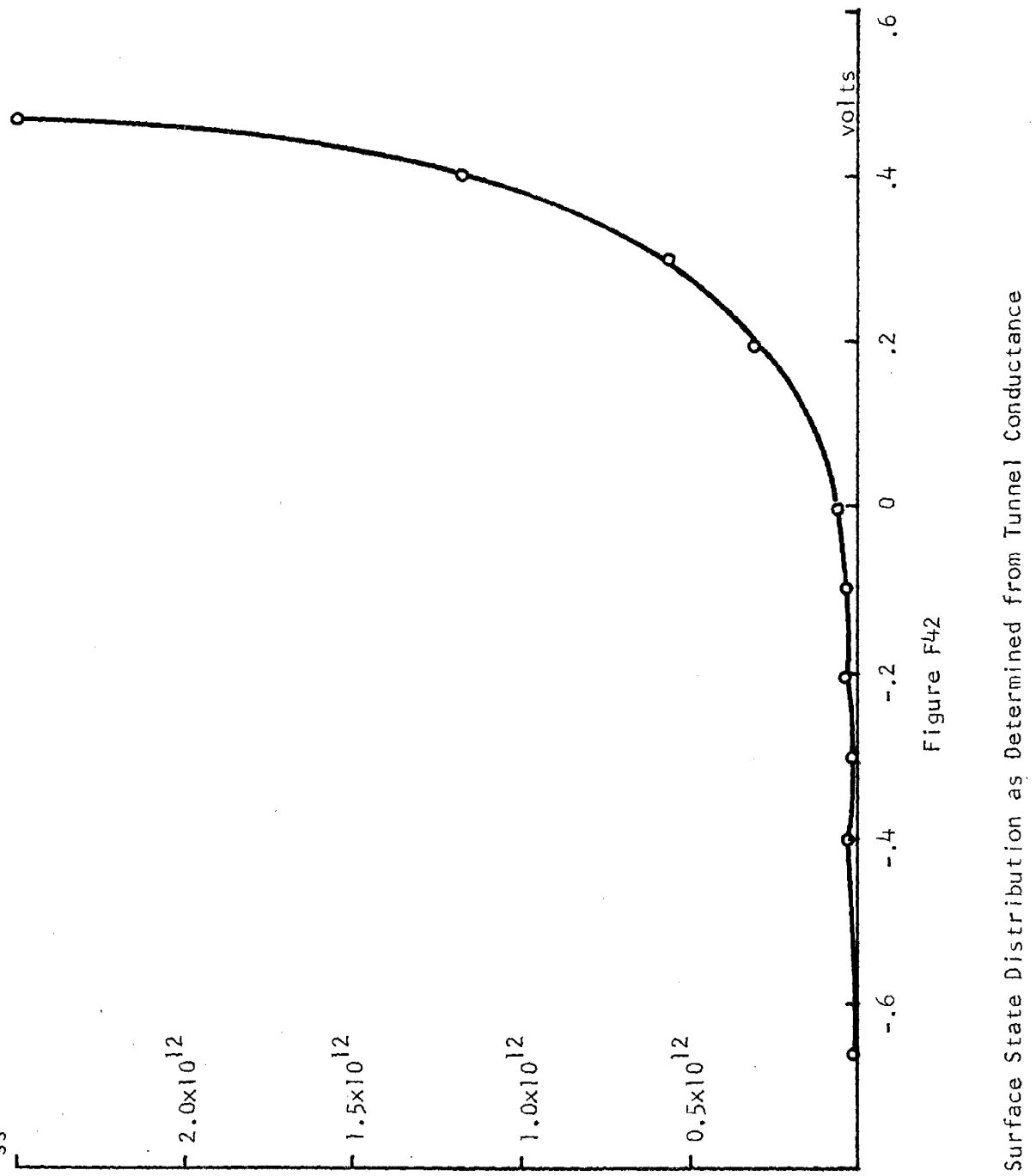


Figure F42

Surface State Distribution as Determined from Tunnel Conductance

Wafer N-124

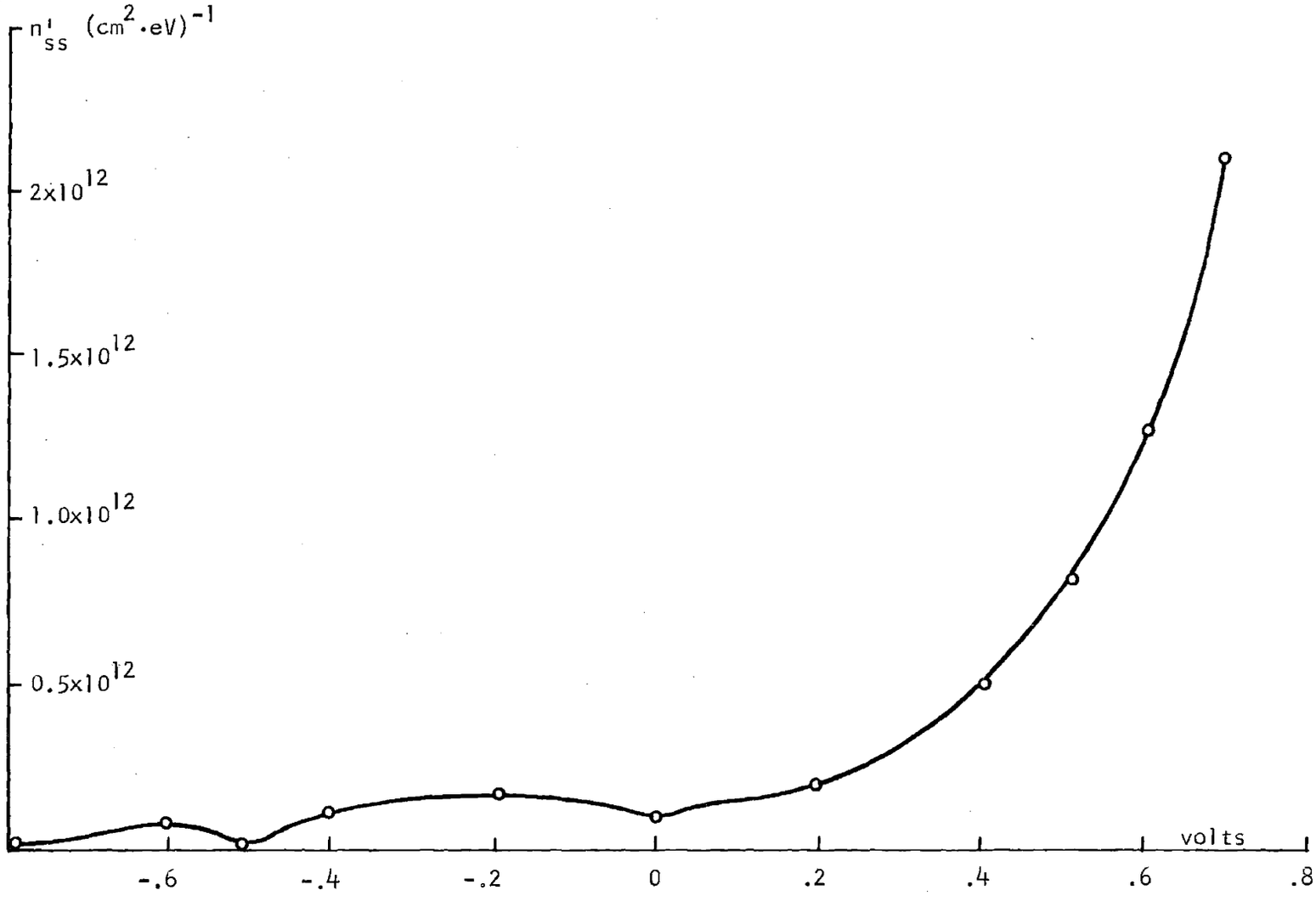
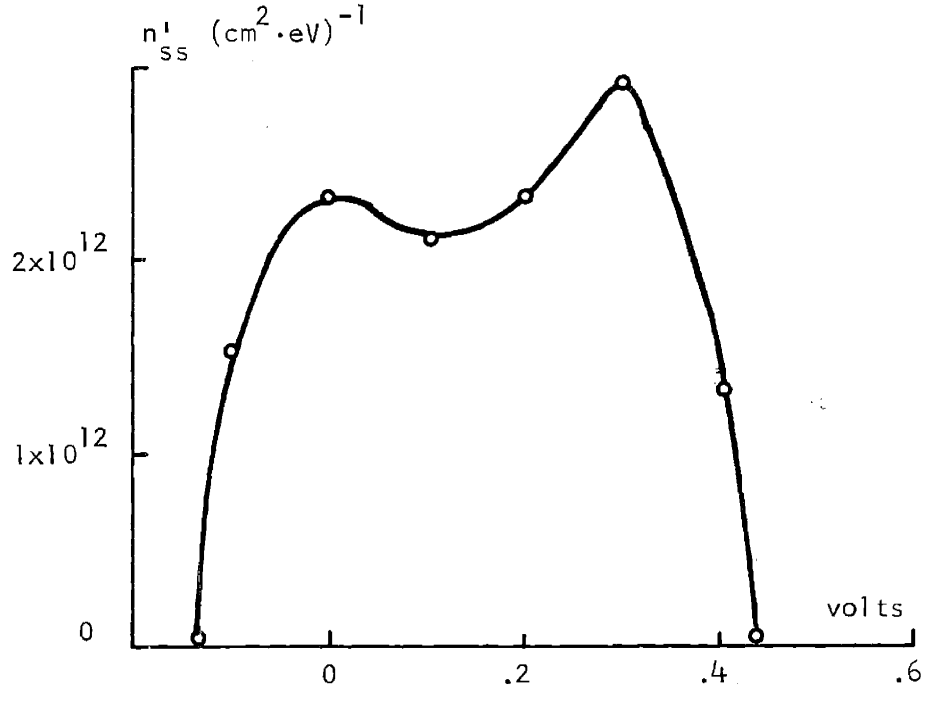


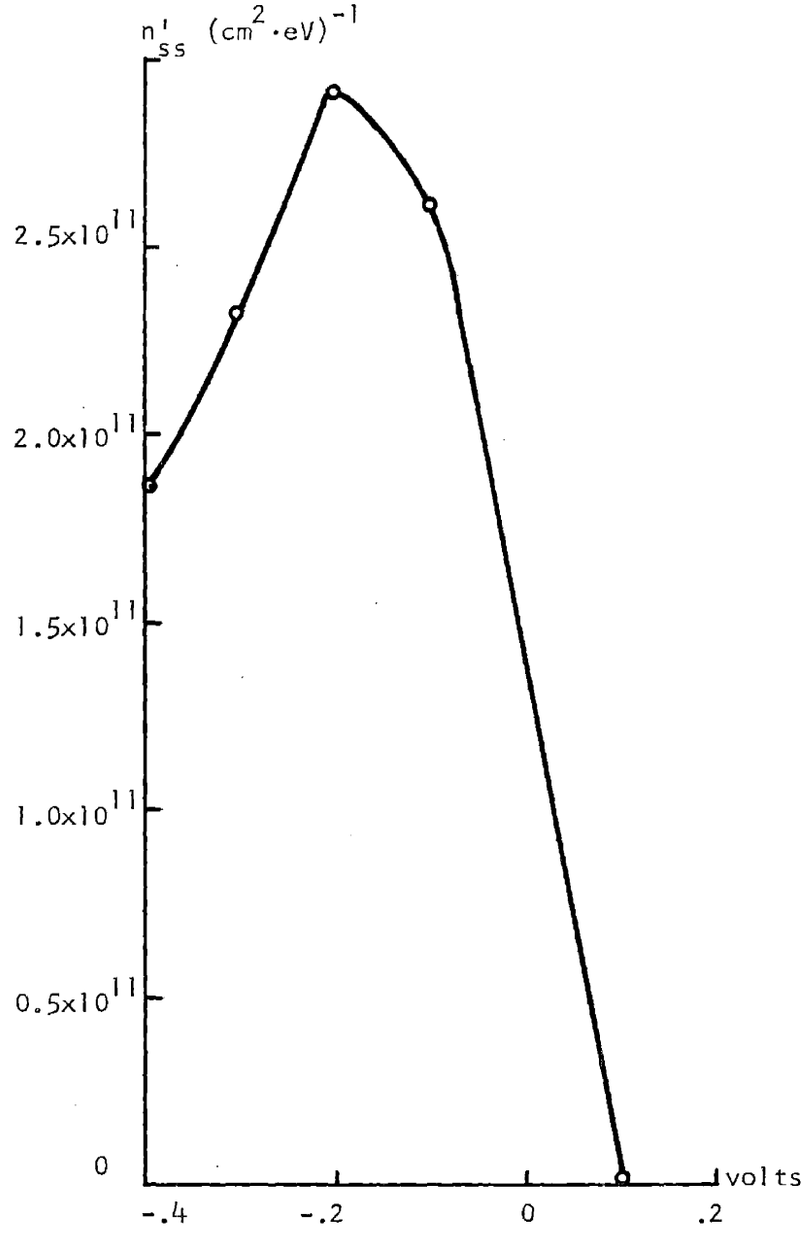
Figure F43

Surface State Distribution as Determined from Tunnel Conductance
Wafer N-134



Surface State Distribution as Determined from Tunnel Conductance
Wafer N-144

Figure F44



Surface State Distribution as Determined from Tunnel Conductance
Wafer P-154

Figure F45

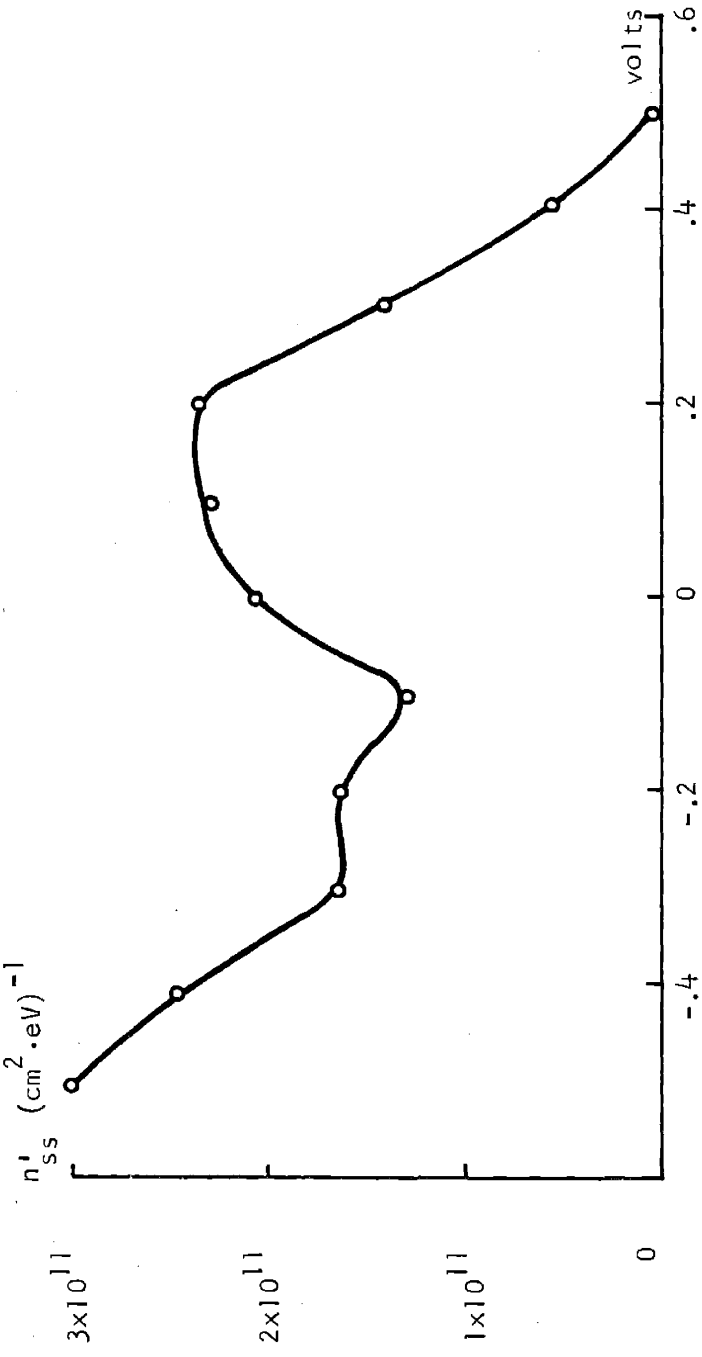
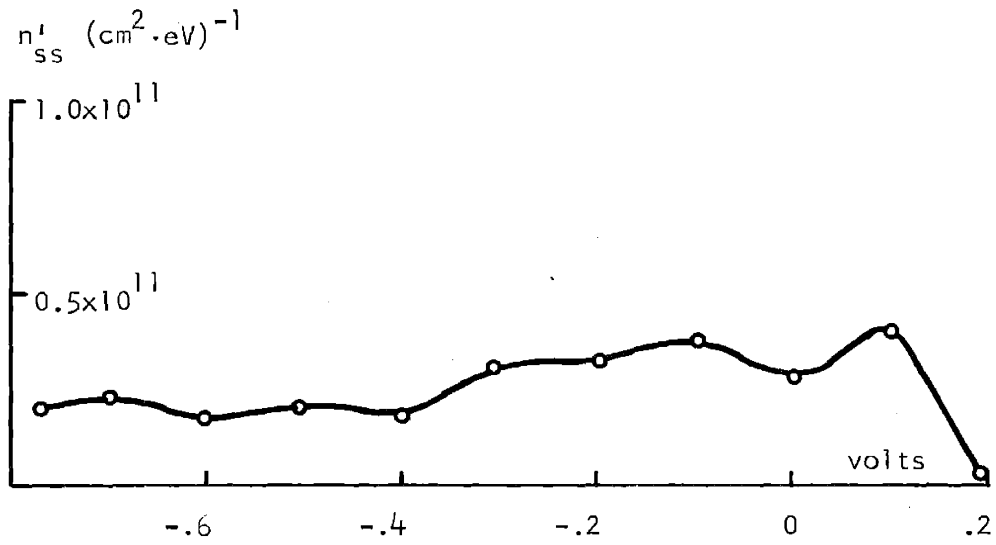


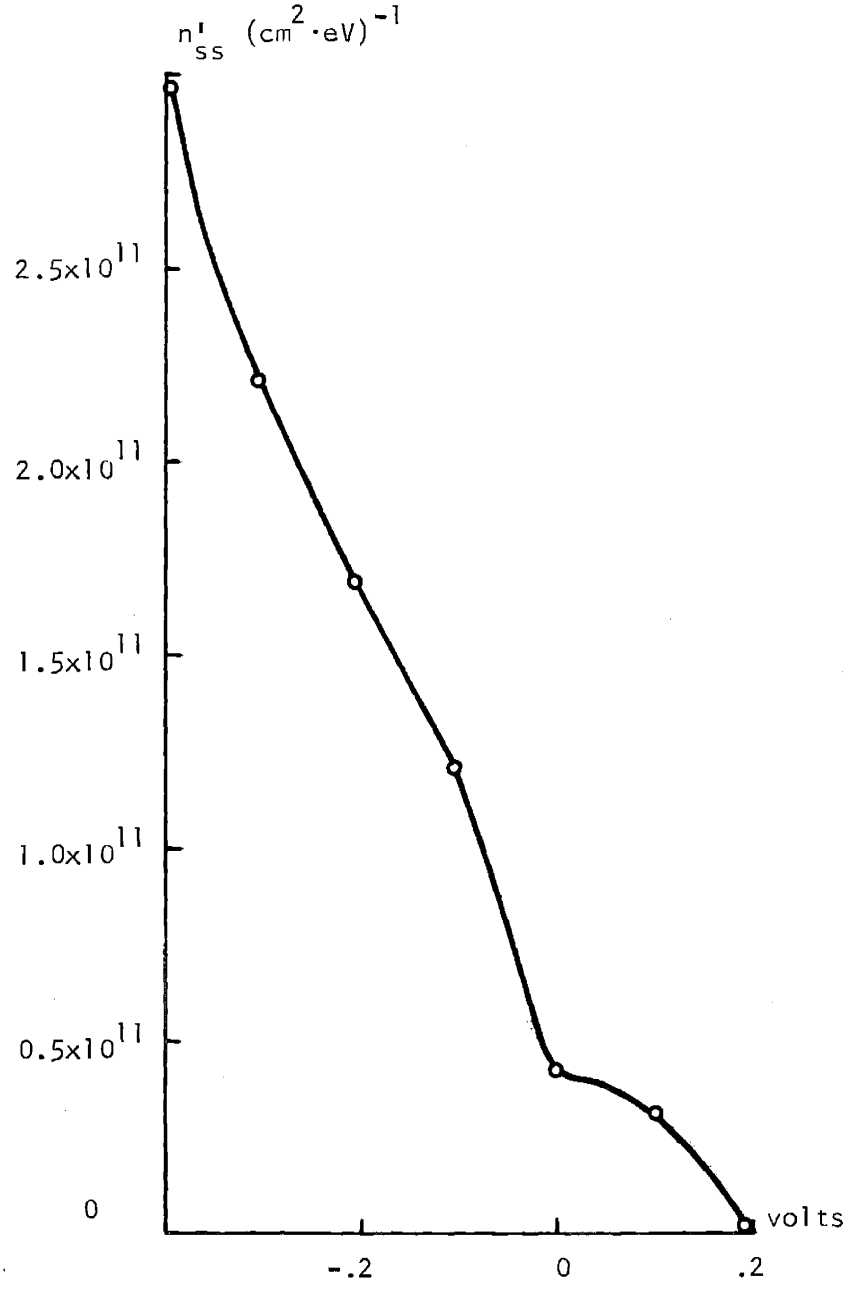
Figure F46

Surface State Distribution as Determined from Tunnel Conductance
Wafer P-174



Surface State Distribution as Determined from Tunnel Conductance
Wafer P-184

Figure F47



Surface State Distribution as Determined from Tunnel Conductance
Wafer P-194

Figure F48

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The author received a National Science Foundation Fellowship and National Aeronautics and Space Administration Traineeship for support in graduate school. He is a member of Eta Kappa Nu, Tau Beta Pi, Sigma Xi, American Association for the Advancement of Science, the Institute of Electrical and Electronic Engineers, and the Electrochemical Society.

He also served in a part time capacity as a staff physicist to the National Aeronautics and Space Administration Electronics Research Center in Cambridge, Massachusetts from June 1965 to June 1970. He was presented with the Apollo Achievement Award from NASA.

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