

Integrated Feedback Circuit for Organic LED Display Driver

by

Matthew Reid Powell

Submitted to the Department of Electrical Engineering and Computer
Science

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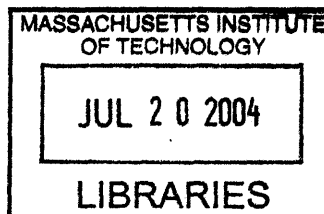
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Abstract

Organic LEDs (OLEDs) offer the potential of ultra low power, portable display technology. The chief barrier to their usage lies in producing OLEDs that will emit light at predictable and consistent amplitudes. We propose the use of optical feedback to generate the desired luminosity pixel by pixel. We implement this technique in an integrated silicon chip. The simulation and verification of fabricated integrated circuits with deposited OLEDs validates the utility of the technique.

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Chapter 1

Introduction

Portable electronics are quickly becoming an integral and omnipresent part of our public and private lives. From camera cell phones to digital hand held video recorders, we are inundated with products most people would not have dreamed possible just fifteen years ago. And yet manufacturers of consumer electronics are not closed to finished, promising even further integration of digital tools and toys into our daily lives.

This dramatic progress has been largely due to rapid advancement in integrated circuit technology. However, other components of portable electronic devices have not developed or improved as quickly. The designs for such components generate bottlenecks in our passage into a mobile information age. Display technology is an example of one of the principle challenges in developing mobile electronics. Power hungry, heavy and space-consuming, designers are always looking for ways to improve the performance and efficiency of their displays whether they are for labtops or simply cell phones.

1.1 Thesis Objectives

This thesis aims to explore the possibility of using Organic Light Emitting Diodes (OLED) as a display technology. An integrated circuit is designed and built to drive an OLED display using pixel by pixel optical feedback. This technique addresses

the nonlinearity of OLED devices, mismatching between devices, and performance degradation over the device lifetime.

1.2 Thesis Motivation

The principle requirement on portable displays are that they be slim and consume as little power as possible. The most common solution today, frequently appearing in notebook/palmtop computers, are liquid crystal displays (LCD). However, LCDs are typically highly inefficient and frequently have a limited viewing angle. Typical efficiency of an LCD display is roughly 1 lm/w (lumens/watt). OLEDs function much like forward biased LEDs in silicon. Light is emitted as a function of the current through the device. As a direct emission technology, OLEDs appear to be an affordable, highly efficient alternative. The best efficiencies of OLEDs are 5 lm/W for blue OLEDs, 600 lm/W for green OLEDs and 15 lm/W for red OLEDs. [1]

In the hopes of realizing the potential advantages inherent to OLED displays, many researchers have worked to find practical solutions to their shortcomings. But the development of OLED technology is behind that of LCDs. First and foremost, building OLEDs with operating characteristics and a lifetime suitable for commercial use has proved elusive. It was not until 1987 that the first vacuum-deposited OLEDs with low operating voltages were demonstrated. [2] Researches have found that various forms of encapsulation of OLEDs can extend their lifetime by as much as two orders of magnitude. Research suggests that devices' continual operation lifetime could easily exceed 1000 hours. [3] However, the power-efficiency curves and I-V relationships of OLEDs are extremely difficult to match between devices. Moreover, both of these characteristics will degrade over a device's lifetime.

None-the-less, work has been done to develop flat panel OLED displays. Much of the prior work has concentrated on driving a fixed current through each OLED to avoid voltage threshold variations. [4] This thesis aims at developing a feedback mechanism to control optical light output via an integrated circuit. This is a direct continuation of similar work done in a thesis by Eko Lisuwandi, who developed a

discrete version of a similar circuit. [5] This thesis seeks to advance that work and demonstrate the feasibility and scalability of using optical feedback implemented in a silicon integrated circuit to control OLED displays.

1.3 Organization

Chapter 2 contains a discussion of OLEDs, their advantages, disadvantages and the technique we will use to address their shortcomings, namely optical feedback. In Chapter 3, the integrated circuit design will be discussed and specified. The analog feedback loop and its components will be addressed in detail and the digital control aspects of the design will be dealt with briefly. Simulated circuits' performance will also be mentioned. Chapter 4 contains a discussion of the test setup and results. The thesis concludes in Chapter 5.

Chapter 2

Organic LED displays

OLEDs are an exciting new technology, but certain aspects of their performance leave a lot to be desired.

2.1 Advantages

As one of the dominant technologies on the market today, LCD displays are contrasted with OLEDs.

A basic LCD display is composed of a liquid crystal material sandwiched between two polarized layers. The liquid crystal material itself is polarized, and its optical axis can be rotated with the application of an electric field across the material. When the optical axis of the liquid crystal is aligned with the other polarizers, light passes through freely. When it is rotated 90 degrees, no light is able to pass through.

This technology works well enough, but it has a few problems. The liquid crystal is not a direct emission technology; it does not emit light on its own. In order for the LCD to generate an image some other light source must be employed. Unfortunately, the polarizers and liquid crystal layers may absorb as much as 50 percent of the light on their own. Overall, the light output of the display may be as low as 5 percent of the light generated by the source. This means the display is very inefficient and power hungry. Additionally, the optical properties of the liquid crystal and polarizers distort the image at sharp viewing angles reducing the effectiveness of the display.

The principle advantage of OLEDs is that they are a direct emission technology. As such, they directly address both of the limitations posed by LCDs. Overall, it is believed that OLED based displays could be brighter, thinner and lighter than LCDs, while solving the viewing angle problem. Furthermore, OLEDs can be made out of transparent materials, allowing them to be viewed from either side or used in a heads-up display. Transparent OLEDs can also be stacked, so blue, red and green OLEDs do not share space at each pixel, but lie on top of one another, each fully visible. Finally, the thickness of an OLED structure, typically less than a micrometer, allows for mechanical flexibility, holding the potential of flexible, and thus more portable, displays. [6]

One might wonder why if OLEDs are so promising, LEDs are not promising as well. There are, however, a variety of difficulties posed by LED technology that limit their practicality in the development of visual displays. The principle difficulty with LEDs is that it is still very challenging to generate certain colors, particularly blue. Any full color display would surely require three colors, blue being one of them. Blue LEDs have been made, but it is not feasible to piece together displays, pixel by pixel with discrete components. The color of LEDs are closely linked to their material composition and a standard CMOS process would not suffice to produce the different desired colors. This is where the problem lies. It is unclear what, if any, process would be able to support all of the necessary colors. And if it could be done, it would surely be prohibitively expensive. So the lack of LED displays should not disabuse us of the feasibility of an OLED display. OLEDs do not possess the same limitations.

2.2 Disadvantages

Unfortunately, there are drawbacks to OLEDs as well. Principally, the I-V characteristics of OLEDs tend to vary dramatically from device to device due to variations in the organic layer thickness, [7] making it very difficult to build drivers that can consistently produce the same optical output from different OLEDs with the same input. Furthermore, OLED performance is substantially affected by the operating

temperature. [8] Finally, OLEDs tend to degrade over time at differing rates, [9] producing greater non-uniformity in optical output and shorter device lifetimes.

2.3 Optical Feedback

To address these difficulties with OLEDs, this thesis proposes to use optical feedback to correct for nonlinearities or variations in OLED optical output. Using photodiodes as sensors and a reasonable amount of gain in the feedback loop, OLED performance should only be limited by performance of the photodiode.

2.3.1 Control at the Array Level

In this design we would like to have direct optical feedback for each pixel on an individual basis. In the simplest approach, we would have a feedback loop laid out around and under each pixel. However, we are designing the electronics for an OLED display laid out on the top of an integrated chip. If we are going to demonstrate the scalability of such a design the display should be at least 16 pixels by 128 pixels. Given the size of an integrated chip, this means the projected pixel size would be 25-50 microns on a side. That is not a lot of area under each pixel, and it would be a tremendous disadvantage to have a lot of non-transmitting area around each of the pixels, producing a small fill factor. Since it is therefore not possible to place a feedback loop at each pixel, our design must have a minimum of electronics at each pixel with the feedback generating circuitry outside of the array. Further, it is likely that the parasitic power dissipated by the circuit will be proportional to the number of op-amps in the feedback networks. If there is a feedback loop at each pixel, that power will scale as the number of pixels. With a feedback loop per column, that power only scales as the square root of the number of pixels. Since power dissipation is a principle concern in any display, this advantage in scalability is significant.

Instead of a feedback loop per pixel there will be a feedback loop per column. To generate a single image, all of the rows are selected one after another, with each feedback loop driving one pixel in that row. The voltage necessary to generate the

desired optical output is found and then stored until the next time the row is selected. For an effective display, the refresh rate will be determined by the time it takes to cycle through all the rows. This time will be the settling time of the feedback loop multiplied by the number of rows. To increase the refresh rate one must decrease the settling time.

2.3.2 Circuitry at the Pixel Level

The aim is to use a minimum number of components at each pixel. Our design choices reflect that goal. A schematic is shown in Figure 2-1. There are only three transistors driving the OLED. The first two, M1 and M2, are the row select switch and a dummy transistor to reduce charge injection on the gate of M3. M3 is set up as a transconductance amplifier. The key feature in this topology is that the principal limiting factor in the response time of the OLED is the small signal capacitance of the OLED in parallel with the output resistance of the transistor. The pole thus generated will drive the design of the rest of the feedback circuitry. Rough estimates place the pole in the lowest case to be 100 kHz.

Also needed at each pixel is a photodiode, which functions as a sensor mechanism. In reverse-bias, a photodiode's reverse current is linearly related to the amount of light incident on the photodiode. Our photodiode will draw current from the capacitance at the gate of M5. When M6 is switched on, M5 is driven by a current source provided to the entire pixel column. The current source is not shown in the pixel schematic. M5 acts as a source follower and the sensor output tracks the gate of M5. This allows the sensor to drive the capacitance on the line all the way back to the rest of the feedback circuitry. M4 acts as a switch allowing the capacitance on the gate of M5 to be reset to ground while the sensor is not being used. A miniature simplified version of the array is seen in Figure 2-2.

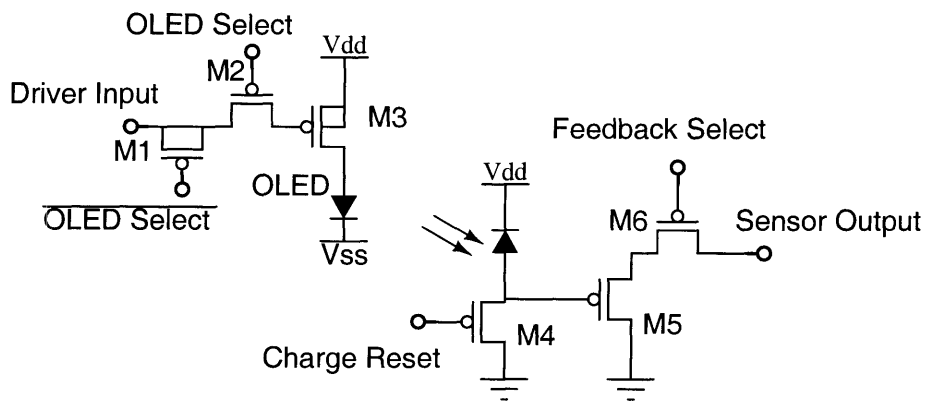


Figure 2-1: Circuit diagram of a pixel

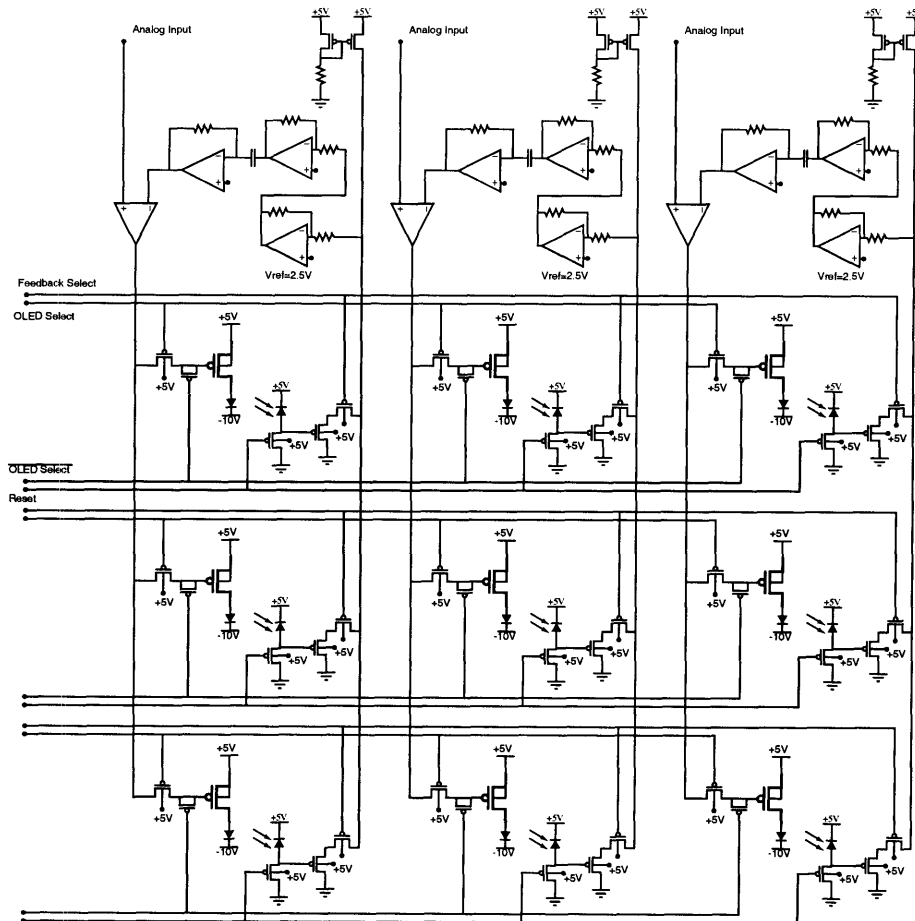


Figure 2-2: One feedback loop per column

Chapter 3

Circuit Design

The OLED display driver was designed with both analog and digital circuitry. The control for the system is a continuous time analog feedback loop. The loop employs op-amps with switched capacitor filters. The display array requires a digital row address circuit and the pixels require four digital control signals, with proper timing.

3.1 Analog Feedback Loop

The feedback loop links the output from the photodiode sensor to the OLED current driver. There are three important requirements for the feedback loop. It must be stable. It must compensate for the OLED's nonlinearity. And it must have a settling time fast enough to allow for an adequate refresh rate on an OLED display. However, any design must address the constraints posed by the OLED and sensor networks.

3.1.1 Design Constraints

The primary design constraint in the feedback loop stems from the response time of the OLED. Although the voltage-current relationship of the OLED is highly nonlinear, it can be modeled as an equivalent small-signal resistance (R_{OLED}) at any bias point. Moreover, its response time can be modeled as an equivalent capacitance (C_{OLED}) in parallel with R_{OLED} . Given these values and the output resistance of the transistor

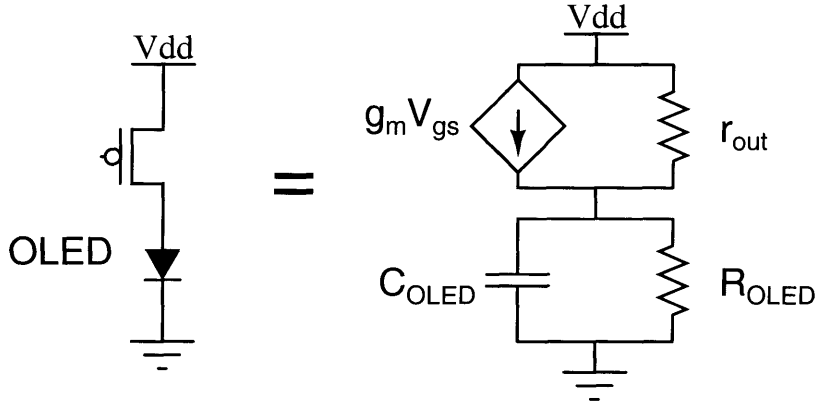


Figure 3-1: A visual explanation of the small signal model used for the OLED

driving the OLED (r_{out}), the response time of the OLED can be modeled as a pole appearing at the following frequency,

$$f = \frac{1}{2\pi C_{OLED}(R_{OLED} || r_{out})} \quad (3.1)$$

Measured data from OLEDs gives an approximation of where this pole will appear. Data is shown in Table 3.1. Capacitance should be increasing linearly with OLED area and resistance should be inversely proportional to OLED area. The pixel area in our array will be roughly 30 microns in diameter. Scaling properly for OLED area, $C_{OLED} \approx 160\text{fF}$ and $R_{OLED} \approx 10\text{M}\Omega$. The output resistance of the silicon transistor is

Table 3.1: Measured OLED response data

Voltage	1mm in diameter			0.25mm diameter		
	Cap (pF)	Res (K Ω)	Freq (KHz)	Cap (pF)	Res (K Ω)	Freq (KHz)
2	169	12.2	77.2	11.7	168.2	80.9
4	170	14.8	63.3	11.8	149.3	90.4
6	175	11.8	77.1	11.8	150.6	89.6
8	162	9.44	104	10.9	74.5	196
10	152	7.11	147	8.9	30.7	583

$$r_{out} = \frac{1}{\lambda I_d} \quad (3.2)$$

Each pixel only requires nanoamperes of current, so the transistor driving the OLED will be biased in the subthreshold region with a very high output resistance. At the largest expected current drive of 10 nA, HSPICE simulation gives an $r_{out} = 30\text{M}\Omega$. Thus it is safe to approximate the position of our pole as

$$f = \frac{1}{2\pi R_{OLED} C_{OLED}} \quad (3.3)$$

Based on our data, this value is about 100 KHz and is independent of the OLED area, thus fixed by the technology. However, substantial variation is expected in these parameters from device to device so the feedback loop design must be robust with respect to the exact frequency of the pole.

Given the response time of the OLED, there are two options for the remainder of the feedback loop. The first is to use the OLED as the dominant pole in the feedback loop and to push all the other poles in the system above the crossover frequency to insure stability. However, the amount of compensation provided by the feedback loop is proportional to its open loop DC gain. Even if this value were as low as 100, with the dominant pole occurring at 100 KHz, the crossover frequency would be at 10 MHz. In order to insure stable operation for a range of OLED response times, the remaining poles in the system would probably have to occur at 30 MHz or higher. Since TSMC's 0.35 micron process was chosen for the project, that is a fairly stringent requirement for a low power circuit. Fortunately, other options exist.

The second option is to introduce a dominant pole at a low frequency and aim for a crossover frequency of 100 KHz while pushing the rest of the system poles above 1 MHz. This has the benefit of providing for stable operation for a wide range of OLED response times while presenting easier specifications to meet for the rest of the feedback loop. The difference from the first option will be that the settling time will be much longer. However, it will still be fast enough. The required time to settle for each pixel row is given by, $t = 1/(\text{refresh rate} * \text{number of rows})$. In the display

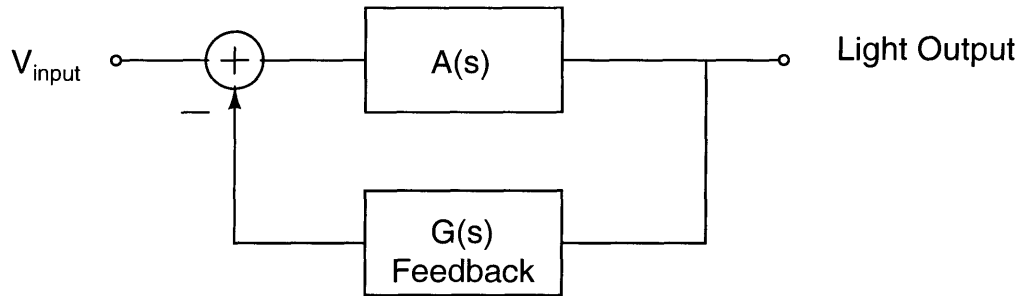


Figure 3-2: A simple look at the feedback loop block diagram

there are 128 rows. Even with a refresh rate of 100 Hz, there are still $80 \mu\text{s}$ for the feedback loop to settle. A single pole system with a crossover frequency of 100 KHz will settle with a time constant of $10 \mu\text{s}$. Adding a pole at the crossover frequency will actually improve the settling time as long as the phase margin does not get worse than 45 degrees. So the feedback loop should have enough time to settle. For these reasons, the second option was chosen for the design of the feedback loop. With this choice, the feedback loop should be stable and have an adequate settling time.

The other principal requirement is that our feedback loop provide good control over the output of the OLED. If the feedback loop has a forward transfer function of $A(s)$ and feedback transfer function $G(s)$, then the closed loop transfer function is

$$H(s) = \frac{A(s)}{1 + G(s)A(s)} \quad (3.4)$$

$A(s)$ includes the transfer function of the OLED, which is expected to vary from device to device and degrade over time. $G(s)$ represents our sensor network and feedback circuit. The transfer function of the feedback circuit should be well known. Ideally, each sensor would have the same response to the light emitted by the locally positioned OLED, though this may prove not to be the case. However, the response of the sensor will not change over time and we can determine $G(s)$ by measuring it for any given pixel and calibrate the display accordingly.

To function as a display, the light output from the OLED does not need to track a rapidly fluctuating input voltage. Given a fixed input voltage, the OLED needs to settle at a predictable light output within the allotted time slot before the array

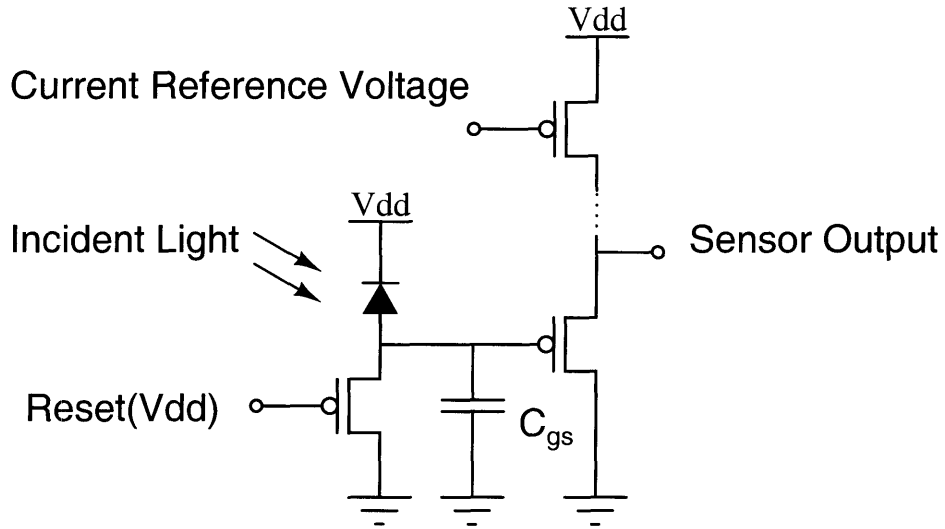


Figure 3-3: A simple circuit model of the sensor output

switches the feedback loop on to the next pixel row. For this proportional control $H(s)$ must be constant with respect to s at low frequencies and well known. If for small s , $A(s)G(s) \gg 1$, $H(s) \approx 1/G(s)$. Then if $G(s)$ is constant and well known at low frequencies, the condition will be satisfied.

Given this requirement, our sensor presents us with our second design constraint. In order to satisfy the conditions on $G(s)$, the feedback loop must compensate for the transfer function of the sensor. The light incident on the photo diode is proportional to the current through the diode. But that current is integrated by the capacitance on the gate of our source follower buffer. So the output voltage of the sensor is proportional to the integral of the light incident on our diode.

$$V_{out} = \int \frac{I_{diode}(t)}{C_{gs}} dt \quad (3.5)$$

Since $H(s) \approx 1/G(s)$, if $G(s)$ contains an integrator, then $H(s)$ will contain a differentiator. Then the light intensity will be proportional to the rate of change of input voltage. This is not the proportional control we are looking for. $1/G(s)$ must be constant for small s so that the system can generate a predictable light output for a given input voltage. Thus, the feedback loop must include a differentiator to cancel this integrator.

Lastly, the DC gain of the system must be large enough to insure that the approximation, $H(s) = 1/G(s)$ is a good one. In actuality,

$$H(s) = \frac{A(s)}{1 + G(s)A(s)} \quad (3.6)$$

When the open loop gain, $A(s)G(s)$, is much larger than unity we get

$$H(s) = \frac{1}{G(s)} \left(1 - \frac{1}{A(s)G(s)} \right) \quad (3.7)$$

If $G(s)$ is known, the output $H(s)$ can be predicted to the accuracy of the lower bound of the inverse of $A(s)G(s)$. If this value is greater than, for example, 500, we will get 9 bits of accuracy and the accuracy will likely be limited by the precision of our sensor, not the feedback control. Furthermore, suppose the performance of the OLEDs does vary. Let $A(s) = \alpha A'(s)$ and $\alpha = 1 + \epsilon$. If ϵ is small compared to unity, then

$$H(s) = \frac{1}{G(s)} \left(1 - \frac{1 - \epsilon}{A'(s)G(s)} \right) \quad (3.8)$$

$$\Delta H(s) = \frac{1}{G(s)} \left(\frac{\epsilon}{A'(s)G(s)} \right) \quad (3.9)$$

The matching between devices is then related to the variation term ϵ divided by the open loop gain.

As the OLEDs age, $A(s)$ will get smaller. Then we have

$$H(s) = \frac{1}{G(s)} \left(1 - \frac{1}{\alpha A'(s)G(s)} \right) \quad (3.10)$$

As α drops, our control will be reduced. However, if our DC gain is 1000 and α drops to 0.1, which would correspond to a drop in OLED efficiency by an order of magnitude, the output will still be accurate to within 1 percent. This suggest that a DC gain of 1000 should be enough to observe the benefits of feedback control. Larger would be better, but an increased DC gain would require shifting the dominant pole to an even lower frequency. This can be difficult on an integrated chip.

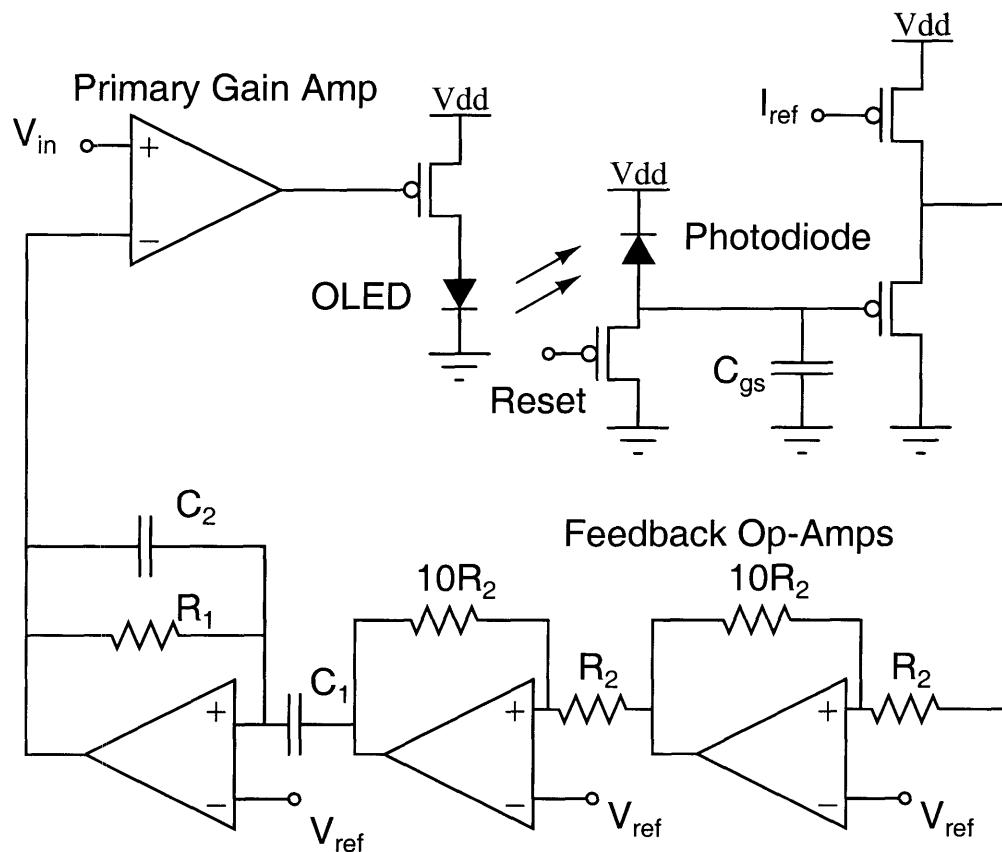


Figure 3-4: The circuit model of the feedback loop

3.1.2 Loop Parameters

The feedback loop is shown in Figure 3-4. The actual circuit uses switched capacitor filters instead of resistors, but the transfer function was designed to match. The op-amp operating in open loop has a gain of roughly 1000 with a cross over frequency of 100 KHz. The rest of the feedback loop is designed to have a gain of at most 1 with any parasitic poles occurring well above 100 kHz. The gain from the voltage on the gate of the transistor driving the OLED to the current out of the photodiode was estimated based on the g_m of the transistor at the expected current drive, the observed efficiency of the OLEDs and the estimated efficiency of the photodiode detector. The gain from the current out of the photodiode to the output of the differentiator is $R_1 C_1 / C_{gs}$. The last two gain stages together have a gain of 100. If the OLED and photodiode operate at the upper range of their approximated gain, then the open

Table 3.2: Device Values

Component	Value
C1	4 pF
C2	1 pF
R1	100 K
R2	300 K

loop transfer function of the overall feedback loop will have a cross over frequency of 100 kHz and the loop will be stable. If the gain is less, the cross over frequency will be less than 100 kHz so the loop will still be stable. Of course, this will also mean the system settles more slowly. If our settling time is too long, the display will have an unacceptably slow refresh rate. However, it is better to have a slow refresh rate than an unstable feedback loop. In estimating the gain, it is best to insure stability and worry about improving settling time in later design iterations after the response time and gain of the pixel is better understood.

In terms of the actual design process, knowing that some feedback compensation would be necessary, I made a first pass at designing the feedback op-amp and observed that a gain-bandwidth product of roughly 100 MHz was achievable. Then I designed the compensation network knowing the requirements the feedback loop as a whole placed on the compensation network but also the likely limitations of the op-amp I would be using.

C_1 is chosen to be as large as is reasonable given layout area constraints. This reduces the gain requirement for the rest of the feedback loop. To stabilize the differentiator circuit itself, a capacitor, C_2 , is included in the differentiator's feedback loop so that the gain levels off at 1 MHz. This will appear as a pole in the feedback loop's transfer function at 1 MHz- well above our 100 kHz cross over frequency. Two additional gain stages were included with a gain of 10 each. If the gain bandwidth product of the op amps used is greater than 10 MHz, then the poles generated by those stages of the feedback loop will be greater than 1 MHz.

3.1.3 Behavioral Modeling

The feedback loop was initially simulated in Matlab using simple block diagrams representing the principal poles and zeroes in the loop. Varying the position of the pole generated by the RC time constant of the OLED from 30 kHz to 300 kHz, the loop was verified to be stable for a range of OLED response times. Settling time varied from 30-50 microseconds.

The feedback loop was later simulated in HSPICE using op amps with resistors in the feedback path. This allows the simulation to incorporate parasitic poles generated by the finite gain bandwidth product of the op amps without requiring time consuming transient analysis. In the simulation with op amps and resistors, the feedback loop was again found to be stable for a range of OLED response times.

3.2 Op-Amp Design

The two basic functions that op-amps perform in the feedback loop require the design of two different op-amps. The requirements for each op-amp are similar, however, so it was possible to design both op-amps with the same topology, but different device parameters.

3.2.1 Topology

A two stage op-amp with an output stage was chosen chiefly for its simplicity. The only specific constraint is bandwidth. The Miller-multiplied capacitor appearing in the common-source amplifier stage of a two stage op-amp allows us good control over the bandwidth and cross-over frequency of an op-amp.

Principal secondary concerns are offset voltage, power consumption, noise and slew rate. Basically, power consumption, offset voltage and noise should be minimized while maintaining a sufficient slew rate. Noise in a two stage amp is minimized by proper device sizing in the input stage. The current in the final leg of the amplifier effectively determines the amp's slew rate. Increasing it improves the slew rate. How-

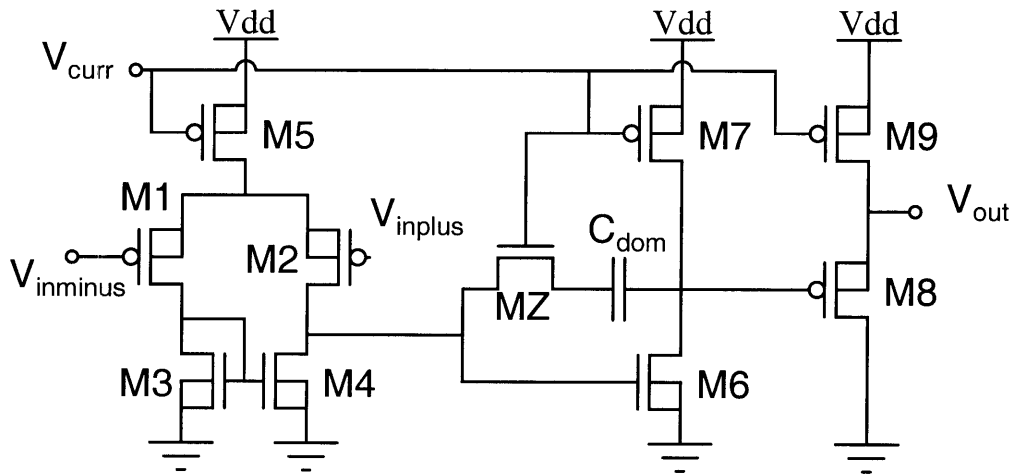


Figure 3-5: Two stage with output stage op-amp topology

ever, minimizing power consumption requires there only be one such higher current stage.

In a two stage amp, however, a gross current mismatch between the legs forces odd device sizing to keep the voltage offset low. This may include using non minimal transistor lengths, which tends to reduce the bandwidth of the amp and is thus undesirable.

At a minimum cost in area we can include an output stage. Then we have three power-consuming current legs, but two of them are low current, so the increase in power consumption is minimal. Device sizes can be adjusted to give effectively zero systematic offset voltage in simulation. Of course, in reality, device mismatch from fabrication will generate some offset that is then determined by the degree of mismatch and the open loop gain. The output stage has the additional benefit of providing a lower output resistance. This will help avoid generating a pole at a low frequency if we operate the op-amp in closed loop with a capacitor in the feedback loop.

3.2.2 Primary Gain Op-Amp

The primary gain op-amp is intended to provide the DC gain for the feedback loop as a whole and to set the cross over frequency for the system by introducing a low frequency pole. Glancing at the schematic, this op-amp appears to be operating open

Table 3.3: Primary gain amp design values

Transistor	Length(μm)	Width(μm)
M1, M2	5.6	0.7
M3, M4	1.4	0.7
M5	0.35	0.8
MZ	2.8	0.7
M6	0.35	1.4
M7	0.35	0.8
M8, M9	0.35	3.2

loop. In actuality, the feedback loop for the op-amp is the overall feedback network.

To decide on device sizes I started with minimum device sizes and adjusted as was appropriate. The reference voltage is intended to generate 1 μA of current through M5. The noise will increase as you decrease the current. Additionally, at lower current g_m is reduced, causing secondary parasitic poles to be more likely a problem. On the balance, 1 μA will be small compared to the 5-8 μA that will be running through the output current leg. Increasing the bias current will cause the op-amp to consume significantly more power. Further decreasing the current will not substantially reduce the power consumption of the op-amp but may lead to other problems.

The primary gain op-amp is designed to generate the needed open loop gain. A two stage op-amp should have a gain that is roughly $(g_m r_{out})^2$. This should be enough to give us the desired DC gain of about 1000. The precise gain is not particularly important so the device values were not chosen with it in mind. However, the cross-over frequency of the primary gain op-amp must be controlled carefully. Assuming the Miller multiplied capacitor generates a dominant pole capacitor, hand analysis gives the following important op-amp equations:

$$A_{dm} = g_{m6}(r_{o6}||r_{o7})\frac{g_{m1} + g_{m2}}{2}(r_{o2}||r_{o4}), \quad g_{m1} = g_{m2}$$

$$f_c = A_{dm}f_{3dB}, \quad f_{3dB} = \frac{1}{2\pi RC}$$

$$C = C_{dom}g_{m6}(r_{o6}||r_{o7}), \quad R = r_{o2}||r_{o4}$$

$$f_c = \frac{g_{m1}}{2\pi C_{dom}} \quad g_{m1} = \sqrt{2(W/L)\mu_p C_{ox} I_d}$$

Given that f_c must be 100 kHz, it is probable that a large C_{dom} will be necessary. However, there will be one feedback loop per column of any display. With a desired pitch of 30-50 microns, large, space-consuming capacitors should be avoided. Instead of increasing C_{dom} further, it is possible to reduce g_{m1} instead. The width is already the minimum size. It is also undesirable to reduce the current any further, in this case, because charging and discharging C_{dom} could prove to be the limiting factor in the slew rate of the op-amp. But lengthening the transistors can also reduce g_{m1} . You can approximate the chip area required for the desired cross-over frequency.

$$f_c = \frac{g_m r_o A_v}{2\pi r_o C}$$

expanding and grouping terms,

$$f_c = \alpha \frac{g_m}{C} = \frac{\alpha}{C} \sqrt{2I_d(W/L)\mu_n C_{ox}} = \frac{\beta}{C\sqrt{L}}$$

$$L = \frac{\gamma}{C^2} \tag{3.11}$$

Equation 3.11 describes the relationship between the length of the transistors in the input stage and the compensation capacitor required to keep the cross-over frequency constant. You can increase C , but then you would have to decrease L , and vice versa. We can use this relationship to determine the C and L that will minimize our area in layout. The answer is independent of the constant factor γ , which is why it is unimportant. Based on the general layout chosen, let the area taken up by the transistors be given as aL and bC be the area consumed by the compensation cap. Both of these are assumed to scale linearly with L and C , as one would expect. Since L and C are related, we can express one in terms of the other.

$$\text{Area} = aL + bC = a\frac{\gamma}{C^2} + bC$$

$$\frac{d \text{ Area}}{d C} = b - \frac{2a\gamma}{C^3} = 0$$

$$C = \sqrt[3]{\frac{2a\gamma}{b}}, \quad L = \sqrt[3]{\frac{b^2\gamma^2}{4a^2}}$$

$$2aL = \sqrt[3]{2ab^2\gamma} = bC \quad (3.12)$$

As can be seen by our result in equation 3.12, it doesn't matter what the constants a and b actually are. But if you minimize the area with respect to the capacitance, you will find that the contribution to the area from the device lengths should be half that of the contribution from the capacitance. So in any given process or layout configuration you can optimize this without too much trouble by at least approximating those constants. In our case, M1 and M2 are longer devices and their specific lengths were determined by the op-amp bandwidth requirement and the layout configuration I chose.

Now the gain of the first stage is $g_{m2}(r_{o2}||r_{o4})$. Since $r_o = 1/(\lambda I_d)$ and $\lambda \propto 1/L$, $r_o \propto L/I_d$. Thus, as we increase the length of M1, g_{m1} decreases, but r_{o1} increases. To maintain the desired DC gain in the op-amp, it is necessary to increase the lengths of M3 and M4 as well, so that r_{o4} increases with r_{o1} and the DC gain remains high.

The DC gain of the op-amp is also related to the gain of the common source amplifier stage. The gain of this stage was maximized by using the minimum current ($1\mu\text{A}$). The width of M6 was adjusted so the voltage needed on the gate of M6 to avoid railing the output of the op-amp was matched to the voltage provided by the first stage. We can approximate this using hand analysis and comparing the current through M4 and M6. Assume that since the current through M3 and M4 are the same and $V_{gs} = V_{ds}$ for M3, the same holds for M4. Then if $I_{d4}(L_4/W_4) = I_{d6}(L_6/W_6)$, V_{ds} for M6 shouldn't have to rail one way or the other to supply the necessary current through M6. However, variations in V_t , the actual voltage present on the drain of M4, and the actual currents in the two legs prevents our hand analysis from matching HSPICE results in this case. The relationship $I_{d6} \propto W_6/L_6$ for a fixed V_{gs} is still useful with the aid of HSPICE in finding a width that minimizes the op-amp's offset.

The output stage is simply designed to carry a slightly higher current to drive larger output loads. The primary driver amplifier has to drive the entire column of pixels beneath it which will include a lot of parasitic capacitances.

Finally, a two stage op-amp using a Miller compensation cap will have a zero at $s = \frac{g_{m6}}{2\pi C_{dom}}$. By adding a series resistance, we can move this zero to $s = \frac{g_{m6}-1/R}{2\pi C_{dom}}$. MZ is sized and biased to generate a resistance to move this zero into the left half plane. The sizing and biasing are done almost entirely using HSPICE. The transistor is connected to the output of the first stage. The gain through the second stage is roughly 30. Thus the variation in the output of the first stage will be 30 times less than the output of the second stage and the bias conditions of the transistor will not be changing very much.

3.2.3 Feedback Op-Amp

Ignoring the contribution from the primary gain op-amp, the feedback loop should have unity gain with a flat frequency response. The topology is the same as for the driver amp, shown in Figure 3-5. The transfer function of the OLED driver and optical sensor will require additional gain and a differentiator. The feedback op-amp will be used in a few simple op-amp circuits to implement these functions.

Once the parameters of the compensation network were decided, I went back and finalized a design for an op-amp that would function in the feedback loop.

Using the design of the primary gain op amp as a starting point, I adjusted accordingly. First, the unity gain frequency of the op-amp needed to be maximized while maintaining closed loop, unity gain stability. So a large compensation capacitor and longer transistors were not needed. Furthermore, a two stage op-amp would easily have 60 dB of gain. That is enough so that the accuracy of the desired gain in closed loop is a function of the matching between the capacitors or resistors in the closed loop not the finite gain of the op-amp.

A current of 1 μ A was sufficient in the first two stages to push parasitic poles resulting from the capacitance on the gates of M3 and M4 or at the gate of M8 well beyond the 100 MHz crossover frequency of the amplifier. This is not surprising

Table 3.4: Feedback op-amp design values

Transistor	Length(μm)	Width(μm)
M1, M2	0.35	2.1
M3, M4	0.35	0.7
M5	0.35	0.8
MZ	11.2	0.7
M6	0.35	1.4
M7	0.35	0.8
M8, M9	0.35	3.2

because the equivalent resistance at those nodes is $1/g_{m3}$ and $1/g_{m6}$, respectively, which will be relatively small. The output of the op-amp may also be loaded with a capacitor because the op-amps will be connected with switched capacitor circuits. The output resistance of the op-amp is $1/g_{m8}$. By increasing the current and width of this device by a factor of 4, the output resistance is correspondingly decreased. This helps to insure that any pole generated by that output resistance and an output load capacitor will at frequency higher than the cross-over frequency of the amplifier. Moreover, the higher current will result in a higher slew rate, which is important for transient settling times in a switched capacitor circuit.

3.2.4 Op-Amp Simulations

Both op-amps were simulated using HSPICE. Since the design is for TSMC's 0.35 micron process, I used the libraries available in the CMC design kit. Using an open loop AC analysis with the output load the op-amp will be driving, it is possible to determine both the bandwidth and the phase margin of the op-amp. A closed loop AC analysis of the feedback op-amp can verify stability in the feedback configurations that the op-amps will be used in and that the desired transfer functions will be generated.

The driver op-amp needs to look like a single pole system. At its cross-over frequency of 81 kHz it has 91.3 degrees of phase delay as seen in Figure 3-6. At 100 kHz it has only a few more degrees of delay. Thus it has the desired cross-over frequency and appears as a single pole system in the frequency range of interest.

The stability of the feedback op amp is shown in Figure 3-7 with 68 degrees of phase margin. In closed loop with constant gain, the feedback op-amp should look like an inverter with 180 degrees of delay. At 100 kHz it has only one extra degree of delay as shown in Figure 3-8. As a differentiator, the feedback amp should have 90 degrees of delay. This is also the case; at 100kHz it has approximately 94 degrees of delay, as shown in Figure 3-9.

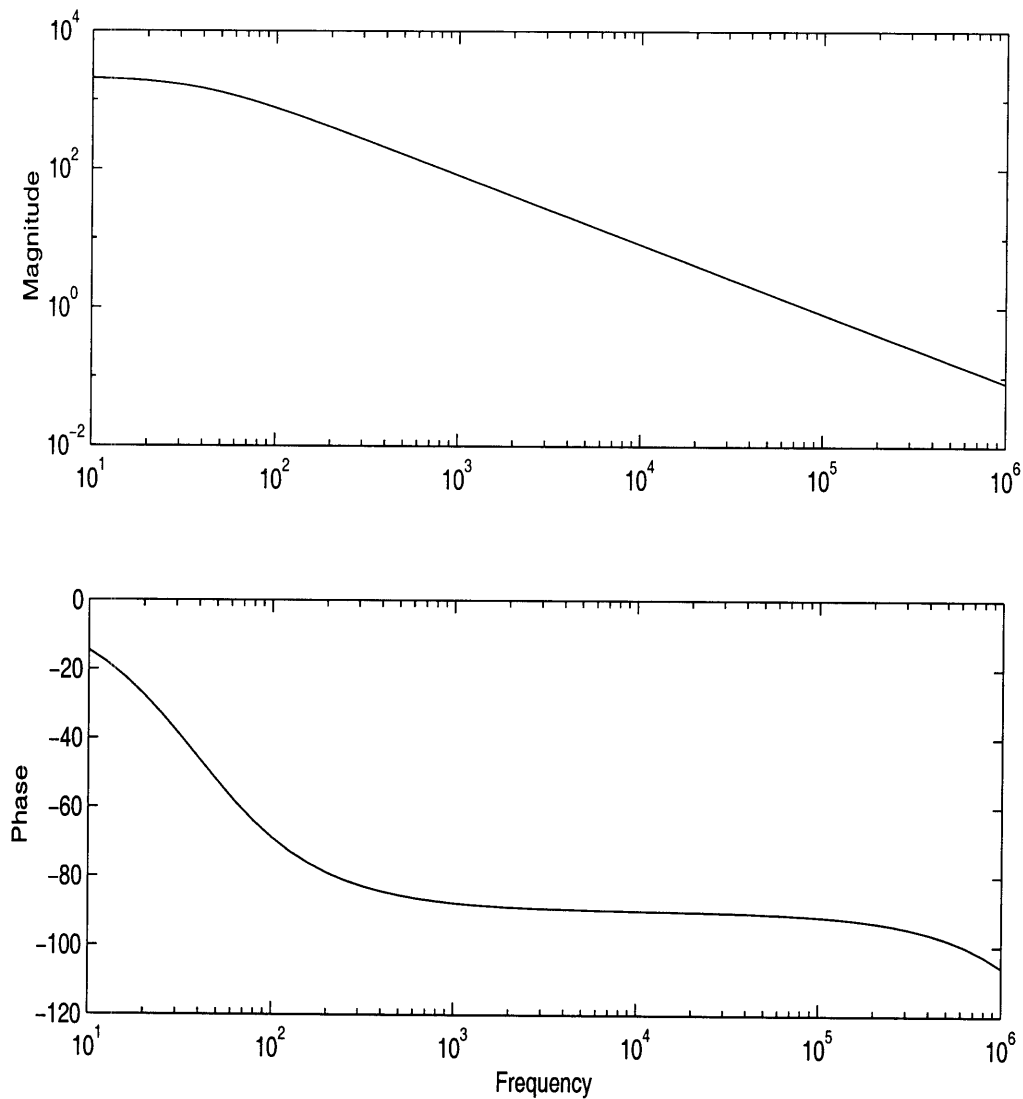


Figure 3-6: Bode plot of the driver op-amp in open loop

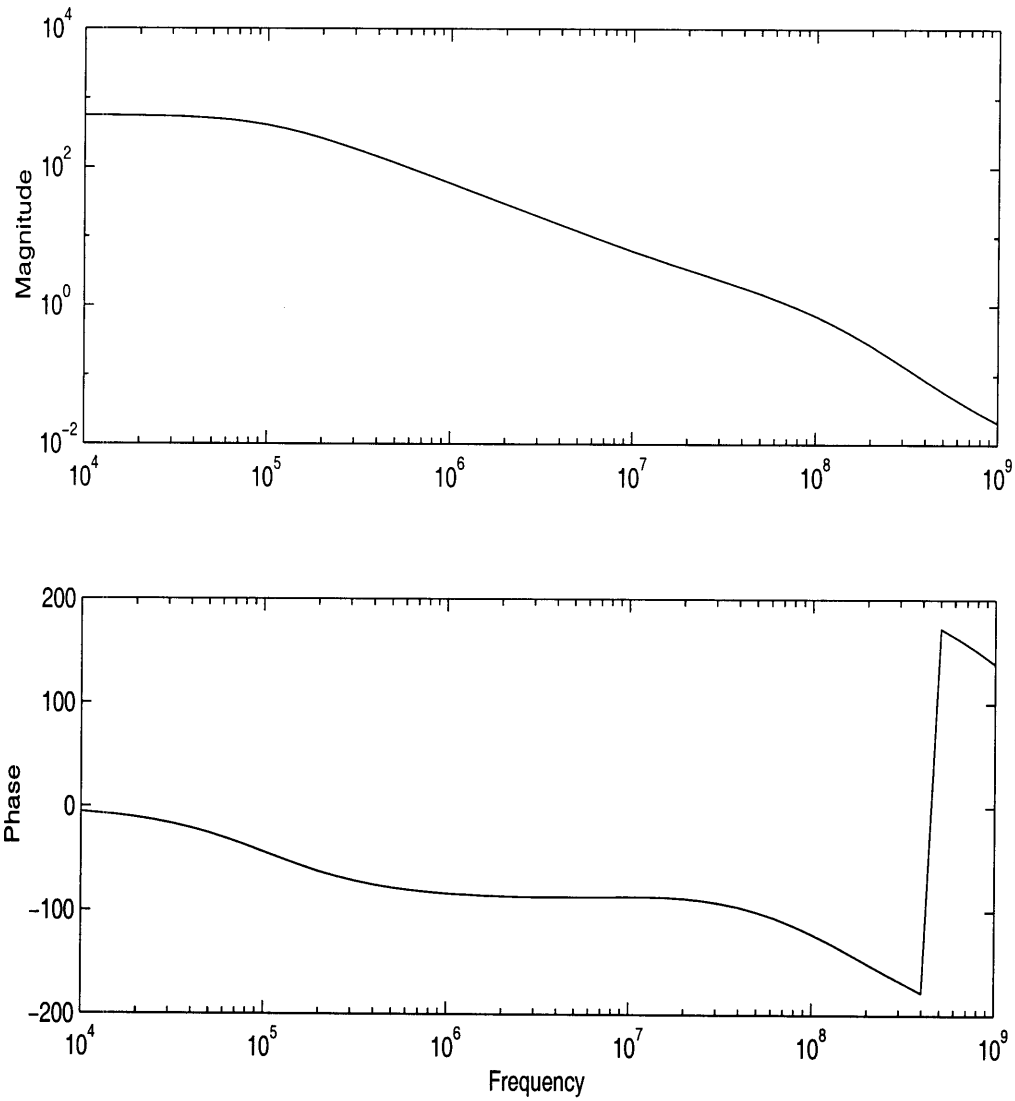


Figure 3-7: Bode plot of the feedback op-amp in open loop

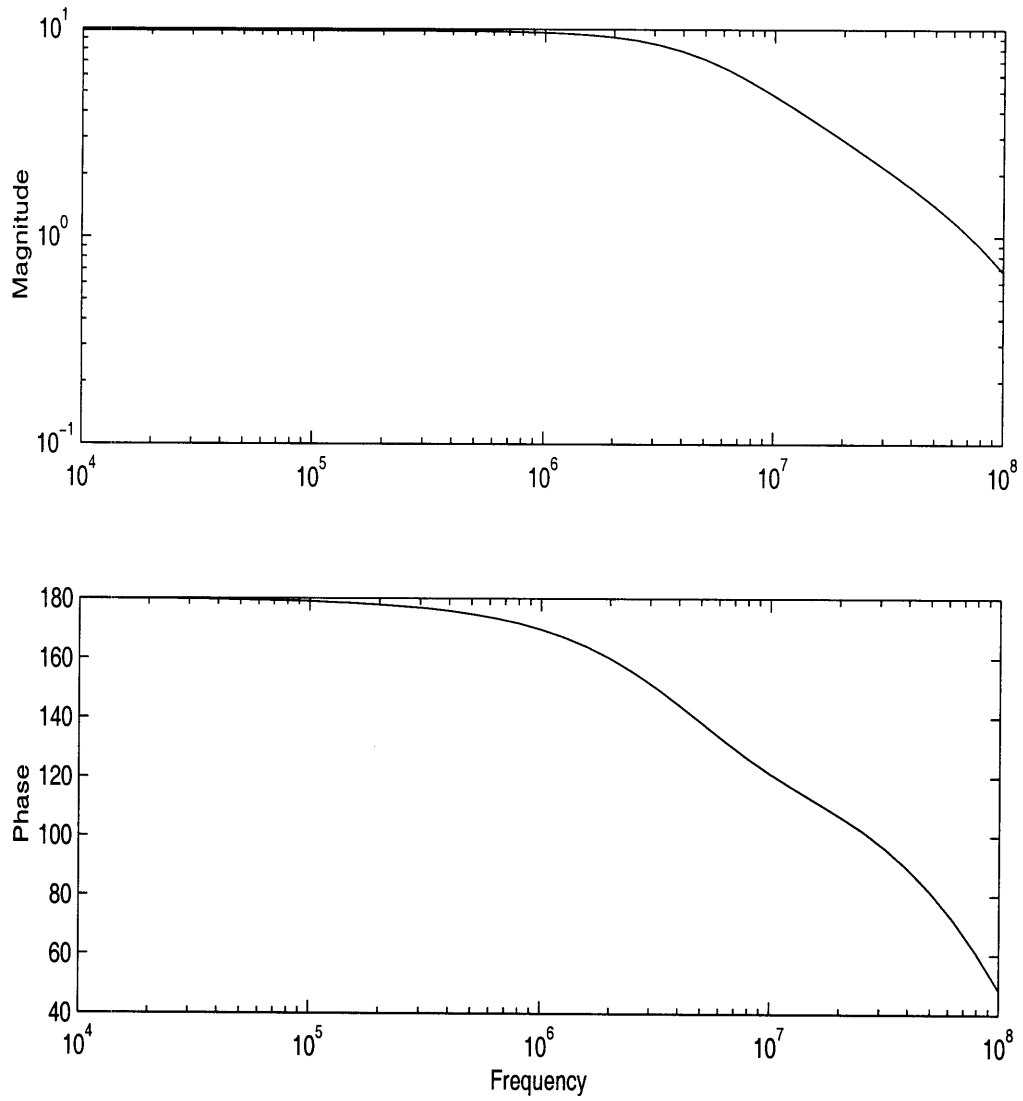


Figure 3-8: Bode plot of the feedback op-amp in closed loop with a constant gain

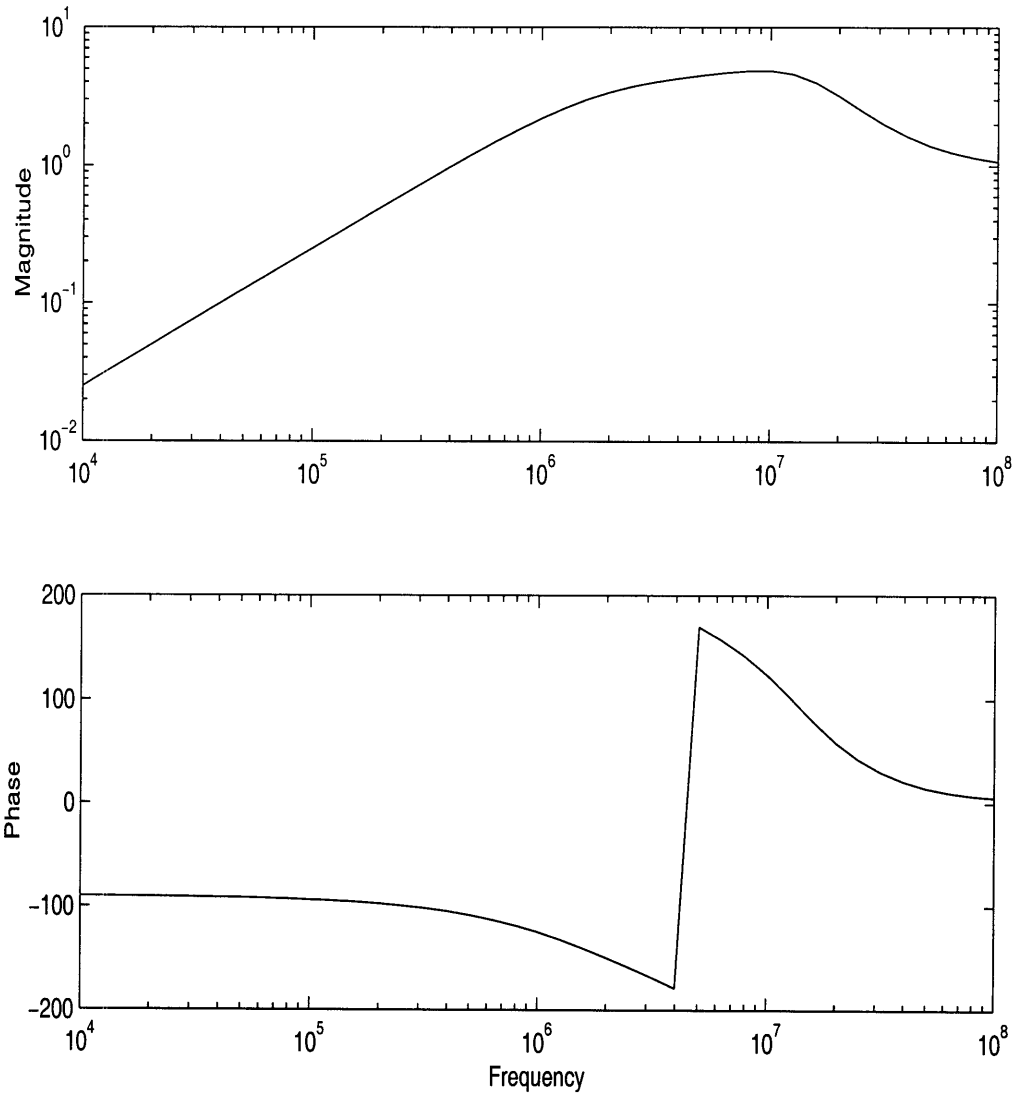


Figure 3-9: Bode plot of the feedback op-amp as a differentiator

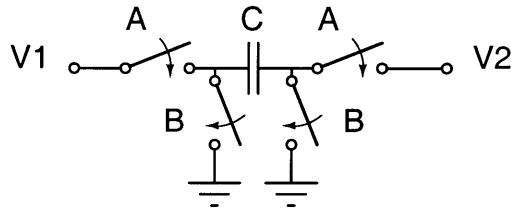


Figure 3-10: An example of a switched capacitor

3.3 Switched Capacitor Networks

Since it is very space consuming to have large poly resistors in CMOS, a switched capacitor filter is employed in the feedback loop. The capacitors also have the advantage of better matching over poly resistors. The basic idea is that charging a capacitor and then discharging it across two nodes will generate an effective resistance at signal frequencies that are small compared to the switching frequency.

3.3.1 Basic Switched Capacitors

The basic idea is shown in Figure 3-10. First, the two switches governed by B are open and those governed by A are shorted. The voltage across C results in an accumulated charge. Then the switches governed by A are opened and the switches to ground are shorted. The charge across the capacitor is dissipated through ground. If f is the switching frequency we have the following:

$$Q = (V1 - V2)C, \quad I = \frac{\delta Q}{\delta t}, \quad I = f(V1 - V2)C$$

$$R_{eff} = \frac{\delta V}{\delta I} = \frac{1}{fC} \quad (3.13)$$

In practice, the switches are replaced by transistors. One might hope to implement a switched capacitor network simply by replacing the resistors in the circuit with switched capacitors as shown in Figure 3-11. Unfortunately, it is not so simple. Assuming the presence of an ideal op-amp and ideal switches, there is nothing wrong with the circuit shown. However, when A is low and those transistors act as open cir-

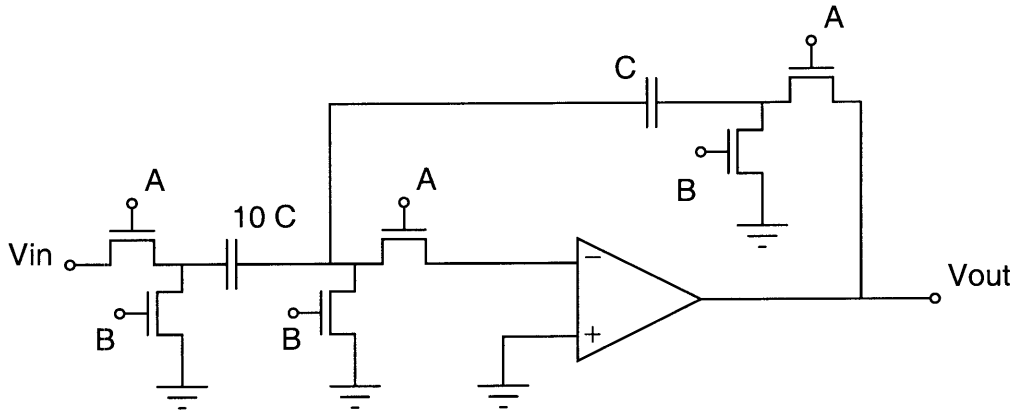


Figure 3-11: A naive switched capacitor circuit implementation

circuits, the op-amp will be operating in open loop. And when the transistor connected to the inverting input of the op-amp is closed, a small amount of channel charge will be injected onto the gate capacitance of the input. In open loop, this small voltage offset will generally be large enough to rail the output of the op-amp. This has two effects. First, the output will only be accurate while A is low. There are techniques to address that problem. But worse, when A goes high again, the op-amp's transient settling time will be limited by the slew rate of the amplifier. And with the output fully railed, that time will be considerable. Given that the cross-over frequency of the op-amp is 100 kHz, we need to insure that switching network has no adverse effect on the feedback loop transfer function at frequencies smaller than 100 kHz. Likely, a switching frequency of 3-10 MHz will be required. This would require the settling time to be substantially less than 100 ns. Without dissipating significant power, there is really no way to recover the output so quickly.

3.3.2 Actual implementation

Fortunately, an alternative approach does exist. Placing actual capacitors in parallel with the switched capacitors insures that the op-amp will never be in open loop. The schematic is shown in Figure 3-12. Charge will still be injected on the gate during each cycle, but the feedback will prevent the op-amp from saturating. Of course, adding capacitors should change the transfer function of the circuit. But actually, to

first order, it remains the same. In the inverting configuration used, let Z_1 denote the input impedance and Z_2 denote the feedback impedance.

$$V_{out} = -A_v V_m, \quad V_m = \frac{Z_2 V_{in} + Z_1 V_{out}}{Z_1 + Z_2}$$

$$\frac{V_{out}}{V_{in}} = \frac{A_v Z_2}{Z_1 + Z_2 + A_v Z_1} \quad (3.14)$$

$$\text{if } A_v Z_1 \gg Z_1 + Z_2, \text{ then } \frac{V_{out}}{V_{in}} = \frac{Z_2}{Z_1} \quad (3.15)$$

$$H_1(s) = \frac{1/(fC)}{1/(f10C)} = 10, \quad H_2(s) = \frac{1/(sC + fC)}{1/(s10C + f10C)} = 10 \quad \forall s \quad (3.16)$$

Thus, at lower frequencies where the assumption that the gain of the op-amp will be large is true, the transfer function will be unchanged. Given that our op-amps have a gain-bandwidth product of 100 MHz, with a closed loop gain of 10, this should be true up to 10 MHz. At this point, one might wonder why we cannot just use the capacitors by themselves without the switched capacitors. The problem is that the inverting input to the op-amp will have no dc path to ground. That is, any charge on that node will have no opportunity to dissipate and a corresponding voltage offset will result. The switched capacitors allow us to dissipate any such charge.

However, an offset will still result from accumulated charge at the inverting input of the op-amp. Each clock cycle, additional charge will be injected at the inverted input as the transistor connected there switches off. We can approximate the output offset as a function of the charge, Q , injected during each cycle. If the input voltage remains fixed, then in steady state, any charge injected onto the input when A drops, will be removed when A is high. First, note that the simple capacitor connecting the output and inverting input, C_1 , is Miller-multiplied by the gain of the op-amp. Thus it is effectively substantially larger than the input capacitor. Any charge removed from the inverting input will be removed almost entirely from C_1 . Thus, a corresponding

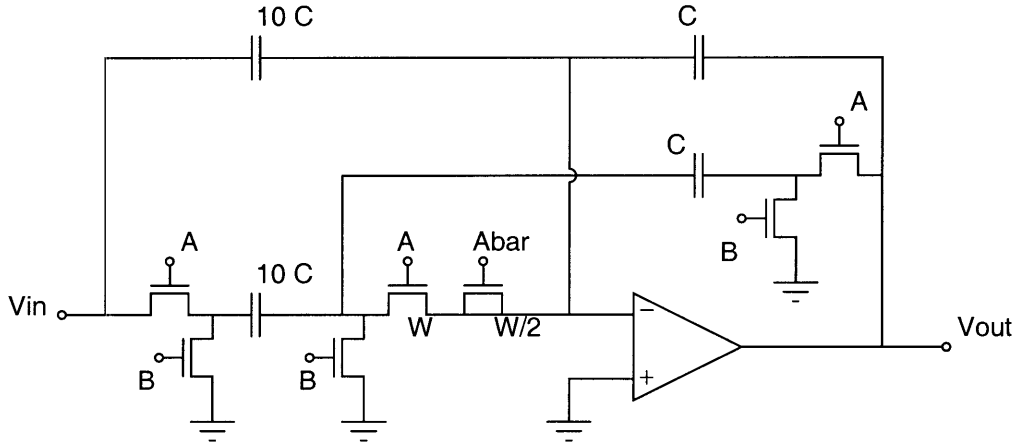


Figure 3-12: Actual switched capacitor circuit implementation

charge must be injected onto the other side of C_1 , at the output of the op-amp. If Q charge is injected onto the node as A drops, Q charge is removed when A rises. So Q charge is injected from the output onto C_1 . Since the inverting input and the non-inverting input will be close to equal in stable feedback, the output will simply be the voltage across C_1 , $V_{off} = Q/C_1$.

The big problem with this offset is that an offset in the first stage of our feedback loop will be multiplied by the following stage. This could rail the signal in the feedback loop, preventing the feedback loop from functioning. This offset can be minimized by increasing C or decreasing Q . The size of C_1 is sharply limited by the availability of area. At first pass, Q is minimized by decreasing the size of the transistor switches. Using minimum resistors, the Q was found in simulation to be roughly 3 fC. Suppose $C_1 = 100$ fA, then $V_{off} = 30$ mV. But if the first stage of our feedback loop has an offset of 30 mV, and that offset voltage is multiplied by 100, the signal will rail. So additional measures have to be taken.

We can actually further reduce Q by using a charge cancellation technique. A simple approach is to include a dummy switching transistor at our sensitive node whose drain and source are shorted to the node. Its width should be one half the width of our actual switching transistor. The theory is that approximately half the channel charge of our switch transistor gets dumped on our sensitive node. The gate of the dummy transistor is attached to an inverted version of the switching signal.

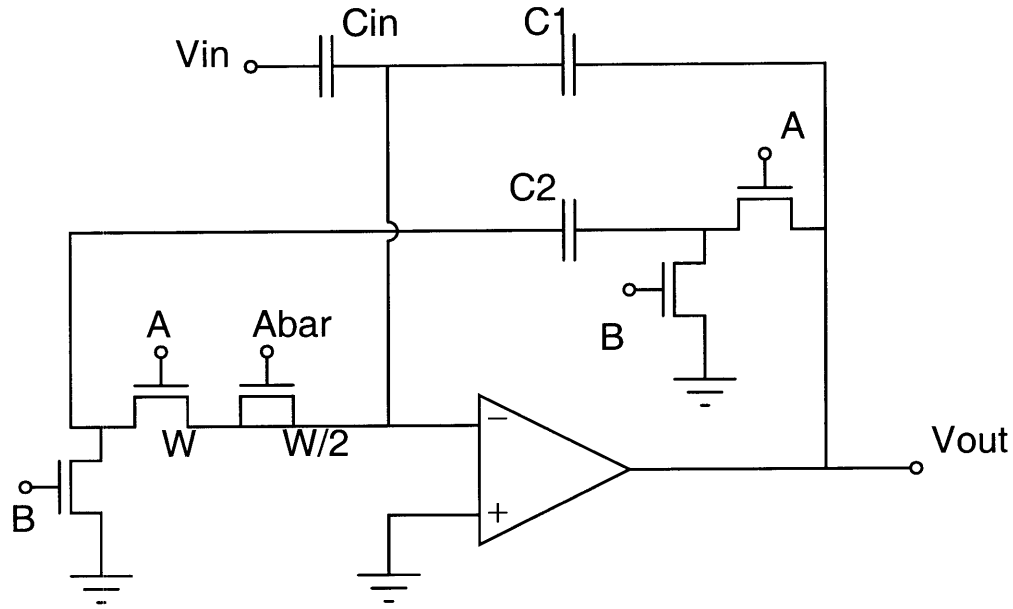


Figure 3-13: Differentiator Switched Capacitor Network

When the switch transistor turns off, the dummy transistor turns on, drawing charge from the sensitive node to fill its channel. Ideally, this would identically match the charge dumped from the real switch. In practice, we can expect Q to be reduced by a factor of 10. This will substantially reduce our output offset. The final circuit for a constant gain stage is shown in Figure 3-12. The differentiator is shown in Figure 3-13.

In addition to using charge cancellation, our feedback loop includes a differentiator. Any DC offset at the input of a differentiator will be blocked because the gain of a differentiator will be zero. Thus, we can move the differentiator to the end of our feedback loop. Then the maximum offset in the feedback loop is the offset in the first stage multiplied by the gain in the second stage (10). And the offset at the input to the primary gain op-amp is only the offset from the differentiator. With this circuit configuration, the offset will be kept sufficiently small.

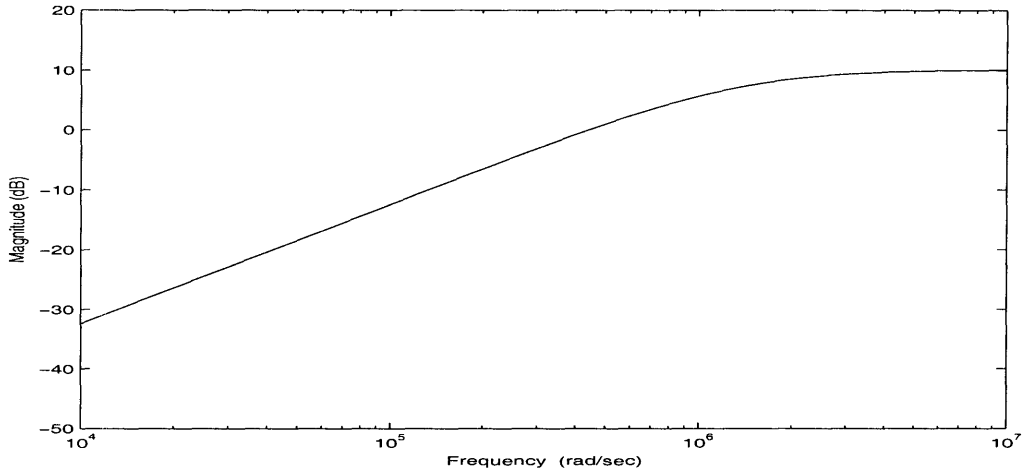


Figure 3-14: Magnitude Frequency Response of Differentiator

3.3.3 Switched Capacitor Simulations

Switched capacitor networks are difficult to test in a circuit simulator because standard AC analysis is not applicable. The transistors switching on and off can not be modeled as linear elements. First, the differentiator is simulated in Matlab assuming perfect switches and a finite gain op-amp. The results are shown in Figure 3-14 and 3-15. Notice the approximately 90 degrees of phase delay at 100 kHz.

To test the effect of real switches it is necessary to run transient simulations in HSPICE. The input to the differentiator is a 200mV peak-to-peak 10 kHz sine wave. The output is shown in Figure 3-16. The output is delayed by 90 degrees as we would expect from a differentiator. The output has a lot of high frequency noise on it from all the switching. Fortunately, both the OLEDs and the human eye filters noise above 1 MHz. The input to the constant gain stage is a 20 mV peak-to-peak 100 KHz sine wave. The output is shown in Figure 3-17. The output is an inverted 200 mV wave with no phase delay. Since the time scale is smaller, the switching noise is more noticeable for the DC gain stage. Also, notice the DC offset. Without using charge cancellation the offset would be unacceptable. The simulation verifies that our stage has a gain of 10 and that any pole occurs well above 100 kHz.

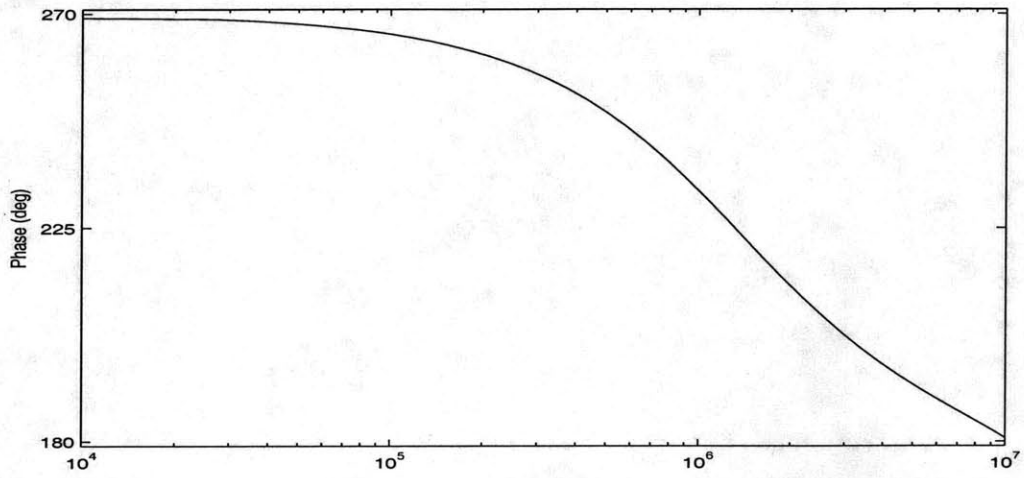


Figure 3-15: Phase Frequency Response of Differentiator

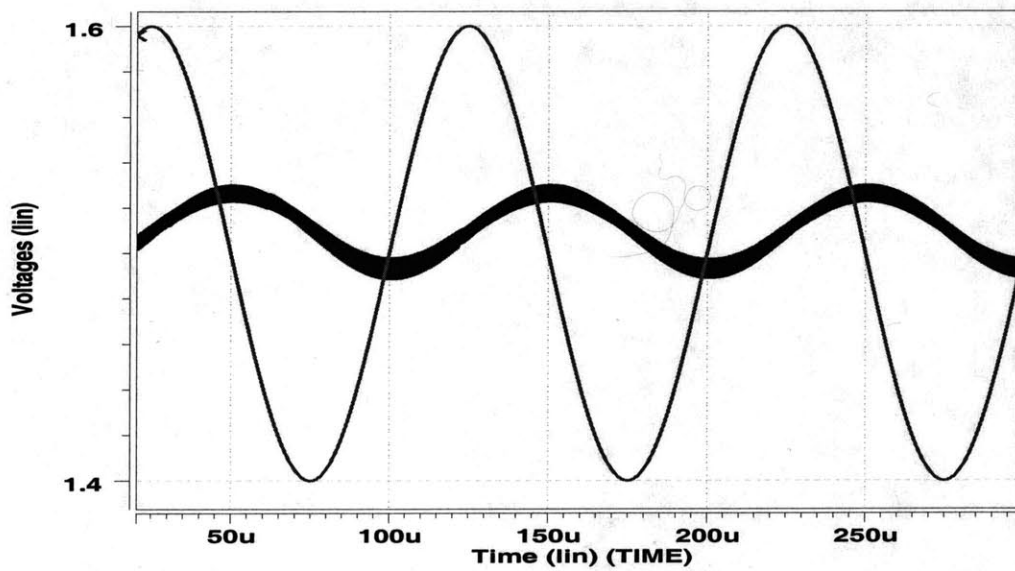


Figure 3-16: Transient simulation of the switched capacitor differentiator

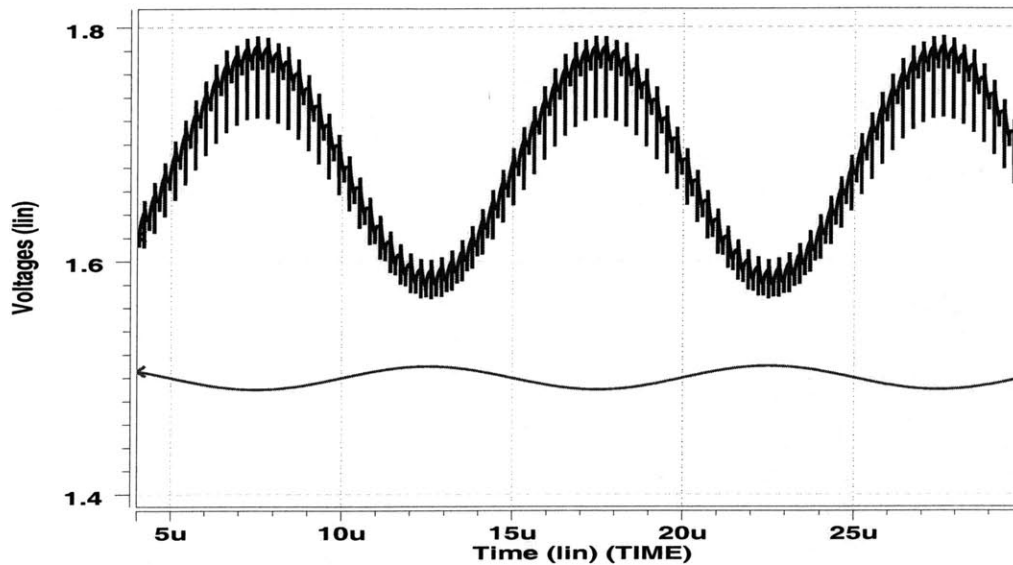


Figure 3-17: Transient simulation of the switched capacitor constant gain stage

3.4 Row Addressing

The system is designed so that there is a feedback loop for each column, and they all operate on one row at the time. There is a set of four digital signals for each row that control when that row is connected to the feedback loop. Each signal has a default value for when that row is not selected. When one desires to set the optical output from a given row, a 7-bit address corresponding to that row is sent to the chip. Then the digital control signals for that row must be set according to four corresponding signals sent to the chip. This setup allows fine tuned control of the control signal timing from off chip.

To address the rows, a simple approach would be to have the 7 address bits and their inverse sent to every row. Then each row would digitally AND the 7 bits corresponding to that row, producing a signal that was logically 1 if and only if that row was being addressed. However, this would require either a large 7-input AND gate, or multiple smaller gates. But the rows have a pitch of 30 microns and it could be difficult to fit a large digital gate into the space for each row.

Instead, I chose to use a scheme that includes pre-processing of the address, and combines the rows into groups of four, reducing the area needed at each individual

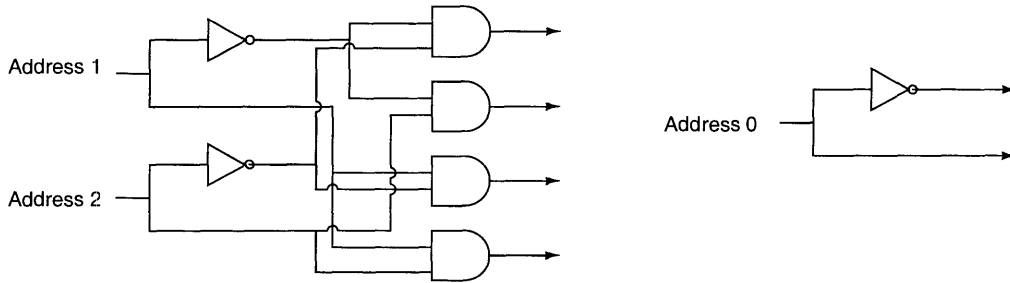


Figure 3-18: Address preprocessing circuits

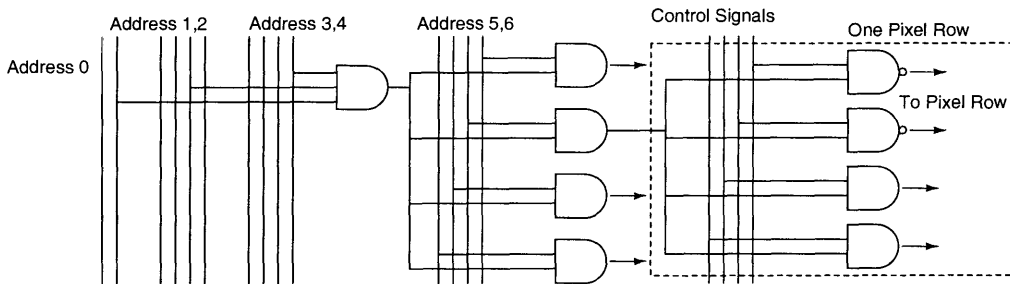


Figure 3-19: Row Addressing Circuit

row. First, the address is pre-processed by grouping the address into 3 groups of 2 and one individual bit. Then for each group, a control line representing each logical possibility for the group is run down the side of the pixel array. For example, a group of two bits will have four lines, corresponding to the logical values 00, 01, 10 and 11. Only one of these lines will be high for any given address input.

Secondly, for each group of 4 rows we first consider address bits 0-4. These correspond to three different groups. From each group, we take one logical value. The three values are combined in a 3-input AND gate. Then the last two bits of the address are considered. For each row in our group of 4, a different logical value is combined in a two input AND gate with the output from our 3-input AND. Call this output *rowselect*.

For any given address, only one row will have *rowselect* be logically high. This value is then combined with each control signal in 4 2-input AND gates. Depending on the default value for the control signal, the output is inverted or not before being sent down the row to the pixels.

The 4 2-input AND gates are unavoidable. However, this scheme uses only one

additional 2-input AND gate for each row and one 3-input AND gate for every four rows. So it should be easy to fit all the gates into the pitch of the rows. Additionally, you would need at the very minimum, 7 address lines running down the side of the pixel array for row addressing. This scheme requires 14 lines and a small amount of pre-processing circuitry at the top of the array.

3.5 Control Signal Timing

The four control signals which govern the operation of each pixel. The first two, OLED and $\overline{\text{OLED}}$ control the input to the pixel driving transistor. One is simply the inverse of the other and operates the dummy transistor that is used to reduce the charge injection. The third signal RESET is normally on to pull the gate voltage on the source follower output down to ground while the pixel is not connected in feedback mode. When the signal turns off, the voltage is able to slowly charge back up while the pixel is in feedback mode and current through the photo diode is deposited on the gate. The fourth signal, SENSOR, switches the output from the sensor into the main feedback path.

The switching time is not particularly crucial for any of these signals, but their relative timing is fairly important. In order to reduce large transients in the feedback path and to insure the correct voltage is left on the gate of the pixel driving transistor at the end of the cycle, the correct timing must be observed.

The first and last signal to switch should be the RESET signal. The feedback loop cannot function properly while it is turned on and there is no harm in turning it off early and turning it on again late. Secondly, the SENSOR signal should be switched on so that the feedback path can begin to settle based on the current OLED output, which should be close to what it is already supposed to be. Last, the OLED and $\overline{\text{OLED}}$ signals should connect the input of the pixel to the main driver line.

At the end of the cycle, it is critical that OLED switch off first so that the right voltage is held on the gate of the transistor driving the pixel. $\overline{\text{OLED}}$ should switch at the same time to minimize the charge injection on the gate. Second, the

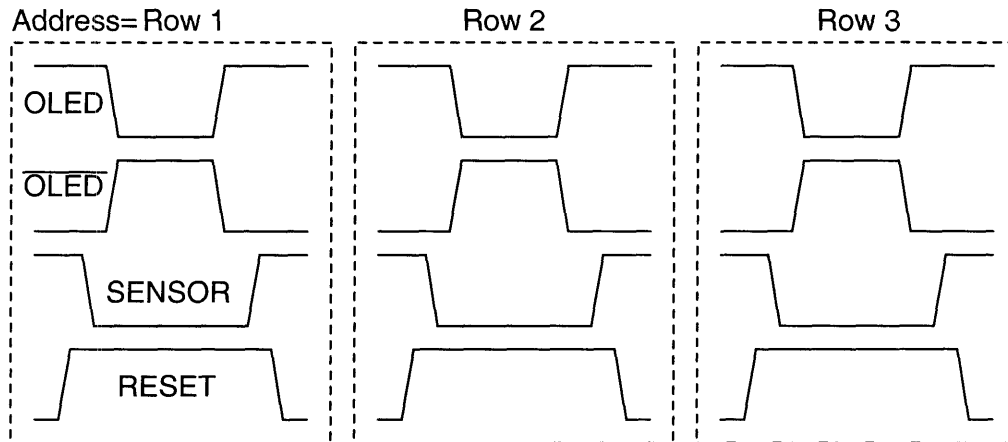


Figure 3-20: Control signal timing diagram for 3 consecutive rows

SENSOR signal can safely disconnect the pixel from the feedback loop. And finally, the RESET signal can be turned on again without introducing unnecessary transients in the feedback path.

Since these signals are controlling PMOS transistor switches, a logical zero corresponds to an analog value of vdd while a logical one corresponds to an analog value of ground.

In addressing the entire pixel array, each cycle of the control signals addresses a different pixel row. Thus the control signal inputs will essentially be digital signals with varying duty cycle and phase. For each cycle/row the correct address must first be entered, the correct control signals set and the correct analog values asserted for each column. The analog values must be held until the end of the cycle, when the control signals switch the pixel row out of the feedback loop and the address changes, moving on to the next row.

Going through the entire array, a different analog value may be asserted for each pixel. To generate an image, you would assert the same values for each pixel each time through the array. To generate a changing image, you can change pixel values each time the array is refreshed.

3.5.1 Layout

The layout was done in TSMC's 0.35 micron process. The pixel array dominates the layout. The feedback control loops are situated above and below the array. The dominant constraint in their layout is matching the pitch of the pixel array. The digital address circuitry runs along the side of the array, also matching the pitch of the array.

The pixel layout is as tight as possible to allow for a small pixel area. The transistors are clustered in one corner. The pad to contact the OLED rests above the transistors and the capacitor that stores the charge at the gate of the OLED driving transistor. The photo diode is shaped in a backwards L around the pad contact. Since the metal pad is not transparent, there is no point to having the diode under the metal layer.

The pads to electrically contact the chip are only allowed on the left side and top. This is due to concerns with regard to the OLED processing stage. There is also an additional pad which runs along the left side of the array and across the top. This is to contact the bottom side of the OLEDs during the OLED processing stage. The very bottom of the chip allows for extra pads since our layout is pad limited. The extra chip area is taken up with extra metal and poly structures to meet fill requirements. The chip dimensions are roughly 6mm by 1mm.

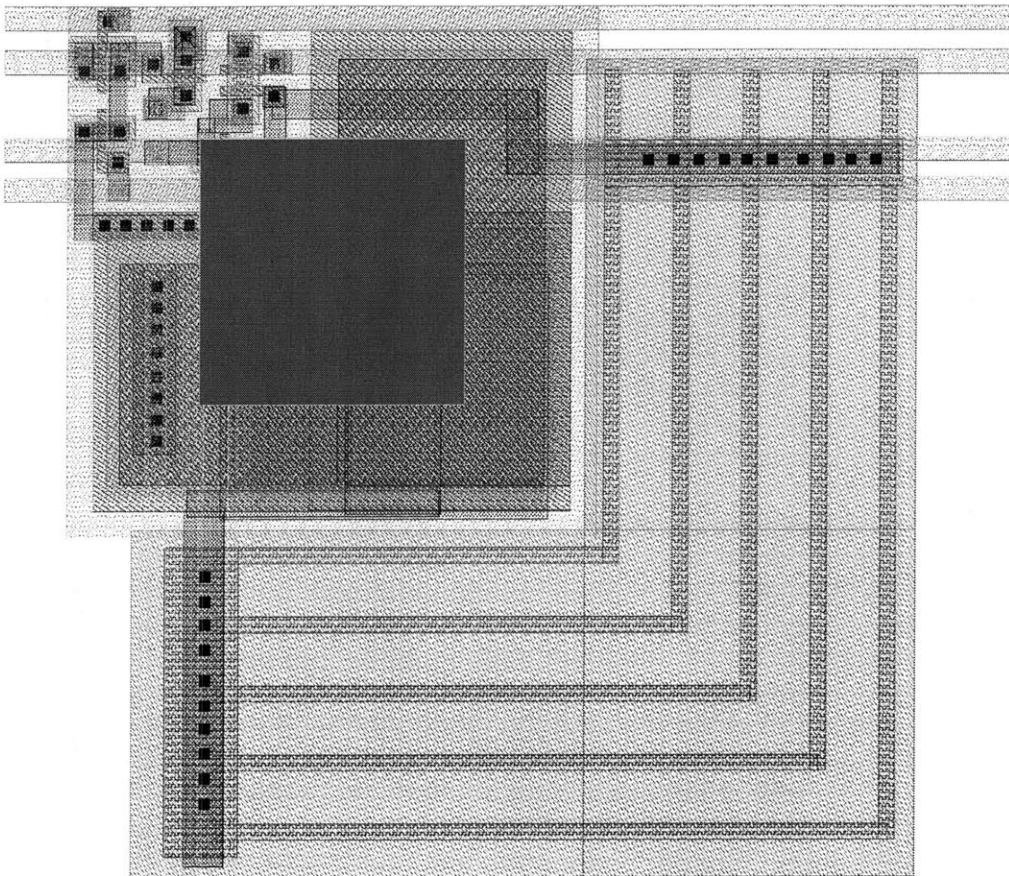


Figure 3-21: Pixel layout

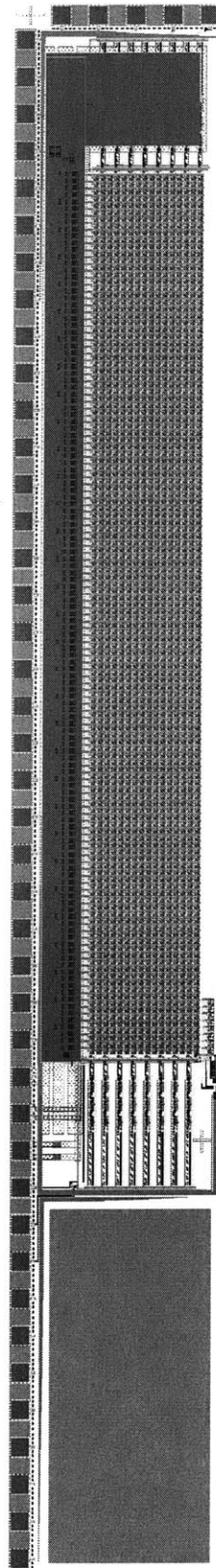


Figure 3-22: Chip layout

Chapter 4

Characterization

The chip was fabricated in TSMC's 0.35 micron process. Samples were subject to a variety of tests to measure performance.

4.1 Test Setup

The basic setup involved a chip mounted in a 180 pin package. The large package was necessary because of the pad arrangement on the chip. Due to OLED post-processing requirements, only two sides of the chip were available to have pads. In particular, one side of the chip contains more than 40 pads. Since bond pads are situated uniformly around a package, a package with 40 pads on one side was needed. Thus, the 180 pin package.

The package mounts vertically on a PCB test board. The PCB generates certain signals and provides connections for others. All the power, current and voltage references are generated on the test board although they can be provided externally as well. Clock signals for controlling the switched capacitor networks are also generated on the board, although the frequency can be determined externally.

Separate connections are provided for the analog input voltages and special sensor output voltages that are provided for testing purposes. The digital control pins are controlled by Labview running on a Windows platform connected to the test board through a digital I/O card.

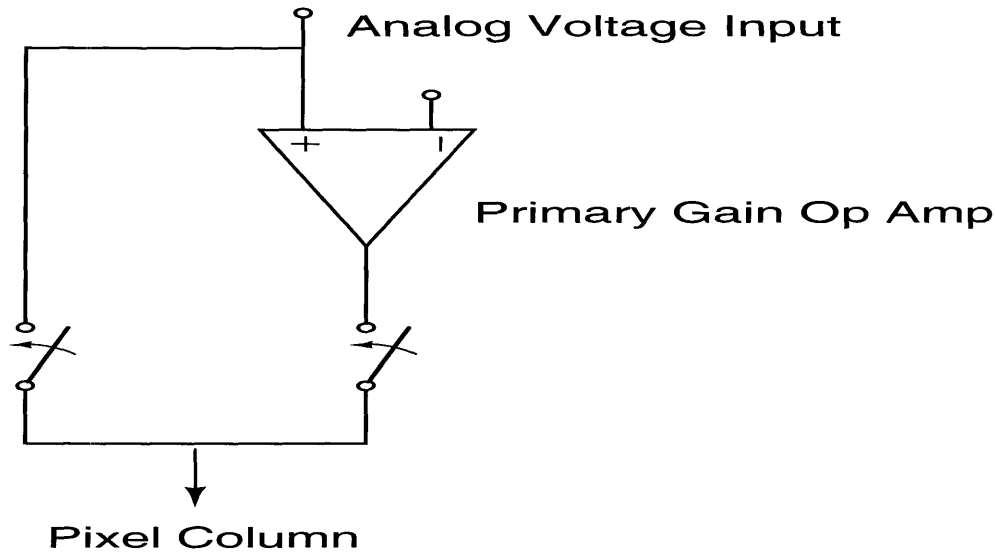


Figure 4-1: Bypassing the primary drive op-amp to drive the pixel column directly

4.2 Characterization

Since it is important to discriminate between functionality in the silicon chip and the OLEDs themselves, the testing is divided into two stages. The first takes place before the OLEDs are deposited.

There are two important aspects of the chip that can be tested without the OLEDs. First, you can test that the pixel is properly driving the pad which will contact the OLEDs. And secondly, you can test that the sensor is responding to incident light as desired.

In the layout of the chip certain arrangements were made in order to facilitate testing. First, it is possible to bypass the primary drive op-amp and drive the pixel column input directly from the analog input to the chip. This is made possible by a switch controlled by a digital signal as shown in Figure 4-1. When the chip is powered up, the address for a particular row is asserted through Labview. Also, the OLED signal is set so that the PFET transimpedance amplifier can be driven for that row. Then, under microscope, a corresponding pixel pad is delicately probed. By connecting a small resistor between the probe and ground, and varying the voltage input, one can test the current supplied by the transimpedance amplifier as a function

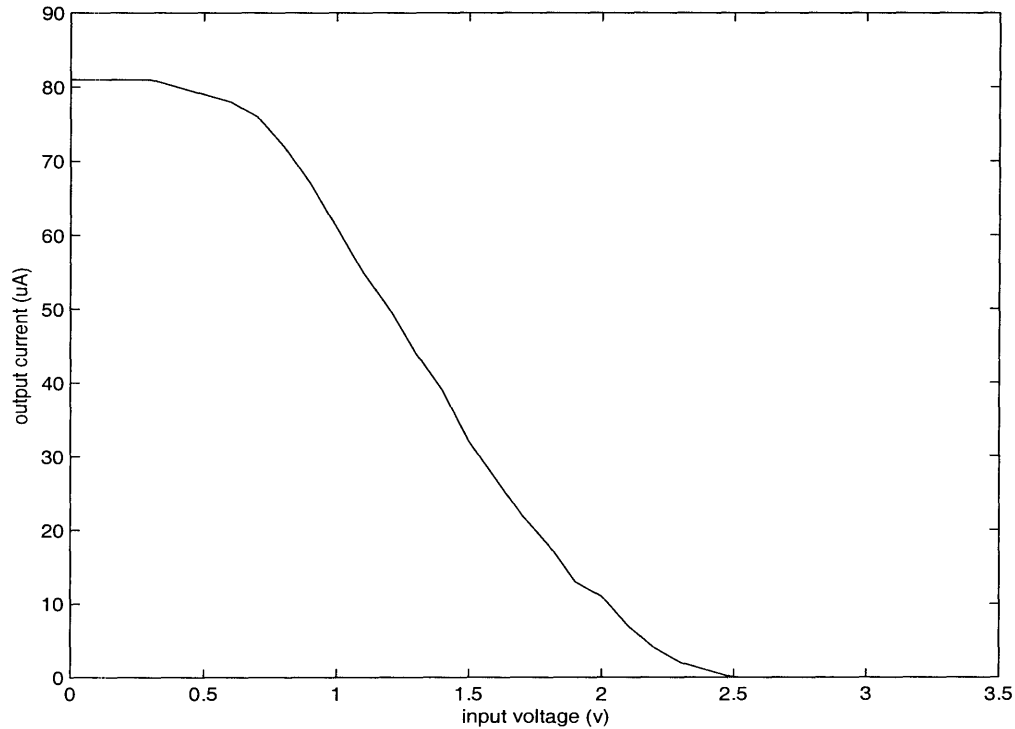


Figure 4-2: Test data from probing the pixel pad directly

of input voltage. By testing different addresses, it is possible to verify that the row addressing scheme is functioning properly. Tests were conducted on two separate rows. It was found that the addressing scheme worked as expected. Results closely matched HPICE simulations for a single PFET transistor. They are displayed in Figure 4-2.

The second significant testing arrangement made in layout was to provide an output pad for two of the pixel columns. Instead of just driving the feedback loop, the output of the source follower from the pixel is also connected to an output pad as shown in Figure 4-3. By providing a light source to the chip, it is possible to measure the sensor response.

Three neutral density filters were chosen for the test. A magnified light was directed on the surface of the chip through a series of filter arrangements. A fixed address address was asserted while the SENSOR signal was set so that the pixel output was available. The RESET signal was controlled via a square wave. A oscilloscope

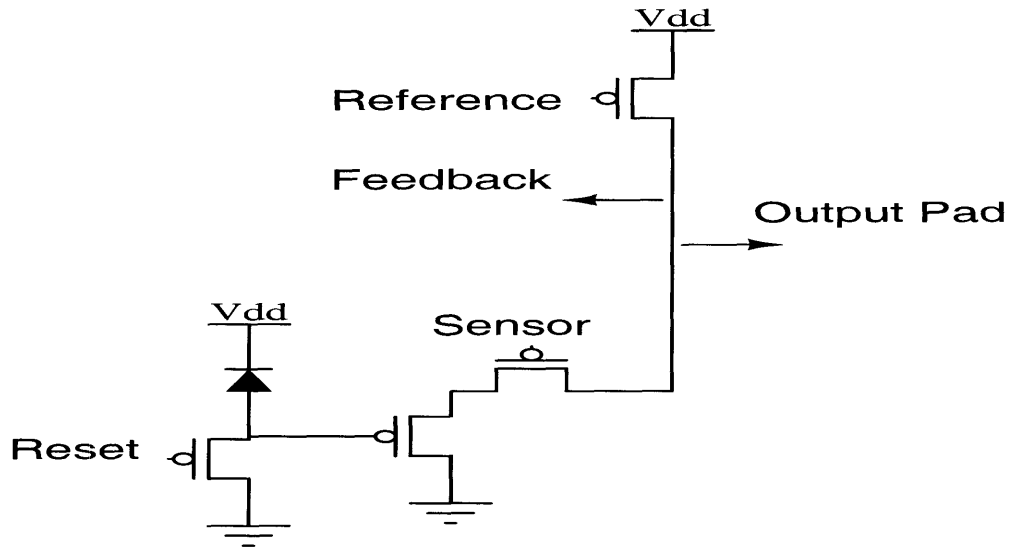


Figure 4-3: Probing the output of the sensor directly

was connected to the output from the pixel and set to trigger on the RESET signal. The slope of the output from the sensor is measured and compared to the incident light intensity. The results are shown in Figure 4-4. The lack of additional filters prevents the measuring of additional data points. But it is clear that the photodiode saturates at high current and is linear over a considerable region below that. At lower light levels, the response flattens off again. This may be because ambient light is leaking onto the sensor unexpectedly.

It turned out that the OLED deposition process was not fully developed at the time this thesis was written. Tests conducted after the OLEDs are deposited should verify the feasibility of the optical feedback technique.

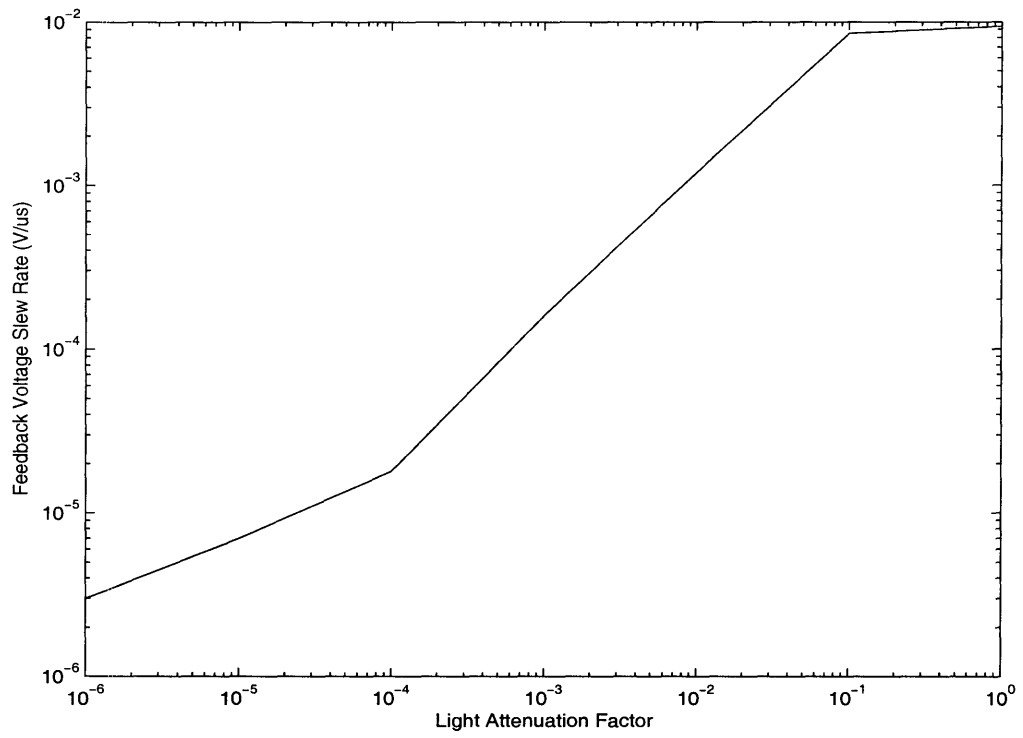


Figure 4-4: Sensor output voltage measured against incident light intensity

Chapter 5

Conclusion

A design for using optical feedback to drive an OLED display was proposed and implemented. The design was verified in simulation and testing of the sample has shown it to be operational. Further testing, after the OLED deposition process is fully developed and successful will provide final validation of the effectiveness of the technique and the functionality of the display.

With the right control signals, analog input and chip design, this technique can be extended to a larger display to generate images and even video. The principle of optical feedback is even more general. With the further development of organic materials processing, optical feedback could, in theory, be implemented with optical transistors and photodiodes.

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