UNIJUNCTION TRANSISTORS IN A RING COUNTER

by

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ABSTRACT

This thesis describes the design, construction, and operation of a ring counter using the unijunction transistor, a semiconductor switching device which exhibits negative resistance characteristics. The unijunction transistor and ring counters are described briefly; then the two are combined in the design of a working unit. Experimental results are presented verbally and graphically. An investigation into the maximum frequency capabilities of the counter completes the study.

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UNIJUNCTION TRANSISTORS IN A RING COUNTER

I. Introduction

The purpose of this thesis is to determine whether it is feasible to use unijunction transistors as binary elements in a ring counter. The goal is to reduce power consumption by replacing two standard silicon transistors with one unijunction transistor. This project involves design, construction, and testing of the counter.

Specifications for the counter were set by the requirements of the group under whose auspices this investigation is being conducted. For purposes of this investigation a five stage counter was designed and constructed. The counter operated satisfactorily up to a pulse repetition frequency of 80 kc. The counter operated at frequencies up to 95 kc., but the outputs became distorted and triggering was unreliable above 80 kc. Limitations inherent in the unijunction transistor prevented further extension of the frequency capabilities of the counter. The conclusion reached was that a ring counter with unijunction transistors at the present state of art is feasible but not for frequencies above 80 kc.

II.

A. The Unijunction Transistor

The unijunction transistor was chosen for this application because it replaces two conventional transistors as the active element of basic binary circuits. The resulting reduction of size, weight, and cost by elimination of components provides incentive for its use in binary circuits where small size and low power drain are important.

The unijunction transistor is a three terminal "device exhibiting open-circuit stable negative resistance characteristics."[1] It is constructed from a bar of doped N-type silicon to which are affixed two ohmic connections, Base 1 and Base 2. The IRE symbol for the unijunction transistor is shown in Figure 1 and a "representative"[2] circuit is shown in Figure 2.

When a voltage V_{BB} is applied across the base terminals of the unijunction transistor, a gradient of voltage is established across the semiconductor material which presents a resistance of about 10K. Since the emitter junction is located about 0.7 of the way between Base 1 and Base 2, about 0.7 of V_{BB} appears at the emitter junction. This voltage is called the peak point voltage (V_p). The fraction of V_{BB}

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[1] S. R. Brown and T. P. Sylvan, "A Collection of Articles on the Silicon Unijunction Transistor," reprinted from Electronic Design, (Nov. 15, 1957, Jan. 8, 1958, and Jan. 22, 1958), p. 3.

[2] Ibid., p. 3.

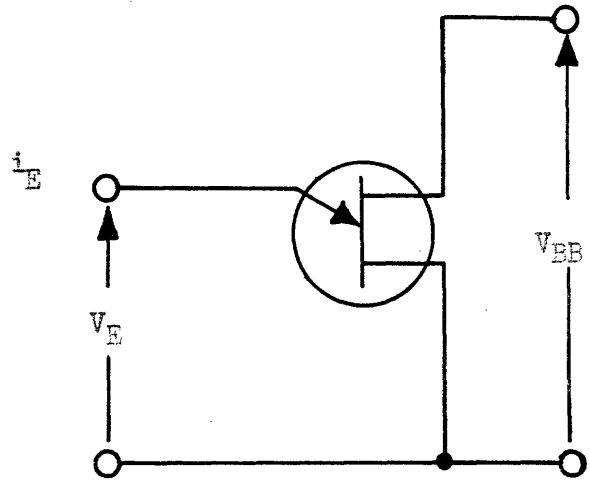

Figure 1. The IRE symbol for the unijunction transistor.

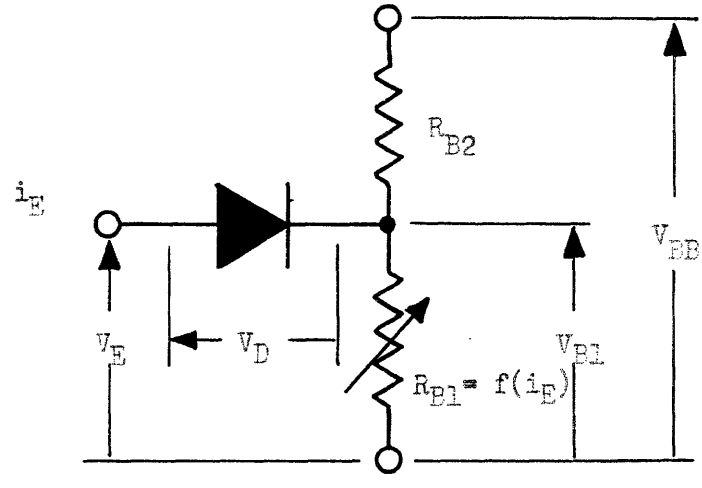

Figure 2. A representative circuit for the unijunction transistor.

appearing as V_P is denoted the intrinsic standoff ratio (η).

Negative resistance characteristics are obtained by modulating the conductivity of the N-type material between the emitter and Base 1. When the emitter junction is forward biased and holes are injected into the bar, the conductivity is greatly increased in the region where holes appear. If the action continues, the resistance decreases as more holes are fed into the bar and a negative resistance region occurs in the characteristic curve of the device (Figure 3).

We may now describe the three regions of interest on the emitter characteristic curve. The first is the cutoff region. In the cutoff region the emitter voltage is less than the peak point voltage which is determined by the ratio $\frac{V_P}{V_{BB}} = \eta$. Thus the emitter junction is back biased and only a very small leakage current flows in the emitter. As the emitter voltage is raised to the peak point voltage V_P, the emitter junction becomes forward biased and conducts. We now enter the negative resistance region of the unijunction. As the number of minority carriers in the emitter to Base 1 region increases, the resistance decreases. This action continues regeneratively until the region between emitter and Base 1 becomes saturated with minority carriers and the emitter current increases to a value corresponding to the valley point of the characteristic curve. Here the emitter voltage is V_V. We now enter the saturation region of the emitter characteristic. In saturation the emitter to Base 1 region

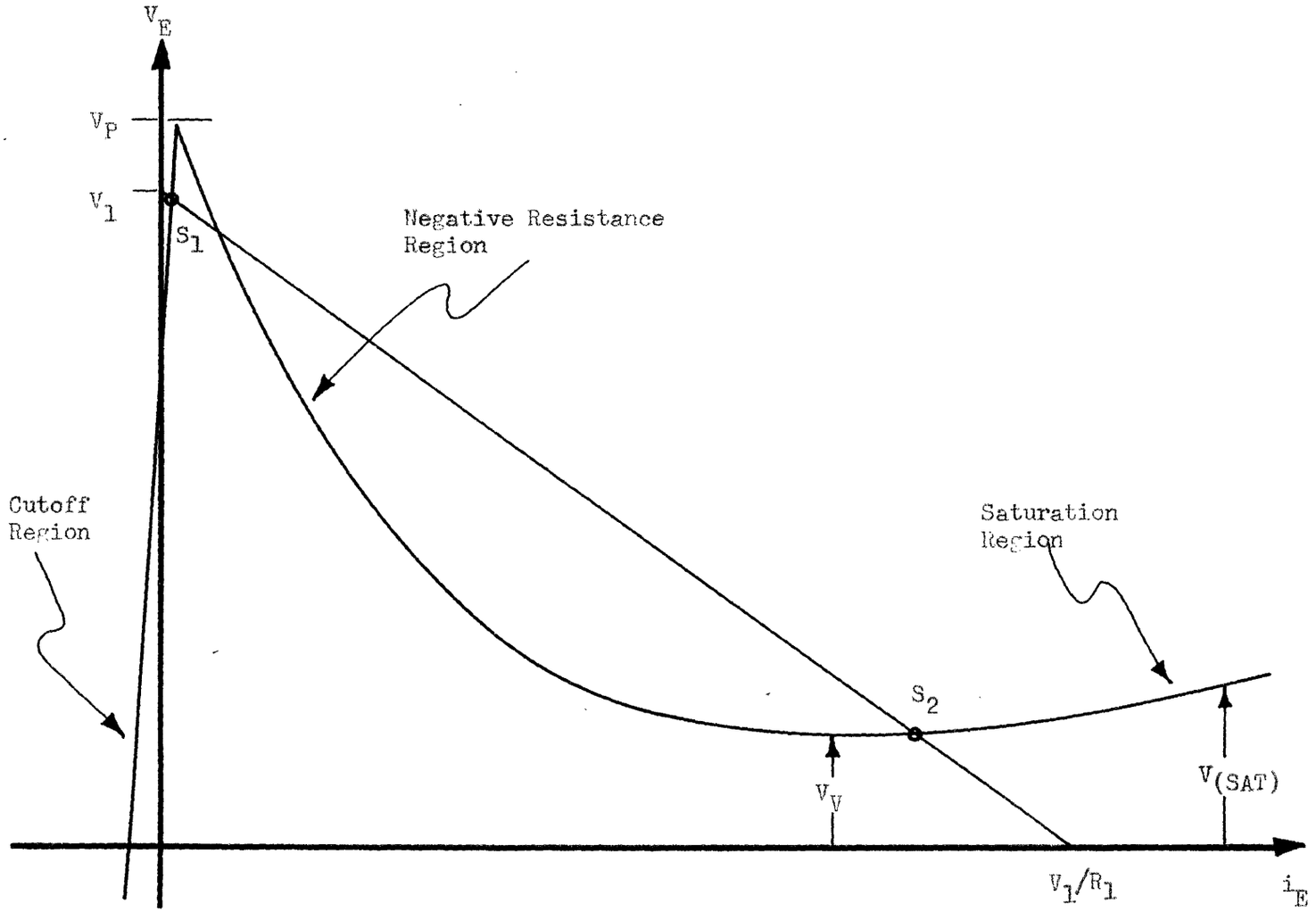

Figure 3. The characteristic curve for the unijunction transistor.

is saturated with minority carriers. Current is high and the resistance is between 5 and 40 ohms.

The cutoff region may be called the "OFF" state of the unijunction and the saturation region the "ON" state. Thus the unijunction is a basic binary element and may be used in applications such as counting.

B. Ring Counters

"Counting is a logical extension of frequency division."[3] While frequency division applies to periodic pulse waveforms, counting may be used with non-periodic pulse waveforms.

Counting pulses, dividing frequency, measurement of time, speed, or frequency, generation of complex pulses, and sequential gating are among the uses of counters.

The basic building block of a ring counter is a binary element or flip-flop. Any active element which can provide an "OFF" and "ON" state may be used in a ring counter. A ring counter is composed of a closed ring of binary elements as indicated in Figure 4.[4] Trigger pulses are applied to all stages simultaneously, but the units are interrelated so that an element will go "ON" only if the element preceeding it is

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[3] Chance et al, Waveforms, Radiation Laboratory Series, No. 19, (New York: McGraw-Hill, 1949), pp. 602-614.

[4] Millman and Taub, Pulse and Digital Circuits, (New York: McGraw-Hill Electrical and Electronic Engineering Series, 1956), Chapter 11.

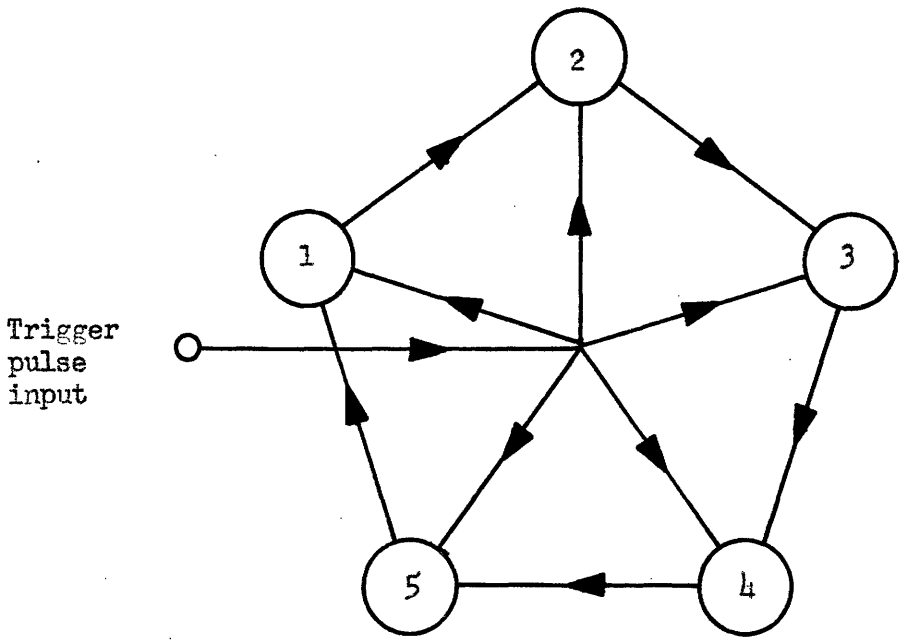


Figure 4. Ring counter block diagram.

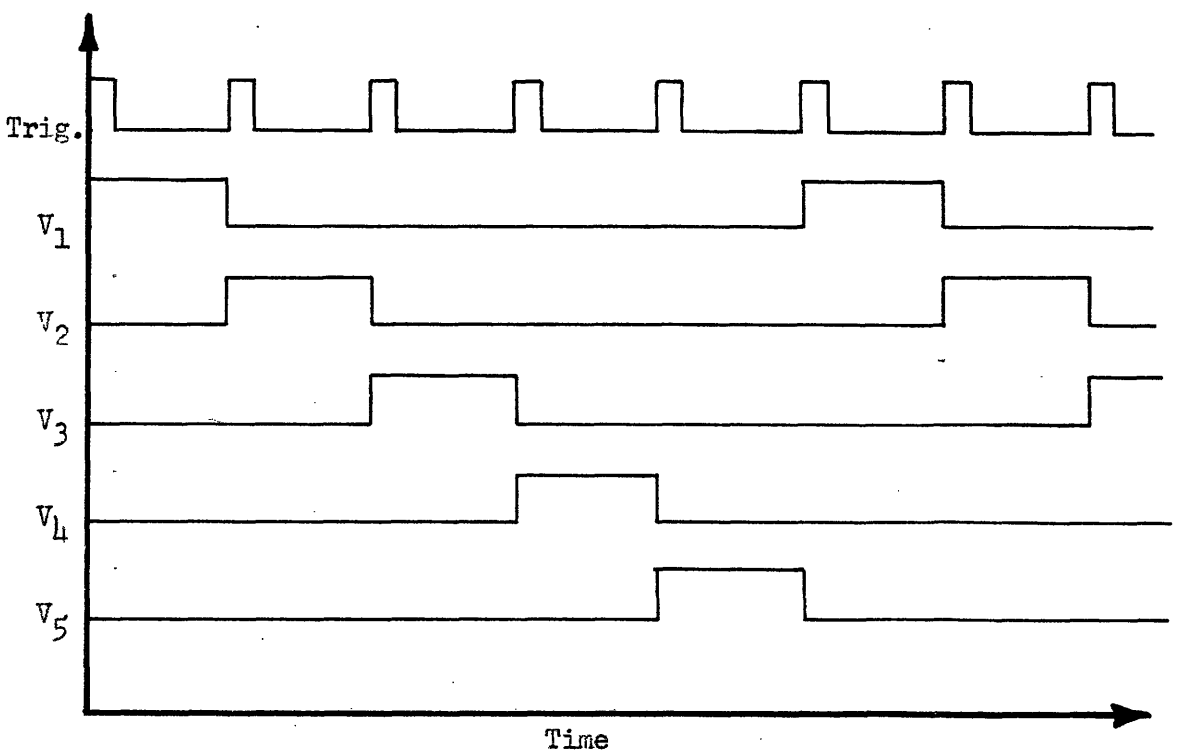


Figure 5. Trigger pulse and output voltages of the ring counter (Figure 4.) for the sequential gating application.

"ON." The counter may be designed so that only one stage is "ON" at a time. Each input pulse advances the "ON" state one more stage around the ring. Outputs may be taken at each of the stages for sequential gating or at one stage for frequency division.

One of the important uses of a ring counter is the sequential gating function illustrated in Figure 5. The output levels obtained at each stage may be used in gating and time coincidence circuits.

In summary, the requirements for a ring counter are:

1. All stages must be identical.
2. All stages must be triggered simultaneously in parallel.
3. The "ON" stage must advance one stage around the ring at each trigger pulse.
4. There must be a provision for initially turning "ON" one stage.
5. The counter must provide voltage level outputs at each stage.

The following section describes the design of a counter to meet these requirements.

III. Design

Since a ring counter is composed of bistable units, we shall first examine the basic unijunction bistable stage. From this basic circuit we shall obtain the basic counter stage and then proceed to the counter as a whole.

Basic Bistable Circuit

The basic bistable circuit is shown in Figure 6. The peak point voltage is established by the voltage V_2. The combination of V_1 and R_1 prescribes the load line shown on the emitter characteristics in Figure 3. This load line intersects the characteristic curve in two stable operating points S_1 and S_2. These define the two stable states of the basic bistable unit. S_1 lies below V_P in the cutoff region where the emitter junction is back biased and not conducting, while S_2 lies to the right of the valley point in the saturation region where the emitter is conducting.

In the counter the basic stage is triggered by applying a pulse at the emitter of sufficient magnitude to raise the load line momentarily above the peak point voltage. Regenerative action occurs, the operating point traverses the negative resistance region and settles in saturation at the second stable point, S_2. To switch the binary back to its "OFF" state (S_1), we interrupt the supply V_1 momentarily. The emitter current drops to zero and when V_1 is re-applied, the binary is stable at S_1 -- since V_1 does not exceed the peak point voltage.

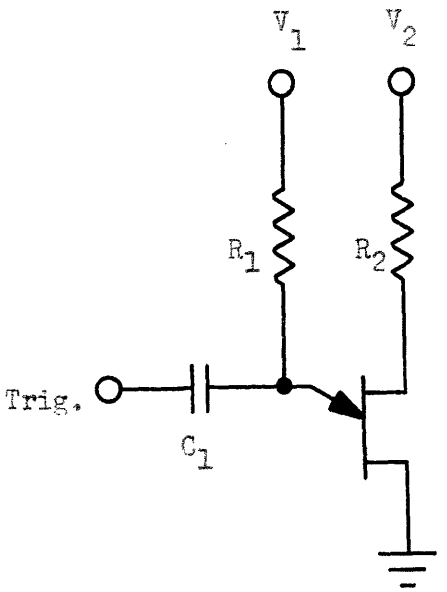


Figure 6. Basic bi-stable stage.

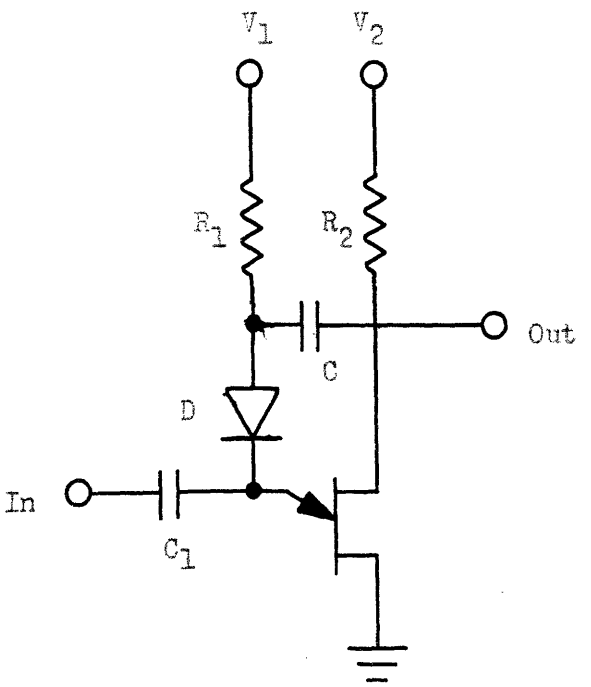


Figure 7. Basic counter stage.

Basic Counter Stage

The circuit for the basic counter stage (Figure 7) modifies the basic bistable circuit by the addition of only two components, the capacitor (C) and the diode (D). The capacitor feeds forward a pulse to trigger the next stage in the ring and the diode prevents this pulse from being fed forward more than one stage.

In the "OFF" stage $V_E = V_1$, but in the "ON" state V_E drops to a value slightly greater than V_V. A corresponding voltage swing occurs at the output (Base 2). In the "OFF" state V_{B2} is slightly less than V_2 due to the voltage divider effect. In the "ON" state more current is drawn from the V_2 supply and the drop across R_2 increases. V_{B2} falls by the amount of this drop.

Triggering is accomplished in the basic counter stage by opening the ground lead from Base 1 momentarily. The mechanism of triggering will be explained more thoroughly below under "Sequence of Operation."

Complete Counter Circuit

The completed counter with trigger circuit and "initial "ON" circuit" is shown in Figure 8.

A switching transistor replaces the switch in the Base 1 to ground lead for triggering. This transistor is biased in saturation so that it looks like a short circuit until a trigger pulse is applied. For the duration of each trigger pulse, the transistor is cut off and looks like an open circuit.

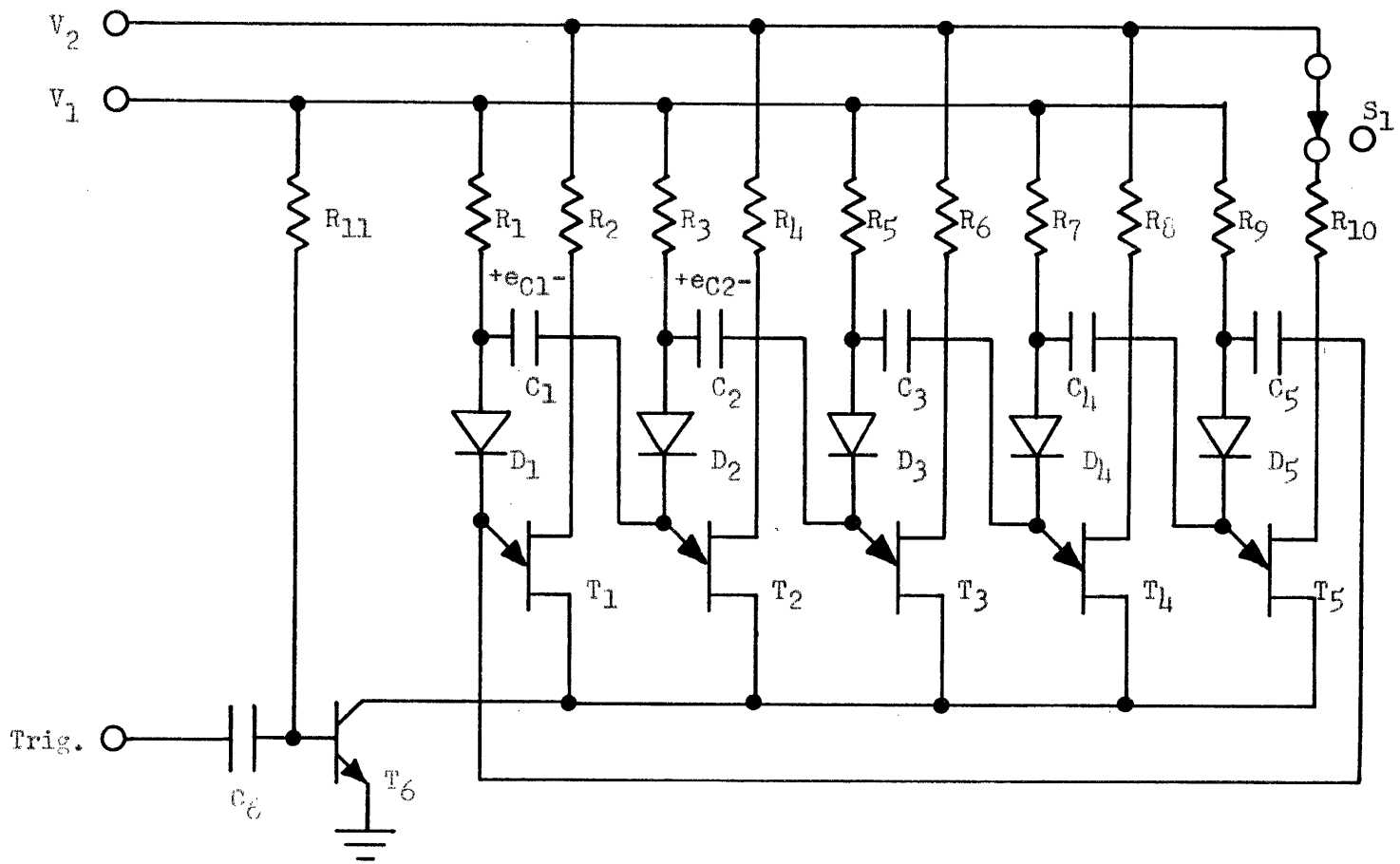


Figure 8. The complete ring counter circuit.

Parameter values:

V_1 -- +10.5 volts D.C.

V_2 -- +22.5 volts D.C.

T_1-T_5 -- 2N492 unijunction

T_6 -- 2N551

R_1-R_{10} -- 470 ohms

R_{11} -- 10K

C_1-C_5 -- .001 microfarad

C_6 -- 2 microfarads

D_1-D_6 -- 60 volts reverse

The switch S_1 may be opened momentarily when operation begins to insure that one stage is initially "ON."

Note the similarity between the completed counter schematic and the block diagram shown in Figure 4. The capacitors are the links between stages and Base 1 is the common trigger point. Outputs are taken at Base 2 of each stage.

Sequence of Operation

Before applying a trigger pulse we must recognize the initial conditions. Suppose stage 2 is "ON" and all other stages are "OFF." Then the voltage at the emitter of T_2 is about 3 volts (slightly greater than V_V), while the voltage at all other emitters is the supply V_1 = 10 volts. The voltage differences between emitters produce static charges on the capacitors C_1 and C_2:

$$e_{C1} = +7 \text{ volts.}$$

$$e_{C2} = -7 \text{ volts.}$$

The following sequence of events describes the operation of the counter as the count advances one stage around the ring. This can be made to occur within about 10 microseconds.

When a trigger pulse is applied, T_6 switches from saturation into cutoff and effectively open-circuits the ground lead from Base 1. In T_2 the emitter current goes to zero and the emitter voltage rises to V_1. Since D_2 is forward biased, C_1 discharges through R_1, R_3, and D_2. C_2 does not discharge because its static voltage is negative so that D_3 is back

biased. The static voltage on C_2 appears in series with V_1 and R_3 producing 10 volts plus 7 volts = 17 volts at the emitter of T_3. Now the trigger pulse goes "OFF" causing T_6 to saturate. Current begins to flow in the emitter of T_3 because 17 volts is sufficient to exceed the peak point voltage and switch "ON" T_3. T_2 remains "OFF" because V_1 is not sufficent to exceed V_P. At each trigger pulse the sequence repeats itself and the count advances one stage around the ring.

The voltage level at Base 2 of any stage drops for the duration of each "ON" period. These output level changes may be used in the sequential gating application mentioned earlier. This counter meets all the requirements specified in Section II. B.

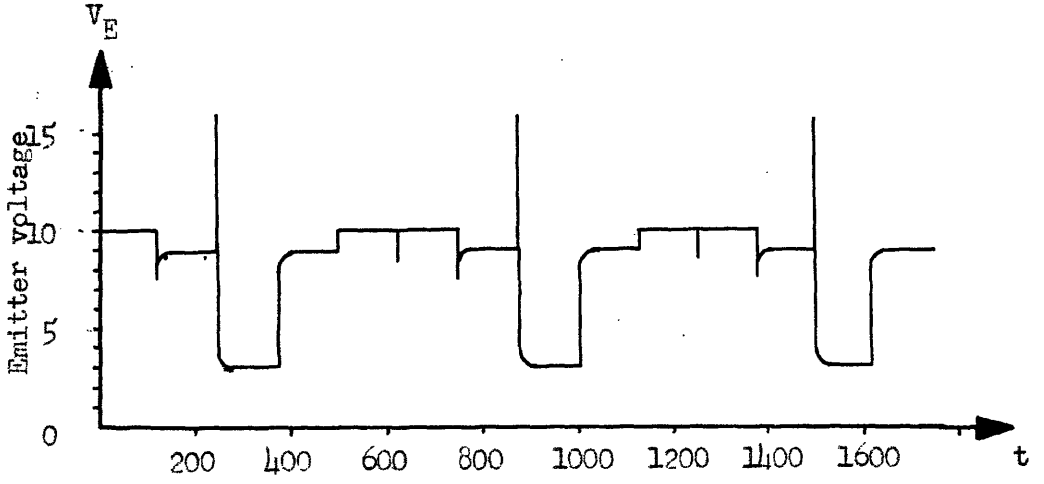
IV. Experimental Results

Operation

The circuit used in the completed counter is shown in Figure 8 with the parameter values as indicated. These values are based on design factors and calculations given in the Appendix. Final values used were those which allowed maximum frequency of operation.

Sketches from photographs of the emitter and Base 2 voltages at 8 kc. and 80 kc. are shown in Figures 9 and 10. The occurance of trigger pulses and voltage level changes are shown clearly at 8 kc. The 5 volt, 4 microsecond trigger pulses appear at Base 2 as positive spikes 125 microseconds apart. The voltage level at the emitter while the stage is "OFF" is 10 volts. In the "ON" state, which occurs once every 625 microseconds, the level drops to 3 volts. The 17 volt pulse fed forward from the previous stage appears just before the emitter voltage level drops to its "ON" value. The output voltage at Base 2 is a much cleaner waveform since it is not affected by variations in the static charges on the capacitors. In the "OFF" state the level at Base 2 is 21 volts, while in the "ON" state it drops to 13 volts. The output available for gating is an 8 volt swing from the "OFF" to the "ON" state.

Rise and fall times are shown more clearly at 80 kc. (Figure 10). At this frequency the duration of the trigger pulse becomes an appreciable fraction of the pulse interval



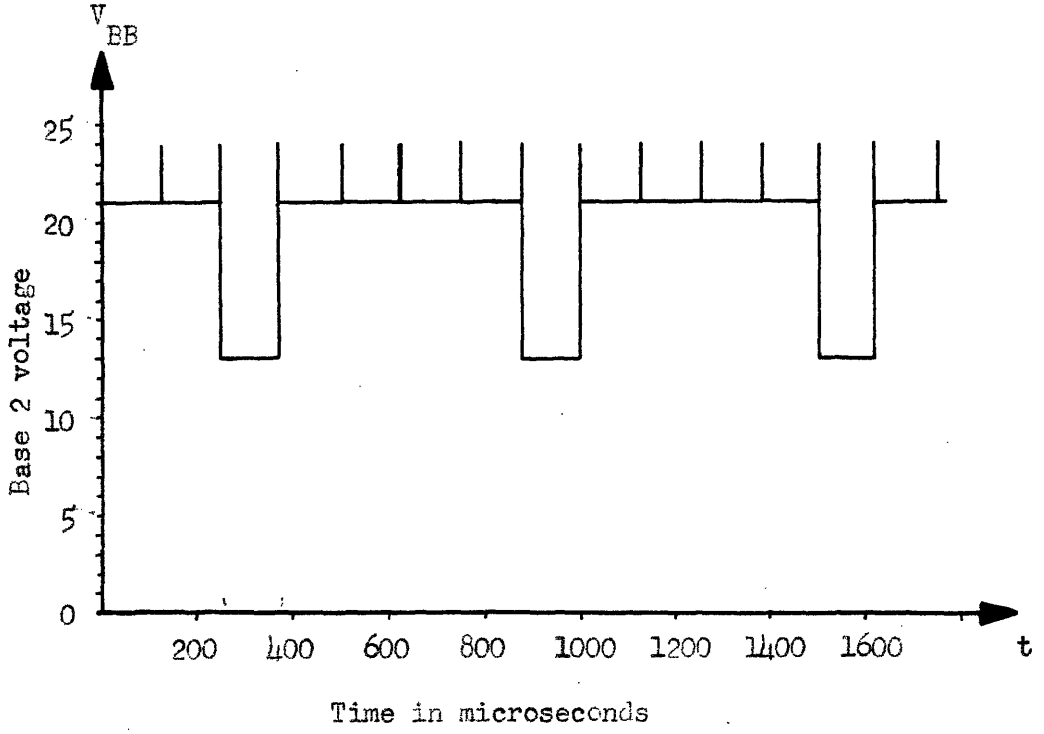
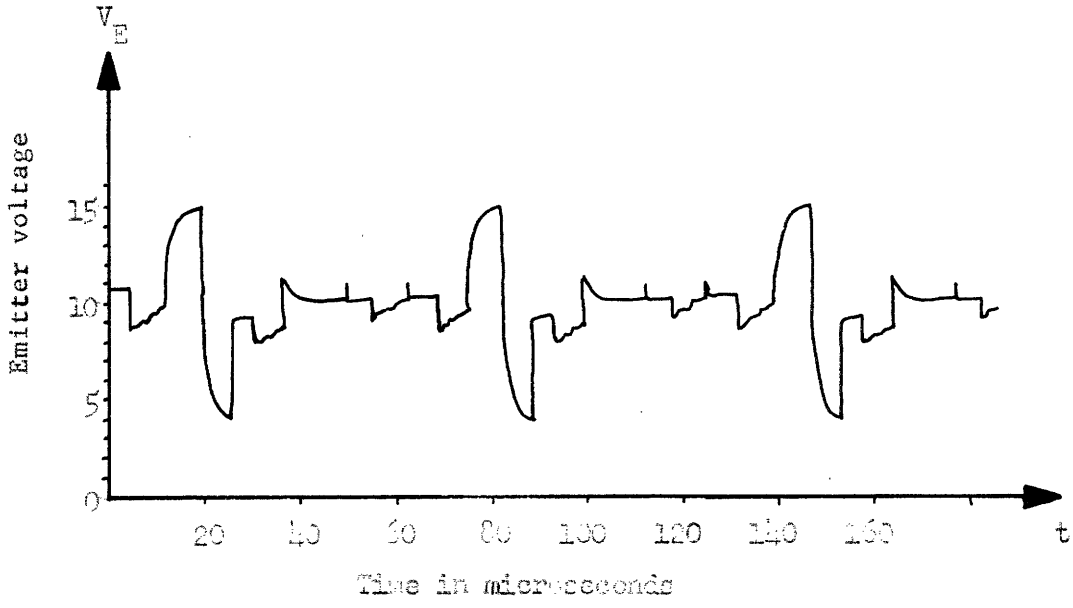


Figure 9. Sketches of emitter and Base 2 voltage waveforms at 8kc.



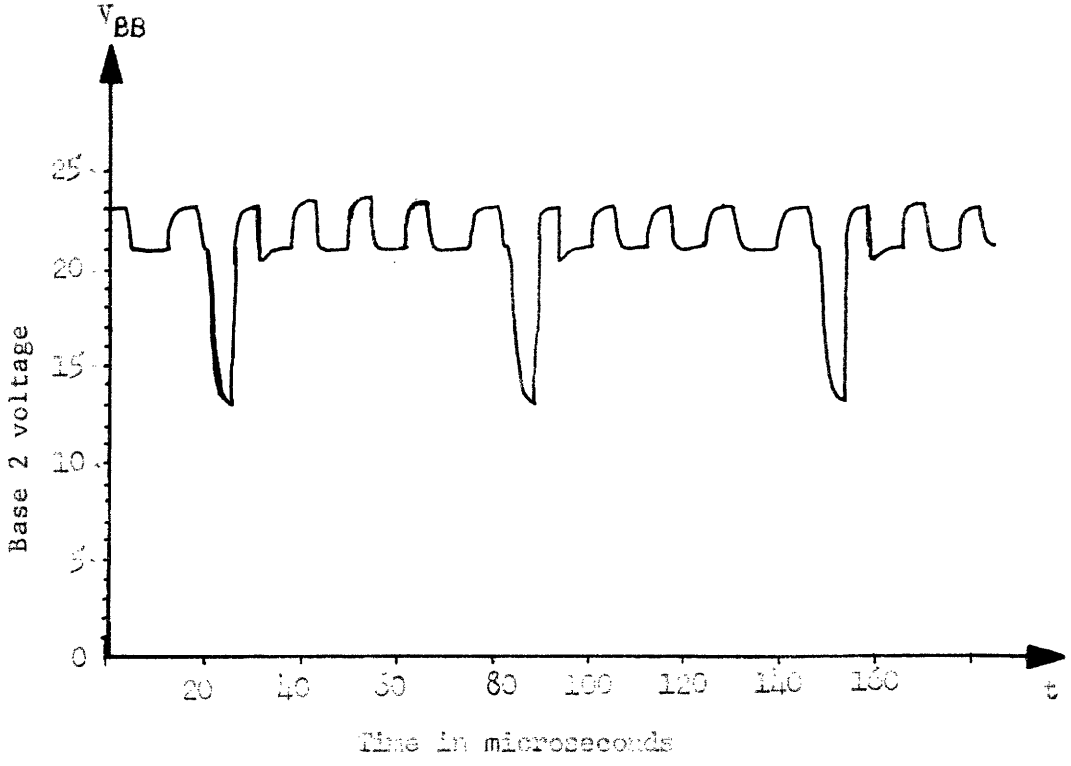


Figure 10. Sketches of emitter and Base 2 voltage waveforms at 80 kc.

and the pulses appear at Base 2 as small square pulses instead of spikes as observed at the lower frequency. The 17 volt pulse from the previous stage appears clearly at the emitter just before the voltage level drops to 3 volts during the "ON" state. The fall of the emitter voltage is shown as well as the simultaneous fall of the voltage level at Base 2. The fall time is approximately 6 microseconds.

Maximum Frequency

By decreasing the capacitor values to a minimum value of 4700 micromicrofarads and decreasing the pulse duration to 3 microseconds, the counter was made to operate for short periods of time at 95 kc. Operation at this frequency was unreliable since small disturbances interrupted operation and more than one stage switched "ON" at a time. For reliable operation, 80 kc. was taken as a maximum. The pulse duration should not be less than 4 microseconds and the capacitor values not much less than .001 microfarads for reliability.

The triggering method which allowed the highest frequency of operation is shown in the overall circuit diagram. Triggering by interrupting the emitter supply voltage and triggering across a small resistor in the Base 1 lead were tried but were not as successful as the method shown.

Equipment List

Wide Range Oscillator	HP-200CD
Pulse Generator	General Radio 1391A
Voltmeter	RCA WC-87A
Oscilloscopes	Tektronix 535 and 551

V. Frequency Limitations

This section is devoted to a description of the frequency limitations of the unijunction transistor ring counter. Since high frequencies are of interest in the sequential gating application of the counter, a knowledge of its high frequency limitations is useful and therefore presented here.

There are two limiting factors which combine to establish a maximum theoretical frequency of operation for the counter. These are the recovery time of the emitter peak point voltage and the fall time from the peak point through the regenerative region to the saturation state.

Recovery Time[5]

In the "ON" state minority carriers saturate the region between the emitter and Base 1 so that the conductivity is very high. In the "OFF" state minority carriers are few and the conductivity is low. The peak point voltage is defined as that portion of V_{BB} appearing across the emitter to Base 1 region in the "OFF" state. When switching from the "ON" state to the "OFF" state, a finite time is required for the saturation carriers to recombine or drift out of the region before the peak point voltage can recover to its steady state value V_{P0}. A plot of the ratio $\frac{V_P}{V_{P0}}$ versis recovery time is shown in Figure 11.

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[5] Notes on the Application of the Silicon Unijunction Transistor, ECG-380, General Electric Company, (February, 1959), pp. 62-64.

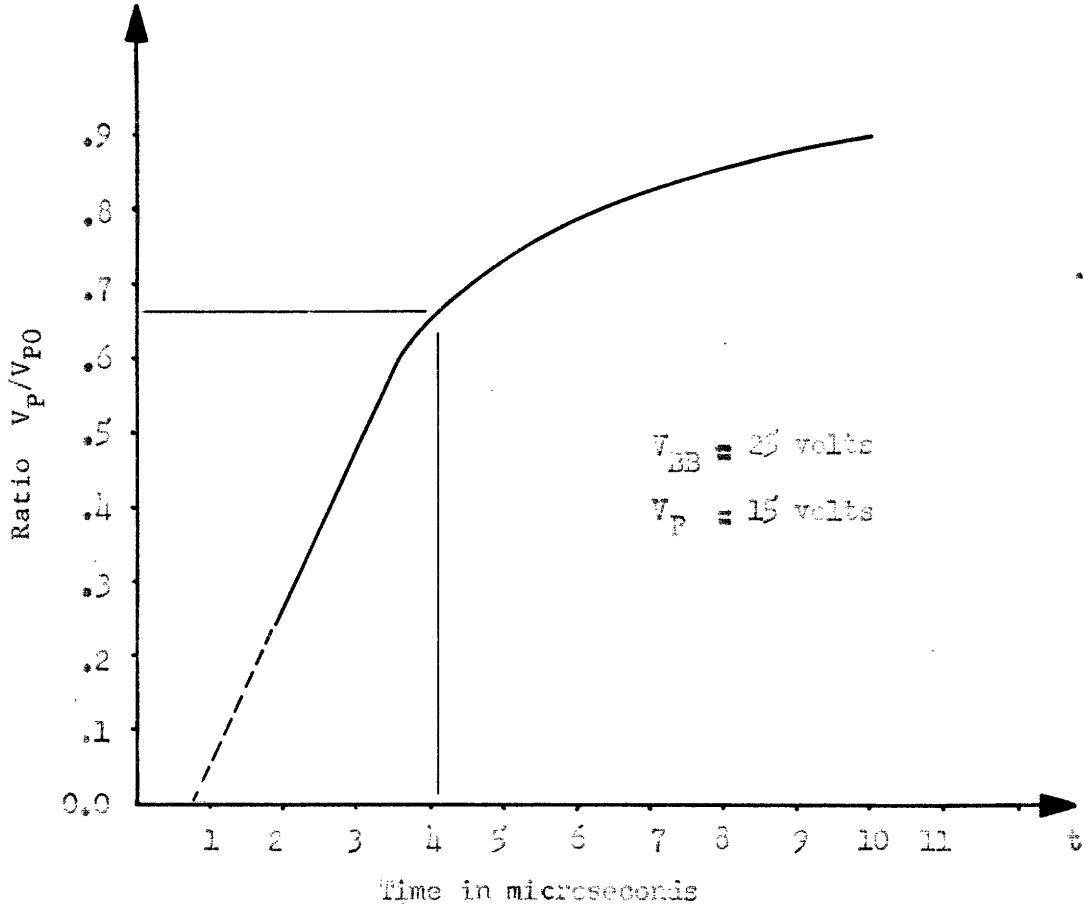

Figure 11. Recovery characteristic of peak point emitter voltage.

In the counter the peak point voltage must recover during the trigger pulse, otherwise re-applying the 10 volt emitter supply will cause the emitter to conduct before recovery is complete, and the unijunction will not turn "OFF." This would result in two stages being "ON" at once in the counter. To prevent this "double counting" the trigger pulse duration must be greater than the value at which 10 volts will retrigger the unijunction. From Figure 11 this value is approximately 4 microseconds.

Fall Time[6]

The second limitation to the switching speed of the unijunction is the mechanism by which conduction is established after exceeding the peak point voltage. A finite time is required for regenerative action to drive the unijunction from cutoff to saturation. When the emitter diode becomes forward biased, holes are injected into the N-type base material at the emitter junction. Since space charge neutrality must be maintained in the semiconductor material, electrons enter at the Base 1 terminal. The charges must build up slowly to maintain charge neutrality so that the regenerative action occurs in a time much greater than the transit time of individual carriers. This time is called the "fall time" and

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[6] Ibid., p. 8.

is given by "the empirical equation:

$$t_f \cong (2 + 5C_T)V_E(SAT)$$

where t_f is in microseconds, C_T is in microfarads, and $V_E(SAT)$ is in volts."[7] C_T, the external capacity from emitter to Base 1 is very small in the ring counter and may be neglected in comparison to the D.C. effect. We have:

$$t_f \cong 2V_E(SAT)$$

Since $V_E(SAT)$ is about 3 volts for the 2N492, the fall time is $t_f \cong 6$ microseconds.

Because the fall time occurs after the trigger pulse is over, the sum of the fall time and the minimum trigger pulse duration gives a figure which determines the maximum pulse repetition frequency for reliable operation of the counter:

$$T = t_f + t_r = 6 + 4 = 10 \text{ microseconds}$$

From this the maximum frequency of operation is:

$$f_{MAX} = \frac{1}{T} = 100 \text{ kc.}$$

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[7] Notes on the Application..., op. cit., p. 40.

VI. Conclusion

A ring counter using unijunction transistors was designed, constructed, and tested. This counter achieved a savings in component parts by elimination of one active element and its associated circuitry from each stage. The circuit is more economical because it requires a very small power drain compared to conventional counters.

Theoretical considerations indicated a maximum frequency of operation of 100 kc. because of limitations inherent in the unijunction. The maximum frequency attained was 95 kc., but reliability was good only to 80 kc. The M.I.T. Instrumentation Laboratory required a higher frequency for their application. The conclusion reached was that a ring counter using unijunction transistors is feasible but not for frequencies greater than 80 kc.

The possibility of interchanging the Base 1 and Base 2 leads and modifying the associated circuitry as necessary should be investigated further since it may lead to higher frequencies of operation.

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Appendix--Calculations

A. Calculation of Peak Point Voltage V_P

The peak point voltage is the portion of V_{BB} appearing across R_{B1} (Figure 2) with the emitter open circuited plus the diode voltage V_D.

$$V_P = V_D + V_{BB}$$

At room temperature $V_D = 0.7$ volts. The voltage V_2 which establishes V_{BB} was chosen for convenience at $V_2 = 22.5$ volts. V_{BB} is given by the voltage divider effect of R_2 and R_{BB}, where $V_{BB} \cong 21$ volts. From the 2N492 unijunction transistor specifications, maximum and minimum values of η are 0.68 and 0.56 respectively while maximum and minimum values of R_{BBO} are 9.1K and 6.2K. From these figures we can calculate upper and lower limits for V_P.

Maximum: $V_P = V_D + \eta V_{BB}$

$$= V_D + \eta \frac{R_{BB}}{R_{BB} + R_2} V_2$$

$$= 0.7 + \frac{(.68)(9.1)(22.5)}{9.1 + .47}$$

$$V_P = 15.3 \text{ volts (Maximum)}$$

Minimum: $V_P = 0.7 + \frac{(.56)(6.2)(22.5)}{6.2 + .47}$

$$= 12.4 \text{ volts (Minimum)}$$

On the basis of these criterion V_1 may be any value below 12.4 volts. For convenience V_1 = 10.5 volts was chosen.

B. Calculation of Resistor R_1 (Figure 7)

The resistor R_1 together with the source voltage V_1 determine the emitter load line. This load line must intersect the characteristic curve just below the peak point voltage in cutoff and slightly to the right of the valley point in saturation. Since recovery time increases with amount of saturation current just before turnoff, the intersection point S_2 (Figure 3) should be as close to the valley point as possible.

Since current at the valley point is about 20 ma.,

$$\frac{V_1}{R_1} > 20 \text{ ma.}$$

and,

$$R_1(MAX) = \frac{10.5}{20} = .525K$$

or,

$$R_1 \leq 525 \text{ ohms.}$$

The minimum value of R_1 is given by the emitter current limitation of 50 ma. D.C. Thus,

$$R_1(MIN) = \frac{10.5}{50} = .21K$$

or,

$$R_1 > 210 \text{ ohms.}$$

For fast switching time and assurance of stability (intersection to the right of valley point) R_1 was chosen as R_1 = 470 ohms.

C. Calculation of R_2

R_2 must be large enough to develop an appreciable output voltage swing, yet it must be small enough that the interbase voltage is not reduced by the voltage divider effect. A value of R_2 which was found to satisfy the above conditions was $R_2 = 470$ ohms. The voltage swing is given by

$$V_{B2} \text{ (OFF state)} - V_{B2} \text{ (ON state)} = V_{B2} \text{ (swing)}$$

Since $$V_{B2}(\text{OFF}) \cong \frac{(7.5\text{K})(22.5)}{7.5\text{K} + .5\text{K}} = 21 \text{ volts}$$

and $$V_{B2}(\text{ON}) \cong \frac{(1\text{K})(22.5)}{1\text{K} + .5\text{K}} = 15 \text{ volts}$$

then $$V_{B2}(\text{swing}) \cong 6 \text{ volts}$$

D. Calculation of R_{11}

The switching transistor T_6 is biased in saturation until a trigger pulse drives it into cutoff. T_6 operates as a switch, normally short circuited, allowing current to flow to ground from Base 1. R_{11} determines the current which flows in the collector and emitter of T_6. Since steady state current to ground through Base 1 is about 25 ma., R_{11} must allow at least this current to flow. For the 2N551 the base current required is about 1 ma.

$$R_{11} = \frac{V_1}{i_B} = \frac{10.5 \text{ volts}}{1 \text{ ma.}} = 10\text{K}.$$

$$R_{11} = 10\text{K}$$

E. Calculation of C_1

C_1 must be small enough that its discharge time through R_1, R_3, and D_2 is less than the duration of the trigger pulse. If discharge is not complete when the trigger pulse ends, the diode D_2 becomes reverse biased and C_1 will hold its charge. If the charge retained by C_1 is large enough, it will prevent triggering of that stage in the next cycle of operation.

$$3\tau = 3(R_1 + R_3)C_1 < \delta \text{ (trigger pulse duration)}$$

Taking δ as 4 microseconds, we have:

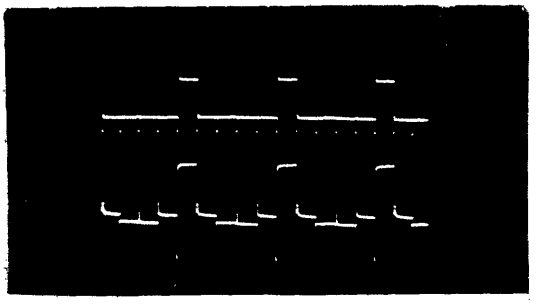
$$C_1 \leq \frac{\delta}{3(R_1 + R_3)}$$

$$\leq \frac{4}{3(470 + 470)}$$

$$\leq .002 \text{ microfarads}$$

The value which gave best results was:

$$C_1 = .001 \text{ microfarads.}$$



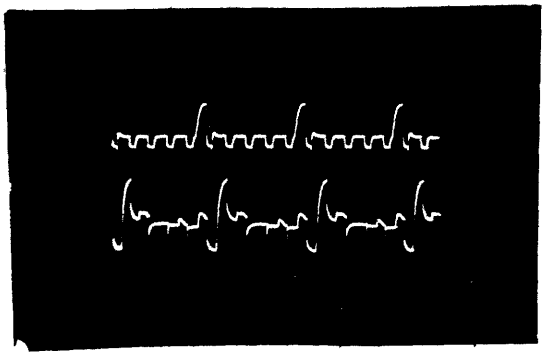
1.

2.

Figure A-1 Counter Output -- 8kc.

1. At Base 2.

2. At Emitter



1.

2.

Figure A-2 Counter Output -- 80kc.

1. At Base 2

2. At Emitter